An Efficient Inductance Modeling for On-Chip Interconnects

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Outline

- Importance of on-chip inductance
- Efficient inductance model
- Applications and conclusions
On-Chip Inductance

- Interconnect impedance is more than resistance
  - \( Z = R + j\omega L \)
  - \( \omega \) is decided not by the clock frequency, but by clock edge
    - \( \omega \propto 1/t_r \)

- On-chip inductance must be considered when \( \omega L \) is comparable to \( R \)
  - wide wires \( \Rightarrow \) low resistance
  - fast clock edge \( \Rightarrow \) high \( \omega \)

Candidates for On-Chip Inductance

- Wide and fast clock trees
  - delay (skew) will be different under RLC and RC models
  - neighboring signals can be disturbed due to large \( di/dt \)

- Wide (>1um) and fast edge rate (~100ps) buses
  - RC model under-estimates crosstalk

- Power grids, especially > 1um
  - higher current and more high-frequency components
Control of On-Chip Inductance

- Coplanar waveguide is often used for clock trees
  - closer and cleaner current return for clock synthesis

- Shielding traces may be inserted to reduce crosstalk for buses
  - shielding traces are connected to either VDD or Ground
Problem Formulation

- **Given:** a block of N traces
  - Two edge traces are AC-grounded, the rest are signal traces

- **Find:** RLC model for the block
  - considering process variation
  - efficient enough for **iterative** layout and simulation

Previous Works

- **Field solver is too expensive to be used**

- **Table-based approach has been proposed**
  - 2.5D capacitance model [Cong-He-Kahng+, DAC’97]
    - Shipped with Cadence SE 5.0
  - Statistically-based RC model [Chang-Kanevsky - Nakagawa+, ICCD’97]
    - Used in Hewlett-Packard

- **An efficient inductance model is still missing**
Outline

- Importance of on-chip inductance
- Efficient inductance model
  - Loop inductance and partial inductance
  - Foundations to reduce problem size
  - Table-based inductance extraction
- Applications and future works

Definition of Loop Inductance

\[ L_y = \frac{\mu}{4\pi} \frac{1}{a_i} \frac{1}{I_j} \int \oint_{\text{loop}_{i}} \oint_{\text{loop}_{j}} \frac{1}{r_{ij}} dI_i dI_j da_i da_j \]
Loop Inductance for N Traces

- Assume edge traces are grounded
  - leads to 3x3 loop inductance matrix
- Inductance has a long range effect
  - e.g., non-negligible coupling between \( t_1 \) and \( t_3 \) with \( t_2 \) between them

<table>
<thead>
<tr>
<th>( T_{wL} )</th>
<th>( T_w )</th>
<th>( T_{wL} )</th>
<th>( T_w )</th>
<th>( T_{wR} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.73</td>
<td>1.15</td>
<td>0.53</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.15</td>
<td>1.94</td>
<td>1.24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.53</td>
<td>1.24</td>
<td>1.92</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table in Brute-Force Way is Expensive

- Self inductance has nine dimensions:
  - (n, length, location, \( T_{wL} \), \( T_{sL} \), \( T_w \), \( T_{sR} \), \( T_{wR} \), \( T_{sR} \))
- Mutual inductance has ten dimensions:
  - (n, length, location1, location2, \( T_{wL} \), \( T_{sL} \), \( T_w \), \( T_{sR} \), \( T_{wR} \), \( T_{sR} \))
- Length is needed because inductance is not linearly scalable
Definition of Partial Inductance

\[ L_{ij} = \frac{\mu}{4\pi} \left( \frac{1}{a_i a_j} \right) \int_{b_i}^{c_i} \int_{b_j}^{c_j} \frac{dl_i dl_j}{r_{ij}} da_i da_j \]

- Partial inductance is the portion of loop inductance for a segment when its current returns via the infinity.
  - called partial element equivalent circuit (PEEC) model
- If current is uniform, the partial inductance is

Partial Inductance for N Traces

<table>
<thead>
<tr>
<th>TW_L</th>
<th>TW</th>
<th>TW</th>
<th>TW</th>
<th>TW_R</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.17</td>
<td>5.43</td>
<td>5.12</td>
<td>4.89</td>
<td>4.66</td>
</tr>
<tr>
<td>5.43</td>
<td>6.79</td>
<td>6.10</td>
<td>5.48</td>
<td>5.04</td>
</tr>
<tr>
<td>5.12</td>
<td>6.10</td>
<td>6.79</td>
<td>6.10</td>
<td>5.33</td>
</tr>
<tr>
<td>4.89</td>
<td>5.48</td>
<td>6.10</td>
<td>6.79</td>
<td>5.77</td>
</tr>
<tr>
<td>4.66</td>
<td>5.04</td>
<td>5.33</td>
<td>5.77</td>
<td>6.50</td>
</tr>
</tbody>
</table>

- Treat edge traces same as inner traces
  - lead to 5x5 partial inductance table
- There is no need to specify current return loop for SPICE simulation
  - in high frequency, the current often returns via nearest quiet traces (rather than edge traces)
Foundation I

The self inductance under the PEEC model for a trace depends only on the trace itself (its length, width, thickness)

$$\begin{array}{cccccc}
T_{W_L} & T_w & T_w & T_w & T_{W_R} \\
6.17 & 5.43 & 5.12 & 4.89 & 4.66 \\
5.43 & 6.79 & 6.10 & 5.48 & 5.04 \\
5.12 & 6.79 & 6.10 & 6.10 & 5.33 \\
4.89 & 5.48 & 6.10 & 6.79 & 5.77 \\
4.66 & 5.04 & 5.33 & 5.77 & 6.50 \\
\end{array}$$

$$T_s$$ $T_s$ $L$ $T_s$ $R$

6.50

Foundation II

The mutual inductance under the PEEC model for two traces depends only on the traces themselves (lengths, widths, and thicknesses)

$$\begin{array}{cccccc}
T_{W_L} & T_w & T_w & T_w & T_{W_R} \\
6.17 & 5.43 & 5.12 & 4.89 & 4.66 \\
5.43 & 6.79 & 6.10 & 5.48 & 5.04 \\
5.12 & 6.79 & 6.10 & 6.10 & 5.33 \\
4.89 & 5.48 & 6.10 & 6.79 & 5.77 \\
4.66 & 5.04 & 5.33 & 5.77 & 6.50 \\
\end{array}$$

$$T_s$$ $T_s$ $L$ $T_s$ $R$

$$t_L$$ $t_1$ $t_2$ $t_3$ $t_{R}$

6.17 $4.66$

4.66 $6.50$
Validation and Implication of Foundations

- Two foundations can also be validated theoretically

- Problem size of inductance extraction can be greatly reduced
  - solve 1-trace problem for self inductance
  - solve 2-trace problem for mutual inductance

- There is no loss of accuracy during reduction

Analytical Solutions to Inductance

- Without considering skin effect and internal inductance
  - Self inductance \[ L(nH) = 2 \mu l \cdot \left[ \ln\left(\frac{2l}{w + l}\right) + 0.5 - k \right] \]
    - \( k = f(w, l) \)
    - \( 0 < k < 0.0025 \)
  - Mutual inductance \[ L(nH) = \frac{\mu l}{2\pi} \cdot \left[ \ln\left(\frac{2l}{s}\right) - 1 + \frac{s}{l} \right] \]

- Inductance is not sensitive to width, thickness and spacing
  - No need to consider process variations for inductance

Not suitable for on-chip interconnects
Table-based Solutions to Inductance

- Only need to solve self and mutual inductance for two-trace structures via numerical extraction
- Built tables for each layer under nominal geometry
  - Self inductance table has two dimensions
    - Width and length
  - Mutual inductance table has four dimensions
    - Two widths, length, and spacing
- Bicubic-spline interpolation and linear extrapolation for inductance not in tables
- It has been integrated with statistically-based RC model

Outline

- Importance of on-chip inductance

- Efficient inductance model
  - Loop inductance and partial inductance
  - Foundations to reduce problem size
  - Table-based inductance extraction

- Applications and future works
  - Coplanar waveguide
  - Buses structure
Coplanar Waveguide

- Wire taping helps to sharpen waveform, but causes reflections
- Coplanar waveguide needs to be synthesized to match impedance
  - with optimized width and spacing for all three traces

Loop inductance for Coplanar Waveguide

- Its loop inductance can be solved analytically in order to match impedance
  - In symmetric case \[ L_{\text{loop}} = L_{p_{22}} - 2L_{p_{23}} + \frac{L_{p_{11}}}{2} + \frac{L_{p_{13}}}{2} \]
Shielding Insertion

- To decide Ns and Ws for given length, widths and spacings for a set of signal traces
  - Ns: number of signal traces between two shielding traces
  - Ws: width of shielding traces

![Diagram showing signal traces with shielding insertion]

Trade-off between Area and Noise

- Total 18 signal traces
  - 2000um long, 0.8um wide
  - separated by 0.8um

- Drivers --130x; Receivers -- 40x

- Power supply: 1.3V

<table>
<thead>
<tr>
<th>Ns</th>
<th>Ws</th>
<th>Noise(V)</th>
<th>Routing Area (um)</th>
<th>Wire Area (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>--</td>
<td>0.71</td>
<td>61.1(0.0%)</td>
<td>46.4(0.0%)</td>
</tr>
<tr>
<td>6</td>
<td>0.8</td>
<td>0.38</td>
<td>64.8</td>
<td>48.0</td>
</tr>
<tr>
<td>6</td>
<td>1.6</td>
<td>0.27</td>
<td>66.4</td>
<td>49.6</td>
</tr>
<tr>
<td>6</td>
<td>2.4</td>
<td>0.22</td>
<td>68.0</td>
<td>51.2</td>
</tr>
<tr>
<td>3</td>
<td>0.8</td>
<td>0.17</td>
<td>69.6(13%)</td>
<td>50.4(8.8%)</td>
</tr>
</tbody>
</table>
Conclusions

- An efficient table-based inductance model has been developed
  - by pre-solving two-trace problems

- The statistically-based RLC model has been used for clock tree modeling and simulation, and shielding insertion in real designs