AN IMPROVED DE-EMBEDDING TECHNIQUE FOR ON-WAFER HIGH-FREQUENCY CHARACTERIZATION

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Abstract

An improved correction procedure for on-wafer S-parameter measurements has been developed and implemented. The new method also takes the effects of series parasitics into account in a simple, straightforward way. The improved performance of the new method with respect to the usual method – that accounts for parallel parasitics only – especially at frequencies exceeding a few *GHz* is demonstrated. Its performance is also compared with that of more complex methods.

Introduction

In order to characterize the ac small-signal behavior of microwave transistors, usually a set of two-port s-parameters is measured using a scalar network analyzer. At present the possibility of on-wafer measurements up to 50GHz exists.

When performing hf measurements on wafer, a two step correction procedure has to be followed. Firstly the measurement system has to be calibrated, defining a reference plane for the S-parameter measurements at the probe tips using a standard calibration technique (SOLT, LRM or other [2,3]). Secondly the on wafer parasitics have to be characterized, so that from the measurement the actual transistor two-port parameters can be obtained.

The conventional method for obtaining the transistor two-port Y-parameters is described in [1]. In this method two measurements are done to obtain transistor Y-parameters: a measurement in which only the interconnect pattern surrounding the transistor (called an 'open') is measured, resulting in the 'open' two-port parameters Y_{open}; and a transistor measurement – which of course includes the interconnect parasitics – described by the two-port Y-parameters Y_{dut}. Assuming an equivalent circuit diagram as depicted in figure 1, the transistor Y-parameters are found from the relation

$$Y_{transistor} = Y_{dut} - Y_{open}. \qquad (1)$$

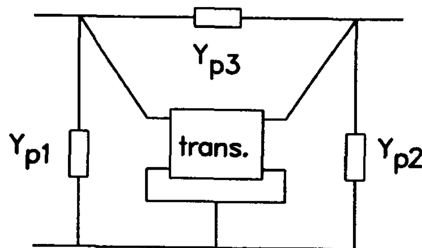

Figure 1: *Equivalent circuit diagram used for conventional deembedding. Only parallel parasitics Y_{p1}, Y_{p2} and Y_{p3} are included.*

This correction procedure only corrects for the parallel parasitics: it is implicitly assumed that series parasitics in the interconnect lines are negligible.

Measurements on modern IC transistors show, however, that this is not always the case, and that for low impedance, high-transconductance devices these series parasitics must be taken into account, even at fairly low frequencies. This requires a more advanced correction procedure.

Correction method

As stated previously, a more complete model for parasitics is necessary when performing high frequency measurements. In this section we will propose a new correction procedure and we will show its validity by a comparison with an even more advanced method.

A suitable equivalent circuit diagram of a transistor with its surroundings is given in figure 2. It shows the actual transistor as a two-port, embedded in parasitics of the interconnect lines and bonding pads.

The parasitics surrounding the transistor can be characterized by measuring two patterns after system calibration: an 'open' interconnect pattern as is shown in figure 3 and is also used in the conventional correction method. This measurement provides us with the 'open' Y-parameters Y_{open}; also a corresponding 'short' pattern (see figure 4) is measured, providing the 'short' Y-parameters Y_{short}. The second measurement is used to determine losses and phase rotation in the interconnect lines.

Assuming such an equivalent circuit, the series impedances can now easily be found from the short measurement by assuming a T-network model with impedances Z_{L1}, Z_{L2} and Z_{L3} as shown in figure 4. The 'short' Y-parameters are first corrected for parallel parasitics obtained from the 'open' measurement and transformed to Z-parameters:

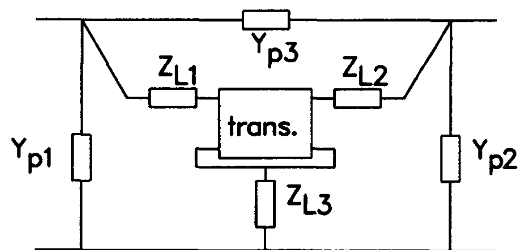

Figure 2: *Equivalent circuit diagram used for the two-step correction method, including both the parallel parasitics Y_{p1}, Y_{p2}, Y_{p3} and the series parasitics Z_{L1}, Z_{L2} and Z_{L3} surrounding the transistor.*

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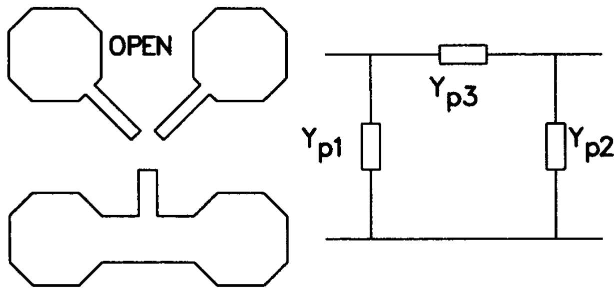

Figure 3: *'Open' pattern on wafer used to characterize the parallel parasitics. Also shown is the equivalent circuit diagram of this open pattern with parallel parasitics Y_{p1}, Y_{p2} and Y_{p3}.*

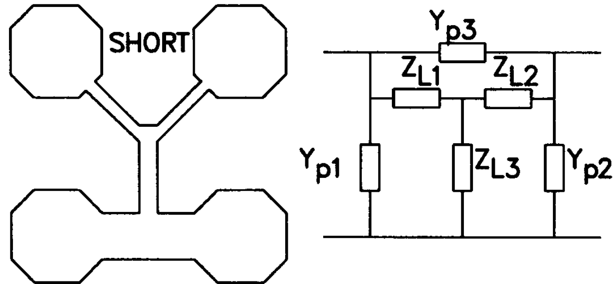

Figure 4: *'Short' pattern on wafer used to characterize the series parasitics. Also shown is the equivalent circuit diagram of this short pattern with series impedances Z_{L1}, Z_{L2} and Z_{L3} embedded in parallel parasitics.*

$$\begin{pmatrix} Z_{L1} + Z_{L3} & Z_{L3} \\ Z_{L3} & Z_{L2} + Z_{L3} \end{pmatrix} = (Y_{short} - Y_{open})^{-1} \qquad (2)$$

Simple mathematics show that for a configuration as in figure 2 with impedances Z_{L1}, Z_{L2} and Z_{L3} in series with a linear two-port the Z-parameters of the two-port can be found by subtraction of the Z-parameter matrix for the T-network from that of the total.

The actual transistor Y-parameters can be obtained from:

$$Y_{trans} = ((Y_{dut} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1}, \qquad (3)$$

with Y_{dut} as the measured Y-parameter matrix of the transistor together with parasitics and Y_{trans} as the actual transistor Y-parameter matrix. In this paper we will refer to this correction procedure as the 'two-step' correction method.

Using this two-step method, transmission line behaviour of the series parasitics is implicitly modelled. In this sense the method is superior over those employing lumped equivalent circuits. Another advantage over other methods is that no changes in the internal calibration values of the network analyzer are necessary for obtaining accurate results (as opposed to [4] for example). Once the measurement system is calibrated, a large range of device geometries can be measured using the same calibration set.

Two experiments were performed to verify the validity of the assumption used in this approach that all parallel parasitics can be located at the bonding pads, while in fact they are partly distributed over the interconnect lines leading to the transistor.

Firstly a comparison was made between different 'open' geometries, in order to verify the contribution of the interconnect leads to the total parallel parasitics. From this experiment we observe that parallel parasitics are indeed located mainly at the bonding pads, as is shown in figure 5. Here we have measured the Y-parameters of two opens, one consisting of only bonding pads and one also including interconnect lines. From the measurements we observe that a maximum of twenty percent of the admittance originates from the interconnect lines. In practice this means that – unless series impedance in the lines are high – all parallel parasitics may be modelled at the outside.

In order to investigate the influence of the interconnect lines further, an even more advanced correction procedure (in this paper referred to as the 'distributed' approach) was implemented. This method distributes the parallel parasitics introduced by the interconnect lines (Y_{lp1}, Y_{lp2} and Y_{lp3}) over the beginning and end of the line (see figure 6), at the cost of one extra 'open' measurement for the correction process and of somewhat more involved mathematics. It is assumed that series impedance in the emitter interconnect line is sufficiently low and that crosstalk occurs between the interconnect lines when these are close together. The second open measurement is used to determine the contribution of the interconnect lines to the parallel parasitics and is in our case performed on an 'open' pattern consisting of the bonding pads only. We have used this distributed method to estimate the accuracy of the two-step method (equations 3

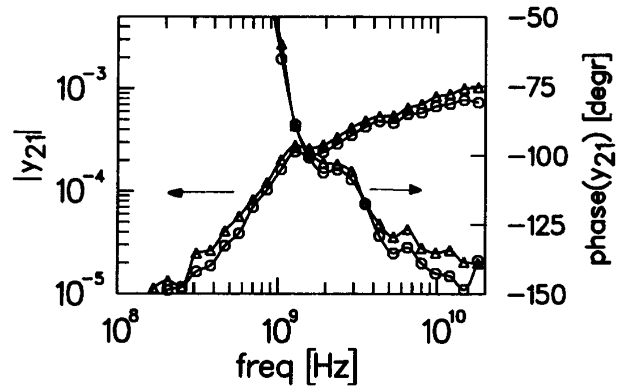

Figure 5: *Measured Y-parameters for two different opens; o: bonding pads only; △: open including interconnect lines.*

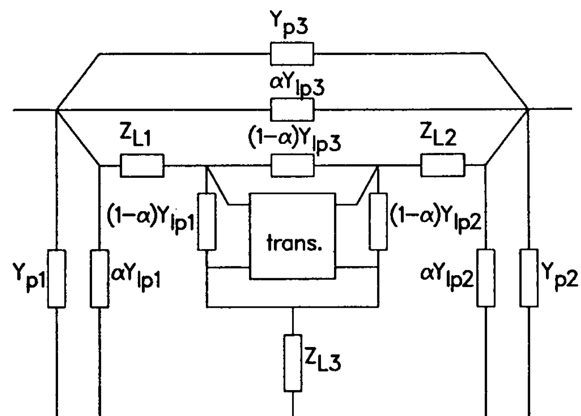

Figure 6: *Equivalent circuit diagram used for the distributed method, including parallel parasitics Y_{p1}, Y_{p2} and Y_{p3} originating from the bonding pads and the series and parallel parasitics Z_{L1}, Z_{L2} and Z_{L3}, Y_{lp1}, Y_{lp2} and Y_{lp3} originating from the interconnect lines.*

and 2). This method can be described using:

$$\begin{aligned} Y_{trans} \;=\; & ((Y_{dut} - \alpha(Y_{open} - Y_{bond}))^{-1} \\ & -(Y_{short} - \alpha(Y_{open} - Y_{bond}))^{-1})^{-1} \qquad (4) \\ & -(1-\alpha)(Y_{open} - Y_{bond}), \end{aligned}$$

with α a weighting factor distributing the parallel parasitics of the lines over beginning and end of the line. Y_{trans}, Y_{dut}, Y_{open}, Y_{bond} and Y_{short} are the Y-parameter matrices of the actual transistor, the transistor with its surroundings, the normal 'open' pattern, the 'bonding-pads' pattern and the 'short' pattern respectively.

In the case $\alpha = 1$ this method is identical to the two-step method, placing all parallel parasitics at the bonding pads. For $\alpha = 1$, the parallel parasitics originating from the interconnect lines are placed directly over the transistor terminals. Since from the 'open' measurements described above and shown in figure 5 we observe that the contribution of the interconnect lines to the parallel parasitics is relatively small, we expect only a marginal improvement in performance when adopting the distributed approach.

Experimental results

The two-step and distributed correction procedures have been used on a variety of test samples. The results shown here were obtained from transistors fabricated in the BASIC process[5], featuring $h_{FE} \approx 100$, $V_{eaf} \approx 20V$ and $f_T \approx 18GHz$. For the measurements presented here the devices were biased at $V_{be} = 0.85V$ and $V_{cb} = 1V$.

An example for a fairly small transistor with emitter dimensions of $0.4 \times 8.4\mu m^2$ on silicon is shown in figure 7. Interconnect lay-out was such that series impedance at the emitter was minimized. Deviations due to series parasitics become noticeable at frequencies higher than a few GHz and should be taken into account.

For transistors that have been designed for performing at lower impedance levels, even at fairly low frequencies there is a significant difference between the old and the new correction procedures (figure 8, emitter dimensions are $1.4 \times 58.4\mu m^2$). This is mainly caused by the fact that these transistors feature a high transconductance, so that any parasitic impedance at the emitter – be it only a few tenths of an Ohm – shows strongly. Especially the differences in y_{11} and y_{21} are striking. Measurements at higher frequencies show that series impedance in the lines – if not taken into account – gives rise to a significant error in the phase of all four Y-parameters. This indicates that for transistor characterisation using measured Y-parameters [6] one of the new correction procedures should be adopted.

It can also be observed from the measurements that no significant improvement in correction results is obtained by using the distributed correction method. Therefore the two-step correction procedure as described in equation 3 is preferable because of its relative simplicity.

This is also the case for another correction method recently proposed in [7], needing four measurements to determine the parasitic element values. Due to the location of the parallel parasitic Y_{p3} in the equivalent circuit diagram, this method will exaggerate the influence of series parasitics. We therefore expect a larger phase correction than obtained using the two-step and distributed methods. When compared with the two-step

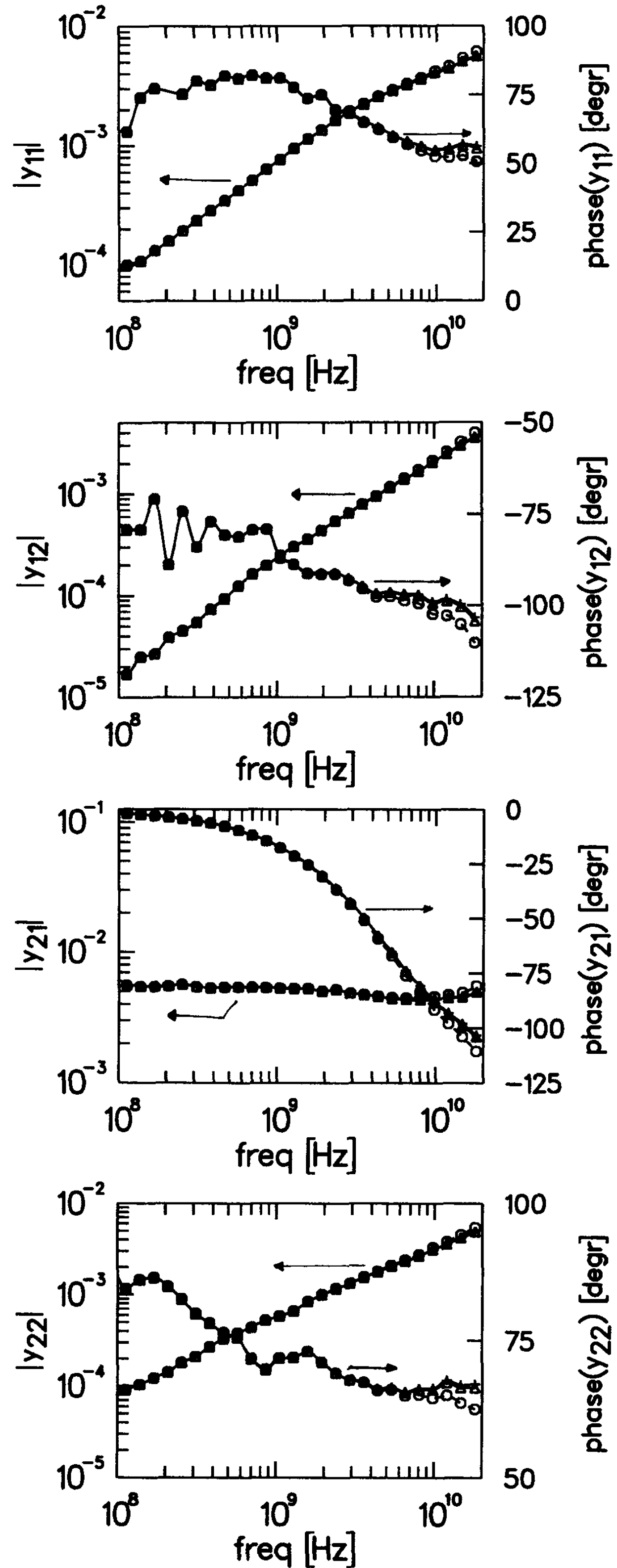

Figure 7: *Measured Y-parameters of a small transistor for the conventional (○), two-step (△) and distributed (+, $\alpha = 0.5$) correction methods.*

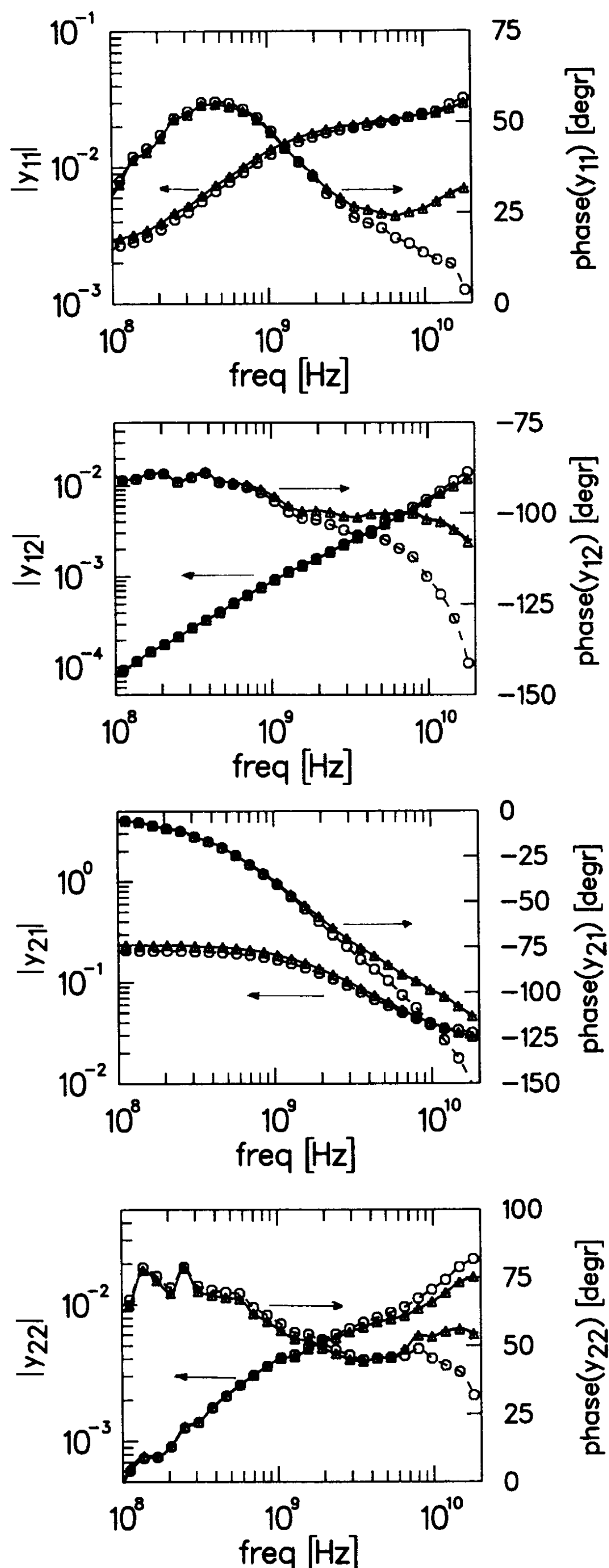

Figure 8: *Measured Y-parameters of a large transistor for the conventional (○), two-step (△) and distributed (+, α = 0.5) correction methods.*

and distributed methods (see figure 9) we see that indeed this method yields a significantly larger phase correction.

From the measurements it can be deduced that series parasitics have to be taken into account when the product of y-parameter and series impedance is in the order of 0.1.

Since series parasitics do not influence the current gain, f_T will not be affected by the choice of correction procedure, as is illustrated in figure 10.

Conclusions

A new, simple two-step method for correcting on-wafer high-frequency measurements has been presented. The new method takes into account the parasitic series impedances surrounding the device. The method has been compared with other more complex methods and has shown to yield accurate results, at the same time offering relative simpleness. Only one extra measurement of a 'short' pattern is necessary, compared to the conventional correction procedure. f_T determined from Y-parameters is not affected by the new correction method, but the individual Y-parameters are. Therefore, for transistor characterization using measured Y-parameters the new correction should be adopted.

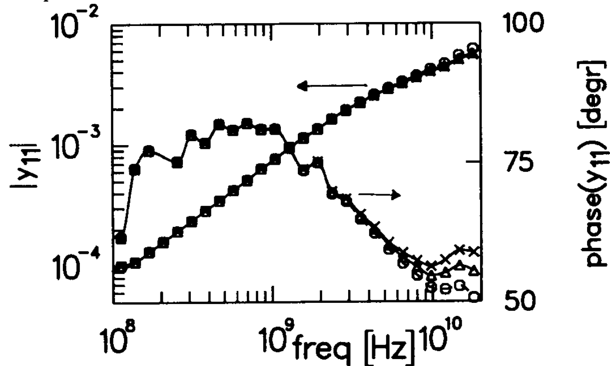

Figure 9: *Measured Y-parameters of a small transistor using classical (○), two-step (△) and three-step (×) ([7]) correction procedures.*

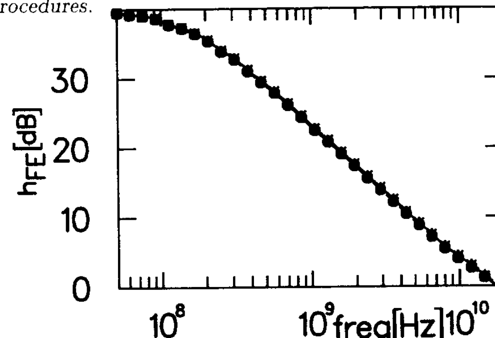

Figure 10: *Current gain as a function of frequency for a large transistor. All four correction methods yield identical results.*

References

[1] P.J. v. Wijnen et al., IEEE BCTM 1987, pp. 70-73.

[2] A. Fraser et al., IEEE BCTM 1988, paper 7.6, pp. 154-157.

[3] A. Davidson et al., 34th ARFTG Conf. Dig. 1989, pp. 61-66.

[4] E.S. Copeland et al., 34th ARFTG Conf. Dig. 1989, pp. 138-146.

[5] J. v.d. Velden et al., IEEE IEDM 1989, paper 9.4, pp. 233.

[6] M.P.J.G. Versleijen, IEEE BCTM 1991.

[7] H. Cho et al., IEEE Trans. El. Dev., Vol. 38, no. 6, june 1991, pp. 1371-1375.