DEVELOPING 3D LAYOUT AUTOMATION

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Contents

- 3D IC Technology Background
- 3D IC Placement Via Transformation
- 3D IC Routing & Thermal Via Planning
- Conclusions & Future Works
What is the 3D Stacked IC

- 3D wafer/die stacking using through silicon-vias (TS-Vias)
  - Pros: area/performance/power, heterogeneous integration
  - Cons: manufacturing cost/yield, thermal/noise issues

Some contents were quoted from the presentation material of Prof. Sung Kyu Lim (GIT)
What is the 3D Stacked IC

- Manufacturing Technology


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Currently Samsung Offers...

- Multi Chip Package (Wire-bonding): Memory & System LSI
- Wafer Stack Package (TS-Via): Memory (Engineering Sample)

- 8 stacks of 2GB NAND Flash (each die 50um thick)

<table>
<thead>
<tr>
<th>Via Type</th>
<th>Via Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Via</td>
<td>About 0.5um</td>
</tr>
<tr>
<td>WSP TS-Via</td>
<td>About 5um</td>
</tr>
<tr>
<td>MCP Bonding Pad</td>
<td>Larger than 50um</td>
</tr>
</tbody>
</table>

Some contents were quoted from the presentation material of Prof. Sung Kyu Lim (GIT)
3D Stacked IC of Near Future

- T-Vias can be used to connect any dies together
- T-Vias can be located anywhere in the chip
- Stacking Approaches: F2F / F2B / B2B

Some contents were quoted from the presentation material of Prof. Sung Kyu Lim (GIT)
Implementing 3D Layout

- **Target**
  - Minimizing manufacturing cost / Increasing yield
    - Making TS-vias is still high cost / low yield manufacturing technique
  - Minimizing thermal problem
    - Vertical stacked multi-layers of active devices causes big power density
    - Thermal conductivity of dielectric layer between silicon is very low

- **Approaches**
  - Try Folding Existing Designs
    - Start with an existing design, Partition it into 2 or 4 parts
    - Stack & connect them and evaluate
    - IBM/Intel: tried, know it works, found many issues
  - Start from Scratch: 3D-Aware
    - Design each die with stacking in mind
    - Stack them and evaluate
    - Takes longer, but better quality

<table>
<thead>
<tr>
<th>Materials</th>
<th>Thermal Conductivity</th>
</tr>
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<tbody>
<tr>
<td>Epoxy</td>
<td>0.05W/mK</td>
</tr>
<tr>
<td>Silicon</td>
<td>150W/mK</td>
</tr>
<tr>
<td>Copper</td>
<td>285W/mK</td>
</tr>
</tbody>
</table>

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Motivation of 3D IC Layout Automation

- Thermal problem is aggravated in 3D IC
  - The devices are more packed, which results in higher power density
  - The insulating dielectric layers much lower thermal conductivities than silicon

- Existing 2D metrics not so efficient
  - a “bounding-cube” might not have enough accuracy for wirelength estimation because of the existence of huge obstacles in z-direction
  - 3D IC physical design problem is usually of higher complexity, with a much enlarged solution space due to the multiple device layer structure

- New thermal aware 3D Implementation tools are under developing
3D IC Physical Design Project in UCLA

- MEVA (Microarchitecture EVAluation)-3D
  - An automated physical design and architecture performance estimation flow for 3D architectural evaluation
  - Including 3D floorplanning, routing, interconnect pipelining and automated thermal via insertion, and associated die size, performance, and thermal modeling capabilities
3D IC - Thermal Modeling

- Assumptions for simplicity
  - Only consider the steady-state heat & heat generated by transistor switches
  - Macro blocks: heat sources with constant power densities.
  - Heat sink is attached to the substrate → Constant room temperature, 27°C
  - The four side walls and top of the chip are treated as adiabatic

- Duality between heat transfer and electrical current flow
  - Heat flow passes a thermal resistance / temperature at any point is analogous to the voltage at that point / heat source is analogous to a fixed current source

- Compact Resistive Thermal Model to speedup run time
  - Can be solved by a linear solver such as SPICE (Modeling error rate is smaller than 2%)

![Diagram of 3D IC thermal modeling with assumptions and models including tiles, resistance, current source, and voltage source.]
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- 3D IC Routing & Thermal Via Planning
- Conclusions & Future Works
3D IC Placement Via Transformation

- Generating 3D thermal-aware placement from existing 2D placement
  - 3D transformation
    - Local stacking transformation, Folding-based transformation
    - Window-based stacking/folding transformation
  - The layer assignment refinement
    - Relaxed conflict-net (RCN) graph representation

- The advantages
  - The existing high-quality 2D placement core engine can be easily reused
  - A discrete layer assignment algorithm based on graph representation
    - No rounding for layer assignment is necessary as in some previous approach
  - A simple yet effective thermal cost
    - No time-consuming thermal profiling is needed during the optimization process
  - Different transformation schemes and the parameter settings in the RCN graph-based layer
    - Enables flexible TS via number and wirelength tradeoff
Local Stacking Transformation (LST)

Stacking
- For K device layer, $(x, y) \rightarrow (x', y')$ where $x' = x / \sqrt{K}$, and $y' = y / \sqrt{K}$

Tetris-style Legalization
1. Sort all cells by x-coordination
2. Starting from left most cell, determine layer and exact location by minimizing relocation cost $R$

$$R = \alpha \cdot d + \beta \cdot v + \gamma \cdot t$$
where $d$ is the cell displacement, $v$ is the TS-via number and $t$ is the thermal cost

Drawback: May generate a great number of TS vias when the cells of local nets are put on top of one another

Figure 3  Local Stacking Transformation
Local Stacking Transformation (LST) – Cont’d

- **Thermal Optimization**
  - Z location tile stacks are considered for faster process
  - Lateral heat flow can be considered during initial thermal aware 2D place
  - Each tile stack is viewed as an independent thermal resistive chain
  - The maximum temperature
    \[
    T = \sum_{i=1}^{k} (R_i \sum_{j=1}^{k} P_{ij}) + R_b \sum_{i=1}^{k} P_i = \sum_{i=1}^{k} P_i (\sum_{j=1}^{k} R_j + R_b)
    \] (2)
  - Thermal cost of assigning cell \( j \) to layer \( i \)
    \[
    t_{i,j} = P_j (\sum_{k=1}^{i} R_k + R_b)
    \]

(a). Tiles Stack Array  (b). Single Tile Stack  (c). Tile Stack Analysis
3D IC Placement Via Transformation

- **Transformation through Folding**
  - Fold the original 2D placement like a piece of paper
  - The distance between any two cells will not increase
  - TS vias are only introduced to the nets crossing the folding line
  - Drawback: May not achieve as much as wirelength reduction as LST because only the length of global net go across the folding lines are reduced

![Diagram of folding transformations](image)

(a) folding-2 transformation   (b) folding-4 transformation

Figure 4 Two Folding-based Transformation Schemes
Window-based Stacking/Folding

Procedure
- Divide the 2D placement into N X N windows (solid lines)
- Apply stacking or folding in every window
- Each window is again divided into four squares (dotted lines)
- The number in each square indicates the layer number

Total Wirelength is reduced than Folding only
- wirelength of nets inside the square is preserved
- wirelength of nets inside the same window & cross the different windows is most likely reduced

Number of TS-vias can be reduced than LST
- Assign layer to minimize Inter-window transition \( \Rightarrow \) Reduce #TS-via

# of windows controls Wirelength vs. #TS-vias tradeoff

Figure 5 2×2 windows with different layer assignments
Refinement: RCN Graph-based Layer Assignment

- Relaxed Conflict-net (RCN) graph: directional acyclic graph.
  - Nodes: Both the cells and the vias (One via node is assigned for each net)
  - Net edges: all cells are connected to the via node by net edges
  - Conflict edges: cells that overlap with each other if they are placed in the same layer

- Costs
  - Conflict edge $\Rightarrow$ If two cells are assigned to the same layer than cost is Infinity, else 0
  - Via node $\Rightarrow$ total TS-via number in that net = height of via in Z direction
  - Cell node $\Rightarrow$ thermal cost $t_{i,j}$ of assigning node $v_j$ to layer $l$
  - Cost of path = sum of edge & node cost along the path

- Solve (Use algorithm in [9])
  - Construct a sequence of maximal induced sub-tree of the graph
  - Apply linear time optimal algorithm (Dynamic Programming) to refine the layer assignment

Figure 6 Relaxed Conflict-Net Graph
Refinement: Relaxed Non-Overlap Constraint

- Non-overlap constraints can be relaxed so that a small amount of overlap “r” is allowed → Affect making conflict edge in RCN graph
- In exchange for more freedom in layer reassignment of the cells
- to further reduce the TS via number

Figure 7 Relaxation of Non-overlap Constraint
Experimental Results

Procedures

- Generate initial legalized wirelength driven 2D global placement
- Apply 3D transformation and refinement
- Run 2D detailed placer for each device layers

Compared with 2D, wirelength reduction about 2X with 4 device layer

Among the 3D transform methods, window based stacking shows best result considering both of WL and via#

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Table 1  Benchmark characteristics and Wirelength Comparison of T3Place and 2D mPL5 [5]

<table>
<thead>
<tr>
<th>circuit</th>
<th>cell #</th>
<th>net #</th>
<th>2D mPL5</th>
<th>LST (r=10%)</th>
<th>LST (r=20%)</th>
<th>Folding-2</th>
<th>Folding-4</th>
<th>LST (8x8 win)</th>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>WL</td>
<td>via #</td>
<td>WL</td>
<td>via #</td>
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<td>Avg</td>
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<td>0.50</td>
<td>1.00</td>
<td>0.56</td>
<td>0.71</td>
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</table>
Experimental Results – Cont’d

Thermal aware result vs. no temperature optimization

- Can reduce the maximum on-chip temperature by 37% on average with 6% more TS vias and 8% longer wirelength

Comparing with a other 3D placement algorithm in [10]

- Over 5X reduction

### Table 2 Thermal-Aware T3Place Results

<table>
<thead>
<tr>
<th>circuit</th>
<th>LST, r = 10% Temp. (°C)</th>
<th>LST, r = 10%, w/ temp optimization Temp. (°C)</th>
<th>WL</th>
<th>via #</th>
<th>Temp. (°C)</th>
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<tr>
<td>Avg.</td>
<td></td>
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<td>1.06</td>
<td>0.54</td>
<td>0.63</td>
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</table>

### Table 3 Comparisons with Existing 3D Placement [13]

<table>
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<tbody>
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<td>46.3</td>
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<td>47.7</td>
<td>252.5</td>
</tr>
</tbody>
</table>
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Overview

Thermal through the silicon (TTS) vias should be additionally placed to exhaust heat into heat sink

- Although thermal-driven floorplan/place was performed, max. temperature is too high to operate properly (150 °C or 302 °F)
- TTS via size (5~10um) affects routing resource and overall chip size

Multilevel routing framework with TTS-via planning

- Formulate the TTS via minimization problem with temperature constraints as a constrained nonlinear programming problem (NLP)
- Develop heuristic algorithm, m-ADVP (Alternative Direction TTS-Via Planning)
  - Solves a sequence of simplified via planning subproblems in alternating direction in a multilevel framework
  - Vertical via distribution is formulated as a convex programming problem
  - Horizontal via planning uses path counting and heat propagation
3D IC Routing & Thermal Via Planning

- 3 Stages of Multilevel routing framework
  - Recursive coarsening
  - Initial Solution Generation
    - First call ADVP on the coarsest level to estimate the number of TTS-vias
  - Level to level Refinement
    - ADVP repeatedly refines TS-via distribution

Figure 2: Multilevel Routing and TS-Via Planning Framework
3D IC Routing & Thermal Via Planning

- **Defines**
  - Design is divided into a 3D array of tiles, \( \{tile_{i,j,k} | 1 \leq i \leq X, 1 \leq j \leq Y, 1 \leq k \leq Z \} \)

- **Inputs**
  
  - \( T_0 \): room temperature at the heat sink
  - \( T_{input} \): user required temperature
  - \( P_{i,j,k} \): power density at \( tile_{i,j,k} \), which is determined by the macro blocks that overlap with \( tile_{i,j,k} \)
  - \( s_{i,j,k} \): STS-via number at \( tile_{i,j,k} \), which is determined by the router
  - \( c_{i,j,k} \): TS-via capacity of \( tile_{i,j,k} \)

- **Process technology related constraints (calculated using thermal simulation tool and can be used any design which has the same tech.)**

  - \( \gamma \): thermal resistance of one TS-via, which is a technology-related constant
  - \( R_{t_{i,j,k}} \): thermal resistance of \( tile_{i,j,k} \) without TS-vias, which is determined by the technology and the tile size
  - \( t_{i,j,k} \): equivalent TS-via number of a \( tile_{i,j,k} \), \( t_{i,j,k} = \gamma / R_{t_{i,j,k}} \). If we assume all tiles are of same shape and size, all device layers are fabricated using the same technology, then all \( t_{i,j,k} = t \) will be the same.
  - \( R_l \): fixed lateral resistances between tiles
3D IC Routing & Thermal Via Planning

**Defines**

- \( v_{i,j,k} \): temperature at \( tile_{i,j,k} \)
- \( I_{i,j,k} \geq 0 \): the vertical heat flow from \( tile_{i,j,k+1} \) to \( tile_{i,j,k} \)
- \( a_{i,j,k} \in Z^* \): total TS-via number at \( tile_{i,j,k} \)
- \( R_{v_{i,j,k}} \): thermal resistance of all TS-vias in \( tile_{i,j,k} \), \( R_{v_{i,j,k}} = \gamma / a_{i,j,k} \)
- \( R_{i,j,k} \): the vertical thermal resistance between \( tile_{i,j,k+1} \) and \( tile_{i,j,k} \), which is the effective resistance of \( R_{t_{i,j,k}} \) and \( R_{v_{i,j,k}} \) connected in parallel

\[
R_{i,j,k} = \frac{1}{1/R_{t_{i,j,k}} + 1/R_{v_{i,j,k}}} = \frac{1}{\gamma + a_{i,j,k}/\gamma} = \frac{1}{\gamma + a_{i,j,k}}
\]

**Duality between heat transfer and electrical current flow**

- Heat flow passes a thermal resistance / temperature at any point is analogous to the voltage at that point / heat source is analogous to a fixed current source

\[
\frac{1}{R_{i,j,k}} = \frac{I_{i,j,k}}{\Delta V} = \frac{I_{i,j,k}}{(v_{i,j,k} - v_{i,j,k-1})}
\]
NLP Problem Formulation Based on Resistive Model

Minimize Total # of TS-via \( f(V, I) = \sum_{k \geq 2} \alpha_{i,j,k} = \sum_{k \geq 2} \left( \frac{\gamma I_{i,j,k}}{v_{i,j,k} - v_{i,j,k-1}} - t \right) \) \( \) (2)

Subject to equation (3),(4),(5) and (6)

a. Temperature constraints.
\( T_0 \leq v_{i,j,k} \leq T_{\text{input}} \) \( \) (3)

b. Tile capacity constraints. The amount of TS-vias assigned to each tile should not exceed the capacity of the tile.
\( \frac{\gamma I_{i,j,k}}{v_{i,j,k} - v_{i,j,k-1}} - t \leq c_{i,j,k} \) \( \) (4)

c. Minimum TS-via number constraints. In order to avoid wirelength increase, \( a_{i,j,k} \) should be larger than or equal to \( s_{i,j,k} \), so that the STS-vias will not be moved to a position where detours will be introduced.
\( \frac{\gamma I_{i,j,k}}{v_{i,j,k} - v_{i,j,k-1}} - t \geq s_{i,j,k} \) \( \) (5)

d. Kirchoff's current law (KCL). For each node \( j \) in \( V \) except the ground, the sum of incoming heat flows should be the same as the sum of outgoing heat flows. For node \( j \), let \( B(j) \) be the set of edges that connect with \( j \), \( d_i \) be the direction of the heat flow on edge \( i \), \( I_i \) is 1 when \( I_i \) is incoming and -1 otherwise.
\( \sum_{i \in B(j)} d_i I_i = 0 \) \( \) (6)
3D IC Routing & Thermal Via Planning

- **m-ADVP: Alternating Direction TTS-via Minimization**
  - Two-step relaxation of the original problem.
    1) Fix the \((x, y)\) locations of the TS-vias and only move the TS-vias in the \(z\) direction
    2) Fix the layers of the TS-vias and move them horizontally within each layer
    3) Iterate between step 1 and step 2 to search for a solution

![Diagram of 3D IC routing with thermal vias](image)

Figure 4: Alternating Direction Via Planning
3D IC Routing & Thermal Via Planning

- **Vertical TTS-via Distribution**
  - Vertical thermal resistance $R_k$
    
    Let $a_k = \sum_{1 \leq i \leq M, 1 \leq j \leq N} (a_{i,j,k} + t)$ be the total TS-via number in layer $k$ of $\Omega$, then $R_k$ can be calculated as follows.
    \[
    R_k = \frac{\gamma}{\sum_{1 \leq i \leq M, 1 \leq j \leq N} (a_{i,j,k} + t)} = \frac{\gamma}{a_k} \tag{7}
    \]
  - Temperature of node $k$ (Similar as Elmore Delay)
    
    \[
    v_k = \sum_{i=1}^{k} R_i \sum_{j=i}^{Z} P_j' + T_0 \tag{8}
    \]
  - Convex programming problem
    \[
    \begin{align*}
    \min & \quad \sum_{k=2}^{Z} a_k \\
    \text{s.t.} & \quad v_Z = \sum_{k=1}^{Z} R_i \sum_{l=k}^{Z} P_l' + T_0 \\
    & \quad \sum_{k=1}^{Z} \frac{\gamma}{a_k} \sum_{l=k}^{Z} P_l' + R_b \sum_{k=1}^{Z} P_k' + T_0 \\
    & \quad s_k \leq a_k \leq c_k, \quad k = 2, \ldots, Z
    \end{align*}
    \tag{9}
    \]

**Figure 5: Vertical TS-Via Planning Models**

- $a_k$: Total TS-via#
- $t$: Equiv. TS-via#
- $\gamma$: Thermal Res. Of one TS-via
- $P_j$: Heat source at layer $j$
- $T_0$: Room temp. at heat sink
- $S_k$: Signal TS-via#
- $C_k$: TS-via capacity
3D IC Routing & Thermal Via Planning

- **Horizontal TTS-Via Distribution**
  - **Challenge**
    - TS-vias cannot be placed directly at the hottest spots since those places are occupied by macro blocks or cells
  - **Mitigation: “Heat propagation”**
    - Initial even distribution of TS-vias
    - The heat generated by the "hot blocks" will then flow to the neighboring whitespace with TS-vias
    - Distribute the TS-vias according to the vertical heat flow at each tile
    - The heat flow of layer $k$ depends on that of the upper layer
    - Algorithm starts from the top layer and ends at bottom layer

The two hottest places, shown with dark colors, are blocked by macros.
Horizontal TTS-Via Distribution – Cont’d

“Path Counting” & Heat Flow Computation

- In order to speedup, we calculate the heat flow through path counting and also assume the temperature at the lower layer is uniform.
- Total thermal resistance of each path is calculated by adding the resistances on the path together.
- Heat will generally flow to the lower layers due to the heat sink. There are many dissipating paths from a layer $k$ tile to the tiles at layer $k-1$.
- By the experimental, the shortest paths less than 10 are enough.

\[
H_{i,j,k} = I_{i,j,k+1} + P_{i,j,k}
\]

Figure 6: Horizontal TS-Via Planning Models
Horizontal TTS-Via Distribution — Cont’d

Heat Flow Computation Example

Assume we count the five shortest paths p1, ..., p5

\[ R(p_1) = R_{i \cdot distance} + R_{i-1,j+1,k} = R_{i \cdot distance} + \gamma/(a_{i-1,j+1,k} + t) \] (17)

The heat flow on \( p_1 \) is then calculated as

\[ I(p_1) = H_{i,j,k} \frac{1}{\sum_{j=1}^{5} 1/R(p_j)} \] (18)

TS-via assignment

After path counting for every tile, we can calculate \( I_{i,j,k} \), where \( I_{i,j,k} \) is the sum of the heat flow on all paths ending at \( tile_{i,j,k-1} \). Then, TS-vias will be assigned to tiles proportional to \( I_{i,j,k} \).

Iteration

After horizontal TS-via distribution at each layer, the heat flow map will be updated and used by the following vertical TS-via distribution as well.
3D IC Routing & Thermal Via Planning

- Pseudo code

<table>
<thead>
<tr>
<th>Table 1: ADVP Algorithm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input:</strong> $\Omega = M \times N \times Z$, $I_{i,j,k}$, $A_0[k]$ from the previous planning result</td>
</tr>
<tr>
<td><strong>Output:</strong> assigned TS-via number for each tile $a_{i,j,k}$</td>
</tr>
</tbody>
</table>

for every device layer $k$, starting from the top

{ 
  set initial distribution = even distribution of $A_0[k]$, 
  heat propagation for layer $k$ to update $\{I_{i,j,k}\}$
}

while not converged

{ 
  for each $i$, $j$, $1 \leq i \leq M$, $1 \leq j \leq N$, 
  vertical TS-via distribution for $\{tile_{i,j,k} | 1 \leq k \leq Z\}$ 
  for every device layer $k$, starting from the top

  { 
    horizontal TS-via distribution for $\{tile_{i,j,k} | 1 \leq i \leq M, 1 \leq j \leq N\}$ 
    heat propagation for layer $k$ to update $\{I_{i,j,k}\}$
  }
}

}
3D IC Routing & Thermal Via Planning

- **Experimental Results**
  - m-ADVP algorithm is more than 200X faster than the direct solution to the NPL formulation for via planning with very similar solution quality (within 1% of TS-vias count)
  - Success to meet the temperature constraint by adding 2X~4X TTS-vias

<table>
<thead>
<tr>
<th>circuits</th>
<th>#nets</th>
<th>init T (°C)</th>
<th>flat level #tile</th>
<th>#STS-via</th>
</tr>
</thead>
<tbody>
<tr>
<td>ami33</td>
<td>133</td>
<td>157.9</td>
<td>22×22×4</td>
<td>500</td>
</tr>
<tr>
<td>ami49</td>
<td>407</td>
<td>191.8</td>
<td>60×59×4</td>
<td>889</td>
</tr>
<tr>
<td>n100</td>
<td>884</td>
<td>208.1</td>
<td>44×40×4</td>
<td>1510</td>
</tr>
<tr>
<td>n200</td>
<td>1584</td>
<td>195.7</td>
<td>42×40×4</td>
<td>2744</td>
</tr>
<tr>
<td>n300</td>
<td>1892</td>
<td>190.2</td>
<td>50×60×4</td>
<td>3559</td>
</tr>
</tbody>
</table>

Table 2: 3-D Routing Examples

<table>
<thead>
<tr>
<th>circuits</th>
<th>T (°C)</th>
<th>TS -via #</th>
<th>planning time(s)</th>
<th>T (°C)</th>
<th>TS -via #</th>
<th>planning time(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ami33</td>
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<td>77.0</td>
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<td>1850</td>
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<tr>
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<tr>
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<tr>
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<td>77.0</td>
<td>18044</td>
<td>1583.6</td>
</tr>
<tr>
<td>Avg.</td>
<td>77.0</td>
<td>1.0</td>
<td>1.0</td>
<td>0.99</td>
<td>200.4</td>
<td></td>
</tr>
</tbody>
</table>

Table 3: Comparison of m-ADVP and Solving NLP
Contents

- 3D IC Technology Background
- 3D IC Placement Via Transformation
- 3D IC Routing & Thermal Via Planning
- Conclusions & Future Works
Conclusions

- 3D Implementation Tools are developing
  - Thermal aware features are essential
  - Transform existed 2D design to 3D design
  - Build the algorithms to handle 3D issues on the top of leading edge 2D layout framework
  - 3D Placement and TS-via assignment techniques are presented

Future Works

- 3D De-cap Planning
  - 3D Floorplans have more whitespace
  - Insert/size de-caps, allow inter-layer access
- 3D Buffered Clock Routing
  - FFs located in multiple layers / Buffers inserted in multiple layers
  - Through vias can reduce wirelength
  - Skews change due to temperature change
References


Home page: http://cadlab.cs.ucla.edu/three_d/3dic.html