An on-chip self-calibration method for current mismatch in D/A Converters

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Abstract:

This paper presents a new on-chip low-power self-calibration apparatus implemented in a 12-bit current-steering 250nm CMOS DAC. The DAC core consists of a non-calibrated binary LSB part and a calibrated thermometer MSB part. The thermometer currents are generated by combining a coarse 10-bit accurate current with a fine calibrating current provided by a small calibrating DAC (CALDAC). The magnitude of the fine current is determined in the digital domain and optimized for overall post-calibration accuracy. This digital process acquires mismatch error information from an on-chip single bit ADC. The whole calibration process is executed once at chip power-up and the calibration results are recorded. During the normal operation of the DAC, no active calibration operations are present and the fine currents are kept static, so that the advantages of calibration are maintained even at very high conversion rates. The self-calibrated DAC achieves 12-bit static and dynamic linearity, while occupying smaller silicon area due to the intrinsic 10-bit accuracy of the DAC core.

1. Introduction

Transistor mismatch of signal current sources is often the predominant error that determines the non-linearity of the static DAC transfer characteristic. This mismatch also limits the dynamic performance, e.g. SFDR or THD, since for lower conversion bandwidths the static transfer characteristic determines the DAC output frequency spectrum. To meet the linearity targets, various approaches are possible, e.g. intrinsically linear [1, 2], externally tuned [3, 4] or self-calibrated [5, 10, 11] static transfer characteristics, dynamic element matching [6], digital pre-correction combined with redundancy [7].

Intrinsically linear DACs invest sufficient design resources to achieve the target accuracy of the signal current sources, relying on the principle that the stochastic spread of a current is inversely proportional to the square root of the transistor area that generates it. [8]. Thus, to improve the accuracy of a DAC by a single bit, the area of the current source transistors should be increased by a factor of 4, [9]. Moreover, to maintain yield, over-designing the DAC is common practice. To prevent waste of resources for over-design, some DACs include correction means that partly compensate for random mismatch and process tolerances. These correction means can be controlled either off-chip or on-chip.

The externally tuned DACs have means to adjust their currents, but they lack the means to acquire information of the errors. For example, in [4] small calibrating DACs (CALDACs) are attached to every calibrated current source, adjusting it to a more accurate value. The CALDACs are externally controlled and require the end-user to implement additional off-chip self-testing and processing circuits. A further integration step is found in those self-calibrated DACs that contain not only the means to adjust the signal currents, but also contain self-testing and associated processing circuitry, e.g. [5, 10, 11]. The different calibration techniques solve different design trade-offs between silicon area, static accuracy, dynamic performance, and CMOS manufacturing process. In [5], the currents are corrected via their bias voltages, allowing very small calibration steps but the calibration voltage deteriorates at higher frequencies. In [10], a back-ground calibration is implemented correcting a large set of errors but requiring a large voltage head-room. In [11], a main DAC core is calibrated by a single parallel calibrating DAC, occupying small extra area but due to the non-identical responses of the two DACs, at higher frequencies the performance is poor. A detailed overview of the main calibration techniques can be found in [12, 13]. For example, in [13], the approach of using small CALDACs attached to every calibrated current is distinguished for its simplicity, low power, moderate chip area, and effectiveness even at higher frequencies, while as a main disadvantage of its application in [4], the off-chip self-testing and processing circuitry is pointed out.

To answer the need of a fully integrated self-calibration approach effective even at higher frequencies, this paper presents a self-calibrated 12-bit current-steering DAC that further develops the potential of [4]. The presented implementation has a fully integrated self-calibration apparatus, based on small CALDACs attached to each thermometer current source, a 1-bit ADC (a current comparator) for self-test, and an 8-state Finite State Machine (FSM) as a processing algorithm, controlling the calibration error for an optimized post-calibration spread. The 12-bit DAC only needs 10-bit intrinsic accuracy, resulting in a reduction of the area of the current sources by about a factor of 16. Through self-calibration, the DAC achieves 12-bit static linearity and SFDR around 80dB up to 5MHz signal frequency.

Section 2 explains the implemented calibration method. Section 3 presents the realized 12-bit self-calibrated current-steering DAC. Section 4 reports measurement results and conclusions are drawn in Section 5.
2. Self-calibration for current mismatch

Current mismatch is a static error. That is why the calibration routine needs to be executed only once at chip power up. This start-up approach, as shown in the high-level scheme of fig.1, is based on 3 integrated activities: self-test (1-bit ADC, a current comparator), processing algorithm (FSM), and self-calibration (small CALDACs, attached to every calibrated current, i.e. every thermometer current, \(I_{th(i)}\), in the presented implementation).

![Figure 1: High level diagram of the calibration scheme.](image1)

The full-scale of each CALDAC is determined by the expected mismatch of the coarse currents \(I_{bin(i)}\), while the CALDAC LSB step size determines the post-calibration accuracy of the calibrated currents. Note that the LSB step size, in combination with the non-calibrated currents, should be small enough to guarantee the required overall post-calibration static linearity of the DAC. A detailed analysis of this trade-off is provided in [12]. The CALDACs are capable of either sourcing or sinking currents, so that they can calibrate out either positive or negative current mismatch errors.

For error acquisition, there are a number of advantages to basing the self-test on a comparator and extending its dynamic range using multiple self-test cycles and digital circuitry (similar to a SAR or Algorithmic ADC) [7, 5, 4]. Firstly, large analog silicon area is traded for much smaller and more robust digital circuitry. Secondly, 1-bit ADCs are linear by definition. Their only problem of concern is the unavoidable input offset \(I_{off}\). To circumvent this problem, in [5] for example, \(I_{off}\) is compensated by calculating the mean of two measurements: the calibrated current versus a reference and vice versa. Note that the errors are measured in the analog domain but they are corrected for in the digital domain, which can introduce linearity errors. In the present approach, \(I_{off}\) is compensated by building the calibration scheme on two phases: phase A and phase B. A detailed FSM chart of the calibration algorithm is shown in fig.2, with P indicating the polarity (direction) of the calibrating current and X1, X2 indicating the CALDAC digital input word for the temporary current \(I_{temp}\) and the \(i^{\text{th}}\) thermometer current to be calibrated \(I_{th(i)}\).

During \(\phi A\), a temporary current source \(I_{temp}\) is calibrated to the reference current \(I_{binref}\). The unavoidable input offset \(I_{off}\) is also recorded, see Eq.1. During \(\phi B\), the reference current is substituted at the input of the comparator by the current to be calibrated \(I_{th(i)}\), inherently canceling the input offset \(I_{off}\) of the comparator:

\[
\begin{align*}
\phi A: & I_{temp} = I_{binref} - I_{off} \\
\phi B: & I_{th(i)} = I_{temp} + I_{off} = I_{binref}
\end{align*}
\]

**Eq. 1**

![Figure 2: FSM chart of the self-calibration algorithm.](image2)

Due to the two phase self-calibration routine, \(I_{off}\) is cancelled at the cost of an enlarged post-calibration spread. To minimize the post-calibration spread, the quantization error of each fine-tuning loop is controlled. The polarity check after state S3 ensures that \(I_{temp}\) is always calibrated to \(I_{binref}\) within a positive quantization error, while the check after S6 ensures that each \(I_{th(i)}\) is always calibrated to \(I_{temp}\) within a negative quantization error. These controls cancel the mean of the quantization errors and minimize the post-calibration spread.

For current-steering segmented DAC implementations, it is useful to implement the reference current as the sum of all binary currents plus one dummy LSB current and to calibrate each thermometer current source to it. This approach practically removes the DNL error in the transition of the static transfer characteristic between the binary and the thermometer parts. Furthermore, only the thermometer current sources are calibrated because a) their impact on the DAC output linearity is greater than the impact of the binary part and b) they are all nominally identical, so shared calibration resources can be used, in terms of an ADC, calibration algorithm, and instances of identical CALDACs. Note that in [14], a theoretical extension of this method is presented, which also calibrates a part of the binary currents and still shares the calibration resources.

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3. A 12-bit self-calibrated DAC

A 12-bit current-steering DAC including the presented self-calibration method is implemented in a standard 250nm 1P5M CMOS process with a power supply of 2.5V. The DAC core was designed for 10-bit accuracy. It has 6-6 segmentation and only the 63 MSB thermometer current sources are calibrated by means of 63 6-bit CALDACS. A high-level block diagram of the self-calibrated DAC scheme is shown in fig.3.

![Self-calibration DAC scheme](image)

The realized 12-bit self-calibrated DAC is shown in fig.4. The dimensions of the DAC core are 1.16mm × 0.98mm. The array of current source transistors occupies only 0.11mm²; the array of CALDACS occupies 0.18mm²; the calibration logic occupies 0.1mm².

Before and after calibration, the power consumption is 270mW. It is almost independent of the conversion speed, because the DAC core uses current mode synchronization latches, as in [2], with only the decoder being realized with differential CMOS logic. The large power consumption is mainly due to the synchronization latches while no power is dissipated in the calibration apparatus during the normal operation of the DAC.

4. Measurement results

The presented results are measured for 20mA full-scale current terminated on a 50Ω differential load resistance. Fig.5 shows static characterization of the DAC before and after self-calibration. Looking at the intrinsic INL, the random mismatch errors predominate and give INL_{max}>1.5LSB. Fig.5c shows the systematic portion of the non-linearity error, which is also corrected by the self-calibration apparatus to within INL_{max}<0.4LSB - see fig.5b and d. After calibration, the remaining errors are due to the non-calibrated binary part. However, since these represent repetitive patterns, they do not deteriorate the dynamic performance only causing higher order harmonic distortion.

![Static DAC performance at 12-bit level](image)

Fig.6a shows the frequency spectrum of the DAC output after calibration for an input signal of 5MHz (4.97MHz) at 50MS/s sampling rate. The measured SFDR is 81.41dB. Fig 6b shows the SFDR performance as a function of the input signal frequency at 50MS/s sampling rate for calibrated and non-calibrated mode. The linearity of the DAC shows around 80dB linearity for frequencies up to 5MHz. The drops of performance at some frequencies are due to non-harmonic spurs entering the signal band. These spurs are intermodulation products with digital noise around 70MHz generated by the input LVDS buffers in combination with parasitic coupling to the output. Because of this limitation, for higher frequencies, in Fig.6c it is preferred to report only the
Figure 6: a) Freq. spectrum for 5MHz@50MS/s; b) SFDR for F_s=50MS/s; c) HD3 and HD5 for F_s=1MHz.

HD3 and HD5 after calibration for 1MHz input signal and sampling rates up to 280MS/s. Nevertheless, the calibration works even at that high speeds and successfully corrects for the mismatch of the current sources.

Table 1 compares the presented work with other recently published DACs having different on-chip self-calibration schemes, as discussed in the Introduction section. The resolution of the presented DAC is only 12-bit, but its dynamic performance competes with published 14-bit DACs calibrated differently. A key advantage of the presented DAC is that it maintains the calibration for higher frequencies, because the CALDACs providing static correction currents are independent of the conversion speed and input signals, as opposed to the other two compared methods [5, 11]. Furthermore, the presented results are comparable to the background calibration of [10], where the correction currents are adapted to the operating environment and hence to the higher speeds, but at the cost of larger areas and voltage headroom.

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<tr>
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<tr>
<td>SFDR</td>
<td><a href="mailto:82dB@8.5MHz">82dB@8.5MHz</a></td>
<td>81dB@5MHz</td>
<td>84dB@100KHz</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35μm</td>
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<td>0.18μm</td>
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<td>Area</td>
<td>11.83mm²</td>
<td>1.14mm²</td>
<td>1.0 mm²</td>
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Table 1: A comparison with other DACs having different on-chip self-calibration schemes. (‘active area reported).

6. Acknowledgments

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References:

[2] Doris, K. et al., “A 12b 500MS/s DAC with >70dB SFDR up to 120MHz in 0.18μm CMOS”, ISSCC 2005.