Stochastic FinFET LER Effect and Stochastic FinFET Circuit Optimization

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Abstract—As the device scales to sub 22nm, FinFETs substitutes MOSFETs and works primarily in current technology. However FinFET integrated circuit performance suffers from great process variation, especially Line Edge Roughness effect. In this paper, we presented approach to simulate FinFET LER effects, building LER effect into current model by principle component analysis and optimizing stochastic FinFET circuit in system level. Results are given and estimate FinFET performance in chip level.

Index Terms—FinFET, LER, Line edge roughness, Principle component analysis, PCA, circuit optimization, stochastic

I. INTRODUCTION

Line edge roughness (LER) is considered to be important Lithography process fluctuation which leads a significant problem in IC manufacturing. As the device dimension continues to scale down, this effect becomes even worse and causes electrical variation in working circuit. The main source of primary circuit variability is emerged by 4 lithography mismatch, which are line edge roughness (LER), gate dielectric thickness (tox) variation, random dopant fluctuations (RDFs), and metal-gate work function (WFV)[1]. In sub 22nm technology, advanced transistor FinFETs substitutes MOSFETs to continue the scaling down[2]. The FinFETs has an ultra-thin body surrounded by three gates, which enhances the gate-control ability. This tri-gate structure releases the demand to scaling tox and high dopant, which is robust to gate dielectric variation and random dopant fluctuation. Nevertheless, due to the tri-gate structure, FinFETs suffers serious variability from LER[3].

LER is fundamental consequence of stochastic resist processing. Erosion of polymer aggregates at the edges of a resist during development has been shown to create a rough profile [4]. Most of prior works attribute LER effects on circuits to devices threshold variation. However, the affection on the circuit performance is multiple aspects, which hasn’t been systematically analyzed so far. In this paper, we analyze the LER effects of FinFETs and proposed a FinFETs system-level circuit optimization to overcome process variation and supply variation. The section I will introduce the analysis of LER effects simulation, section II will use Principle Component Analysis (PCA) to build LER effect device model. section III is the circuit optimization, and section IV is the results.

II. FINFET LER SIMULATION APPROACH

In this section, FinFET LER effect is simulated by Sentaurus TCAD tool. A 3-D FinFET structure with is built with gate length=30nm, Fin width =12nm, and Fin height=20nm and a roughness Fin width is applied. The generation approach of Fin width roughness is showed in fig.3. First, a sequence is generated in a Gaussian distribution with normal deviation equaling to . Secondly, with a cut-off frequency= 6 assumed in this LER effect, in frequency domain sequence is filtered by cutting off over cut-off frequency part [5]. In the end, energy loss in step 2 is made up. From fig.4 we can see difference between filtered sequence and original frequency.

The variation value of threshold voltage, linear threshold voltage, On-current and Off-current is gotten from this simulation.

A. Fitting process

Here I used principle component analysis (PCA) to transform device level FinFET effect to model level. The first step is model matching. Till now, no compact model and commercial model includes LER effects. Therefore, model doesn’t affect this analysis and here I use the empirical model from my EE209AS project. The fig.4 shows the fitting process.
II. SIMULATION APPROACH

B. Building LER model by using PCA

1) PCA is performed on FinFET simulation results to find the principle components. This most dominating Eigen vector represents LER affection on device performance.

2) Build sensitivity matrix. Our model has 9 parameters while I have 4 sequence of parameters ($I_{off}$, $I_{on}$, $V_t$, $V_{linear}$) with variation from FinFET simulation. So the sensitivity matrix from device parameters to our model is a $9 \times 4$ matrix.

3) Used the sensitivity to transfer the principle components of device simulation results to model. So far, we obtain the effects from LER to device model.

$$PCA_{model} \ast Sen = Eigen_{vector_{Devices}}$$

IV. CIRCUIT OPTIMIZATION

A. Model

Power model:

$$P_{TOT} = (P_{DYNN} + P_{leakage})$$

$$P_{DYNN} = \alpha_S N_{CKT} \frac{1}{2} < C > (V_H - V_L)V_{DD} \frac{1}{\beta_I D}$$

$$P_{leakage} = 1.7 \beta_{I_{off}} N_{CKT} V_{DD} W J_{off} (V_T, V_{DD}, t_{ox}, \eta, L_{CH})$$

Delay model:

$$\tau_1 = \frac{V_{DD}(C_{parasitic} + C_{wire} + C_{gateload})}{2I_{eff}}$$

$$\tau_2 = R_{wire} \left( \frac{1}{2} C_{wire} + C_{gateload} \right)$$

$$\tau_3 = L_{wire}/c/2$$
\[ \tau_4 = \left( \frac{\tau_2^{4/3}}{3} + \frac{\tau_3^{4/3}}{3} \right)^{3/4} \quad (8) \]

\[ \tau = \frac{\tau_1 + \tau_4}{0.5 + (1 - V_T/V_{DD})/(1 + \alpha)} \quad (9) \]

Tolerance model: Given a clock frequency, each path has a probability to exceed it which leads to failure. Therefore, the yield is derived as follows.

\[ q = \int_{t_{ck}}^{+\infty} \frac{1}{\sqrt{2\pi} n_1 \sigma_\tau} \exp \left[ \frac{- (t - n_1 \tau_0)^2}{2 n_1 \sigma_\tau^2} \right] dt \quad (10) \]

\[ Y = \prod_i (1 - q_i) \quad (11) \]

\[ \approx -\frac{1}{\sqrt{2\pi}} \left[ \frac{1}{u^2 (l_{\text{max}})} - \frac{1}{u^4 (l_{\text{max}})} \right] \exp \left( -\frac{u^2 (l_{\text{max}})}{2} \right) P(l_{\text{max}}) \frac{|du/dn|_{l_{\text{max}}}}{u^2 (l_{\text{max}})} \]

\( B. \text{ Optimization} \)

In the optimization process, outer loops are device parameters width, length, and threshold voltage, and the inner loop is Vdd, which is used to fulfill the power bound. In each loop, the device parameters and yield are given, and clock frequency can be calculated by the steepest descent method. The input to the optimization process is given upper power bound, and the output is the fast frequency that can be achieved under power requirement.

\( V. \text{ RESULTS} \)

In the optimization process, we consider LER effect inducing variation, supply voltage noise inducing variation and contribute other process variations (intra-die, inter-die and across-die variation) to threshold voltage variation. All of these 3 sources are independent.

The result fig.6 shows the threshold voltage distribution of FinFET with LER effects. From this figure we can find the threshold voltage has a 2% standard deviation of its nominal value.

Result fig.7 shows the leakage current distribution of FinFET with LER effects. From this figure we can find the leakage current has a 5% standard deviation of its nominal value. For the reason that the leakage current variation is exponentially related to LER effect variation, the leakage current spreads more than threshold voltage.

Result fig.8 shows the timing distribution of FinFET with LER effects. From this figure we can find the timing has a 2% standard deviation of its nominal value. This deviation makes a big loss of total yield.

Result fig.9 shows the normalized optimization result. From this curve we can see that as the power bound
decreases, clock period increase rapidly. This optimization is done under total yield equaling 0.9.

Result fig.10 shows the optimization result. As the power bound decreases, the optimizing parameter $V_{dd}$ decreases with power decreasing.

VI. Conclusion

In this paper, we presented a stochastic FinFET circuit optimization work from FinFET LER device simulation to system level. The optimization gives a best device structure in chip level and gives estimation to the performance of FinFET logic chip. This optimization process can also be used to compare different devices’ characteristics in chip-level.