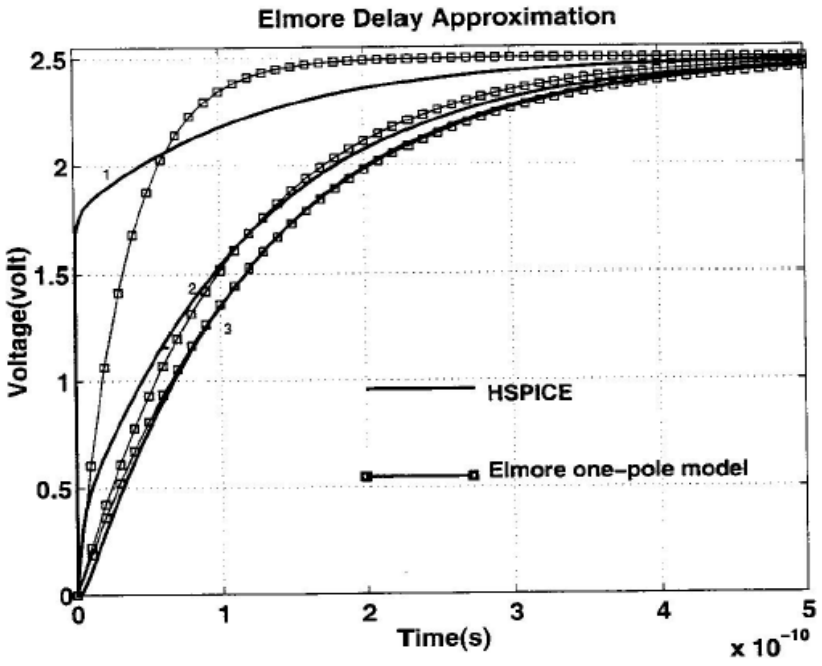
Chapter 2

Interconnect Analysis



Delay Modeling

S2P and Effective Capacitance

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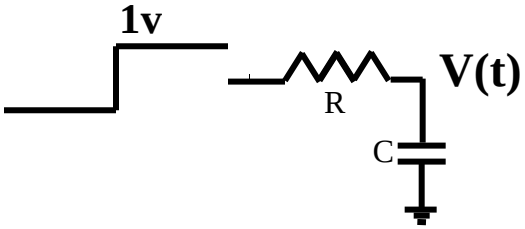
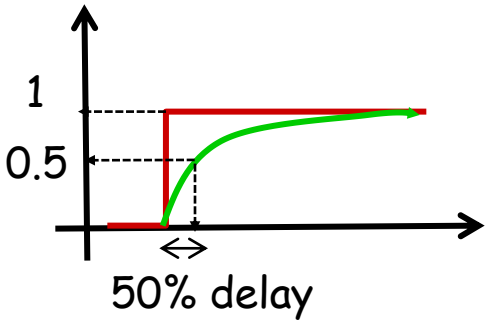
Outline

- Delay models
  - Review of Elmore Delay
  - Second Order Analysis (S2P algorithm)
  - Gate delay

Review of Elmore Delay

50% Delay for lumped RC model



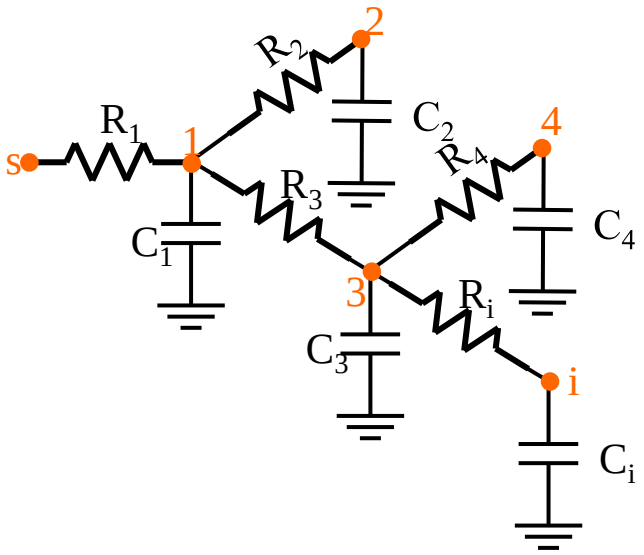


$$V(t) = 1 - e^{-\frac{t}{RC}}$$

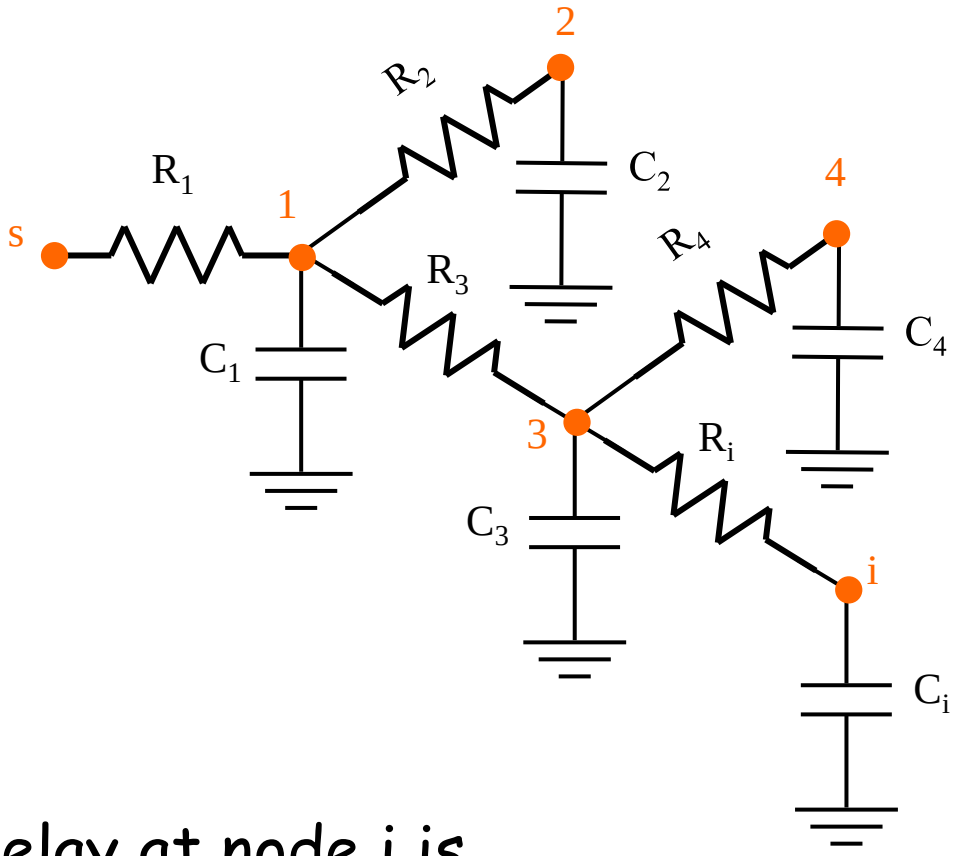
$$e^{-\frac{t}{RC}} = 0.5$$

$$t = 0.69RC$$

How about more complex circuits?



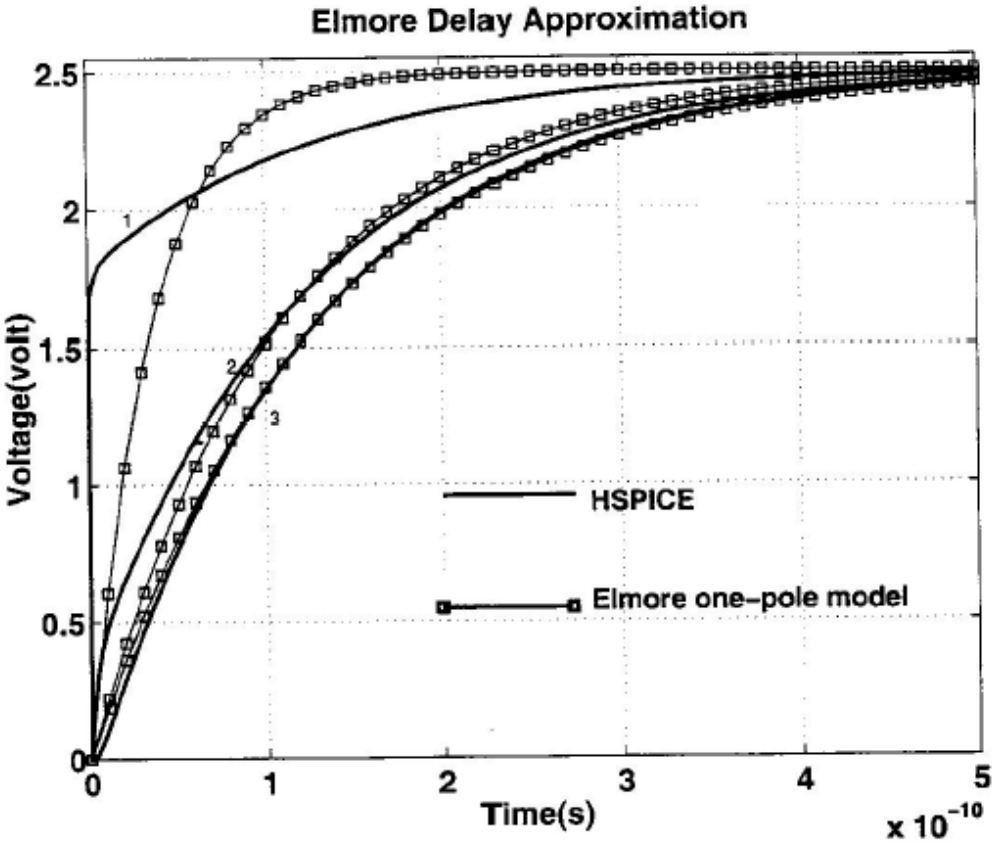
Example



- Elmore delay at node i is

$$\tau_{Di} = 0.69(R_{i1}C_1 + R_{i2}C_2 + R_{i3}C_3 + R_{i4}C_4 + R_{ii}C_i)$$
$$= 0.69(R_1C_1 + R_1C_2 + (R_1 + R_3)C_3 + (R_1 + R_3)C_4 + (R_1 + R_3 + R_i)C_i)$$
$$= 0.69(R_1(C_1 + C_2 + C_3 + C_4 + C_i) + R_3(C_3 + C_4 + C_i) + R_iC_i)$$

Elmore Delay Approximation



The Elmore delay is the metric of choice for performance-driven design applications due to its simple, explicit form and ease with which sensitivity information can be calculated

However, for deep submicron technologies (DSM), the accuracy of the Elmore delay is insufficient

Outline

- Delay models
  - Review of Elmore Delay
  - Second Order Analysis (S2P algorithm)
  - Gate delay

Alternative solution: S2P Algorithm

Second Order Analysis (Stable 2-Pole Delay Algorithm)

General Idea: MOR

Original RC network:

$$H(s), Y(s) = \sum_{n=1}^{q} \frac{k_n}{s - p_n} + k_0$$

2 poles Model: (Model Order Reduction: AWE)

$$h(s) = \frac{b_0 + b_1 s}{1 + a_1 s + a_2 s^2} = \frac{k_1}{s - p_1} + \frac{k_2}{s - p_2}$$

Generate the time domain single from 2P model:

eg:

$$\text{Impulse Response: } \hat{h}(t) = (k_1 e^{p_1 t} + k_2 e^{p_2 t}) \times u(t)$$

*Emrah Acar, Altan Odabasioglu, Mustafa Celik, and Lawrence T. Pileggi. 1999. "*S2P: A Stable 2-Pole RC Delay and Coupling Noise Metric"*. In Proceedings of the Ninth Great Lakes Symposium on VLSI(GLS '99).*

Moments of H(s)

Moments of H(s) are coefficients of the Taylor's Expansion of H(s) about s=0

$$H(s) = H_0 + s\frac{d}{ds}H(s)\Big|_{s=0} + s^2\frac{1}{2!}\frac{d^2}{ds^2}H(s)\Big|_{s=0} + s^3\frac{1}{3!}\frac{d^3}{ds^3}H(s)\Big|_{s=0} + \ldots$$

$$= m^{(0)} + sm^{(1)} + s^2m^{(2)} + s^3m^{(3)} + \ldots$$

$$m^{(j)} = \frac{1}{j!}\frac{d^j}{ds^j}H(s)\Big|_{s=0}$$

Driving Point Admittance

Let *Y(s)* be an driving point admittance function of a general RC circuit. Consider its representation in terms poles and residues

$$Y(s) = \sum_{n=1}^{q} \frac{k_n}{s - p_n} + k_0$$

where *q* is the exact order of the circuit

Moments of *Y(s)* can be written as:

$$m_i = \sum_{n=1}^{q} \frac{k_n}{p_n^{i+1}} \qquad i > 0$$

S2P Algorithm

Compute m1, m2, m3 and m4 for Y(s)

Find the two poles at the driving point admittance as follows:

$$a_1 = \frac{m_2 m_3 - m_1 m_4}{m_1 m_3 - m_2^2}, \qquad a_2 = \frac{m_2 m_4 - m_3^2}{m_1 m_3 - m_2^2} \qquad p_1 = \frac{(-a_1 + \sqrt{a_1^2 - 4a_2})}{2a_2} \qquad p_2 = \frac{(-a_1 - \sqrt{a_1^2 - 4a_2})}{2a_2}$$

To match the voltage moments at the response nodes, choose

$$k_2 = \frac{(m_0^*/p_1 - m_1^*)}{1/p_2 - 1/p_1} p_2 \qquad k_1 = (-m_0^* - k_2/p_2) p_1$$

and the S2P approximation is then expressed as:

$$\hat{h}(s) = \frac{k_1}{s - p_1} + \frac{k_2}{s - p_2}$$

Note that m_0^* and m_1^* are the moments of H(s). m_0^* is the Elmore delay.

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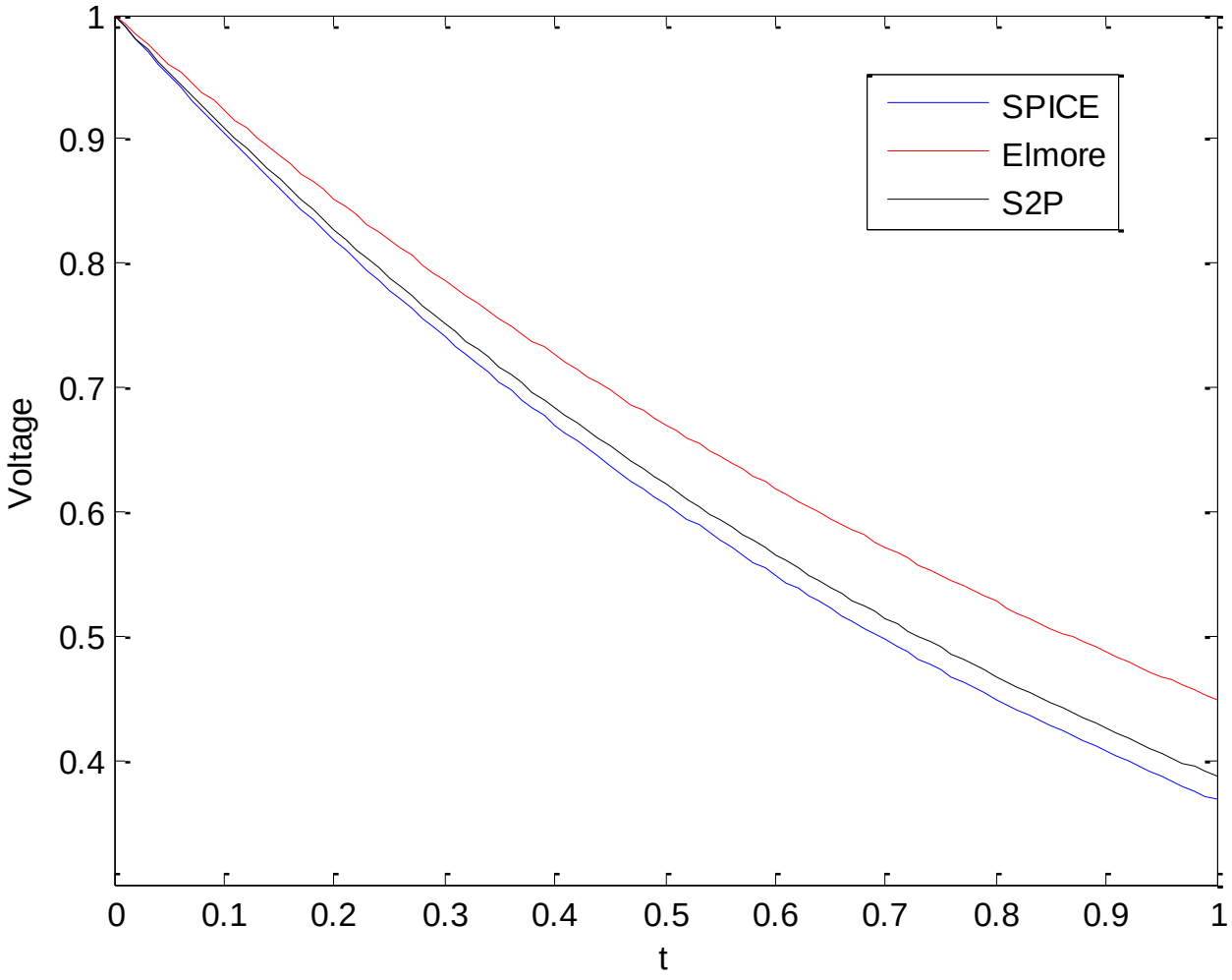
S2P Vs. Elmore Delay



Outline

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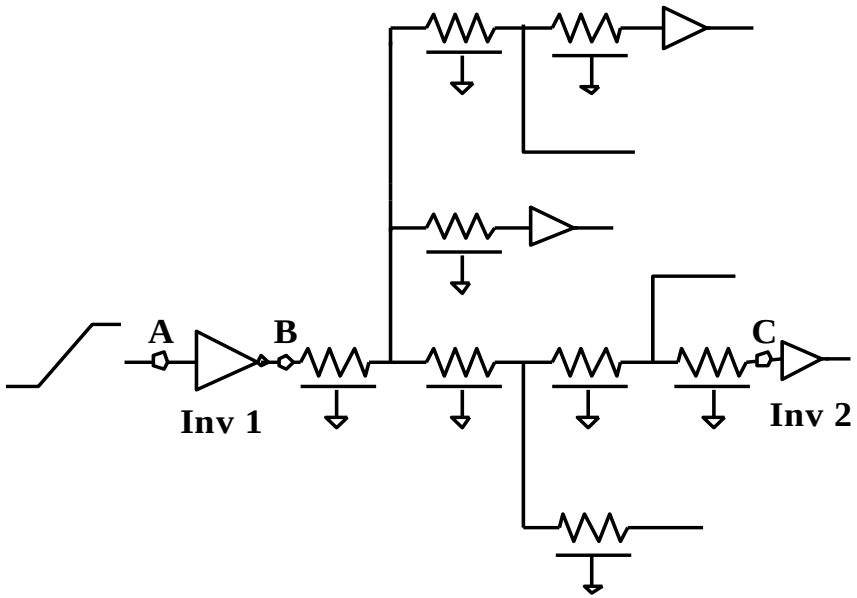
  - Review of Elmore Delay
  - Second Order Analysis (S2P algorithm)
  - Gate delay

Gate Delay

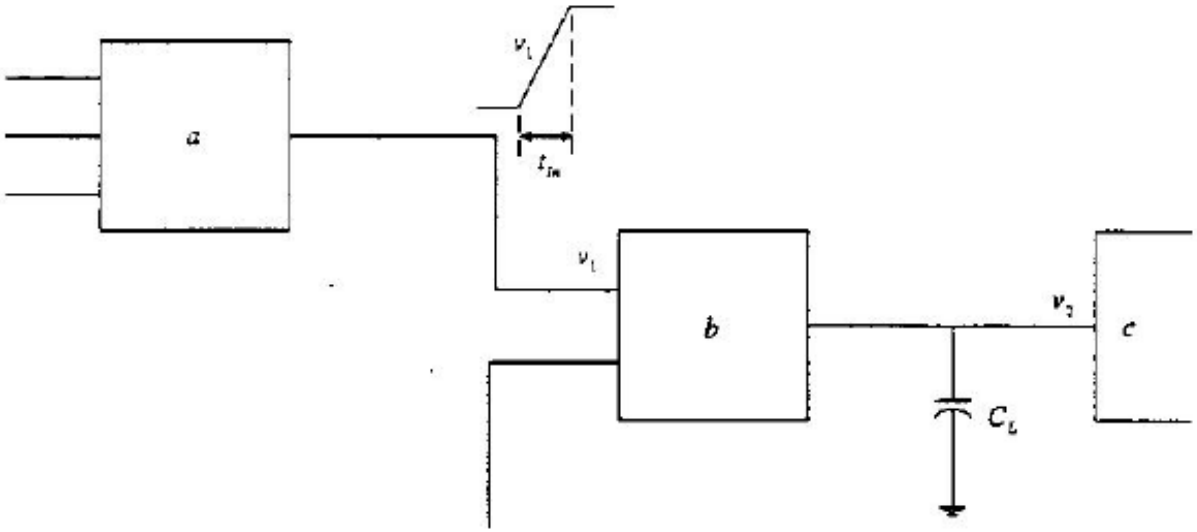
Overall flow of delay calculation

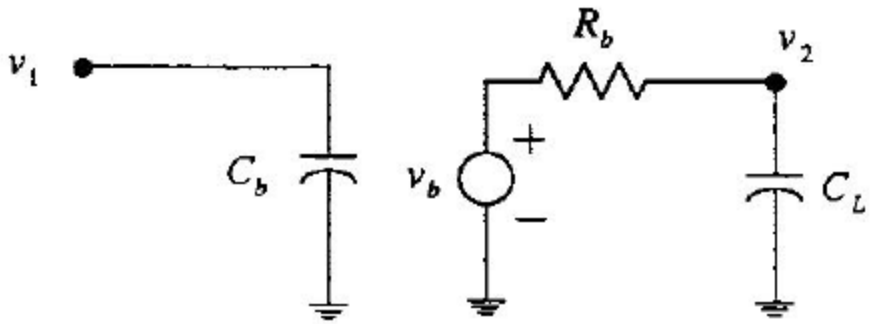


$$Delay_{AC} = Delay_{AB} + Delay_{BC}$$

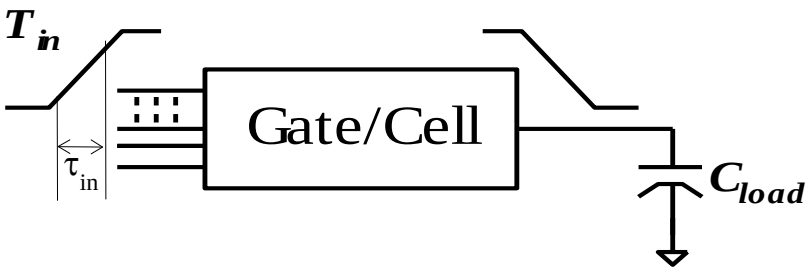
$Delay_{AB}$: Gate delay
$Delay_{BC}$: RC network delay

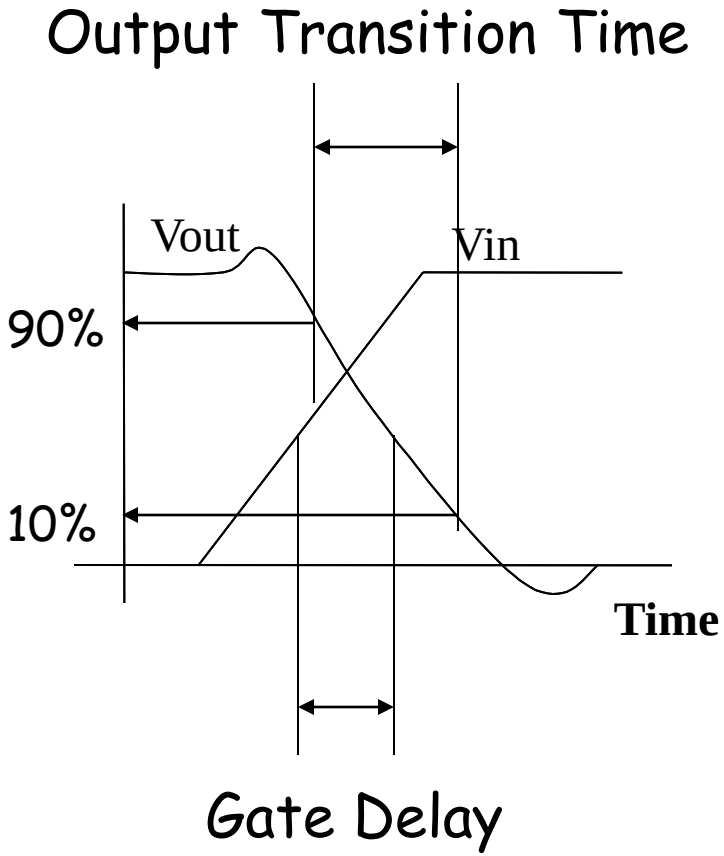
General Model of a Gate



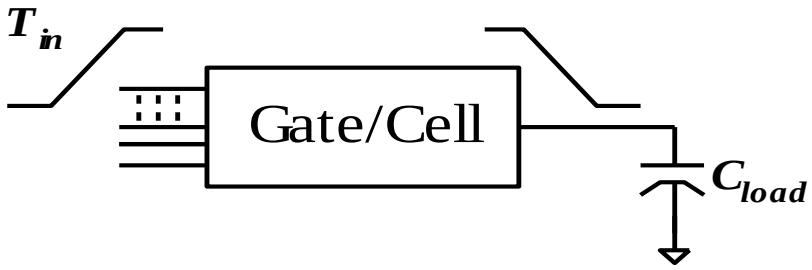


Definitions





Gate Delay and Output Transition Time

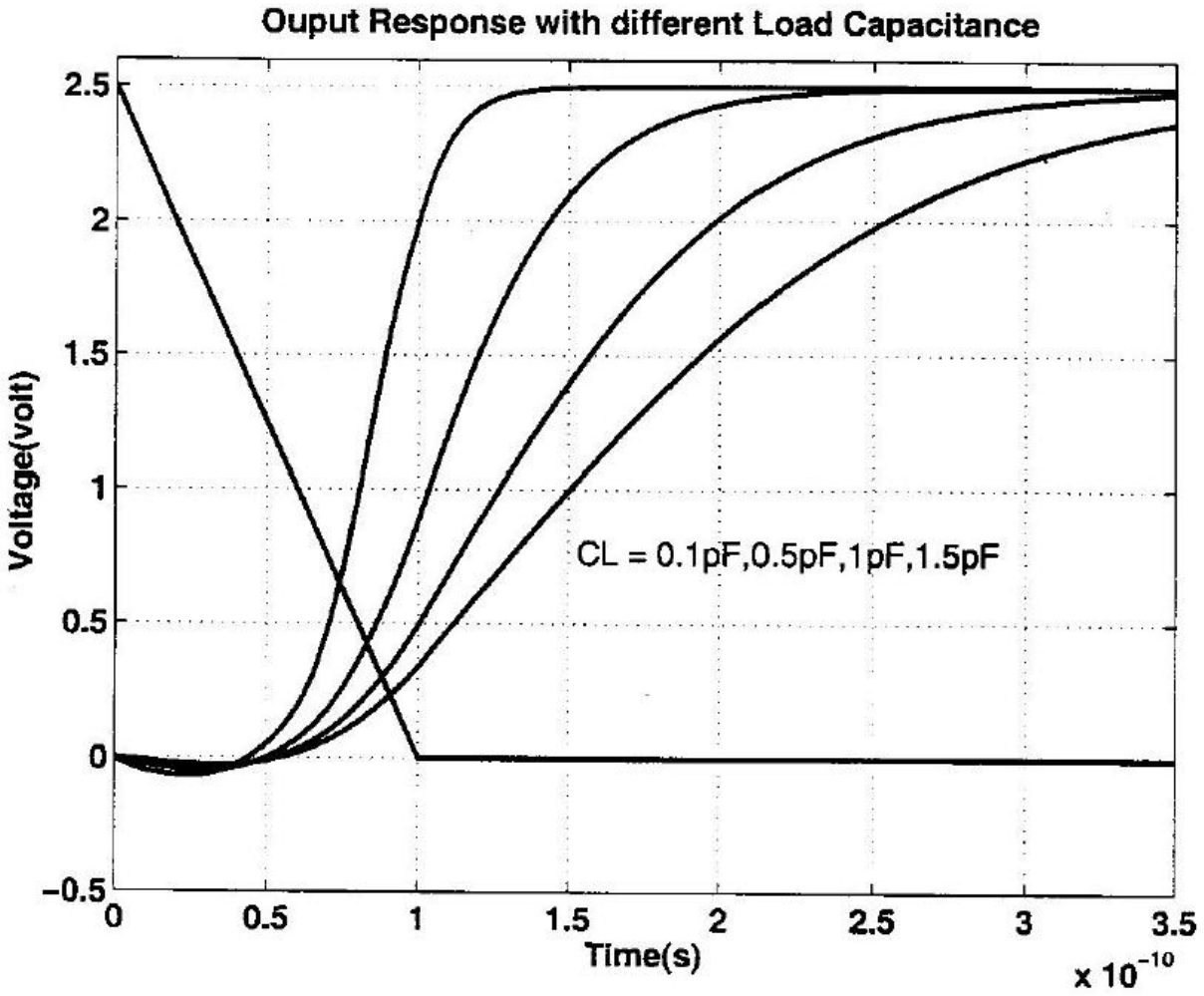


$$Gate \quad Delay = f(T_{in}, C_{load})$$

$$Output \quad Transition \quad Time = f(T_{in}, C_{load})$$

The gate delay and the output transition time are functions of both input slew and the output load

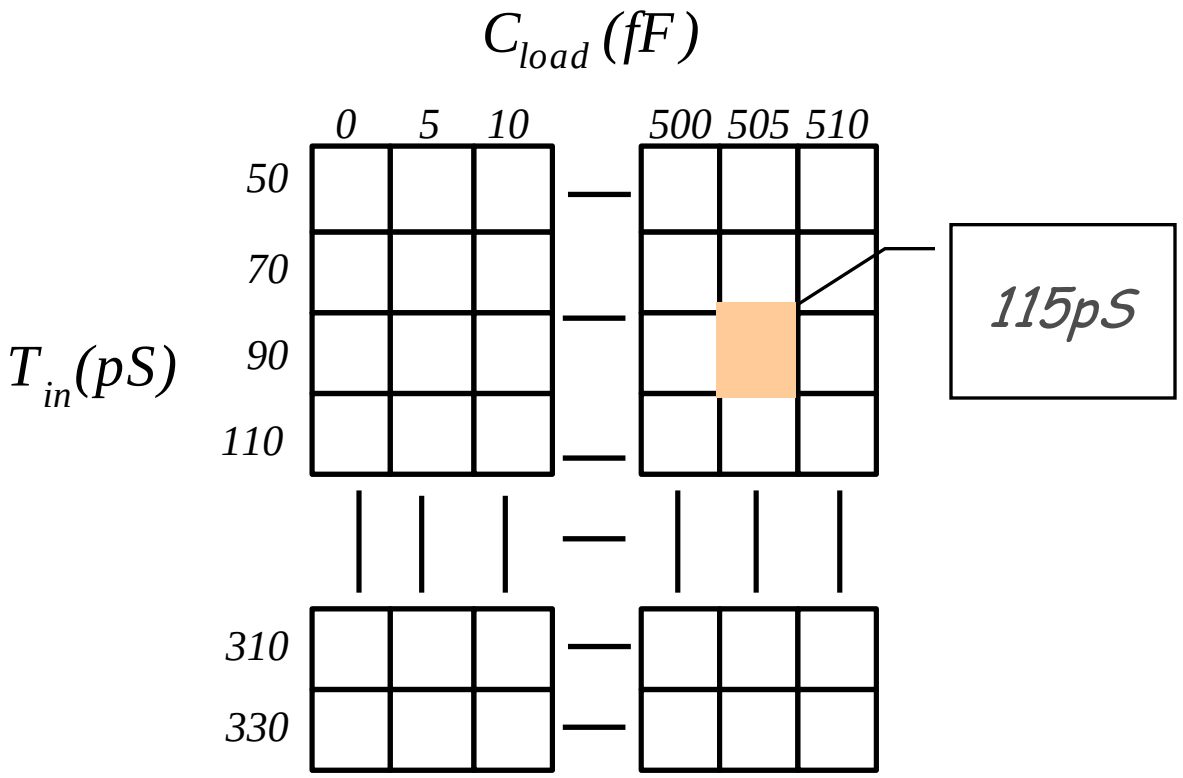
Output Response for Different Loads



ASIC Cell Delay Model

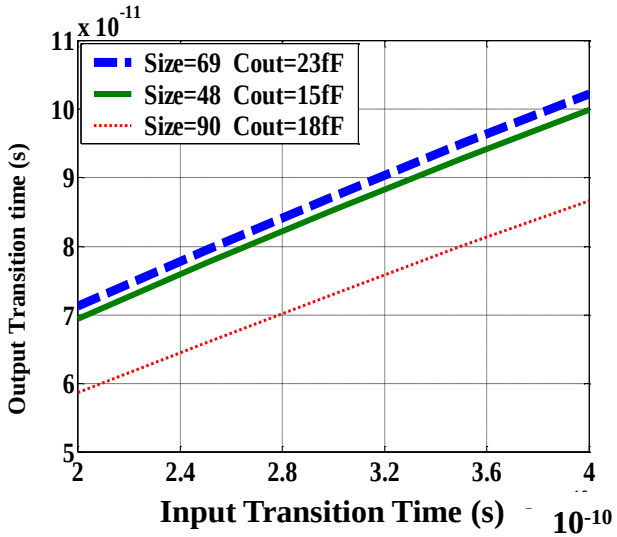
- Three approaches for gate propagation delay computation are based on:
  - Delay look-up tables
  - K-factor approximation
    - Effective capacitance
- Delay look-up table is currently in wide use especially in the ASIC design flow
- Effective capacitance promises to be more accurate when the load is not purely capacitive

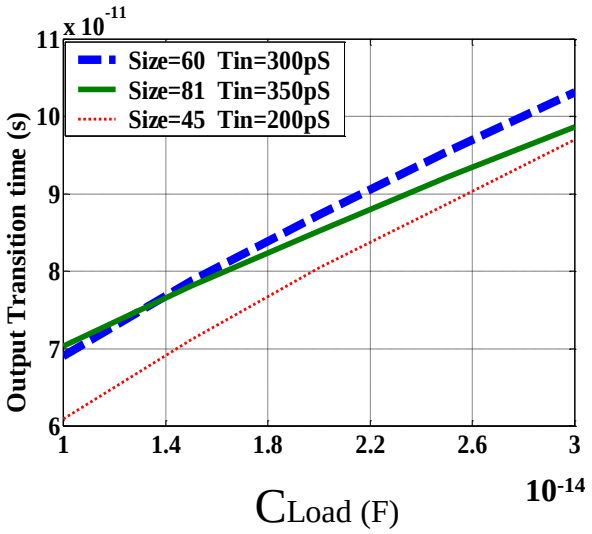
Table Look-Up Method



- What is the delay when Cl_{oad} is $505f\,F$ and T_{in} is $90pS$?

K-factor Approximation



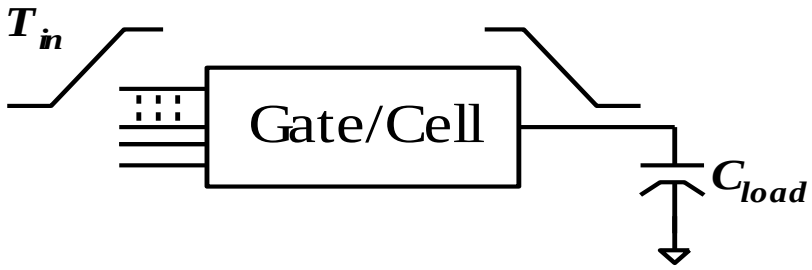


We can fit the output transition time v.s. input transition time and output load as a polynomial function, e.g.

$$T_{output} = k_1 + k_2 C_{load} + T_{in}(k_3 + k_4 C_{load}) - k_5 C_{load}^2$$

A similar equation gives the gate delay

How to calculate the C_{load}??



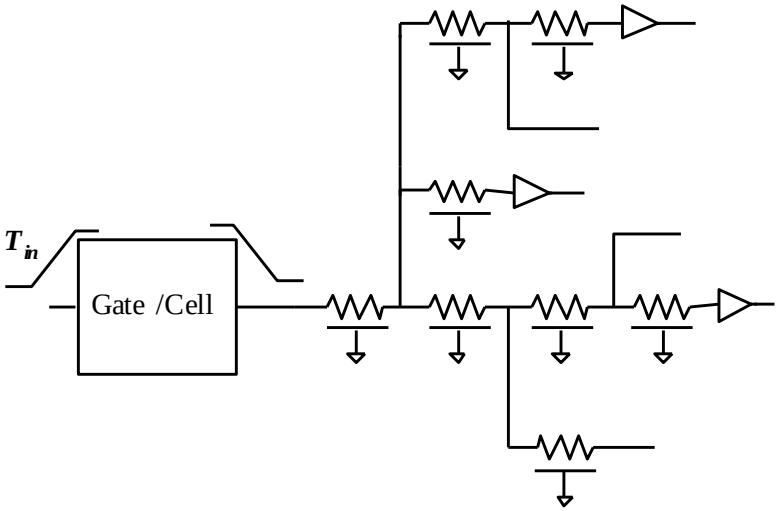
$$Gate \quad Delay = f(T_{in}, C_{load})$$

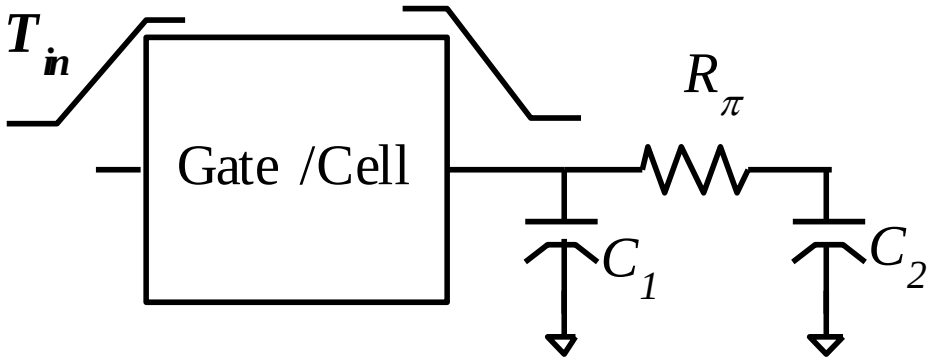
$$Output \quad Transition \quad Time = f(T_{in}, C_{load})$$

The gate delay and the output transition time are functions of both input slew and the output load

Second-order RC-π Model

- Using Taylor Expansion around s = 0



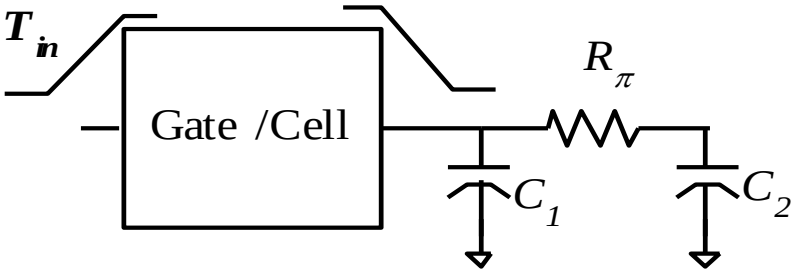


$$Y_{in}(s) = A_1 s + A_2 s^2 + A_3 s^3 + ...$$

$$\hat{Y}_{in}(s) = (C_1 + C_2)s - R_\pi C_2^{\,2} s^2 + R_\pi^{\,2} C_2^{\,3} s^3 + ...$$

$$C_1 = A_1 - \frac{A_2^{\,2}}{A_3} \qquad R_\pi = -\frac{A_3^{\,2}}{A_2^{\,3}} \qquad C_2 = \frac{A_2^{\,2}}{A_3}$$

Second-order RC-π Model (Cont'd)

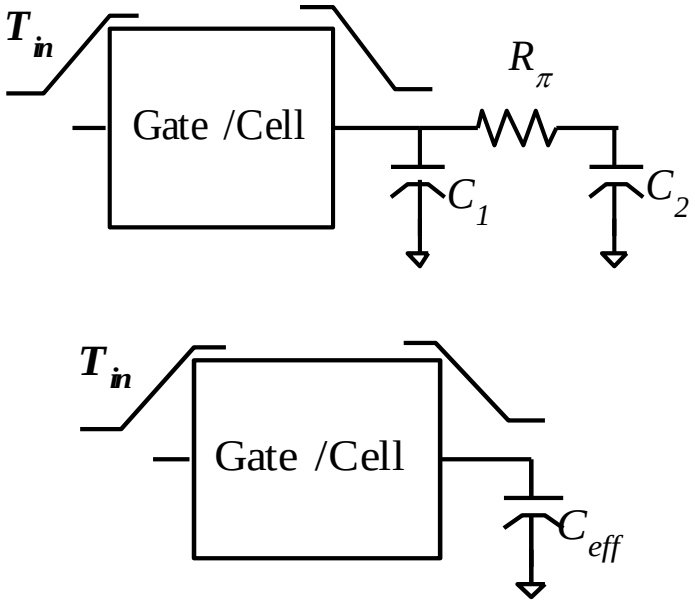


$$Gate \quad Delay = f(T_{in}, C_1, R_\pi, C_2)$$

- This equation requires creation of a four-dimensional table to achieve high accuracy

- This is however costly in terms of memory space and computational requirements

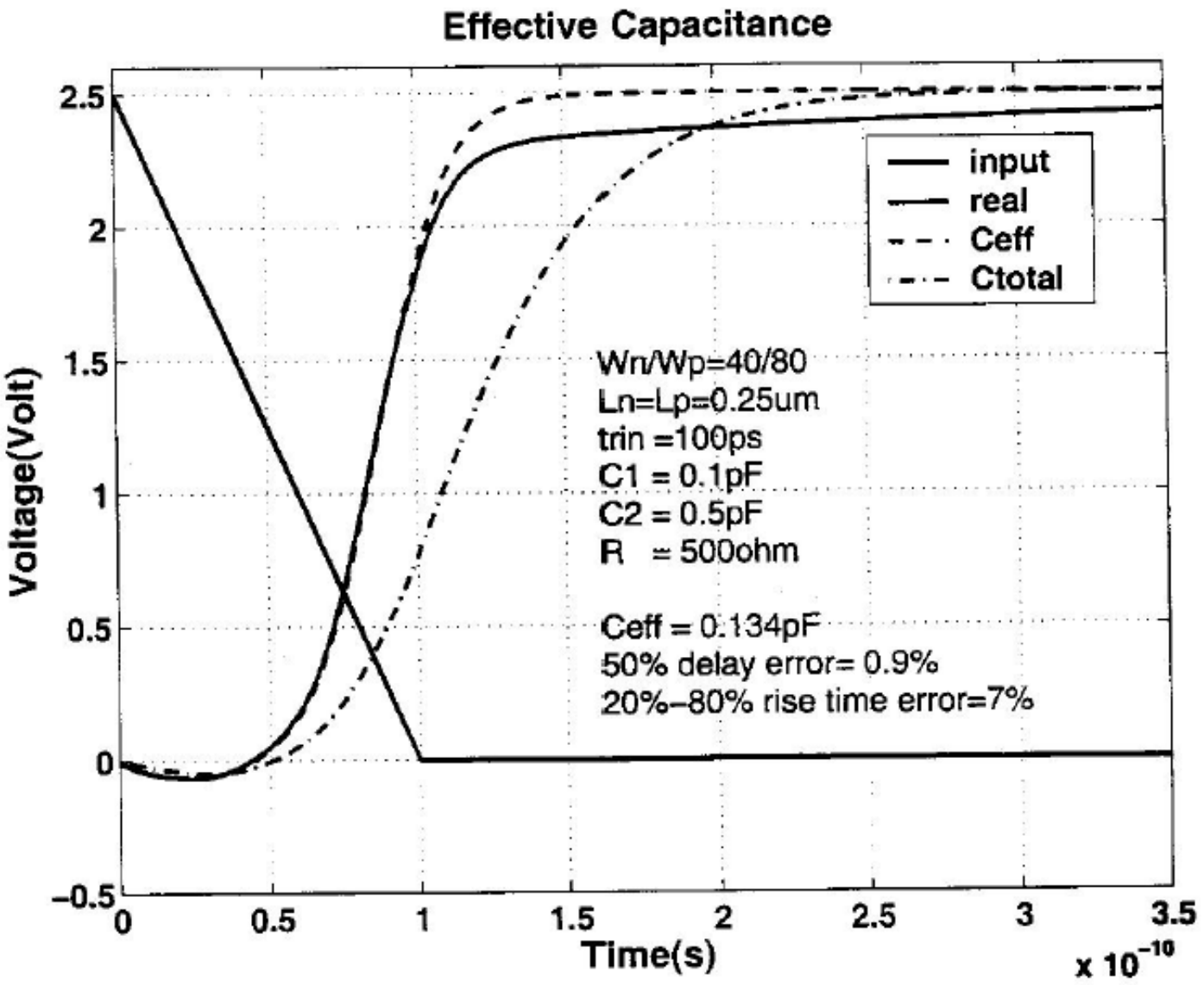
Effective Capacitance Approach



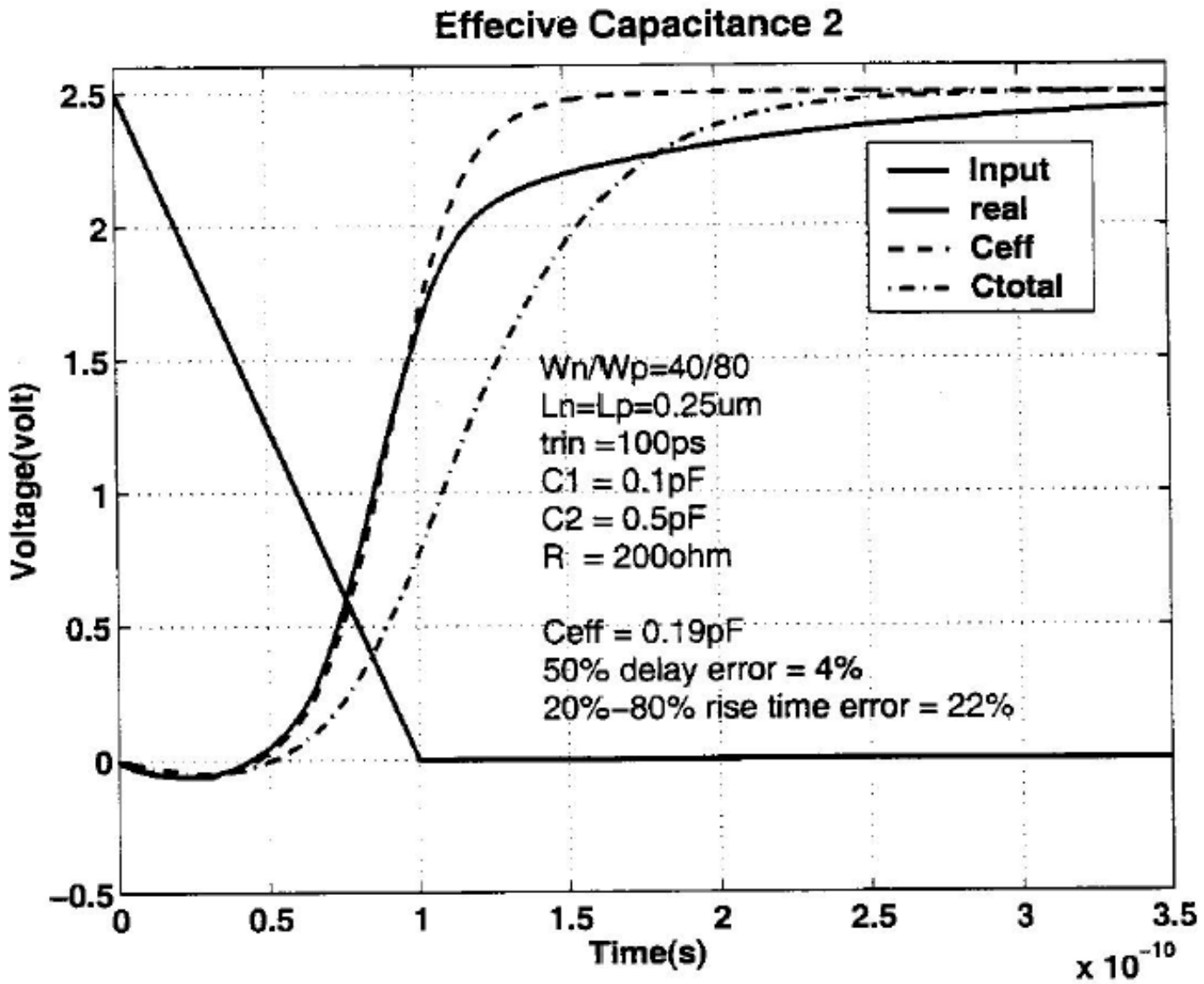
The "Effective Capacitance" approach attempts to find a single capacitance value that can be replaced instead of the RC-π load such that both circuits behave similarly during transition

What's the value of Ceff, C1+C2???

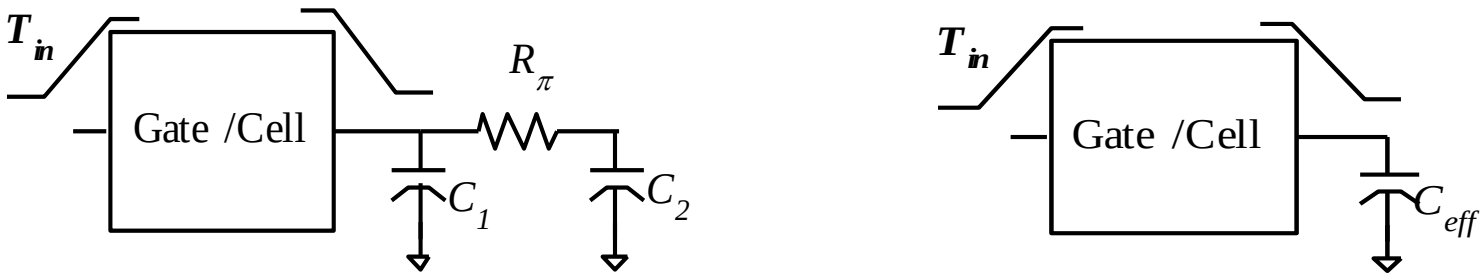
Output Response for Effective Capacitance



Effective Capacitance (Cont'd)



Effective Capacitance (Cont'd)



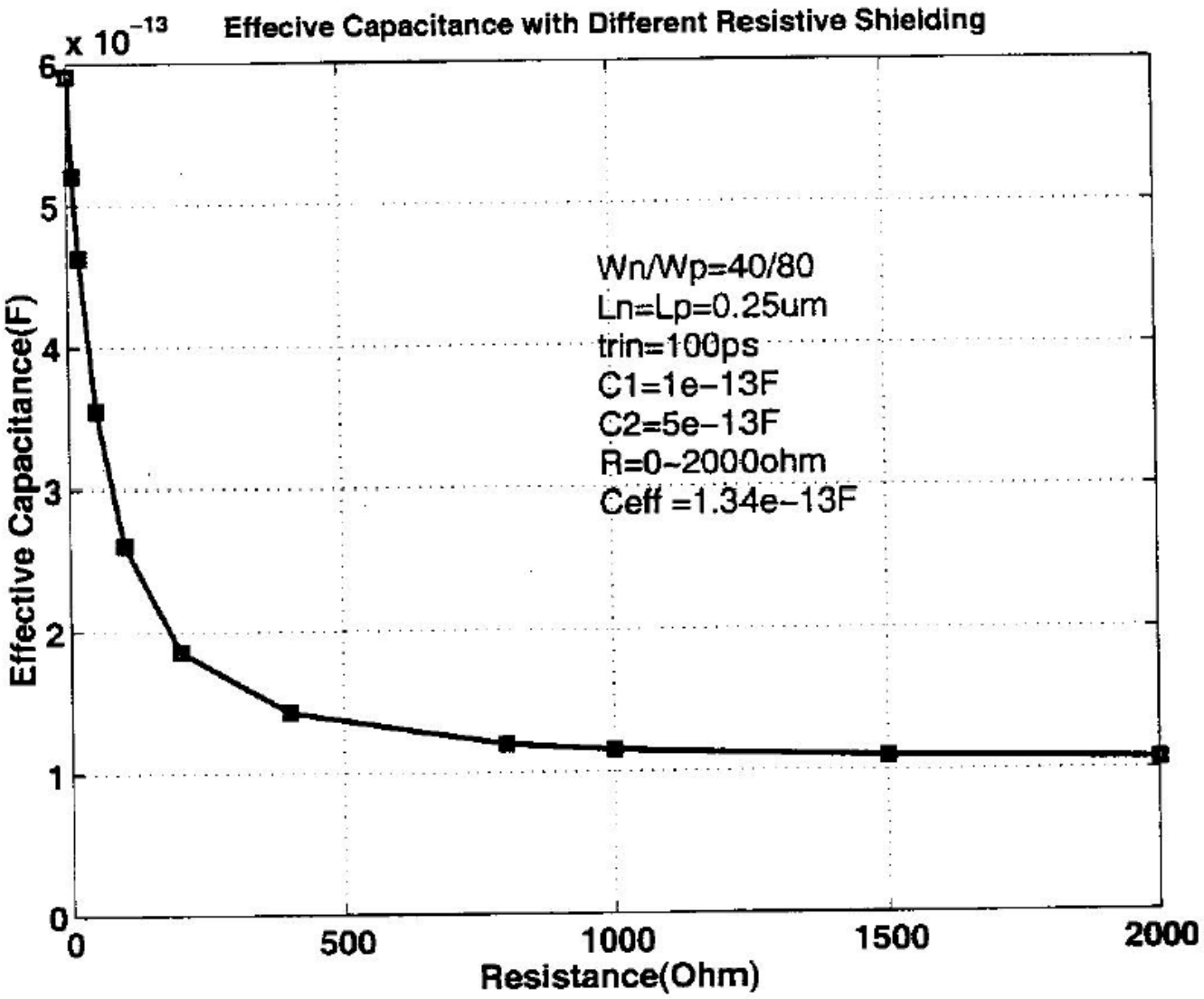
$$C_{eff} = C_1 + kC_2$$ **0<k<1**

- Because of the shielding effect of the interconnect resistance , the driver will only "see" a portion of the far-end capacitance C2

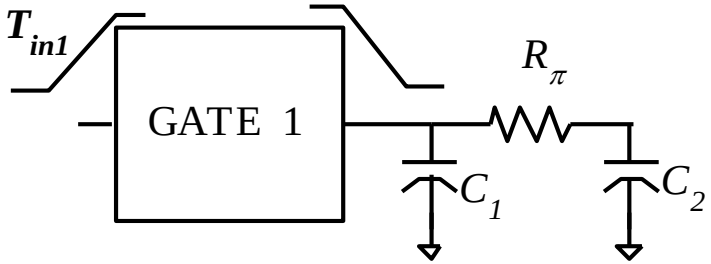
$$R_\pi \longrightarrow 0 \Longrightarrow k = 1$$

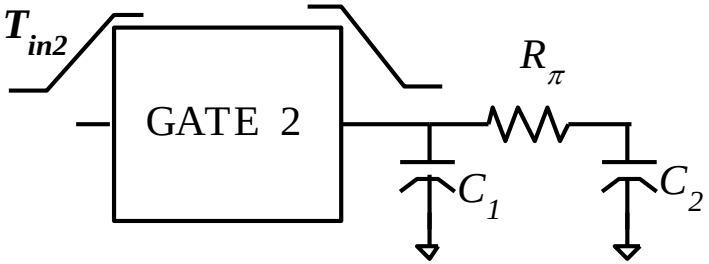
$$R_\pi \longrightarrow \infty \Longrightarrow k = 0$$

Effective Capacitance for Different Resistive Shielding



Macy's Approach





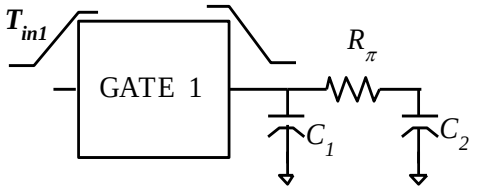
Assumption: If two circuits have the same loads and output transition times, then their effective capacitances are the same

=> the effective capacitance is only a function of the output transition time and the load

R. Macys and S. McCormick, "A New Algorithm for Computing the "Effective Capacitance" in Deep Sub-micron Circuits", Custom Integrated Circuits Conference 1998, pp. 313-316

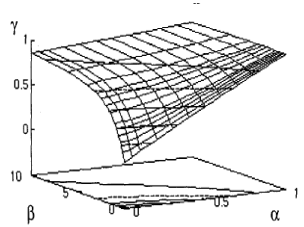
Macy's Iterative Solution

1. Compute α from C_1 and C_2
2. Choose an initial value for C_{eff}
3. Compute T_{out} for the given C_{eff} and T_{in}
4. Compute β
5. Compute γ from α and β
6. Find new C_{eff}
7. Go to step 3 until C_{eff} converges



$$\alpha = \frac{C_1}{C_1 + C_2}$$

$$\beta = \frac{T_{out}}{R_\pi C_2}$$

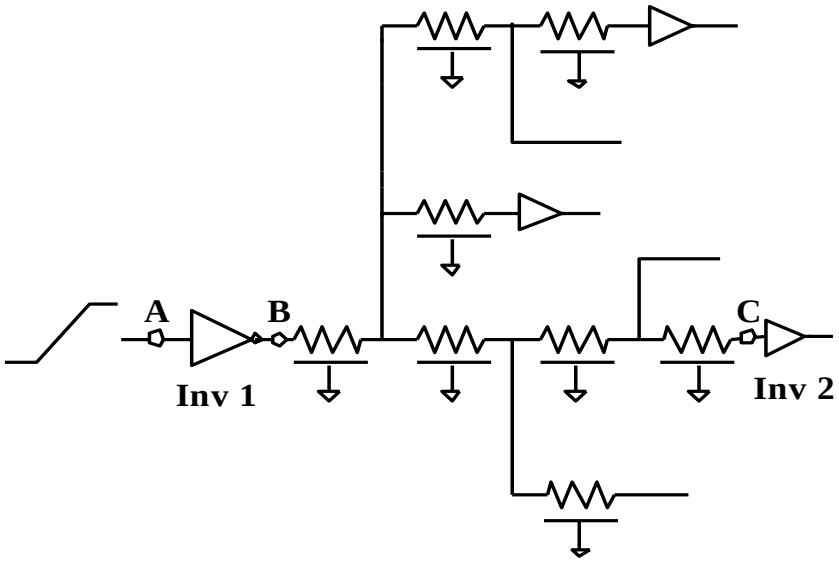


$$\gamma = \frac{C_{eff}}{C_1 + C_2}$$

R. Macys and S. McCormick, "A New Algorithm for Computing the "Effective Capacitance" in Deep Sub-micron Circuits", Custom Integrated Circuits Conference 1998, pp. 313-316

Summary

- Delay model
  - Elmore Delay model
  - S2P model
    - Reduce the RC network to a 2-pole model
    - AWE is adopted for MOR
  - Gate delay:
    - look-up table, k-factor approximation,
    - effective capacitance



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