Signal Integrity Analysis and Simulation on 3D-ICs

Nikolaos Gkolemis
Department of Electrical Engineering
University of California, Los Angeles
ngkolemis@ucla.edu

Yubo Wang
Department of Electrical Engineering
University of California, Los Angeles
ybwang@ucla.edu

***Abstract*—Signal Integrity (SI) is an important issue as dimensions keep shrinking and IC performance increasing day by day. Among the main issues of concern for SI, crosstalk between adjacent traces and Trough-Silicon Vias (TSV) is of great importance and its reduction is crucial in order to achieve a successful design. This report studies the crosstalk between channels. IC interconnection between driver and load is studied. Finally, simulation results are given based on the Multiple Transmission Line (MTL) model.**

Keywords-SI;TSV;Trace;Crosstalk;MTL Model

I. INTRODUCTION

As demands accelerate for increasing density, higher bandwidths, reduced delay and lower power, attention of IC design teams turns to 3D ICs with through-silicon vias (TSVs). 3D ICs promise “more than Moore” integration by packing a great deal of functionality into small form factors, while increasing performance, improving yield and reducing costs [1], [3]. 3D IC packages may accommodate multiple heterogeneous die—such as logic, memory, analog, RF, and micro-electrical mechanical systems (MEMS)—at different process nodes, such as 28nm for high-speed logic and 130nm for analog.

Although 3D ICs seem to be an appealing new approach to overcome problems arising from 2D IC designs, a lot of research still needs to be done in order to allow us to fully explore the problems related with them and make use of the advantages that they offer. This study aims to make 2 significant contributions. 1st analyze the effects of crosstalk over the whole transmission line so that is can be seen clearly which part of the line is affected the most and future research should focus on, and 2nd come up with an analytical model that takes as input the R,L,G,C matrixes of the circuit and computes crosstalk in a more efficient way than SPICE but still with comparable accuracy. Section II presents the concept of Signal Integrity (SI) on 3D ICs and the main issues of concern related to it. Section III presents the effects of crosstalk on TSVs and suppression techniques already proposed. Section IV discusses the method to extract the S parameter from RLGC of transmission line. It gives the general method to get the Multiple Transmission Line model. Finally Section V shows the simulation results and conclusion is drawn in Section VI.

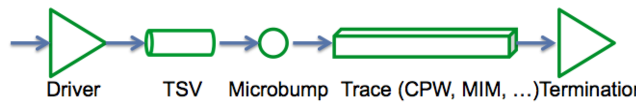


Fig.1. Complete Transmission Line Model for 3D ICs

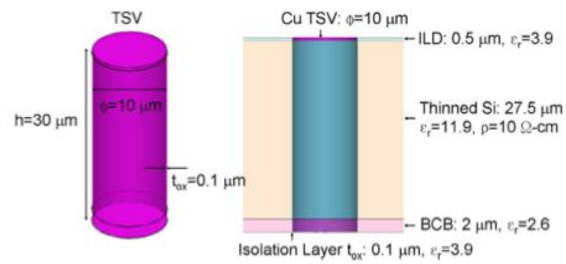


Fig.2. Typical TSV dimensions

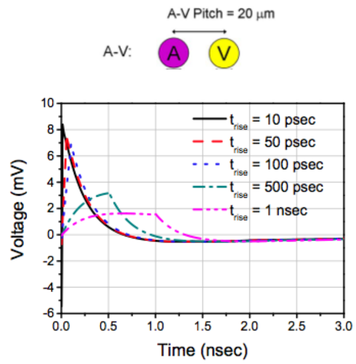
II. SIGNAL INTEGRITY AND MAIN ISSUES OF CONCERN

One big concern for every IC design is signal integrity, which refers to a set of measures of the quality of an electrical signal. Distortions on signals transmitted through TSVs and traces can be in terms of induced noise or delay. Some of the main issues of concern for signal integrity are Crosstalk, Inter-Symbol-Interference (ISI), ringing, signal loss and Power/Ground noise.

Ringing is unwanted oscillation of a voltage or current due to signal reflection. It happens when an electrical pulse causes the parasitic capacitances and inductances in the circuit to resonate at their characteristic frequency. It causes extra current to flow thereby wasting energy, delaying arrival time and can even cause unwanted triggering of some circuit’s elements. Using terminators at the ends of transmission lines, which greatly reduce signal reflections, can minimize this noise source.

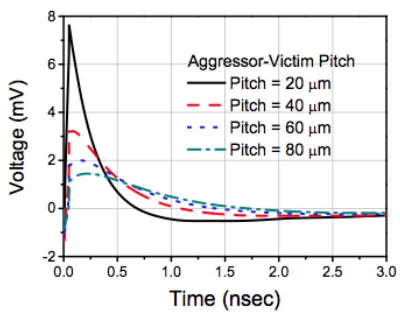
ISI is defined as a reduction in the pulse (bit) distinction, caused by overlapping energy from neighboring bits. It is caused by signal propagation though a line with lossy and dispersive properties, which induces signal waveform distortion and attenuation. The ISI strongly affects the signal shape and amplitude and in case of data transmission may also cause delay.

Power/Ground noise refers to the noise induced on the



Rise Time (psec)	10	50	100	500	1000
Noise Peak (mV)	8.40	7.63	6.91	3.27	1.62

Fig.3. Rising Time of Aggressor vs Voltage on Victim (Crosstalk Noise)



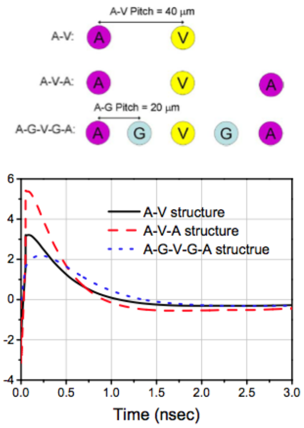
A-V Pitch (μm)	20	40	60	80
Noise Peak (mV)	7.63	3.22	2.00	1.45

Fig.4. Pitch between Aggressor – Victim TSVs vs Voltage on Victim (Crosstalk Noise).

transmission lines by the power/ground network. The parasitic resistance and inductance of the power and ground distribution networks produce voltage drops, reducing the overall voltage across the load. An efficient way to deal with this problem is the use of decoupling capacitors allocated across the die in an efficient manner. The problem is more severe in high-end ICs –like most of 3D ICs- where the ratio of signal to Power/Ground transmission lines is almost 1:1, which shows the significant effect that Power/Ground noise has on the transmission lines on these chips [4]. The reliable distribution of power and ground voltages presents a real challenge due to high current demands, reduced operation voltages and small noise margins.

Crosstalk is the undesired energy impaired into a transmission line (victim) due to signal propagations in adjacent conductors (aggressors). The magnitude of crosstalk is dependent on rise time, signal line geometry, termination and data patterns. It can change the characteristic impedance of transmission lines (TSVs & traces) and also the signal propagation velocity, resulting in adverse impacts on timings and signal integrity.

Over the last 10 years there has been substantial research on estimating crosstalk effects on traces and many techniques have been proposed that help reduce the amount of noise and delay induced by it on the victim line (Relative work in [9],



TSV Structure	A-V	A-V-A	A-G-V-G-A
Noise Peak (mV)	3.22	5.42	2.18

Fig. 5. Different TSV Network Implementations vs Voltage on Victim (Crosstalk Noise).

Victim TD	Aggressor Pulse	Victim Pulse	Aggressor Pulse
450 fsec	Off	-	Off
650 fsec	-	-	Off
250 fsec	+	-	Off
860 fsec	-	-	-
850 fsec	+	-	-
40 fsec	+	-	+

Fig. 6. Aggressors' Switching Pattern Impact on the Time Delay of the Victim Signal in an A-V-A structure (off means no switching, + positive switching 🡅, - negative switching 🡇).

[10],[11],[12]). But studying the effects of crosstalk on 3D ICs is a relative new research area with lots of publications over the last few years.

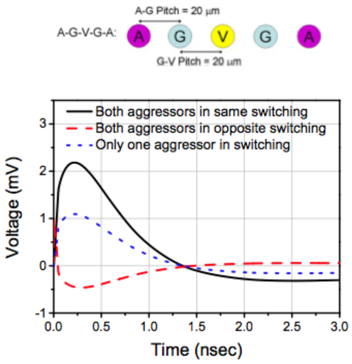
The majority of these papers studies the effects of crosstalk on TSVs and proposes ways to reduce it. But all these papers only focus on a component of 3D ICs transmission lines (TSVs) and it's behavior under crosstalk noise, failing to provide a study that fully investigates the effect of crosstalk over the whole transmission line (with is now made of the transmitter, TSV, microbump, trace and receiver, as seen in Fig.1.).

III. CROSSTALK EVALUATION AND SUPPRESSION IN TSV NETWORK

A lot of studies have been done concerning the effects and suppression of crosstalk under different TSV geometries [6], [7] and network implementations [5]. Some interesting case studies were performed in [8] and important conclusions about TSV network designs were drown. We briefly present some of these studies here.

Using the typical dimensions for TSVs (fig.2.) the effect of rise time, pitch between TSVs, insertion of guarding TSVs and switching Patterns are analyzed and presented below.

From Fig.3. we can clearly see that in order to decrease crosstalk the fast rise time devices should be avoided unless they are necessary for performance in some specific circuit parts. Enlarging the TSV pitch always reduces crosstalk noise but uses more circuit area (Fig.4.). Using guarding TSVs helps



A-G-V-G-A Switching	The Same	The Opposite	The One
Noise Peak (mV)	2.18	0.97	1.09

Fig. 7. Aggressors' Switching Pattern Impact on Victim's noise.

further reduce capacitive and inductive coupling (Fig.5.). If possible, further shorting or terminating the guarding TSVs decreases reflections, leading to a small crosstalk. Multiple aggressors increase the noise on the victim, while inserting guarding TSVs is able to compensate it. We can also observe that voltage patterns on the aggressor TSVs affect the time delay and crosstalk level of the victim TSV (Fig.6.,Fig.7.). The time delay variation of a victim TSV signal becomes large when multiple aggressors exist. Due to their importance on crosstalk noise and delay, signal switching patterns should always be taken into account during crosstalk analysis of circuits.

Four different designs of TSV networks are also examined for crosstalk suppression and results are plotted (Fig.8.).

Based on the results we can see that (a) is the best design in terms of crosstalk performance, while (c) is the worst. The reasons are that the signal TSVs in (a) are placed farthest (twice the pitch) and the ground TSVs partially isolate the "noisy" TSVs. The design in (b) has a medium crosstalk, and the performance of (d) is much better than that of (b) by adding one more line of the ground TSVs on the other side.

IV. ALGORITHM DESCRIPTION

The intent of this project is to help users study the characteristic of a channel in IC interconnect. The tool can automatically extract the jitter and noise of an eye-diagram without manual measurement. The designed user interface can also extract system response with the RLGC input only. To meet this requirement, an algorithm to extract impulse response of a certain transmission line should first be developed. The impulse response is convoluted with the input signal in time domain or multiplied in frequency domain in order to get the input response of a certain signal. And then another algorithm that automatically measures the jitter and noise of the output signal should be developed. It must been pointed out that the main matric to measure the characteristic of a channel is through eye diagram. This study is based on [13].

Transmission line characteristics are in general described by Telegrapher's equations. Consider the transmission line

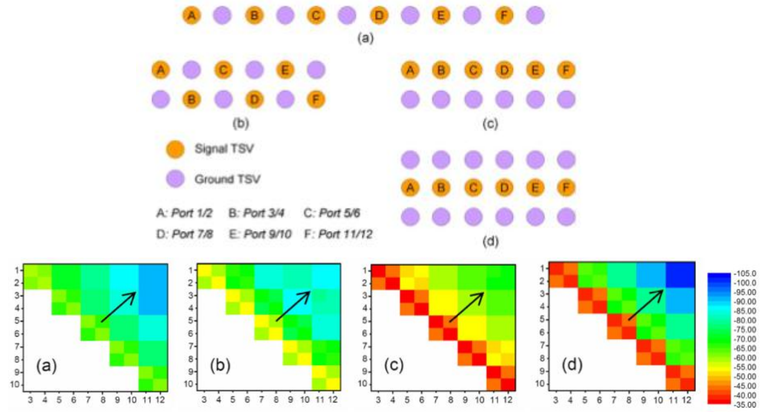


Fig.8. Different designs of TSV networks and crosstalk contours (dB) between different ports (inputs-outputs of lines) for 20GHz frequency.

system shown in Fig.9. Telegrapher's equations for such structure can be derived by discretizing the line into infinitesimal sections of length and assuming uniform parameters of resistance (R), inductance (L), conductance (G), and capacitance (C). Each section then includes a resistance (RΔx), inductance (LΔx), conductance (GΔx), and capacitance (CΔx) as show in Fig.10. Using Kirchhoff's current and voltage laws, we can write the following equation

$$v(x+\Delta x, t) = v(x,t) - R\Delta x i(x,t) - L\Delta x \frac{\partial}{\partial t} i(x,t) \quad (1)$$

Taking the limit Δx -> 0, we have

$$\frac{\partial}{\partial t} v(x,t) = -Ri(x,t) - L\frac{\partial}{\partial t} i(x,t) \quad (2)$$

Similarly, we can obtain the second transmission line equation

$$i(x+\Delta x, t) = i(x,t) - G\Delta x v(x+\Delta x, t) - C\Delta x \frac{\partial}{\partial t} v(x+\Delta x, t) \quad (3)$$

Substituting (2) in (3), we have

$$i(x+\Delta x, t) = i(x,t) - G\Delta x\left(v(x,t) - R\Delta x i(x,t) - L\Delta x \frac{\partial}{\partial t} i(x,t)\right) - C\,\Delta x \frac{\partial}{\partial t}\left(v(x,t) - R\Delta x i(x,t) - L\Delta x \frac{\partial}{\partial t} i(x,t)\right) \quad (4)$$

Taking the limit Δx -> 0, we have

$$\frac{\partial}{\partial t} i(x,t) = -Gv(x,t) - C\frac{\partial}{\partial t} v(x,t) \quad (5)$$

Taking the Laplace transform of (5) we have

$$\frac{\partial}{\partial t} V(x,s) = -(R+sL)I(x,s) = -ZI(x,s) \quad (6)$$

$$\frac{\partial}{\partial t} I(x,s) = -(G+sC)V(x,s) = -YV(x,s) \quad (7)$$

where Z and Y represent the p.u.l. (Per Unit Length) impedance and admittances of the transmission line, given by

$$Z = R + sL,\ Y = G + sC \quad (8)$$

With further deduction, one can get

$$\frac{\partial^2}{\partial x^2} V(x,s) = ZYV(x,s) = \gamma^2 V(x,s) \quad (9)$$

$$\frac{\partial^2}{\partial x^2} I(x,s) = YZV(x,s) = \gamma^2 I(x,s) \quad (10)$$

where $\gamma(s)$ is the complex propagation constant given by

$$\gamma(s) = \alpha + j\beta = \sqrt{ZY} = \sqrt{(R+jwL)(G+jwC)} \quad (11)$$

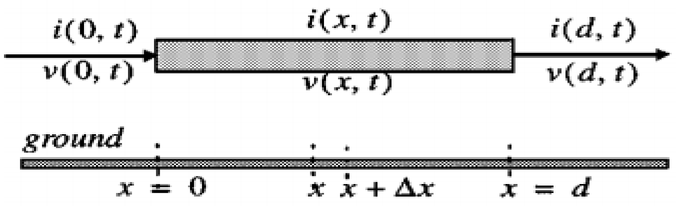


Fig. 9 Sigle transmission line

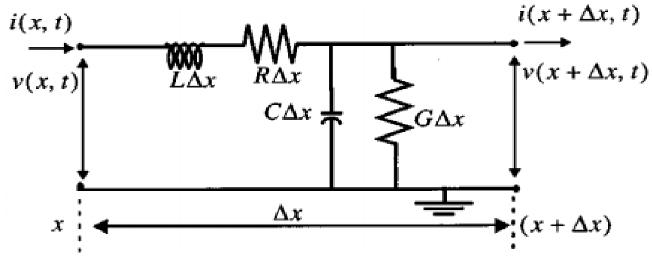


Fig.10 Abstract single transmission line

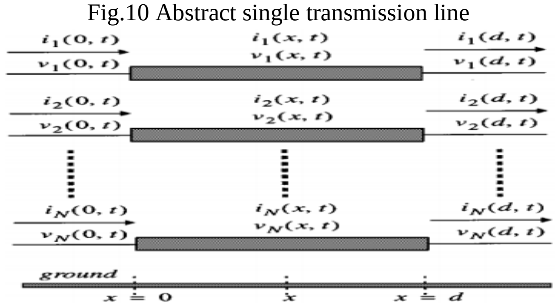


Fig. 11 Multiple Transmission Line Model

where α and β represents the real and imaginary part of the constant. The solution of (9) and (10) can be obtained as a combination of forwarded-reflected waves traveling on the line as follows:

$$V(x,s) = V(0,s)e^{\pm\gamma(s)x} \tag{12}$$

$$I(x,s) = I(0,s)e^{\pm\gamma(s)x} \tag{13}$$

If the lines are lossless, the propagation constant is given by the imaginary part of (12) only.

Consider the multi-conductor transmission line (MTL) system, with coupled conductors, shown in Fig. 11.Using steps similar to the case of single transmission line; we can derive the multi-conductor transmission line equations. Per-unit-length parameters (RLGC) in this case become matrices and voltage–current variables become vectors. We can rewrite (3) as

$$\frac{\partial}{\partial x}v(x,t) = -Ri(x,t) - L\frac{\partial}{\partial t}i(x,t) \tag{14}$$

$$\frac{\partial}{\partial x}i(x,t) = -Gv(x,t) - Cv(x,t) \tag{15}$$

The above equation can be rewritten as

$$\frac{\partial}{\partial t}\begin{bmatrix} v(x,t) \\ i(x,t) \end{bmatrix} = -\begin{bmatrix} 0 & R \\ G & 0 \end{bmatrix}\begin{bmatrix} v(x,t) \\ i(x,t) \end{bmatrix} - \begin{bmatrix} 0 & L \\ C & 0 \end{bmatrix}\frac{\partial}{\partial t}\left(\begin{bmatrix} v(x,t) \\ i(x,t) \end{bmatrix}\right) \tag{16}$$

For MTL (6)-(8) can be rewritten in a way that all parameters representing vectors. We derive a stamp relating the terminal cur-rents and voltages of MTL structures, suitable for inclusion in SPICE-like simulators. The transmission line stamp is derived through decoupling of MTL equations. Differentiating the partial differential equation is given as:

$$\frac{\partial^2}{\partial x^2}V(x,s) = -Z\frac{\partial}{\partial x}I(x,s) \tag{17}$$

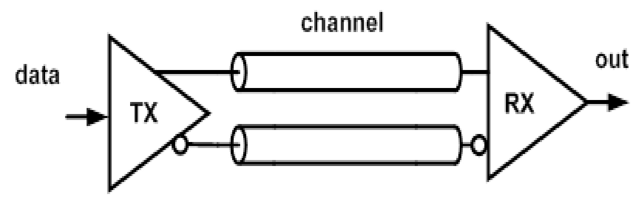


Fig.12 Simulation block

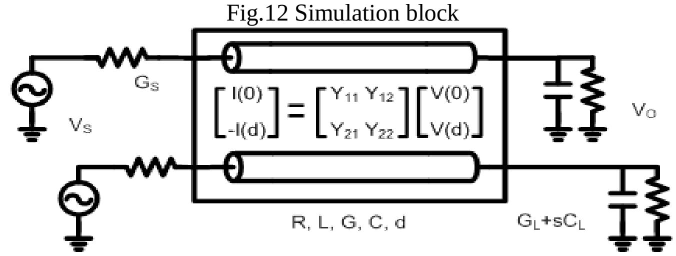


Fig. 13 Abstracted simulation diagram

$$\frac{\partial^2}{\partial x^2}I(x,s) = -Y\frac{\partial}{\partial x}V(x,s) \tag{18}$$

We can further deduct the following equations:

$$\frac{\partial^2}{\partial x^2}V(x,s) = -ZYV(x,s) \tag{20}$$

$$\frac{\partial^2}{\partial x^2}I(x,s) = -YZI(x,s) \tag{21}$$

We need further decoupling (19) (20), introduce a transformation W relating the circuit voltages V as

$$V(x,s) = WP(x,s) \tag{22}$$

where P(x, s) is the modal voltage. Hence (20) can be rewritten as,

$$\frac{\partial^2}{\partial x^2}WP = ZYWP \tag{23}$$

$$\frac{\partial^2}{\partial x^2}P = (W^{-1}ZYW)P \tag{24}$$

For effective decoupling of equations to take place, the matrix product in parenthesis must lead to a diagonal matrix as

$$W^{-1}ZYW = \begin{bmatrix} \gamma 1 & 0 & 0 \\ 0 & \ldots & 0 \\ 0 & 0 & \gamma n \end{bmatrix} \tag{25}$$

where the diagonal matrix contains the eigenvalues of the product ZY, which corresponds to the roots of the characteristic equation

$$|\gamma_k^2 U - ZY| = 0, \quad k=1,2\ldots,N \tag{26}$$

where represents the unity matrix. Having obtained the propagation constants, the solution of (24) can be written in the standard form as

$$P_k(x) = e^{-\gamma_k}c_{ki} + e^{\gamma_k}c_{kr} \tag{27}$$

where represents $P_k(x)$the kth modal voltage and c_{ki} and c_{kr} are the corresponding constants. Finally, the decoupled equation can be written as

$$\begin{bmatrix} I(0) \\ -I(d) \end{bmatrix} = \begin{bmatrix} Y11 & Y12 \\ Y21 & Y22 \end{bmatrix}\begin{bmatrix} V(0) \\ V(d) \end{bmatrix} = \begin{bmatrix} W_i E_1 W^{-1} & W_i E_2 W^{-1} \\ W_i E_2 W^{-1} & W_i E_1 W^{-1} \end{bmatrix}\begin{bmatrix} V(0) \\ V(d) \end{bmatrix} \tag{29}$$

where

$$E_1 = diag\left\{\frac{1+e^{-2\gamma_k d}}{1-e^{-2\gamma_k d}}\right\}$$

$$E_2 = diag\left\{\frac{-2e^{-2\gamma_k d}}{1-e^{-2\gamma_k d}}\right\}$$

Now we can obtain the transfer function of MTL with RLGC data only.

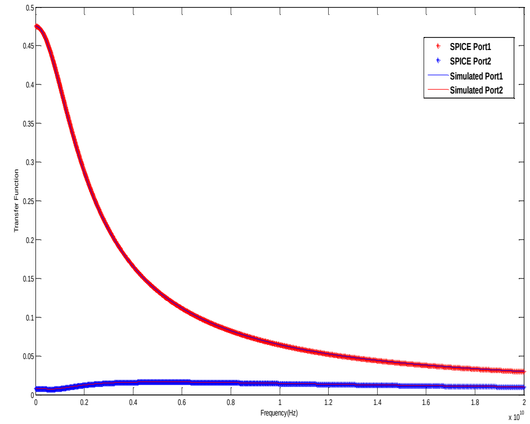


Fig. 14 Simulation results for transfer function

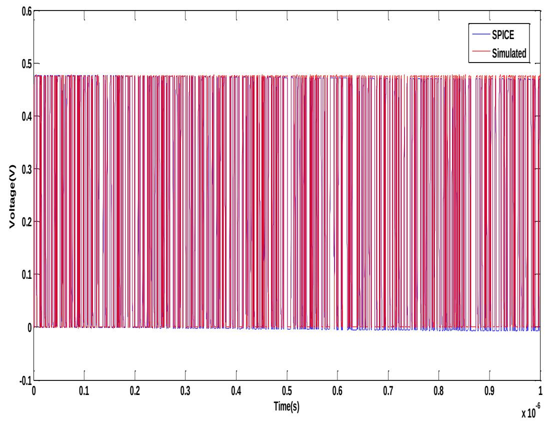


Fig.15 Comparison of simulated and SPICE results for 1000 bits

V. SIMULATION RESULTS

The simulation results for the proposed algorithm are shown in Fig.12, The case can be further abstracted as Fig.13. The simulation result in frequency domain for transfer function is shown in Fig 14,

Having this function, we can further add an input to this transfer function to show a real case study with the mentioned scenario. The simulation results for 1000 random bits are shown in the Fig. 15.

Then signal integrity problem is studied. Eye diagram of the previous 1000 signal is generated as shown in Fig. 16.

According to our algorithm, the jitter and noise should be measured automatically. Table 1 shows the measurement results for the proposed methods.

Table 1. Measurement for jitter and noise

	Jitter	Up Noise	Down Noise
SPICE	33.5ps	0.0144V	0.0144V
Simulated	51.9ps	0.0124V	0.0131V

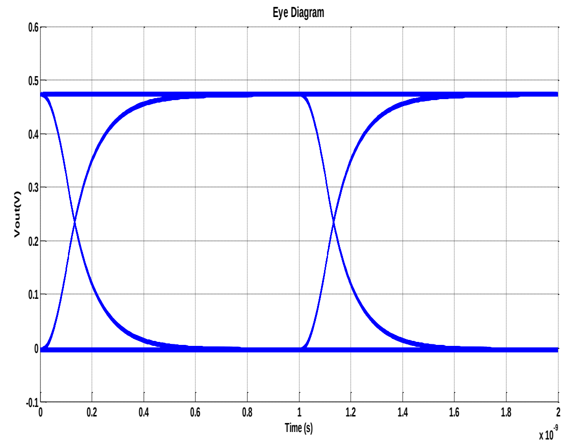


Fig. 15 Eye Diagram of 1000 random signal

The results need further improvement. The error should be result from the inaccuracy when generating the input signal in our simulation file. So the work can be further improved in the future.

VI. CONCLUSION

This report studies several important issues of SI and deeply looks into the crosstalk. Crosstalk effects on different TSV Network designs and suppression techniques are examined. A model intended to study the SI of the IC inter-connection is setup. The model of MTL is build and finally simulated with a real case. Simulation results showed the correctness of the proposed method, nevertheless, lots of improvement can be made.

ACKNOWLEDGMENT

We would like to thank Prof. He and Wei Yao for guidance.

REFERENCES

[1] Cadence While Paper, “3D ICs With TSVs – Design Challenges and Requirements”, 2010 Cadence Design Systems

[2] S.Tarzia, “A survey of 3D Circuit Integration”, 2008

[3] W.R. Davis, J.Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. M. Sule, M. Steer and P.D. Franzon, “Demystifying 3D ICs: The Pros and Cons of Going Vertical”, 2005, IEEE

[4] Y.J. Lee, M. Healy and S.K. Lim, “Co-design of Reliable Signal and Power Interconnects in 3D Stacked ICs”, 2009, IEEE

[5] C. Liu, T. Song and S.K. Lim, “Signal Integrity Analysis and Optimization for 3D ICs”, 2011, IEEE

[6] T. Song, C. Liu, D.H. Kim and S.K. Lim, “Analysis of TSV-to-TSV Coupling with High-Impedance Termination in 3D ICs”, 2011, IEEE

[7] C. Xu, H. Li, R. Suaya and K. Banerjee, “Compact AC Modeling and Performance Analysis of Through-Silicon Vias in 3-D ICs”, 2010, IEEE

[8] Z, Xu, A. Beece, D. Zhang, Q. Chen, K.N. Chen, K. Rose and J.Q. Lu, “Crosstalk Evaluation, Suppression and Modeling in 3D Through-Strata-Via (TSV) Network”, 2010, IEEE

[9] M. Cuviello, S.Dey, X. Bai and Yi Zhao, “Fault Modeling and Simulation for Crasstalk in System-on-Chip Interconnects”, in IEEE, 1999.

[10] Jun Chen and Lei He, "Determination of Worst-Case Crosstalk Noise for Non- Switching Victims in GHz+ Interconnects", in ASPDAC, 2002.

[11] Hao Yu and Lei He, "Staggered Twisted- Bundle Interconnect for Crosstalk and Delay Reduction" in ISQED, 2005.

[12] Hao Yu, Lei He and Mau-Chung Frank Chang, "Robust On-Chip Signaling by Staggered and Twisted Bundle", in IEEE, 2009.

[13] Achar,R.and Nakhla,M.S." Simulation of high-speed interconnects" Proceeding of IEEE, 2005, 89(5):693-7