FinFET sensitivity studies

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Background

• Bulk-Si MOS scaling challenges:

• As devices are scaled down, Vt variation and subthreshold swing are getting worse - Drain competes with Gate to control the channel barrier-short channel effect (SCE)

• In order to suppress SCE, heavy halo and channel doping will be required degrading carrier mobility

One solution- FinFET

- The gate controls the thin body from more than one side suppressing SHE- 3-D structure
- Process flow and layout similar to that of the conventional MOS
- Easy to scale
- Since 2011, ITRS shows FinFET and ultra-thin-body SOI as the two successor of MOSFETs
- Intel will use 3-D FinFET for 22nm
Parameter identification

- Doping
- Channel length
- Oxide thickness
- Silicon thickness
- $V_{dd}$

- To check the sensitivity of: Delay and Power consumption (static power, total power, dynamic power)
Methodology

- Model: SOI-based PTM model for FinFET
- Simulation Tool: HSPICE
- For delay, we measure the FO4 delay with 3 stages
Methodology

Power Components

\[ P = f_{\text{clk}} \int_{0}^{T_{\text{clk}}} Vdd \cdot I_{\text{supply}} \, dt \]

Dynamic Power
- capacitive switching
- short circuit power
- glitch power

Static Power
- Leakage currents
- DC standby power (e.g. pseudo-nmos circuits)

http://users.ece.gatech.edu/~jeff/ece4420/powerlecture.pdf
Methodology

- For static power consumption

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http://users.ece.gatech.edu/~jeff/ece4420/powerlecture.pdf
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Static power low output measurement  
Static power high output measurement
Methodology

• For dynamic power:
• First measure the average switching power of H-L and L-H per Clock Period (total power)

\[ E_{total_{HL}} = E_{static_{L}} + E_{dynamic_{HL}} \]
\[ E_{total_{LH}} = E_{static_{H}} + E_{dynamic_{LH}} \]

http://users.ece.gatech.edu/~jeff/ece4420/powerlecture.pdf
Static power dissipation

- Static Power vs channel length
Static power dissipation varies with channel length

- Sub threshold leakage current (VT and SS)

Fig. 10 Threshold voltage roll-off of n-channel FinFET in terms of $L_{eff}/T_{eff}$ for $V_{ds} = 0.1$ V and $L_g = 30$ nm

Fig. 6 Subthreshold swing of n-channel FinFET in terms of $L_g$ for different values of $T_{fin}$ and $V_{ds} = 1.5$ V

Static power dissipation

- Static Power vs Pnch

![Graph showing static power dissipation vs doping concentration. The graph plots static power (in aJ) on the y-axis and doping concentration (in cm^-3) on the x-axis. Two curves are shown, one labeled staticL and the other staticH, indicating different levels of static power dissipation at various doping concentrations.](image-url)
Static power dissipation varies with doping concentration

Opposite with our simulation result: probably due to random dopant fluctuation

A simple calculation: AR=5, T=30nm, H=150nm, L=45nm, V=2.025E-16cm³, less than one atom within the fin!!!

Total power and dynamic power

- Average Power per switch vs Pnch
- Dynamic Power vs Pnch

Not very sensitive
Total power and dynamic power

- Average Power per switch vs len

- Dynamic Power vs len
Simulation Results

- Input vs Output
Delay

- Delay vs \( I_{on} \) (channel resistance), load capacitance: gate capacitance and parasitic capacitance

As devices are scaled down, parasitic capacitance starts to dominate the effective capacitance.
Delay

- Delay vs Pnch
Conclusion

• Total power dissipation is not very sensitive to channel length or doping concentration
• FO4 inverter delay increases with channel length and doping concentration
• Random variation associated with the discreteness of dopant atoms needs to be carefully included into the model
• With superior control of SCE and higher driving current, FinFET is a promising solution to surmount the challenges of increasing leakage current and device-to-device variability for future high-density, low-power ICs.