SINO/SPR: SIGNAL AND POWER NET SYNTHESIS UNDER RLC MODEL

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Outline

- Overview of RLC Noise Avoidance Techniques
- Interconnect Design Considering On-Chip Inductance
  - Figure of Merit of Inductive Coupling – Keff Model
  - SINO Problem
  - SPR Problem
  - Extension of SINO/SPR under Explicit Noise Model

Noise Avoidance Techniques

- **Net Ordering (track assignment / net placement)**
  - Effective to reduce Cx coupling
    - Cx only exists between adjacent wires – short range effect
    - Place sensitive nets far away from each other can reduce/eliminate Cx noise
  - Not effective to reduce Lx coupling — a long-range effect

- **Shield Insertion**
  - Shield is a wire directly connected to Vdd or Gnd
  - Effective to reduce both Cx and Lx coupling

Figure of Merit of Inductive Coupling

- A formula-based Keff model has been developed
  - High fidelity between formula and noise voltage for SINO solutions

Problem Formulations

- Given: A set of signal nets
- Find: A minimal area track assignment P via simultaneous shield insertion and net ordering such that:
  - For SINO/NF problem:
    - P is capacitive noise free
    - P is inductive noise free
  - For SINO/NB problem
    - P is capacitive noise free
    - All nets in P have inductive noise less than a given value in terms of weighted sum of Keff

Greedy Shield Insertion

- **Shield Insertion (SI)**
  - **Insert shield when a Cx or Lx violation occurs**
  - **Results depend strongly on the initial net placement**
- **Net Ordering + Shield Insertion (NO+SI)**
  - **First remove Cx coupling by net ordering, then perform shield insertion for Lx**
  - **Results depend weakly on the initial net placement**

⇨ Separated NO+SI—simultaneous algorithm works better

Simulated Annealing SINO (SA)

- Cost Function is a weighted sum of:
  - Number of Cx violations
  - Number of Lx violations
  - Inductance Violation Figure (quantizes level of inductive noise)
  - Area of Placement
- Random Moves
  - Combine two random blocks in placement P
  - Swap two (arbitrary) random s-wires in P
  - Move a single random s-wire in P
  - Insert a shield wire at a random location in P

Experimental Results

K_{thresh}	SINO/NF	Noise Bounded		
		Greedy SI	NO+SI	SINO/SA
Net Sensitivity Rate: 40%				
1.0	8.5	15.9	5.3	4.4
2.0	6.0	13.8	3.2	3.2
Net Sensitivity Rate: 50%				
1.0	11.0	18.4	5.7	5.4
2.0	8.0	17.5	4.4	3.8
Net Sensitivity Rate: 60%				
1.0	12.0	22.1	6.0	5.8
2.0	9.0	21.5	4.3	4.1

Max. clique size in the sensitivity graph

# of shields is fewer than lower bound for SINO/NF
CPU time is much less than existing net ordering algorithms

Motivation of SPR — p-SINO Problem

- SINO problem
  - Shield can be inserted randomly at any place without pre-routed P/G wires
  - Not consider pre-routed P/G structure that are shields as well
  - How to estimate routing congestion?

- p-SINO problem
  - P/G wires are pre-routed and are shields as well
  - Signal and shielding nets are assigned to tracks not occupied by P/G wires
  - Readily solved by enhanced SA algorithm

Number of Shields in p-SINO

Sensitivity rate	Pitch size of P/G structures					
	7	8	9	10	11	12
30%	7.6/3.6	7.0/3.0	8.4/5.4	6.2/3.2	4.0/2.0	4.8/2.8
50%	8.2/4.2	7.4/3.4	6.6/3.6	5.4/2.4	5.8/3.8	5.2/3.2
70%	8.8/4.8	6.2/2.2	8.8/5.8	7.8/4.8	7.4/5.4	6.6/4.6

- Average cases for 48-bit buses
- Different P/G structures lead to different areas
- How to estimate the optimal P/G structure?

SPR Problem

- Given a number of signal nets and an inductive noise constraint
  - decides a regular P/G structure
  - assigns signal nets and shields to routing tracks
- The resulting solution has
  - a minimum area
  - shields fewer than P/G wires
  - any signal net is free of capacitive noise and its inductive noise is less than the given bound

SPR Algorithm

- Brute force solution
  - Enumerate all possible P/G structures using p-SINO algorithm
  - SPR solution is p-SINO solution w/ minimum area
- Two-phase SPR algorithm based on the interconnect estimation
  - Speculate a P/G structure based on interconnect estimation
  - Search the 1st-order neighborhood of the speculated P/G structure

Pre-SINO Estimations

- The number of shields (Ns) is a function of sensitivity rates (S), K_{th}, and number of nets (N)

Speculate Optimal P/G Structure according to pre-SINO estimations

- Optimal P/G pitch space is estimated as:

$$PS = \left\lceil \alpha \cdot \frac{N}{N_s} \right\rceil, (\alpha = 1.70)$$

- α is insensitive to noise bound
- Estimated optimal P/G structure is within 1st-order neighborhood of optimal P/G structure

SPR Solutions (48 Nets, K_{thresh}=1.0)

Sensitivity rate		P/G pitch space			Shields/g-wires	
		Estimation	SPR	Uniform P/G structure (UPG)	SPR	UPG
Uniform	30%	13	12	4	6.2/2.2	13/0
	50%	10	9	3	8.2/3.2	17/0
	70%	8	8	2	11.4/5.4	25/0
Non-uniform	Case 1	9	8	4	7.2/3.2	13/0
	Case 2	10	10	4	5.6/2.6	13/0
	Case 3	11	10	4	5.8/2.8	13/0

- SPR saves up to 1/3 area compared with UPG

Conclusions

- Developed SINO and SPR solutions under Keff models
  - [He-Lepak, ISPD'00], [Ma-He,SLIP'01]
- Extended SINO to explicit noise model
  - The noise bound is given in terms of voltage
  - [Lepak-et al, DAC'01]
- Initial extension of SPR to explicit noise model
- Incorporating SPR into a global router
  - Min-area solution under constraints of routability and RLC signal integrity