Simultaneous Shield Insertion and Net Ordering for Capacitive and Inductive Coupling Minimization

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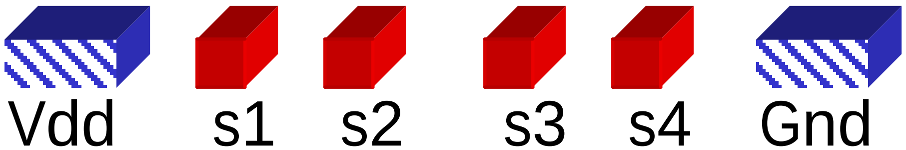
Outline

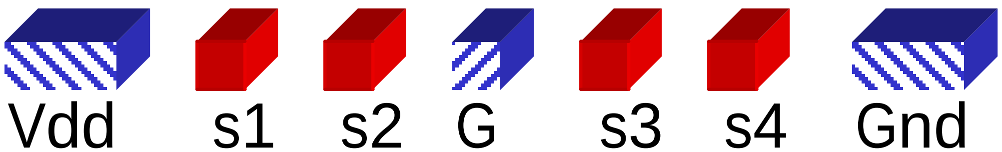
1. Previous net ordering and shielding work
2. SINO problem formulations
3. SINO problem properties
4. SINO algorithms
5. Experimental results
6. Conclusions

Interconnect Model

- Assume coplanar parallel interconnect structures (termed a "placement"),



- Noise avoidance techniques:
  - Net ordering
  - Shield insertion



Previous Net Ordering Work

- Gao, Liu: ICCAD 1993, 1994
  - ILP-based track assignment for channel and switchbox routing
- Xue, Kuh: IEEE TCAD (1997)
  - ILP-based track assignment for global routing
- Yim, Kyung: DAC 1999
  - SA-based track assignment for datapath design

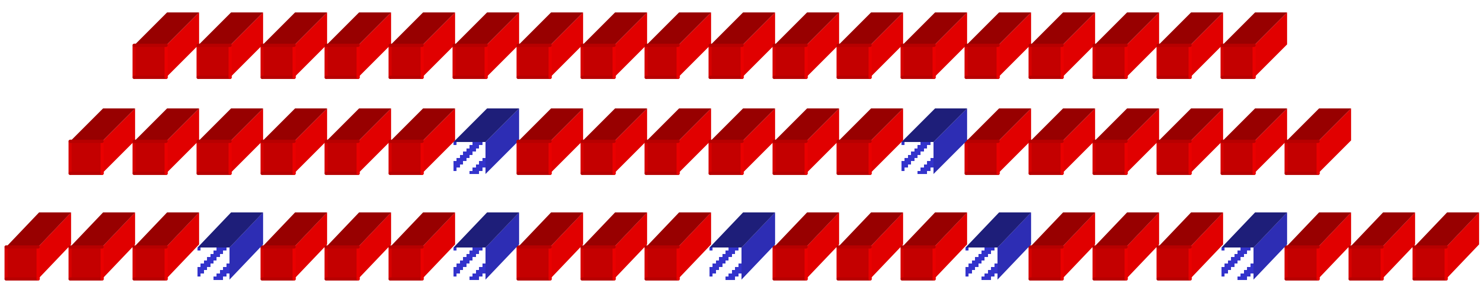
➡ Does not consider coupling to non-adjacent nets (no Lx but only Cx coupling)

Characteristics of Coupling

# of Shields	Noise (% of Vdd)
0 (a)	0.71V (55%)
2 (b)	0.38V (29%)
5 (c)	0.17V (13%)

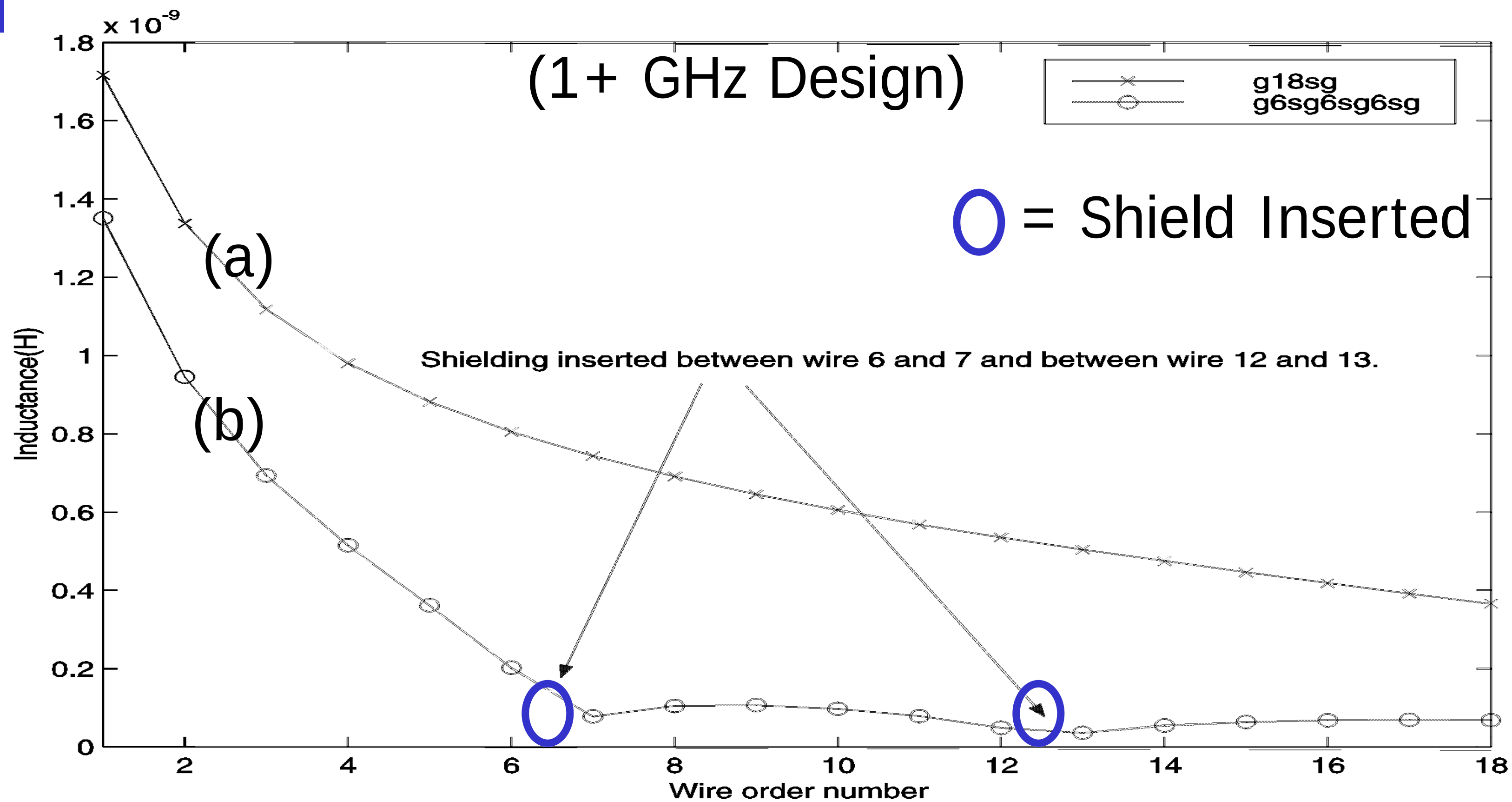
(18 bit bus structure from He et. al., CICC 1999)

(a)
(b)
(c)



- Lx coupling between non-adjacent nets is non-trivial
- Shielding is effective to reduce Lx coupling

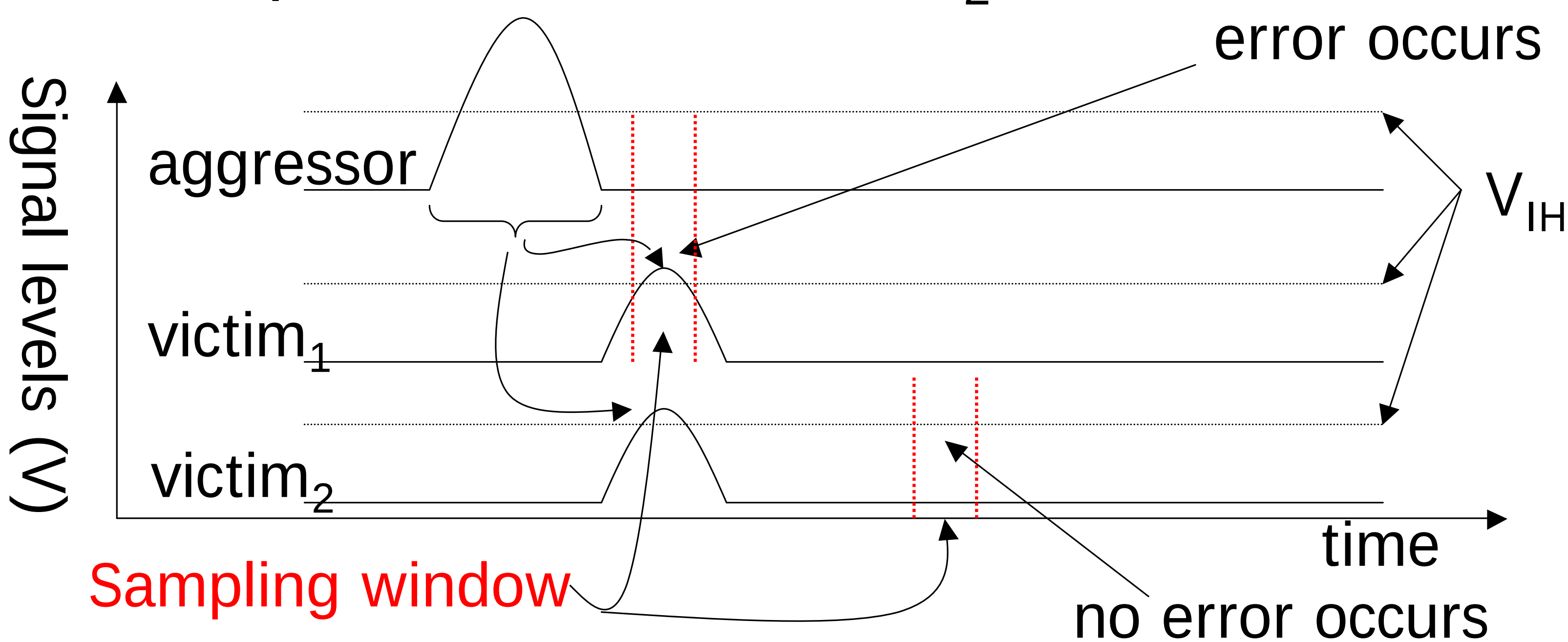
Characteristics of Inductance



Coupling inductance/noise beyond shields is negligible

Net Sensitivity

- Two nets are considered sensitive if a switching event on signal s_1 happens during a sample time window for s_2



A New Formulation

- Simultaneous shield insertion and net ordering (SINO)
  - Net ordering eliminates Cx noise
  - Shield insertion removes Lx noise

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SINO/NF Problem Formulation

- Given: An initial placement P
- Find: A new placement P' via simultaneous shield insertion and net ordering such that:
  - P' is capacitive noise free
    - Sensitive nets are not adjacent to each other
  - P' is inductive noise free
    - Sensitive nets do not share a block
  - P' has minimal area

SINO/NB Problem Formulation

- Given: An initial placement P
- Find: A new placement P' via simultaneous shield insertion and net ordering such that:
  - P' is capacitive noise free
  - ***All nets in P' have inductive noise less than a given value***
  - P' has minimal area

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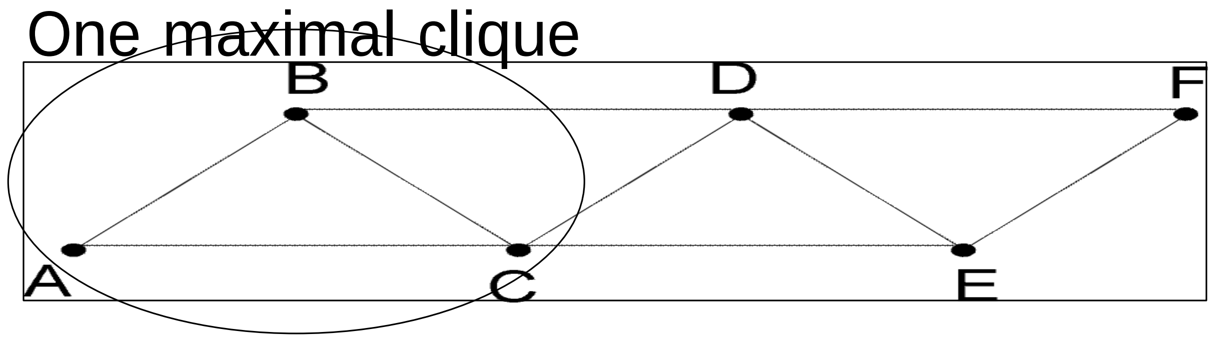
Properties of SINO Problems

- Theorem: The optimal SINO/NF problem is NP-hard
- Theorem: The optimal SINO/NB problem is NP-hard
- Theorem: The maximum clique in the sensitivity graph is a lower bound on the number of blocks required for all SINO/NF solutions

Lower Bound for SINO/NF

- Sensitivity graph: Graph indicating which nets are sensitive to one-another (vertices=nets, edges=nets are sensitive)



Sensitivity graph with clique size = 3

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Model for Inductive Coupling

- We consider inductive coupling coefficient defined as

$$K = Lij / \sqrt{L_i \bullet L_j}$$

- We use a formula-based Keff model
  - High fidelity between formula and noise voltage [He-Xu, 2000]

Greedy Shield Insertion

- Shield Insertion (SI)
  - Insert shield when a Cx or Lx violation occurs
  - Results depend strongly on the initial placement
- Net Ordering + Shield Insertion (NO+SI)
  - First remove Cx coupling by net ordering, then perform shield insertion for Lx
  - Results depend weakly on the initial placement

➡ Separated NO+SI—simultaneous algorithm works better

Graph Coloring SINO (GC)

- Our implementation: Greedy-based GC
- Can solve with other GC methods as well
- Main contributions of SINO-GC:
  - Provide lower bound measurements for SINO/NF
  - Comparative reference point

Simulated Annealing SINO (SA)

- Cost Function is a weighted sum of:
  - Number of Cx violations
  - Number of Lx violations
  - Inductance Violation Figure (quantizes level of inductive noise)
  - Area of Placement
- Random Moves
  - Combine two random blocks in placement P
  - Swap two (arbitrary) random s-wires in P
  - Move a single random s-wire in P
  - Insert a shield wire at a random location in P

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Shield Traces Required

of shields required

	SINO/NF	SINO/NB			
K_{thresh}	GC	SI	NO+SI	GC	SA
Net Sensitivity Rate: 10%					
1.0	3.2	5.0	2.8	2.0	1.8
2.0		4.2	1.2	2.0	1.0
Net Sensitivity Rate: 30%					
1.0	6.0	13.2	4.4	4.2	3.0
2.0		13.2	2.8	3.8	2.0
Net Sensitivity Rate: 60%					
1.0	13.6	22.4	5.4	8.2	5.0
2.0		22.4	4.0	8.2	3.4

SA always achieves the best result, with up to 78% improvement vs SI, 35% vs NO+SI, and 59% vs GC

Lower Bound Comparison

	SINO/NF	SINO/NB			
K_{thresh}	GC	SI	NO+SI	GC	SA
Net Sensitivity Rate: 10%					
1.0	3.2	5.0	2.8	2.0	1.8
2.0	(2.0)	4.2	1.2	2.0	1.0
Net Sensitivity Rate: 30%					
1.0	6.0	13.2	4.4	4.2	3.0
2.0	(3.8)	13.2	2.8	3.8	2.0
Net Sensitivity Rate: 60%					
1.0	13.6	22.4	5.4	8.2	5.0
2.0	(8.2)	22.4	4.0	8.2	3.4

Max. clique in the sensitivity graph

SA is even better than the SINO/NF lower bound

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Conclusions

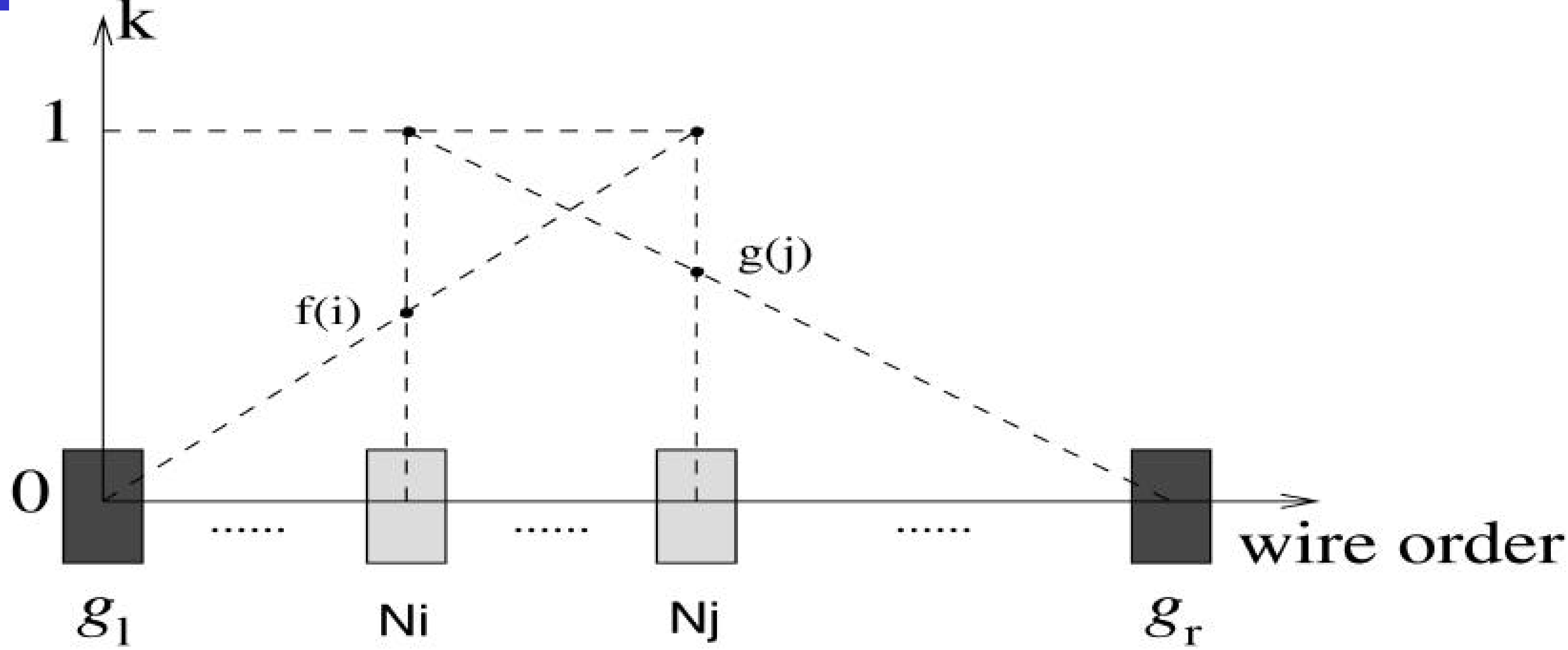
- Net-ordering is no longer sufficient when inductive coupling is considered
- We formulate the simultaneous shield insertion and net ordering (SINO) problem to minimize noise for GHz+ designs
- We present algorithms to efficiently and effectively solve the SINO problem

Ongoing Works

- SINO considering explicit noise computation in place of K_{eff} model
- Simultaneous buffer insertion, shield insertion, and net ordering
- . . .

Backup Slides

Illustration of K_{eff} Computation



$$K_{eff}(i,j) = (f(i) + g(j)) / 2$$

$$f(i) = (N_i - g_l)/(N_j - g_l); \; g(j) = (g_r - N_j)/(g_r - N_i)$$

Simulated Annealing SINO

- Temperature Adjustment
  - Set initial temperature *T* (experimentally)
  - Temperature steps are a simple multiplicative constant of current temp.
- Stopping Criterion
  - At a given *T*, stability is determined by cost variance over the last *m* moves
  - Stopping *T* (freezing point) determined experimentally