Electrical Engineering Department (Boelter Hall 6731D)
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LEI HE

EMPLOYMENT

- 2011/07-present University of California Los Angeles, CA
  Founding Director of UCLA Global Clean Energy Research Center (CERC-LA, http://cerc.ucla.edu).
  CERC-LA is an interdisciplinary research center to tackle many of the grand challenges related to the generation, transmission, storage and management of energy, involving over 20 faculty members at UCLA and is a part of UCLA Strategic Research Initiatives. It hosts an US-China Research Consortium involving many members from US and China, and was awarded US-China Ecopartnership by US Department of State and China National Development and Reform Commission in 2012.

- 2002-present University of California Los Angeles, CA
  Area Director of integrated circuits and embedded systems (2010/09-present), Full professor (2010/07-present), Associate Professor (2006/07-2010/06), Assistant Professor (2002/04-2006/06)
  1999-2002 University of Wisconsin Madison, WI
  Assistant Professor
  Teaching and research on VLSI circuits and systems, cyber-physical systems and Internet-of-Everything Systems for smart grid, electric vehicle, energy and water conservation, and health care.
  Primary investigator for projects with extramural funding of about $500,000 per year, and author of over 200 technical publications (over 5,000 citations, h-index of 36, and reprints at http://eda.ee.ucla.edu).

- 2008-present
  Guest Chair Professor with Fudan University, and visiting professor at National Taiwan University, National Tsinghua University, China National Laboratory on Optoelectronics

- 2013-present
  Co-founder of Silicon Cloud International, a startup with headquarters in Singapore and branches in US and Malaysia and working on cloud computing and internet-of-things (IoT).

- 2014-present
  Founder and Chair of Rainest Inc, a California based startup applying cloud and IoT technologies to water and energy conservation.

- 2000-present
  Consultant to various companies such as Cisco, Intel, HP, Globalfoundries, Cadence Design Systems, and Synopsys.
  Member of Technical Advisory Board for various companies such as RIO Design Automation (acquired by Magma Design Automation in 2006), Apache Design Solutions (acquired by Ansoft in 2011), Empyrean Software, and Pride Power System Technology.

EDUCATION

- 1994-1999 University of California Los Angeles, CA
  Ph.D. in Computer Science
  Dissertation: Modeling and Optimization of VLSI Interconnects

- 1986-1990 Fudan University Shanghai, China
  B.S. in Electrical Engineering
  Thesis: Fast Timing Simulation for CMOS Circuits

AWARDS

- IEEE Design Automation Conference (DAC) Top 10 Author Award for fifth Decade, 2004-2013.
- IEEE Design Automation Conference Prolific Author Award, "DAC 25 Club", 2013.
- US-China Ecopartnershp Award, US Department of State, China National Development and Reform Commission, 2012.
- IEEE Circuits and Systems Society Darlington Best Paper Award, 2011.
- Best Paper Award, the ACM Trans. on Design Automation of Electronic Systems, 2010.
- Faculty Advisor for the project winning "Best Contribution Award" in the 2008 IEEE Programming Challenge at the IEEE International Workshop on Logic and Synthesis.
- SRC Inventor Award, 2007.
- Best Paper Award, the 2006 ACM/IEEE International Symposium on Physical Design.
- Nomination of Best Paper, ACM/IEEE Design Automation Conference (DAC 2006, 2008, 2009, 2010), International Conference on Computer-Aided Design (ICCAD 2006, 2007, 2008, 2009). Less than 2% of submitted papers were nominated based on blind review first by the technical program committee and then by the award committee.
- Northrop Grumman Excellence in Teaching Award, 2005.
- IBM Faculty Partner Award, 2003.
- Faculty Advisor for Best Student Paper Award, the 2003 IEEE International Conference on Application Specific Integrated Circuits.
- UCLA Chancellor's Early Faculty Development Award (highest class), 2003.
- National Science Foundation CAREER Award, 2000.
- Distinguished PhD Award, UCLA Henry Samueli School of Engineering and Applied Science, 2000.
- Nomination of Best Paper, the 1999 IEEE Custom Integrated Circuit Conference.
- GTE Fellowship from UCLA, 1997.
- Prize for Engineering and Technology, the Dimitris N. Chorafas Foundation, 1997.

- Best Paper Award, Chinese Computer Foundation CAD/CAM Conference, 1993.
- Motorola Fellowship, Fudan University, 1992.
- Top Graduating Student Award, Fudan University, 1990.

EDITORAL BOARDS

- Associate Editor, IEEE Transactions on Design Automation of VLSI Circuits and Systems (2013-present)
- Associate Editor, IEEE Transactions on Circuits and Systems I (2008).
- Associate Editor, ACM Transactions on Reconfigurable Technology and Systems (2008 - present).
- Associate Editor, Elsevier Microelectronics Journal (2008 – 2012).

PROFESSIONAL REVIEW PANELS AND COMMITTEES

- Panelist, US National Science Foundation, Communications, Circuits and Sensor-Systems, (2012)
- Panelist, US Advanced Research Funding Agency for Energy, GENI program (2011)
- Panelist, US National Science Foundation, Multi-Core (2008), CAREER program (2001), Major Research Instrument program (2000).
- External Reviewer, Research Grants Council, Hong Kong, 2008, 2009, 2010.
- External Reviewer, KACST (i.e., National Science Agency of Saudi Arabia), 2010.
- External Reviewer, Austria Nation Science Agency, 2010.
- Member of three-person External Review Committee: five-year review of the Center for Embedded Computer Systems, University of California, Irvine (2005).

TECHNICAL PROGRAM COMMITTEE ASSIGNEMENTS

- IEEE/ACM Design Automation Conference (2004-2006, 2015), and Chair of Technical Program Subcommittee on “Beyond the Die” (2006).
- IEEE/ACM International Conference on Computer-Aided Design (2006-2008, 2010), and Chair of Technical Program Subcommittee on “System Design and Optimization” (2010).
- IEEE/ACM Asia and South Pacific Design Automation Conference, Member of Organization Committee (2006), Tutorial Chair (2006).
- IEEE/ACM International Symposium on Low Power Electronics and Design (2004-2007).
- IEEE/ACM International Symposium on Field Programmable Gate Arrays (2006-2012).
- IEEE International Conference on Field Programmable Technology (2008, 2009, 2011, 2014).
- IEEE International Conference on Communications, Circuits and Systems, Co-chair of circuits and systems track (2006-2008), and Co-Chair of Design Automation Track (2009).
- IEEE International Symposium on Circuits and Systems, CAD Track Chair, organizing and leading a technical sub-committee with over 30 members (2002).
- IEEE International Symposium on Quality of Electronic Design (2000-2004).
- IEEE International Conference on Computer Design (2003).
- IEEE Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (2003).
- IEEE International ASIC/SOC Conference (2001-2002).
- IEEE Great Lakes Symposium on VLSI Circuits and Systems (2002).

REVIWER FOR JOURNALS

- IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems.
- IEEE Transactions on Very Large Scale Integrated Circuits and Systems.
- IEEE Transactions on Circuits and Systems I, and II.
- IEEE Transactions on Electronic Devices.
- IEEE Electronic Device Letters.
- IEEE Transactions on Microwave Theory and Techniques.
- ACM Transactions on Design Automation of Electronic Systems.
- ACM Transactions on Reconfigurable Technology and Systems.
- SIAM Journal on Control and Optimization.
- Elsevier Microelectronics Journal.
- Elsevier Integration Journal.

TUTORIALS AND INVITED, PANEL OR KEYNOTE TALKS

- Keynote Speaker, "Information Technology and Intelligent Material for Water and Energy Conservation", Tsinghua University Next Generation Energy Workshop, October 2014.
- Panel Speaker, Grid Storage, Verdexchange 2013.
- Panel Speaker, "South-South Collaboration Workshop on Climate Changes", organized by China National Development and Reform Commission and World Institute of Resources.
- Keynote Speaker, "US Policy and Incentives for Smart Grid", China-Germany Workshop on Smart Grid, 2012.
- Panel Speaker, Green Technology Commercialization, Verdexchange 2012.
- Lei He, and Yiyu Shi, "Modeling and Design for Beyond-the-Die Power Integrity," embedded tutorial, IEEE/ACM International Conference on Computer-Aided Design (2010)
- Silvakumar P. Mudanai, Noel Menezes, and Lei He, "Transistor, Cell, and Interconnect Modeling: Basics to Advances," half day tutorial, IEEE/ACM International Conference on Computer-Aided Design (2006).
- Paul M. Harvey, Howard Chen, Lei He, Chung-Kuan Cheng, and Kaushik Sheth, "Surviving and Thriving in the World of Chip and Package Co-Design," full day tutorial, IEEE/ACM Design Automation Conference (2006).
- Paul M. Harvey, Howard Chen, Chung-Kuan Cheng, Manjit Borah, Lei He, and Sheldon Tan, "High Performance Interconnect and Packaging," full-day tutorial, IEEE/ACM Asia South-Pacific Design Automation Conference (2006).
- A. Devgan, S. Elassaad, and L. He, "Chip-Package Co-design," half-day tutorial, IEEE/ACM International Conference on Computer-Aided Design (2005).
- L. He, M. Hutton, Time Tuan, and S. Wilton, "Challenges and Opportunities for Low Power FPGA in Nanometer Technologies," embedded tutorial, IEEE/ACM International Symposium on Low Power Electronics and Design (2005).
- L. Daniel, L. He, and B. Krauter, "Package-Chip Co-Design: Strategies and Challenges," half-day tutorial, IEEE/ACM International Symposium on Quality Electronic Design (2005).
- H. Chen, E. Chiprout, and L. He, "Power, Timing and Signal Integrity in SoC Designs," half-day tutorial, IEEE/ACM Asia South-Pacific Design Automation Conference (2003).
- L. He and S. Lin, "Signal Integrity for High-Performance Low-Power Circuits," half-day

tutorial, IEEE International Symposium on Circuits and Systems (2002).

- L. He and S. Lin, “Interconnect Modeling and Design for Gigascale Systems-on-Chip with Consideration of Inductance,” half-day tutorial, IEEE International ASIC/SOC Conference (2002).
- J. Cong, L. He, K. Y. Khoo, C. K. Koh and Z. Pan, “Interconnect Design for Deep Submicron ICs,” embedded tutorial, IEEE/ACM International Conference on Computer-Aided Design, November 1997.

BEST PAPER AWARDS AND NOMINFATIONS

- Hao Yu, Joanna Ho and Lei He, "Allocating Power Ground Vias in 3D ICs for Simultaneous Power and Thermal Integrity" ACM Transactions on Design Automation of Electronic Systems (TODAES), May 2009. (2010 TODAES Best Paper Award)
- Manu Jose, Yu Hu, Rupak Majumdar and Lei He, "Rewiring for Robustness", DAC 2010 (Nomination for Best Paper Award)
- Zhe Feng, Yu Hu, Lei He and Rupak Majumdar, "IPR: In-Place Reconfiguration for FPGA Fault Tolerance", ICCAD 2009 (Nomination for Best Paper Award) (ppt)
- Yiyu Shi, Jinjun Xiong, Howard Chen, and Lei He, "Stochastic Current Prediction Enabled Frequency Actuator for Runtime Resonance Noise Reduction", ASPDAC 2009. (Nomination for Best Paper Award) (pdf) (ppt) Yu Hu, Zhe Feng, Lei He, and Ruapk Majumdar, “Robust FPGA Resynthesis Based on Fault Tolerant Boolean Matching,” IEEE/ACM International Conf. on Computer-Aided Design, 2008 (Nomination for Best Paper).
- Yu Hu, Victor Shih, Rupak Majumdar, and Lei He, “Mapping and Resynthesis for LUT-based FPGAs with an Efficient SAT-Based Boolean Matching,” Best Contribution Award of the IEEE Programming Contest, IEEE International Symposium on Logic and Synthesis, 2008.
- Zhen Cao, Brian Foo, Lei He, and Mihaela van der Schaar, “Optimality and Improvement of Dynamic Voltage Scaling Algorithms for Multimedia Applications,” IEEE/ACM Design Automation Conference, June, 2008, Anaheim, CA (Nomination for Best Paper).
- Yiyu Shi, Jinjun Xiong, Chunchen Liu and Lei He, “Efficient Decoupling Capacitance Budgeting Considering Operational and Processing Variations,” IEEE/ACM International Conf. on Computer-Aided Design, 2007 (Nomination for Best Paper).
- Hao Yu, Joanna Ho, and Lei He, “Simultaneous Power and Thermal Integrity Driven Via Stapling in 3D ICs,” IEEE/ACM International Conf. on Computer-Aided Design, 2006 (Nomination for Best Paper).
- Hao Yu, Yiyu Shi, and Lei He. “Fast Analysis of Structured Power Grid by Triangularization Based Structure Preserving Model Order Reduction,” IEEE/ACM Design Automation Conference, 2006 (Nomination for Best Paper).
- Jinjun Xiong, Vladimir Zolotov, and Lei He, “Robust Extraction of Spatial Correlation,” IEEE/ACM International Symposium on Physical Design, 2006 (Best Paper Award).
- L. Zhang, T. Jing, X. Hong, J. Xu, J. Xiong and L. He, “Global Routing for Performance Optimization with RLC Crosstalk Constraints,” IEEE International Conference on Application Specific Integrated Circuits, Volume 1, 21-24, pp. 191-194, October 2003 (Best Student Paper Award).
- L. He, N. Chang, S. Lin, and O. S. Nakagawa, “An Efficient Inductance Modeling for On-chip

Interconnects," IEEE Custom Integrated Circuits Conference, pp. 457-460, May 1999 (Nomination for Best Paper).

PUBLISHED BOOK

Sheldon X.-D. Tan, and Lei He, "Advanced Model Order Reduction Techniques for VLSI Designs," Cambridge University Press, pp 1-217, 2006.

PUBLISHED BOOK CHAPTERS

B8. Ming-Chun Huang, Wenyao Xu, Jason J. Liu, Yi Su, Lei He, Majid Sarrafzadeh, "Inconspicuous Personal Computer Protection with Touch-Mouse ," , ISBN: 978-3-642-39344-0, Springer Berlin Heidelberg , July 2013.

B7. Yiyu Shi, Jinjun Xiong and Lei He, "Stochastic Optimization Over Correlated Data Set: A Case Study on VLSI Decoupling Capacitance Budgeting," , ISBN: 978-953-307-829-8, InTech , February 2011.

B6. Y. Lin and L. He, "Design Methods in Sub-Micron Technologies," chapter 4 of "FPGA-Based Design and Applications," edited by Arifur Rahman and Jason Anderson, Springer-Verlag Publisher, Nov 2012.

B5. W. Liao and Lei He, "Coupled Power and Thermal Simulation with Active Cooling," Springer-Verlag Publisher, Springer Lecture Notes in Computer Science, Vol. 3164, special issue on Power Aware Computer Systems, Pages 148-163, 2004.

B4. W. Liao and L. He, "Power Modeling and Reduction of VLIW Processors," Compilers and Operating Systems for Low Power, edited by L. Benini, M. Kandemir and J. Ramanujam, ISBN: 1-4020-7573-1, Kluwer Academic Publishers, August 2003, Chapter 9, pp 155-172.

B3. L. He, "Interconnect Modeling and Design with Consideration of On-Chip Inductance," a chapter in Layout Optimizations in VLSI Designs, edited by D. Z. Du and S. Sapatnekar, Kluwer Academic Publishers, November 2001, pp. 155-190.

B2. Z. Tang, N. Chang, S. Lin, W. Xie, S. Nakagawa, and L. He, "Ramping Functional Units for Inductive Noise Reduction," a chapter in Springer Lecture Notes in Computer Science, Vol. 2008, Power Aware Computer Systems, edited by B. Falsafi and T. N. Vijaykumar, July 2001, pp. 13 -24.

B1. J. Cong, L. He and C. K. Koh, "Layout Level Optimization For Low Power," a chapter in Low Power Design in Deep Submicron Electronics, edited by W. Nebel and J. Mermet, Kluwer Academic Publishers, 1997, pp. 205-265.

PUBLISHED AND ACCEPTED JOURNAL PAPERS

J79. Wensheng Guo, Guowu Yang, Wei Wu, Lei He, Mingyu Sun, "A Parallel Attractor Finding Algorithm Based on Boolean Satisfiability for Genetic Regulatory Networks", PLOS ONE , vol.9, issue.4, April 2014.

J78. Wenyao Xu, Ming-Chun Huang, Amini, N., Lei He, Sarrafzadeh. M," eCushion: A Textile Pressure Sensor Array Design and Calibration for Sitting Posture Analysis", Sensors Journal, IEEE , vol.13, issue.10, October 2013 pp.3926-3934.

J77. Chaofan Yu, Lingli Wang, Chun Zhang, Yu Hu, Lei He," Fast Filter-Based Boolean Matchers", IEEE Embedded System Letters , September 2013, pp 65-68.

J76. Wei Wu, Fang Gong, Krishnan, R., Lei He, Hao Yu," Exploiting Parallelism by Data Dependency Elimination: A Case Study of Circuit Simulation Algorithms", Design & Test, IEEE ,

vol.30, issue.1, February 2013 pp.26-35 (pdf)

J75. Wei Wu, Fang Gong, Rahul Krishnan, Hao Yu, Lei He," Exploiting Parallelism by Data Dependency Elimination: A Case Study of Circuit Simulation Algorithms", IEEE Design and Test of Computers, wol. 30, issue. 1, February 2013 pp. 26-35.

J74. Fang Gong, Sina Basir-Kazeruni, Lei He, Hao Yu, "Stochastic Behavioral Modeling and Analysis for Analog/Mixed-Signal Circuits", IEEE Trans. on CAD of Integrated Circuits and Systems, vol. 32, issue. 1 January 2013 pp 24-33

J73. Sina Basir-Kazeruni, Hao Yu, Fang Gong, Yu Hu, Chunchen Liu, Lei He," SPECO: Stochastic Perturbation based Clock tree Optimization considering temperature uncertainty",Integration, the VLSI Journal , vol.46, issue.1, January 2013 pp.22-32

J72. Naifeng Jing, Ju-Yueh Lee, Zhe Feng, Weifeng He, Zhigang Mao, Lei He" SEU Fault Evaluation and Characteristics for SRAM-based FPGA Architectures and Synthesis Algorithms", ACM Transactions on Design Automation of Electronic Systems (TODAES) ,vol. 18, issue. 1, December 2012 Article No.13

J71. Fang Gong, Hao Yu, Lingli Wang, Lei He, "A Parallel and Incremental Extraction of Variational Capacitance With Stochastic Geometric Moments", IEEE Trans. VLSI Syst , vol.20, issue.9, September 2012 pp.1729-1737

J70. Lerong Cheng, Fang Gong, Wenyao Xu, Jinjun Xiong, Lei He, Majid Sarrafzadeh, "Fourier Series Approximation for Max Operation in Non-Gaussian and Quadratic Statistical Static Timing Analysis", IEEE Trans. VLSI Syst , vol.20, issue.8, August 2012 pp.1383-1391

J69. Lerong Cheng, Wenyao Xu, Fang Gong, Yan Lin, Ho-Yan Wong, Lei He," Statistical Timing and Power Optimization of Architecture and Device for FPGAs", ACM Transactions on Reconfigurable Technology and Systems , vol.5, issue.2, June 2012

J68. Fang Gong, Wenyao Xu, Jueh-Yu Lee, Lei He, Majid Sarrafzadeh" NeuroGlasses: A Neural Sensing Healthcare System for 3-D Vision Technology", IEEE Transactions on Information Technology in Biomedicine , vol.16, issue.2, March 2012 pp.198-204

J67. Fang Gong, Xuexin Liu, Hao Yu, Sheldon X.D. Tan and Lei He, "A Fast Non-Monte-Carlo Yield Analysis and Optimization by Stochastic Orthogonal Polynomials", ACM Transactions on Design Automation of Electronic Systems (TODAES),Vol 17, Issue 1, Jan. 2012.

J66. Yao, W.; Shi, Y.; He, L.; Pamarti, S.; , "Worst-Case Estimation for Data-Dependent Timing Jitter and Amplitude Noise in High-Speed Differential Link," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.20, no.1, pp.89-97, Jan. 2012

J65. Lei He, Shauki Elassaad, Yiyu Shi, Yu Hu, Wei Yao:"System-in-Package: Electrical and Layout Perspectives", Foundations and Trends in Electronic Design Automation .vol.4 no.4, pp. 223-306, 2011 (**invited survey**)

J64. Wenyao Xu, Jia Wang, Yu Hu, Ju-Yueh Lee, Fang Gong, Lei He and Majid Sarrafzadeh, "In-Place FPGA Retiming for Mitigation of Variational Single-Event Transient Faults," IEEE Transactions on Circuits and Systems I, vol.58, no.6,pp.1372 - 1381,May 2011

J63. Lerong Cheng, Fang Gong, Wenyao Xu, Jinjun Xiong, Lei He, Majid Sarrafzadeh, "Fourier Series Approximation for Max Operation in Non-Gaussian and Quadratic Statistical Static Timing Analysis," IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol.PP, no.99,pp.1-9,Jun.2011 .

J62. Fang Gong, Hao Yu, Lingli Wang, Lei He, "A Parallel and Incremental Extraction of Variational Capacitance With Stochastic Geometric Moments," IEEE Transactions on Very Large

Scale Integration Systems (TVLSI), vol.PP, no.99,pp1-9.Jun.2011

J61. Lerong Cheng, Puneet Gupta, Costas J. Spanos, Kun Qian, and Lei He, "Physically Justifiable Die-Level Modeling of Spatial Variation in View of Systematic Across Wafer Variability", IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems , Volume: 30, Issue:3, March 2011, pp. 388 - 401.

J60. D. Chen, J. Cong, C. Dong, L. He, F. Li, C. Peng, "Technology Mapping and Clustering for FPGA Architectures with Dual Supply Voltages," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: 29, Issue: 11, Nov. 2010, pp. 1709-1722.

J59. Chun Zhang, Yu Hu, Lingli Wang, Lei He, Jiarong Tong, "Accelerating Boolean Matching Using Bloom Filter", IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Volume:93A, Issue:10, Oct. 2010, pp.1775-1781 .

J58. Hao Yu, Chunta Chu, Yiyu Shi, David Smart, Lei He, Sheldon X.-D. Tan, "Fast Analysis of a Large-Scale Inductive Interconnect by Block-Structure-Preserved Macromodeling", IEEE Transaction on VLSI System , Volume:18, Issue:10, Oct. 2010, pp.1399-1411.

J57. Shenghua Liu, Guoqiang Chen, Tom Tong Jing, Lei He, Robi Dutta, Xianlong Hong: "Effective congestion reduction for IC package substrate routing", ACM Transactions on Design Automation of Electronic Systems (TODAES) , Volume 15, Issue 3, May 2010.

J56. Zhen Cao, Brian Foo, Lei He and Mihaela van der Schaar, "Optimality and Improvement of Dynamic Voltage Scaling Algorithms for Multimedia Applications," IEEE Transactions on Circuits and Systems I , Volume 57, Issue 3, March 2010, pp. 681-690. **(IEEE Circuits and Systems Society Darlington Award)**

J55. Yiyu Shi, Lei He, "EMPIRE: An Efficient and Compact Multiple-Parameterized Model-Order Reduction Method for Physical Optimization", IEEE Transaction on VLSI System , Volume:18, Issue:1, Jan. 2010, pp.108-118.

J54. Shenghua Liu, Guoqiang Chen, Tom Tong Jing, Lei He, Robi Dutta, Xianlong Hong: “Effective congestion reduction for IC package substrate routing”, ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 15, Issue 3, May 2010.

J53. Zhen Cao, Brian Foo, Lei He and Mihaela van der Schaar, "Optimality and Improvement of Dynamic Voltage Scaling Algorithms for Multimedia Applications" IEEE Transactions on Circuits and Systems I, Volume 57, Issue 3, March 2010, pp. 681-690 (**2011 IEEE Circuits and Systems Society Darlington Award**).

J52. Yiyu Shi and Lei He, "EMPIRE: An Efficient and Compact Multiple-Parameterized Model Order Reduction Method for Physical Optimization", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 18, Issue 11, Jan. 2010, pp. 108-118.

J51. Yiyu Shi, Jinjun Xiong, Howard Chen and Lei He, "Runtime Resonance Noise Reduction with Current Prediction Enabled Frequency Actuator" IEEE Transactions on Very large Scale Integration Systems(TVLSI), Volume PP, Issue 99, Dec. 2009, pp. 1-5.

J50. Lerong Cheng, Puneet Gupta, and Lei He, "Efficient Additive Statistical Leakage Estimation" IEEE Transactions on CAD(TCAD), Volume 28, Issue 11, Nov. 2009, pp. 1777-1781

J49. Hao Yu, Lei He, and M.C. Frank Chang, "Robust On-chip Signaling using Staggered and Twisted Interconnect", IEEE Design and Test of Computers (DTC), vol.26, no.5, pp92-104, September 2009.

J48. Hao Yu, Joanna Ho and Lei He, "Allocating Power Ground Vias in 3D ICs for Simultaneous Power and Thermal Integrity", ACM Transactions on Design Automation of Electronic Systems

(TODAES), May 2009 (**2010 ACM TODAES Best Paper Award**).

J47. Yu Hu, Satyaki Das, Steve Trimberger and Lei He, "Design and Synthesis of Programmable Logic Block with Mixed LUT and Macro-Gate", IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems, April 2009.

J46. Shenghua Liu, Guoqiang Chen, Tom Tong Jing, Lei He, Tianpei Zhang, Robi Dutta, and Xian-Long Hong, "Topological Routing to Maximize Routability for Package Substrate", IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems, Feb 2009.

J45. Lerong Cheng, Jinjun Xiong, Lei He, "Non-Gaussian Statistical Timing Analysis Using Second-Order Polynomial Fitting", IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems, Jan 2009.

J44. Yu Hu, Victor Shih, Rupak Majumdar, and Lei He, "Exploiting Symmetries to Speed-Up SAT-Based Boolean Matching for Logic Synthesis of FPGAs," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL. 27, NO. 10, Oct 2008.Page(s):1751-1760

J43. Hao Yu, Yiyu Shi, Lei He and Tanay Karnik, "Thermal Via Allocation for 3D ICs Considering Temporally and Spatially Variant Thermal Power", IEEE Transactions on Very Large Scale Integration Systems. Low Power Electronics and Design, Oct. 2006. ISLPED'06. Page(s):156-161.

J42. King Ho Tam, Yu Hu, Lei He, Tom Tong Jing, and Xinyi Zhang, "Dual-Vdd Buffer Insertion for Power Reduction," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL.27, NO. 8 August 2008 Page(s):1498-1502.

J41. Yiyu Shi, Jinjun Xiong, Chunchen Liu and Lei He, "Efficient Decoupling Capacitance Budgeting Considering Operation and Process Variations," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 7, July 2008 Page(s):1253 – 1263.

J40. Yu Hu, Yan Lin, Lei He and Tim Tuan, "Physical Synthesis for FPGA Interconnect Power Reduction by Dual-Vdd Budgeting and Retiming," ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 13, Issue 2, April 2008.

J39. Zhen Cao, Tom Tong Jing, Jinjun Xiong, Yu Hu, Zhe Feng, Lei He and Xianlong Hong, "Fashion: A Fast and Accurate Solution to Global Routing Problem," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.27, No.4, pp.726-737, April 2008.

J38. Yan Lin, Lei He and Mike Hutton, "Stochastic Physical Synthesis Considering Pre-routing Interconnect Uncertainty and Process Variation for FPGAs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Feb. 2008, Volume: 16, Issue: 2, page(s): 124-133.

J37. Xinyi Zhang, Lei He, Vassilios Gerousis, Li Song and Chin-Chi Ten, "Case Study and Efficient Modeling for Variational Chemical-Mechanical Planarization," IET Circuits, Devices & Systems. 2008, 2, (1), pp. 30–36.

J36. Yiyu Shi, Paul Mesa, Hao Yu and Lei He, "Circuit Simulated Obstacle-Aware Steiner Routing," ACM Transactions on Design Automation of Electronic Systems, Volume 12, Issue 3, August 2007.

J35. Yan Lin, Mike Hutton and Lei He, "Statistical Placement for FPGAs considering process variation," IET Computers & Digital Techniques, July 2007, Volume 1, Issue 4, p. 267-275.

J34. Changbo Long, Lucanus J. Simonson, Weiping Liao and Lei He, "Microarchitecture Configurations and Floorplanning Co-Optimization," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 15, Issue 7, July 2007, Pages: 830 – 841.

J33. Liu P., Tan S. X.-D., McGaughy B., Wu L. and He L., "TermMerg: An Efficient Terminal

Reduction Method for Interconnect Circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Issue 99, 2007.

J32. Cheng, L., Li, F., Lin, Y., Wong, P. and He, L, "Device and Architecture Cooptimization for FPGA Power Reduction," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 26, Issue 7, July 2007 Page(s):1211 – 1221.

J31. Jinjun Xiong, and Lei He, "Probabilistic Transitive-closure Ordering and its Application on Variational Buffer insertion", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.26, No.4, April, 2007.

J30. Jun Chen, Lei He, "Efficient In-Package Decoupling Capacitor Optimization for I/O Power Integrity," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006.

J29. Jinjun Xiong, Vladimir Zolotov, Lei He, "Robust Extraction of Spatial Correlation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006.

J28. Fei Li, Yan Lin, and Lei He, "Field Programmability of Supply Voltages for FPGA Power Reduction," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006

J27. Lei He, Andrew Kahng, King Ho Tam, and Jinjun Xiong, "Simultaneous Buffer Insertion and Wire Sizing Considering Systematic CMP Variation and Random Leff Variation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 12 pages.

J26. J. Xiong and L. He, "Full-Chip Multi-Level Routing for Power and Signal Integrity", Integration, the VLSI Journal, 18 pages.

J25. Y. Lin and L. He, "Dual-Vdd Interconnect with Chip-level Time Slack Allocation for FPGA Power Reduction," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 25, Issue 10, Oct. 2006 Page(s): 2023 - 2034.

J24. J. Chen and L. He, "Modeling and Synthesis of Multi-Port Transmission Line for Multi-Channel Interconnect," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 25, Issue 9, Sept. 2006 Page(s): 1664 - 1676.

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