Electrical Engineering Department (Boelter Hall 6731D)
University of California, Los Angeles, CA 90095
Phone: (310)206-2037 Fax: (310)825-8282 lhe@ee.ucla.edu

LEI HE

EMPLOYMENT

- 2002-present University of California Los Angeles, CA
  1999-2002 University of Wisconsin Madison, WI
  Associate Professor Step III (2007/07 - present), Associate Professor Step II (2006/07-2007/06), and Assistant Professor (1999/08-2006/06).
  Teaching and research on VLSI layout, circuit and interconnect modeling and design, programmable logic devices and interconnects, and embedded computer systems.
  Primary investigator for projects with extramural funding of about $500,000 per year, and author of over 180 technical publications (reprints at http://eda.ee.ucla.edu).

- 2000-present
  Consultant to various companies such as Intel, Cadence, and Synopsys.
  Member of Technical Advisory Board, RIO Design Automation and Apache Design Solutions.

- 1998/7-1999/2 Hewlett-Packard Research Laboratories Palo Alto, CA
  Proposed an efficient inductance extraction methodology for the state-of-the-art microprocessor designs.

EDUCATION

- 1994-1999 University of California Los Angeles, CA
  Ph.D. in Computer Science
  Dissertation: Modeling and Optimization of VLSI Interconnects

- 1986-1990 Fudan University Shanghai, China
  B.S. in Electrical Engineering
  Thesis: Fast Timing Simulation for CMOS Circuits

AWARDS

- Faculty Advisor for the project winning "Best Contribution Award" in the 2008 IEEE Programming Challenge at the IEEE International Workshop on Logic and Synthesis.
- SRC Inventor Award, 2007.
- Best Paper Award, the 2006 ACM/IEEE International Symposium on Physical Design.
- Nomination of Best Paper, ACM/IEEE Design Automation Conference (DAC 2006, 2008), International Conference on Computer-Aided Design (ICCAD 2006, 2007, 2008). Less than 2% of submitted papers were nominated based on blind review first by the technical program committee and then by the award committee.

- Northrop Grumman Excellence in Teaching Award, 2005.
- IBM Faculty Partner Award, 2003.
- Faculty Advisor for Best Student Paper Award, the 2003 IEEE International Conference on Application Specific Integrated Circuits.
- UCLA Chancellor's Early Faculty Development Award (highest class), 2003.
- National Science Foundation CAREER Award, 2000.
- Distinguished PhD Award, UCLA Henry Samueli School of Engineering and Applied Science, 2000.
- Nomination of Best Paper, the 1999 IEEE Custom Integrated Circuit Conference.
- GTE Fellowship from UCLA, 1997.
- Prize for Engineering and Technology, the Dimitris N. Chorafas Foundation, 1997.
- Best Paper Award, Chinese Computer Foundation CAD/CAM Conference, 1993.
- Motorola Fellowship, Fudan University, 1992.
- Top Graduating Student Award, Fudan University, 1990.

EDITORAL BOARDS

- Associate Editor, IEEE Transactions on Circuits and Systems I (2008 - present).
- Associate Editor, ACM Transactions on Reconfigurable Technology and Systems (2008 - present).

PROFESSIONAL REVIEW PANELS AND COMMITTEES

- External Reviewer, Research Grants Council, Hong Kong (2008, 2009).
- Member of three-person External Review Committee: five-year review of the Center for Embedded Computer Systems, University of California, Irvine (2005).
- Panelist, NSF Multi-Core (2008).
- Panelist, NSF CAREER program (2001).
- Panelist, NSF Major Research Instrument program (2000).

TECHNICAL PROGRAM COMMITTEE ASSIGNEMENTS

- IEEE/ACM Design Automation Conference (2004-2006), and Chair of Technical Program Subcommittee on "Beyond the Die" (2006).
- IEEE/ACM International Conference on Computer-Aided Design (2006-2008, 2010), and Chair of Technical Program Subcommittee on "System Design and Optimization" (2010).
- IEEE/ACM Asia and South Pacific Design Automation Conference, Member of Organization Committee (2006), Tutorial Chair (2006).
- IEEE/ACM International Symposium on Low Power Electronics and Design (2004-2007).
- IEEE/ACM International Symposium on Field Programmable Gate Arrays (2006-2007).
- IEEE International Conference on Field Programmable Technology (2008, 2009).
- IEEE International Conference on Communications, Circuits and Systems, Co-chair of circuits and systems track (2006-2008), and Co-Chair of Design Automation Track (2009).
- IEEE International Symposium on Circuits and Systems, CAD Track Chair, organizing and leading a technical sub-committee with over 30 members (2002).
- IEEE International Symposium on Quality of Electronic Design (2000-2004).
- IEEE International Conference on Computer Design (2003).

- IEEE Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (2003).
- IEEE International ASIC/SOC Conference (2001-2002).
- IEEE Great Lakes Symposium on VLSI Circuits and Systems (2002).

REVIWER FOR JOURNALS

- IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems.
- IEEE Transactions on Very Large Scale Integrated Circuits and Systems.
- IEEE Transactions on Circuits and Systems I, and II.
- IEEE Transactions on Electronic Devices.
- IEEE Electronic Device Letters.
- IEEE Transactions on Microwave Theory and Techniques.
- ACM Transactions on Design Automation of Electronic Systems.
- ACM Transactions on Reconfigurable Technology and Systems.
- SIAM Journal on Control and Optimization.
- Elsevier Microelectronics Journal.
- Elsevier Integration Journal.

TUTORIALS

- Silvakumar P. Mudanai, Noel Menezes, and Lei He, "Transistor, Cell, and Interconnect Modeling: Basics to Advances," half day tutorial, IEEE/ACM International Conference on Computer-Aided Design (2006).
- Paul M. Harvey, Howard Chen, Lei He, Chung-Kuan Cheng, and Kaushik Sheth, "Surviving and Thriving in the World of Chip and Package Co-Design," full day tutorial, IEEE/ACM Design Automation Conference (2006).
- Paul M. Harvey, Howard Chen, Chung-Kuan Cheng, Manjit Borah, Lei He, and Sheldon Tan, "High Performance Interconnect and Packaging," full-day tutorial, IEEE/ACM Asia South-Pacific Design Automation Conference (2006).
- A. Devgan, S. Elassaad, and L. He, "Chip-Package Co-design," half-day tutorial, IEEE/ACM International Conference on Computer-Aided Design (2005).
- L. He, M. Hutton, Time Tuan, and S. Wilton, "Challenges and Opportunities for Low Power FPGA in Nanometer Technologies," embedded tutorial, IEEE/ACM International Symposium on Low Power Electronics and Design (2005).
- L. Daniel, L. He, and B. Krauter, "Package-Chip Co-Design: Strategies and Challenges," half-day tutorial, IEEE/ACM International Symposium on Quality Electronic Design (2005).
- H. Chen, E. Chiprout, and L. He, "Power, Timing and Signal Integrity in SoC Designs," half-day tutorial, IEEE/ACM Asia South-Pacific Design Automation Conference (2003).
- L. He and S. Lin, "Signal Integrity for High-Performance Low-Power Circuits," half-day tutorial, IEEE International Symposium on Circuits and Systems (2002).
- L. He and S. Lin, "Interconnect Modeling and Design for Gigascale Systems-on-Chip with Consideration of Inductance," half-day tutorial, IEEE International ASIC/SOC Conference (2002).
- J. Cong, L. He, K. Y. Khoo, C. K. Koh and Z. Pan, "Interconnect Design for Deep Submicron ICs," embedded tutorial, IEEE/ACM International Conference on Computer-Aided Design,

November 1997.

BEST PAPER AWARDS AND NOMINFATIONS

- Yu Hu, Zhe Feng, Lei He, and Ruapk Majumdar, "Robust FPGA Resynthesis Based on Fault Tolerant Boolean Matching," IEEE/ACM International Conf. on Computer-Aided Design, 2008 (Nomination for Best Paper).
- Yu Hu, Victor Shih, Rupak Majumdar, and Lei He, "Mapping and Resynthesis for LUT-based FPGAs with an Efficient SAT-Based Boolean Matching," Best Contribution Award of the IEEE Programming Contest, IEEE International Symposium on Logic and Synthesis, 2008.
- Zhen Cao, Brian Foo, Lei He, and Mihaela van der Schaar, "Optimality and Improvement of Dynamic Voltage Scaling Algorithms for Multimedia Applications," IEEE/ACM Design Automation Conference, June, 2008, Anaheim, CA (Nomination for Best Paper).
- Yiyu Shi, Jinjun Xiong, Chunchen Liu and Lei He, "Efficient Decoupling Capacitance Budgeting Considering Operational and Processing Variations," IEEE/ACM International Conf. on Computer-Aided Design, 2007 (Nomination for Best Paper).
- Hao Yu, Joanna Ho, and Lei He, "Simultaneous Power and Thermal Integrity Driven Via Stapling in 3D ICs," IEEE/ACM International Conf. on Computer-Aided Design, 2006 (Nomination for Best Paper).
- Hao Yu, Yiyu Shi, and Lei He. "Fast Analysis of Structured Power Grid by Triangularization Based Structure Preserving Model Order Reduction," IEEE/ACM Design Automation Conference, 2006 (Nomination for Best Paper).
- Jinjun Xiong, Vladimir Zolotov, and Lei He, "Robust Extraction of Spatial Correlation," IEEE/ACM International Symposium on Physical Design, 2006 (Best Paper Award).
- L. Zhang, T. Jing, X. Hong, J. Xu, J. Xiong and L. He, "Global Routing for Performance Optimization with RLC Crosstalk Constraints," IEEE International Conference on Application Specific Integrated Circuits, Volume 1, 21-24, pp. 191-194, October 2003 (Best Student Paper Award).
- L. He, N. Chang, S. Lin, and O. S. Nakagawa, "An Efficient Inductance Modeling for On-chip Interconnects," IEEE Custom Integrated Circuits Conference, pp. 457-460, May 1999 (Nomination for Best Paper).

PUBLISHED BOOK

Sheldon X.-D. Tan, and Lei He, "Advanced Model Order Reduction Techniques for VLSI Designs," Cambridge University Press, pp 1-217, 2006.

PUBLISHED BOOK CHAPTERS

B5. W. Liao and Lei He, "Coupled Power and Thermal Simulation with Active Cooling," Springer-Verlag Publisher, Springer Lecture Notes in Computer Science, Vol. 3164, special issue on Power Aware Computer Systems, Pages 148-163, 2004.

B4. W. Liao and L. He, "Power Modeling and Reduction of VLIW Processors," Compilers and Operating Systems for Low Power, edited by L. Benini, M. Kandemir and J. Ramanujam, ISBN: 1-4020-7573-1, Kluwer Academic Publishers, August 2003, Chapter 9, pp 155-172.

B3. L. He, "Interconnect Modeling and Design with Consideration of On-Chip Inductance," a

chapter in Layout Optimizations in VLSI Designs, edited by D. Z. Du and S. Sapatnekar, Kluwer Academic Publishers, November 2001, pp. 155-190.

B2. Z. Tang, N. Chang, S. Lin, W. Xie, S. Nakagawa, and L. He, "Ramping Functional Units for Inductive Noise Reduction," a chapter in Springer Lecture Notes in Computer Science, Vol. 2008, Power Aware Computer Systems, edited by B. Falsafi and T. N. Vijaykumar, July 2001, pp. 13 -24.

B1. J. Cong, L. He and C. K. Koh, "Layout Level Optimization For Low Power," a chapter in Low Power Design in Deep Submicron Electronics, edited by W. Nebel and J. Mermet, Kluwer Academic Publishers, 1997, pp. 205-265.

PUBLISHED AND ACCEPTED JOURNAL PAPERS

J50. Hao Yu, Lei He, and M.C. Frank Chang, "Robust On-chip Signaling using Staggered and Twisted Interconnect", accepted by IEEE Design and Test of Computers (DTC), 2009.

J49. Hao Yu, Joanna Ho and Lei He, "Allocating Power Ground Vias in 3D ICs for Simultaneous Power and Thermal Integrity", accepted by ACM Transactions on Design Automation of Electronic Systems (TODAES), 2009.

J48. Yu Hu, Satyaki Das, Steve Trimberger and Lei He, "Design and Synthesis of Programmable Logic Block with Mixed LUT and Macro-Gate", IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems, April 2009.

J47. Shenghua Liu, Guoqiang Chen, Tom Tong Jing, Lei He, Tianpei Zhang, Robi Dutta, and Xian-Long Hong, "Topological Routing to Maximize Routability for Package Substrate", IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems, Feb 2009.

J46. Lerong Cheng, Jinjun Xiong, Lei He, "Non-Gaussian Statistical Timing Analysis Using Second-Order Polynomial Fitting", IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems, Jan 2009.

J45. Yiyu Shi and Lei He, "EMPIRE: An Efficient and Compact Multiple-Parameterized Model Order Reduction Method for Physical Optimization", accepted by IEEE Transactions on Very Large Scale Integration Systems.

J44. Yu Hu, Victor Shih, Rupak Majumdar, and Lei He, "Exploiting Symmetries to Speed-Up SAT-Based Boolean Matching for Logic Synthesis of FPGAs," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL. 27, NO. 10, Oct 2008.Page(s):1751-1760

J43. Hao Yu, Yiyu Shi, Lei He and Tanay Karnik, "Thermal Via Allocation for 3D ICs Considering Temporally and Spatially Variant Thermal Power," IEEE Transactions on Very Large Scale Integration Systems. Low Power Electronics and Design, Oct. 2006. ISLPED'06. Page(s):156-161.

J42. Xinyi Zhang, Lei He, Vassilios Gerousis, Li Song and Chin-Chi Ten, "Case Study and Efficient Modeling for Variational Chemical-Mechanical Planarization," accepted by IET Circuits, Devices & Systems.

J41. King Ho Tam, Yu Hu, Lei He, Tom Tong Jing, and Xinyi Zhang, "Dual-Vdd Buffer Insertion for Power Reduction," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL.27, NO. 8 August 2008 Page(s):1498-1502.

J40. Yiyu Shi, Jinjun Xiong, Chunchen Liu and Lei He, "Efficient Decoupling Capacitance Budgeting Considering Operation and Process Variations," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 7, July 2008 Page(s):1253 – 1263.

J39. Yu Hu, Yan Lin, Lei He and Tim Tuan, "Physical Synthesis for FPGA Interconnect Power

Reduction by Dual-Vdd Budgeting and Retiming," ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 13, Issue 2, April 2008.

J38. Zhen Cao, Tom Tong Jing, Jinjun Xiong, Yu Hu, Zhe Feng, Lei He and Xianlong Hong, "Fashion: A Fast and Accurate Solution to Global Routing Problem," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.27, No.4, pp.726-737, April 2008.

J37. Yan Lin, Lei He and Mike Hutton, "Stochastic Physical Synthesis Considering Pre-routing Interconnect Uncertainty and Process Variation for FPGAs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Feb. 2008, Volume: 16, Issue: 2, page(s): 124-133.

J36. Yiyu Shi, Paul Mesa, Hao Yu and Lei He, "Circuit Simulated Obstacle-Aware Steiner Routing," ACM Transactions on Design Automation of Electronic Systems, Volume 12, Issue 3, August 2007.

J35. Yan Lin, Mike Hutton and Lei He, "Statistical Placement for FPGAs considering process variation," IET Computers & Digital Techniques, July 2007, Volume 1, Issue 4, p. 267-275.

J34. Changbo Long, Lucanus J. Simonson, Weiping Liao and Lei He, "Microarchitecture Configurations and Floorplanning Co-Optimization," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 15, Issue 7, July 2007, Pages: 830 – 841.

J33. Liu P., Tan S. X.-D., McGaughy B., Wu L. and He L., "TermMerg: An Efficient Terminal Reduction Method for Interconnect Circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Issue 99, 2007.

J32. Cheng, L., Li, F., Lin, Y., Wong, P. and He, L, "Device and Architecture Cooptimization for FPGA Power Reduction," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 26, Issue 7, July 2007 Page(s):1211 – 1221.

J31. Jinjun Xiong, and Lei He, "Probabilistic Transitive-closure Ordering and its Application on Variational Buffer insertion," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.26, No.4, April, 2007.

J30. Jun Chen, Lei He, "Efficient In-Package Decoupling Capacitor Optimization for I/O Power Integrity," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006.

J29. Jinjun Xiong, Vladimir Zolotov, Lei He, "Robust Extraction of Spatial Correlation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006.

J28. Fei Li, Yan Lin, and Lei He, "Field Programmability of Supply Voltages for FPGA Power Reduction," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006

J27. Lei He, Andrew Kahng, King Ho Tam, and Jinjun Xiong, "Simultaneous Buffer Insertion and Wire Sizing Considering Systematic CMP Variation and Random Leff Variation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 12 pages.

J26. J. Xiong and L. He, "Full-Chip Multi-Level Routing for Power and Signal Integrity," Integration, the VLSI Journal, 18 pages.

J25. Y. Lin and L. He, "Dual-Vdd Interconnect with Chip-level Time Slack Allocation for FPGA Power Reduction," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 25, Issue 10, Oct. 2006 Page(s): 2023 - 2034.

J24. J. Chen and L. He, "Modeling and Synthesis of Multi-Port Transmission Line for Multi-Channel Interconnect," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 25, Issue 9, Sept. 2006 Page(s): 1664 - 1676.

J23. Z. Qi, H. Yu, P. Liu, S. Tan and L. He, "Wideband Passive Multi-Port Model Order Reduction and Realization of RLCM Circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 13 pages.

J22. Weiping Liao and Lei He, "Microarchitecture Level Interconnect Modeling Considering Layout Optimization," Journal of Low Power Electronics, American Scientific Publishers, January 2006.

J21. Weiping Liao and Lei He, "Microarchitecture-Level Leakage Reduction with Data Retention," IEEE Transactions on Very Large Scale Integration Systems, November 2005.

J20. Yan Lin, Fei Li and Lei He, "Circuits and Architecture Evaluation for Field Programmable Gate Array with Configurable Supply Voltage," IEEE Transactions on Very Large Scale Integration Systems, September 2005, pp. 1035 – 1047.

J19. Fei Li, Yan Lin, Lei He, Deming Chen, Jason Cong, "Power Modeling and Characteristics of Field Programmable Gate Arrays," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, October 2005, pp. 1712 – 1724.

J18. Fei Li, Lei He, Joe Basile, Rakesh J. Patel and Hema Ramamurthy, "Leakage Current Aware High-Level Estimation for VLSI Circuits," IEEE Proceeding on Computers & Digital Techniques, special issue for 2003 International Workshop on Power and Timing Modeling, Optimization and Simulation.

J17. Hao Yu and Lei He, "A Provably Passive and Cost Efficient Model for Inductive Interconnects," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 11 pages, August 2005, pp. 1283-1294.

J16. Jun Chen and Lei He, "Worst-Case Crosstalk Noise for Non-Switching Victims in High-Speed Buses," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 9 pages, August 2005, pp. 1275 - 1283.

J15. Weiping Liao, Lei He and Kevin Lepak, "Temperature and Supply Voltage Aware Performance and Power Modeling at Microarchitecture Level," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, July 2005, 1042 – 1053.

J14. Jun Chen and Lei He, "Piece-wise Linear Model for Transmission Line with Capacitive Loading and Ramp Input," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, June 2005, pp. 928 – 937.

J13. Jinjun Xiong and Lei He, "Extended Global Routing with RLC Crosstalk Constraints," IEEE Transactions on Very Large Scale Integration Systems, Vol. 13, Issue 3, Pages 319-329, March 2005.

J12. Changbo Long and Lei He, "Distributed Sleep Transistor Network for Power Reduction," IEEE Transactions on Very Large Scale Integration Systems, Pages 937-946, September 2004.

J11. Kevin M. Lepak, Min Xu, Jun Chen and Lei He, "Simultaneous shield insertion and net ordering for capacitive and inductive coupling minimization," ACM Transactions on Design Automation of Electronic Systems, Volume 9, Issue 3, Pages 290 - 309, 2004.

J10. Ling Zhang, Tong Jing, Xianlong Hong, Jingyu Xu, Jinjun Xiong and Lei He, "CEE-Gr: A Global Router with Performance Optimization under Multi-Constraints," Chinese Journal of Semiconductors, 2004, 25(5): 508-515.

J9. J. Xiong, L. He, "Full-chip Routing Optimization with RLC Crosstalk Budgeting," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: 23, Issue: 3, March 2004 Pages: 366 - 377.

J8. J. Cong, L. He, C. K. Koh, and Z. Pan, "Interconnect Sizing and Spacing Considering Coupling Capacitance," IEEE Transactions on Computer-Aided Design, vol. 20, no. 9, pp.1164-1169, September 2001.

J7. J. Cong and L. He, "Theory and Algorithm of Local Refinement Based Optimization with Application to Device and Interconnect Sizing," IEEE Transactions on Computer-Aided Design, April 1999, pp. 406-420.

J6. J. Cong, L. He, C.-K. Koh and P. H. Madden, "Performance Optimization of VLSI Interconnect Layout," **invited survey**, Integration, the VLSI Journal, vol. 21, 1996, pp. 1-94.

J5. J. Cong and L. He, "Optimal Wire sizing for Interconnects with Multiple Sources," ACM Transactions on Design Automation of Electronic Systems, October, 1996, pp. 478-511.

J4. L. He, K. H. Zhang and P. S. Tang, "FTSIM: A switch level fast timing simulator," CIE *Acta Electronica Sinica*, February 1995, vol.23, (no.2):17-21.

J3. L. He, K. H. Zhang and P. S. Tang, "Fast Timing Simulation Considering Feedback Processing," CIE Journal of Electronics, April 1994.

J2. L. He, J. R. Tong and P. S. Tang, "Development and Maintenance of CAD Software," CCF Journal of CAD and Graphics, vol. 6, No. 1, January 1994.

J1. Y. Q. Zhang, L. He, J. R. Tong and P. S. Tang, "An Integrated CAD Software Development Environment," CCF Journal of CAD and Graphics, vol. 5, No. 3, March 1993.

PUBLISHED AND ACCEPTED CONFERENCE PAPERS

Reprints at http://eda.ee.ucla.edu

C128 Lerong Cheng, Puneet Gupta, Costas Spanos, Kun Qian, and Lei He, "Physically Justiable Die-Level Modeling of Spatial Variation in View of Systematic Across Wafer Variability", DAC 2009.

C127 Fang Gong, Hao Yu, and Lei He, "PiCAP: A Parallel and Incrementel Capacitance Extraction Considering Stochastic Process Variation", DAC 2009.

C126. Ju-Yueh Lee, Yu Hu, Rupak Majumdar, and Lei He, "Simultaneous Test Pattern Compaction, Ordering and X-Filling for Testing Power Reduction", ISQED 2009.

C125. Wei Yao, Yiyu Shi, Lei He and Sudhakar Parmati, "Worst Case Timing Jitter and Amplitude Noise in Differential Signaling", ISQED 2009.

C124. Lerong Cheng, Puneet Gupta, and Lei He, "Accounting for Non-linear Dependence Using Function Driven Component Analysis", ASPDAC 2009.

C123. Yiyu Shi, Wei Yao, Jinjun Xiong, and Lei He, "Incremental and On-demand Random Walk for Iterative Power Distribution Network Analysis", ASPDAC 2009.

C122. Yiyu Shi, Jinjun Xiong, Howard Chen, and Lei He, "Stochastic Current Prediction Enabled Frequency Actuator for Runtime Resonance Noise Reduction", ASPDAC 2009.

C121. Yiyu Shi, Lei He, and C.-J. Richard Shi, "Scalable Symbolic Model Order Reduction", IEEE Behaviorial Modeling and Simulation Conference 2008. C120. Yu Hu, Zhe Feng, Lei He, and Ruapk Majumdar, "Robust FPGA Resynthesis Based on Fault Tolerant Boolean Matching," accepted by the 2008 IEEE/ACM International Conf. on Computer-Aided Design (**nomination for Best Paper**).

C119. Zhen Cao, Brian Foo, Lei He, and Mihaela van der Schaar , "Optimality and Improvement of Dynamic Voltage Scaling Algorithms for Multimedia Applications," IEEE/ACM Design

Automation Conference, June, 2008, Anaheim, CA (**nomination for Best Paper**).

C118. Yu Hu, Victor Shih, Rupak Majumdar, and Lei He, "FPGA Area Reduction by Multi-Output Function Based Sequential Resynthesis," IEEE/ACM Design Automation Conference, June, 2008, Anaheim, CA.

C117. Shenghua Liu, Guoqiang Chen, Tom Tong Jing, Lei He, Tianpei Zhang, Robi Dutta, and Xian-Long Hong, "Topological Routing to Maximize Routability for Package Substrate," IEEE/ACM Design Automation Conference, June, 2008, Anaheim, CA.

C116. Yu Hu, Zhe Feng, Rupak Majumdar, and Lei He, "Templates and Algorithms of Boolean Matching for Fault Tolerance in FPGAs," IEEE International Workshop on Logic and Synthesis, June 2008, Lake Tahoe, CA.

C115. Yu Hu, Victor Shih, Rupak Majumdar, and Lei He, "FPGA Area Reduction by Multi-Output Function Based Sequential Resynthesis," IEEE International Workshop on Logic and Synthesis, 200, Lake Tahoe, CA.

C114. Lerong Cheng, Jinjun Xiong, and Lei He, "Non-Gaussian Statistical Timing Analysis Using Second-Order Polynomial Fitting," Proc. Asia South Pacific Design Automation Conf., 2008.

C113. Lerong Cheng, Yan Lin, Lei He, and Yu Cao, "Trace Based Framework for Concurrent Development of Process and FPGA Architecture Considering Process Variation and Reliability," Proc. ACM Intl. Symp. Field-Programmable Gate Arrays, 2008.

C112. Chun-Ta Chu, Xinyi Zhang, Lei He and Tom Tong Jing, "Temperature Aware Microprocessor Floorplanning Considering Application Dependent Power Load," IEEE/ACM International Conf. on Computer-Aided Design (ICCAD), 2007.

C111. Yan Lin and Lei He, "Device and Architecture Concurrent Optimization for FPGA Transient Soft Error Rate," IEEE/ACM International Conf. on Computer-Aided Design (ICCAD), 2007.

C110. Yu Hu, Satyaki Das, Steve Trimberger and Lei He, "Design, Synthesis and Evaluation of Heterogeneous FPGA with Mixed LUTs and Macro-Gates," ICCAD, 2007.

C109. Yu Hu, Victor Shih, Rupak Majumdar and Lei He, "Exploiting Symmetry in SAT-Based Boolean Matching for Heterogeneous FPGA Technology Mapping," ICCAD, 2007.

C108. Yiyu Shi, Jinjun Xiong, Chunchen Liu and Lei He, "Efficient Decoupling Capacitance Budgeting Considering Operation and Process Variations," ICCAD 2007, (**nomination for Best Paper**).

C107. Yiyu Shi and Lei He, "EMPIRE: An Efficient and Compact Multiple-Parameterized Model Order Reduction Method for Physical Optimization," SRC Techcon Conference 2007.

C106. Hao Yu, Yu Hu, Chun-Chen Liu and Lei He, Minimal Skew Clock Synthesis Considering Time Variant Temperature Gradient. SRC Techcon Conference, 2007.

C105. Lerong Cheng, Jinjun Xiong and Lei He, "Non-Linear Statistical Static Timing Analysis for Non-Gaussian Variation Sources," in proceedings of IEEE/ACM Design Automation Conference, 2007.

C104. Hao Yu, Chunta Chu and Lei He, "Off-chip Decoupling Capacitor Allocation for Chip Package Co-Design," in proceedings of IEEE/ACM Design Automation Conference, 2007.

C103. Yu Hu, Satyaki Das and Lei He, "Design, Synthesis and Evaluation of Heterogeneous FPGA with Mixed LUTs and Macro-Gates ," IWLS, 2007.

C102. Yu Hu, Victor Shih, Rupak Majumdar and Lei He, "Exploiting Symmetry in SAT-Based Boolean Matching for Heterogeneous FPGA Technology Mapping ," IWLS, 2007.

C101. Yan Lin and Lei He "Statistical Dual-Vdd Assignment for FPGA Interconnect Power

Reduction ," IEEE/ACM Design Automation and Test in Europe, April 2007.

C100. Hao Yu, Yu Hu, Chuenchen Liu, and Lei He, "Minimal Skew Clock Embedding Considering Time Variant Temperature Variation Gradient," ACM International Symposium on Physical Design (ISPD), March 2007.

C99. Yiyu Shi and Lei He, "EMPIRE: An Efficient and Compact Multiple-Parameterized Model Order Reduction Method for Physical Optimization," International Symposium on Physical Design (ISPD), 2007

C98. Yu Hu, King Ho Tam, Tong Jing and Lei He, "Fast Power-optimal Buffering Based on Interconnect Prediction and Sampling," IEEE/ACM System Level Interconnect Prediction (SLIP), Austin, Texas, March, 2007.

C97. Lerong Cheng, Jinjun Xiong, and Lei He, "Non-Linear Statistical Static Timing Analysis for Non-Gaussian Variation Sources," ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems(TAU), Feb. 2007.

C96. Yan Lin and Lei He, "Stochastic Physical Synthesis for FPGAs with Pre-routing Interconnect Uncertainty and Process Variation," IEEE/ACM International Symposium on Field-Programmable Gate Arrays , Feb 2007

C95. Zhen Cao, Tong Jing, Jinjun Xiong, Yu Hu, Lei He, and Xianlong Hong, "DpRouter: A Fast and Accurate Dynamic-Pattern-Based Global Routing Algorithm," IEEE/ACM Asia and South Pacific Design Automation Conference(ASPDAC), Japan, 2007.

C94. Hao Yu, Yiyu Shi, and Lei He, "A First Order Block Structure Preserving Model Order Reduction with Inversed Inductance," IEEE/ACM International Conf. on Computer-Aided Design, San Jose, CA, Nov. 6-9, 2006.

C93. Hao Yu, Joanna Ho, and Lei He, "Simultaneous Power and Thermal Integrity Driven Via Stapling in 3D ICs," IEEE/ACM International Conf. on Computer-Aided Design, San Jose, CA, Nov. 6-9, 2006. **(Nomination for Best Paper)**

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