Fang Gong

Contact Information

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Research Interests

- Theoretical foundation of probabilistic modeling and statistical analysis
- Pervasive computing for mobile health
- Cyber-physical security and mobile security
- Variation-aware design automation of VLSI circuit and system
- High-performance and energy-efficient computing

Education

Ph.D., University of California, Los Angeles, Los Angeles, 09/2008 to 12/2012
- Thesis Topic: *Variability-aware stochastic modeling of custom integrated circuits*
- Design Automation Lab, Department of Electrical Engineering
- Adviser: Professor Lei He
- Area of Study: Circuits and Embedded Systems

M.S., Tsinghua University, Beijing, 09/2005 to 07/2008
- Thesis Topic: *Efficient Impedance Extraction of 3D VLSI Interconnects*
- Electronic Design Automation Lab, Department of Computer Science
- Adviser: Professor Zeyi Wang
- Area of Study: Interconnect Parasitic Extraction

B.S., Beihang University, Beijing, 09/2001 to 06/2005
- Software Engineering Institute, Department of Computer Science and Technology
- Emphasis on information security and data management
- Adviser: Professor Bo Lang
- Area of Study: Computer and Information Systems

Awards and Honors

- Awarded "IBM Ph.D. Scholarship", IBM Corp., New York, 2012.
- Awarded "Graduate Researcher Grant", CANDE workshop, San Jose, 2011.
- Awarded "SIGDA Ph.D. Forum", Design Automation Conference, San Diego, 2011.
- Awarded "UCLA Travel Grant", Electrical Engineering Department, UCLA, 2011.
- Awarded "Young Researcher Program", Design Automation Conference, 2009.
- Awarded "UCLA Graduate Fellowship", UCLA, Fall 2008-Spring 2009.
- Awarded "Tsinghua Graduate Fellowship", Tsinghua University, 2005-2008.
- Awarded "Second Place Scholarship", Beihang University, 2004.

Industry Experience

Cadence Design Systems, Simulation Group, San Jose, CA

Senior Member of R&D Technical Staff **08/2013 to present**
- Developed next-generation circuit simulation for VLSI.
- Researched statistical analysis to compensate the process variations.
- Tested on real customer circuit designs.

IBM Corp., Systems and Technology Group, Hopewell Junction, NY

Research Intern **07/2012 to 09/2012**
- Developed a multi-threaded noise analysis tool for VLSI chip design.
- Researched and solved the thread-safety issues to assure the accuracy.
- Tested on large-scale industrial circuit designs to show significant speedup.
- Supervisor: Chandu Visweswariah

Academic Experience

University of California, Los Angeles, Los Angeles, CA

Research Associate **01/2013 to 06/2013**

- Research novel algorithms of stochastic circuit modeling.
- Participate research on renewable energy modeling and analysis.
- Prototype embedded system for healthcare purpose.
- Supervisor: Prof. Lei He.

University of California, Los Angeles, Los Angeles, CA

Graduate Researcher **09/2008 to 12/2012**

- Developed algorithms for stochastic circuit modeling and analysis.
- Proposed analysis and optimization methodology for memory circuit design.
- Prototyped a portable Brain-Computer-Interface system to monitor EEG signals.
- Participated in an interdisciplinary research on battery modeling.
- Supervisor: Prof. Lei He.

Tsinghua University, Beijing, P.R.China

Graduate Researcher **09/2005 to 06/2008**

- Proposed an efficient parasitic extraction algorithm for VLSI circuit and system.
- Improved the algorithm with efficient numerical and optimization techniques.
- The developed work had been used by industrial company in production.
- Supervisor: Prof. Zeyi Wang.

Refereed Journal Publications

[1] **F. Gong**, Y. Shi, H. Yu, L. He, "Variability-Aware Parametric Yield Estimation for Analog/Mixed-Signal Circuits: Concepts, Algorithms and Challenges", *IEEE Design and Test of Computer*, Feb. 2014.

[2] W. Wu, **F. Gong**, H. Yu and L. He, "Exploiting the Parallelism in EDA Algorithms by Dependency Elimination", *IEEE Design and Test of Computer*, vol.30, no.1, pp.26-35, Feb. 2013.

[3] **F. Gong**, S. Basir-Kazeruni, H. Yu and L. He, "Stochastic Behavioral Modeling Analysis of Analog/Mixed-Signal Circuits", *IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems (TCAD)*, vol.32, no.1, pp.24-33, Jan. 2013.

[4] X. Xu, Y. Chen, W. Xu, **F. Gong**, "An Efficient Algorithm for Mobile Localization in Sensor Networks", *International Journal of Automation and Computing*, pp.594-599, Dec. 2012.

[5] L. Cheng, W. Xu, **F. Gong**, Y. Lin, H.-Y. Wong and L. He, "Statistical Timing and Power Optimization of Architecture and Device for FPGAs", *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 5, no. 2, Article 9, 19 pages, June 2012.

[6] S. Basir-Kazeruni, H. Yu, **F. Gong**, Y. Hu, C. Liu and L. He, "SPECO: Stochastic Perturbation Based Clock Tree Optimization Considering Temperature Uncertainty", *Integration, the VLSI Journal (IVLSI)*, vol. 46, no. 1, Page(s): 22-32, January 2013.

[7] **F. Gong**, W. Xu, J.-Y. Lee, L. He and M. Sarrafzadeh, "NeuroGlasses: A Neural Sensing Healthcare System for 3-D Vision Technology", *IEEE Transactions on Information Technology in BioMedicine (TITB)*, vol. 6, no. 1, Page(s): 1-7, Nov. 2011.

[8] L. Cheng, **F. Gong**, W. Xu, J. Xiong, L. He and M. Sarrafzadeh, "Fourier Series Approximation for Max Operation in Non-Gaussian and Quadratic Statistical Static Timing Analysis", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 20, no. 8, Page(s): 1383-1391, Aug. 2011.

[9] W. Xu, J. Wang, Y. Hu, J.-Y. Lee, **F. Gong**, L. He and M. Sarrafzadeh, "In-Place FPGA retiming for mitigation of variational single-event transient faults", *IEEE Transactions on Circuits and Systems Part I (TCAS-I)*, Vol.58, no. 6, Page(s): 1372-1381, May 2011.

[10] W. Xu and **F. Gong**, "A Brain-Computer Interface to Help the Elderly Reduce the Risk of Falling", *Bruin Innovation and Technology (BIT) Magazine*, Issue 1, Spring 2011, Pages 1-4.

[11] **F. Gong**, H. Yu, L. Wang and L. He,"A Parallel and Incremental Extraction of Variational Capacitance with Stochastic Geometric Moments", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 20, no. 9, Page(s): 1729-1737, 2012.

[12] **F. Gong**, X. Liu, H. Yu, S.-X.D. Tan and L. He, "A Fast Non-Monte-Carlo Yield Analysis and Optimization by Stochastic Orthogonal Polynomials", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 17, No. 1, Article 10, 23 pages, January 2012.

[13] **F. Gong**,W. Yu, C. Yan and Z. Wang, "An Algorithm Based on Mixed Boundary Element Integral Formulations for Extracting Frequency-Dependent Impedances of 3D VLSI Interconnects", *Journal of Computer Aided Design and Computer Graphics*. Vol.19, No.10, pp. 1252-1258, Oct.,2007.

Conference Publications

[14] W. Wu, **F. Gong**, G. Chen, L. He, "A Fast and Provably Bounded Failure Analysis of Memory Circuits in High Dimensions", *IEEE Asia South Pacific Design Automation Conference* (ASPDAC), pp.424-429, Jan. 2014.

[15] R. Krishnan, W. Wu, **F. Gong** and L. He, "Stochastic Behavior Modeling of Analog/Mixed-Signal Circuits by Maximizing Entropy", *in Proc. 14th International Symposium on Quality Electronic Design* (ISQED'13), Santa Clara, CA, pp. 572-579, March 4-6, 2013.

[16] **F. Gong**, Y. Shi, L. Dolecek and L. He, "Breaking the Curse of High Dimensionality: An Efficient Rare-Event Estimation Algorithm in High Dimension", *ACM/IEEE 49th Design Automation Conference Work-In-Progress Workshop (WIP)* (DAC'12), San Francisco, CA, June 3-7, 2012.

[17] **F. Gong**, S. Basir-Kazeruni, L. Dolecek and L. He, "A Fast Estimation of SRAM Failure Rate Using Probability Collectives", *ACM International Symposium on Physical Design* (ISPD'12), Napa Valley, CA, March 25-28, 2012. Page(s):41-47.

[18] **F. Gong**, W. Fei, H. Yu and L. He, "Challenges in Transient Noise Analysis for High-precision Analog/RF Circuits", *International Conference on Materials for Advanced Technologies* (ICMAT'11), Suntec, Singapore, Jun 26-Jul 1, 2011.

[19] **F. Gong**, H. Yu and L. He, "Fast Non-Monte-Carlo Transient Noise Analysis for High-Precision Analog/RF Circuits by Stochastic Orthogonal Polynomials", *in Proceedings of the 48th IEEE Design Automation Conference* (DAC'11), San Diego, CA, June5-10, 2011. Page(s):298-303.

[20] W. Xu, **F. Gong**, L. He and M. Sarrafzadeh, "Wearable Assistive System Design for Fall Prevention", *3rd Joint Workshop on High Confidence Medical Devices, Software, and Systems & Medical Device Plug-and-Play Interoperability* (HCMDSS/MDPnP 2011), Chicago, Illinois, April 11, 2011.

[21] **F. Gong**, H. Yu and L. He, "Stochastic Analog Circuit Behavior Modeling by Point Estimation Method", *in Proceedings of the 2011 International Symposium on Physical Design 2011* (ISPD'11), Santa Barbara, California, March 27-30, 2011. Page(s): 175-182.

[22] **F. Gong**, Y. Shi, H. Yu and L. He, "Parametric Yield Estimation for SRAM Cells: Concepts, Algorithms and Challenges", *ACM/IEEE 47th Design Automation Conference Knowledge Center* (DAC'10), June 8, 2010.

[23] **F. Gong**, H. Yu, Y. Shi, D. Kim, J. Ren and L. He, "QuickYield: An Efficient Global-Search Based Parametric Yield Estimation With Performance Constraints", *in Proc. ACM/IEEE 47th Design Automation Conference* (DAC'10), Anaheim, California, June 13 - 18, 2010. Page(s):392-397.

[24] **F. Gong**, H. Yu and L. He, "PiCAP: A Parallel and Incrementel Capacitance Extraction Considering Stochastic Process Variation", *in Proc. ACM/IEEE 46th Annual Design Automation Conference* (DAC'09), San Francisco, California, July 26 - 31, 2009. Page(s): 764-769.

[25] S. Zeng, W. Yu, **F. Gong**, X. Hong, J. Shi, Z. Wang and C. Cheng, "Efficient Frequency-Dependent Extraction for Large-Scale Power/Ground Grid", *in Proc. 9th International Conference on Solid-State and Integrated-Circuit Technology* (ICSICT 2008), Oct. 2008. Page(s):2292-2295.

[26] **F. Gong**, W. Yu, Z. Wang and Z. Yu, "Efficient Techniques for 3-D Impedance Extraction Using Mixed Boundary Element Method", *in Proc. IEEE 13th Asia South Pacific Design Automation Conference* (ASPDAC'08), Seoul, Korea, Jan.21-24, 2008. Page(s):158-163.

Teaching Experience

University of California, Los Angeles, Los Angeles, CA

Teaching Assistant **Winter 2011, Winter 2012**
EE201C: Modeling of VLSI Circuits and Systems

- **Topics:** Interconnect Analysis, Model Order Reduction, Static Timing Analysis, Stochastic Modeling, Statistical Static Timing Analysis (SSTA), On-Chip Power Integrity, Stochastic Circuit Optimization, IC/Package Co-Design.
- **Duties:** lecture notes preparation, guest lecture, homework design and grading, Q&A session, final project assignment and grading.

Teaching Assistant **Winter 2010, Spring 2010**
EE110L: Circuit Measurement Laboratory

- **Topics:**Basic circuit theorems, Superposition, Thevenin or Norton equivalent, Bode plot, Resonance circuits, Filters, Amplifier, Oscillator circuit.
- **Duties:** lab experiment instruction, report grading, Q&A session.

Talks and Presentations

Conference Presentations

- UCLA Electrical Engineering Research Review, Los Angeles, CA, Dec. 4, 2012.
- International Symposium on Physical Design, Napa Valley, CA, March 26, 2012.
- IEEE PhD Forum Design Automation Conference, San Diego, CA, June 5-10, 2011.
- Computer-Aided Network Design (CANDE) workshop, San Jose, CA, Nov. 10, 2011.

- IEEE Design Automation Conference, San Diego, CA, June 5-10, 2011.
- International Symposium on Physical Design, Santa Barbara, CA, March 27, 2011.
- IEEE Design Automation Conference, Anaheim, CA, June 13 - 18, 2010.
- IEEE Design Automation Conference, San Francisco, CA, July 26 - 31, 2009.
- IEEE Asia South Pacific Design Automation Conference, Seoul, Korea, Jan.21, 2008.

Invited Talks

- "Stochastic Modeling and Analysis for Custom Circuits", Berkeley Design Automation Inc., San Jose, CA, March 15, 2012.
- "Circuit Level Evaluation for Advanced Technologies", Globalfoundries Inc., Santa Clara, CA, July 16, 2012.
- "Stochastic Circuit Modeling and Validation for Analog/Mixed-Signal Circuits", Strategy CAD Research Group, Intel Corp., San Jose, CA, Feb. 16, 2012.
- "Stochastic Modeling and Validation for Analog/Mixed-Signal Circuits", CAD Reliability Analysis Group, Intel Corp., San Jose, CA, Feb. 21, 2012.
- "Stochastic Modeling and Validation of Analog/Mixed-Signal Circuit", UCLA Electrical Engineering Faculty Lunch Forum, UCLA, Oct. 10, 2012.

Professional Service

Journal Referee Service

- IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems
- IEEE Transactions on Very Large Scale Integration Systems
- IEEE Transactions on Circuits and Systems II
- IEEE Transactions on Nanotechnology
- Journal of Electronic Science and Technology
- International Journal of Communication Systems
- International Journal of Automation and Computing
- the Integration, the VLSI Journal

Conference Reviewer Service

- IEEE/ACM Design Automation Conference (DAC)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
- IEEE/ACM International Symposium on Circuit and System (ISCAS)
- IEEE/ACM International Symposium on Physical Design (ISPD)
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)

Conference Session Chair

- IEEE/ACM Design Automation Conference (DAC) 2014 with session: "Anti-Aging Secrets for Chips"