ECE 298

Modeling and Optimization of VLSI Circuits and Systems

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Office hour: 4-5pm

Course Prerequisites

- **Prerequisites**
  - **Mainly self-contained**
- **Knowledge to help you appreciate more**
  - **EE115C Digital Electronic Circuits**
  - **CS180 Introduction to Algorithms**
  - **EE101 Engineering Electromagnetics**

References

- **Cong-He-et al, Performance Optimization of VLSI Interconnect Layout, *Integration, the VLSI Journal* 21 (1996) 1--94.**
- **Selected papers from major circuit and CAD conferences and journals**
- **Raminderpal Singh, "Signal Integrity Effects in Custom IC and ASIC Designs," IEEE Press, 2002.**

Related VLSI CAD Conferences and Journals

- **ACM IEEE Design Automation Conference (DAC)**
- **International Conference on Computer Aided Design(ICCAD)**
- **IEEE International Symposium on Circuits and Systems (ISCAS)**
- **Design, Automation and Test in Europe (DATE)**
- **Asia and South Pacific Design Automation Conference (ASP-DAC)**
- **International symposium on physical design (ISPD)**
- **IEEE Transactions on CAD of Circuits and systems (TCAD)**
- **ACM Trans. on Design Automation of Electronic Systems (TODAES)**
- **IEEE Transactions on Circuits and Systems (TCAS)**
- **IEEE Trans. on VLSI Systems (TVLSI)**

Grading Policy

- **Homework** **20%**
- **Quiz and Midterm** **20%**
- **Paper presentation** **10%**
  - **Use transparencies or video projector**
  - **Graded by fellow students**
- **Term project** **50%**
- **Bonus points**
  - **For active participation**

- **Grade A for score > 85**

Term Project

- **One of the following:**
  - **Survey of selected papers (1 person, at most 40 points)**
  - **Programming project (2 persons in a term)**
  - **Writing requirements**
    - **In a conference paper style**

Course Outline

- **Overview and Introduction (1 lecture)**

- **Interconnect Extraction and Modeling (3 lectures)**
- **Timing models, Delay Calculation, and Timing Analysis (2 lectures)**
- **Wireload model, logic effort and fanout optimization (2 lectures)**
- **Interconnect Synthesis and Routing Optimization (2 lectures)**

Course Outline

- **Noise Modeling, Avoidance and Control (3 lectures)**
- **Power Supply Modeling and Optimization (2 lectures)**
- **High-level Area/Power Estimation and Layout Planning (2 lectures)**
- **System-level Interconnect design** (1 lecture)**

Skills to Learn

- **Interconnect modeling and design**
  - **A course parallel to EE216M**
- **Algorithm / Programming / writing / presentation**

Course Web Site

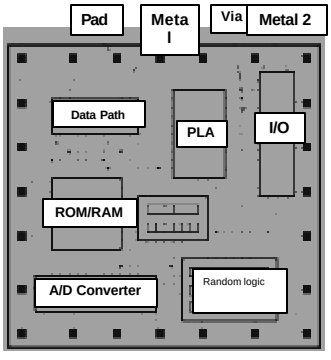
- **Examples of previous projects**
  - **http://eda.ece.wisc.edu/ece902.html**
- **Course website**
  - **http://eda.ee.ucla.edu/ee298.html**

Overview

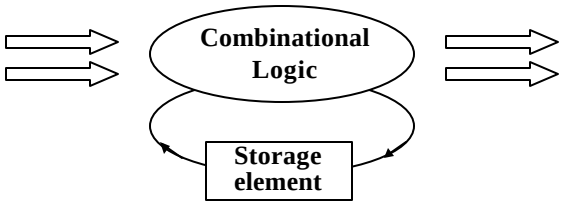
- **Moore's Law**
- **CMOS scaling theory**
- **Interconnect performance implied by NTRS'97**
- **Need for a new design paradigm**

Basic Components In VLSI Circuits

- **Devices**
  - Transistors
  - Logic gates and cells
  - Function blocks
- **Interconnects**
  - Local signals
  - Global signals
  - Clock signals
  - Power/ground networks



Determining Factors of System Performance



Clock Period $\geq$ $t_{d\text{-}gates} + t_{d\text{-}interconnects} + t_{skew} + t_{su} + t_{ds}$

$t_{d\text{-}gates}$ = gate delay in comb. logic

$t_{d\text{-}interconnects}$ = interconnect delay in comb. logic

t_{skew} = clock skew

t_{su} = set-up time

t_{ds} = delay within storage elements

} Interconnect delay

Importance of VLSI Interconnect Design

- **Technology Trends:**
  - **Deep sub-micron design:** < 0.18 micron CMOS technology
  - **High-Speed :** > 500 MHz ~ 5 GHz
- **Impact on VLSI System Design**
  - **Interconnect delay becomes the dominating factor in system performance**
    - Consumes 50%-70% clock cycle
  - **Distributed nature of interconnects becomes significant**
    - Becomes distributed RCL circuits or lossy transmission lines.

→ **Interconnect-Driven Design**

Moore's Law and NTRS

- **Moore's Law**
  - The min. transistor feature size decreases by 0.7X every three years (Electronics Magazine, Vol. 38, April 1965)
  - True in the past 30 years!
- **National Technology Roadmap for Semiconductors (NTRS'97)**

Technology (um)	*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
Year	1997	1999	2001	2003	2006	2009
# transistors	11M	21M	40M	76M	200M	520M
On-Chip Clock (MHz)	750	1200	1400	1600	2000	2500
Area (mm^2)	300	340	385	430	520	620
Wiring Levels	6	6-7	7	7	7-8	8-9

Ideal Scaling of MOS Transistors

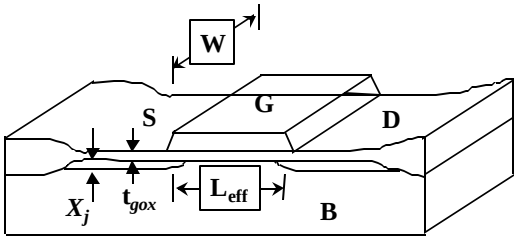


Figure 1.1 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). The main dimensions that determine device properties are gate oxide thickness t_{gox}; gate length *L*, gate width *W*; and junction depth X_j

Assumptions:

- **All horizontal & vertical dimensions of a transistor(*W*, *L*, t_{gox}, X_j) are reduced by S**
- **All voltages (V_{oo}, V_{TN}, V_{TP}) are reduced by S**
- **Substrate doping (N_{sub}) is increased by S**
- **(V_{TN}, V_{TP}: threshold voltages of N and P transistors)**

TABLE 1.1 Scaling of MOS Transistors

Parameter	Scaling Factor
Dimensions (W, L, t_{gox}, X_j)	1/S
Substrate doping (N_{SUB})	S
Voltages (V_{DD}, V_{TN}, V_{TP})	1/S
Current per device ($I_{DS} \propto \frac{W}{L}\frac{\varepsilon_{ox}}{t_{gox}}(V_{DD}-V_T)^2$)	1/S
Gate capacitance ($C_g = \varepsilon_{ox}\frac{WL}{t_{gox}}(V_{DD}-V_T)^2$)	1/S
Transistor on-resistance ($R_{tr} \propto \frac{V_{DD}}{I_{DS}}$)	1
Intrinsic date delay ($\tau = \frac{C_g \Delta V}{I_{av}} = R_{tr}C_g$)	1/S
Power-dissipation per gate ($P=IV$)	$1/S^2$
Power-delay product per gate ($P \times \tau$)	$1/S^3$
Area per device ($A=WL$)	$1/S^2$
Power-dissipation density (P/A)	1

Current Through an n-channel MOS Transistor

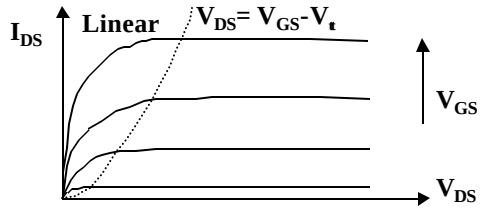


FIGURE 2.2 I-V characteristics of an nMOS transistor

$$I_{os}=\begin{cases} 0 & V_{gs} \le V_{tn} \quad \text{(Cut-off)} \\ \beta_n\left[(V_{gs}-V_{tn})V_{os}-V_{os}^2/2\right] & V_{ds} \le V_{gs}-V_{tn} \quad \text{(Linear in terms of } V_{GS}\text{)} \\ \beta_n = \dfrac{(V_{gs}-V_{tn})}{2} & V_{ds} \ge V_{gs}-V_{tn} \quad \text{(Saturation, independent of } V_{DS}\text{)} \end{cases}$$

$$\beta_n = \mu_n . C_{gox} \cdot \frac{W}{L} \leftarrow \text{Gain Factor}$$

μ_n → electron mobility

$C_{gox} = \dfrac{\varepsilon_{ox}}{\tau_{gox}}$

$\frac{W}{L}$ → geometric dimentsions of the transistor

Ideal Scaling of VLSI Interconnects

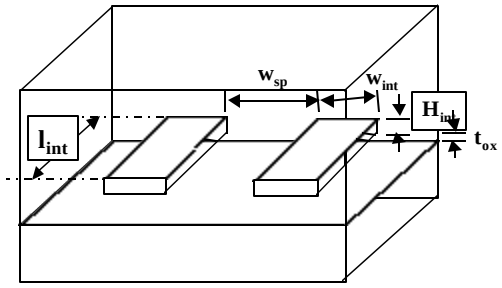


Figure 1.2 Basic interconnection parameters

Assumptions:

- **Cross Sectional dimensions (Wint, Hint, Wsp, Tox) are reduced by S**
- **Die Size and global interconnection Lengths are increased by S_c**

Table 1.2 Scaling of Local and Global Interconnections

Parameter	Scaling Factor
Cross sectional Dimensions (W_{int}, H_{int}, W_{sp}, t_{ox})	1/S
Resistance per unit length ($R_{int} = \tilde{n}_{int}\frac{1}{W_{int}H_{int}}$)	S^2
Capacitance per unit length ($C_{int} = \varepsilon_{ox}\frac{W_{int}}{t_{ox}}$)	1
RC constant per unit length ($R_{int}C_{int}$)	S^2
Local interconnection length (l_{loc})	1/S
Local interconnection RC delay ($R_{int}C_{int}l_{loc}^2$)	1 ←
Die size (D_C)	S_C
Global interconnection length (l_{int})	S_C
Global interconnection RC delay ($R_{int}C_{int}l_{int}^2$)	$S^2(S_C)^2$ ←
Transistor line time of flight (l_{int}/v_c)	S_C

Local Interconnects under Different Scaling Rules

Table 5.1 Scaling of Local Interconnections

Parameter	Ideal Scaling	Qussi-Ideal Scaling	Constant-R Scaling	Generalized Scaling
Thickness (H_{int})	$1/S$	$1/\sqrt{S}$	$1/\sqrt{S}$	$1/S_H$
Width (W_{int})	$1/S$	$1/S$	$1/\sqrt{S}$	$1/S_W$
Separation (W_{sp})	$1/S$	$1/S$	$1/\sqrt{S}$	$1/S_{sp}$
Insulator thickness (t_{ox})	$1/S$	$1/\sqrt{S}$	$1/\sqrt{S}$	$1/S_{ox}$
Length (l_{loc})	$1/S$	$1/S$	$\approx 1/S$	$1/S$
Resistance (R_{int})	S	$\sqrt{S}$	1	$S_W S_H/S$
Capacitance to substrate	$1/S$	$1/S^{3/2}$	$\approx 1/S$	S_{ox}/SS_W
Capacitance between lines	$1/S$	$1/\sqrt{S}$	$\approx 1/S$	S_{sp}/SS_H
RC delay (T)	1	$\approx 1/\sqrt{S}$	$\approx 1/S$	$\approx S_W S_H/S^2$
Voltage drop (IR)	1	$1/\sqrt{S}$	$1/S$	$S_W S_H/S^2$
Current density (J)	S	$\sqrt{S}$	1	$S_W S_H/S$

↑ not good for packing density

Global Interconnects under Different Scaling Rules

Table 5.2 Scaling of Global Interconnections

Parameter	Ideal Scaling	Constant Dimension	Constant Delay	Generalized Scaling
Thickness (H_{int})	$1/S$	1	S_C	$1/S_H$
Width (W_{int})	$1/S$	1	S_C	$1/S_W$
Separation (W_{sp})	$1/S$	1	S_C	$1/S_{sp}$
Insulator thickness (t_{ox})	$1/S$	1	S_C	$1/S_{ox}$
Length (l_{loc})	S_C	S_C	S_C	S_C
Resistance (R_{int})	$S^2 S_C$	S_C	$1/S_C$	$S_W S_H S_C$
Capacitance (C_{int})	S_C	S_C	S_C	$\approx S_C$
RC delay (T)	$S^2 (S_C)^2$	$(S_C)^2$	1	$S_W S_H (S_C)^2$

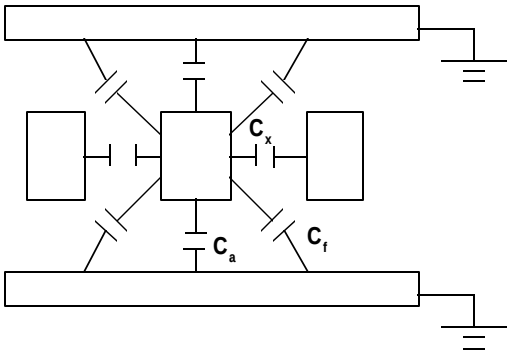
S: Scaling factor for device dimensions.

S_c:Scaling factor for chip size

Interconnect Parameters from NTRS'97

Technology (um)	*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
Res. r (uΩ/cm)	3.3	2.2	2.2	2.2	2.2	1.8
Dielectric constant	3.55	2.75	2.25	1.75	1.75	1.5
Min. wire width	0.25	0.18	0.15	0.13	0.10	0.07
Min. wire spacing	0.34	0.24	0.21	0.17	0.14	0.10
Metal aspect ratio	1.8:1	1.8:1	2.0:1	2.1:1	2.4:1	2.7:1
Via aspect ratio	2.2:1	2.2:1	2.4:1	2.5:1	2.7:1	2.9:1
Vdd (V)	2.15	1.65	1.35	1.35	1.05	0.75

Capacitance Computation

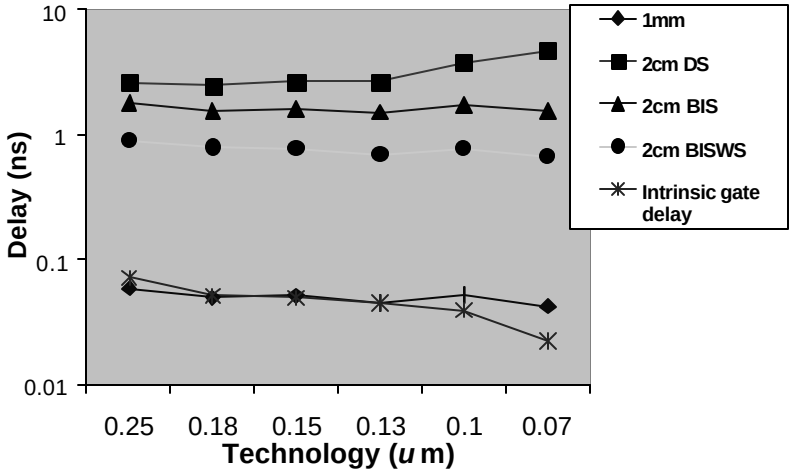


- **Capacitance extraction using a 3D field solver (FastCap)**

Derived Interconnect & Device Parameters

Technology (um)		*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
2X min. width & spacing	Ca (aF/um)	29.0	21.2	16.2	12.0	14.4	8.56
	Cf (aF/um)	41.8	30.2	24.8	18.3	14.1	14.8
	Cx(aF/um)	71.0	58.3	49.4	42.8	45.3	41.6
5X min. width & spacing	Ca (aF/um)	73.5	53.6	40.6	30.0	26.6	19.5
	Cf (aF/um)	63.5	47.3	38.4	28.5	28.2	23.6
	Cx(aF/um)	18.3	16.9	15.4	14.8	16.5	16.7
Buffer input cap. (fF)		0.17	0.12	0.11	0.085	0.070	0.042
Buffer Rd (x10K^{W})		1.71	1.86	2.26	2.25	2.39	2.42
Buffer intrin. delay (ps)		70.5	51.1	48.7	45.8	39.2	21.9

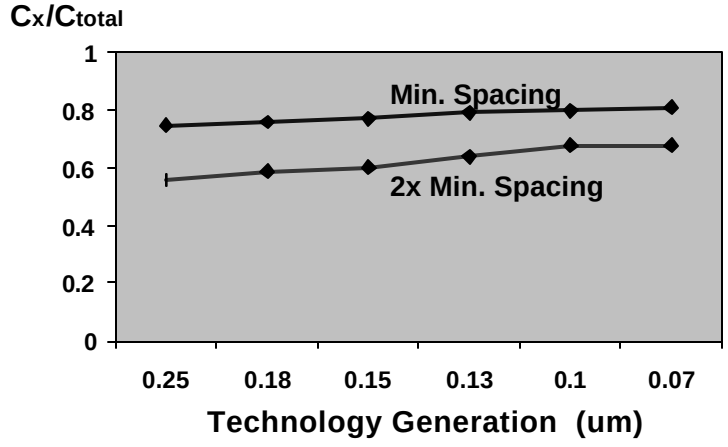
Impact of Interconnect Optimization on Future Technology Generations



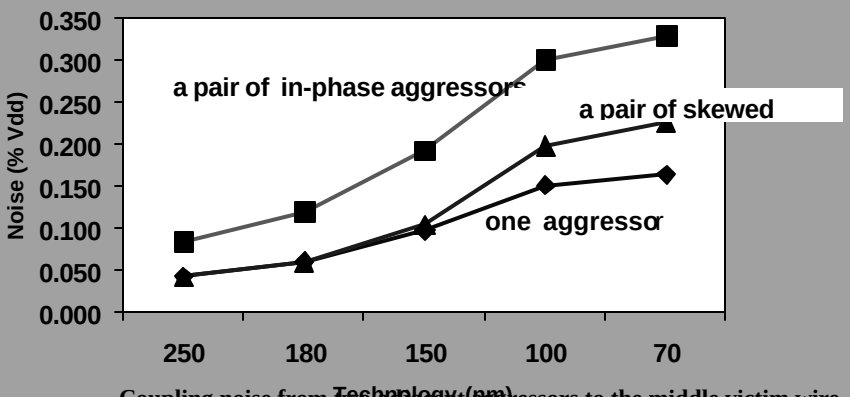
Impact of Interconnect Optimization on Future Technology Generations

Technology (um)	*0.25*	*0.18*	*0.15*	*0.13*	*0.10*	*0.07*
1mm (ns)	0.059	0.049	0.051	0.044	0.052	0.042
2cm DS (ns)	2.589	2.48	2.65	2.62	3.73	4.67
2cm BIS (ns)	1.779	1.55	1.59	1.51	1.74	1.55
2cm BISWS (ns)	0.895	0.793	0.77	0.7	0.77	0.672

Significance of Coupling Capacitance



Coupling Noise



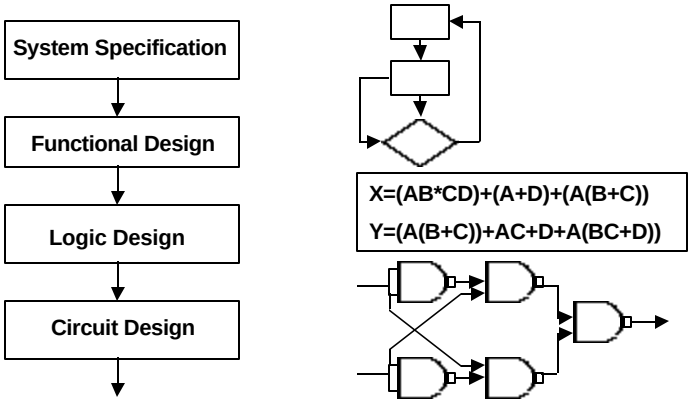
Coupling noise from two adjacent aggressors to the middle victim wire with 2x min. spacing. Rise time is 10% of project clock period.

•**Capacitive coupling depends strongly on both spatial and temporal relations!**

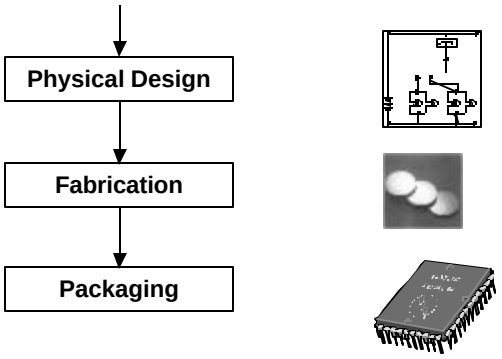
Implications

- **Communication is more expensive than computation**
- **Interconnect performance has become the bottleneck of the overall circuit/system performance**
- **Interconnect modeling and optimization has become very difficult due to the distributed nature of interconnects and their spatial and temporal interactions**
- **A new design paradigm/flow is needed to handle interconnect-dominated designs in the future**

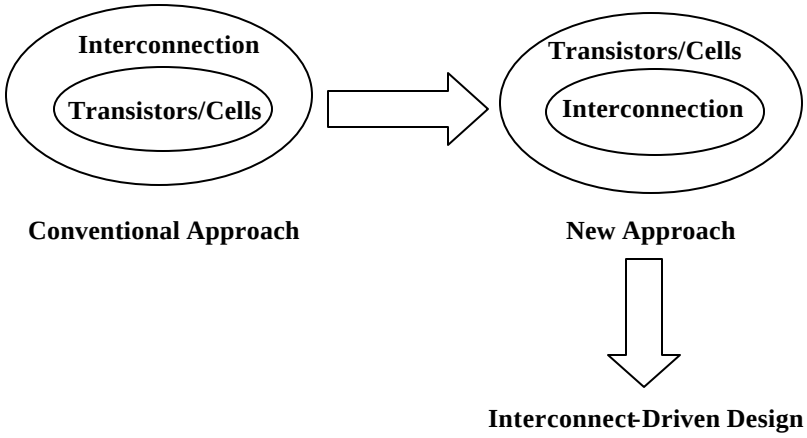
VLSI Design Cycle



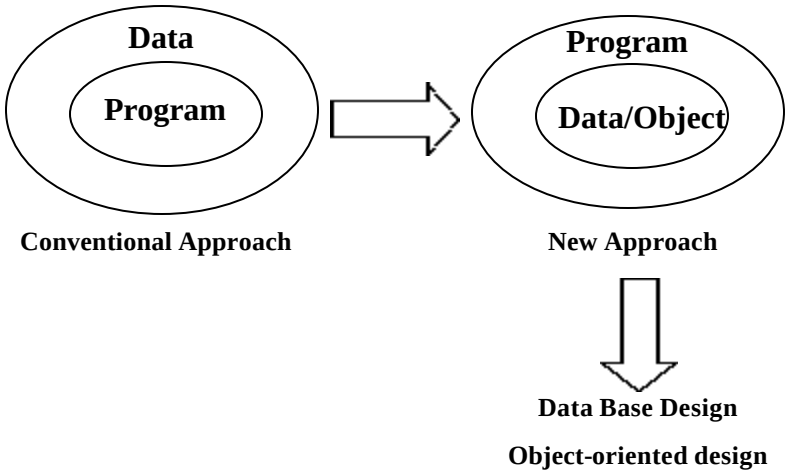
VLSI Design Cycle (cont.)



Need A New Paradigm for VLSI Design



Paradigm Change in Software Design



Summary

- **Technology scaling according to Moore's Law has been the driving force behind the exponential growth of the semiconductor industry**
- **Interconnect (esp. global interconnect) performance and noise have become the bottleneck of the overall system design**
- **Interconnect modeling and optimization has become very important, yet difficult**
- **A new design paradigm is needed for interconnect-driven (or interconnect-centric) design**

Homework (due next Thursday)

- **Read ITRS ORTC and Interconnect**
  - **ORTC: overall roadmap technology characteristics**
  - **http://public.itrs.net/Files/2000UpdateFinal/2kUdfinal.htm**
  - **Find two categories of differences between NTRS'97 (in this notes) and ITRS'00 interconnect characteristics, and explain reasons for such changes**