Quartus II Version 6.0 Handbook

Volume 1: Design & Synthesis

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Chapter Revision Dates

The chapters in this book, *Quartus II Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

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Chapter 11. Synopsys Design Compiler FPGA Support
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Chapter 12. Analyzing Designs with Quartus II Netlist Viewers
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About this Handbook

This handbook provides comprehensive information about the Altera® Quartus® II design software, version 6.0.

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Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section I. Design Flows

The Altera® Quartus® II, version 6.0 design software provides a complete multi-platform design environment that easily adapts to your specific design needs. The Quartus II software also allows you to use the Quartus II graphical user interface, EDA tool interface, or command-line interface for each phase of the design flow. This section explains the Quartus II, version 6.0 software options that are available for each of these flows.

This section includes the following chapters:

Revision History

The chapter, *Hierarchical Block-Based & Team-Based Design Flows*, was removed from this handbook. The table below shows the revision history for Chapters 1 to 4.

Chapter(s)	Date / Version	Changes Made (Part 1 of 2)
1	May 2006 v6.0.0	Name changed to *Quartus II Incremental Compilation for Hierarchical & Team-Based Design*. Updated for the Quartus II software version 6.0.0 • Added new device support information. • Added top-down and bottom-up design flow information. • Added incremental compilation design compiling information. • Added recommendations for creating good floorplan location assignments. • Added register packing & partition boundary information. • Added engineering management with the Chip Editor. • Added information on how to check and save to reapply SignalProbe™. • Added user scenarios.
	December 2005 v5.1.1	Minor typographic update.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	August 2005 v5.0.1	Added documentation on cross-partition register packing.
	May 2005 v5.0.0	Initial release.
2	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	December 2005 v5.1.1	Minor typographic and formatting updates.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	Chapter 2 was formerly Chapter 1 in version 4.2.
	Dec. 2004 v2.1	Updated for Quartus II software version 4.2. • Chapter 1 was formerly Chapter 2. • General formatting, editing updates, and figure updates. • FLEX® 600 device support added. • Assignment Editor, Timing Assignments, and Synthesis updated. • APEX II support for balanced optimization technique removed, MAX II support added. • Minor updates to Place & Route. • Tcl commands no longer supported for the Quartus II Simulator Tool. • Excel-based power calculator replaced by PowerPlay Early Power Estimation spreadsheet. • Added support for erase capability for CPLDs.
	June 2004 v2.0	• Updates to tables, figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.

Chapter(s)	Date / Version	Changes Made (Part 2 of 2)
3	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	• Chapter 3 was formerly Chapter 2. • Updated for consistency with the *Quartus II Support for HardCopy II Devices* and *Quartus II Support for HardCopy Stratix Devices* chapters in the *HardCopy Series Handbook*.
	Jan. 2005 v2.1	• Added HardCopy II Device Material.
	Dec. 2004 v2.1	• Chapter 2 was formerly Chapter 3. • Updates to tables, figures. • New functionality for Quartus II software 4.2
	June 2004 v2.0	• Updates to tables, figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.
4	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	Chapter 4 was formerly Chapter 3 in version 4.2.
	Dec. 2004 v2.1	Updated for Quartus II software version 4.2: • Chapter 4 was formerly Chapter 3. • General formatting and editing updates. • Device family support descriptions updated. • Updated HardCopy structured support for performance improvements. • Quartus II Archive File automatically receives buffer insertion. • Power Calculator now Power Estimator for affected devices. • Updates to tables, figures. • The description of How to Design HardCopy Stratix Devices was updated. • The description of HardCopy Timing Optimization Wizard was updated. • HardCopy Floorplans & Timing Modules was renamed to Design Optimization. • The description of Performance Estimation was updated. • Added new section on Buffer Insertion. • Location Constraints was updated. • Targeting Designs to HardCopy APEX 20KC and HardCopy APEX 20KE Devices was removed. • A new section Altera Recommended HDL Coding Guidelines was added. • Table 2–5 was added. It lists the HardCopy Stratix design files collected by the hardCopy Files Wizard. • The description of the HardCopy APEX Power Estimator was updated. • A new section on Targeting Designs to HardCopy APEX Devices was added.
	June 2004 v2.0	• Updates to tables, figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.

1. Quartus II Incremental Compilation for Hierarchical & Team-Based Design

QII51015-6.0.0

Introduction

For today's high-density, high-performance FPGA designs, the ability to iterate rapidly during the design and debugging stages is critical. The Quartus® II software delivers advanced technology to create designs for high-density FPGAs. Altera® has introduced the FPGA industry's first true incremental design and compilation flow, providing the following benefits:

- Preserves the results and performance for unchanged logic in your design as you make changes elsewhere.
- Reduces design iteration time by an average of about 60%, allowing you to perform more design iterations per day and achieve timing closure more efficiently.
- Provides ease of use through the GUI.
- Includes Tcl scripting, command-line, and makefile support.
- Facilitates modular and team-based design flows using top-down or bottom-up methodologies.
- Supports full incremental compilation for Stratix®, Stratix II, Cyclone™ , and Cyclone II devices, and incremental synthesis for the MAX® II device family. Supports full incremental compilation for native HardCopy® II device development, however, you cannot migrate a Stratix II design with full incremental compilation enabled to a HardCopy II device.

Quartus II incremental compilation is an optional compilation flow. This chapter provides an overview of the Quartus II design flow with and without incremental compilation. However, for an overview of the Quartus II design flow and features, refer to the *Introduction to Quartus II Manual*.

To take advantage of incremental compilation, organize your design into logical partitions and physical regions for synthesis and fitting (or place and route). Incremental compilation preserves the compilation results and performance of unchanged partitions in your design, dramatically reducing design iteration time by focusing new compilations only on changed design partitions. New compilation results are then merged with the previous compilation results from unchanged design partitions. Additionally, you can target optimization techniques, such as physical synthesis, to specific design partitions while leaving other partitions untouched.

In conventional FPGA design, a hierarchical design is flattened into a single netlist before logic synthesis and fitting, and the entire design is recompiled every time the design changes. The Quartus II incremental compilation feature provides the ability to partition a design along any of its hierarchical boundaries. The Quartus II software separately synthesizes and fits each individual hierarchical design partition then merges the partitions into a complete netlist for subsequent stages of the compilation flow. When recompiling the design, you can choose to use source code, post-synthesis results, or post-fitting results for each partition. If you want to preserve the fitter results, you can choose to keep just the fitter netlist, keep the placement results, or keep both the placement and routing results.

Incremental compilation supports top-down design methodologies, in which one designer manages the project for the entire design, as well as bottom-up design methodologies in which each design block can be developed independently. Bottom-up methodologies include team-based design flows in which design partitions are created by team members in another location or by third-party intellectual property (IP) providers. For bottom-up flows, you can generate scripts from the top-level design that pass constraints to lower-level design blocks compiled in separate Quartus II projects.

The goal of this chapter is to provide the following information:

- Provide an overview of the Quartus II design flow with and without incremental compilation
- Describe how to use the Quartus II incremental compilation feature
- Provide you the level of understanding required to make good design decisions to achieve timing closure while speeding up design iterations
- Present several applications of incremental compilation in the form of user scenarios, along with the rationale behind them and the steps required to carry out the tasks

This chapter includes the following sections:

Quartus II Design Flow

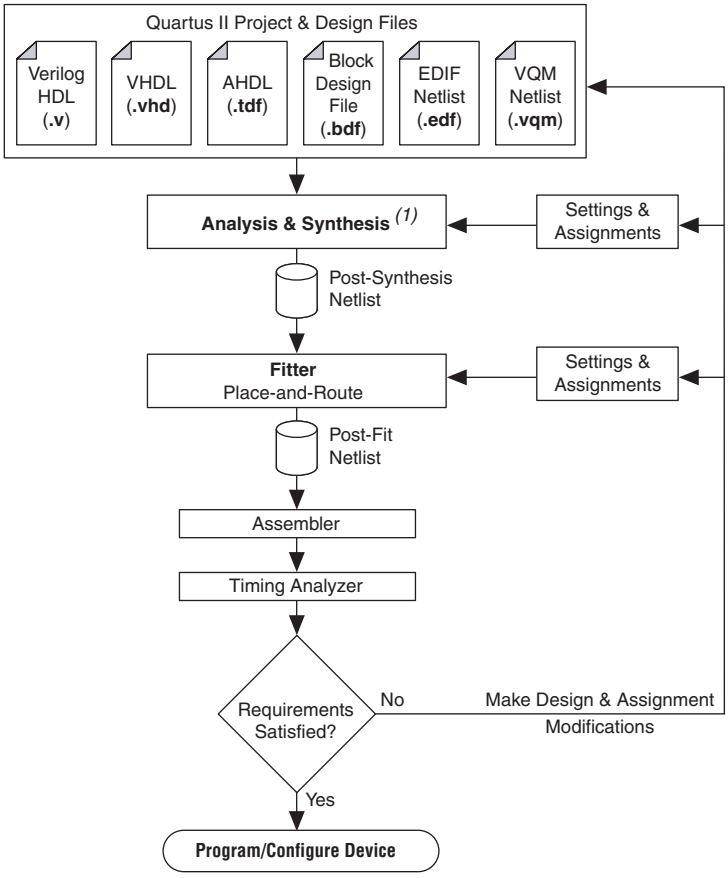
Quartus II incremental compilation enhances the standard Quartus II design flow by allowing you to reuse satisfactory results from previous compilations and save compilation time. This section outlines the standard compilation flow and the incremental flow, highlights the differences, and explains some of the reasons you might want to use the incremental flow.

The standard Quartus II compilation flow consists of the following essential modules:

- **Analysis & Synthesis**—performs logic synthesis to minimize the design logic and performs technology mapping to implement the design logic using device resources such as logic elements. This stage also generates the project database that integrates the design files (including netlists from third-party synthesis tools). When you are using EDIF or VQM netlists created by third-party synthesis tools, the Analysis & Synthesis stage performs logic synthesis and technology mapping only for black boxes and Altera megafunctions.
- **Fitter**—places and routes the logic of a design into a device.
- **Assembler**—converts the Fitter's device, logic, and pin assignments into programming files for the device.
- **Timing Analyzer**—analyzes and validates the timing performance of all the logic in a design.

Figure 1–1 shows a block diagram of the Quartus II standard design flow.

Figure 1–1. Quartus II Standard Design Flow



Note to Figure 1–1:

(1) When you are using EDIF or VQM netlists created by third-party EDA synthesis tools, the Analysis & Synthesis stage of the compilation is performed to create the design database, but logic synthesis and technology mapping are performed only for black boxes and Altera megafunctions.

In the standard Quartus II compilation flow, you can use smart compilation to allow the compiler to determine which compiler modules are required based on the changes made to the design since the last smart compilation, and then skip any modules that are not required. For example, when smart compilation is selected, the compiler skips the Analysis & Synthesis module if the design source files were unchanged. Smart compilation skips only entire compiler stages. It cannot make

incremental changes within a given stage of the compilation flow. On the Assignments menu, click **Settings**. In the Category list, select **Compilation Process Settings** and click **Use Smart Compilation**.

In the standard compilation flow, all of the source code is processed with the Analysis & Synthesis module, and all the logic is placed by the Fitter module whenever the design is recompiled after any change in any part of the design. One reason for this behavior is to obtain optimal quality of results. By processing the entire design, the compiler can perform global optimizations to improve area and performance.

However, there are situations in which a more incremental compilation flow is desirable. When the design partitions are well chosen and placed in the device floorplan, you can speed up your design compilation time while maintaining or even improving the quality of results. "Creating Design Partitions" on page 1–17 provides tips for choosing design partitions.

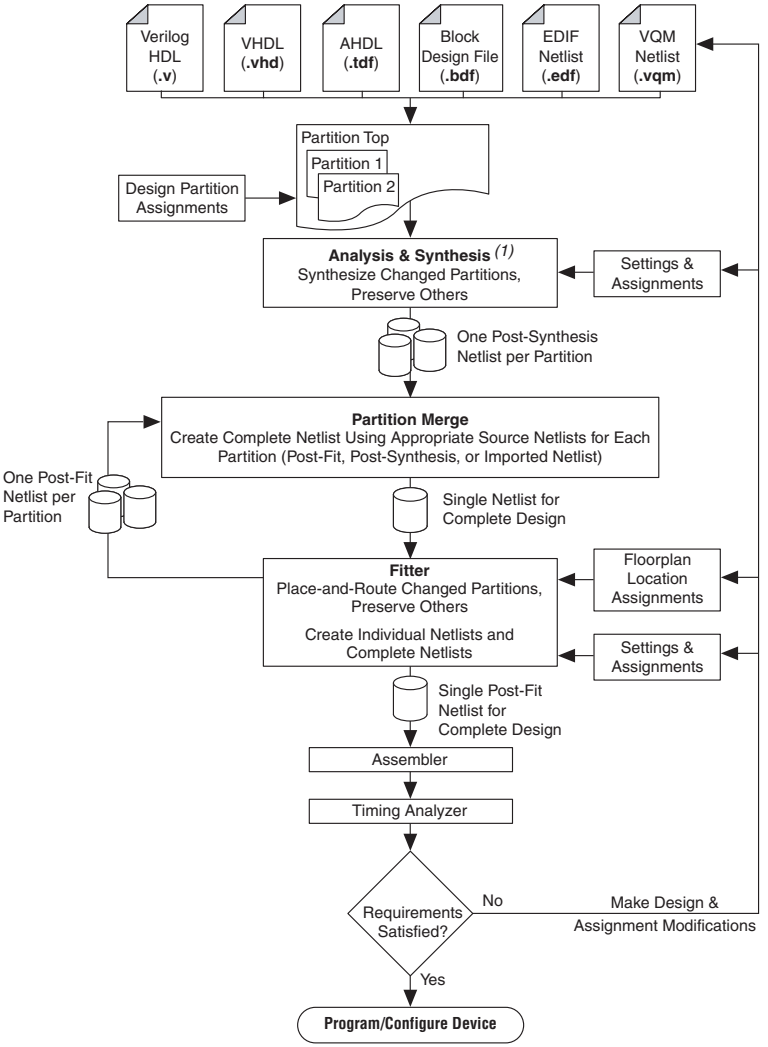
You may want to use incremental compilation later in the design cycle when you are not interested in improving the majority of the design any further, and want to make changes to or optimize one specific block. In this case, you may want to preserve the performance of modules that are unmodified and to reduce compilation time on subsequent iterations. There are also situations in which incremental compilation is useful both for reducing compilation time and for achieving timing closure. For example, you may want to specify which partitions should be preserved in subsequent incremental compilations, and then recompile the other partitions with advanced optimizations turned on.

You might also have part of your design that is not yet complete, for which you can create an empty partition while compiling the completed partitions, and then save results for the complete partitions while you work on the new part of the design. Alternately, different designers or IP providers may be working on different blocks of the design using a team-based methodology, and you want to combine them in a bottom-up compilation flow.

For more detailed user scenarios, refer to "User Scenarios—Incremental Compilation Application Examples" on page 1–48.

Figure 1–2 shows a block diagram of the Quartus II design flow using incremental compilation.

Figure 1–2. Quartus II Design Flow Using Incremental Compilation



Note to Figure 1–2:

(1) When you are using EDIF or VQM netlists created by third-party EDA synthesis tools, the Analysis & Synthesis stage of the compilation is performed to create the design database, but logic synthesis and technology mapping are performed only for black boxes and Altera megafunctions.

In this flow, you partition the design, then perform logic synthesis and technology mapping for each partition individually with Analysis & Synthesis.

Analysis & Synthesis reads the project assignments to determine the partition boundaries. The example in Figure 1–2 shows a top-level partition and two lower-level partitions. If any part of the design changes, Analysis & Synthesis processes the changed partitions and keeps the existing netlist for the unchanged partitions. After completion of Analysis & Synthesis, there is one post-synthesis netlist for each partition.

The partition merge step creates a single, complete netlist that can be comprised of post-synthesis and/or post-fitting netlists, or netlists imported from lower-level projects, depending on the netlist type you specify for each partition. For more information, refer to "Setting the Netlist Type for Design Partitions" on page 1–26.

The Fitter then processes the merged netlist, preserving the placement or placement and routing of unchanged partitions, refitting only those partitions that have changed. The Fitter generates the complete netlist for use in further stages of the compilation flow, including timing analysis and programming file generation. It also generates individual netlists for each partition so that the partition merge step can use the post-fit netlist to preserve the placement and routing of a partition if you specify to do so in future compilations.

If the design does not meet its requirements (functionality, timing, or area), you can make changes to the design and recompile. The Quartus II software does not resynthesize or refit unchanged partitions that have a netlist type assignment that specifies the use of a post-synthesis or post-fit netlist, respectively.

Top-Down vs. Bottom-Up Design Flows

The Quartus II incremental compilation feature supports both top-down and bottom-up compilation flows. With top-down compilation, one designer or project lead compiles the entire design in the software. Different designers or IP providers can design and verify different parts of the design, and the project lead can add design entities to the project as they are completed. However the project lead compiles and optimizes the top-level project as a whole. Completed parts of the design can have fitting results and performance fixed as other parts of the design are changing.

Bottom-up design flows allow individual designers to complete the optimization of their design in separate projects and then integrate each lower-level project into one top-level project. Incremental compilation

provides export and import features to enable this design methodology. Designers of lower-level blocks can export the optimized netlist for their design, along with a set of assignments such as LogicLock regions. Then the project lead imports each design block as a design partition in a top-level project. In this case, the project lead must provide guidance to designers of lower-level blocks to ensure that each partition uses the appropriate device resources.

It is important to realize that with the full incremental compilation flow, users who traditionally relied on a bottom-up approach for the sole reason of performance preservation can now employ a top-down approach to achieve the same goal. This ability is important for two reasons. First, a top-down flow is generally simpler to perform than its bottom-up counterpart. For example, the need to export and import lower-level designs is eliminated. Second, a top-down approach provides the design software with information about the entire design so it can perform global optimizations. In a bottom-up design methodology, you must perform resource balancing and time-budgeting because the software does not have any information about the other partitions in the top-level design when it compiles individual lower-level partitions. For more information about the export and import operations, and how to use design partition scripts to help with design planning, refer to "Exporting & Importing Partitions for Bottom-Up Design Flows" on page 1–35.

Using Incremental Synthesis Only Instead of Full Incremental Compilation

You can turn on incremental compilation for only the synthesis stage of compilation to perform incremental synthesis, with no incremental place-and-route. In this mode, the Fitter uses a flattened netlist without partition boundaries and therefore performs cross-boundary optimizations that help timing performance. The difference between this flow and the one shown in Figure 1–2 is that the partition merge stage does not accept post-fit netlists produced by the Fitter, and the Fitter does not compile partitions separately.

Incremental synthesis only is the default compilation option when using incremental compilation. This is because, although the potential benefit offered by **Full incremental compilation** can be higher than that offered by incremental synthesis alone, many additional design considerations and a deeper understanding of the compilation process are required to use the full incremental compilation flow successfully.

Table 1–1 lists the different characteristics between the two compilation options.

Table 1–1. Characteristics of Using Incremental Synthesis Only, Compared to Full Incremental Compilation

Characteristic	Incremental Synthesis Only	Full Incremental Compilation
Compilation Time Savings	Roughly 15-40% of total time; savings limited to Quartus II integrated synthesis.	Roughly 50-70% of total time; savings in both Quartus II integrated synthesis and the Fitter.
Performance Preservation	None since placement cannot be preserved.	Excellent when critical paths are contained within a partition, because you can preserve post-fitting information for unchanged partitions.
Node Name Preservation	Preserves post-synthesis node names for unchanged partitions.	Preserves post-fitting node names for unchanged partitions.
Area Changes	Area might increase due to lack of cross-boundary optimizations. If design is partitioned appropriately, small or no change in area.	Area increases by 5% on average in addition to any synthesis area change, since placement and register packing are restricted.
f_{MAX} Changes	f_{MAX} might be reduced due to lack of cross-boundary optimizations. If the design is partitioned appropriately, no negative impact on f_{MAX}.	If the design is partitioned and the floorplan location assignments are created appropriately, no negative impact on f_{MAX}. You may get a slight performance increase by employing a good partition and floorplan scheme.
Ease of Use	Simply create partitions.	Specify which partitions you want to preserve, and create floorplan location assignments in most cases.
Floorplan Creation	Not required.	Required in most cases for best quality of results.
When Design is Resynthesized	Change in source code or synthesis assignments.	Change in source code (unless you specify to use a post-fit netlist strictly), or when you specify to use the source file.
When Design is Refit	Always	Change in source code (unless you specify to use a post-fit netlist strictly), when you specify to use the source or post-synthesis netlist, or when you specify to use a post-fit netlist with a fitter preservation level of Netlist Only.
When to Use in the Design Flow	Can use with equal value throughout the design process.	Useful mostly when performing placement and routing, especially during iterative timing closure and for late design changes, or when part of the design is incomplete.
User Base	Quartus II integrated synthesis users only; limited application for third-party synthesis tool users.	Potentially all Quartus II software users; typically more experienced users who may have previously used LogicLock™ assignments.

For usage details specific to the **Incremental synthesis only** option, refer to the *Incremental Synthesis* section in the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

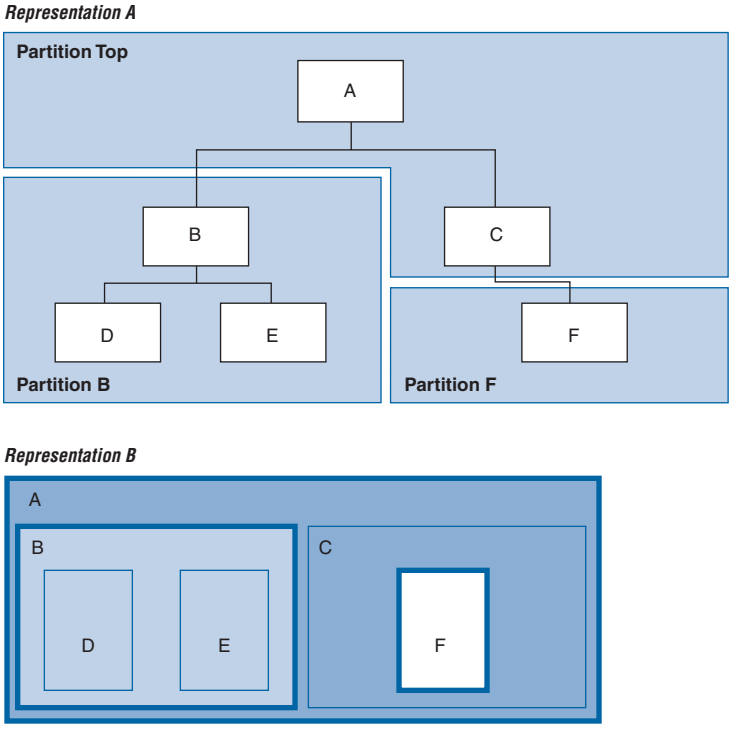
Design Partitions

It is common design practice to create modular or hierarchical designs in which you develop each design entity separately and then instantiate them in a higher-level entity, forming a complete design. The software does not consider each design entity automatically to be a design partition for incremental compilation; rather, you must designate one or more design hierarchies below the top-level project to be a design partition. Creating partitions prevents the compiler from performing optimizations across partition boundaries, as discussed in "Creating Design Partitions" on page 1–17 and illustrated in Figure 1–8. However, this allows for separate synthesis and placement for each partition, making incremental compilation possible.

Partitions must have the same boundaries as hierarchical blocks in the design because partitions cannot be a portion of the logic within a hierarchical entity. When you declare a partition, every hierarchical entity within that partition becomes part of the same partition. You can create new partitions for hierarchical entities within an existing partition, in which case the entities within the new partition are no longer included with the higher-level partition, as described in the following example.

In Figure 1–3, hierarchical entities **B** and **F** form partitions in the complete design, which is made up of entities **A**, **B**, **C**, **D**, **E**, and **F**. The shaded boxes in Representation A indicate design partitions in a "tree" representation of the hierarchy. In Representation B, the lower-level entities are represented inside the higher-level entities, and the partitions are illustrated with different colored shading. The top-level partition, called Top, automatically contains the top-level entity in the design, and contains any logic not defined as part of another partition. The design file for the top-level may be just a wrapper for the hierarchical entities below it, or it may contain its own logic. In this example, the partition for top-level entity **A** also includes the logic in one of its lower-level entities, **C**. Because entity **F** is contained in its own partition, it is not treated as part of the top-level partition. Another separate partition, **B**, contains the logic in entities **B**, **D**, and **E**.

Figure 1–3. Partitions in a Hierarchical Design



Design Partitions Compared to Physical Regions

Design partitions for incremental compilation are logical partitions, different from physical regions in the device floorplan. Physical regions specify locations in the device floorplan using LogicLock assignments in the Quartus II software. Physical regions have a size and location on the device floorplan, and you can assign multiple design instances and nodes to a physical region to place them close to each other. A logical design partition does not refer to a physical section of the device and does not directly control the placement of instances. A logical design partition sets up a virtual boundary between design hierarchies so each is compiled separately, preventing logical optimizations from occurring between them.

Altera recommends that you assign each design partition to a physical region using the LogicLock feature to improve quality of results when performing a full incremental compilation. Create floorplan location assignments for design partitions using LogicLock regions as discussed in "Creating a Design Floorplan With LogicLock Location Assignments" on page 1–29. Physical location assignments are not required for logical design partitions if you are using the **Incremental Synthesis Only** option.

Preparing a Design for Incremental Compilation

To set up your design for incremental compilation, use the following general steps. Detailed descriptions for some of these steps are included in later sections of this chapter. The flow chart in Figure 1–5 illustrates these steps in the complete incremental design flow.

1. Elaborate the design. On the Processing menu, point to Start and click **Start Analysis & Elaboration**, or run any compilation flow that includes this step. This allows the Quartus II software to identify your design's hierarchy.

2. On the Assignments menu, click **Settings**. On the Compilation Process page of the **Settings** dialog box, select **Incremental compilation** and turn on **Full incremental compilation**, as shown in Figure 1–4.

3. Create partitions in your design by applying the **Set as Design Partition** or `PARTITION_HIERARCHY` assignment to the appropriate instances. Refer to the section "Creating Design Partitions" on page 1–17 for more details on design partitions and how to make good assignments.

When you specify your first partition, a dialog box is shown that asks whether you wish to enable incremental compilation if you have not already done so. Selecting **Full incremental compilation** in this dialog box also turns on incremental compilation as in Step 2. You can also turn on incremental compilation in the **Design Partitions Window** on the Assignments menu.

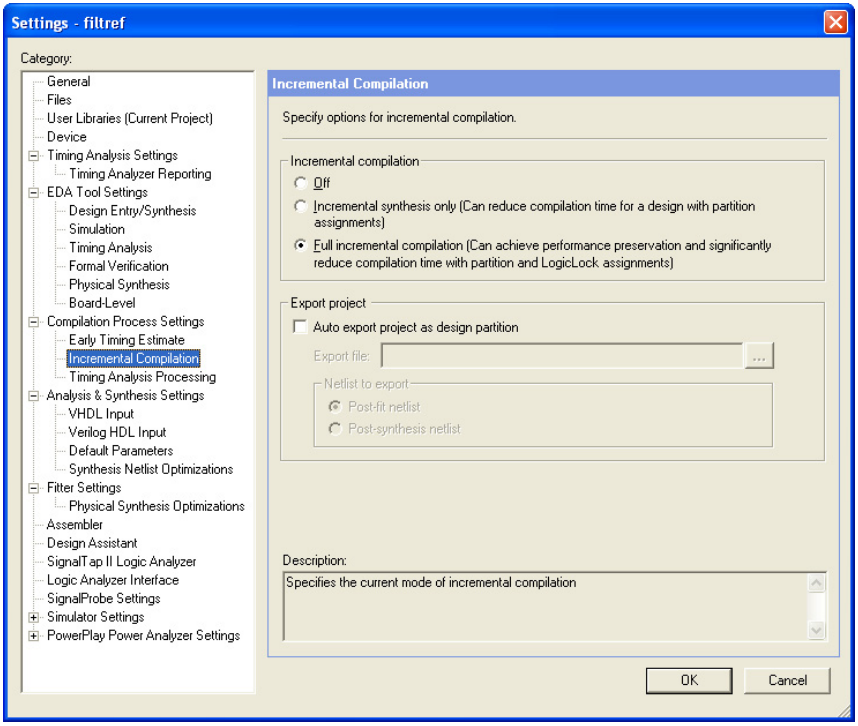
Selecting **Off** on the Incremental Compilation page of the **Settings** dialog box turns off all forms of incremental synthesis and incremental compilation, but does not remove any partition assignments. Partition assignments have no effect on the design if incremental compilation is turned off.

4. Make location assignments for each partition in the design with the LogicLock feature to create a design floorplan. Each partition should be assigned to a physical region on the device. Refer to the section "Creating a Design Floorplan With LogicLock Location Assignments" on page 1–29 for details on making these assignments.

5. On the Processing menu, click **Start Compilation** to compile the design. The first compilation after making the partition and LogicLock assignments is a complete compilation that prepares the design for subsequent incremental compilations.

To use incremental synthesis only, follow Step 1 through Step 3, but, in Step 2 select **Incremental synthesis only** instead of **Full incremental compilation** on the **Incremental Compilation** page in the **Settings** dialog box in Figure 1–4.

Figure 1–4. Full Incremental Compilation Enabled in the Settings Dialog Box



For details specific to using only the incremental synthesis option, refer to the *Incremental Synthesis* section in the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

Compiling a Design Using Incremental Compilation

After compiling the design once and then making changes, you can take advantage of incremental compilation to recompile the changed parts of the design while preserving the results for the unchanged partitions, saving time on subsequent compilations. To do this, perform the following general steps:

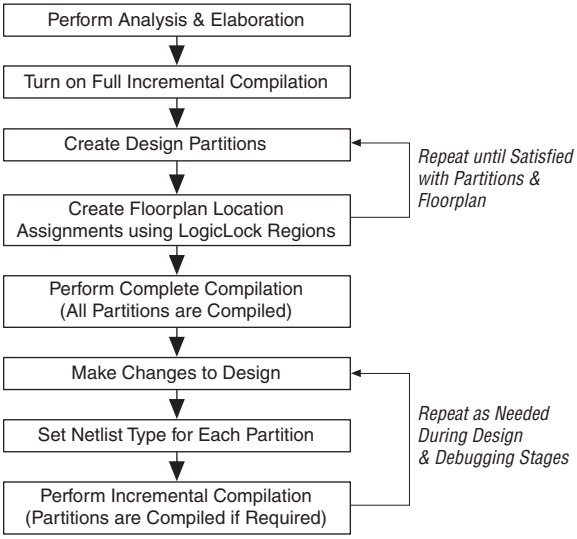
1. To preserve previous compilation results for a partition, set the **Netlist Type** assignment for that partition to **Post-Fit**. To save just the synthesis results, set the **Netlist Type** assignment for that partition to **Post-Synthesis.** If you have imported a partition from another Quartus II project, choose **Imported**. For details on setting this partition property and specifying the fitter preservation level for post-fit netlists, refer to "Setting the Netlist Type for Design Partitions" on page 1–26.

2. Compile the design. When you start a compilation for a partitioned design with incremental compilation turned on, the Quartus II software automatically uses the incremental compilation flow, preserving the results as specified in Step 1.

If you preserve the compilation results using the Post-Fit netlist, you do not have to back-annotate logic location assignments. You should not use the incremental compilation and the back-annotation features in the same Quartus II project.

The flow chart in Figure 1–5 illustrates these steps in the complete incremental design flow.

Figure 1–5. Summary of Design Flow Using Incremental Compilation



What Represents a Source Change for Incremental Compilation?

The Quartus II software uses an internal checksum to determine whether the contents of a source file have changed. Source files are the design files used to create the design, and consist of VHDL files, Verilog HDL files, AHDL files, Block Design Files (**.bdf**), EDIF netlists, and VQM netlists. Changes in other files such as vector waveform files for simulation do not trigger recompilation.

The project database folder (**\db**) includes all the netlist information for previous compilations. To avoid unnecessary recompilations, the database files must not be altered or deleted.

Synthesis and Fitter assignments, including optimization settings, timing assignments, or Fitter location assignments such as pin assignments or LogicLock assignments, do not trigger automatic recompilation in the incremental compilation flow. To recompile a partition with new assignments, change the **Netlist Type** assignment for that partition to **Source File** to recompile with all new settings, or to **Post-Synthesis** to recompile using existing synthesis results but new fitter settings, or to **Post-Fit** with the **Fitter preservation Level** set to **Placement** to re-run routing using existing placement results except for any new routing settings including delay chain settings. For information about the **Netlist Type** and **Fitter Preservation Level** assignments, refer to "Setting the Netlist Type for Design Partitions" on page 1–26.

Determining Which Partitions Will be Recompiled

When design files in a partition have dependencies on other files, changing one file may trigger an automatic recompilation of another file. The **Partition Dependent Files** table in the Analysis & Synthesis report lists the design files that contribute to each design partition, so you can use this table to determine which files are recompiled when a specific partition is recompiled.

For example, if a design has files **a.v** that contains entity **a**, **b.v** that contains entity **b**, and **c.v**, that contains entity **c**, then the **Partition Dependent Files** table for the partition containing entity **a** lists file **a.v**, the table for the partition containing entity **b** lists file **b.v**, and the table for the partition containing entity c lists file **c.v**. Any dependencies are transitive, so if file **a** depends on **b**, and **b** depends on **c**, then the entities in file **a** depend on files **b** and **c** so entities **b** an **c** are listed in the report table.

If a design contains common files, such as a file `includes.v` that is referenced in each entity by the command `include includes.v`, then all partitions are dependent on this file, and a change to `includes.v` causes the entire design to be recompiled. The VHDL statement `use work.all` also typically results in unnecessary recompilations.

To avoid this type of problem, ensure that files common to all entities such as a common include file contain only the set of information that is truly common to all entities. Remove `use work.all` statements in your VHDL file or replace them by including only the specific packages needed for each entity.

Forcing Use of the Post-Fitting Netlist When a Source File has Changed

Forcing the use of the post-fitting netlist when the contents of a source file has changed is recommended only for advanced users who thoroughly understand when a partition must be recompiled. To force the Fitter to use a previously generated post-fit netlist when there are changes to the source files, you can use the **Post-Fit (Strict)** Netlist Type assignment. For information about the **Post-Fit (Strict)** Netlist Type, refer to "Setting the Netlist Type for Design Partitions" on page 1–26.

Misuse of the **Post-Fit (Strict)** Netlist Type can result in the generation of a functionally incorrect netlist when source design files change. Use caution in applying this assignment.

Creating Design Partitions

You can make partition assignments to HDL or schematic design instances, or to VQM or EDIF netlist instances (from third-party synthesis tools). To take advantage of incremental compilation when source files change, the top-level design entity of each partition should have a unique design file. If you define two different entities of separate partitions but they are in the same design file, you cannot maintain incremental compilation because the software would have to recompile both partitions if you changed either entity in the design file.

When you are using a third-party synthesis tool, create a separate netlist file for each partition to allow each partition to be treated incrementally. To create separate netlists for each partition, you may have to create a top-level HDL wrapper file that instantiates the lower-level netlist files and then create separate projects in your synthesis tool for each of the lower-level partitions. In this case, the lower-level blocks should be treated as a black box in the top-level design. Some synthesis tools allow you to create separate netlist files for different design blocks within a single project.

For information on using incremental compilation with third-party synthesis tools, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

For suggestions on determining which parts of your design should be set as design partitions, refer to "Guidelines for Creating Good Design Partitions" on page 1–20.

Creating Design Partitions in the GUI

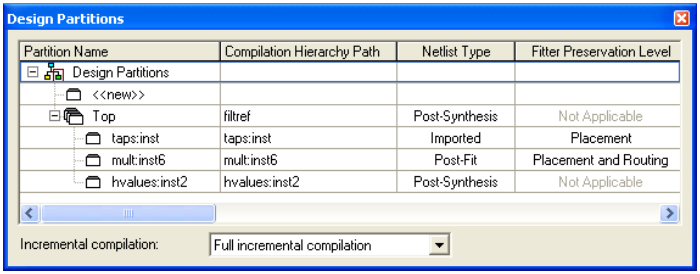
You can create design partitions in the Quartus II GUI with the Design Partitions Window or the Project Navigator.

On the Assignments menu, click **Design Partitions Window** (Figure 1–6) to create your partitions in one of the following ways:

- Create new partitions for one or more instances by dragging and dropping them from the **Hierarchy** tab of the **Project Navigator**, into the Design Partitions window. Using this method, you can create multiple partitions at once.
- Create new partitions by double-clicking the <<*new*>> cell in the Partition Name column. In the **Create New Partitions** dialog box, select the design instance and click **OK**.

To delete partitions in the Design Partitions window, right-click a partition and click **Delete**, or press the **Delete** key.

Figure 1–6. Design Partitions Window

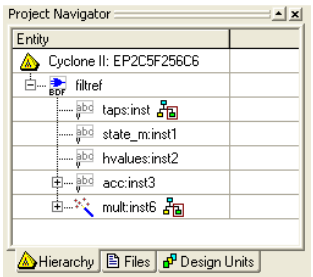


Alternately, you can use the list of instances under the **Hierarchy** tab in the **Project Navigator**. Right-click on an instance in the **Project Navigator** and click **Set as Design Partition**.

A design partition icon appears next to each instance that is set as a partition (Figure 1–7).

To remove an existing partition assignment, right-click the instance in the **Project Navigator** and click **Set as Design Partition** again. (This process turns off the option.)

Figure 1–7. Project Navigator Showing Design Partitions



Partition Name

When you create a partition, the Quartus II software automatically generates a name based on the instance name and hierarchy path. Change the name by double-clicking on the partition name in the Design Partitions window, or right-click the partition and click **Rename**. Alternately, you can right-click the partition in the Design Partitions window and click **Properties** to open the **Design Partition Properties** dialog box. On the **General** tab, enter the Name. By renaming your

partitions you can avoid referring to them by their hierarchy path, which can sometimes be long, especially important when using command-line commands or assignments. Partition names can be from 1 to 1024 characters in length, and must be unique. The name can only consist of alphanumeric characters, the pipe (|), the colon (:), and the underscore (_) characters.

Methodology for Creating Good Partitions

There is an inherent tradeoff between compilation time and quality of results when you vary the number of partitions in a project. You can reduce this effect by ensuring that you follow a good methodology during the partitioning process. In any incremental compilation flow in which you can compile the source code for each partition during the partition planning phase, Altera recommends the following iterative flow:

1. Start with a complete design that is not partitioned and has no location or LogicLock assignments.

2. On the Processing menu, point to Start and click **Start Early Timing Estimate** to perform a placement and timing analysis estimate.

   You must perform Analysis & Synthesis before performing an Early Timing Estimate. If incremental compilation is already turned on, you must also perform Partition Merge.

   To run a full compilation instead of the Early Timing Estimate, on the Processing menu, click **Start Compilation**.

3. Record the quality of results from the Compilation Report (f_{MAX}, area, etc.).

4. Enable incremental compilation as described in "Preparing a Design for Incremental Compilation" on page 1–12.

5. Create design partitions as described in "Preparing a Design for Incremental Compilation" on page 1–12 using the guidelines in "Guidelines for Creating Good Design Partitions" on page 1–20.

6. Perform another Early Timing Estimate or full compilation.

7. Record the quality of results from the Compilation Report. If the quality of results is significantly worse than that obtained in the previous compilation in Step 3, repeat Step 5 through this step (Step 7) to change your partition assignments and use a different partitioning scheme.

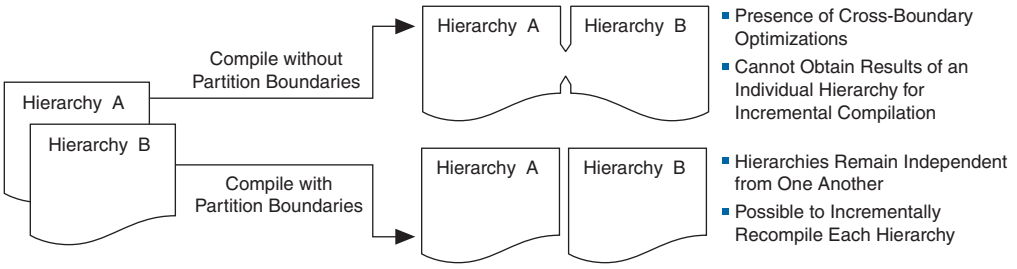
8. Even if the quality of results is acceptable, you can repeat Step 5 through Step 7 by further dividing a large partition into several smaller partitions. Doing so improves compilation time in future incremental compilations. You can repeat this step until you achieve a good tradeoff point (that is, all critical paths are localized within partitions and the quality of results is not negatively affected, and the size of each partition is reasonable).

Guidelines for Creating Good Design Partitions

When planning your design, keep in mind the size and scope of each partition, and the likelihood that different parts of your design might change as your design develops.

Creating partitions prevents the compiler from performing optimizations across partition boundaries (Figure 1–8), allowing the software to synthesize and place each partition separately.

Figure 1–8. Effects of Partition Boundaries During Optimization



Since cross-boundary optimizations cannot occur when using partitions, the quality of results and performance of the design may decrease as the number of partitions increases. Having more partitions allows for greater reduction in compilation time, however, you should limit the number of partitions to prevent degradation of the quality of results. This effect is more pronounced when using full incremental compilation than when using incremental synthesis only, and can have more effect in a bottom-up methodology than a top-down methodology.

Altera recommends that you also observe the following important hierarchical design considerations when creating partitions:

- Register all inputs and outputs of each partition. This helps avoid any delay penalty on signals that cross partition boundaries. At the very least, either the inputs or the outputs should be registered. The Statistics reports described in the "Partition Statistics Reports" section list the ports registered for each partition.

While this can be difficult in practice, greater adherence to this principle results in less timing degradation and area increase when using incremental flows. Registering lessens the need for the cross-partition optimizations that are prevented by partitioning.

- Minimize the number of paths that cross partition boundaries. If there are critical paths crossing between partitions, rework the partition(s) to avoid these inter-partition paths. The Statistics reports described in the "Partition Statistics Reports" section list the number of input and output ports for each partition.
- Ensure that the size of each partition is not too small, (for example, not less than 1,000 logic elements (LEs) or adaptive logic modules (ALMs)). The Statistics reports described in the "Partition Statistics Reports" section list the logic utilization of each partition.
- Minimize the number of unconnected ports at partition boundaries. This helps avoid errors in the Fitter during full incremental compilation where the netlist cannot be split. The Statistics reports described in the "Partition Statistics Reports" section list the number of unconnected input and output ports for each partition.
- Do not use tri-state signals or bidirectional ports on hierarchical boundaries, unless the port is connected directly to a top-level I/O pin on the device. If you use boundary tri-states in a lower-level block, synthesis pushes the tri-states through the hierarchy to the top-level to take advantage of the tri-state drivers on the output pins of the device.
  In an incremental compilation flow, internal tri-states are supported only when all the destination logic is contained in the same partition, in which case Analysis & Synthesis implements the internal tri-state signals using multiplexing logic. For a bidirectional port that feeds a bidirectional pin at the top-level, all the logic that forms the bidirectional I/O cell must reside in the same partition.
- Note that logic is not synthesized or optimized across partition boundaries, which means any constant value (for example, a signal set to `GND`) is not propagated across partitions.
- You may have to perform some manual resource balancing across partitions if device resources are overused in the individual partitions. Refer to "Resource Balancing" on page 1–23 for details.
- You may have to perform some timing budgeting if paths that cross partition boundaries require further optimization. Refer to "Timing Budgeting" on page 1–25 for details.

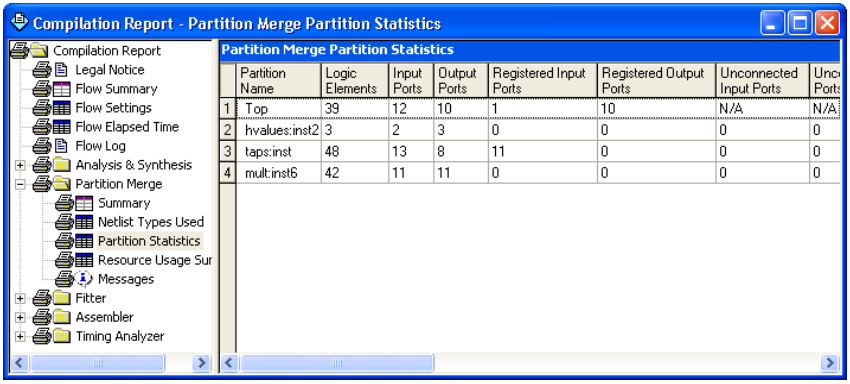
For more guidelines on design hierarchical partitioning, refer to *Hierarchical Design Partitioning* in the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Partition Statistics Reports

You can view statistics about design partitions in the Partition Merge Partition Statistics compilation report and the **Statistics** tab in the **Design Partitions Properties** dialog box.

The **Partition Statistics** page under the **Partition Merge** folder of the **Compilation Report** lists statistics about each partition. The statistics for each partition (each row in the table) include the number of logic cells it contains, as well as the number of input and output pins it contains and how many are registered or unconnected. This report is useful when optimizing your design partitions in a top-down compilation flow, or when you are compiling the top-level design in a bottom-up compilation flow, ensuring that the partitions meet the guidelines presented previously. Figure 1–9 shows the report window.

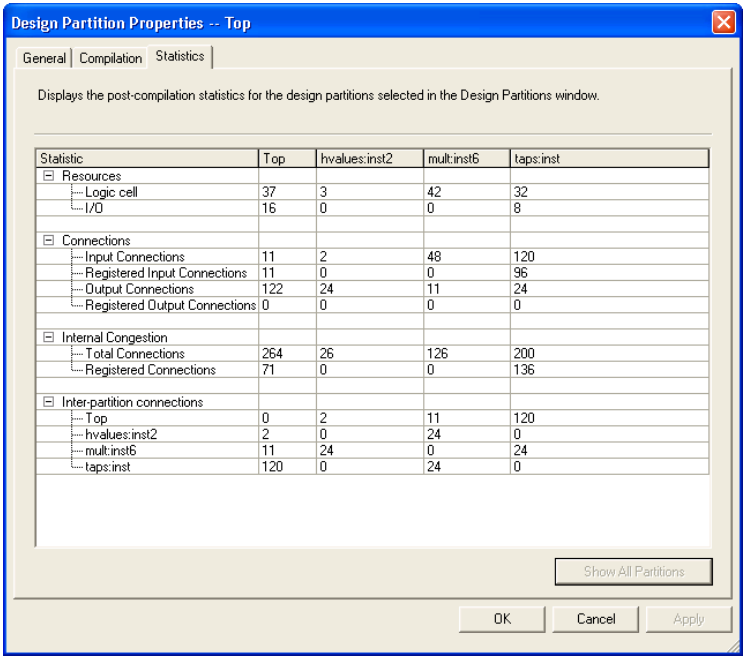
Figure 1–9. Partition Merge Partition Statistics Report



	Partition Name	Logic Elements	Input Ports	Output Ports	Registered Input Ports	Registered Output Ports	Unconnected Input Ports	Unc Ports
1	Top	39	12	10	1	10	N/A	N/A
2	hvalues:inst2	3	2	3	0	0	0	0
3	taps:inst	48	13	8	11	0	0	0
4	mult:inst6	42	11	11	0	0	0	0

You can also view statistics about the resource and port connections for a particular partition on the **Statistics** tab of the **Design Partition Properties** dialog box. On the **Assignments** menu, click **Design Partitions Window**. Right-click on a partition and click **Properties** to open the dialog box (Figure 1–10).

Figure 1–10. Statistics Tab in the Design Partitions Properties Dialog Box



Statistic	Top	hvalues:inst2	mult:inst6	taps:inst
Resources				
Logic cell	37	3	42	32
I/O	16	0	0	8
Connections				
Input Connections	11	2	48	120
Registered Input Connections	11	0	0	96
Output Connections	122	24	11	24
Registered Output Connections	0	0	0	0
Internal Congestion				
Total Connections	264	26	126	200
Registered Connections	71	0	0	136
Inter-partition connections				
Top	0	2	11	120
hvalues:inst2	2	0	24	0
mult:inst6	11	24	0	24
taps:inst	120	0	24	0

Resource Balancing

When using incremental compilation, the software synthesizes each partition separately, with no data about the resources used in other partitions. This means that device resources could be overused in the individual partitions during synthesis, and thus the design may not fit in the target device when the partitions are merged.

In a bottom-up design flow in which designers optimize their lower-level designs and export them to a top-level design, the software also places and routes each partition completely separately. In some cases, partitions can use conflicting resources when combined at the top level.

To avoid these effects, you may have to perform manual resource balancing across partitions.

RAM & DSP Blocks

In the regular synthesis flow, when DSP blocks or RAM blocks are overused, the Quartus II Compiler can perform resource balancing and convert some of the logic into regular logic cells (for example, LEs or ALMs). Without data about resources used in other partitions, it is possible for the logic in each separate partition to maximize the use of a particular device resource, such that the design does not fit once all the partitions are merged. In this case, you may be able to manually balance the resources by using the Quartus II synthesis options to control inference of megafunctions that use the DSP or RAM blocks. You can also use the MegaWizard® Plug-In Manager to customize your RAM or DSP megafunctions to use regular logic instead of the dedicated hardware blocks.

For more information on resource balancing when using Quartus II synthesis, refer to the *Megafunction Inference Control* section in the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*. For more tips on resource balancing and reducing resource utilization, refer to the appropriate *Resource Utilization Optimization Techniques* section in the *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Altera recommends using a LogicLock region for each partition to minimize the chance that the logic in more than one partition uses the same logic resource. However, there are situations in which partition placement may still cause conflicts at the top level. For example, you can design a partition one way in a lower level design (such as using an M-RAM memory block) and then instantiate it in two different ways in the top level (such as one using an M-RAM block and another using an M4K block). In this case, you can use a post-fit netlist only with no placement information to allow the software to refit the logic.

Global Routing Signals

Global routing signals can cause conflicts when multiple projects are imported into a top-level design. The Quartus II software automatically promotes high fan-out signals to use global routing resources available in the device. It is possible for lower-level partitions to use the same global routing resources, causing conflicts at the top level.

In addition, LAB placement depends on whether the inputs to the LCELLs within the LAB are using a global clock signal. Therefore, problems can occur if a design does not use a global signal in the lower-level design, but does use a global signal in the top-level design.

To avoid these problems, the project lead should determine which partitions will use particular global routing signals, then each designer of a lower-level partition can assign the appropriate global signals manually, and prevent other signals from using global routing resources. Use the **Global Signal** assignment set to a value of **On** or **Off** in the Assignment Editor to place a signal on a global routing line, or to prevent the signal from using a global routing line. If you want to disable the automatic global promotion performed in the Fitter, turn off the **Auto Global Clock** and **Auto Global Register Control Signals**. On the Assignments menu, click **Settings**. On the **Fitter Settings** page, click **More Settings** and change the settings to **Off**.

Alternately, to avoid problems when importing, direct the Fitter to discard the placement and routing of the imported netlist by setting the Fitter preservation level property of the partition to Netlist Only. With this option, the Fitter re-assigns all the global signals for this particular partition when compiling the top-level design.

If you are performing a bottom-up flow using the design partition scripts, then the software can automatically write the commands to pass global constraints and turn off the automatic options. Refer to "Generating Bottom-Up Design Partition Scripts for Project Management" on page 1–42 for details.

Timing Budgeting

If you optimize lower-level partitions and import them to the top level, any unregistered paths that cross between partitions are not optimized as an entire path. One way to reduce this effect is to ensure input and output ports of the partitions are registered whenever possible.

To ensure that the Compiler correctly optimizes the input and output logic in each partition, you may be required to perform some manual timing budgeting. For each unregistered timing path that crosses between partitions, make timing assignments on the corresponding I/O path in each partition to constrain both ends of the path to the budgeted timing delay. Timing budgets may be required for these I/O ports because when the Compiler optimizes each partition, it has no information about the placement of the logic that connects to that port. If the logic in one partition is placed far away from logic in another partition, the routing delay between the logic could lead to problems meeting the timing requirements. Assigning a timing budget for each part of the connection ensures that the Compiler optimizes the paths appropriately.

When performing manual timing budgeting, you can also use **Virtual Pin** assignments. By assigning location and timing constraints to the **Virtual Pins**, you can further improve the quality of the timing budget.

If you are performing a bottom-up flow using the design partition scripts, then the software can write virtual pin assignments and I/O timing budget constraints automatically. Refer to "Generating Bottom-Up Design Partition Scripts for Project Management" on page 1–42 for details.

Setting the Netlist Type for Design Partitions

The **Netlist Type** is a property of each design partition that allows you to specify the type of netlist or source file that the compiler should use as the input for each partition, as described in Table 1–2. This property determines which netlist is used by the Partition Merge stage in the next compilation. To view and modify the **Netlist Type**, on the Assignments menu, click **Design Partition Window**. Double-click the **Netlist Type** for an entry. Alternatively, right-click on an entry, click **Design Partition Properties**, then modify the **Netlist Type** on the **Compilation** tab.

Table 1–2. Netlist Type Settings (Part 1 of 2)

Partition Netlist Type	Quartus II Behavior for Partition During Compilation
Source File	Always compiles the partition using the associated design source file(s). You can use this netlist type to recompile a partition from the source code using new synthesis or fitter settings. If the partition has an associated imported netlist, compiling it with netlist type set to Source File removes the imported netlist.
Post-Synthesis	Preserves post-synthesis results for the partition and uses the post-synthesis netlist as long as the following conditions are true: • A post-synthesis netlist is available from a previous synthesis • No change has been made to the associated source files since the previous synthesis Compiles the partition from the source files if there are source changes or if a post-synthesis netlist is not available. Changes to the assignments do not cause recompilation. You can use this netlist type to preserve the synthesis results unless source files change, but refit the partition using any new fitter settings. If a partition has an associated imported netlist, this setting is not available.
Post-Fit	Preserves post-fit results for the partition and uses the post-fit netlist as long as the following conditions are true: • A post-fit netlist is available from a previous fitting • No change has been made to the associated source files since the previous fitting Compiles the partition from the source files if there are source changes or if a post-fit netlist is not available. Changes to assignments do not cause recompilation. The **Fitter Preservation Level** specifies what type of information is preserved from the post-fit netlist. You can use this netlist type to preserve the fitter results unless source files change. You can also use this netlist type to apply global optimizations, such as Physical Synthesis optimizations, to certain partitions while preserving the fitting results for other partitions. If a partition has an associated imported netlist, this setting is not available.
Post-Fit (Strict)	Always preserves post-fit results for the partition. Uses the post-fit netlist even if changes have been made to the associated source files since the previous fitting. The **Fitter Preservation Level** specifies what type of information is preserved from the post-fit netlist. If a partition has an associated imported netlist, this setting is not available.

Table 1–2. Netlist Type Settings (Part 2 of 2)

Partition Netlist Type	Quartus II Behavior for Partition During Compilation
Imported	Compiles the design partition using a netlist imported from a Quartus II Exported Partition File **(.qxp)**. The **Fitter Preservation Level** specifies what type of information is preserved from the imported netlist. The software does not modify or overwrite the original imported netlist during compilation. To preserve changes made to the imported netlist (such as movement of an imported LogicLock region), use the "Post-Fit (Import-based)" setting following a successful compilation with the imported netlist. For additional details, refer to "Exporting & Importing Partitions for Bottom-Up Design Flows" on page 1–35. If a partition does not have an associated imported netlist, this setting is not available.
Post-Fit (Import-based)	Preserves post-fit results for the partition and uses the post-fit netlist as long as the following conditions are true: ● A post-fit netlist is available from a previous fitting ● No change has been made to the associated imported netlist since the previous fitting Compiles the partition from the imported netlist if the imported netlist changes (which means it has been reimported) or if a post-fit netlist is not available. Changes to assignments do not cause recompilation. The **Fitter Preservation Level** specifies what type of information is preserved from the post-fit netlist. You can use this netlist type to preserve changes to the placement and routing of the imported netlist. If a partition does not have an associated imported netlist, this setting is not available.
Empty	Uses an empty placeholder netlist for the partition and uses virtual pins at the partition boundaries. You can use this netlist type to skip the compilation of a lower-level partition. For more details on the Empty setting, refer to "Empty Partitions" on page 1–28.

Fitter Preservation Level

The Fitter Preservation Level property specifies which information the compiler will use from a post-fit or imported netlist. The property is only available if the **Netlist Type** is set to **Post-Fit**, **Post-Fit (Strict)**, **Imported**, or **Post-Fit (Import-based)**.

On the Assignments menu, click **Design Partitions Window**. You can view and modify the **Fitter Preservation Level** by double-clicking an entry. You can also right-click and click **Properties**, then edit the **Fitter Preservation Level** on the **Compilation** tab.

Table 1–3 describes the Fitter preservation level settings.

Table 1–3. Fitter Preservation Level Settings

Fitter Preservation Level	Quartus II Behavior for Partition During Compilation
Placement	Preserves the netlist atoms and their placement in the design partition. Re-routes the design partition. This setting saves significant compilation time because the Fitter does not need to re-fit the nodes in the partition. Note that the Fitter may need to modify the placement for timing or legality reasons. This setting might not be available if netlist type is set to **Imported** and the imported netlist does not contain placement data.
Placement and Routing	Preserves the netlist atoms and their placement and routing in the design partition. This setting minimizes compilation time. Note that the Fitter may need to modify the placement and routing for timing or legality reasons. This setting may not be available if netlist type is set to **Imported** and the imported netlist does not contain routing data.
Netlist Only	Preserves the netlist atoms of the design partition, but replaces and re-routes the design partition. Unlike a Post-Synthesis netlist, a Post-Fit netlist with the atoms preserved contains any fitter optimizations, for example, registers duplicated by Physical Synthesis during a previous Fitting. You can use this setting to preserve Fitter optimizations but allow the software to perform placement and routing again. You can also use this setting to re-apply certain fitter optimizations (that is, physical synthesis) that would otherwise be impossible when the placement is locked down.

Empty Partitions

To set the **Netlist Type** to **Empty**, on the Assignments menu, click **Design Partitions Window**, or double-click an entry, or right-click an entry and click **Design Partition Properties** and select **Empty**. This setting specifies that the Quartus II Compiler should use an empty placeholder netlist for the partition.

You can use the **Empty** setting to skip the compilation of a lower-level partition that is incomplete or missing from the top-level design. You can also use it if you want to compile only some partitions in the design, such as during optimization or if the compilation time is large for one partition and you want to exclude it.

When a partition **Netlist Type** is defined as **Empty**, virtual pins are created at the boundary of the partition. This means that the software temporarily maps I/O pins in the lower-level design entity to internal cells and not to pins during compilation.

Any sub-partitions below an empty partition are also considered empty, regardless of their settings.

You can use a design flow in which some partitions are set to **Empty** in a variation of a bottom-up design flow, where you develop pieces of the design separately and then combine them at the top-level at a later time. When you implement part of the design without information about the rest of the project, it is impossible for the Compiler to perform global placement optimizations. One way to reduce this effect is to ensure input and output ports of the partitions are registered whenever possible, as recommended in "Guidelines for Creating Good Design Partitions" on page 1–20.

When you set a design partition to **Empty**, a design file is required in Analysis & Synthesis to specify, at minimum, the port interface information so that it can connect the partition correctly to other logic and partitions in the design. If the design file is missing, you must create a wrapper file (called a black box or hollow-body file) that defines the design block and specifies the input, output, and/or bidirectional ports.

Creating a Design Floorplan With LogicLock Location Assignments

Once you have partitioned the design, create floorplan location assignments for the design as discussed in this section when using the full incremental compilation flow to improve quality of results.

The simplest way to create a floorplan for a partitioned design is to create one LogicLock region per partition (including the top-level partition). Initially, leave each region with the default settings of Auto size and Floating location to allow the Quartus II software to determine the optimal size and location for the regions. Then, after compilation, back-annotate the Fitter-determined size and location properties. Check the quality of results obtained for your floorplan location assignments and make changes to the regions as needed.

For more information on why creating a design floorplan is important, refer to "The Importance of Floorplan Location Assignments in Incremental Compilation" on page 1–32.

To create a LogicLock region for each design partition, use the following general methodology:

1. On the Assignments menu, click **Design Partitions Window** and ensure that all partitions have their **Netlist Type** set to **Source** or **Post-Synthesis**. If the **Netlist Type** is set to **Post-Fit**, floorplan location assignments are not used when recompiling the design.

2. Create a LogicLock region for a partition using one of the following methods:
   - On the Assignments menu, click **LogicLock Regions Window**. Drag an individual partition from the **Design Partitions Window** and drop it in the **<<new>>** row of the **LogicLock Regions Window**.
   - Under **Compilation Hierarchy** in the **Project Navigator**, right-click an instance that is denoted as a partition and click **Create New LogicLock Region**.
3. Repeat Step 2 for each partition, including the top-level entity, which is automatically considered a partition.
4. On the Processing menu, point to Start and click **Start Early Timing Estimate** to place auto-sized, floating-location LogicLock regions.

   You must perform Analysis & Synthesis and Partition Merge before performing an Early Timing Estimate.

   To run a full compilation instead of the Early Timing Estimate, on the Processing menu, click **Start Compilation**.
5. On the Assignments menu, click **LogicLock Regions Window**, and click on each LogicLock region while holding the Ctrl key to select all regions (including the top-level region).
6. Right-click on the last selected LogicLock region, and click **Properties**.
7. On the **Location** tab, click **Back-annotate Origin and Lock** to back-annotate the Fitter-determined size and location properties, then click **OK**.

   It is important that you use the Fitter-chosen locations only as a starting point to make the regions of a fixed size and location. Regions with fixed size and location yield better f_{MAX} than auto-sized regions on average.

   Do not back-annotate the contents of the region, just save the location and size using the **Back-annotate Origin and Lock** command. Placement is preserved through the use of the post-fit netlist instead of back-annotated content assignments.
8. If required, modify the size and location via the **LogicLock Regions Window** or the **Timing Closure Floorplan**.

9. On the Processing menu, point to Start and click **Start Early Timing Estimate** to estimate the timing performance of your design with these LogicLock regions.

10. Repeat steps 8 and 9 until you are satisfied with the quality of results for your design floorplan. On the Processing menu, click **Start Compilation** to run a full compilation.

Recommendations for Creating Good Floorplan Location Assignments

If your design contains hierarchical partitions (that is, parent-child relationships between partitions), you can create hierarchical LogicLock regions to ensure that the logic in the child partition is physically placed inside the LogicLock region for the parent partition. This can be useful when the parent partition does not contain registers at the boundary with the lower-level child partition. To create a hierarchical relationship between regions in the **LogicLock Regions Window**, drag and drop the child region to the parent region.

If resource utilization is low, you may enlarge the Fitter-chosen region. Doing so usually improves the final results because it gives the Fitter more freedom to place additional logic added to the partition during future incremental compilations.

If the quality of results has worsened after creating floorplan location assignments, try to improve the floorplan by enlarging the area of each region using the following guidelines:

- Ideally, the entire device should be covered by LogicLock regions. You may move the region origins to satisfy this requirement, but Altera recommends preserving the Fitter-determined relative placement of the regions.
- Regions should not overlap in the device floorplan.
- Give more area to regions that are densely populated.

For more information on making and editing LogicLock regions, consult the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

Excluding or Filtering Certain Device Elements (Such as RAM or DSP Blocks)

If your design contains memory or digital signal processing (DSP) elements, you may want to exclude these elements from the LogicLock region. You can use a LogicLock resource filter to prevent elements of certain types from being assigned to a region. Note that the filter does not

prevent them from being placed inside the region boundaries unless the region's "Reserved" property is set to on. Defining a resource filter instructs the Fitter that certain blocks are not required to be inside a region. Resource filters are useful in cases where it is difficult to place rectangular regions for design blocks that contain memory and DSP elements, because of their placement in columns throughout the device floorplan. Filtering these elements can help to resolve no-fit errors that are caused by regions spanning too many resources, especially for designs that are memory and/or DSP-intensive. If desired, you can also create separate regions for the memory or DSP blocks, which can be shaped to accommodate the columns in the device to control the placement of those design elements.

To view any resource filters, right-click in the LogicLock Regions window and click **Properties**. In the **LogicLock Region Properties** dialog box, View the **Excluded Resources** column in the **Members** box. To set up a resource filter, highlight the appropriate region member and click **Edit Excluded Resources**, then turn on the design element types to be excluded from the region. You can choose to exclude combinational logic or registers from logic cells, or any of the sizes of TriMatrix™ memory blocks, or DSP blocks.

For more information on excluding nodes from LogicLock regions, consult the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

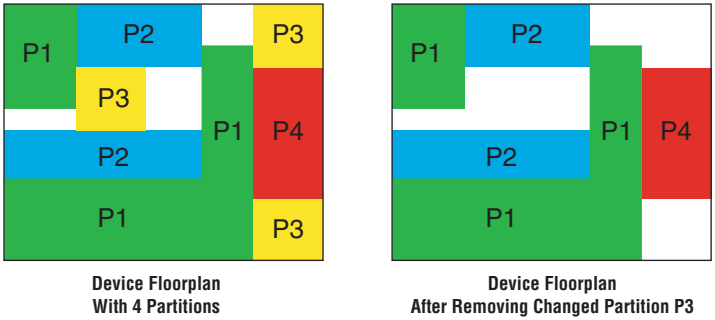
The Importance of Floorplan Location Assignments in Incremental Compilation

Floorplan location planning is very important for a design that uses full incremental compilation, because it helps to avoid the situation that arises when the Fitter is directed to place or replace a portion of the design in an area of the device where most resources have already been claimed. In this case, the placement of the post-fit netlists of other modules forces the Fitter to place the new portion of the design in the empty parts of the device. There are two immediate disadvantages to this situation. First, the Fitter must work harder because of the higher number of physical constraints, and therefore compilation time probably increases. Second, the quality of results often decreases, sometimes dramatically, because the placement of the target module is now scattered throughout the device.

Figures 1–11 and 1–12 illustrate the problems associated with refitting designs that do not have floorplan location assignments. Figure 1–11 shows the initial placement of a four-partition design (**P1**–**P4**) without floorplan location assignments. The second part of the figure shows the

situation if a change occurs to **P3**. After removing the logic for the changed partition, the Fitter must replace and reroute the new logic for **P3** using the white space shown in the figure.

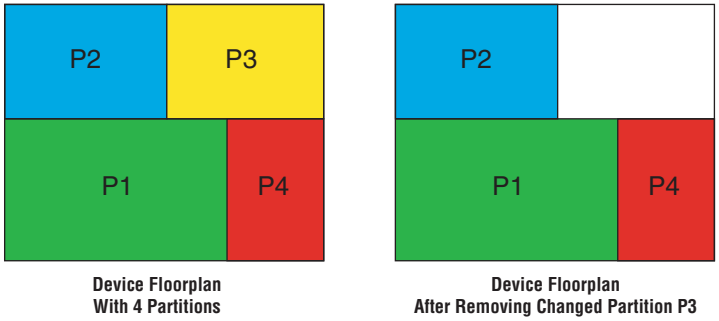
Figure 1–11. Representation of Device Floorplan without Location Assignments



Performing this placement is very difficult. The Fitter may not be able to find any legal placement for the logic in partition **P3**, even if it was able to do so in the initial compilation. If the Fitter does find a legal placement, the results are probably sub-optimal.

Figure 1–12 shows the initial placement of a four-partition design with floorplan location assignments made by the user, and the situation after partition **P3** is removed in this case.

Figure 1–12. Representation of Device Floorplan with Location Assignments



This placement presents a much more reasonable task to the Fitter and yields better results than the previous case that does not have floorplan location assignments.

Taking Advantage of the Early Timing Estimator

The general methodology steps described above take advantage of the Early Timing Estimator to enable quick compilations of the design while creating assignments. The Early Timing Estimator feature provides a timing estimate for a design as much as 45 times faster than running a full compilation, yet estimates are, on average, within 11 percent of final design timing. You can use the Timing Closure Floorplan editor to view the "placement estimate" created by this feature, identify critical paths, and if necessary, add or modify floorplan constraints. You can then rerun the Early Timing Estimator to quickly assess the impact of any floorplan location assignments or logic changes, enabling rapid iterations on design variants to help you find the best solution.

For information on timing analysis and early timing estimation, refer to the *Classic Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Criteria for Successful Partition & Floorplan Schemes

The end results of design partitioning and floorplan creation differ from design to design. However, it is important to evaluate your results to ensure that your scheme is successful. Compare the results before creating your floorplan location assignments to the results after doing so, and consider using another scheme if any of the following guidelines are not met:

- No degradation in f_{MAX} should be observed after the design is partitioned and floorplan location assignments are created. In many cases, a slight increase in f_{MAX} is possible.
- The area increase should be no more than 5 percent after the design is partitioned and floorplan location assignments are created.
- The time spent in the routing stage should not significantly increase.

The amount of compilation time spent in the routing stage is reported in the Messages window with an Info message indicating the elapsed time for Fitter routing operations. If you notice a dramatic increase in routing time, the floorplan location assignments may be creating substantial routing congestion. In this case, decrease the number of LogicLock regions. Doing so typically reduces the compilation time in subsequent incremental compilations, and may also improve design performance.

To help you modify your LogicLock regions, you can identify areas of congested routing in your design using the Timing Closure Floorplan. On the Assignments menu, click **Timing Closure Floorplan** and turn on **Show Routing Congestion**. This feature is available only when you click **Field View** on the View menu.

For details on using the Timing Closure Floorplan, refer to the *Timing Closure Floorplan* chapter in volume 2 of the *Quartus II Handbook*.

Exporting & Importing Partitions for Bottom-Up Design Flows

The bottom-up flow refers to the design methodology in which a project is first divided into smaller sub-designs that are implemented as separate projects, potentially by different designers. The compilation results of these lower-level projects are then exported and given to the designer (or the project lead) who is responsible for importing them into the top-level project to obtain a fully functional design.

There are at least two benefits associated with a bottom-up design flow:

- It facilitates team-based development.
- It permits the reuse of compilation results from another project, with the ultimate goals of performance preservation and compilation time reduction.

A bottom-up design flow also has some potential drawbacks that require careful planning:

- It may be difficult to achieve timing closure for the full design, because you compile the lower-level sub-modules independently without any information about each other. This problem may be avoided by careful timing budgeting and special design rules such as always registering the ports at the module boundaries.
- For the same reason, resource budgeting and allocation may be needed to avoid resource conflicts and overuse. Floorplan creation is typically very important in a bottom-up flow.

In a bottom-up design flow, the top-level project lead can do much of the design planning, and then pass constraints on to the designers of lower-level blocks. The bottom-up design partition scripts generated by the Quartus II software can make it easier to plan a bottom-up design, and limit the difficulties that can arise when integrating separate designs.

Preparing the Top-Level Design for a Bottom-Up Incremental Compilation Methodology

To set up your design for bottom-up incremental compilation, use the following general steps:

1. Create a top-level project that will be compiled by the project lead and will eventually incorporate the entire design. The top-level design file must include the top-level entity that instantiates all the lower-level subdesign that you plan to compile in separate Quartus II projects and import as separate design partitions.

2. In your top-level project, include a wrapper design file for each subdesign partition that defines at least the port interface of the subdesign. Analysis & Elaboration requires this wrapper file (also known as a "stub" or "black box" file) to connect all the separate design partitions at the top level. The wrapper file does not have to contain any logic definition, just the module or entity and architecture, and the port list for the design block.

3. Create all global assignments, including the device assignment, pin location assignments, and timing assignments, so that the final design meets its requirements. Lower-level project designers can add their own constraints for their partitions as needed, and later export them to top-level, but the basic constraints can be passed down from the top-level to avoid any conflicts and ensure that lower-level projects use the correct assignments.

4. Set up the top-level design with design partitions, turn on incremental compilation, and create a design floorplan using LogicLock assignments. Follow the steps in "Preparing a Design for Incremental Compilation" on page 1–12.

5. Ensure that you allocate device resources appropriately, as described in "Resource Balancing" on page 1–23.

6. Optionally, you can use the Quartus II software to generate bottom-up design partition scripts that help with design planning and project management at the top level of the project. Refer to "Generating Bottom-Up Design Partition Scripts for Project Management" on page 1–42 for details.

Exporting a Partition to be Used in a Top-Level Project

Each lower-level subdesign is compiled as a separate Quartus II project. In each project, use the following guidelines to improve the exporting and importing process:

- Ensure that the LogicLock region uses only the resources allocated by the top-level project lead.
- Ensure that you know which clocks should be allocated to global routing resources so that there are no resource conflicts in the top-level design.
  - Set the **Global Signal** assignment to On for the high fan-out signals that should be routed on global routing lines.
  - To avoid other signals being placed on global routing lines, on the Assignments menu, click **Settings** and turn off **Auto Global Clock and Auto Global Register Controls** under **More Settings** on the Fitter page of the **Settings** dialog box.

  - Alternately, you can set the **Global Signal** assignment to Off for signals that should not be placed on global routing lines. Placement for LABs depends on whether the inputs to the logic cells within the LAB use a global clock, so you may encounter problems if signals do not use global lines in the lower level design but use global routing in the top level.
- Use the **Virtual Pin** assignment to indicate pins of a subdesign that do not drive pins in the top-level design. This is critical when a subdesign has more output ports than the number of pins available in the target device. Using virtual pins also helps optimize cross-partition paths for a complete design by enabling you to provide more information about the subdesign ports, such as location and timing assignments.
- Because subdesigns are compiled independently without any information about each other, you should provide more information about the timing paths that may be affected by other partitions in the top-level design. You can apply location assignments for each pin to indicate where the port connection will be located after it is incorporated in the top-level design. You can also apply timing assignments to the I/O ports of the subdesign to perform timing budgeting as described in "Timing Budgeting" on page 1–25.

When your subdesign partition has been compiled using these guidelines, and is ready to be incorporated into the top-level design, export a subdesign as a partition using the following steps:

1. In the subdesign project, on the Project menu, click **Export Project as Design Partition**. The **Export Project as Design Partition** dialog box opens (Figure 1–13).

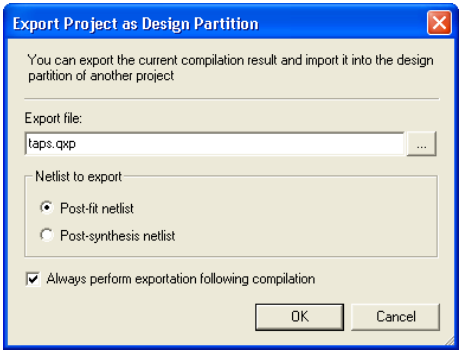
2. In the **Export file** box, type the name of the Quartus II Exported Partition file (**.qxp**). By default, the directory path and file name are the same as the current project.

3. Under **Netlist to export**, select either **Post-fit netlist** or **Post-synthesis netlist**. The default is **Post-Fit netlist**.

4. To automatically create a new version of the Quartus II Exported Partition file after each subsequent compilation, turn on **Always perform exportation following compilation**.

5. Click **OK**. The Quartus II software creates the Quartus II Exported Partition file in the specified directory.

Figure 1–13. Export Project as Design Partition Dialog Box



Importing a Lower-Level Partition Into the Top-Level Project

The import process involves importing the design netlist from the Quartus II Exported Partition file and adding the netlist to the database for the top-level project. Importing also filters the assignments from the subdesign and creates the appropriate assignments in the top-level project.

To import a subdesign partition into a top-level design:

1. In the top-level project, on the Project menu, click **Import Design Partition**. Alternately, right-click on the partition that you want to import in the Design Partitions window and click **Import Design Partition**, this opens the **Import Design Partition** dialog box.

2. In the **Partition(s)** box, click **browse** to select the desired partition. To browse for a partition, highlight the partition name in the **Select Partition(s)** dialog box and use the appropriate buttons to select or deselect the desired partition(s).

   Note that you can select multiple partitions if your top-level design has multiple instances of the subdesign partition and you want to use the same imported netlist.

3. Under **Import file**, type the name of the Quartus II Exported Partition file or browse for the file that you want to import into the selected partition. Note that this file is required only during importation, but is not used during subsequent compilations.

If you have already imported the Quartus II Exported Partition file for this partition at least once, you can use the same location as the previous import instead of specifying the file name again. To do so, turn on **Reimport using the latest import files at previous locations**. This option is especially useful when you want to import the new Quartus II Exported Partition files for several partitions that you have already imported at least once. You can select all the partitions to be imported in the Partition(s) box and then use the **Reimport using latest import files at previous locations** option to import all partitions using their previous locations, without specifying individual file names.

4. To view the contents of the selected Quartus II Exported Partition file, click **Load Properties**. The properties displayed include the Netlist Type, Entity name, Device and statistics about the partition size and ports.

5. Click **Advanced Import Settings** and make selections, as appropriate, to control how assignments and regions are integrated from a subdesign into a top-level design partition. During importation, some regions may be resized or slightly moved. Click **OK** to apply the settings.

   For more information about the advanced settings, refer to "Importing Assignments & Advanced Import Settings" on page 1–39.

6. In the **Import Design Partition** dialog box, click **OK** to start importation. The specified Quartus II Exported Partition file is imported into the database for the current top-level project.

Importing Assignments & Advanced Import Settings

When you import a subdesign partition into a top-level design, the software sets certain assignments by default and also imports relevant assignments from the subdesign into the top-level design.

Design Partition Properties After Importing

When you import a subdesign partition, the import process sets the partition's Netlist Type to **Imported**.

If you compile the design and want to make and preserve changes to the place-and-route results, use the **Post-Fit (Import-based)** Netlist Type on the subsequent compilation. To discard an imported netlist and recompile

from source code, simply compile the partition with netlist type set to **Source File** and be sure to include the relevant source code with the top-level project.

The import process sets the partition's Fitter Preservation Level to the setting with the highest degree of preservation supported by the imported netlist. For example, if a post-fit netlist is imported with placement information, the level is set to **Placement**, but you can change it to the **Netlist Only** value.

Refer to "Setting the Netlist Type for Design Partitions" on page 1–26 for details about the Netlist Type and Fitter Preservation Level setting.

Importing Design Partition Assignments Within the Subdesign

Design partitions defined within the subdesign project are currently not imported to the top-level.

Importing LogicLock Assignments

LogicLock regions are set to a fixed size when imported. If you instantiate multiple instances of a subdesign in the top-level design, the imported LogicLock regions will be set to a Floating location. Otherwise, they are set to a Fixed location. You can change the location of LogicLock regions after they are imported, or change them to a Floating location to allow the software to place each region but keep the relative locations of nodes within the region wherever possible. If you want to preserve changes made to a partition after compilation, use the Netlist Type **Post-Fit (Import-Based)**.

The LogicLock Member State assignment is set to Locked to signify that it is a preserved region.

LogicLock back-annotation and node location data is not imported because the Quartus II Exported Partition file contains all the relevant placement information. Altera strongly recommends that you do not add to or delete members from an imported LogicLock region.

Importing Other Instance Assignments

All instance assignments are imported, with the exception of design partition assignment, and LogicLock assignments, as described previously.

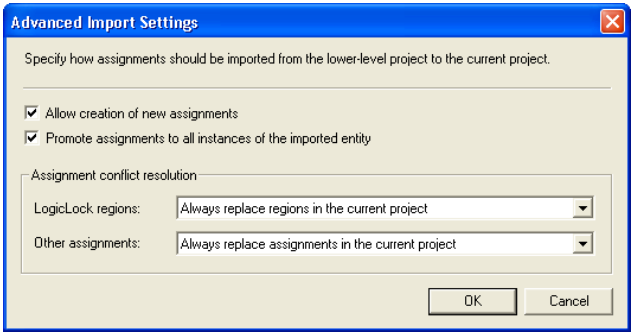
Importing Global Assignments

Global assignments are not imported. The project lead should make global assignments, such as clock settings in the top-level design.

Advanced Import Settings

The **Advanced Import Settings** dialog box, shown in Figure 1–15, allows you to specify the options in this section that control how assignments and regions are integrated and how to resolve assignment conflicts when importing a subdesign partition into a top-level design. The following sub-sections describe each of these options.

Figure 1–14. Advanced Import Settings Dialog Box



Allow Creation of New Assignments
Allows the import command to add new assignments from the imported project to the top-level project.

When this option is turned off, it imports updates to existing assignments, but no new assignments are allowed.

Promote Assignments to all Instances of the Imported Entity
Converts and promotes entity-level assignments from the subdesign into instance-level assignments in the top-level design.

Assignment Conflict Resolution: LogicLock Regions
Choose one of the following options to determine how to handle conflicting LogicLock assignments (that is, subdesign assignments that do not match the top-level assignments):

- **Always replace regions in the current project** (default)—Deletes existing regions and replaces them with the new subdesign region. Note that any changes made to the LogicLock region after the assignments were imported are also deleted.
- **Always update regions in the current projects**—Overwrites existing region assignments to reflect any new subdesign assignments, with the exception of the LogicLock Origin in case the project lead has made floorplan location assignments in the top-level design.
- **Skip conflicting regions**—Ignores and does not import subdesign assignments that conflict with any assignments that exist in the top-level design.

Assignment Conflict Resolution: Other Assignments
Choose one of the following options to determine how to handle conflicts with other types of assignments (that is, the subdesign assignments do not match the top-level assignments):

- **Always replace assignments in the current project** (default)—Overwrites or updates existing instance assignments with the new subdesign assignments.
- **Skip conflicting assignments**—Ignores and does not import subdesign assignments that conflict with any assignments that exist in the top-level design.

Generating Bottom-Up Design Partition Scripts for Project Management

The bottom-up design partition scripts automate the process of transferring top-level project information to lower-level modules. The software provides a project manager interface for managing resource and timing budgets in the top-level design. This makes it easier for designers of lower-level modules to implement the instructions from the project lead, and avoid conflicts between projects when importing and incorporating the projects into the top-level design. This helps reduce the need to further optimize the designs after integration, and improves overall designer productivity and team collaboration.

Generating bottom-up design partition scripts is optional in any bottom-up design methodology.

In a typical bottom-up design flow, the project lead must perform some or all of the following tasks to ensure successful integration of the sub-projects:

- Manually determine which assignments should be propagated from the top-level to the bottom-levels. This requires detailed knowledge of which Quartus II assignments are needed to set up low-level projects.
- Manually communicate the top-level assignments to the low-level projects. This requires detailed knowledge of Tcl or other scripting languages to efficiently communicate project constraints.
- Manually determine appropriate timing and location assignments that will help overcome the limitations of bottom-up design. This requires examination of the logic in the lower levels to determine appropriate timing constraints.
- Perform final timing closure and resource conflict avoidance at the top level. Because the low-level projects have no information about each other, meeting constraints at the lower levels does not guarantee they will be met when integrated at the top-level. It then becomes the project lead's responsibility to resolve the issues, even though information about the low-level implementation may not be available.

Using the Quartus II feature that generates bottom-up design partition scripts from the top level of the design makes these tasks much easier and eliminates the chance of error when communicating between the project lead and lower-level designers. Partition scripts pass on assignments made in the top-level design, and create some new assignments that guide the placement and help the lower-level designers see how their design connects to other partitions.

Generate design partition scripts after a successful compilation of the top-level design. On the Project menu, click **Generate Bottom-Up Design Partition Scripts**. The design can have empty partitions as placeholders for lower-level blocks, and you can perform an Early Timing Estimation instead of a full compilation to reduce compilation times.

The following subsections describe the information that you can choose to be included in the bottom-up design partition Tcl scripts. Use the options in the **Generate Bottom-Up Design Partition Scripts** dialog box to choose which types of assignments you want to pass down and create in the lower-level partition projects.

For information about current limitations in the bottom-up partition scripts, refer to the "Bottom-Up Design Partition Script Limitations" on page 1–61.

Project Creation

You can use the **Create lower-level project if one does not exist** option for the partition scripts to create lower level projects if they are required. The Quartus II Project File for each lower-level project has the same name as the entity name of its corresponding design partition.

With this project creation feature, the scripts work by themselves to create a new project, or can be sourced to make assignments in an existing project.

Assignments from the Top-Level Design

By default, any assignments made at the top-level (not including default assignments or project information assignments) are passed down to the appropriate low-level projects in the scripts. The software uses the assignment variables and determines the logical partition(s) to which the assignment pertains (this includes global assignments, instance assignments, and entity-level assignments). The software then changes the assignments so that they are syntactically valid in a project with its target partition's logic as the top-level entity.

The scripts process wildcard assignments correctly, provided there is only one wildcard. Assignments with more than one wildcard are ignored and warning messages are issued.

Use the options described in the following section to specify which of the following types of assignments you would like passed down to the lower-level projects:

- **Timing assignments**—When this option is turned on, all global timing assignments for the lower-level projects are included in the script, including t_{CO}, t_{SU}, and f_{MAX} constraints. It may also optionally include timing constraints on internal partition connections.
- **Design partition assignments**—When this option is turned on, script assignments related to design partitions in the lower-level projects are included, as well as assignments associated with LogicLock regions.
- **Pin location assignments**—When this option is turned on, all pin location assignments for lower-level project ports that connect to pins in the top-level design are included in the script, controlling the overuse of I/Os at the top-level during the integration phase and preserving placement.

Virtual Pin Assignments

When **Create virtual pins at low-level ports connected to other design units** is turned on, the Quartus II software searches partition netlists and identifies all ports that have cross-partition dependencies. For each lower-level project pin associated with an internal port in another partition or in the top-level project, the script generates a virtual pin assignment, ensuring more accurate placement, because virtual pins are not directly connected to I/O ports in the top-level project. These pins are removed from a lower-level netlist when it is imported into the top-level design.

Virtual Pin Timing & Location Assignments

One of the main issues in bottom-up design methodologies is that each individual design block includes no information about how it is connected to other design blocks. If you turn on the option to write virtual pin assignments, you can also turn on options to constrain these virtual pins to achieve better timing performance once the lower-level partitions are integrated at the top level.

When **Place created virtual pins at location of at top-level source/sink** is turned on, the script includes location constraints for each virtual pin created. Virtual output pins are assigned to the location of the connection's destination in the top-level project, and virtual input pins are assigned to the location of the connection's source in the top-level project. Note that if the top-level design uses Empty partitions, the final location of the connection is not known but the pin is still assigned to the LogicLock region that contains its source or destination.

As a result, these virtual pins are no longer placed inside the LogicLock region of the lower-level project, but at their location in the top-level design, eliminating resource consumption in the lower-level project and providing more information about lower-level projects and their port dependencies. These location constraints are not imported into the top-level project.

When **Add maximum delay to/from created virtual pins** is turned on, the script includes a timing constraint for each virtual pin created. The value you enter in the dialog box is the maximum delay allowed to and from all paths between virtual pins to help meet the timing requirements for the complete design. The software uses the OUTPUT_MAX_DELAY assignment or INPUT_MAX_DELAY assignment to apply the constraint.

This option allows the project lead to specify a general timing budget for all lower-level internal pin connections. The lower-level designer can override these constraints by applying individual node-level assignments on any specific pin as needed.

LogicLock Region Assignments

When **Copy LogicLock region assignments from top-level** is turned on, the script includes assignments identifying the LogicLock assignment for the partition.

The script can also pass assignments to create the LogicLock regions for all other partitions. When **Include all LogicLock regions in lower-level projects** is turned on, the script for each partition includes all LogicLock region assignments for the top-level project and each lower-level partition, revealing the floorplan for the complete design in each partition. Regions that do not belong to other partitions contain virtual pins representing the source and destination ports for cross-partition connections. This allows each designer to more easily view the connectivity between their partition and other partitions in the top-level design, and helps ensure that resource conflicts at the top-level are minimized.

When **Remove existing LogicLock regions from lower-level projects** is turned on, the script includes commands to remove LogicLock regions defined in the lower-level project prior to running the script. This ensures that LogicLock regions not part of the top-level project do not become part of the complete design, and avoids any location conflicts by ensuring lower-level designs use the LogicLock regions specified at the top level.

Global Signal Promotion Assignments

To help prevent conflicts in global signal usage when importing projects into the top-level design, you can choose to write assignments that control how signals are promoted to global routing resources in the lower-level partitions. These options can help resource balancing of global routing resources.

When **Promote top-level global signals in lower-level projects** is turned on, the Quartus II software searches partition netlists and identifies global resources, including clock signals. For the relevant partitions, the script then includes a global signal promotion assignment, providing information to the lower-level projects about global resource allocation.

When **Disable automatic global promotion in lower-level projects** is turned on, the script includes assignments that turn off all automatic global promotion settings in the lower-level projects. These settings include: the Auto Global Memory Control Signals logic option, output enable logic options, and clock and register control promotions. If you select the **Disable automatic global promotion in lower-level projects** option in conjunction with the **Promote top-level global signals in**

lower-level projects option, you can ensure that only signals promoted to global resources in the top-level are promoted in the lower-level projects.

Makefile Generation

Makefiles allow you to use 'make' commands to ensure that a bottom-up project is up-to-date if you have a make utility installed on your computer. The **Generate makefiles to maintain lower-level and top-level projects** option creates a makefile for each design partition in the top-level design, as well as a master makefile that can run the lower-level project makefiles. The Quartus II software places the master makefiles in the top-level directory, and the partition makefiles in their corresponding lower-level project directories.

Makefiles use the directory locations generated using the **Create lower-level project if one does not exist** option. If you created your lower-level projects without using this option, you must modify the variables at the top of the makefile to specify the directory location for each lower-level project.

To run the makefiles, use a command such as `make -f master_makefile.mak` from the script output directory. The master makefile first runs each lower-level makefile, which sources its Tcl script and then generates a Quartus II Exported Partition file to export the project as a design partition. Next, the top-level makefile is run which specifies these newly generated Quartus II Exported Partition files as the import files for their respective partitions in the top-level project. The top-level makefile then imports the lower-level results and performs a full compilation, producing a final design.

To exclude a certain partition from being compiled, edit the `EXCLUDE_FLAGS` section of **master_makefile.mak** according to the instructions in the file, and specify the appropriate options. You can also exclude some partitions from being built, exported, or imported using make commands. To exclude a partition, run the makefile using a command such as the one for the GNU make utility shown in the following example:

```
gnumake –f master_makefile.mak exclude_<partition directory>=1 ↵
```

This command instructs that the partition whose output files are in <*partition directory*> are not built. Multiple directories can be excluded by adding multiple `exclude_`<*partition directory*> commands. Command-line options override any options in the makefile.

Another feature of makefiles is the ability to have the master makefile invoke the low-level makefiles in parallel on systems with multiple processors. This option can help designers working with multiple CPUs greatly improve their compilation time. For the GNU make utility, add the `-j<N>` flag to the make command. The value <*N*> is the number of processors that can be used to run the build.

User Scenarios—Incremental Compilation Application Examples

To better illustrate the applications and behavior of the full incremental compilation flow, the following section presents several possible user scenarios. All scenarios assume you have set up the project to use the full incremental compilation flow, using the steps described in "Preparing a Design for Incremental Compilation" on page 1–12. These scenarios are divided into two sections:

- Top-Down Incremental Design Flows
- Bottom-Up Design Flows

Top-Down Incremental Design Flows

There are four top-down incremental design flow examples:

- Scenario 1—Changing a Source File for One of Multiple Partitions in a Top-Down Compilation Flow
- Scenario 2—Optimizing the Placement for One of Multiple Partitions in a Top-Down Compilation Flow
- Scenario 3—Preserving One Critical Partition in a Multiple-Partition Design in a Top-Down Compilation Flow
- Scenario 4—Placing All but One Critical Partition in a Multiple-Partition Design in a Top-Down Compilation Flow

Scenario 1—Changing a Source File for One of Multiple Partitions in a Top-Down Compilation Flow

Background: You have just performed a lengthy, complete compilation of a design that consists of multiple partitions. An error is found in the HDL source file for one partition and it is being fixed. Because the design is currently meeting timing requirements and the fix is not expected to affect timing performance, it makes sense to compile only the affected partition and preserve the rest of the design.

Perform the following steps to update the single source file:

1. Apply and save the fix to the HDL source file.

2. On the Assignments menu, click **Design Partition Window**.

3. For the partitions that should be preserved, change the **Netlist Type** to **Post-Fit**. You can set the **Fitter Preservation Level** to either **Placement** or **Placement and Routing**. For the partition that contains the fix, you can change the netlist type to **Source File**. Making the Source File setting is optional because the Quartus II software recompiles partitions if changes are detected in a source file.

4. Click **Start Compilation** to incrementally compile the fixed HDL code. This compilation should take much less time than the initial full compilation.

5. Run simulation again to ensure that the bug is fixed, and use the Timing Analyzer report to ensure that timing results have not degraded.

Scenario 2—Optimizing the Placement for One of Multiple Partitions in a Top-Down Compilation Flow

Background: You have just performed a lengthy full compilation of a design that consists of multiple partitions. The Timing Analyzer reports that the f_{MAX} timing requirement is not met. After some analysis, you believe that timing closure can be achieved if placement can be improved for one particular partition. You have at least three optimization techniques in mind: raising the Placement Effort Multiplier, enabling Physical Synthesis, and running the Design Space Explorer. Because these techniques all involve significant compilation time, it makes sense to apply them (or just one of them) to only the partition in question.

Perform the following steps to raise the Placement Effort Multiplier or enable Physical Synthesis:

1. On the Assignments menu, click **Design Partition Window**.

2. For the partition in question, set the **Netlist Type** to **Post-Synthesis**. This causes the partition to be placed and routed with the new Fitter settings (but not resynthesized) during the next compilation.

3. For the remaining partitions (including the top-level entity), set the **Netlist Type** to **Post-Fit**. Set the **Fitter Preservation Level** to **Placement** to allow for the most flexibility during routing. To reduce compilation time further, use the **Placement and Routing** setting. These partitions are preserved during the next compilation.

4. Apply the desired optimization settings.

5. Click **Start Compilation** to incrementally compile the design with the new settings. During this compilation, the Partition Merge stage automatically merges the post-synthesis netlist of the critical partition with the post-fit netlists of the remaining partitions. This "merged" netlist is fed to the Fitter. The Fitter then refits only one partition. Since the effort is reduced as compared to the initial full compilation, the compilation time is also reduced.

To use Design Space Explorer, perform the following steps:

1. Repeat steps 1–3 of the previous set of steps.

2. Save the project and run Design Space Explorer.

Scenario 3—Preserving One Critical Partition in a Multiple-Partition Design in a Top-Down Compilation Flow

Background: Prior to any compilation, you have some insight into which partition will be the most critical (in terms of timing) after placement and routing. To help achieve timing closure, you decide to use the following compilation flow.

The critical partition is placed and routed by itself, with all optimizations turned on (manually or through Design Space Explorer). After timing closure is achieved for this partition, its content and placement are preserved and the remaining partitions are fit with normal or reduced optimization levels so that the compilation time can be reduced.

This flow generally works only if the critical path is contained inside the partition in question. This is one reason why both the inputs and outputs of each partition should be registered.

For this scenario, perform the following steps:

1. Perform partitioning and floorplan location assignment creation.

2. For the partition expected to be critical, on the Assignments menu, click **Design Partition Window** and set **Netlist Type** to **Source File**.

3. For the remaining partitions (other than any direct or indirect parents of the critical one), set the **Netlist Type** to **Empty**.

4. Click **Start Compilation** to compile with the desired optimizations turned on, or use Design Space Explorer.

5. Check the Timing Analyzer report to ensure that the timing requirements are met. If so, proceed to step 6. Otherwise, repeat step 4 and step 5 until the requirements are met.

6. In the **Design Partition Window**, set the **Netlist Type** to **Post-Fit** for the critical partition. Set the **Fitter Preservation Level** to **Placement and Routing** to preserve the results.

7. Change the **Netlist Type** from **Empty** to **Source File** for the remaining partitions.

8. Turn off the optimizations set in step 4, and compile the design. Turning off the optimizations at this point does not affect the fitted partition, because its Netlist Type is set to **Post-Fit**.

9. Check the Timing Analyzer report to ensure that the timing requirements are met. If not, make design or option changes and repeat step 8 and step 9 until the requirements are met.

This flow is similar to a bottom-up design flow in which a module is implemented separately and is merged into the rest of the design afterwards. Refer to *"Empty Partitions" on page 1–28* for more information about potential issues. Ensure that if there are any partitions representing a design file that is missing from the project, you create a placeholder wrapper file that defines the port interface.

Scenario 4—Placing All but One Critical Partition in a Multiple-Partition Design in a Top-Down Compilation Flow

Background: Prior to any compilation, you have some insight into which partition will be the most critical (in terms of timing) after placement and routing. To help achieve timing closure, you decide to use the following compilation flow.

Only the non-critical partitions are placed and routed initially, using floorplan location assignments. These non-critical partitions are then preserved when the critical partition is introduced into the Fitter, with various optimizations turned on (manually or through Design Space Explorer).

For this scenario, perform the following steps:

1. Perform partitioning and floorplan creation.

2. For the partition expected to be critical, on the Assignments menu, click **Design Partition Window** and set the **Netlist Type** to **Empty**.

3. For the remaining partitions, set the **Netlist Type** to **Source File**.
4. Click **Start Compilation** to compile the non-critical partitions.
5. Check the Timing Analyzer report to ensure that the timing requirements are met. If so, proceed to step 6. Otherwise, make design or option changes and repeat steps 4 and 5 until the requirements are met.
6. In the **Design Partition Window**, set the **Netlist Type** to **Post-Fit** for the processed partitions. Set the **Fitter Preservation Level** to **Placement** to allow for the most flexibility during routing.
7. Change the **Netlist Type** from **Empty** to **Source File** for the partition expected to be critical.
8. Click **Start Compilation** to compile the design with optimizations turned on, or use Design Space Explorer.
9. Check the Timing Analyzer report to ensure that the timing requirements are met. If not, make design or option changes and repeat steps 8 and 9 until the requirements are met.

This flow is similar to a bottom-up design flow, in which a module is implemented separately and is merged into the rest of the design afterwards. Refer to *"Empty Partitions" on page 1–28* for more information about potential issues. Ensure if there are any partitions representing a design file that is missing from the project, that you create a placeholder wrapper file that defines the port interface.

Bottom-Up Design Flows

There are two bottom-up design flow examples:

- Scenario 5—Team-Based Bottom-Up Design Flow
- Scenario 6—Design Iteration in a Bottom-Up Design Flow

Scenario 5—Team-Based Bottom-Up Design Flow

This scenario describes how to use incremental compilation in a bottom-up design flow.

Background: A project consists of several lower-level subdesigns that are implemented separately by different designers. The top-level project instantiates each of these subdesigns exactly once. The subdesign designers want to optimize their designs independently and pass on the results to the project lead.

As the project lead in this scenario, perform the following steps to prepare the design for a successful bottom-up design methodology.

1. Create a new Quartus II project that will ultimately contain the full implementation of the entire design.

2. To prepare for the bottom-up methodology, create a "skeleton" of the design that defines the hierarchy for the subdesigns that will be implemented by separate designers. The top-level design implements the top-level entity in the design and instantiates wrapper files that represent each subdesign by defining only the port interfaces but not the implementation.

3. Make project-wide settings. Select the device, make global assignments for clocks and device I/O ports, and make any global signal constraints to specify which signals can use global routing resources.

4. In the **Settings** dialog box, expand **Compilation Process Settings** and select **Incremental Compilation**. Turn on **Full incremental compilation**, and click **OK**.

5. Make design partition assignments for each subdesign and set the Netlist Type for each design partition that will be imported to **Empty** in the Design Partitions window.

6. Create LogicLock regions for each of the lower-level partitions to create a design floorplan. This floorplan should consider the connectivity between partitions and estimates of the size of each partition based on any initial implementation numbers and knowledge of the design specifications.

7. On the Project menu, click **Generate Bottom-Up Design Partition Scripts**, or launch the script generator from Tcl or the command prompt.

8. Make any changes to the default script options as desired. Altera recommends that you pass all the default constraints, including LogicLock region, for all partitions and virtual pin location assignments. Altera further recommends that you add a maximum delay timing constraint for the virtual I/O connections in each

partition to help timing closure during integration at the top level. If lower-level projects have not already been created by the other designers, use the partition script to set up the projects so that you can easily take advantage of makefiles.

9. Provide each lower-level designer with the Tcl file to create their project with the appropriate constraints. If you using makefiles, provide the makefile for each partition.

As the designer of a lower-level subdesign in this scenario, perform the appropriate set of steps to successfully export your design, whether your design team is using makefiles, or exporting and importing the design manually.

If you are using makefiles, perform the following steps:

1. Use the `make` command and the makefile provided by the project lead to create a Quartus II project with all design constraints, and compile the project.

2. The information about which source file should be associated with which partition is not available to the software automatically, so you must specify this information in the makefile. You must specify the dependencies before the software will rebuild the project after the initial call to the makefile.

3. When you have achieved the desired compilation results and the design is ready to be imported into the top-level design, the project lead can use the `master_makefile` to export this lower-level partition and create a Quartus II Exported Partition file, and then import it into the top-level design.

If you are not using makefiles, perform the following steps:

1. Create a new Quartus II project for the subdesign.

2. Make LogicLock region assignments and global assignments (including clock settings) as specified by the project lead.

3. Make Virtual Pin assignments for ports which represent connections to core logic instead of external device pins in the top-level module.

4. Make floorplan location assignments to the Virtual Pins so that they are placed in their corresponding regions as determined by the top-level module. This provides the Fitter with more information about the timing constraints between modules. Alternately, you can apply timing I/O constraints to the paths that connect to virtual pins.

5. Turn on **Full incremental compilation** and proceed to compile and optimize the design as needed.

6. When you have achieved the design compilation results, on the Project menu, click **Export Project as Design Partition**.

7. Under **Netlist to export**, select the netlist type **Post-fit** netlist to preserve the placement and performance of the subdesign. You can export **Post-Synthesis** netlist instead if placement or performance preservation is not required.

8. Provide the Quartus II Exported Partition file to the project lead.

Finally, as the project lead in this scenario, perform the appropriate set of steps to import the files sent in by the designers of each lower-level subdesign partition.

If you are using makefiles, perform the following steps:

1. Use the `master_makefile` to export each lower-level partition and create Quartus II Exported Partition files, and then import them into the top-level design.

2. The software does not have information about which source file should be associated with which partition, so you must specify this information in the makefile. The software cannot rebuild the project if source files change unless you specify the dependencies.

If you are not using makefiles, perform the following steps:

1. After you obtain the Quartus II Exported Partition file for each subdesign from the other designers on the team, on the Project menu, click **Import Design Partition** and specify the partition in the top-level project that is represented by the subdesign Quartus II Exported Partition file.

2. Repeat the import process described in step 1 for each partition in the design. After you have imported each partition once, you select all the design partitions and use the **Reimport using latest import files at previous locations** option to import all of the files from their previous locations at one time.

Resolving Assignment Conflicts During Import

When importing the subdesigns, the project lead may become aware of some assignment conflicts. This can occur, for example, if the subdesign designers changed their LogicLock regions to account for additional logic or placement constraints, or if the designers applied I/O port timing constraints that differ from constraints added to the top-level project by the project lead. To address these conflicts, the project lead may want to do one or both of the following:

- Allow new assignments to be imported
- Allow existing assignments to be replaced or updated

When LogicLock region assignment conflicts occur, the project lead may want to do one of the following:

- Allow the imported region to replace the existing region
- Allow the imported region to update the existing region
- Skip assignment import for regions with conflicts

The project lead can address all of these situations using the **Advanced Import Settings** as described in **"Importing Assignments & Advanced Import Settings" on page 1–39**.

If the placement of different subdesigns conflict, the project lead can also set the partition's Fitter **Preservation Level to Netlist Only**, which allows the software to re-perform placement and routing with the imported netlist.

Importing a Partition to be Instantiated Multiple Times

In this variation of the scenario, one of the subdesigns is instantiated more than once in the top-level design. The designer of the subdesign may want to compile and optimize the entity once under a lower-level project, and then import the results as multiple partitions in the top-level project.

In this case, placement conflict resolution as described in *"Resolving Assignment Conflicts During Import" on page 1–56* is mandatory because the top-level partitions share the same imported post-fit netlist. If you import multiple instances of a subdesign in the top-level design, the imported LogicLock regions are automatically set to Floating status.

If you choose to resolve conflicts manually, you can use the import options and manual LogicLock assignments to specify the placement of each instance in the top-level design.

Scenario 6—Design Iteration in a Bottom-Up Design Flow

Background: A project consists of several lower-level subdesigns that have been exported from separate Quartus II projects and imported into the top-level design in a bottom-up compilation flow. In this scenario, integration at the top-level has failed because the timing requirements are not met. The timing requirements are met in each individual lower-level project, but critical inter-partition paths in the top-level are causing timing requirements to fail.

After trying various optimizations at the top-level, the project lead determines that they cannot meet the timing requirements given the current lower-level partition placements that were imported. The project lead decides to pass additional constraints to the lower-level projects to improve the placement.

For this scenario, perform the following steps:

1. In the top-level design, on the Project menu, click **Generate Bottom-Up Design Partition Scripts**, or launch the script generator from Tcl or the command line.

2. Because lower-level projects have already been created for each partition, turn off **Create lower-level project if one does not exist**.

3. Make any additional changes to the default script options as desired. Altera recommends that you pass all the default constraints, including LogicLock regions, for all partitions and virtual pin location assignments. Altera also recommends that you add a maximum delay timing constraint for the virtual I/O connections in each partition.

4. The Quartus II software generates Tcl scripts for all partitions, but in this scenario, you would focus on the partitions that make up the cross-partition critical paths. Following are the important assignments in the script:

    - Virtual pin assignments for module pins not connected to device I/O ports in the top-level design.
    - Location constraints for the virtual pins that reflect the initial top-level placement of the pin's source or destination. These help make the lower-level placement "aware" of its

surroundings in the top-level, leading to a greater chance of timing closure during integration at the top-level.
- INPUT_MAX_DELAY and OUTPUT_MAX_DELAY timing constraints on the paths to and from the I/O pins of the partition. These constrain the pins to optimize the timing paths to and from the pins.

5. The project lead provides the scripts to the low-level designers who source the file.
   - To source the Tcl script from the Quartus II GUI, on the Tools menu, click **Utility Windows** and open the Tcl console. Navigate to the script's directory, and type the following command:

     `source <filename> ↵`

   - To source the Tcl script at the command line, type the following command:

     `quartus_cdb -t <filename>.tcl ↵`

6. The lower-level designers recompile their designs with the new assignments.
7. The lower-level designers re-export their results.
8. The top-level designer re-imports the results.
9. You can now analyze the design to determine if the timing requirements have been achieved. Since the lower-level partitions were compiled with more information about connectivity at the top-level, it is more likely that the inter-partition paths have improved placement which helps to meet the timing requirements.

Incremental Compilation Restrictions

This section documents the restrictions and limitations that you may encounter when using incremental compilation, including interactions with other Quartus II features. Some restrictions apply to both top-down and bottom-up design flows, while some additional restrictions apply only to bottom-up design flows.

Using Incremental Compilation with Quartus II Archive Files

The post-synthesis and post-fitting netlist information for each design partition is stored in the project database. When you archive a project, the database information is not included in the archive unless you include the database files in the Quartus II Archive file (**.qar**). In addition, when you

import a design partition into a top-level design, the lower-level design netlist is stored in the project database for the top-level design (the top-level project does not use the original source files or the Quartus II Exported Partition file). If you archive the top-level project, the imported design information is not included unless the database files are included in the Quartus II Archive file.

Altera recommends that you select **Compilation and simulation database files** in the **Archive Project** dialog box if any form of incremental compilation is used so that compilation results are preserved.

OpenCore Plus MegaCore Functions

The circuitry that provides OpenCore® Plus MegaCore® functions is currently incompatible with incremental compilation.

Engineering Change Management With the Chip Editor

When you use the Resource Property Editor to make changes due to engineering change orders (ECOs) after performing a full compilation, recompiling the entire design is not necessary. These changes are made directly to the netlist without performing a new placement and routing. The changes are not made again automatically when you recompile the design.

Because the netlist generated by the Chip Editor is always overwritten by a recompilation, the changes do not appear in the final netlist after recompilation unless they are reapplied. There are change management features to allow you to reapply the changes on subsequent compilations using the Chip Editor, or you can merge the changes back to the source files before the recompilation.

This behavior applies in any compilation, whether or not incremental compilation is turned on.

SignalProbe Feature

SignalProbe® pins are added to the design after compilation so you can add them incrementally to your design without performing a new compilation. However, in the Quartus II software version 6.0, these SignalProbe pins are not part of the netlist after a recompilation of the design using full incremental compilation. Reapply the SignalProbe pin assignments on subsequent compilations, then, on the Processing menu, point to Start and click **Start Check & Save All Netlist Changes**.

During the export of a lower-level design in a bottom-up compilation flow, the software removes SignalProbe logic. You can use SignalProbe in lower-level projects to debug your design and then export the design without these debugging ports when it is imported and combined with other logic at the top level.

SignalTap II Logic Analyzer & Logic Analyzer Interface in Bottom-Up Compilation Flows

The SignalTap® II logic analyzer and External Logic Analyzer Interface are not supported in lower-level projects in a bottom-up incremental compilation flow. These features are supported for the top-level project only after lower-level partitions have been imported, and are fully supported in top-down incremental compilation.

For details about using the SignalTap II logic analyzer in an incremental design flow, refer to the *Design Debugging Using the SignalTap II Embedded Logic Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Restrictions on Megafunction Partitions

The Quartus II software does not support partitions for megafunction instantiations. If you use the MegaWizard Plug-In Manager to customize a megafunction variation, the MegaWizard-generated wrapper file instantiates the megafunction. You can create a partition for the MegaWizard-generated megafunction custom variation wrapper file.

The Quartus II software does not support the creation of a partition for inferred megafunctions (that is, where the software infers a megafunction to implement logic in your design). If you have a module or entity for the logic that is inferred, you can create a partition for that hierarchy level in the design.

The Quartus II software does not support creation of a partition for any Quartus II internal hierarchy that is dynamically generated during compilation to implement the contents of a megafunction.

Nodes Created & Changed During Routing

Node names are preserved through synthesis and fitting when using incremental compilation. Some nodes that the router creates and inserts may change if the Fitter preservation level is not set to **Placement and Routing**. You may also see slightly different numbers of logic cells due to logic cells being used to achieve better routing. In addition, the fit results

may be slightly different due to optimizations performed during routing, such as rotation of the inputs to the look-up table (LUT) within the logic cell.

Routing Preservation in Bottom-Up Compilation Flows

The Quartus II software does not export routing information from lower-level partitions in a bottom-up methodology, so you can not import routing information into the top-level partition.

For imported netlists, the Post-Fit netlist contains the atoms and the placement information of the partition. Therefore, when the Quartus II software uses a Post-Fit netlist for a partition, the placement of the partition is preserved. Performance preservation can typically be achieved even though the routing of the partition is not restored, because the router is generally not as sensitive to small changes in input as the Fitter. In some designs, you may see variation in performance due to changed routing. To ensure that you do not experience any problems due to this effect, you can optimize your design to achieve a margin of 1 or 2% on your timing requirements.

Delay chain values are not preserved with bottom-up incremental compilation. Delay chain values are routing-dependent, and because routing is not preserved, delay chain values may change even if a Post-Fit netlist is used.

Bottom-Up Design Partition Script Limitations

The Quartus II software version 6.0 has some limitations related to bottom-up design partition scripts. Many of these limitations will be removed in future versions of the software.

Wildcard Support in Bottom-Up Design Partition Scripts

When applying constraints with wildcards, wildcards are not analyzed across hierarchical boundaries. For example, an assignment could be made to these nodes: **Top|A:inst|B:inst|***, where **A** and **B** are lower-level partitions, and hierarchy **B** is a child of **A**, that is **B** is instantiated in hierarchy **A**. This assignment is applied to modules **A**, **B** and all children instances of **B**. However, the assignment **Top|A:inst|B:inst*** is applied to hierarchy **A**, but is not applied to the **B** instances because the single level of hierarchy represented by **B:inst*** is not expanded into multiple levels of hierarchy. To avoid this issue, ensure that you apply the wildcard to the hierarchical boundary if it should represent multiple levels of hierarchy.

When using the wildcard to represent a level of hierarchy, only single wildcards are supported. This means assignments such as **Top|A:inst|*|B:inst|*** are not supported. The Quartus II software issues a warning in these cases.

Derived Clocks & PLLs in Bottom-Up Design Partition Scripts

If a clock in the top level is not directly connected to a pin of a lower-level partition, then the lower-level partition does not receive assignments and constraints from the top-level pin in the design partition scripts.

This issue is of particular importance for clock pins that require timing constraints and clock group settings. Problems can occur if your design uses logic or inversion to derive a new clock from a clock input pin. Make appropriate timing assignments in your lower-level Quartus II project to ensure that clocks are not unconstrained.

In addition, if you use a PLL in your top-level design and connect it to lower-level partitions, the lower-level partitions do not have information about the multiplication or phase shift factors in the PLL. Make appropriate timing assignments in your lower-level Quartus II project to ensure that clocks are not unconstrained or constrained with the incorrect frequency.

Virtual Pin Timing Assignments in Bottom-Up Design Partition Scripts

The design partition scripts use INPUT_MAX_DELAY and OUTPUT_MAX_DELAY assignments to specify the inter-partition delays associated with input and output pins which would not otherwise be visible to the project. These assignments require that the software specify the clock domain for the assignment, and the software sets this clock domain to **'*'**. This means that there may be some paths constrained and reported by the timing analysis engine that are not required.

To restrict which clock domains are included in these assignments, edit the generated scripts or change the assignments in your lower-level Quartus II project.

Top-Level Ports that Feed Multiple Lower-Level Pins in Bottom-Up Design Partition Scripts

When a single top-level I/O port drives multiple pins on a lower-level module, it unnecessarily restricts the quality of the synthesis and placement at the lower-level. This occurs because in the lower-level design, the software must maintain the hierarchical boundary and cannot use any information about pins being logically equivalent at the top level. In addition, because I/O constraints are passed from the top-level pin to

each of the children, it is possible to have more pins in the lower level than at the top level, and these pins use the top-level I/O constraints and placement options that might make them impossible to place at the lower-level. The software avoids this situation when possible, but it is best to avoid this design practice to avoid these potential problems. Restructure your design so that the single I/O port feeds the design partition boundary, and then the connection is split into multiple signals within the lower-level partition.

Support for the TimeQuest Timing Analyzer & SDC Constraints

If you use constraints with the TimeQuest Timing Analyzer, the assignments are not passed to the lower levels. You must use constraints made for the Classic Timing Analyzer. You can then use the **Generate SDC File from QSF** command to convert the Classic Timing Analyzer constraints in a Quartus II Settings File (**.qsf**) to a Synopsys Design Constraints (**.sdc**) for the TimeQuest analyzer.

For more information about timing constraints and conversion from the QSF file to the SDC file, refer to *Classic Timing Analyzer*, *TimeQuest Timing Analyzer*, and *Switching to the TimeQuest Timing Analyzer* chapters in volume 3 of the *Quartus II Handbook*.

Register Packing & Partition Boundaries

The Quartus II software automatically performs register packing during compilation. However, when incremental compilation is enabled, logic in different partitions cannot be packed together because partition boundaries prevent cross-boundary optimization. (Refer to "Guidelines for Creating Good Design Partitions" on page 1–20 for more information.) This restriction applies for all types of register packing, including I/O cells, DSP blocks, sequential logic, and unrelated logic.

I/O Register Packing

Cross-partition register packing of I/O registers is allowed in certain cases where your input and output pins exist in the top hierarchy level (and the Top partition), but the corresponding I/O registers exist in other partitions.

The following specific circumstances are required for cross-partition register packing of input pins:

- The input pin feeds exactly one register
- The path between the input pin and the register includes only input ports of partitions that have one fan-out each

The following specific circumstances are required for cross-partition register packing of output registers:

- The register feeds exactly one output pin
- The output pin is fed by only one signal
- The path between the register and the output pin includes only output ports of partitions that have one fan-out each

Output pins with an output enable signal cannot be packed into the device I/O cell if the output enable logic is part of a different partition from the output register. To allow register packing for output pins with an output enable signal, structure your HDL code or design partition assignments so that the register and the tri-state logic are defined in the same partition.

Bidirectional pins are handled in the same way as output pins with an output enable. If the registers that need to be packed are in the same partition as the tri-state logic, then register packing can be performed.

The restrictions on tri-state logic are due to the fact that the I/O atom (device primitive) is created as part of the partition that contains the tri-state logic. If an I/O register and its tri-state logic are contained in the same partition, the register can always be packed with the tri-state logic into the I/O atom. The same cross-partition register packing restrictions also apply to I/O atoms for input and output pins. The I/O atom must feed the I/O pin directly with exactly one signal and the path between the I/O atom and the I/O pin must include only ports of partitions that have one fan-out each.

Examples of I/O Register Packing Across Partition Boundaries

The following examples provide detailed explanations for various I/O and partition configurations. The examples use BDF schematics to illustrate the design logic.

Example 1—Output Register in Partition Feeding Output Pin
In this example, a subdesign contains a single register, as shown in Figure 1–15. As shown in Figure 1–16, the top-level design instantiates the subdesign with a single fanout directly feeding an output pin, and designates the subdesign as a separate design partition.

Figure 1–15. Subdesign with One Register, Designated as a Separate Partition

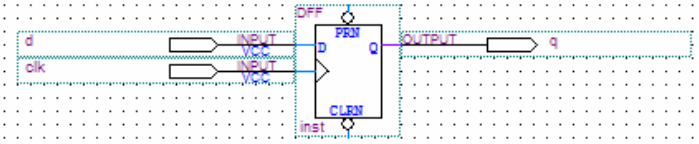
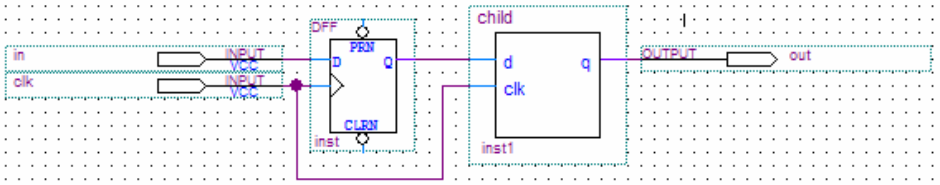


Figure 1–16. Top-level Design Instantiating the Subdesign in Figure 1–15 as an Output Register

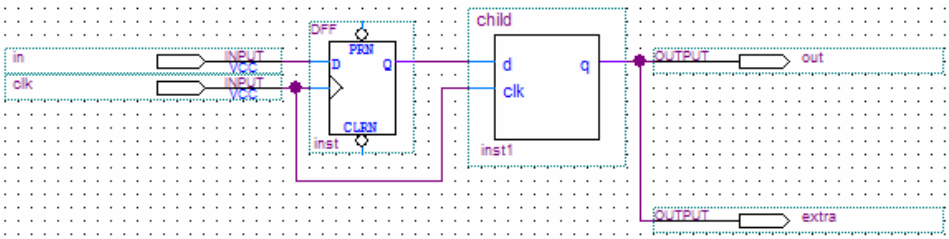


The Quartus II software performs cross-partition register packing if there is a Fast Output Register assignment on pin "out." This type of cross-partition output register packing is permitted because the port interface of the subdesign partition does not need to be changed and the partition port feeds an output pin directly.

Example 2—Output Register in Partition Feeding Multiple Output Pins

In this example, a subdesign designated as a separate partition contains a register as in Figure 1–15. The top-level design instantiates the subdesign as an output register with more than one fanout signal, as shown in Figure 1–17.

Figure 1–17. Top-level Design Instantiating the Subdesign in Figure 1–15 with Two Output Pins



In this case, the software does not perform output register packing. If there is a Fast Output Register assignment on pin "out", the software issues a warning that the fitter can't pack the node to an I/O pin because the node and the I/O cell are connected across a design partition boundary.

This kind of cross partition register packing is not permitted because it would require modification to the interface of the subdesign partition. In order to perform incremental compilation, the interface of design partitions must be preserved.

To allow the software to pack the register in the subdesign from Figure 1–15 with the output pin "out" in Figure 1–17, make one of the following changes:

- Remove the design partition assignment to the subdesign. This allows the fitter to perform all cross hierarchy optimizations, however, prevents you from using incremental compilation for this block of hierarchy. A good design partition should have a well-defined interface so that the Fitter does not have to perform cross-boundary optimizations.
- Restructure your HDL code to place the register in the same partition as the output pin. The simplest option is to move the register from the subdesign partition into the partition containing the output pin. This guarantees that the fitter can optimize the two nodes without violating any partition boundaries.
- Restructure your HDL code so the register feeds only one output pin. Turn off the Analysis & Synthesis setting **Remove Duplicate Registers**. Duplicate the register in your subdesign HDL as in Figure 1–18 so that each register feeds only one pin, then connect the extra output pin to the new port in the top-level design as shown in Figure 1–19. This converts the cross-partition register packing into the simplest case where the register has a single fanout.

Figure 1–18. Modified Subdesign from Figure 1–15 with Two Output Registers & Two Output Ports

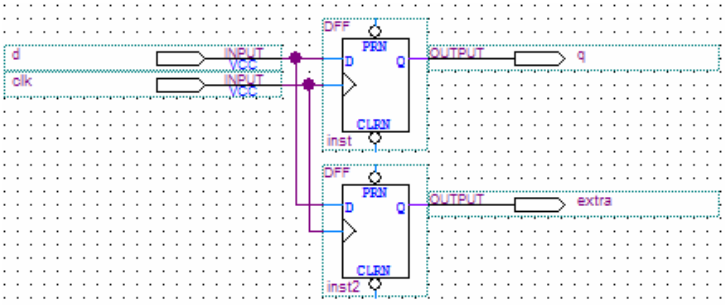
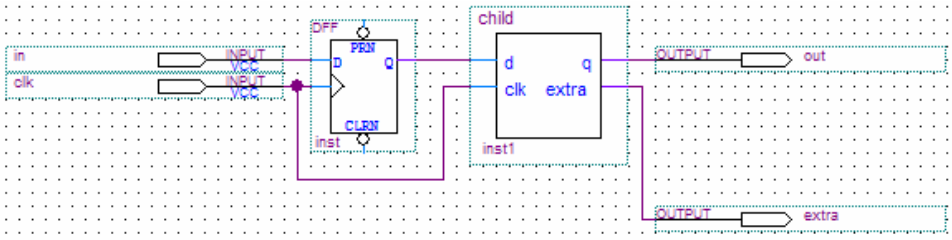


Figure 1–19. Modified Top-Level Design from Figure 1–17 Connecting Two Output Ports to Output Pins



Example 3—Output Register, Output Enable Register & Tri-State Logic in Partition Feeding Output Pin

In this example, a subdesign designated as a separate partition contains an output register, an output enable register, and the tri-state logic to drive the output pin, as shown in Figure 1–20. The top-level design instantiates the subdesign with a single fanout directly feeding an output pin, as shown in Figure 1–21.

Figure 1–20. Subdesign with Output Register, Output Enable Register & Tri-State Logic, Designated as a Separate Partition

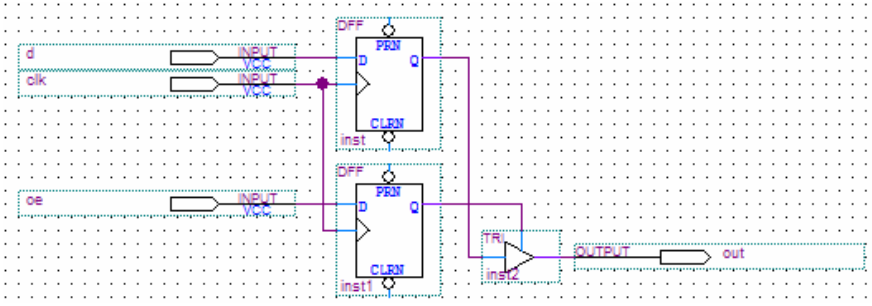
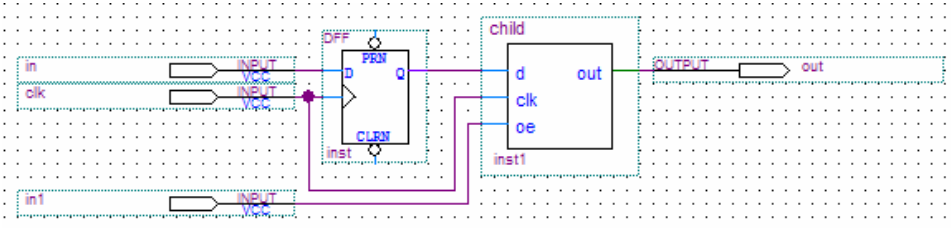


Figure 1–21. Top-level Design Instantiating the Subdesign in Figure 1–20



The Quartus II software performs cross-partition register packing if there is a Fast Output Register assignment and/or Fast Output Enable Register assignment on pin "out." This kind of cross-partition output register packing is permitted because the port interface of the subdesign partition does not need to be changed, no logic needs to be optimized across the partition boundary, and the partition port feeds an output pin directly.

Example 4—Output Register and/or Output Enable Register in Partition Feeding Tri-State Output Pin

In this example, a subdesign designated as a separate partition contains two registers, as shown in Figure 1–22. The top-level design instantiates the subdesign with the registers driving the output and the output enable signal for an output pin, as shown in Figure 1–23.

Figure 1–22. Subdesign with Two Registers, Designated as a Separate Partition

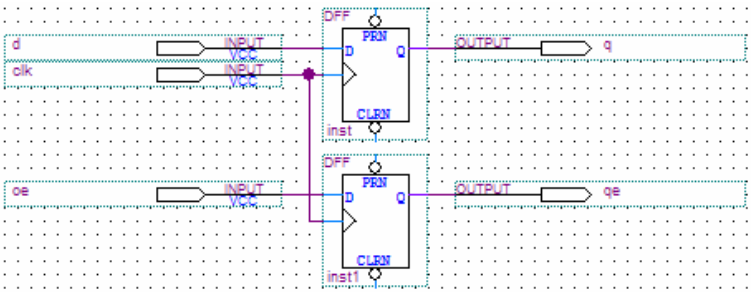
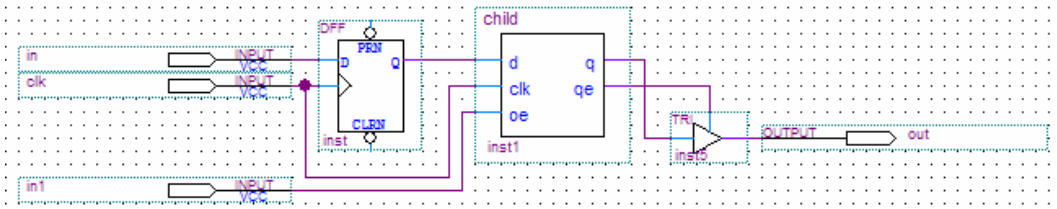


Figure 1–23. Top-level Design Instantiating the Subdesign in Figure 1–24 to Drive Output Enable Logic



In this case, the software can not perform register packing. If there is a Fast Output Register or Fast Output Enable Register assignment on pin "out," the software issues a warning that the fitter can't pack the node to an I/O pin because the node and the I/O cell are connected across a design partition boundary.

The same restrictions apply in the case that the top-level design includes either the output register or the output enable register as well as the tri-state logic. The software can not pack the register that is part of the subdesign partition into the I/O register.

This type of register packing is not permitted because it would require moving logic across a design partition boundary to place into a single I/O device atom. To perform register packing, either the register(s) must be moved out of the subdesign partition or the tri-state logic must be moved into the subdesign partition. In order to guarantee correctness of the design with subsequent incremental compilations, the contents of design partitions must be preserved.

To allow the software to pack the output register and/or output enable register in the subdesign from Figure 1–22 with the output pin "out" in Figure 1–23, make one of the following changes:

- Remove the design partition assignment to the subdesign. This allows the Fitter to perform all cross hierarchy optimizations, however, prevents you from using incremental compilation for this block of hierarchy. A good design partition should have a well defined interface so that the Fitter does not need to perform cross-boundary optimizations.
- Restructure your HDL code to place the register in the same partition as the output pin. The simplest option is to move the register from the subdesign partition into the top-level partition containing the output pin. This guarantees that the fitter can optimize the two nodes without violating any partition boundaries.
- Restructure your HDL code so the register and the tri-state logic are contained in the same partition. Move the tri-state logic from the top-level block into the subdesign with both registers as shown in Figure 1–20. Then connect the subdesign to an output pin in the top-level design, as shown in Figure 1–21.

Example 5—Bidirectional Logic in Partition Feeding Bidirectional Pin
The behavior for bidirectional pins is similar to that of an output pin with an output enable. To allow register packing, the registers must be included in the same partition as the tri-state logic that drives the bidirectional pin.

In this example, a subdesign designated as a separate partition contains three registers and the tri-state logic for a bidirectional pin, as shown in Figure 1–24. The top-level design instantiates the subdesign with ports feeding bidirectional and output pins, as shown in Figure 1–25.

Figure 1–24. Subdesign with Three Registers & Tri-State Logic, Designated as a Separate Partition

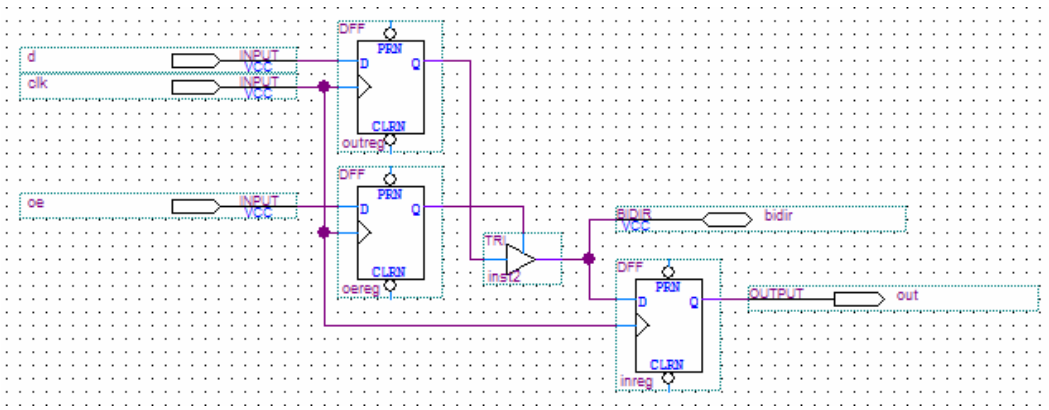
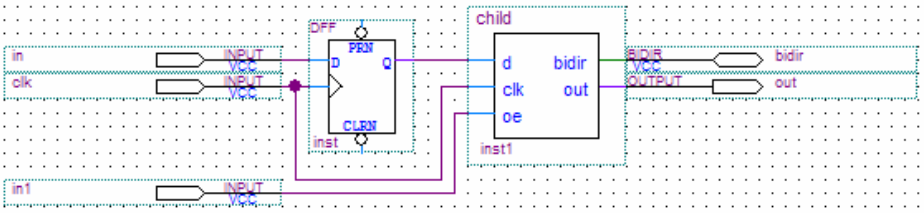


Figure 1–25. Top-level Design Instantiating the Subdesign in Figure 1–27



The Quartus II software performs cross-partition register packing if there is a Fast Output Register, Fast Output Enable Register, or Fast Input Register assignment on pin `bidir`. This type of cross-partition output register packing is permitted because the port interface of the subdesign partition does not need to be changed and the partition port feeds a bidirectional pin directly.

Registers can not be packed in designs that have the registers and tri-state logic in different partitions. The situations described in "Example 4—Output Register and/or Output Enable Register in Partition Feeding Tri-State Output Pin" on page 1–68 apply similarly to bidirectional pins if you replace the output pin "out" with a bidirectional pin in the top-level design.

Example 6—Input Register in Partition Fed by Input Pin
In this example, a subdesign contains a single register, as shown in Figure 1–26. The top-level design instantiates the subdesign with a single `fanin` directly fed by an input pin, as shown in Figure 1–27, and designates the subdesign to be a separate design partition.

Figure 1–26. Subdesign with One Register, Designated as a Separate Partition

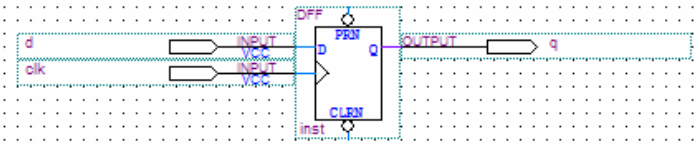
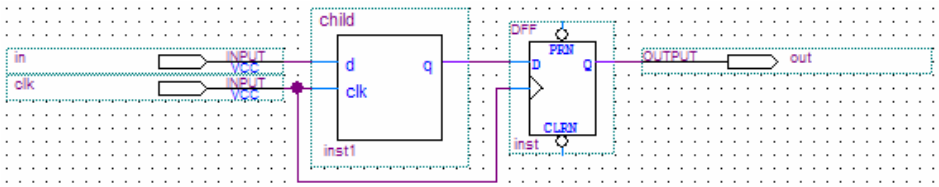


Figure 1–27. Top-level Design Instantiating the Subdesign in Figure 1–26 as an Input Register

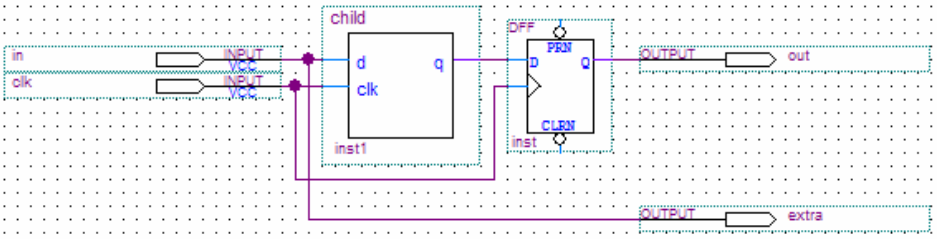


The Quartus II software performs cross-partition register packing if there is a Fast Input Register assignment on pin "in." This type of cross-partition output register packing is permitted because the port interface of the subdesign partition does not have to be changed and the partition port is fed by an input pin directly.

Example 7—Input Register in Partition Fed by Input with Multiple Fanout

In this example, a subdesign designated as a separate partition contains a register as in Figure 1–26. The top-level design instantiates the subdesign as an input register but the input pin also feeds another destination, as shown in Figure 1–28.

Figure 1–28. Top-level Design Instantiating the Subdesign in Figure 1–26 as an Input Register for a Pin with Two Destinations



In this case, the software does not perform input register packing. If there is a Fast Input Register assignment on pin "in," the software issues a warning that the fitter can't pack the node to an I/O pin because the node and the I/O cell are connected across a design partition boundary.

This type of cross-partition register packing is not permitted because it would require modification to the interface of the subdesign partition. In order to perform incremental compilation, the interface of design partitions must be preserved.

To allow the software to pack the register in the subdesign from Figure 1–26 with the input pin "in" in Figure 1–28, make one of the following changes:

- Remove the design partition assignment to the subdesign. This allows the fitter to perform all cross-hierarchy optimizations, however, it also prevents you from using incremental compilation for this block of hierarchy. A good design partition should have a well defined interface so that the Fitter does not have to perform cross-boundary optimizations.
- Restructure your HDL code to place the register in the same partition as the input pin. The simplest option is to move the register from the subdesign partition into the partition containing the input pin. This guarantees that the fitter can optimize the two nodes without violating any partition boundaries.

Example 8—Inverted Input Register in Partition Fed by Input Pin
In this example, a subdesign designated as a separate partition contains an inverted register as in Figure 1–29. The top-level design instantiates the subdesign as an input register, as shown in Figure 1–30.

Figure 1–29. Subdesign with an Inverted Register, Designated as a Separate Partition

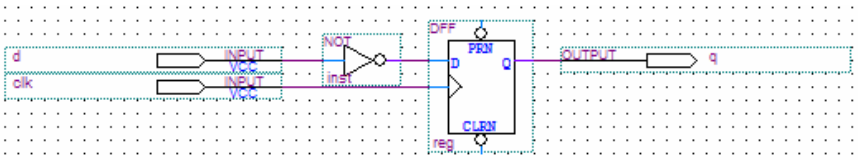
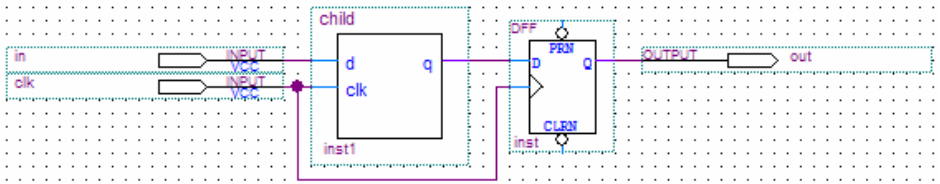


Figure 1–30. Top-level Design Instantiating the Subdesign in Figure 1–29 as an Input Register



The Quartus II software performs cross-partition register packing if there is a Fast Input Register assignment on pin "in." This kind of cross-partition input register packing is permitted because the software can implement the logic for the inversion with the input register inside the partition, and then the partition port is fed by an input pin directly.

Example 9—Input Register in Partition Fed by Inverted Input Pin, or Output Register in Partition Feeding Inverted Output Pin

In this example, a subdesign designated as a separate partition contains a register as in Figure 1–31. The top-level design in Figure 1–32 instantiates the subdesign as an input register with the input pin inverted. The top-level design in Figure 1–33 instantiates the subdesign as an output register with the signal inverted before feeding an output pin.

Figure 1–31. Subdesign with One Register, Designated as a Separate Partition

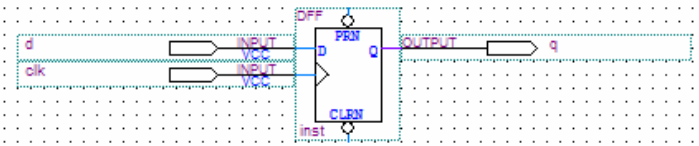


Figure 1–32. Top-level Design Instantiating the Subdesign in Figure 1–31 as an Input Register with an Inverted Input Pin

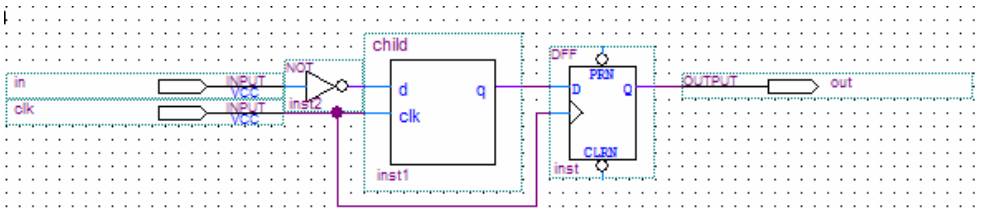
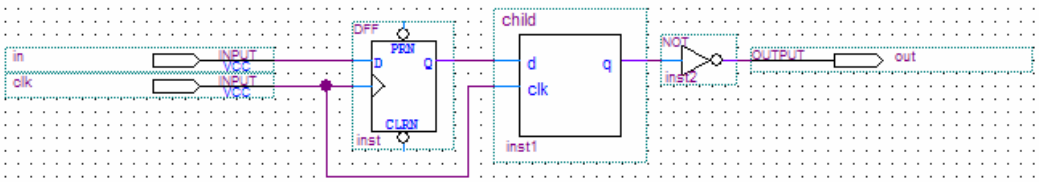


Figure 1–33. Top-level Design Instantiating the Subdesign in Figure 1–32 as an Output Register Feeding an Inverted Output Pin



In these cases, the software does not perform register packing. If there is a Fast Input Register assignment on "in" in Figure 1–32 or a Fast Output Register assignment on pin "out" in Figure 1–33, the software issues a warning that the fitter can't pack the node to an I/O pin because the node and the I/O cell are connected across a design partition boundary.

This type of register packing is not permitted because it would require moving logic across a design partition boundary to place into a single I/O device atom. To perform register packing, either the register must be moved out of the subdesign partition or the inverter must be moved into the subdesign partition to be implemented in the register. In order to guarantee correctness of the design with subsequent incremental compilations, the contents of design partitions must be preserved.

To allow the software to pack the register in the subdesign from Figure 1–31 with the input pin "in" in Figure 1–32 or the output pin "out" in Figure 1–33, make one of the following changes:

- Remove the design partition assignment from the subdesign. This allows the fitter to perform all cross hierarchy optimizations, however, it prevents you from using incremental compilation for this block of hierarchy. A good design partition should have a well defined interface so that the Fitter does not have to perform cross-boundary optimizations.
- Restructure your HDL code to place the register in the same partition as the pin. The simplest option is to move the register from the subdesign partition into the top-level partition containing the pin. This ensures that the fitter can optimize the two nodes without violating any partition boundaries.
- Restructure your HDL code so the register and the inverter are contained in the same partition. Move the inverter from the top-level block into the subdesign as shown in Figure 1–29 for an input pin. Then connect the subdesign to a pin in the top-level design, as shown in Figure 1–30 for an input pin.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The *Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Generate Incremental Compilation Tcl Script Command

To create a template Tcl script for full incremental compilation, use the Generate Incremental Compilation Tcl Script feature. Right-click in the **Design Partition Window** and click **Generate Incremental Compilation Tcl Script**.

If you have made any partition assignments in the user interface, this script contains the Tcl equivalents of the assignments. The Tcl assignments are described in the following sections.

Preparing a Design for Incremental Compilation

To set or modify the current mode of incremental compilation, use the following command:

```
set_global_assignment -name INCREMENTAL_COMPILATION \
<value>
```

The incremental compilation <*value*> setting must be one of the following values:

- `FULL_INCREMENTAL_COMPILATION`—Full incremental compilation
- `INCREMENTAL_SYNTHESIS`—Incremental synthesis only
- `OFF`—No incremental compilation is performed

Creating Design Partitions

To create a partition, use the following command:

```
set_instance_assignment -name PARTITION_HIERARCHY \
<file name> -to <destination> -section_id <partition name>
```

The <*destination*> should be the entity's short hierarchy path. A short hierarchy path is the full hierarchy path without the top-level name (including quotation marks), for example:

```
"ram:ram_unit|altsyncram:altsyncram_component"
```

(with quotation marks). For the top-level partition, you can use the pipe (|) symbol to represent the top-level entity.

For more information on hierarchical naming conventions, refer to *Node-Naming Conventions in Quartus II Integrated Synthesis* in the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

The <*partition name*> is the user-designated partition name, which must be unique and less than 1024 characters. The name can consist only of alphanumeric characters, and the pipe (|), colon (:), and underscore (_) characters. Altera recommends enclosing the name in double quotation marks (`" "`).

The <*file name*> is the name used for internally generated netlists files during incremental compilation. Netlists are named automatically by the Quartus II software based on the instance name if you create the partition in the user interface. If you are using Tcl to create your partitions, you must assign a custom file name that is unique across all partitions. For the top-level partition, the specified file name is ignored, and you can use any dummy value. To ensure the names are safe and platform independent, file names must be unique regardless of case. For example, if a partition uses the file name `my_file`, no other partition can use the file name `MY_FILE`. For simplicity, Altera recommends that you base each file name on the corresponding instance name for the partition.

The software stores all netlists in the **\db** compilation database directory.

Setting Properties of Design Partitions

After a partition is created, set its Netlist Type with the following command:

```
set_global_assignment -name PARTITION_NETLIST_TYPE <value> -section_id \
<partition name>
```

The netlist type <*value*> setting is one of the following values:

- `SOURCE`—Source File
- `POST_SYNTH`—Post-Synthesis
- `POST_FIT`—Post-Fit
- `STRICT_POST_FIT`—Post-Fit (Strict)
- `IMPORTED`—Imported
- `IMPORT_BASED_POST_FIT`—Post-Fit (Import-based)
- `EMPTY`—Empty

Set the Fitter Preservation Level for a post-fit or imported netlist using the following command:

```
set_global_assignment -name PARTITION_FITTER_PRESERVATION_LEVEL <value>\
-section_id <partition name>
```

The fitter preservation level <*value*> setting should be one of the following values:

- `NETLIST_ONLY`—Netlist Only
- `PLACEMENT`—Placement
- `PLACEMENT_AND_ROUTING`—Placement and Routing

For details about these partition properties, refer to "Setting Properties of Design Partitions" on page 1–77.

Recommendations for Creating Good Floorplan Location Assignments—Excluding or Filtering Certain Device Elements (Such as RAM or DSP Blocks)

Resource filtering uses the optional Tcl argument `-exclude_resources` in the `set_logiclock_contents` function of the LogicLock Tcl package. If left unspecified, no resource filter is created.

The argument takes a list of resources-to-be-excluded as input. The list is a colon-delimited string of the following keywords:

Table 1–4. Resources-to-be-Excluded Keywords

Keyword	Resource
REGISTER	Maps to any registers in the logic cells
COMBINATIONAL	Maps to any combinational elements in the logic cells
SMALL_MEM	Maps to the M512 memory blocks
MEDIUM_MEM	Maps to the M4K memory blocks
LARGE_MEM	Maps to the M-RAM memory blocks
DSP	Maps to any DSP blocks

For example, the following command assigns everything under **alu:alu_unit** to the ALU region, excluding all the DSP and M512 blocks:

```
set_logiclock_contents -region ALU -to alu:alu_unit -exclude_resources \
"DSP:SMALL_MEM"
```

In the QSF file, resource filtering uses an extra LogicLock membership assignment called `LL_MEMBER_RESOURCE_EXCLUDE`. For example, the following line in the QSF is used to specify a resource filter for the **alu:alu_unit** entity assigned to the ALU region. The value of the assignment takes the same format as the resource listing string taken by the previous Tcl command.

```
set_instance_assignment -name LL_MEMBER_RESOURCE_EXCLUDE "DSP:SMALL_MEM" \
-to "alu:alu_unit" -section_id ALU
```

Generating Bottom-Up Design Partition Scripts

To generate scripts, type the following Tcl command at a Tcl prompt:

```
generate_bottom_up_scripts <options> ↵
```

The command is part of the `database_manager` package, which must be loaded using the following command before the command can be used:

```
load_package database_manager
```

You must open a project before you can generate scripts.

The Tcl options are the same as those available in the GUI. The exact format of each option is specified in Table 1–5.

Table 1–5. Options for Generating Bottom-Up Partition Scripts with Tcl Commands

Option	Default
`-include_makefiles` <*on*|*off*>	On
`-include_project_creation` <*on*|*off*>	On
`-include_virtual_pins` <*on*|*off*>	On
`-include_virtual_pin_timing` <*on*|*off*>	On
`-include_virtual_pin_locations` <*on*|*off*>	On
`-include_logiclock_regions` <*on*|*off*>	On
`-include_all_logiclock_regions` <*on*|*off*>	On
`-include_global_signal_promotion` <*on*|*off*>	Off
`-include_pin_locations` <*on*|*off*>	On
`-include_timing_assignments` <*on*|*off*>	On
`-include_design_partitions` <*on*|*off*>	On
`-remove_existing_regions` <*on*|*off*>	On
`-disable_auto_global_promotion` <*on*|*off*>	Off
`-bottom_up_scripts_output_directory` <*output directory*>	Current project directory
`-virtual_pin_delay` <*delay in ns*>	*(1)*

Note to Table 1–5:
(1) No default.

The following example shows how to use the Tcl command:

```
load_package database_manager
set project test_proj
project_open $project
generate_bottom_up_scripts -bottom_up_scripts_output_directory test \
    -include_virtual_pin_timing on -virtual_pin_delay 1.2
project_close
```

Command Line Support

To generate scripts at the command prompt, type the following command:

```
quartus_cdb <project name> --generate_bottom_up_scripts=on <options> ↵
```

Once again the options map to the same as those in the GUI. To add an option, append "--<*option_name*>=<*val*>" to the command line call.

The command prompt options are the same as those available in the GUI, and are listed in Table 1–6.

Table 1–6. Options for Generating Bottom-Up Partition Scripts

Option	Default
--include_makefiles_with_bottom_up_scripts=<*on*|*off*>	On
--include_project_creation_in_bottom_up_scripts=<*on*|*off*>	On
--include_virtual_pins_in_bottom_up_scripts=<*on*|*off*>	On
--include_virtual_pin_timing_in_bottom_up_scripts=<*on*|*off*>	On
--bottom_up_scripts_virtual_pin_delay=<*delay in ns*>	*(1)*
--include_virtual_pin_locations_in_bottom_up_scripts=<*on*|*off*>	On
--include_logiclock_regions_in_bottom_up_scripts=<*on*|*off*>	On
--include_all_logiclock_regions_in_bottom_up_scripts=<*on*|*off*>	On
--include_global_signal_promotion_in_bottom_up_scripts=<*on*|*off*>	Off
--include_pin_locations_in_bottom_up_scripts=<*on*|*off*>	On
--include_timing_assignments_in_bottom_up_scripts=<*on*|*off*>	On
--include_design_partitions_in_bottom_up_scripts=<*on*|*off*>	On
--remove_existing_regions_in_bottom_up_scripts=<*on*|*off*>	On
--disable_auto_global_promotion_in_bottom_up_scripts=<*on*|*off*>	Off
--bottom_up_scripts_output_directory=<*output directory*>	Current project directory

Note to Table 1–6:
(1) No default. You must provide this option if you are including virtual pin timing.

Exporting a Partition to be Used in a Top-Level Project

Use the quartus_cdb executable to export a file for a bottom-up incremental compilation flow with the following command:

```
quartus_cdb --INCREMENTAL_COMPILATION_EXPORT=<file> ↵
```

The <*file*> argument is the file path to the exported file.

The command reads the assignment `INCREMENTAL_COMPILATION_EXPORT_NETLIST_TYPE` to determine which netlist type to export; the default is post-fit.

You can also use the flow `INCREMENTAL_COMPILATION_EXPORT` in the `execute_flow` Tcl command contained in the `flow` Tcl package.

The following example exports a post-fit netlist for the current project.

```
load_package flow
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_FILE alu.qxp
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_NETLIST_TYPE \
POST_FIT
execute_flow -INCREMENTAL_COMPILATION_EXPORT
```

To specify the name of the Quartus II Exported Partition file, use the following Tcl command:

```
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_FILE \
<filname>.qxp
```

To turn on the option to always perform exportation following compilation, use the following Tcl command:

```
set_global_assignment -name AUTO_EXPORT_INCREMENTAL_COMPILATION ON
```

Importing a Lower-Level Partition into the Top-Level Project

Use the **quartus_cdb** executable to import a lower-level partition with the following command:

```
quartus_cdb -- INCREMENTAL_COMPILATION_IMPORT ↵
```

You can also use the flow called `INCREMENTAL_COMPILATION_IMPORT` in the `execute_flow` Tcl command contained in the `flow` Tcl package.

The following example script shows how to import a partition using a Tcl script:

```
load_package flow
# commands to set the import-related assignments for each partition
execute_flow --INCREMENTAL_COMPILATION_IMPORT
```

Specify the location for the imported file with the PARTITION_IMPORT_FILE assignment. Note that the file specified by this assignment is read only during importation. For example, the project is completely independent from any files from the lower-level projects after importing. In the command-line and Tcl flow, any partition that has this assignment set to a non-empty value will be imported.

The following assignments specify how the partition should be imported:

```
PARTITION_IMPORT_PROMOTE_ASSIGNMENTS = on | off
PARTITION_IMPORT_NEW_ASSIGNMENTS = on | off
PARTITION_IMPORT_EXISTING_ASSIGNMENTS = \
replace_conflicting | skip_conflicting
PARTITION_IMPORT_EXISTING_LOGICLOCK_REGIONS = \
replace_conflicting | update_conflicting | skip_conflicting
```

Make Files

For an example of how to use incremental compilation with a makefile as part of the bottom-up design flow, refer to the *read_me.txt* file that accompanies the incr_comp example located in the **/qdesigns/incr_comp_makefile** subdirectory. When using a bottom-up incremental compilation flow, the Generate Bottom-Up Design Partition Scripts feature can write makefiles that automatically export lower-level design partitions and import them into the top-level project whenever design files change.

User Scenarios—Incremental Compilation Application Examples

This section provides scripting examples that cover some of the topics discussed in the main section of the chapter.

The script shown in Example 1–1 opens a project called AB_project, sets up two partitions, entities **A** and **B**, for the first time, and performs an initial complete compilation.

Example 1–1. AB_project

```
set project AB_project

package require ::quartus::flow
project_open $project

# Turn on incremental compilation
set_global_assignment -name INCREMENTAL_COMPILATION \
FULL_INCREMENTAL_COMPILATION

# Set up the partitions
set_instance_assignment -name PARTITION_HIERARCHY \
 db/A_inst -to A -section_id "Partition_A"
set_instance_assignment -name PARTITION_HIERARCHY \
 db/B_inst -to B -section_id "Partition_B"

# Set the netlist types to post-fit for subsequent
# compilations (all partitions are compiled during the
# initial compilation since there are no post-fit
# netlists)
set_global_assignment -name PARTITION_NETLIST_TYPE \
 POST_FIT -section_id "Partition_A"
set_global_assignment -name PARTITION_NETLIST_TYPE \
 POST_FIT -section_id "Partition_B"

# Run initial compilation:
export_assignments
execute_flow -full_compile

project_close
```

Scenario 1—Changing a Source File for One of Multiple Partitions

Background: You have run the initial compilation shown in the example script under "User Scenarios—Incremental Compilation Application Examples" on page 1–82. You have modified the HDL source file for partition **A**, and would like to recompile it.

Run the standard flow compilation command in your Tcl script:

```
execute_flow -full_compile
```

Or, run the following command at a system command prompt:

```
quartus_sh --flow compile AB_project↵
```

Assuming the source files for partition **B** do not depend on **A**, only **A** is recompiled. The placement of **B** and its timing performance is preserved, which also saves significant compilation time.

Scenario 2—Optimizing the Placement for One of Multiple Partitions

Background: You have run the initial compilation shown in the example script under "User Scenarios—Incremental Compilation Application Examples" on page 1–82. You would like to apply fitter optimizations, such as physical synthesis, only to partition **A**. No changes have been made to the HDL files.

To ensure the previous compilation result for partition **B** is preserved, and to ensure that fitter optimizations are applied to the post-synthesis netlist of partition **A**, set the netlist type of **B** to Post-Fit (which was already done in the initial compilation, but is repeated here for safety), and the netlist type of **A** to Post-Synthesis, as shown in the following script:

```
set project AB_project

package require ::quartus::flow
project_open $project

# Turn on Physical Synthesis Optimization
set_global_assignment -name \
PHYSICAL_SYNTHESIS_REGISTER_RETIMING ON

# For A, set the netlist type to post-synthesis
set_global_assignment -name PARTITION_NETLIST_TYPE POST_SYNTH \
-section_id "Partition_A"

# For B, set the netlist type to post-fit
set_global_assignment -name PARTITION_NETLIST_TYPE POST_FIT \
-section_id "Partition_B"

# Run incremental compilation:
export_assignments
execute_flow -full_compile

project_close
```

Conclusion

With the Quartus II incremental compilation feature described in this chapter, you can preserve the results and the performance of unchanged logic in your design as you make changes elsewhere. The various applications of incremental compilation enable you to improve your productivity while designing for high-density FPGAs , using either top-down or bottom-up design methodologies. Using the techniques and recommendations presented in this chapter allows you to make good design decisions to achieve timing closure while reducing design iteration time by an average of about 60%.

2. Quartus II Design Flow for MAX+PLUS II Users

QII60002-6.0.0

Introduction

The feature-rich Quartus® II software helps you shorten your design cycles and reduce time-to-market. With FLEX®, ACEX®, APEX™, Stratix® II, Stratix GX, Stratix, Cyclone™ II, Cyclone™, MAX®, and MAX II family support, the Quartus II software is the most widely accepted Altera® design software tool today.

This chapter describes how to convert MAX+PLUS® II designs to Quartus II projects, as well as the similarities and differences between the MAX+PLUS II and Quartus II design flows. This discussion includes supported device families, graphical user interface (GUI) comparisons, and the advantages of the Quartus II software.

There are many features in the Quartus II software to help MAX+PLUS II users easily transition to the Quartus II software design environment. These include a customizable **Look & Feel** feature, which changes the GUI to display menus, toolbars, and utility windows as they appear in the MAX+PLUS II software without sacrificing Quartus II software functionality.

Chapter Overview

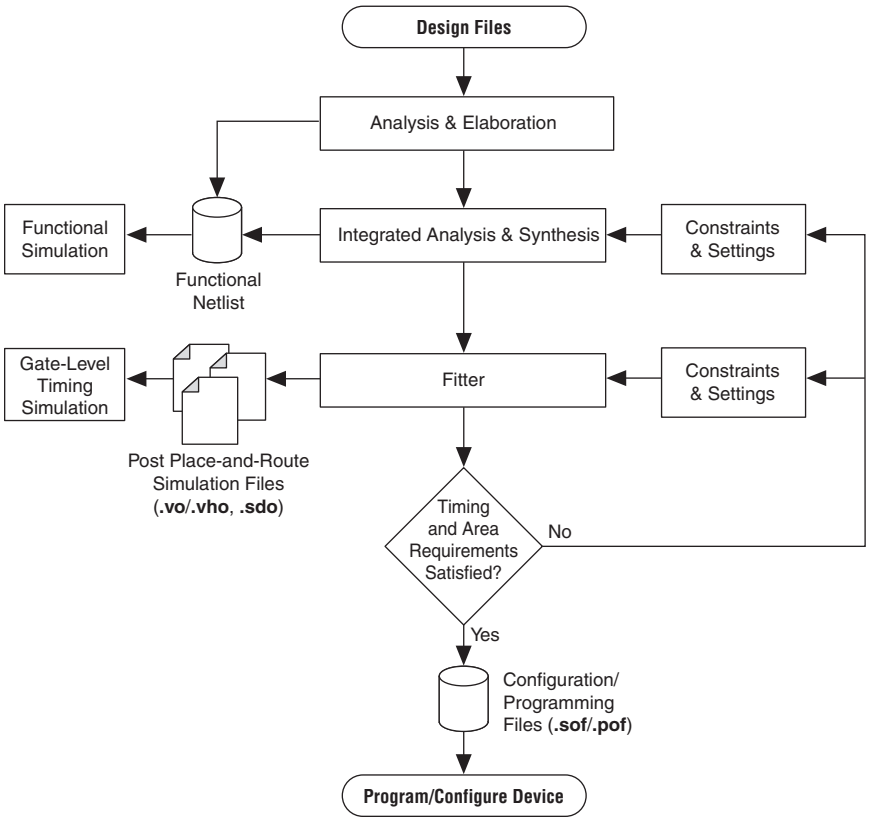
This chapter covers the following topics:

- Typical Design Flow
- Device Support
- Quartus II GUI Overview
- Setting Up MAX+PLUS II Look & Feel in Quartus II
- Compiler Tool
- Quartus II Design Flow
- Quick Menu Reference

Typical Design Flow

Figure 2–1 shows a typical design flow with the Quartus II software.

Figure 2–1. Quartus II Software Design Flow



Device Support

The Quartus II software supports most of the devices supported in the MAX+PLUS II software, but it does not support any obsolete devices or packages. The devices supported by these two software packages are shown in Table 2–1.

Table 2–1. Device Support Comparison

Device Supported	Quartus II	MAX+PLUS II
MAX II	✓	—
Classic™	—	✓
MAX 3000A	✓	✓
MAX 7000S/AE/B	✓	✓
MAX 7000E	—	✓
MAX 9000	—	✓
ACEX® 1K	✓	✓
FLEX® 6000	✓	✓
FLEX 8000	—	✓
FLEX 10K	✓ *(1)*	✓
FLEX 10KA	✓	✓
FLEX 10KE	✓ *(2)*	✓
Mercury™	✓	—
APEX™ 20K/ APEX II	✓	—
Stratix	✓	—
Stratix GX	✓	—
Stratix II	✓	—
Cyclone™	✓	—
Cyclone II	✓	—
Hardcopy® Series	✓	—

Notes to Table 2–1:

(1) PGA packages (represented as package type G in the ordering code) are not supported in the Quartus II software.

(2) Some packages are not supported.

Quartus II GUI Overview

The Quartus II software provides the following utility windows to assist in the development of your designs:

- Project Navigator
- Node Finder
- Tcl Console
- Messages
- Status
- Change Manager

Project Navigator

The **Hierarchy** tab of the Project Navigator window is similar to the MAX+PLUS II Hierarchy Display and provides additional information such as logic cell, register, and memory bit resource utilization. The **Files** and **Design Units** tabs of the Project Navigator window provide a list of project files and design units.

Node Finder

The Node Finder window provides the equivalent functionality of the MAX+PLUS II **Search Node Database** dialog box and allows you to find and use any node name stored in the project database.

Tcl Console

The Tcl Console window allows access to the Quartus II Tcl shell from within the GUI. You can use the Tcl Console window to enter Tcl commands and source Tcl scripts to make assignments, perform customized timing analysis, view information about devices, or fully automate and customize the way you run all components of the Quartus II software. There is no equivalent functionality in the MAX+PLUS II software.

For more information on using Tcl with the Quartus II software, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Messages

The Messages window is similar to the Message Processor window in the MAX+PLUS II software, providing detailed information, warnings, and error messages.You also can use it to locate a node from a message to various windows in the Quartus II software.

Status

The Status window displays information similar to the MAX+PLUS II Compiler window. Progress and elapsed time are shown for each stage of the compilation.

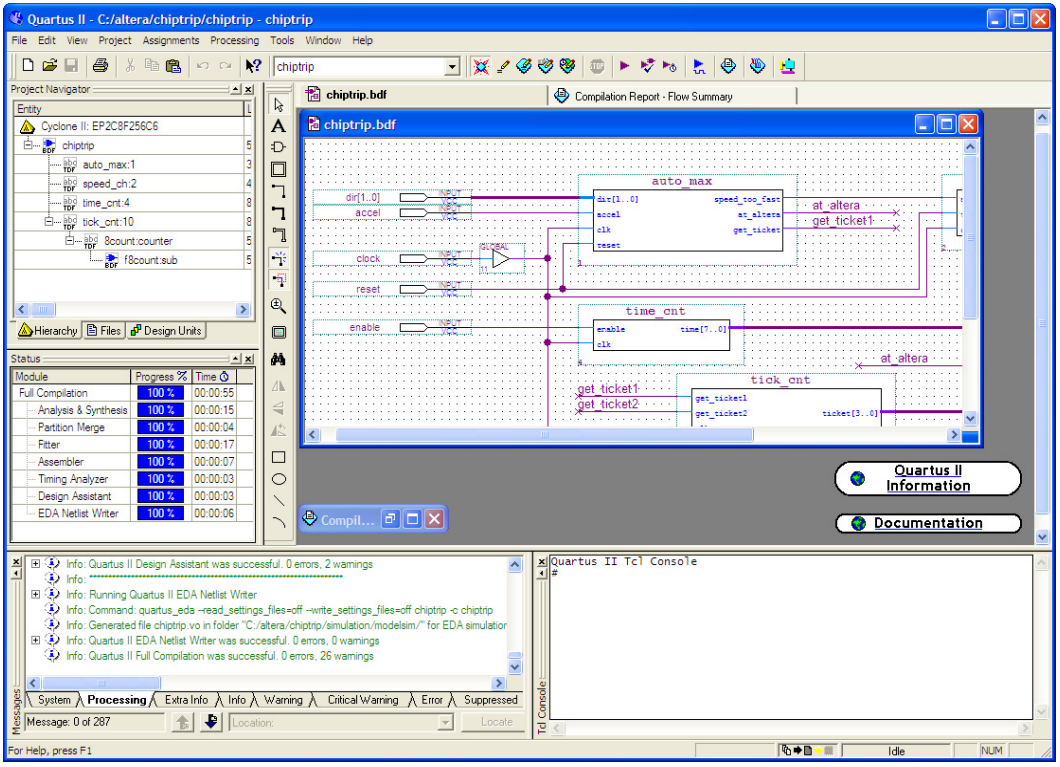
Change Manager

The Change Manager provides detailed tracking information on all design changes made with the Chip Editor.

For more information about the Engineering Change Manager and the Chip Editor, refer to the *Design Analysis & Engineering Change Management with Chip Editor* chapter in volume 3 of the *Quartus II Handbook*.

Figure 2–2 shows a typical Quartus II software display.

Figure 2–2. Quartus II Look & Feel



Setting Up MAX+PLUS II Look & Feel in Quartus II

You can choose the MAX+PLUS II look and feel by selecting MAX+PLUS II in the **Look & Feel** box of the **General** tab of the **Customize** dialog box on the Tools menu.

Any changes to the look and feel do not become effective until you restart the Quartus II software.

By default, when you select the MAX+PLUS II look and feel, the **MAX+PLUS II** quick menu (Figure 2–21 on page 2–35) appears on the left side of the menu bar. You can turn the Quartus II and MAX+PLUS II quick menus on or off. You also can change the preferred positions of the two quick menus. To change these options, perform the following steps:

1. On the Tools menu, click **Customize**. The **Customize** dialog box is shown.
2. Click the **General** tab.
3. Under **Quick menus**, select your preferred options.

MAX+PLUS II Look & Feel

The MAX+PLUS II look and feel in the Quartus II software closely resembles the MAX+PLUS II software. Figures 2–3 and 2–4 compare the MAX+PLUS II software appearance with the Quartus II MAX+PLUS II look and feel.

Figure 2–3. MAX+PLUS II Software GUI

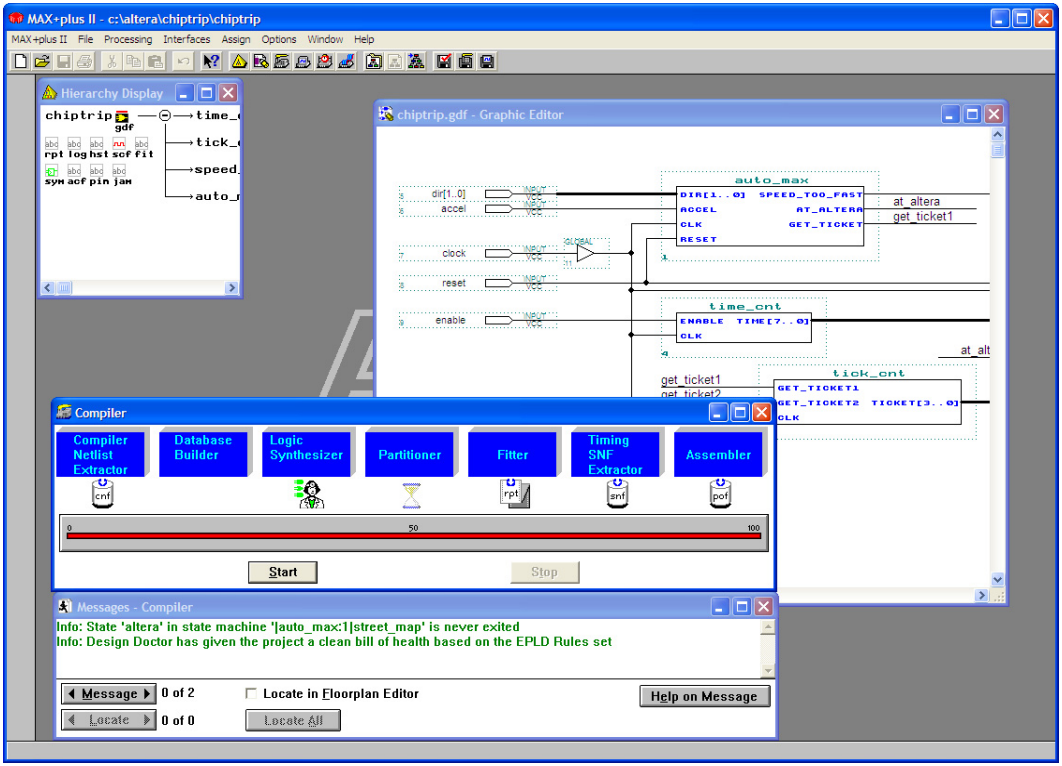
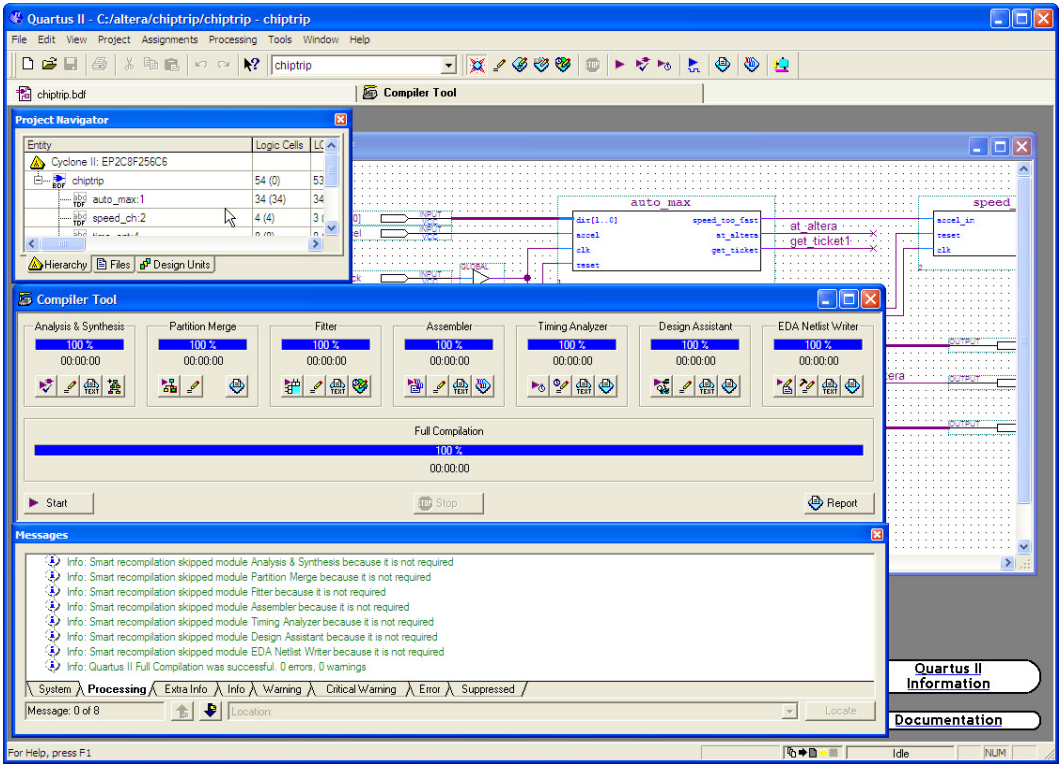


Figure 2–4. Quartus II Software with MAX+PLUS II Look & Feel



The standard MAX+PLUS II toolbar is also available in the Quartus II software with the MAX+PLUS II look and feel in the Quartus II software (Figure 2–5).

Figure 2–5. Standard MAX+PLUS II Toolbar

Compiler Tool

The Quartus II Compiler Tool provides an intuitive MAX+PLUS II style interface. You can edit the settings and view result files for the following modules:

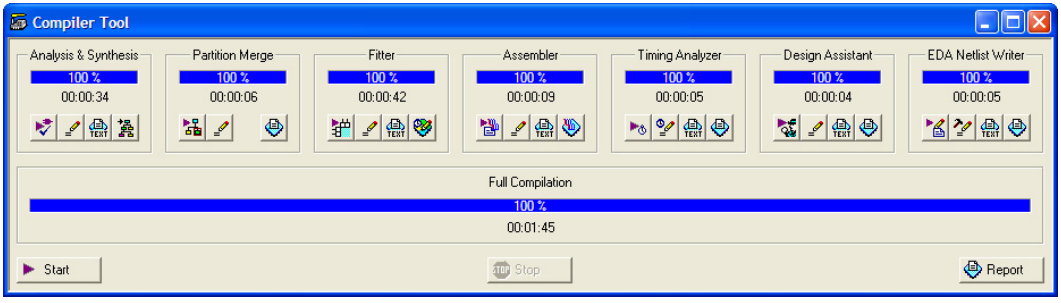
- Analysis & Synthesis
- Partition Merge
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer
- Design Assistant

Each of these modules is described later in this section.

To start a compilation using the Compiler Tool, click **Compiler Tool** from either the MAX+PLUS II menu or the Tools menu and click **Start** in the Compiler Tool. The Compiler Tool, shown in Figure 2–6, displays all modules, including optional modules such as Partition Merge, Assembler, EDA Netlist Writer, and the Design Assistant.

For information about using the Quartus II software modules at the command line, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Figure 2–6. Running a Full Compilation with the Compiler Tool



Analysis & Synthesis

The Quartus II Analysis & Synthesis module analyzes your design, builds the design database, optimizes the design for the targeted architecture, and maps the technology to the design logic.

In MAX+PLUS II software, these functions are performed by the Compiler Netlist Extractor, Database Builder, and Logic Synthesizer. There is no module in the Quartus II software similar to the MAX+PLUS II Partitioner module.

Partition Merge

The optional Quartus II Partition Merge module merges the partitions to create a flattened netlist for further stages of the Quartus II compilation flow. The Partition Merge module is not similar to the MAX+PLUS II Partitioner. This tool is available only if you turn on incremental compilation. You can turn on incremental compilation by performing the following steps:

1. On the Assignment menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, click the **+** icon to expand **Compilation Process Settings**, and select **Incremental Compilation**. The **Full Incremental Compilation** page appears.
3. Under **Incremental compilation**, turn on Incremental Compilation.

Fitter

The Quartus II Fitter module uses the PowerFit™ fitter to fit your design into the available resources of the targeted device. The Fitter places and routes the design. The Fitter module is similar to the Fitter stage of the MAX+PLUS II software.

Assembler

The optional Quartus II Assembler module creates a device programming image of your design so that you can configure your device. You can select from the following types of programming images:

- Programmer Object File (**.pof**)
- SRAM Output File (**.sof)**
- Hexadecimal (Intel-Format) Output File (**.hexout**)
- Tabular Text File (**.ttf)**
- Raw Binary File (**.rbf**)
- Jam™ STAPL Byte Code 2.0 File (**.jbc)**
- JEDEC STAPL Format File (**.jam**)

You can turn off the Assembler module during compilation by turning off **Run assembler** in the **Compilation Process Settings** page in the **Settings** dialog box. You also can turn off the Assembler by right-clicking in the Compiler Tool window. The Assembler module is similar to the Assembler stage of the MAX+PLUS II software.

Timing Analyzer

The Quartus II Timing Analyzer allows you to analyze more complex clocking schemes than is possible with the MAX+PLUS II Timing Analyzer. The Quartus II Timing Analyzer analyzes all clock domains in your design, including paths that cross clock domains, and also reports both f_{MAX} and slack. Slack is the margin by which the timing requirement is met or is not met. For more information on the Timing Analyzer, refer to "Timing Analysis" on page 2–27.

EDA Netlist Writer

The optional Quartus II EDA Netlist Writer module generates a netlist for simulation with an EDA simulation tool. The EDA Netlist Writer module is comparable to the VHDL and Verilog Netlist Writer in the MAX+PLUS II software.

Design Assistant

The optional Quartus II Design Assistant module checks the reliability of your design based on a set of design rules. The Design Assistant analyzes and generates messages for a design targeting any Altera device and is especially useful for checking the reliability of a design to be converted to HardCopy series devices. The Design Assistant is similar to the Design Doctor in the MAX+PLUS II software.

In the Quartus II software, you can reduce subsequent compilation time significantly by turning **Use Smart compilation** on before compiling your design. The Smart Compilation feature skips any compilation stages which are not required and which may use more disk space. This Quartus II smart compilation option is similar to the MAX+PLUS II **Smart Recompile** command. To turn the **Use Smart compilation** option on, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Compilation Process Settings**. The **Compilation Process Settings** page appears.
3. Turn on **Use Smart compilation**.

MAX+PLUS II Design Conversion

With the Quartus II software, you can open MAX+PLUS II designs and convert MAX+PLUS II assignments and files.

The Quartus II software is project based. All the files for your design (HDL input, simulation vectors, assignments, and other relevant files) are associated with a project file. For more information about creating a new project, refer to "Creating a New Project" on page 2–16.

Converting an Existing MAX+PLUS II Design

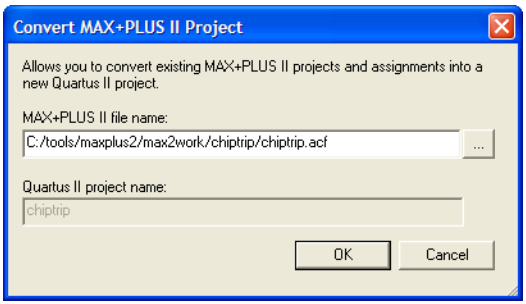
You can easily convert an existing MAX+PLUS II design for use with the Quartus II software with the **Convert MAX+PLUS II Project** command in the Quartus II software or the **Open Project** command. You can find these commands on the File menu

If you use the **Convert MAX+PLUS II Project** command, browse to the MAX+PLUS II Assignments and Configuration File (**.acf**) or top-level design file (Figure 2–7) and click **Open**. The **Convert MAX+PLUS II Project** command generates a Quartus II Project File (**.qpf**) and a Quartus II Settings File (**.qsf**). The Quartus II software stores project and design assignments in the Quartus II Settings File, which is equivalent to the Assignments and Configuration File in the MAX+PLUS II software.

You also can open and convert a MAX+PLUS II design with the **Open Project** command. In the **Open Project** dialog box, browse to the Assignments and Configuration File or the top-level design file. Click **Open** to display the **Convert MAX+PLUS II Project** dialog box.

The Quartus II software can import all MAX+PLUS II-generated files, but it cannot save files in the MAX+PLUS II format. You cannot open a Quartus II project in the MAX+PLUS II software, nor can you convert a Quartus II project to a MAX+PLUS II project.

Figure 2–7. Convert MAX+PLUS II Project Dialog Box



The conversion process performs the following actions:

- Converts the MAX+PLUS II Assignments and Configuration File into a Quartus II Settings File (equivalent to importing all MAX+PLUS II assignments)
- Creates a Quartus II Project File
- Displays all errors and warnings in the Quartus II message window

The Quartus II software can read MAX+PLUS II generated Graphic Design Files (**.gdf**) and Simulation Channel Files (**.scf**) without converting them. These files are not modified during a MAX+PLUS II design conversion.

Converting MAX+PLUS II Graphic Design Files

The Quartus II Block Editor (similar to the MAX+PLUS II Graphic Editor) saves files as Block Design Files (**.bdf**). You can convert your MAX+PLUS II Graphic Design File into a Quartus II Block Design File using one of the following methods:

1. Open the Graphic Design File and on the File menu, click **Save As**. The **Save As** dialog box is shown.
2. In the **Save as type** list, select **Block Diagram/Schematic File** (*.**bdf**).

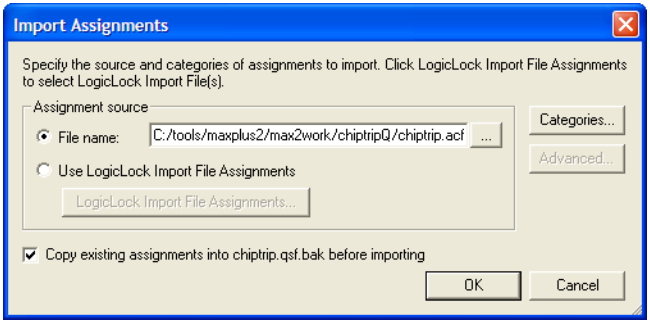
3. Run the **quartus_g2b.exe** command line executable located in the \<*Quartus II installation*>**bin** directory. For example, to convert the **chiptrip.gdf** file to a Block Design File, type the following command at a command prompt:

```
quartus_g2b.exe chip_trip.gdf ↵
```

Importing MAX+PLUS II Assignments

You can import MAX+PLUS II assignments into an existing Quartus II project. Open the project, and on the Assignments menu, click **Import Assignments**. Browse to the Assignments and Configuration File (Figure 2–8). You can also import Quartus II Settings Files and Entity Setting Files (**.esf**).

Figure 2–8. Import Assignments Dialog Box



The Quartus II software accepts most MAX+PLUS II assignments. However, some assignments can be imported incorrectly from the MAX+ PLUS II software into the Quartus II software due to differences in node naming conventions and the advanced Quartus II integrated synthesis algorithms.

The differing node naming conventions in the Quartus II and MAX+PLUS II software can cause improper mapping when importing your design from MAX+PLUS II software into the Quartus II software. Improper node names can interfere with the design logic if you are unaware of these node name differences and do not take appropriate

steps to prevent improper node name mapping. Table 2–2 compares the differences between the naming conventions used by the Quartus II and MAX+PLUS II software.

Table 2–2. Quartus II & MAX+PLUS II Node & Pin Naming Conventions

Feature	Quartus II Format	MAX+PLUS II Format
Node name	`auto_max:auto|q0`	`|auto_max:auto|q0`
Pin name	`d[0], d[1], d[2]`	`d0, d1, d2`

When you import MAX+PLUS II assignments containing node names that use numbers, such as `signal0` or `signal1`, the Quartus II software imports the original assignment and also creates an additional copy of the assignment. The additional assignment has square brackets inserted around the number, resulting in `signal[0]` or `signal[1]`. The square bracket format is legal for signals that are part of a bus, but creates illegal signal names for signals that are not part of a bus in the Quartus II software. If your MAX+PLUS II design contains node names that end in a number and are not part of a bus, you can edit the Quartus II Settings File to remove the square brackets from the node names after importing them.

You can remove obsolete assignments in the **Remove Assignments** dialog box. Open this dialog box on the Assignments menu by clicking **Remove Assignments**.

The Quartus II software may not recognize valid MAX+PLUS II node names, or may split MAX+PLUS II nodes into two different nodes. As a result, any assignments made to synthesized nodes are not recognized during compilation.

For more information about Quartus II node naming conventions, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

Quartus II Design Flow

The following sections include information to help you get started using the Quartus II software. They describe the similarities and differences between the Quartus II software and the MAX+PLUS II software. The following sections highlight improvements and benefits in the Quartus II software.

Creating a New Project

The Quartus II software provides a wizard to help you create new projects. On the File menu, click **New Project Wizard** to start the New Project Wizard. The New Project Wizard generates the Quartus II Project File and Quartus II Settings File for your project.

Design Entry

The Quartus II software supports the following design entry methods:

- Altera HDL (AHDL) Text Design File (**.tdf**)
- Block Diagram File
- EDIF Netlist File (**.edf**)
- Verilog Quartus Mapping Netlist File (**.vqm**)
- VHDL (**.vhd**)
- Verilog HDL (**.v**)

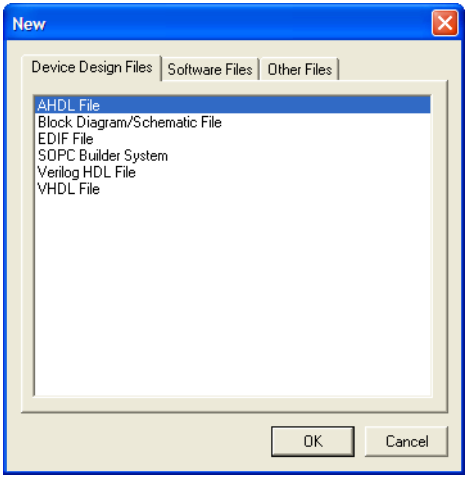
The Quartus II software has an advanced integrated synthesis engine that fully supports the Verilog HDL and VHDL languages and provides options to control the synthesis process.

For more information, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

To create a new design file, perform the following steps:

1. On the File menu, click **New**. The **New** dialog box appears.
2. Click the **Device Design Files** tab.
3. Select a design entry type.
4. Click **OK** (see Figure 2–9).

Figure 2–9. New Dialog Box

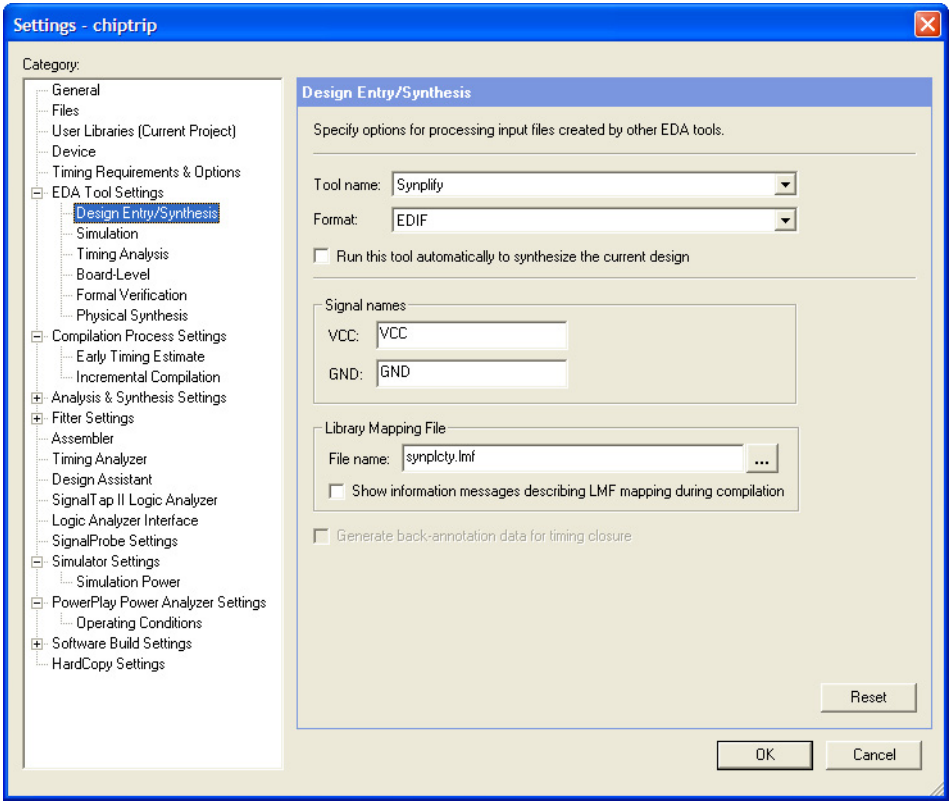


You can create other files from the **Software Files** tab and **Other Files** tab of the **New** dialog box on the File menu. For example, the Vector Waveform File (**.vwf**) is located in the **Other Files** tab.

To analyze a netlist file created by an EDA tool, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Design Entry & Synthesis**. The **Design Entry & Synthesis** page appears.
3. In the **Tool** name list, select the synthesis tool used to generate the netlist (Figure 2–10).

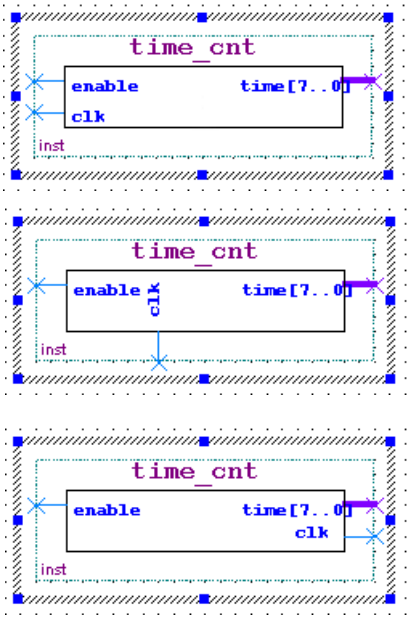
Figure 2–10. Settings Dialog Box Specifying Design Entry Tool



The Quartus II Block Editor has many advantages over the MAX+PLUS II Graphic Editor. The Block Editor offers an unlimited sheet size, multiple region selections, an enhanced Symbol Editor, and conduits.

The Symbol Editor allows you to change the positions of the ports in a symbol (refer to the three images in Figure 2–11). You can reduce wire congestion around a symbol by changing the positions of the ports.

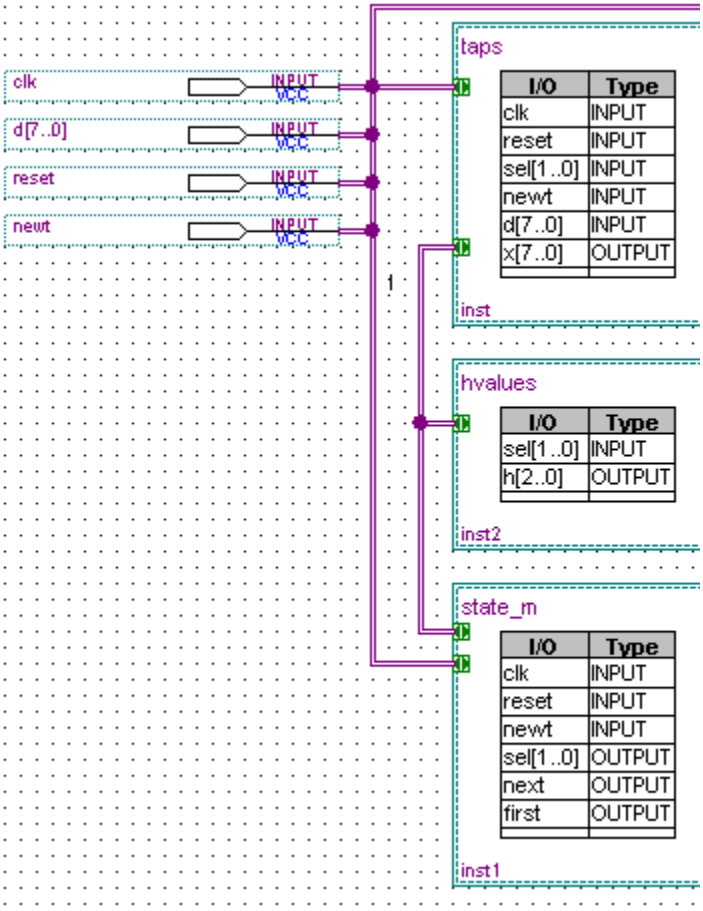
Figure 2–11. Various Port Position for a Symbol



To make changes to a symbol in a Block Design File, right-click a symbol in the Block Editor and select **Properties** to display the **Symbol Properties** dialog box. This dialog box allows you to change the instance name, add parameters, and specify the line and text color.

You can use conduits to connect blocks (including pins) in the Block Editor. Conduits contain signals for the connected objects (see Figure 2–12). You can determine the connections between various blocks in the **Conduit Properties** dialog box by right-clicking a conduit and clicking **Properties**.

Figure 2–12. Blocks & Pins Connected with Conduits



Making Assignments

The Quartus II software stores all project and design assignments in a Quartus II Settings File, which is a collection of assignments stored as Tcl commands and organized by the compilation stage and assignment type. The Quartus II Settings File stores all assignments, regardless of how they are made, from the Floorplan Editor, the Pin Planner, the Assignment Editor, with Tcl, or any other method.

Assignment Editor

The Assignment Editor is an intuitive spreadsheet interface designed to allow you to make, change, and manage a large number of assignments easily. With the Assignment Editor, you can list all available pin numbers and design pin names for efficiently creating pin assignments. You also can filter all assignments based on assignment categories and node names for viewing and creating assignments.

The Assignment Editor is composed of the Category Bar, Node Filter Bar, Information Bar, Edit Bar, and spreadsheet.

To make an assignment, follow these steps:

1. On the Assignments menu, click **Assignment Editor**. The **Assignment Editor** window appears.
2. Select an assignment category in the **Category** bar.
3. Select a node name using the Node Finder or type a node name filter into the **Node Filter** bar. (This step is optional; it excludes all assignments unrelated to the node name.)
4. Type the required values into the spreadsheet.
5. On the File menu, click **Save**.

If you are unsure about the purpose of a cell in the spreadsheet, select the cell and read the description displayed in the **Information** bar.

You can use the **Edit** bar to change the contents of multiple selected cells simultaneously. Select cells in the spreadsheet and type the value in the **Edit** box.

Other advantages of the Assignment Editor include clipboard support in the spreadsheet and automatic font coloring to identify the status of assignments.

For more information, refer to the *Assignment Editor* chapter in volume 1 of the *Quartus II Handbook.*

Timing Assignments

You can use the timing wizard to help you set your timing requirements. On the Assignments menu, click **Timing Wizard** to create global clock and timing settings. The settings include f_{MAX}, setup times, hold times, clock to output delay times, and individual absolute or derived clocks.

You also can set timing settings manually by performing the following steps:

1. On the Assignments menu, click **Settings**. The **Setting** dialog box is shown.
2. In the **Category** list, select **Timing Requirements & Options**. The **Timing Requirements & Options** page is shown.
3. Set your timing settings.

You can make more complex timing assignments with the Quartus II software than allowed by the MAX+PLUS II software, including multicycle and point-to-point assignments using wildcards and time groups.

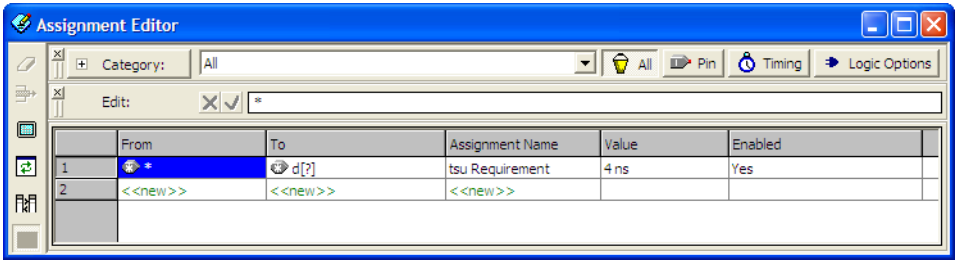
A time group is a collection of design nodes grouped together and represented as a single unit for the purpose of making timing assignments to the collection.

Multicycle timing assignments allow you to identify register-to-register paths in the design where you expect a delayed latch edge. This assignment enables accurate timing analysis of your design.

Point-to-point timing assignments allow you to specify the required delay between two pins, two registers, or a pin and a register. This assignment helps you optimize and verify your design timing requirements.

Wildcard characters "?" and " * " allow you to apply an assignment to a large number of nodes with just a few assignments. For example, Figure 2–13 shows a 4 ns t_{SU} requirement assignment to all paths from any node to the "d" bus in the Assignment Editor.

Figure 2–13. Single t_{SU} Timing Assignment Applied to All Nodes of a Bus



For more information, refer to the *Classic Timing Analyzer* or the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Synthesis

The Quartus II advanced integrated synthesis software fully supports the hardware description languages, Verilog HDL, VHDL, and AHDL, schematic entry, and also provides options to control the synthesis process. With this synthesis support, the Quartus II software provides a complete, easy-to-use, stand-alone solution for today's designs.

You can specify synthesis options in the **Analysis & Synthesis Settings** page of the **Settings** dialog box. Similar to MAX+PLUS II synthesis options, you select one of these optimization techniques: **Speed, Area,** or **Balanced**.

To achieve higher design performance, you can turn on synthesis netlist optimizations that are available when targeting certain devices. You can unmap a netlist created by an EDA tool and remap the components in the netlist back to Altera primitives by turning on **Perform WYSIWYG primitive resynthesis**. Additionally, you can move registers across combinational logic to balance timing without changing design functionality by turning on **Perform gate-level register retiming**. Both of these options are accessible from the **Synthesis Netlist Optimizations** page under **Analysis & Synthesis Settings** in the **Settings** dialog box on the Assignments menu.

For more information, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

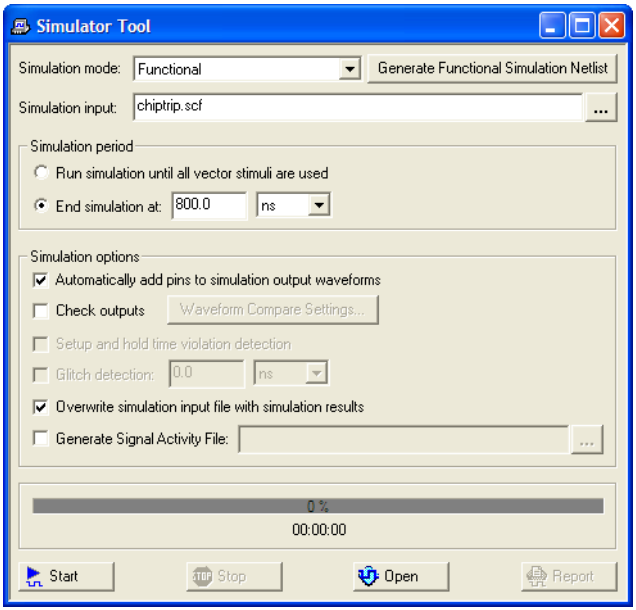
Functional Simulation

Similar to the MAX+PLUS II Simulator, the Quartus II Simulator Tool performs both functional and timing simulations.

To open the Simulator Tool, on MAX+PLUS II menu, click **Simulator** or on the Tools menu, click **Simulator Tool**. Before you perform a functional simulation, an internal functional simulation netlist is required. Click **Generate Functional Simulation Netlist** in the **Simulator Tool** window (Figure 2–14), or on the Processing menu, click **Generate Functional Simulation Netlist**.

Generating a functional simulation netlist creates a separate database that improves the performance of the simulation significantly.

Figure 2–14. Simulator Tool Dialog Box



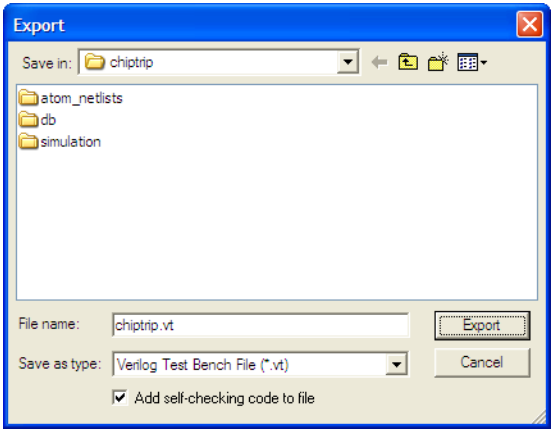
You can view and modify the simulator options on the **Simulator** page of the **Settings** dialog box or in the **Simulator Tool** window. You can set the simulation period and turn **Check outputs** on or off. You can choose to display the simulation outputs in the simulation report or in the Vector Waveform File. To display the simulation results in the simulation input vector waveform file, which is the MAX+PLUS II behavior, turn on **Overwrite simulation input file with simulation results**.

When using either the MAX+PLUS II or Quartus II software, you may have to compile additional behavioral models to perform a simulation with an EDA simulation tool. In the Quartus II software, behavioral models for library of parameterized modules (LPM) functions and Altera-specific megafunctions are available in the **altera_mf** and **220model** library files, respectively. The **220model** and **altera_mf** files can be found in the \<*Quartus II Installation*>**eda\sim_lib** directory.

The Quartus II schematic design files (Block Design File, or **.bdf**) are not compatible with EDA simulation tools. To perform a register transfer level (RTL) functional simulation of a Block Design File using an EDA tool, convert your schematic designs to a VHDL or Verilog HDL design file. Open the schematic design file and on the File menu, click **Create/Update > Create HDL Design File for Current File** to create an HDL design file that corresponds to your Block Design File.

You can export a Vector Waveform File or Simulator Channel File as a Verilog HDL or VHDL test bench file for simulation with an EDA tool. Open your Vector Waveform File or Simulator Channel File and on the File menu, click **Export**. See Figure 2–15. Select **Verilog** or **VHDL Test Bench File (*.vt)** from the **Save as type** list. Turn on **Add self-checking code to file** to add additional self-checking code to the test bench.

Figure 2–15. Export Dialog Box



Place & Route

The Quartus II PowerFit is an incremental fitter that performs place-and-route to fit your design into the targeted device. You can control the Fitter behavior with options in the **Fitter Settings** page of the **Settings** dialog box on the Assignments menu.

High-density device families supported in the Quartus II software, such as the Stratix series, sometimes require significant fitter effort to achieve an optimal fit. The Quartus II software offers several options to reduce the time required to fit a design. You can control the effort the Quartus II Fitter expends to achieve your timing requirements with these options:

- **Optimize timing** performs timing-based placement using the timing requirements you specify for the design. You can use this option by itself or with one or more of the options below.
- **Optimize hold timing** optimizes the hold times within a device to meet timing requirements and assignments you specify. You can select this option only if the Optimize timing option is also chosen.
- **Optimize fast-corner timing** instructs the Fitter, when optimizing your design, to consider fast-corner delays, in addition to slow-corner delays, from the fast-corner timing model (fastest manufactured device, operating in low-temperature and high-voltage conditions). You can select this option only if the **Optimize timing** option is also chosen.

If minimizing compilation time is more important than achieving specific timing results, you can turn these options off.

Another way to decrease the processing time and effort the Fitter expends to fit your design is to select either **Standard Fit** or **Fast Fit** in the **Fitter Effort** box of the **Fitter Settings** page in the **Settings** dialog box on the Assignments menu. The option you select affects the Fitter behavior and your design as described below.

- Select **Standard Fit** for the Fitter to use the highest effort and preserve the performance from previous compilations.
- Select **Fast Fit** for up to 50% faster compilation times, although this may reduce design performance.

You can also select **Auto Fit** to decrease compilation time by directing the Fitter to reduce Fitter effort after meeting your timing requirements. The **Auto Fit** option is available for select devices.

For more information, refer to the *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

To further reduce compilation times, turn on **Limit to one fitting attempt** in the **Fitter Settings** page in the **Settings** dialog box on the Assignments menu.

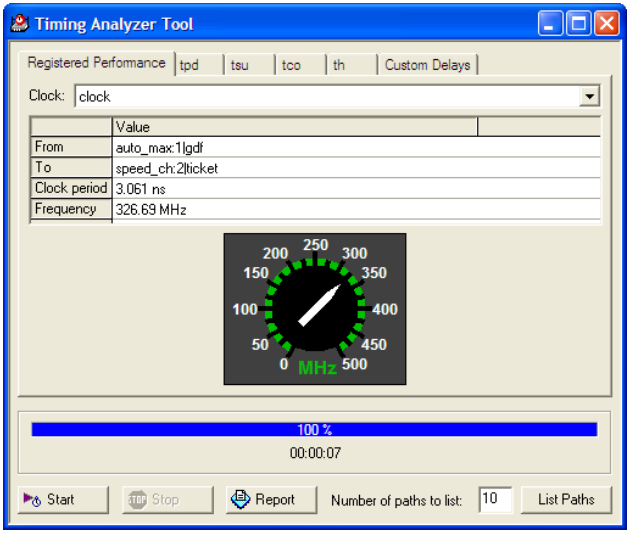
If your design is very close to meeting your timing requirements, you can control the seed number used in the fitting algorithm by changing the value in the **Seed** box of the **Fitter Settings** page of the **Settings** dialog box on the Assignments menu. The default seed value is 1. You can specify any non-negative integer value. Changing the value of the seed only repositions the starting location of the Fitter, but does not affect compilation time or the Fitter effort level. However, if your design is difficult to fit optimally or takes a long time to fit, sometimes you can improve results or processing time by changing the seed value.

Timing Analysis

You can use the Quartus II Timing Analyzer to analyze more complex clocking schemes than is possible with the MAX+PLUS II Timing Analyzer.

Launch the Timing Analyzer Tool on the MAX+PLUS II menu by clicking **Timing Analyzer** or on the Tools menu by clicking **Timing Analyzer Tool**. See Figure 2–16. To start the analysis, click **Start** in the Timing Analyzer Tool or on the Processing menu, by pointing to Start, and clicking **Start Timing Analyzer**.

Figure 2–16. Registered Performance Tab of the Timing Analyzer Tool



The Quartus II Timing Analyzer analyzes all clock domains in your design, including paths that cross clock domains. You can ignore paths that cross clock domains by using the following options in the **Timing Requirements & Options** page in the **Settings** dialog box on the Assignments menu:

- Create a **Cut Timing Path** assignment
- Turn on **Cut paths between unrelated clock domains**

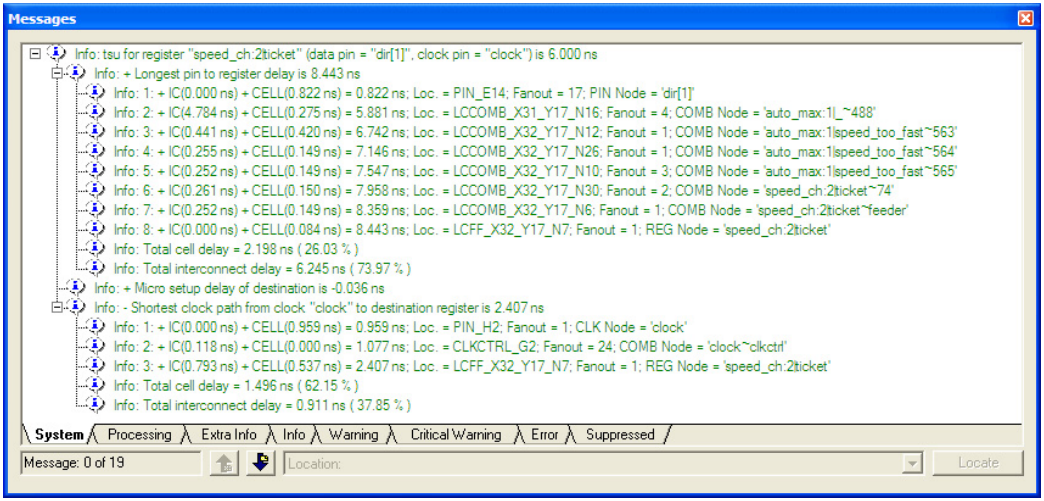
To view the results from the Timing Analyzer Tool, you can click on the **Report**, or to get specific information, click on any of the following tabs at the top of the Timing Analyzer window:

- Registered Performance
- t_{PD}
- t_{SU}
- t_{CO}
- t_{H}
- Custom Delays

The Quartus II Timing Analyzer reports both f_{MAX} and slack. Slack is the margin by which the timing requirement was met or not met. A positive slack value, displayed in black, indicates the margin by which a requirement was met. A negative slack value, displayed in red, indicates the margin by which a requirement was not met.

To analyze a particular path in more detail, select a path in the Timing Analyzer Tool and click **List Paths**. This displays a detailed description of the path in the **System** tab of the **Messages** window (Figure 2–17).

Figure 2–17. Messages Window Displaying Detailed Timing Information



For more information, refer to the *Classic Timing Analyzer* or the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Timing Closure Floorplan

The Quartus II Timing Closure Floorplan is similar to the MAX+PLUS II Floorplan Editor but has many improvements to help you more effectively view and debug your design. With its ability to display logic cell usage, routing congestion, critical paths, and LogicLock™ regions, the Timing Closure Floorplan also makes the task of improving your design performance much easier.

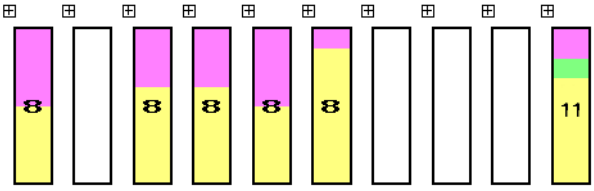
To view the Timing Closure Floorplan, on the MAX+PLUS II menu, click **Floorplan Editor** or **Timing Closure Floorplan**.

The Timing Closure Floorplan Editor provides Interior Cell views equivalent to the MAX+PLUS II logic array block (LAB) views. In addition to these views, available from the View menu, you also can select from the Interior MegaLABs (where applicable), Interior LABs, and Field views.

The Pin Planner is equivalent to the MAX+PLUS II Device view. The Pin Planner can be launched from the Timing Closure Floorplan Editor by selecting **Package** (Top or Bottom) from the View menu or on the Assignments menu by clicking **Pin Planner**.

The Interior LABs view hides cell details for logic cells, Adaptive Logic Modules (ALM), and macrocells, and shows LAB information (see Figure 2–18). You can display the number of cells used in each LAB on the View menu by clicking **Show Usage Numbers**.

Figure 2–18. Interior LAB View of the Timing Closure Floorplan



The Field view is a color-coded, high-level view of your device resources that hides both cell and LAB details. In the Field view, you can see critical paths and routing congestion in your design.

The View Critical Paths feature shows a percentage of all critical paths in your floorplan. You can enable this feature on the View menu by clicking **Show Critical Paths**. You can control the number of critical paths shown by modifying the settings in the **Critical Paths Settings** dialog box on the View menu.

The View Congestion feature displays routing congestion by coloring and shading logic resources. Darker shading shows greater resource utilization. This feature assists in identifying locations where there is a lack of routing resources.

To show lower level details in any view, right-click on a resource and click **Show Details**.

For more information, refer to the *Timing Closure Floorplan* chapter in volume 2 of the *Quartus II Handbook*.

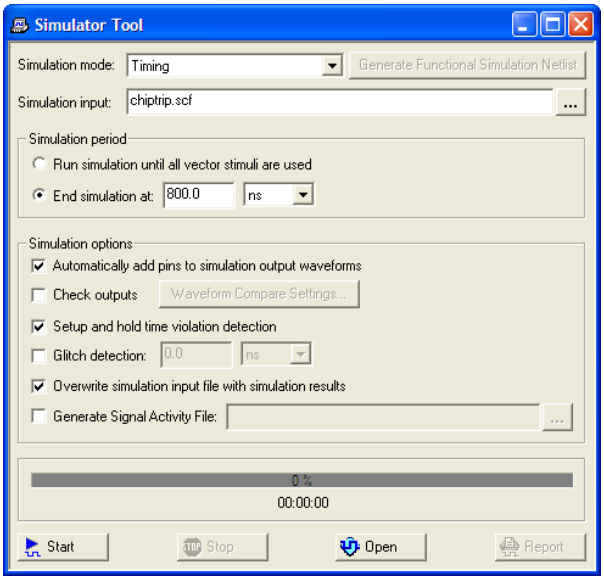
Timing Simulation

Timing simulation is an important part of the verification process. The Quartus II software supports native timing simulation and exports simulation netlists to third-party software for design verification.

Quartus II Simulator Tool

The Quartus II Simulator tool is an easy-to-use integrated solution that uses the compiler database to simulate the logical and timing performance of your design (Figure 2–19). When performing timing simulation, the simulator uses place-and-route timing information.

Figure 2–19. Quartus II Simulator Tool



You can use Vector Table Output Files (**.tbl**), Vector Waveform Files, Vector Files (**.vec**), or an existing Simulator Channel File as the vector stimuli for your simulation.

The simulation options available are similar to the options available in the MAX+PLUS II Simulator. You can control the length of the simulation and the type of checks performed by the Simulator. When the MAX+PLUS II look and feel is selected, the **Overwrite simulation input file with simulation results** option is on by default. If you turn it off, the simulation results are written to the report file. To view the report file, click **Report** in the Simulator Tool window.

EDA Timing Simulation

The Quartus II software also supports timing simulation with other EDA simulation software. Performing timing simulation with other EDA simulation software requires a Quartus II generated timing netlist file in the form of a Verilog Output File (**.vo**) or VHDL Output File (**.vho**), a Standard Delay Format Output File (**.sdo**), and a device-specific atom file (or files), shown in Table 2–3.

Table 2–3. Altera Timing Simulation Library Files

Verilog	VHDL
<*device_family*>_atoms.v	<*device_family*>_atoms_87.vhd
	<*device_family*>_atoms.vhd
	<*device_family*>_components.vhd

Specify your EDA simulation tool by performing the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page appears.
3. In the **Tool name list**, select your EDA Tool.

You can generate a timing netlist for the selected EDA simulator tool by running a full compile or on the Processing menu, by pointing to Start and clicking **Start EDA Netlist Writer**. The generated netlist and SDF file are placed into the \<*project directory*>**\simulation**\<*EDA simulator tool*> directory. The device-specific atom files are located in the \<*Quartus II Install*>**\eda\sim_lib** directory.

Power Estimation

To develop an appropriate power budget and to design the power supplies, voltage regulators, heat sink, and cooling system, you need an accurate estimate of the power that your design consumes. You can estimate power by using the PowerPlay Early Power Estimation spreadsheet available on the Altera Web Site at **www.altera.com**, or with the PowerPlay Power Analyzer in the Quartus II software.

You can perform early power estimation with the PowerPlay Early Power Estimation spreadsheet by entering device resource and performance information. The Quartus II PowerPlay Analyzer tool performs

vector-based power analysis by reading either a Signal Activity File (**.saf**), generated from a Quartus II simulation, or a Value Change Dump File (VCD) generated from a third-party simulation.

For more information about how to use the PowerPlay Power Analyzer tool, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Programming

The Quartus II Programmer has the same functionality as the MAX+PLUS II Programmer, including programming, verifying, examining, and blank checking operations. Additionally, the Quartus II Programmer now supports the erase capability for CPLDs. To improve usability, the Quartus II Programmer displays all programming-related information in one window (Figure 2–20).

Click **Add File** or **Add Device** in the Programmer window to add a file or device, respectively.

Figure 2–20. Programmer Window

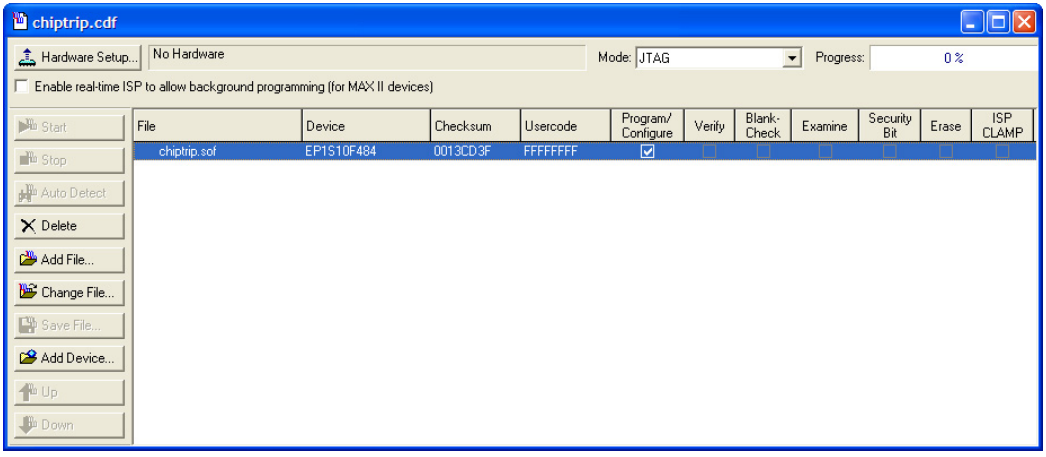


Figure 2–20 shows that the Programmer Window now supports Erase capability.

You can save the programmer settings as a Chain Description File (**.cdf**). The CDF is an ASCII text file that stores device name, device order, and programming file name information.

Conclusion

The Quartus II software is the most comprehensive design environment available for programmable logic designs. Features such as the MAX+PLUS II look and feel help you make the transition from Altera's MAX+PLUS II design software and become more productive with the Quartus II software. The Quartus II software has all the capabilities and features of the MAX+PLUS II software and many more to speed up your design cycle.

Quick Menu Reference

The commands displayed in the MAX+PLUS II Quick Menu and the Quartus II Quick Menu vary based on whichever window is active (Figures 2–21). In the following figure, the Graphic Editor window is active.

Figure 2–21. MAX+PLUS II Quick Menus in MAX+PLUS II and Quartus II Software

Quartus II Command Reference for MAX+PLUS II Users

Table 2–4 lists the commands in the MAX+PLUS II software and gives their equivalent commands in the Quartus II software.

NA means either Not Applicable or Not Available. If a command is not listed, then the command is the same in both tools.

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 1 of 10)

MAX+PLUS II Software	Quartus II Software
MAX+PLUS II Menu	
Hierarchy Display	View menu, Utility Windows, **Project Navigator**
Graphic Editor	Block Editor
Symbol Editor	Block Symbol Editor
Text Editor	Text Editor
Waveform Editor	Waveform Editor
Floorplan Editor	Assignments menu, **Timing Closure Floorplan**
Compiler	Tools menu, **Compiler Tool**
Simulator	Tools menu, **Simulator Tool**
Timing Analyzer	Tools menu, **Timing Analyzer Tool**
Programmer	Tools menu, **Programmer**
Message Processor	View menu, Utility Windows, **Messages**
File Menu	
File menu, Project, **Name** (Ctrl+J)	File menu, **Open Project** (Ctrl+J)
File menu, Project, **Set Project to Current File** (Ctrl+Shift+J)	Project menu, **Set as Top-Level Entity** (Ctrl+Shift+J) or File menu, **New Project Wizard**
File menu, Project, **Save & Check** (Ctrl+K)	Processing menu, Start, **Start Analysis & Synthesis** (Ctrl+K) *or* Processing menu, Start, **Start Analysis & Elaboration**
File menu, Project, **Save & Compile** (Ctrl+L)	Processing menu, **Start Compilation** (Ctrl+L)

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 2 of 10)

MAX+PLUS II Software	Quartus II Software
File menu, Project, **Save & Simulate** (Ctrl+Shift+L)	Processing menu, **Start Simulation** (Ctrl+I)
File menu, Project, **Compile & Simulate** (Ctrl+Shift+K)	Processing menu, **Start Compilation & Simulation** (Ctrl+Shift+K)
File menu, Project, **Archive**	Project menu, **Archive Project**
File menu, Project, <*Recent Projects*>	File menu, <*Recent Projects*>
File menu, **Delete File**	NA
File menu, **Retrieve**	NA
File menu, **Info** (Ctrl+I)	File menu, **File Properties**
File menu, **Create Default Symbol**	File menu, Create/Update, **Create Symbol Files for Current File**
File menu, **Edit Symbol**	(Block Editor) Edit menu, **Edit Selected Symbol**
File menu, **Create Default Include File**	File menu, Create/Update, **Create AHDL Include Files for Current File**
File menu, **Hierarchy Project Top** (Ctrl+T)	Project menu, Hierarchy, **Project Top** (Ctrl+T)
File menu, Hierarchy, **Up** (Ctrl+U)	Project menu, Hierarchy, **Up** (Ctrl+U)
File menu, Hierarchy, **Down** (Ctrl+D)	Project menu, Hierarchy, **Down** (Ctrl+D)
File menu, Hierarchy, **Top**	NA
File menu, Hierarchy, **Project Top** (Ctrl+T)	Project menu, Hierarchy, **Project Top** (Ctrl+T)
File menu, **MegaWizard Plug-In Manager**	Tools menu, **MegaWizard Plug-In Manager**
(Graphic Editor) File menu, **Size**	NA
(Waveform Editor) File menu, **End Time**	(Waveform Editor) Edit menu, **End Time**
(Waveform Editor) File menu, **Compare**	(Waveform Editor) View menu, **Compare to Waveforms in File**
(Waveform Editor) File menu**, Import Vector File**	File menu, **Open** (Ctrl+O)
(Waveform Editor) File menu**, Create Table File**	File menu, **Save As**
(Hierarchy Display) File menu, **Select Hierarchy**	NA
(Hierarchy Display) File menu, **Open Editor**	(Project Navigator) Double-click
(Hierarchy Display) File menu, **Close Editor**	NA
(Hierarchy Display) File menu, **Change File Type**	(Project Navigator) Select file in Files tab and select Properties on right click menu
(Hierarchy Display) File menu, **Print Selected Files**	NA

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 3 of 10)

MAX+PLUS II Software	Quartus II Software
(Programmer) File menu, **Select Programming File**	File menu, **Open**
(Programmer) File menu, **Save Programming Data As**	File menu, **Save**
(Programmer) File menu, **Inputs/Outputs**	NA
(Programmer) File menu, **Convert SRAM Object Files**	File menu, **Convert Programming Files**
(Programmer) File menu, **Archive JTAG Programming Files**	NA
(Programmer) File menu, **Create Jam or SVF File**	File menu, Create/Update, **Create JAM, SVF, or ISC File**
(Message Processor) Select Messages	NA
(Message Processor) Save Messages As	(Messages) Save Messages on right click menu
(Timing Analyzer) Save Analysis As	Processing menu, **Compilation Report** - Save Current Report on right click menu in Timing Analyzer sections
(Simulator) Create Table File	(Waveform Editor) File menu, **Save As**
(Simulator) Execute Command File	NA
(Simulator) Inputs/Outputs	NA
Edit Menu	
(Waveform Editor) Edit menu, **Overwrite**	(Waveform Editor) Edit menu, **Value**
(Waveform Editor) Edit menu, **Insert**	(Waveform Editor) Edit menu, **Insert Waveform Interval**
(Waveform Editor) Edit menu, **Align to Grid** (Ctrl+Y)	NA
(Waveform Editor) Edit menu, **Repeat**	(Waveform Editor) Edit menu, **Repeat Paste**
(Waveform Editor) Edit menu, **Grow or Shrink**	Edit menu, **Grow or Shrink** (Ctrl+Alt+G)
(Text Editor) Edit menu, **Insert Page Break**	(Text Editor) Edit menu, **Insert Page Break**
(Text Editor) Edit menu, **Increase Indent** (F2)	(Text Editor) Edit menu, **Increase Indent**
(Text Editor) Edit menu, **Decrease Indent** (F3)	(Text Editor) Edit menu, **Decrease Indent**
(Graphic Editor) Edit menu, **Toggle Connection Dot** (Double-Click)	(Block Editor) Edit menu, **Toggle Connection Dot**
(Graphic Editor) Edit menu, **Flip Horizontal**	(Block Editor) Edit menu, **Flip Horizontal**
(Graphic Editor) Edit menu, **Flip Vertical**	(Block Editor) Edit menu, **Flip Vertical**
(Graphic Editor) Edit menu, **Rotate**	(Block Editor) Edit menu, **Rotate by Degrees**

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 4 of 10)

MAX+PLUS II Software	Quartus II Software
View Menu	
 View menu, **Fit in Window** (Ctrl+W)	 View menu, **Fit in Window** (Ctrl+W)
 View menu, **Zoom In** (Ctrl+Space)	 View menu, **Zoom In** (Ctrl+Space)
 View menu, **Zoom Out** (Ctrl+Shift+Space)	 View menu, **Zoom Out** (Ctrl+Shift+Space)
View menu, **Normal Size** (Ctrl+1)	NA
View menu, **Maximum Size** (Ctrl+2)	NA
(Hierarchy Display) View menu, **Auto Fit in Window**	NA
(Waveform Editor) View menu, **Time Range**	 View menu, **Zoom**
Assign menu, **Device**	 Assignments menu, **Device** *or*  Assignments menu, **Settings** (Ctrl+Shift+E)
Assign menu, **Pin/Location/Chip**	 Assignments menu, **Assignment Editor** - Locations category
Assign menu, **Timing Requirements**	 Assignments menu, **Assignment Editor** - Timing category
Assign menu, **Clique**	 Assignments menu, **Assignment Editor** - Cliques category
Assign menu, **Logic Options**	 Assignments menu, **Assignment Editor** - Logic Options category
Assign menu, **Probe**	NA
Assign menu, **Connected Pins**	 Assignments menu, **Assignment Editor** - Simulation category
Assign menu, **Local Routing**	 Assignments menu, **Assignment Editor** - Local Routing category
Assign menu, **Global Project Device Options**	 Assignments menu, **Device** - Device & Pin Options
Assign menu, **Global Project Parameters**	 Assignments menu, **Settings** - Analysis & Synthesis - Default Parameters
Assign menu, **Global Project Timing Requirements**	 Assignments menu, **Timing Settings**
Assign menu, **Global Project Logic Synthesis**	 Assignments menu, **Settings** - Analysis & Synthesis
Assign menu, **Ignore Project Assignments**	 Assignments menu, **Assignment Editor** - disable
Assign menu, **Clear Project Assignments**	Assignments menu, **Remove Assignments**
Assign menu, **Back-Annotate Project**	Assignments menu, **Back-Annotate Assignments**

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 5 of 10)

MAX+PLUS II Software	Quartus II Software
Assign menu, **Convert Obsolete Assignment Format**	NA
Utilities Menu	
 Utilities menu, **Find Text** (Ctrl+F)	Edit menu, **Find** (Ctrl+F)
 Utilities menu, **Find Node in Design File** (Ctrl+B)	 Project menu, Locate, **Locate in Design File**
 Utilities menu, **Find Node in Floorplan**	 Project menu, Locate, **Locate in Timing Closure Floorplan**
Utilities menu, **Find Clique in Floorplan**	NA
Utilities menu, **Find Node Source** (Ctrl+Shift+S)	NA
Utilities menu**, Find Node Destination** (Ctrl+Shift+D)	NA
Utilities menu, **Find Next** (Ctrl+N)	 Edit menu, **Find Next** (F3)
Utilities menu, **Find Previous** (Ctrl+Shift+N)	NA
Utilities menu, **Find Last Edit**	NA
 Utilities menu, **Search and Replace** (Ctrl+R)	 Edit menu, **Replace** (Ctrl+H)
Utilities menu, **Timing Analysis Source** (Ctrl+Alt+S)	NA
Utilities menu, **Timing Analysis Destination** (Ctrl+Alt+D)	NA
Utilities menu, **Timing Analysis Cutoff** (Ctrl+Alt+C)	NA
Utilities menu, **Analyze Timing**	NA
Utilities menu, **Clear All Timing Analysis Tags**	NA
(Text Editor) Utilities menu, **Go To** (Ctrl+G)	 Edit menu, **Go To** (Ctrl+G)
(Text Editor) Utilities menu, **Find Matching Delimiter** (Ctrl+M)	 (Text Editor) Edit, **Find Matching Delimiter** (Ctrl+M)
(Waveform Editor) Utilities menu, **Find Next Transition** (Right Arrow)	(Waveform Editor) View menu, **Next Transition** (Right Arrow)
(Waveform Editor) Utilities menu, **Find Previous Transition** (Left Arrow)	(Waveform Editor) View menu, **Next Transition** (Left Arrow)
Options Menu	
Options menu, **User Libraries**	 Assignments menu, **Settings** (Ctrl+Shift+E) Tools, Options, **Global User LIbraries**
Options menu, **Color Palette**	Tools menu, **Options**

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 6 of 10)

MAX+PLUS II Software	Quartus II Software
Options menu, **License Setup**	Tools menu, **License Setup**
Options menu, **Preferences**	Tools menu, **Options**
(Hierarchy Display) Options menu, **Orientation**	NA
(Hierarchy Display) Options menu, **Compact Display**	NA
(Hierarchy Display) Options menu, **Show All Hierarchy Branches**	(Project Navigator) Expand All on right click menu
(Hierarchy Display) Options menu, **Hide All Hierarchy Branches**	NA
(Editors) Options menu, **Font**	Tools menu, **Options**
(Editors) Options menu, **Text Size**	Tools menu, **Options**
(Graphic Editor) Options menu, **Line Style**	Edit menu, **Line**
 (Graphic Editor) Options menu, **Rubberbanding**	 Tools menu, **Options**
(Graphic Editor) Options menu, **Show Parameters**	 View menu, **Show Parameter Assignments**
(Graphic Editor) Options menu, **Show Probes**	NA
(Graphic Editor) Options menu**, Show Pins/Locations/Chips**	 View menu, **Show Pin and Location Assignments**
(Graphic Editor) Options menu, **Show Clique, Timing & Local Routing Assignments**	NA
(Graphic Editor) Options menu, **Show Logic Options**	NA
 (Graphic Editor) Options menu, **Show All** (Ctrl+Shift+M)	NA
(Graphic Editor) Options menu, **Show Guidelines** (Ctrl+Shift+G)	Tools menu, **Options** - Block/Symbol Editor page
(Graphic Editor) Options menu, **Guideline Spacing**	Tools menu, **Options** - Block/Symbol Editor page
(Symbol Editors) Options menu, **Snap to Grid**	Tools menu, **Options** - Block/Symbol Editor page
(Text Editor) Options menu, **Tab Stops**	Tools menu, **Options** - Text Editor page
(Text Editor) Options menu, **Auto-Indent**	Tools menu, **Options** - Text Editor page
(Text Editor) Options menu, **Syntax Coloring**	NA
(Waveform Editor) Options menu, **Snap to Grid**	 View menu, **Snap to Grid**
(Waveform Editor) Options menu, **Show Grid** (Ctrl+Shift+G)	Tools menu, **Options** - Waveform Editor page
(Waveform Editor) Options menu, **Grid Size**	Edit menu, **Grid Size** - Waveform Editor page

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 7 of 10)

MAX+PLUS II Software	Quartus II Software
(Floorplan Editor) Options menu, **Routing Statistics**	NA
 (Floorplan Editor) Options menu, **Show Node Fan-In**	 View menu, Routing, **Show Fan-In**
 (Floorplan Editor) Options menu, **Show Node Fan-Out**	 View menu, Routing, **Show Fan-Out**
 (Floorplan Editor) Options menu, **Show Path**	 View menu, Routing, **Show Paths between Nodes**
(Floorplan Editor) Options menu, **Show Moved Nodes in Gray**	NA
(Simulator) Options menu, **Breakpoint**	Processing menu, Simulation Debug, **Breakpoints**
(Simulator) Options menu, **Hardware Setup**	NA
(Timing Analyzer) Options menu, **Time Restrictions**	 Assignments menu, **Timing Settings**
(Timing Analyzer) Options menu, **Auto-Recalculate**	NA
(Timing Analyzer) Options menu, **Cell Width**	NA
(Timing Analyzer) Options menu, **Cut Off I/O Pin Feedback**	 Assignments menu, **Timing Settings**
(Timing Analyzer) Options menu, **Cut Off Clear & Reset Paths**	 Assignments menu, **Timing Settings**
(Timing Analyzer) Options menu, **Cut Off Read During Write Paths**	 Assignments menu, **Timing Settings**
(Timing Analyzer) Options menu, **List Only Longest Path**	NA
(Programmer) Options menu, **Sound**	NA
(Programmer) Options menu, **Programming Options**	Tools menu, **Options** - Programmer page
(Programmer) Options menu, **Select Device**	(Programmer) Edit menu, **Change Device**
(Programmer) Options menu, **Hardware Setup**	(Programmer) Edit menu, **Hardware Setup**
Symbol (Graphic Editor)	
Symbol menu, **Enter Symbol** (Double-Click)	 (Block Editor) Edit menu, **Insert Symbol** (Double-Click)
Symbol menu, **Update Symbol**	 Edit menu, **Update Symbol or Block**
Symbol menu, **Edit Ports/Parameters**	 Edit menu, **Properties**
Element (Symbol Editor)	
Element menu, **Enter Pinstub**	Double-click on edge of symbol

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 8 of 10)

MAX+PLUS II Software	Quartus II Software
Element menu, **Enter Parameters**	NA
Templates (Text Editor)	
Templates	(Text Editor) Edit menu, **Insert Template**
Node (Waveform Editor)	
Node menu, **Insert Node** (Double-Click)	Edit menu, **Insert Node or Bus** (Double-Click)
Node menu, **Enter Nodes from SNF**	Edit menu, **Insert Node** - click on Node Finder…
Node menu, **Edit Node**	Double-click on the Node
Node menu, **Enter Group**	Edit menu, **Group**
Node menu, **Ungroup**	Edit menu, **Ungroup**
Node menu, **Sort Names**	Edit menu, **Sort**
Node menu, **Enter Separator**	NA
Layout (Floorplan Editor)	
Layout menu, **Full Screen**	View menu, **Full Screen** (Ctrl+Alt+Space)
Layout menu, **Report File Equation Viewer**	View menu, **Equations**
Layout menu, **Device View** (Double-Click)	View menu, **Package Top** or View menu, **Package Bottom**
Layout menu, **LAB View** (Double-Click)	View menu, **Interior Labs**
Layout menu, **Current Assignments Floorplan**	View menu, Assignments, **Show User Assignments**
Layout menu, **Last Compilation Floorplan**	View menu, Assignments, **Show Fitter Assignments**
Processing (Compiler)	
Processing menu, **Design Doctor**	Processing menu, Start, **Start Design Assistant**
Processing menu, **Design Doctor Settings**	Assignments menu, **Settings** - Design Assistant
Processing menu, **Functional SNF Extractor**	Processing menu, **Generate Functional Simulation Netlist**
Processing menu, **Timing SNF Extractor**	Processing menu, **Start Analysis & Synthesis**
Processing menu, **Optimize Timing SNF**	NA
Processing menu, **Linked SNF Extractor**	NA

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 9 of 10)

MAX+PLUS II Software	Quartus II Software
Processing menu, **Fitter Settings**	Assignments menu, **Settings** - Fitter Settings
Processing menu, **Report File Settings**	Assignments menu, **Settings**
Processing menu, **Generate AHDL TDO File**	NA
Processing menu, **Smart Recompile**	Assignments menu, **Settings** - Compilation Process
Processing menu, **Total Recompile**	Assignments menu, **Settings** - Compilation Process
Processing menu, **Preserve All Node Name Synonyms**	Assignments menu, **Settings** - Compilation Process
Interfaces (Compiler)	Assignments menu, **EDA Tool Settings**
Initialize (Simulator)	
Initialize menu, **Initialize Nodes/Groups**	NA
Initialize menu, **Initialize Memory**	NA
Initialize menu, **Save Initialization As**	NA
Initialize menu, **Restore Initialization**	NA
Initialize menu, **Reset to Initial SNF Values**	NA
Node (Timing Analyzer)	
Node menu, **Timing Analysis Source** (Ctrl+Alt+S)	NA
Node menu, **Timing Analysis Destination** (Ctrl+Alt+D)	NA
Node menu, **Timing Analysis Cutoff** (Ctrl+Alt+C)	NA
Analysis (Timing Analyzer)	
Analysis menu, **Delay Matrix**	(Timing Analyzer Tool) Delay tab
Analysis menu, **Setup/Hold Matrix**	NA
Analysis menu, **Registered Performance**	(Timing Analyzer Tool) Registered Performance tab
JTAG (Programmer)	
JTAG menu, **Multi-Device JTAG Chain**	(Programmer) Mode: JTAG
JTAG menu, **Multi-Device JTAG Chain Setup**	(Programmer) Window
JTAG menu, **Save JCF**	File menu, **Save**
JTAG menu, **Restore JCF**	File menu, **Open**
JTAG menu, **Initiate Configuration from Configuration Device**	Tools menu, **Options** - Programmer page

Table 2–4. Quartus II Command Reference for MAX+PLUS II Users (Part 10 of 10)

MAX+PLUS II Software	Quartus II Software
FLEX (Programmer)	
FLEX menu, **Multi-Device FLEX Chain**	(Programmer) Mode: Passive Serial
FLEX menu, **Multi-Device FLEX Chain Setup**	(Programmer) Window
FLEX menu, **Save FCF**	File menu, **Save**
FLEX menu, **Restore FCF**	File menu, **Open**

3. Quartus II Support of HardCopy Series Devices

QII51004-6.0.0

Introduction

This chapter includes Quartus® II Support for HardCopy® II and HardCopy Stratix devices. This chapter is divided into the following sections:

- Quartus II Support for HardCopy II Devices
- Quartus II Support for HardCopy Stratix® Devices

HardCopy II Device Support

Altera® HardCopy II devices feature 1.2-V, 90 nm process technology, and provide a structured ASIC alternative to increasingly expensive multi-million gate ASIC designs. The HardCopy II design methodology offers a fast time-to-market schedule, providing ASIC designers with a solution to long ASIC development cycles. Using the Quartus II software, you can leverage a Stratix II FPGA as a prototype and seamlessly migrate your design to a HardCopy II device for production.

This document discusses the following topics:

- HardCopy II design development flow and companion devices
- HardCopy II Device Resource Guide
- Recommended Quartus II software settings
- HardCopy II Utilities menu options and functions

For more information about HardCopy II, HardCopy Stratix, and HardCopy APEX™ devices, refer to the respective device data sheets in the *HardCopy Series Handbook*.

HardCopy II Design Benefits

Designing with HardCopy II structured ASICs offers substantial benefits over other structured ASIC offerings:

- Prototyping using a Stratix II FPGA for functional verification and system development reduces total project development time
- Seamless migration from a Stratix II FPGA prototype to a HardCopy II device reduces time to market and risk
- Unified design methodology for Stratix II FPGA design and HardCopy II design reduces the need for ASIC development software
- Low up-front development cost of HardCopy II devices reduces the financial risk to your project

Quartus II Features for HardCopy II Planning

With the Quartus II software you can design a HardCopy II device using a Stratix II device as a prototype. The Quartus II software contains the following expanded features for HardCopy II device planning:

- **HardCopy II Companion Device Assignment**—Identifies compatible HardCopy II devices for migration with the Stratix II device currently selected.

  This feature constrains the pins of your Stratix II FPGA prototype making it compatible with your HardCopy II device. It also constrains the correct resources available for the HardCopy II device making sure that your Stratix II FPGA design does not become incompatible.

- **HardCopy II Utilities**—The HardCopy II Utilities functions create or overwrites HardCopy II companion revisions, change revisions to use, and compare revisions for equivalency.
- **HardCopy II Advisor**—The HardCopy II Advisor helps you follow the necessary steps to successfully submit a HardCopy II design to Altera's HardCopy Design Center.

  The HardCopy II Advisor is similar to the Resource Optimization Advisor and Timing Optimization Advisor. The HardCopy II Advisor provides guidelines you can follow during development, reporting the tasks completed as well as the tasks that you still need to complete during development.

- **HardCopy II Floorplan**—The Quartus II software can show a preliminary floorplan view of your HardCopy II design's Fitter placement results.
- **HardCopy II Design Archiving**—The Quartus II software archives the HardCopy II design project's files needed to handoff the design to the HardCopy Design Center.

  This feature is similar to the Quartus II software HardCopy Files Wizard used for HardCopy Stratix and HardCopy APEX families.

- **HardCopy II Device Preliminary Timing**—The Quartus II software performs a timing analysis of HardCopy II devices based on preliminary timing models and Fitter placements. Final timing results for HardCopy II devices are provided by the HardCopy Design Center.

- **HardCopy II Handoff Report**—The Quartus II software generates a handoff report containing information about the HardCopy II design used by the HardCopy Design Center in the design review process.
- **Formal Verification**—Cadence Encounter Conformal software can now perform formal verification between the source RTL design files and post-compile gate level netlist from a HardCopy II design.

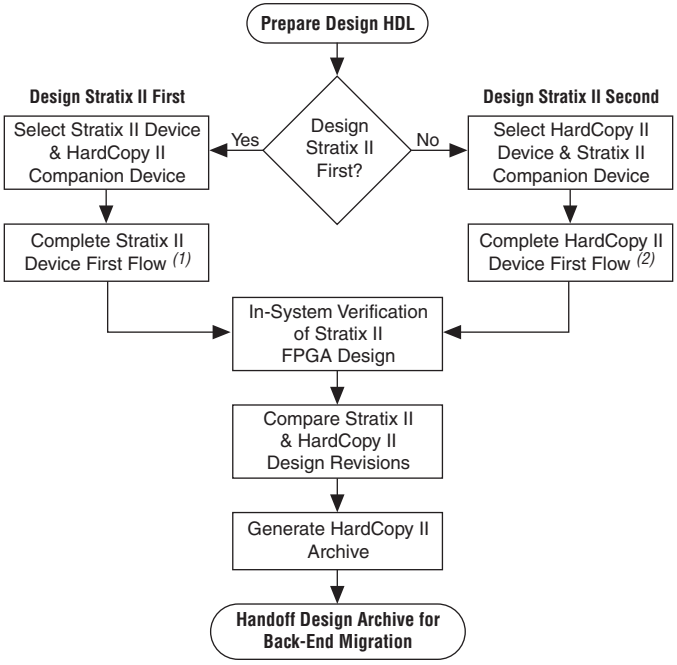
HardCopy II Development Flow

In the Quartus II software, you have two methods for designing your Stratix II FPGA and HardCopy II companion device together in one Quartus II project.

- Design the HardCopy II device first, and create the Stratix II FPGA companion device second and build your prototype for in-system verification
- Design the Stratix II FPGA first and create a HardCopy II companion device second

Both of these flows are illustrated at a high level in Figure 3–1. The added features in the HardCopy II Utilities menu assist you in completing your HardCopy II design for submission to Altera's HardCopy Design Center for back-end implementation.

Figure 3–1. HardCopy II Flow in Quartus II Software



Notes for Figure 3–1:
(1) Refer to Figure 3–2 for an expanded description of this process.
(2) Refer to Figure 3–3 for an expanded description of this process.

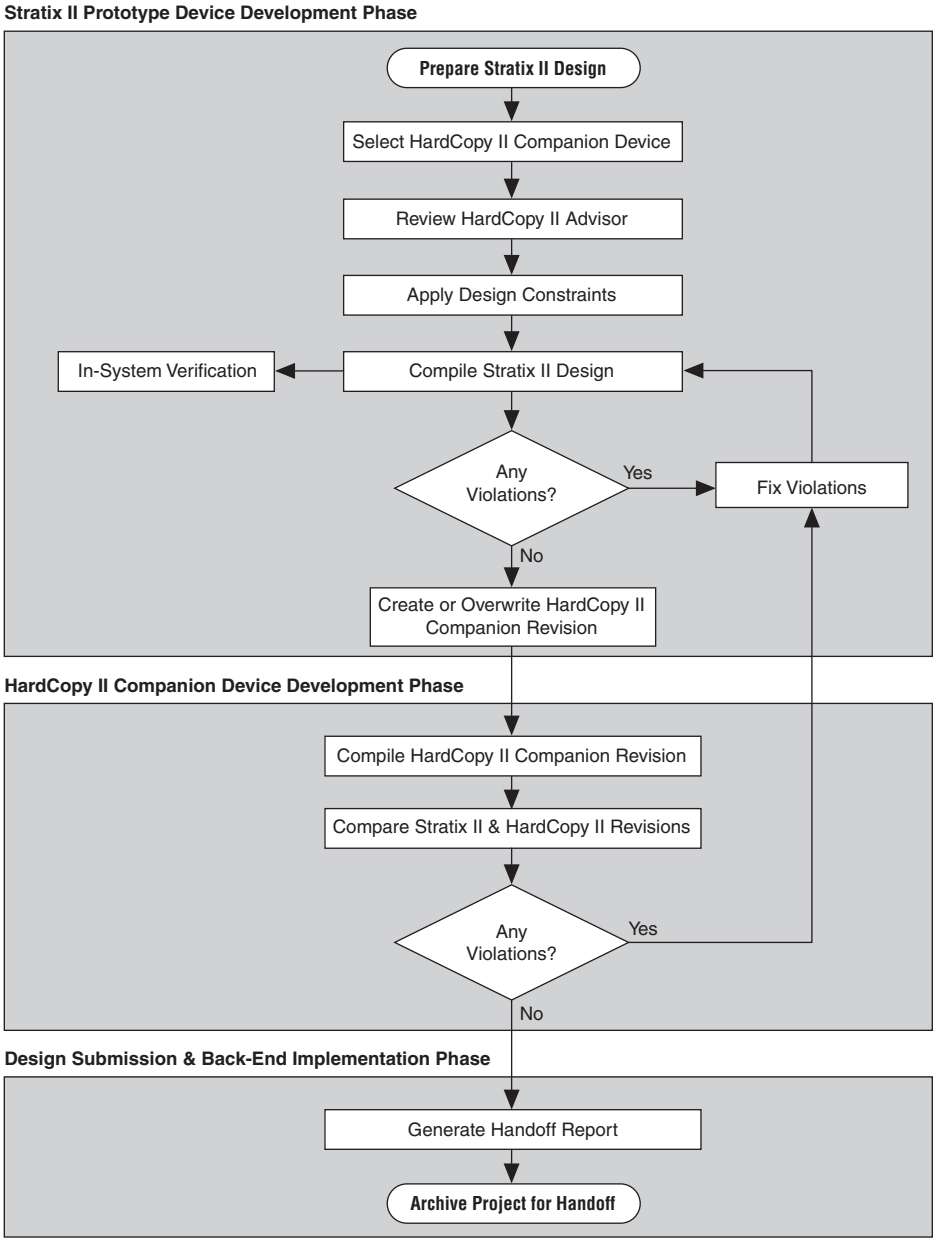
Designing the Stratix II FPGA First

The HardCopy II development flow beginning with the Stratix II FPGA prototype is very similar to a traditional Stratix II FPGA design flow, but requires a few additional tasks to be performed to migrate the design to the HardCopy II companion device. To design your HardCopy II device using the Stratix II FPGA as a prototype, complete the following tasks:

- Specify a HardCopy II device for migration
- Compile the Stratix II FPGA design
- Create and compile the HardCopy II companion revision
- Compare the HardCopy II companion revision compilation to the Stratix II device compilation

Figure 3–2 provides an overview highlighting the development process for designing with a Stratix II FPGA first and creating a HardCopy II companion device second.

Figure 3–2. Designing Stratix II Device First Flow



Prototype your HardCopy II design by selecting and then compiling a Stratix II device in the Quartus II software.

Once you compile the Stratix II design successfully, you can view the HardCopy II Device Resource Guide in the Quartus II software Fitter report to evaluate which HardCopy II devices meet your design's resource requirements. When you are satisfied with the compilation results and the choice of Stratix II and HardCopy II devices, on the Assignments menu, click **Settings**. In the **Category** list, select **Device**. In the **Device** page, select a HardCopy II companion device.

After you select your HardCopy II companion device, do the following:

- Review the HardCopy II Advisor for required and recommended tasks to perform
- Enable Design Assistant to run during compilation
- Add timing and location assignments
- Compile your Stratix II design
- Create your HardCopy II companion revision
- Compile your design for the HardCopy II companion device
- Use the HardCopy II Utilities to compare the HardCopy II companion device compilation with the Stratix II FPGA revision
- Generate a HardCopy II Handoff Report using the HardCopy II Utilities
- Generate a HardCopy II Handoff Archive using the HardCopy II Utilities
- Arrange for submission of your HardCopy II handoff archive to Altera's HardCopy Design Center for back-end implementation

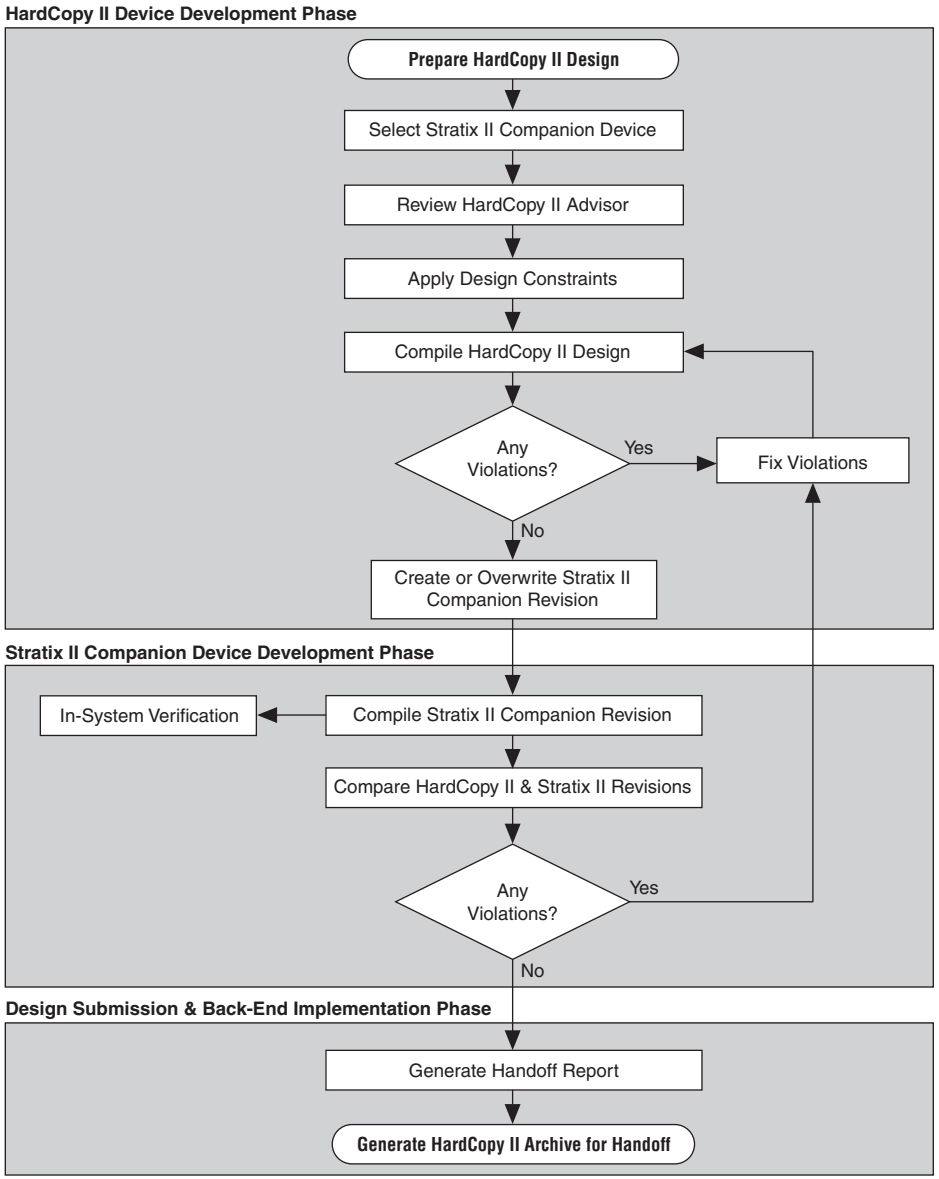
For more information about the overall design flow using the Quartus II software, refer to the *Introduction to Quartus II* manual on the Altera web site at www.altera.com.

Designing the HardCopy II Device First

The HardCopy II family presents a new option in designing unavailable in previous HardCopy families. You can design your HardCopy II device first and create your Stratix II FPGA prototype second in the Quartus II software. This allows you to see your potential maximum performance in the HardCopy II device immediately during development, and you can create a slower performing FPGA prototype of the design for in-system verification. This design process is similar to the traditional HardCopy II design flow where you build the FPGA first, but instead, you merely change the starting device family. The remaining tasks to complete your design for both Stratix II and HardCopy II devices roughly follow the

same process (Figure 3–3). The HardCopy II Advisor adjusts its list of tasks based on which device family you start with, Stratix II or HardCopy II, so that you can complete the process seamlessly.

Figure 3–3. Designing HardCopy II Device First Flow



HardCopy II Device Resource Guide

The HardCopy II Device Resource Guide compares the resources required to successfully compile a design with the resources available in the various HardCopy II devices. The report rates each HardCopy II device and each device resource for how well it fits the design. The Quartus II software generates the HardCopy II Device Resource Guide for all designs successfully compiled for Stratix II devices, and is found in the Fitter folder of the Compilation Report. Figure 3–4 shows an example of the HardCopy II Device Resource Guide. Refer to Table 3–1 for an explanation of the color codes in Figure 3–4.

Figure 3–4. HardCopy II Device Resource Guide

HardCopy II Device Resource Guide

Color Legend:
-- Green:
-- Package Resource: The HardCopy II package can be migrated from the Stratix II FPGA selected package, and the design has been fitted with the target device migration enabled.

	Resource	Stratix II EP2S130	HC210W*	HC210	HC220	HC220	HC230	HC240	HC240
1	Migration Compatibility		None	None	None	None	Medium	None	None
2	Primary Migration Constraint		Package	Package	Package	Package	Package	Package	Package
3	Package	FBGA - 1020	FBGA - 484	FBGA - 484	FBGA - 672	FBGA - 780	FBGA - 1020	FBGA - 1020	FBGA - 1508
4	⊟ Logic	--	19%	19%	10%	10%	6%	4%	4%
5	-- Logic cells	35572 ALUTs	--	--	--	--	--	--	--
6	-- DSP elements	0	--	--	--	--	--	--	--
7	⊟ Pins								
8	-- Total	515	515 / 302	515 / 335	515 / 493	515 / 495	515 / 699	515 / 743	515 / 952
9	-- Differential Input	0	0 / 66	0 / 70	0 / 90	0 / 90	0 / 128	0 / 224	0 / 272
10	-- Differential Output	0	0 / 44	0 / 50	0 / 70	0 / 70	0 / 112	0 / 200	0 / 256
11	-- PCI / PCI-X	0	0 / 153	0 / 167	0 / 245	0 / 247	0 / 359	0 / 367	0 / 472
12	-- DQ	0	0 / 20	0 / 20	0 / 50	0 / 50	0 / 204	0 / 204	0 / 204
13	-- DQS	0	0 / 8	0 / 8	0 / 18	0 / 18	0 / 72	0 / 72	0 / 72
14	⊟ Memory								
15	-- M-RAM	6	6 / 0	6 / 0	6 / 2	6 / 2	6 / 6	6 / 9	6 / 9
16	-- M4K blocks & M512 blocks**	44	44 / 190	44 / 190	44 / 408	44 / 408	44 / 614	44 / 816	44 / 816
17	⊟ PLLs								
18	-- Enhanced	2	2 / 2	2 / 2	2 / 2	2 / 2	2 / 4	2 / 4	2 / 4
19	-- Fast	0	0 / 2	0 / 2	0 / 2	0 / 2	0 / 4	0 / 8	0 / 8
20	DLLs	0	0 / 1	0 / 1	0 / 1	0 / 1	0 / 2	0 / 2	0 / 2
21	⊟ SERDES								
22	-- RX	0	0 / 17	0 / 21	0 / 31	0 / 31	0 / 46	0 / 92	0 / 116
23	-- TX	0	0 / 18	0 / 19	0 / 29	0 / 29	0 / 44	0 / 88	0 / 116
24	⊟ Configuration								
25	-- CRC	0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
26	-- ASMI	0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
27	-- Remote Update	0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
28	-- JTAG	0	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1	0 / 1

* Device is preliminary. Overall performance is expected to be degraded.
** Design contains one or more M512 blocks, which cannot be migrated to HardCopy II devices.

Use this report to determine which HardCopy II device is a potential candidate for migration of your Stratix II design. The HardCopy II device package must be compatible with the Stratix II device package. A logic

resource usage greater than 100% or a ratio greater than 1/1 in any category indicates that the design does not fit in that particular HardCopy II device.

Table 3–1. HardCopy II Device Resource Guide Color Legend

Color	Package Resource *(1)*	Device Resources
Green (High)	The design can migrate to the Hardcopy II package and the design has been fit with target device migration enabled in the **HardCopy II Companion Device** dialog box.	The resource quantity is within the range of the HardCopy II device and the design can likely migrate if all other resources also fit.
Orange (Medium)	The design can migrate to the Hardcopy II package. However, the design has not been fit with target device migration enabled in the **HardCopy II Companion Device** dialog box.	The resource quantity is within the range of the HardCopy II device. However, the resource is at risk of exceeding the range for the HardCopy II package. Consult your Product Field Applications Engineer for a recommended course of action.
Red (None)	The design cannot migrate to the Hardcopy II package.	The resource quantity exceeds the range of the HardCopy II device. The design cannot migrate to this HardCopy II device.

Note to Table 3–1:

(1) The package resource is constrained by the Stratix II FPGA that the design was compiled for. Only vertical migration devices within the same package are able to migrate to HardCopy II devices.

The HardCopy II architecture consists of an array of fine-grained HCells, which are used to build logic equivalent to Stratix II adaptive logic modules (ALMs) and digital signal processing (DSP) blocks. The DSP blocks in HardCopy II devices match the functionality of the Stratix II DSP blocks, though timing of these blocks will be different than the FPGA since they are constructed of HCell Macros. The M4K and M-RAM memory blocks in HardCopy II devices are equivalent to the Stratix II memory blocks. Preliminary timing reports of the HardCopy II device are available in the Quartus II software. Final timing results of the HardCopy II device are provided by the HardCopy Design Center after back-end migration is complete.

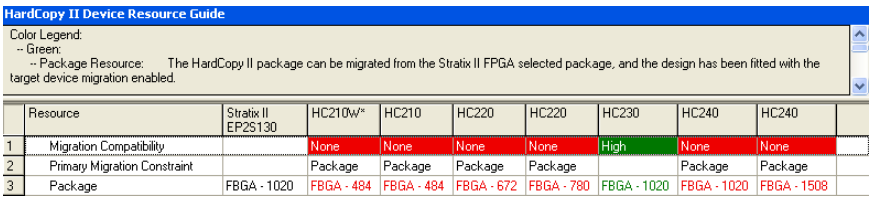
For more information about the HardCopy II device resources, refer to the *Introduction to HardCopy II Devices* and the *Description, Architecture & Features* chapters in the *HardCopy II Device Family Data Sheet* in the *HardCopy Series Handbook*.

The report example in Figure 3–4 shows the resource comparisons for a design compiled for a Stratix II EP2S130F1020 device. Based on the report, the HC230F1020 device in the 1,020-pin FineLine BGA® package is an appropriate HardCopy II device to migrate to. If the HC230F1020 device was not specified as a migration target during the compilation, its package and migration compatibility would be rated orange or Medium.

The migration compatibility of the other HardCopy II devices are rated red, or None, because the package types are incompatible with the Stratix II device. The 1,020-pin FBGA HC240 device is rated red because it is only compatible with the Stratix II EP2S180F1020 device.

Figure 3–5 shows the report after the (unchanged) design was recompiled with the HardCopy II HC230F1020 device specified as a migration target. Now the HC230F1020 device package and migration compatibility are rated green or High.

Figure 3–5. HardCopy II Device Resource Guide with Target Migration Enabled



HardCopy II Device Resource Guide

Color Legend:
-- Green:
-- Package Resource: The HardCopy II package can be migrated from the Stratix II FPGA selected package, and the design has been fitted with the target device migration enabled.

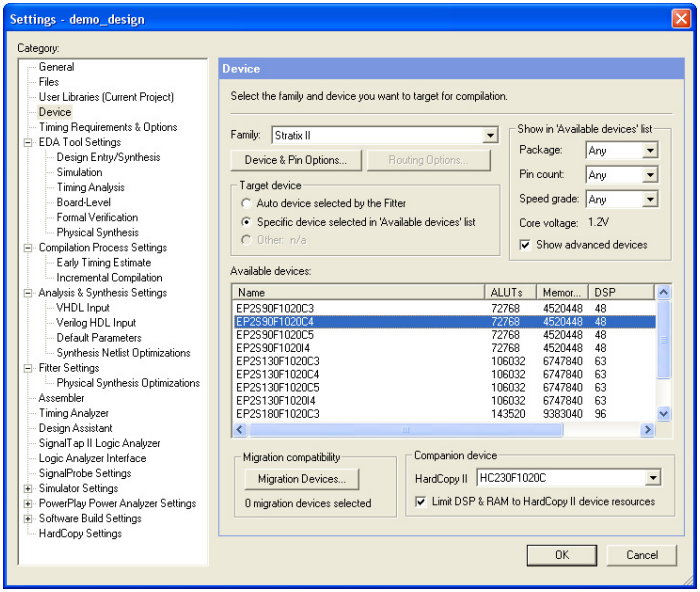
	Resource	Stratix II EP2S130	HC210W*	HC210	HC220	HC220	HC230	HC240	HC240
1	Migration Compatibility		None	None	None	None	High	None	None
2	Primary Migration Constraint		Package	Package	Package	Package		Package	Package
3	Package	FBGA - 1020	FBGA - 484	FBGA - 484	FBGA - 672	FBGA - 780	FBGA - 1020	FBGA - 1020	FBGA - 1508

HardCopy II Companion Device Selection

In the Quartus II software, you can select a HardCopy II companion device to help structure your design for migration from a Stratix II device to a HardCopy II device. To make your HardCopy II companion device selection, on the Assignments menu, click **Settings**. In the **Settings** dialog box in the **Category** list, select **Device** (Figure 3–6) and select your companion device from the **Available devices** list.

Selecting a HardCopy II Companion device to go with your Stratix II prototype constrains the memory blocks, DSP blocks, and pin assignments, so that your Stratix II and HardCopy II devices are migration-compatible. Pin assignments are constrained in the Stratix II design revision so that the HardCopy II device selected is pin-compatible. The Quartus II software also constrains the Stratix II design revision so it does not use M512 memory blocks or exceed the number of M-RAM blocks in the HardCopy II companion device.

Figure 3–6. Quartus II Settings Dialog Box



You can also specify your HardCopy II companion device using the following Tcl command:

```
set_global_assignment -name
DEVICE_TECHNOLOGY_MIGRATION_LIST <HardCopy II Device Part Number>
```

For example, to select the HC230F1020 device as your HardCopy II companion device for the EP2S130F1020C4 Stratix II FPGA, the Tcl command is:

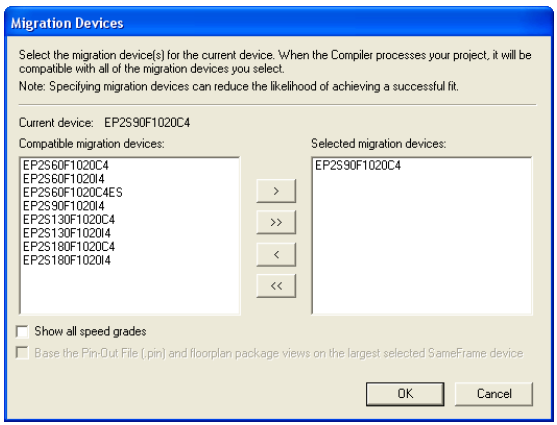
```
set_global_assignment -name
DEVICE_TECHNOLOGY_MIGRATION_LIST HC230F1020
```

Migration Compatibility Filtering

The **Migration Devices** dialog box displays which devices are vertically migratable within the same package and family for all Altera devices. When you are designing for HardCopy II devices with a Stratix II prototype device, the **Migration Devices** dialog box filters the compatible devices between Stratix II devices and HardCopy II devices within the same package.

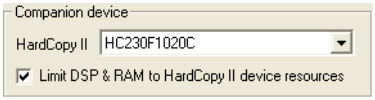
To view all Stratix II devices that are vertically migratable to a Stratix II device, on the Assignments menu, click **Settings**. In the **Category** list, select **Device** and on the **Device** page, in the **Family** list select **Stratix II**. In the **Available devices** list, select the desired device. Under **Companion device** in the **HardCopy II** list, select **<None>**, and click **Migration Devices**. The **Migration Devices** dialog box shows the Stratix II devices that are vertically migratable to the currently selected Stratix II device (Figure 3–7).

Figure 3–7. Available Migration Devices without Selecting a HardCopy II Device



Without HardCopy II companion device constraints, all Stratix II devices in the 1,020-pin FineLine BGA package are available for vertical migration. Selecting a HardCopy II companion device in the **Device** page, as shown in Figure 3–8, filters the list of migration devices to only those Stratix II devices that are vertically migratable within the same package and are usable as HardCopy II prototype devices.

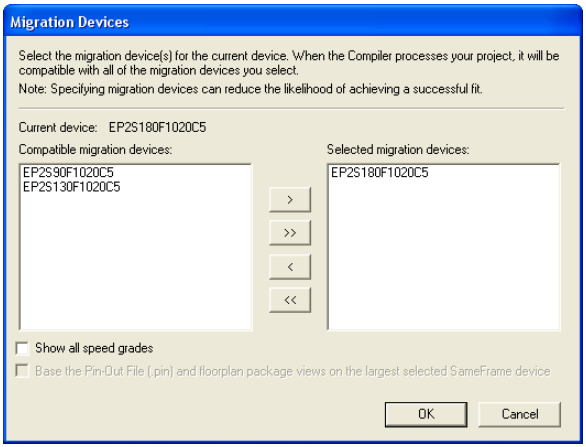
Figure 3–8. Setting a HardCopy II Companion Device



For example, if you select the HC230F1020 device as the companion device, the **Migration Devices** dialog box shows the EP2S90F1020C4 and EP2S180F1020C4 devices as possible companion devices to the EP2S130F1020C4 device currently selected (Figure 3–9). However, the

EP2S60F1020C4 device is not a compatible device to the HC230F1020 device, even though it is in the same package, so it is not listed in the **Migration Devices** dialog box.

Figure 3–9. Available Migration Devices after Selecting a HardCopy II Device



HardCopy II Recommended Settings in the Quartus II Software

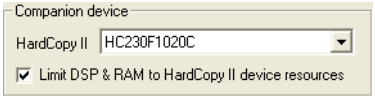
The HardCopy II development flow involves additional planning and preparation in the Quartus II software compared to a standard FPGA design. This is because you are developing your design to be implemented in two devices: a prototype of your design in a Stratix II prototype FPGA, and a companion revision in a HardCopy II device for production. You need additional settings and constraints to make the Stratix II design compatible with the HardCopy II device and, in some cases, you must remove certain settings in the design. This section explains the additional settings and constraints necessary for your design to be successful in both Stratix II FPGA and HardCopy II structured ASIC devices.

Limit DSP & RAM to HardCopy II Device Resources

On the Assignments menu, click **Settings** to view the **Settings** dialog box. In the **Category** list, select **Device**. In the **Family** list, select **Stratix II**. Under **Companion device**, **Limit DSP & RAM to HardCopy II device resources** is turned on by default (Figure 3–10). This maintains compatibility between the Stratix II and HardCopy II devices by ensuring your design does not use resources in the Stratix II device that are not available in the selected HardCopy II device.

If you require additional memory blocks or DSP blocks for debugging purposes using SignalTap® II, you can temporarily turn this setting off to compile and verify your design in your test environment. However, your final Stratix II and HardCopy II designs submitted to Altera for back-end migration must be compiled with this setting turned on.

Figure 3–10. Limit DSP & RAM to HardCopy II Device Resources Check Box



Enable Design Assistant to Run During Compile

You must use the Quartus II Design Assistant to check all HardCopy series designs for design rule violations before submitting the designs to the Altera HardCopy Design Center. Additionally, you must fix all critical and high-level errors.

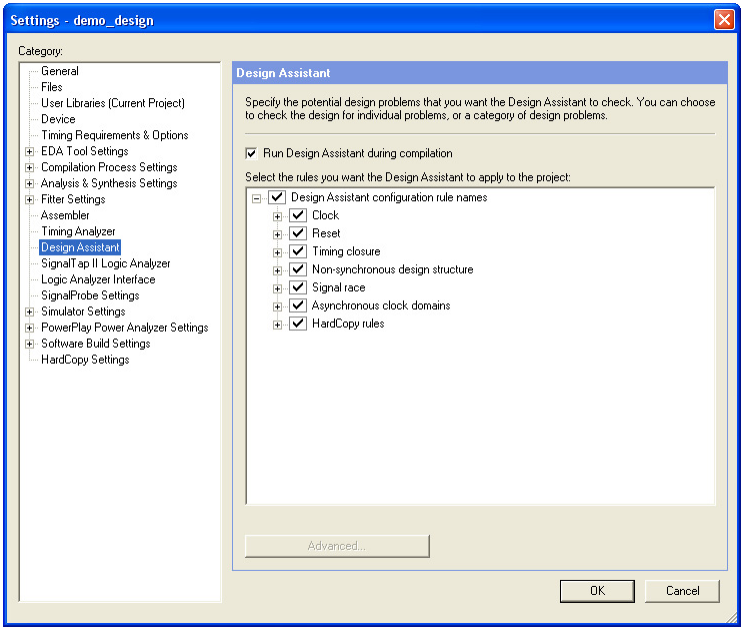
Altera recommends turning on the Design Assistant to run automatically during each compile, so that during development, you can see the violations you must fix.

For more information about the Design Assistant and the rules it uses, refer to the *Design Guidelines for HardCopy Series Devices* chapter of the *HardCopy Series Handbook*.

To enable the Design Assistant to run during compilation, on the Assignment menu, click **Settings**. In the **Category** list, select **Design Assistant** and turn on **Run Design Assistant during compilation** (Figure 3–11) or by entering the following Tcl command in the Tcl Console:

```
set_global_assignment -name ENABLE_DRC_SETTINGS ON
```

Figure 3–11. Enabling Design Assistant



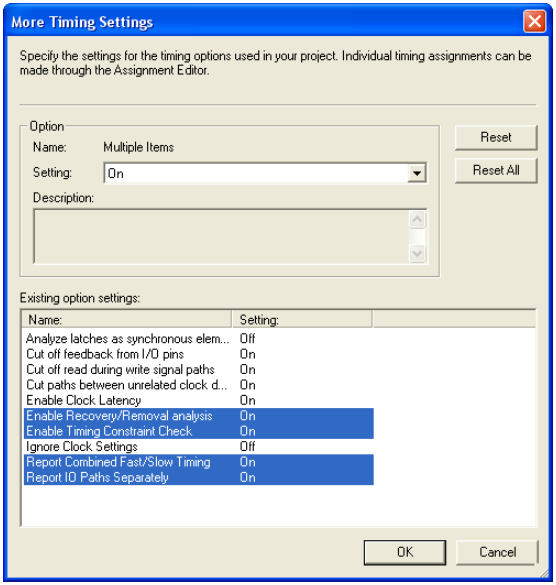
Timing Settings

In the **More Timing Settings** dialog box, you can specify optional timing settings, some of which are crucial to HardCopy II development. To specify these options, on the Assignments menu, click **Settings**. In the **Category** list, select **Timing Requirements & Options** and click **More Settings**. In the More Settings dialog box, set the desired timing settings (Figure 3–12).

For Stratix II and HardCopy II co-development, Altera recommends that you turn on the following settings:

- Enable Clock Latency
- Enable Recovery/Removal analysis
- Enable Timing Constraint Check
- Report Combined Fast/Slow Timing
- Report IO Paths Separately

Figure 3–12. More Timing Settings



Enable Clock Latency

Turning on the **Enable Clock Latency** option enables support for clock latency in the Timing Analyzer. Latency on a clock is a delay on the clock path and affects clock skew. This is different from an offset, which instead alters the setup relationship between two clocks.

When you enable clock latency, the design adjusts for early and late clock latency assignments. The phase-locked loop (PLL) compensation delay is analyzed as latency and does not affect the offset. For clock settings where you have not specified an offset, the design automatically treats computed offset as latency. By using latency for these automatically calculated clock offsets, the setup relationship for registers driven by these clocks does not vary with routing. This can potentially remove the need for multicycle assignments, as well as improve results by ensuring that timing results are more consistent for each Fitter iteration.

Once enabled, you might need to add, modify, or remove multicycle assignments for the PLL output clocks because of the potential change in the setup relationship for these clocks.

Use the following Tcl command to enable clock latency:

```
set_global_assignment -name ENABLE_CLOCK_LATENCY ON
```

Enable Recovery/Removal Analysis

This setting allows the Quartus II Timing Analysis tool to calculate recovery and removal times on control and reset signals. The recovery time is the minimum length of time that an asynchronous control input pin must be stable before the clock active edge. The removal time is the minimum length of time that an asynchronous control input pin must be stable after the clock active edge.

Altera recommends that you turn on register recovery/removal analysis in the Timing Analysis tool during development for more complete recovery/removal analysis of all logic paths in your design. However, if your design does not have a timing requirement for reset logic this option may be turned off.

Use the following Tcl command to enable recovery and removal analysis:

```
set_global_assignment -name \
ENABLE_RECOVERY_REMOVAL_ANALYSIS ON
```

Enable Timing Constraint Check

The **Enable Timing Constraint Check** setting enables the Timing Analysis tool to review your timing constraints for complete minimum and maximum timing coverage for all inputs, outputs, and bidirectional pins, as well as clock settings for all clock sources. Asynchronous pins such as resets and static control signals are also checked for minimum and maximum delay constraints. You must perform this check and review the results before handoff of the design to the HardCopy Design Center.

Use the following Tcl command to enable Timing Constraint Check:

```
set_global_assignment -name \
FLOW_ENABLE_TIMING_CONSTRAINT_CHECK ON
```

Report Combined Fast/Slow Timing

The Quartus II software can perform a separate timing analysis for worst-case and best-case conditions as independent reports. The **Report Combined Fast/Slow Timing** setting allows the Quartus II software to report slow corner delay case and fast corner delay case timing in one combined report. This setting provides a better timing report for your design by allowing you to see all hold-time issues as well as setup issues in one report. This report is required for HardCopy II device

development. Turning on the **Report Combined Fast/Slow Timing** setting requires the Quartus II software to run the Timing Analyzer twice, once for the fast corner delay model and once for the slow corner delay model.

Use the following Tcl command to enable the **Report Combined Fast/Slow Timing** setting:

```
set_global_assignment -name DO_COMBINED_ANALYSIS ON
```

Report IO Paths Separately

Turn on the **Report IO Paths Separately** setting to create separate report panels for I/O paths constrained by the `INPUT_MAX_DELAY`, `INPUT_MIN_DELAY`, `OUTPUT_MAX_DELAY`, or `OUTPUT_MIN_DELAY` parameters. To specify these constraints, on the Assignments menu, click **Assignment Editor**. By default, I/O paths are reported in the **Clock Setup** and **Clock Hold** sections of the **Timing Analyzer** compilation report.

Altera recommends that you turn on the **Report IO Paths Separately** setting to make it easier to view the I/O timing analysis reports for each device pin. This is optional in FPGA designs, but is helpful for HardCopy II development because the I/O timing requirements you specify must be met in both Stratix II I/O timing and HardCopy II I/O timing results. This setting helps to guarantee drop-in compatibility between your Stratix II FPGA prototype and your HardCopy II structured ASIC.

Use the following Tcl command to enable the **Report IO Paths Separately** setting:

```
set_global_assignment -name \
REPORT_IO_PATHS_SEPARATELY ON
```

Quartus II Software Version 6.0 Features Supported for HardCopy II Designs

The Quartus II software supports optimization features for HardCopy II prototype development including:

- Physical Synthesis Optimization
- LogicLock Regions
- PowerPlay Power Analyzer

Physical Synthesis Optimization

To enable the Physical Synthesis Optimizations for the Stratix II FPGA revision of the design, on the Assignments menu, click **Settings**. In the **Settings** dialog box, in the **Category** list, select **Fitter Settings**. These optimizations get migrated into the HardCopy II companion revision for placement and timing closure. When designing with a HardCopy II device first, physical synthesis optimizations can be enabled for the HardCopy II device, and these post-fit optimizations get migrated to the Stratix II FPGA revision.

LogicLock Regions

The use of LogicLock Regions in the Stratix II FPGA are supported for designs migrating to HardCopy II. However, the LogicLock Regions are not passed into the HardCopy II Companion Revision. You can use LogicLock in the HardCopy II design but you must create new LogicLock Regions in the HardCopy II companion revision. In addition, LogicLock Regions in HardCopy II devices can not have their properties set to Auto Size or Floating Location. HardCopy II LogicLock Regions must be manually sized and placed in the floorplan. When LogicLock Regions are created in a HardCopy II device, they start with width and height dimensions set to (1,1), and the origin coordinates for placement are at X1_Y1 in the lower left corner of the floorplan. You must adjust the size and location of your LogicLock Regions created in the HardCopy II device before compiling the design.

For information about using LogicLock Regions, refer to the *LogicLock Design Methodology*, chapter in volume 2 of the *Quartus II Handbook* on the Altera web site at www.altera.com.

PowerPlay Power Analyzer

You can perform power estimation and analysis of your HardCopy II and Stratix II devices using the PowerPlay Early Power Estimator and PowerPlay Power Analyzer for more accurate estimation of your device's power consumption. The PowerPlay Early Power Estimation is available in the Quartus II software version 5.1 and later. The PowerPlay Power Analyzer supports HardCopy II devices in version 6.0 and later of the Quartus II software.

For more information about using the PowerPlay Power Analyzer, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Quartus II Features Not Presently Supported for HardCopy II Designs

The Quartus II software version 6.0 does not support HardCopy II devices with all of the advanced design features available for other Altera devices. Many of these features are scheduled for subsequent releases of the Quartus II software.

The Quartus II software version 6.0 does not support the following features for HardCopy II prototype development using the Stratix II FPGA:

- Incremental compilation (Synthesis and Fitter)
- Maximum fan-out assignments

Chip Editor for HardCopy II Devices

When using the Quartus II Chip Editor for your HardCopy II design, the Chip Editor changes are done in the following two ways:

- A Chip Editor change is applied to a compiled Stratix II design revision and a new HardCopy II Companion Revision is created afterwards, incorporating the Chip Editor modifications.
- A Chip Editor change is performed separately on compiled, existing Stratix II and HardCopy II design revisions. No new companion revisions are created.

If you want to use the Quartus II Chip Editor on a Stratix II design you want to migrate to a HardCopy II device, it is best if you start with a compiled Stratix II project and a new HardCopy II Companion Revision created or overwritten using the HardCopy II Utilities.

Using the Chip Editor on a compiled HardCopy II design revision, requires that you manually complete the changes in both HardCopy II and Stratix II revisions, and then use the HardCopy II Companion Comparison Utility and third-party formal verification software to determine if they are equivalent.

The Chip Editor for HardCopy II has the following enabled features:

- Add/Modify/Remove an HCell Macro of a Combinational Function, Register, or Adder/Subtractor and connect wires to them
- Create new wires in the design
- Edit IO Cell properties such as drive strength or programmable delay values
- Edit PLL settings such as M/N counter settings or phase shift of derived clocks

For more information about using the Quartus II Chip Editor, refer to the *Engineering Change Management* chapter in volume 1 of the *Quartus II Handbook*.

Formal Verification of Stratix II & HardCopy II Revisions

Third party formal verification software is available for your HardCopy II design. Cadence Encounter Conformal verification software is used for Stratix II and HardCopy II families, as well as several other Altera product families.

In order to use the Conformal software with the Quartus II software project for your Stratix II and HardCopy II design revisions, you must enable the **EDA Netlist Writer.** It is necessary to turn on the EDA Netlist Writer so it can generate the necessary netlists and command files needed to run the Conformal software. To automatically run the EDA Netlist Writer during the compile of your Stratix II and HardCopy II design revisions, perform the following steps:

1. On the Assignment menu, click **EDA Tool Settings**. The **Settings** dialog box displays.
2. In the **EDA Tool Settings** list, select **Formal Verification**, and in the **Tool name** list, select **Conformal LEC**.
3. Compile your Stratix II and Hardcopy II design revisions, with both the EDA Tool Settings and the Conformal LEC turned on so the EDA Netlist Writer automatically runs.

The Quartus II EDA Netlist Writer produces one netlist for Stratix II when it is run on that revision, and generates a second netlist when it runs on the HardCopy II revision. You can compare your Stratix II post-compile netlist to your RTL source code using the scripts generated by the EDA Netlist Writer. Similarly, you can compare your HardCopy II post-compile netlist to your RTL source code with scripts provided by the EDA Netlist Writer.

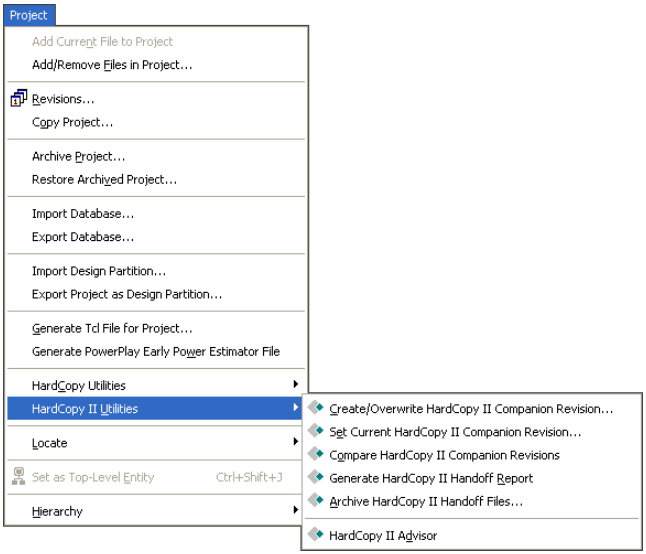
For more information about using the Cadence Encounter Conformal verification software, refer to the *Cadence Encounter Conformal Support* chapter in volume 3 of the *Quartus II Handbook*.

HardCopy II Utilities Menu

The **HardCopy II Utilities** menu is shown in the Quartus II software (Figure 3–13). To access this menu, on the Project menu, click **HardCopy II Utilities**. This menu contains the main functions you use to develop your HardCopy II design and Stratix II FPGA prototype companion revision. From the HardCopy II Utilities menu, you can:

- Create or update HardCopy II companion revisions
- Set which HardCopy II companion revision is the current revision
- Generate HardCopy II Handoff Report for design reviews
- Archive HardCopy II Handoff Files for submission to the HardCopy Design Center
- Compare the companion revisions for functional equivalence
- Track your design progress using the HardCopy II Advisor

Figure 3–13. HardCopy II Utilities Menu



Each of the features within the **HardCopy II Utilities** is summarized in Table 3–2. The process for using each of these features is explained in the following sections.

Table 3–2. HardCopy II Utilities Menu Options

Menu	Description	Applicable Design Revision	Restrictions
Create/Overwrite HardCopy II Companion Revision	Create a new companion revision or update an existing companion revision for your Stratix II and HardCopy II design.	Stratix II prototype design and HardCopy II Companion Revision	• Must disable Auto Device selection • Must set a Stratix II device and a HardCopy II companion device
Set Current HardCopy II Companion Revision	Specify which companion revision to associate with current design revision.	Stratix II prototype design and HardCopy II Companion Revision	Companion Revision must already exist
Compare HardCopy II Companion Revisions	Compares the Stratix II design revision with the HardCopy II companion design revision and generates a report.	Stratix II prototype design and HardCopy II Companion Revision	Compilation of both revisions must be complete
Generate HardCopy II Handoff Report	Generate a report containing important design information files and messages generated by the Quartus II compile	Stratix II prototype design and HardCopy II Companion Revision	• Compilation of both revisions must be complete • Compare HardCopy II Companion Revisions must have been executed
Archive HardCopy II Handoff Files	Generate a Quartus II Archive File specifically for submitting the design to the HardCopy Design Center. Similar to the HardCopy Files Wizard for HardCopy Stratix and APEX.	HardCopy II Companion Revision	• Compilation of both revisions must be completed • Compare HardCopy II Companion Revisions must have been executed • Generate HardCopy Handoff Report must have been executed
HardCopy II Advisor	Open an Advisor, similar to the Resource Optimization Advisor, helping you through the steps of creating a HardCopy II project.	Stratix II prototype design and HardCopy II Companion Revision	None

Companion Revisions

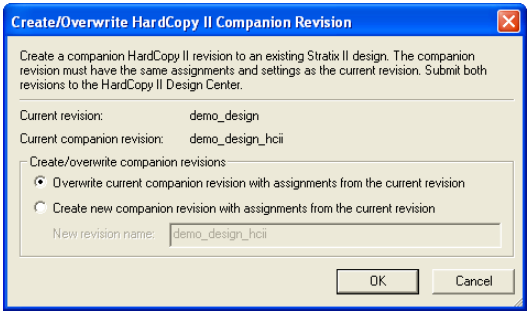
HardCopy II designs follow a different development flow in the Quartus II software compared with previous HardCopy families. You can create multiple revisions of your Stratix II prototype design, but you can also create separate revisions of your design for a HardCopy II device.

The Quartus II software creates specific HardCopy II design revisions of the project in conjunction to the regular project revisions. These parallel design revisions for HardCopy II devices are called companion revisions.

Although you can create multiple project revisions, Altera recommends that you maintain only one Stratix II FPGA revision once you have created the HardCopy II *companion revision*.

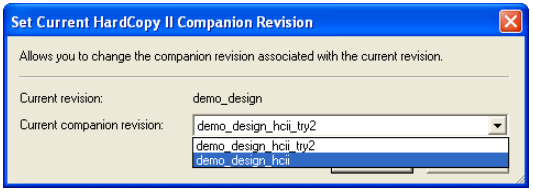
When you have successfully compiled your Stratix II prototype FPGA, you can create a HardCopy II companion revision of your design and proceed with compiling the HardCopy II companion revision. To create a companion revision, on the Project menu, point to HardCopy II Utilities and click **Create/Overwrite HardCopy II Companion Revision**. Use the dialog box to create a new companion revision or overwrite an existing companion revision (Figure 3–14).

Figure 3–14. Create or Overwrite HardCopy II Companion Revision



You can associate only one Stratix II revision to one HardCopy II companion revision. If you created more than one revision or more than one companion revision, set the current companion for the revision you are working on. On the Project menu, point to HardCopy II Utilities and click **Set Current HardCopy II Companion Revision** (Figure 3–15).

Figure 3–15. Set Current HardCopy II Companion Revision

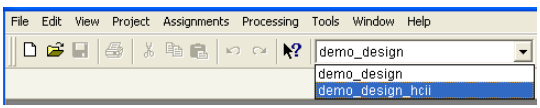


Compiling the HardCopy II Companion Revision

The Quartus II software enables you to compile your HardCopy II design with preliminary timing information. The timing constraints for the HardCopy II companion revision can be the same as the Stratix II design used to create the revision. The Quartus II software contains preliminary timing models for HardCopy II devices and you can gauge how much performance improvement you can achieve in the HardCopy II device compared to the Stratix II FPGA. Altera verifies that the HardCopy II Companion Device timing requirements are met in the HardCopy Design Center.

After you create your HardCopy II companion revision from your compiled Stratix II design, select the companion revision in the Quartus II software design revision drop-down box (Figure 3–16) or from the **Revisions** list. Compile the HardCopy II companion revision. After the Quartus II software compiles your design, you can perform a comparison check of the HardCopy II companion revision to the Stratix II prototype revision.

Figure 3–16. Changing Current Revision



Comparing HardCopy II & Stratix II Companion Revisions

Altera uses the companion revisions in a single Quartus II project to maintain the seamless migration of your design from a Stratix II FPGA to a HardCopy II structured ASIC. This methodology allows you to design with one set of Register Transfer Level (RTL) code to be used in both Stratix II FPGA and HardCopy II structured ASIC, guaranteeing functional equivalency.

When making changes to companion revisions, use the Compare HardCopy II Companion Revisions feature to ensure that your Stratix II design matches your HardCopy II design functionality and compilation settings. To compare companion revisions, on the Project menu, point to HardCopy II Utilities and click **Compare HardCopy II Companion Revisions**.

You must perform this comparison after both Stratix II and HardCopy II designs are compiled in order to hand off the design to Altera's HardCopy Design Center.

The Comparison Revision Summary is found in the Compilation Report and identifies where assignments were changed between revisions or if there is a change in the logic resource count due to different compilation settings.

Generate HardCopy II Handoff Report

In order to submit a design to the HardCopy Design Center, you must generate a HardCopy II Handoff Report providing important information about the design that you want the HardCopy Design Center to review. To generate the HardCopy II Handoff Report, you must:

- Successfully compile both Stratix II and HardCopy II revisions of your design
- Successfully run the Compare HardCopy II Companion Revisions utility

Once you generate the HardCopy II Handoff Report, you can archive the design using the Archive HardCopy II Handoff Files utility described in "Archive HardCopy II Handoff Files" on page 3–26.

Archive HardCopy II Handoff Files

The last step in the HardCopy II design methodology is to archive the HardCopy II project for submission to the HardCopy Design Center for back-end migration. The HardCopy II archive utility creates a different Quartus II Archive File than the standard Quartus II project archive utility generates. This archive contains only the necessary data from the Quartus II project needed to implement the design in the HardCopy Design Center.

In order to use the **Archive HardCopy II Handoff Files** utility, you must complete the following:

- Compile both the Stratix II and HardCopy II revisions of your design
- Run the Compare HardCopy II Revisions utility
- Generate the HardCopy II Handoff Report

To select this option, on the Project menu point to HardCopy II Utilities and click **Archive HardCopy II Handoff File** utility.

HardCopy II Advisor

The HardCopy II Advisor provides the list of tasks you should follow to develop your Stratix II prototype and your HardCopy II design. To run the HardCopy II Advisor, on the Project menu, point to HardCopy II Utilities and click **HardCopy II Advisor**. The following list highlights the

checkpoints that the HardCopy II Advisor reviews. This list includes the major check points in the design process; it does not show every step in the process for completing your Stratix II and HardCopy II designs:

1. Select a Stratix II device.
2. Select a HardCopy II device.
3. Turn on the **Design Assistant**.
4. Set up timing constraints.
5. Check for incompatible assignments.
6. Compile and check Stratix II design.
7. Create or overwrite companion revision.
8. Compile and check HardCopy II companion results.
9. Compare companion revisions.
10. Generate Handoff Report.
11. Archive Handoff Files and send to Altera.

The HardCopy II Advisor shows the necessary steps that pertain to your current selected device. The Advisor shows a slightly different view for a design with Stratix II selected as compared to a design with HardCopy II selected.

In the Quartus II software, you can start designing with the HardCopy II device selected first, and build a Stratix II companion revision second. When you use this approach, the HardCopy II Advisor task list adjusts automatically to guide you from HardCopy II development through Stratix II FPGA prototyping, it then completes the comparison archiving and handoff to Altera.

When your design uses the Stratix II FPGA as your starting point, Altera recommends following the Advisor guidelines for your Stratix II FPGA until you complete the prototype revision.

When the Stratix II FPGA design is complete, create and switch to your HardCopy II companion revision and follow the Advisor steps shown in that revision until you are finished with the HardCopy II revision and are ready to submit the design to Altera for back-end migration.

Each category in the HardCopy II Advisor list has an explanation of the recommended settings and constraints, as well as quick links to the features in the Quartus II software that are needed for each section. The HardCopy II Advisor displays:

- A green check box when you have successfully completed one of the steps
- A yellow caution sign for steps that must be completed before submitting your design to Altera for HardCopy development
- An information callout for items you must verify

Selecting an item within the HardCopy II flow menu provides a description of the task and recommended action. The view in the HardCopy II Advisor differs depending on the device you select.

Figure 3–17 shows the HardCopy II Advisor with the Stratix II device selected.

Figure 3–17. HardCopy II Advisor with Stratix II Selected

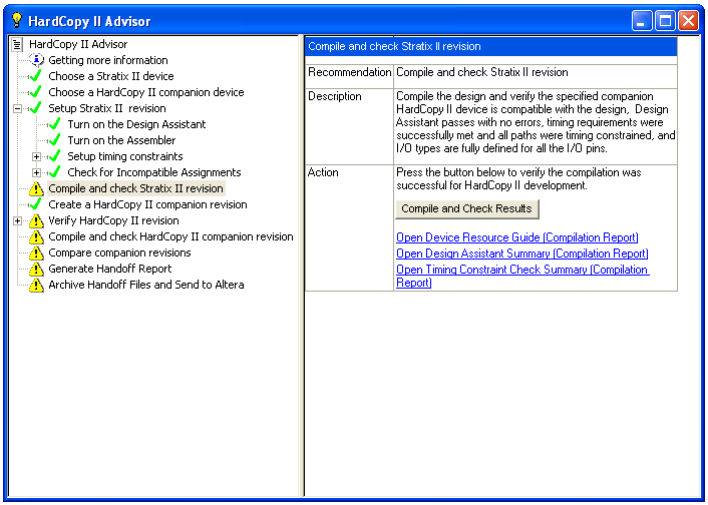
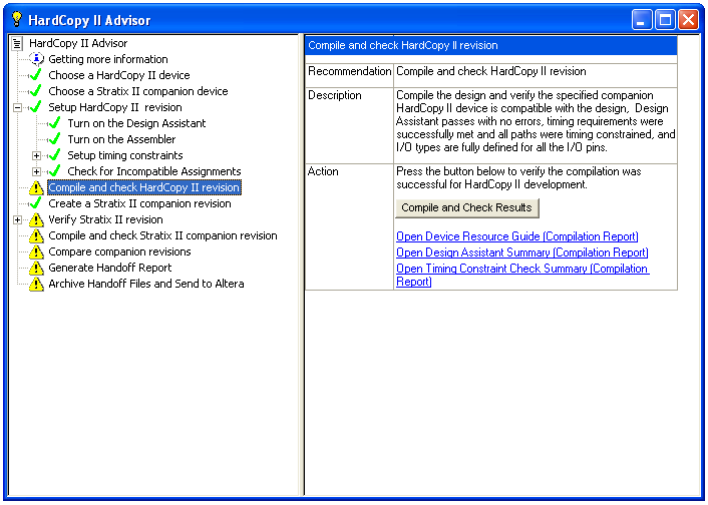


Figure 3–18 shows the HardCopy II Advisor with the HardCopy II device selected.

Figure 3–18. HardCopy II Advisor with HardCopy II Device Selected

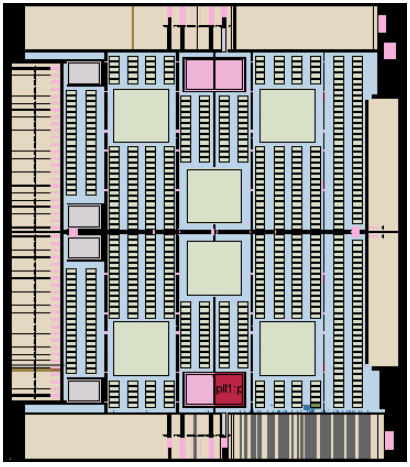


HardCopy II Floorplan View

The Quartus II software displays the preliminary timing closure floorplan and placement of your HardCopy II companion revision. This floorplan shows the preliminary placement and connectivity of all I/O pins, PLLs, memory blocks, HCell macros, and DSP HCell macros. Congestion mapping of routing connections can be viewed using the Bird's Eye viewer settings. This is useful in analyzing densely packed areas of your floorplan that could be reducing the peak performance of your design. The HardCopy Design Center verifies final HCell macro timing and placement to guarantee timing closure is achieved.

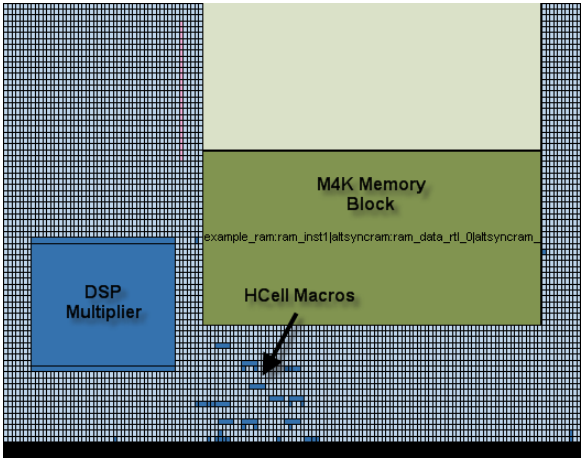
Figure 3–19 shows an example of the HC230F1020 device floorplan.

Figure 3–19. HC230F1020 Device Floorplan



In this small example design, the logic is placed near the bottom edge. You can see the placement of a DSP block constructed of HCell Macros, various logic HCell Macros, and an M4K memory block. A labeled close-up view of this region is shown in Figure 3–20.

Figure 3–20. Close-Up View of Floorplan



The HardCopy Design Center performs final placement and timing closure on your HardCopy II design based on the timing constraints provided in the Stratix II design.

For more information about the HardCopy Design Center's process, refer to the *Back-End Design Flow for HardCopy Series Devices* chapter in volume 1 of the *HardCopy Series Device Handbook*.

Conclusion

You can use the Quartus II software to design HardCopy II devices and to develop prototypes using Stratix II FPGAs. This is done using the standard FPGA development process with the addition of the HardCopy II Device Resource Guide, HardCopy II Companion Devices assignment HardCopy II Utilities, and the HardCopy II Advisor.

The addition of the HardCopy II Advisor to the Quartus II software provides an instrumental development guide for you to complete your HardCopy II and Stratix II device designs. The HardCopy II Utilities included in the Quartus II software provide you with the tools necessary to complete your Stratix II FPGA prototype and HardCopy II structured ASIC design. The addition of the HardCopy II companion revisions feature to the process allows for rapid development and verification that your HardCopy II design is functionally equivalent to your Stratix II FPGA prototype.

HardCopy Stratix Device Support

The Altera HardCopy devices provide a comprehensive alternative to ASICs. HardCopy structured ASICs offer a complete solution from prototype to high-volume production, and maintain the powerful features and high-performance architecture of their equivalent FPGAs with the programmability removed. You can use the Quartus II design software to design HardCopy devices in a manner similar to the traditional ASIC design flow and you can prototype with Altera's high density Stratix, APEX 20KC, and APEX 20KE FPGAs before seamlessly migrating to the corresponding HardCopy device for high-volume production.

HardCopy structured ASICs provide the following key benefits:

- Improves performance, on the average, by 40% over the corresponding -6 speed grade FPGA device
- Lowers power consumption, on the average, by 40% over the corresponding FPGA
- Preserves the FPGA architecture and features, and minimizes risk
- Guarantees first-silicon success through a proven, seamless migration process from the FPGA to the equivalent HardCopy device
- Offers a quick turnaround of the FPGA design to a structured ASIC device—samples are available in about eight weeks

Altera's Quartus II software has built-in support for HardCopy Stratix devices. The HardCopy design flow in Quartus II software offers the following advantages:

- Unified design flow from prototype to production
- Performance estimation of the HardCopy Stratix device allows you to design systems for maximum throughput
- Easy-to-use and inexpensive design tools from a single vendor
- An integrated design methodology that enables system-on-a-chip designs

This section discusses the following areas:

- How to design HardCopy Stratix and HardCopy APEX structured ASICs using the Quartus II software
- An explanation of what the HARDCOPY_FPGA_PROTOTYPE devices are and how to target designs to these devices
- Performance and power estimation of HardCopy Stratix devices
- How to generate the HardCopy design database for submitting HardCopy Stratix and HardCopy APEX designs to the HardCopy Design Center

Features

Beginning with version 4.2, the Quartus II software contains several powerful features that facilitate design of HardCopy Stratix and HardCopy APEX devices:

- **HARDCOPY_FPGA_PROTOTYPE Devices**
  These are virtual Stratix FPGA devices with features identical to HardCopy Stratix devices. You must use these FPGA devices to prototype your designs and verify the functionality in silicon.

- **HardCopy Timing Optimization Wizard**
  Using this feature, you can target your design to HardCopy Stratix devices, providing an estimate of the design's performance in a HardCopy Stratix device.

- **HardCopy Stratix Floorplans and Timing Models**
  The Quartus II software supports post-migration HardCopy Stratix device floorplans and timing models and facilitates design optimization for design performance.

- **Placement Constraints**
  Location and LogicLock™ constraints are supported at the HardCopy Stratix floorplan level to improve overall performance.

- **Improved Timing Estimation**
  Beginning with version 4.2, the Quartus II software determines routing and associated buffer insertion for HardCopy Stratix designs, and provides the Timing Analyzer with more accurate information about the delays than was possible in previous versions of the Quartus II software. The Quartus II Archive File automatically receives buffer insertion information, which greatly enhances the timing closure process in the back-end migration of your HardCopy Stratix device.

- **Design Assistant**
  This feature checks your design for compliance with all HardCopy device design rules and establishes a seamless migration path in the quickest time.

- **HardCopy Files Wizard**
  This wizard enables you to deliver to Altera the design database and all the deliverables required for migration. This feature is used for HardCopy Stratix and HardCopy APEX devices.

The HardCopy Stratix and HardCopy APEX PowerPlay Early Power Estimator is available on the Altera web site at www.altera.com.

HARDCOPY_FPGA_PROTOTYPE, HardCopy Stratix & Stratix Devices

You must use the HARDCOPY_FPGA_PROTOTYPE virtual devices available in the Quartus II software to target your designs to the actual resources and package options available in the equivalent post-migration HardCopy Stratix device. The programming file generated for the HARDCOPY_FPGA_PROTOTYPE can be used in the corresponding Stratix FPGA device.

The purpose of the HARDCOPY_FPGA_PROTOTYPE is to guarantee seamless migration to HardCopy by making sure that your design only uses resources in the FPGA that can be used in the HardCopy device after migration. You can use the equivalent Stratix FPGAs to verify the design's functionality in-system, then generate the design database necessary to migrate to a HardCopy device. This process ensures the seamless migration of the design from a prototyping device to a production device in high volume. It also minimizes risk, assures samples in about eight weeks, and guarantees first-silicon success.

HARDCOPY_FPGA_PROTOTYPE devices are only available for HardCopy Stratix devices and are not available for the HardCopy II or HardCopy APEX device families.

Table 3–3 compares HARDCOPY_FPGA_PROTOTYPE devices, Stratix devices, and HardCopy Stratix devices.

Table 3–3. Qualitative Comparison of HARDCOPY_FPGA_PROTOTYPE to Stratix & HardCopy Stratix Devices

Stratix Device	HARDCOPY_FPGA_PROTOTYPE Device	HardCopy Stratix Device
FPGA	Virtual FPGA	Structured ASIC
FPGA	Architecture identical to Stratix FPGA	Architecture identical to Stratix FPGA
FPGA	Resources identical to HardCopy Stratix device	M-RAM resources different than Stratix FPGA in some devices
Ordered through Altera part number	Cannot be ordered, use the Altera Stratix FPGA part number	Ordered by Altera part number

Table 3–4 lists the resources available in each of the HardCopy Stratix devices.

Table 3–4. HardCopy Stratix Device Physical Resources

Device	LEs	ASIC Equivalent Gates (K) *(1)*	M512 Blocks	M4K Blocks	M-RAM Blocks	DSP Blocks	PLLs	Maximum User I/O Pins
HC1S25F672	25,660	250	224	138	2	10	6	473
HC1S30F780	32,470	325	295	171	2 *(2)*	12	6	597
HC1S40F780	41,250	410	384	183	2 *(2)*	14	6	615
HC1S60F1020	57,120	570	574	292	6	18	12	773
HC1S80F1020	79,040	800	767	364	6 *(2)*	22	12	773

Notes to Table 3–4:
(1) Combinational and registered logic do not include DSP blocks, on-chip RAM, or PLLs.
(2) The M-RAM resources for these HardCopy devices differ from the corresponding Stratix FPGA.

For a given device, the number of available M-RAM blocks in HardCopy Stratix devices is identical with the corresponding HARDCOPY_FPGA_PROTOTYPE devices, but may be different from the corresponding Stratix devices. Maintaining the identical resources between HARDCOPY_FPGA_PROTOTYPE and HardCopy Stratix devices facilitates seamless migration from the FPGA to the structured ASIC device.

For more information about HardCopy Stratix devices, refer to the *HardCopy Stratix Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook.*

The three devices, Stratix FPGA, HARDCOPY_FPGA_PROTOTYPE, and HardCopy device, are distinct devices in the Quartus II software. The HARDCOPY_FPGA_PROTOTYPE programming files are used in the Stratix FPGA for your design. The three devices are tied together with the same netlist, thus a single SRAM Object File (**.sof)** can be used to achieve the various goals at each stage. The same SRAM Object File is generated in the HARDCOPY_FPGA_PROTOTYPE design, and is used to program the Stratix FPGA device, the same way that it is used to generate the HardCopy Stratix device, guaranteeing a seamless migration.

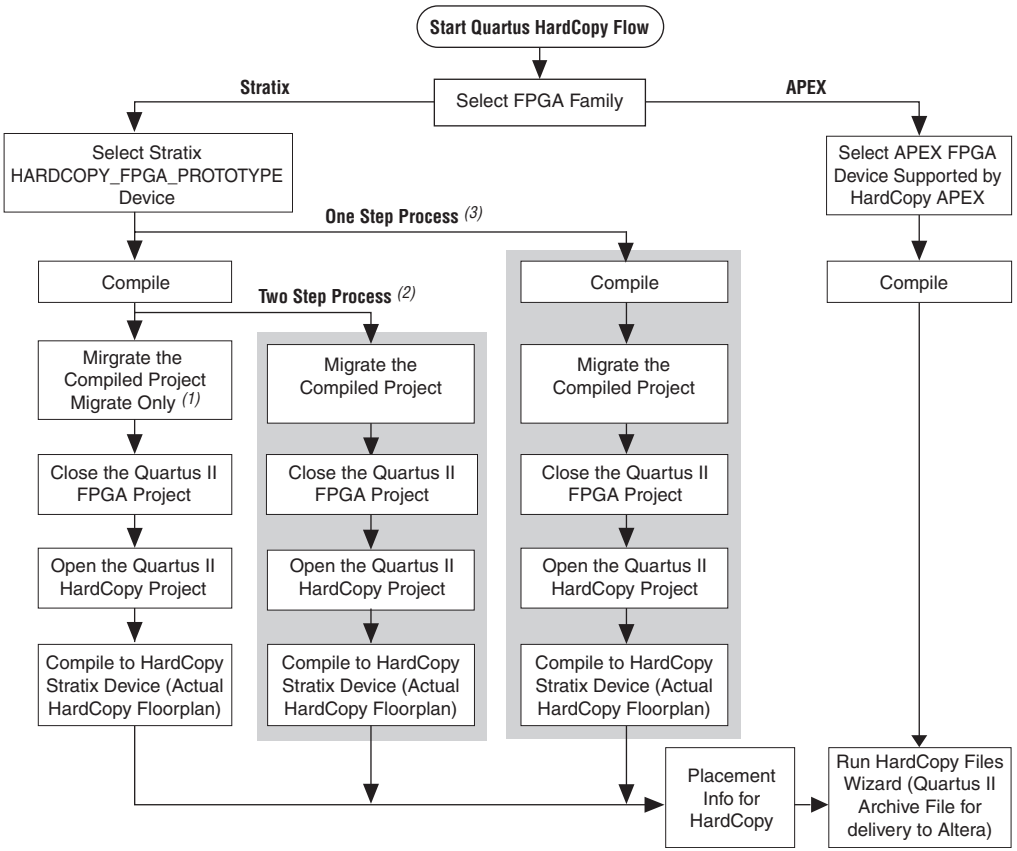
For more information about the SRAM Object File and programming Stratix FPGA devices, refer to the *Programming and Configuration* chapter of the *Introduction to Quartus II Manual*.

HardCopy Design Flow

Figure 3–21 shows a HardCopy design flow diagram. The design steps are explained in detail in the following sections of this chapter. The HardCopy Stratix design flow utilizes the HardCopy Timing Optimization Wizard to automate the migration process into a one-step process. The remainder of this section explains the tasks performed by this automated process.

For a detailed description of the HardCopy Timing Optimization Wizard and HardCopy Files Wizard, refer to "HardCopy Timing Optimization Wizard" on page 3–39 and "Generating the HardCopy Design Database" on page 3–50.

Figure 3–21. HardCopy Stratix & HardCopy APEX Design Flow Diagram



Notes for Figure 3–21:
(1) Migrate-Only Process: The displayed flow is completed manually.
(2) Two-Step Process: Migration and Compilation are done automatically (shaded area).
(3) One-Step Process: Full HardCopy Compilation. The entire process is completed automatically (shaded area).

The Design Flow Steps of the One Step Process

The following sections describe each step of the full HardCopy compilation (the One Step Process), as shown in Figure 3–21.

Compile the Design for an FPGA

This step compiles the design for a HARDCOPY_FPGA_PROTOTYPE device and gives you the resource utilization and performance of the FPGA.

Migrate the Compiled Project

This step generates the Quartus II Project File (**.qpf**) and the other files required for HardCopy implementation. The Quartus II software also assigns the appropriate HardCopy Stratix device for the design migration.

Close the Quartus FPGA Project

Because you must compile the project for a HardCopy Stratix device, you must close the existing project which you have targeted your design to a HARDCOPY_FPGA_PROTOTYPE device.

Open the Quartus HardCopy Project

Open the Quartus II project that you created in the "Migrate the Compiled Project" step. The selected device is one of the devices from the HardCopy Stratix family that was assigned during that step.

Compile for HardCopy Stratix Device

Compile the design for a HardCopy Stratix device. After successful compilation, the Timing Analysis section of the compilation report shows the performance of the design implemented in the HardCopy device.

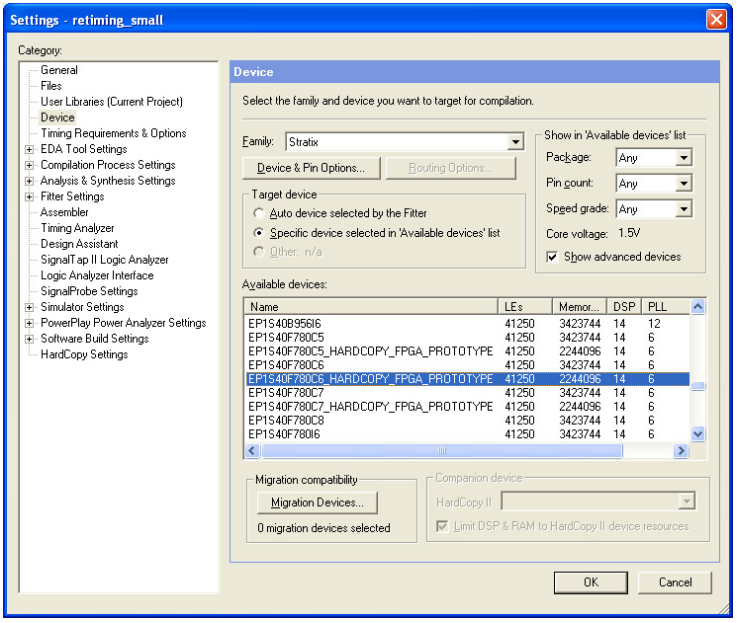
How to Design HardCopy Stratix Devices

This section describes the process for designing for a HardCopy Stratix device using the HARDCOPY_FPGA_PROTOTYPE as your initial selected device. In order to use the HardCopy Timing Optimization Wizard, you must first design with the HARDCOPY_FPGA_PROTOTYPE in order for the design to migrate to a HardCopy Stratix device.

To target a design to a HardCopy Stratix device in the Quartus II software, follow these steps:

1. If you have not yet done so, create a new project or open an existing project.
2. On the Assignments menu, click **Settings**. In the **Category** list, select **Device**.
3. On the **Device** page, in the **Family** list, select **Stratix**. Select the desired HARDCOPY_FPGA_PROTOTYPE device in the **Available Devices** list (Figure 3–22).

Figure 3–22. Selecting a HARDCOPY_FPGA_PROTOTYPE Device



By choosing the HARDCOPY_FPGA_PROTOTYPE device, all the design information, available resources, package option, and pin assignments are constrained to guarantee a seamless migration of your project to the HardCopy Stratix device. The netlist resulting from the HARDCOPY_FPGA_PROTOTYPE device compilation contains information about the electrical connectivity, resources used, I/O placements, and the unused resources in the FPGA device.

4. On the Assignments menu, click **Settings**. In the **Category** list, select **HardCopy Settings** and specify the input transition timing to be modeled for both clock and data input pins. These transition times are used in static timing analysis during back-end timing closure of the HardCopy device.

5. Add constraints to your HARDCOPY_FPGA_PROTOTYPE device, and on the Processing menu, click **Start Compilation** to compile the design.

HardCopy Timing Optimization Wizard

After you have successfully compiled your design in the HARDCOPY_FPGA_PROTOTYPE, you must migrate the design to the HardCopy Stratix device to get a performance estimation of the HardCopy Stratix device. This migration is required before submitting the design to Altera for the HardCopy Stratix device implementation. To perform the required migration, on the Project menu, point to HardCopy Utilities and click **HardCopy Timing Optimization Wizard**.

At this point, you are presented with the following three choices to target the designs to HardCopy Stratix devices (Figure 3–23):

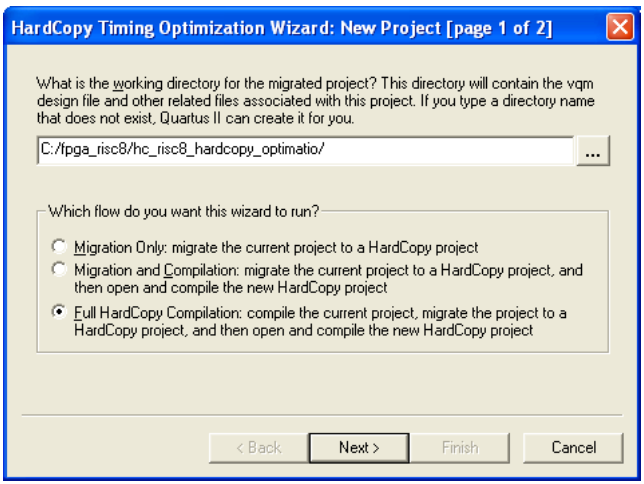
- **Migration Only**: You can select this option after compiling the HARDCOPY_FPGA_PROTOTYPE project to migrate the project to a HardCopy Stratix project.

  You can now perform the following tasks manually to target the design to a HardCopy Stratix device. Refer to"Performance Estimation" on page 3–42 for additional information about how to perform these tasks.
  - Close the existing project
  - Open the migrated HardCopy Stratix project
  - Compile the HardCopy Stratix project for a HardCopy Stratix device

- **Migration and Compilation**: You can select this option after compiling the project. This option results in the following actions:
  - Migrating the project to a HardCopy Stratix project
  - Opening the migrated HardCopy Stratix project and compiling the project for a HardCopy Stratix device

- **Full HardCopy Compilation**: Selecting this option results in the following actions:
  - Compiling the existing HARDCOPY_FPGA_PROTOTYPE project
  - Migrating the project to a HardCopy Stratix project
  - Opening the migrated HardCopy Stratix project and compiling it for a HardCopy Stratix device

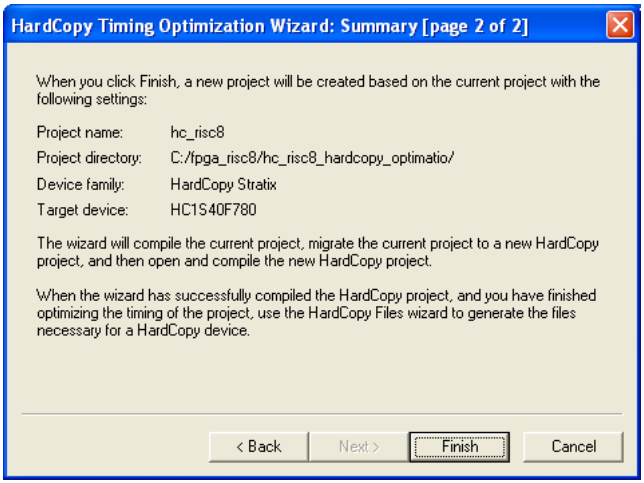
Figure 3–23. HardCopy Timing Optimization Wizard Options



The main benefit of the HardCopy Timing Wizard's three options is flexibility of the conversion process automation. The first time you migrate your HARDCOPY_FPGA_PROTOTYPE project to a HardCopy Stratix device, you may want to use Migration Only, and then work on the HardCopy Stratix project in the Quartus II software. As your prototype FPGA project and HardCopy Stratix project constraints stabilize and you have fewer changes, the Full HardCopy Compilation is ideal for one-click compiling of your HARDCOPY_FPGA_PROTOTYPE and HardCopy Stratix projects.

After selecting the wizard you want to run, the "HardCopy Timing Optimization Wizard: Summary" page shows you details about the settings you made in the Wizard, as shown in Figure 3–24.

Figure 3–24. HardCopy Timing Optimization Wizard Summary Page



When either of the second two options in Figure 3–23 are selected (**Migration and Compilation** or **Full HardCopy Compilation**), designs are targeted to HardCopy Stratix devices and optimized using the HardCopy Stratix placement and timing analysis to estimate performance. For details on the performance optimization and estimation steps, refer to "Performance Estimation" on page 3–42. If the performance requirement is not met, you can modify your RTL source, optimize the FPGA design, and estimate timing until you reach timing closure.

Tcl Support for HardCopy Migration

To complement the GUI features for HardCopy migration, the Quartus II software provides the following command-line executables (which provide the tool command language (Tcl) shell to run the `--flow` Tcl command) to migrate the HARDCOPY_FPGA_PROTOTYPE project to HardCopy Stratix devices:

```
quartus_sh --flow migrate_to_hardcopy <project_name> [-c <revision>] ↵
```

This command migrates the project compiled for the HARDCOPY_FPGA_PROTOTYPE device to a HardCopy Stratix device.

```
quartus_sh --flow hardcopy_full_compile <project_name> [-c <revision>] ↵
```

This command performs the following tasks:

- Compiles the exsisting project for a HARDCOPY_FPGA_PROTOTYPE device.
- Migrates the project to a HardCopy Stratix project.
- Opens the migrated HardCopy Stratix project and compiles it for a HardCopy Stratix device.

Design Optimization & Performance Estimation

The HardCopy Timing Optimization Wizard creates the HardCopy Stratix project in the Quartus II software, where you can perform design optimization and performance estimation of your HardCopy Stratix device.

Design Optimization

Beginning with version 4.2, the Quartus II software supports HardCopy Stratix design optimization by providing floorplans for placement optimization and HardCopy Stratix timing models. These features enable you to refine placement of logic array blocks (LAB) and optimize the HardCopy design further than the FPGA performance. Customized routing and buffer insertion done in the Quartus II software are then used to estimate the design's performance in the migrated device. The HardCopy device floorplan, routing, and timing estimates in the Quartus II software reflect the actual placement of the design in the HardCopy Stratix device, and can be used to see the available resources, and the location of the resources in the actual device.

Performance Estimation

Figure 3–25 illustrates the design flow for estimating performance and optimizing your design. You can target your designs to HARDCOPY_FPGA_PROTOTYPE devices, migrate the design to the HardCopy Stratix device, and get placement optimization and timing estimation of your HardCopy Stratix device.

In the event that the required performance is not met, you can:

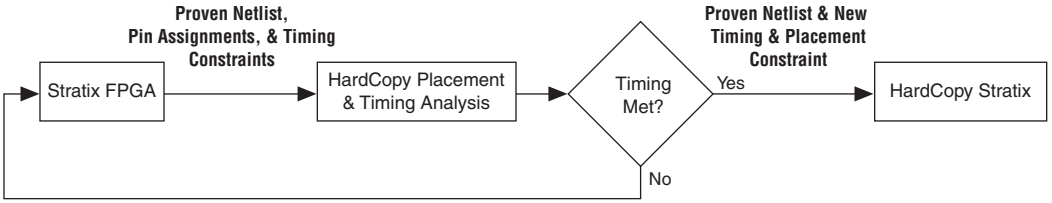
- Work to improve LAB placement in the HardCopy Stratix project.

  or

- Go back to the HARDCOPY_FPGA_PROTOTYPE project and optimize that design, modify your RTL source code, repeat the migration to the HardCopy Stratix device, and perform the optimization and timing estimation steps.

On average, HardCopy Stratix devices are 40% faster than the equivalent -6 speed grade Stratix FPGA device. These performance numbers are highly design dependent, and you must obtain final performance numbers from Altera.

Figure 3–25. Obtaining a HardCopy Performance Estimation



To perform Timing Analysis for a HardCopy Stratix device, follow these steps:

1. Open an existing project compiled for a HARDCOPY_FPGA_PROTOYPE device.

2. On the Project menu, point to HardCopy Utilities and click **HardCopy Timing Optimization Wizard**.

3. Select a destination directory for the migrated project and complete the HardCopy Timing Optimization Wizard process.

   On completion of the HardCopy Timing Optimization Wizard, the destination directory created contains the Quartus II project file, and all files required for HardCopy Stratix implementation. At this stage, the design is copied from the HARDCOPY_FPGA_PROTOTYPE project directory to a new directory to perform the timing analysis. This two-project directory structure enables you to move back and forth between the HARDCOPY_FPGA_PROTOTYPE design database and the HardCopy Stratix design database. The Quartus II software creates the <*project name*>**_hardcopy_optimization** directory.

   You do not have to select the HardCopy Stratix device while performing performance estimation. When you run the HardCopy Timing Optimization Wizard, the Quartus II software selects the HardCopy Stratix device corresponding to the specified HARDCOPY_FPGA_PROTOTYPE FPGA. Thus, the information necessary for the HardCopy Stratix device is available from the earlier HARDCOPY_FPGA_PROTOTYPE device selection.

All constraints related to the design are also transferred to the new project directory. You can modify these constraints, if necessary, in your optimized design environment to achieve the necessary timing closure. However, if the design is optimized at the HARDCOPY_FPGA_PROTOTYPE device level by modifying the RTL code or the device constraints, you must migrate the project with the HardCopy Timing Optimization Wizard.

If an existing project directory is selected when the HardCopy Timing Optimization Wizard is run, the existing information is overwritten with the new compile results.

The project directory is the directory that you chose for the migrated project. A snapshot of the files inside the <*project name*>**_hardcopy_optimization** directory is shown in Table 3–5.

Table 3–5. Directory Structure Generated by the HardCopy Timing Optimization Wizard

<*project name*>**_hardcopy_optimization**
- <*project name*>**.qsf**
- <*project name*>**.qpf**
- <*project name*>**.sof**
- <*project name*>**.macr**
- <*project name*>**.gclk**
- **db**
- **hardcopy_fpga_prototype**
  - fpga_<*project name*>**_violations.datasheet**
  - fpga_<*project name*>**_target.datasheet**
  - fpga_<*project name*>**_rba_pt_hcpy_v.tcl**
  - fpga_<*project name*>**_pt_hcpy_v.tcl**
  - fpga_<*project name*>**_hcpy_v.sdo**
  - fpga_<*project name*>**_hcpy.vo**
  - fpga_<*project name*>**_cpld.datasheet**
  - fpga_<*project name*>**_cksum.datasheet**
  - fpga_<*project name*>**.tan.rpt**
  - fpga_<*project name*>**.map.rpt**
  - fpga_<*project name*>**.map.atm**
  - fpga_<*project name*>**.fit.rpt**
  - fpga_<*project name*>**.db_info**
  - fpga_<*project name*>**.cmp.xml**
  - fpga_<*project name*>**.cmp.rcf**
  - fpga_<*project name*>**.cmp.atm**
  - fpga_<*project name*>**.asm.rpt**
  - fpga_<*project name*>**.qarlog**
  - fpga_<*project name*>**.qar**
  - fpga_<*project name*>**.qsf**
  - fpga_<*project name*>**.pin**
  - fpga_<*project name*>**.qpf**
- **db_export**
  - <*project name*>**.map.atm**
  - <*project name*>**.map.hdbx**
  - <*project name*>**.db_info**

4. Open the migrated Quartus II project created in Step 3.

5. Perform a full compilation.

   After successful compilation, the Timing Analysis section of the Compilation Report shows the performance of the design.

Performance estimation is not supported for HardCopy APEX devices in the Quartus II software. Your design can be optimized by modifying the RTL code or the FPGA design and the constraints. You should contact Altera to discuss any desired performance improvements with HardCopy APEX devices.

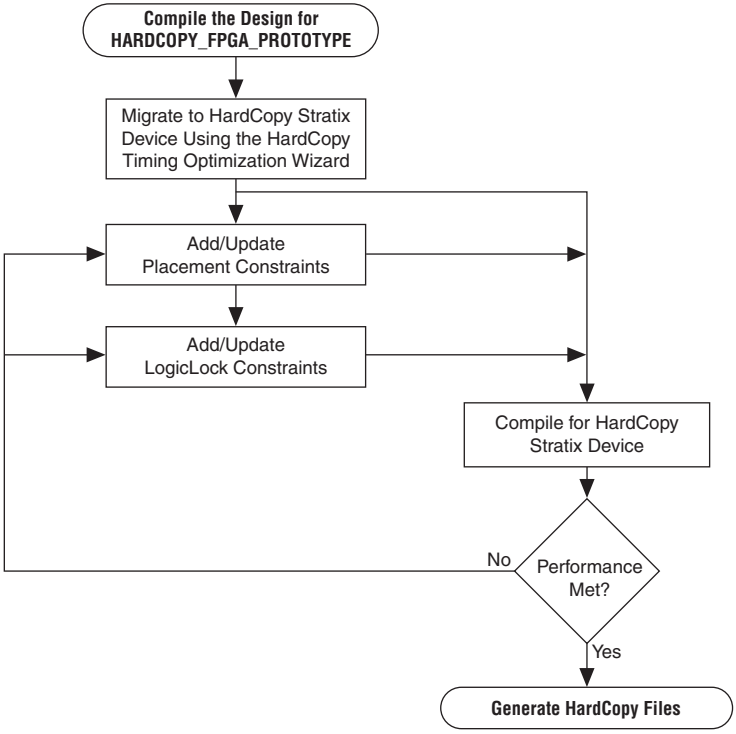
Buffer Insertion

Beginning with version 4.2, the Quartus II software provides improved HardCopy Stratix device timing closure and estimation, to more accurately reflect the results expected after back-end migration. The Quartus II software performs the necessary buffer insertion in your HardCopy Stratix device during the Fitter process, and stores the location of these buffers and necessary routing information in the Quartus II Archive File. This buffer insertion improves the estimation of the Quartus II Timing Analyzer for the HardCopy Stratix device.

Placement Constraints

Beginning with version 4.2, the Quartus II software supports placement constraints and LogicLock regions for HardCopy Stratix devices. Figure 3–26 shows an iterative process to modify the placement constraints until the best placement for the HardCopy Stratix device is achieved.

Figure 3–26. Placement Constraints Flow for HardCopy Stratix Devices



Location Constraints

This section provides information about HardCopy Stratix logic location constraints.

LAB Assignments

Logic placement in HardCopy Stratix is limited to LAB placement and optimization of the interconnecting signals between them. In a Stratix FPGA, individual logic elements (LE) are placed by the Quartus II Fitter into LABs. The HardCopy Stratix migration process requires that LAB contents cannot change after the Timing Optimization Wizard task is done. Therefore you can only make LAB-level placement optimization and location assignments after migrating the HARDCOPY_FPGA_PROTOTYPE project to the HardCopy Stratix device.

The Quartus II software supports these LAB location constraints for HardCopy Stratix devices. The entire contents of a LAB is moved to an empty LAB when using LAB location assignments. If you want to move the logic contents of LAB A to LAB B, the entire contents of LAB A are moved to an empty LAB B. For example, the logic contents of LAB_X33_Y65 can be moved to an empty LAB at LAB_X43_Y56 but individual logic cell LC_X33_Y65_N1 can not be moved by itself in the HardCopy Stratix Timing Closure Floorplan.

LogicLock Assignments

The LogicLock feature of the Quartus II software provides a block-based design approach. Using this technique you can partition your design and create each block of logic independently, optimize placement and area, and integrate all blocks into the top level design.

To learn more about this methodology, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

LogicLock constraints are supported when you migrate the project from a HARDCOPY_FPGA_PROTOTYPE project to a HardCopy Stratix project. If the LogicLock region was specified as "Size=Fixed" and "Location=Locked" in the HARDCOPY_FPGA_PROTOTYPE project, it is converted to have "Size=Auto" and "Location=Floating" as shown in the following LogicLock examples. This modification is necessary because the floorplan of a HardCopy Stratix device is different from that of the Stratix device, and the assigned coordinates in the HARDCOPY_FPGA_PROTOTYPE do not match the HardCopy Stratix floorplan. If this modification did not occur, LogicLock assignments would lead to incorrect placement in the Quartus II Fitter. Making the regions auto-size and floating, maintains your LogicLock assignments, allowing you to easily adjust the LogicLock regions as required and lock their locations again after HardCopy Stratix placement.

Example 3–1 and Example 3–2 show two examples of LogicLock assignments.

Example 3–1. LogicLock Region Definition in the HARDCOPY_FPGA_PROTOTYPE Quartus II Settings File

```
set_global_assignment -name LL_HEIGHT 15 -entity risc8 -section_id test
set_global_assignment -name LL_WIDTH 15 -entity risc8 -section_id test
set_global_assignment -name LL_STATE LOCKED -entity risc8 -section_id test
set_global_assignment -name LL_AUTO_SIZE OFF -entity risc8 -section_id test
```

Example 3–2. LogicLock Region Definition in the Migrated HardCopy Stratix Quartus II Settings File

```
set_global_assignment -name LL_HEIGHT 15 -entity risc8 -section_id test
set_global_assignment -name LL_WIDTH 15 -entity risc8 -section_id test
set_global_assignment -name LL_STATE FLOATING -entity risc8 -section_id
test
set_global_assignment -name LL_AUTO_SIZE ON -entity risc8 -section_id test
```

Checking Designs for HardCopy Design Guidelines

When you develop a design with HardCopy migration in mind, you must follow Altera recommended design practices that ensure a straightforward migration process or the design will not be able to be implemented in a HardCopy device. Prior to starting migration of the design to a HardCopy device, you must review the design and identify and address all the design issues. Any design issues that have not been addressed can jeopardize silicon success.

Altera-Recommended HDL Coding Guidelines

Designing for Altera PLD, FPGA, and HardCopy structured ASIC devices requires certain specific design guidelines and hardware description language (HDL) coding style recommendations be followed.

For more information about design recommendations and HDL coding styles, refer to the *Design Guidelines* Section in volume 1 of the *Quartus II Handbook*.

Design Assistant

The Quartus II software includes the Design Assistant feature to check your design against the HardCopy design guidelines. Some of the design rule checks performed by the Design Assistant include the following rules:

- Design should not contain combinational loops
- Design should not contain delay chains
- Design should not contain latches

To use the Design Assistant, you must have at least run Analysis and Synthesis on the design in the Quartus II software. Altera recommends that you run the Design Assistant to check for compliance with the HardCopy design guidelines early in the design process and after every compilation.

Design Assistant Settings

You must select the design rules in the **Design Assistant** page prior to running the design. On the Assignments menu, click **Settings**. In the **Settings** dialog box, in the Category list, select **Design Assistant** and turn on **Run Design Assistant during compilation**. Altera recommends enabling this feature to run the Design Assistant automatically during compilation of your design.

Running Design Assistant

To run Design Assistant independently of other Quartus II features, on the Processing menu, point to Start and click **Start Design Assistant**.

The Design Assistant automatically runs in the background of the Quartus II software when the HardCopy Timing Optimization Wizard is launched, and does not display the Design Assistant results immediately to the display. The design is checked before the Quartus II software migrates the design and creates a new project directory for performing timing analysis.

Also, the Design Assistant runs automatically whenever you generate the HardCopy design database with the HardCopy Files Wizard. The Design Assistant report generated is used by the Altera HardCopy Design Center to review your design.

Reports & Summary

The results of running the Design Assistant on your design are available in the Design Assistant Results section of the Compilation Report. The Design Assistant also generates the summary report in the <*project name*>**hardcopy** subdirectory of the project directory. This report file is titled <*project name*>**_violations.datasheet**. Reports include the settings, run summary, results summary, and details of the results and messages. The Design Assistant report indicates the rule name, severity of the violation and the circuit path where any violation occurred.

To learn about the design rules and standard design practices to comply with HardCopy design rules, refer to the Quartus II Help and the *HardCopy Series Design Guidelines* chapter in volume 1 of the *HardCopy Series Handbook*.

Generating the HardCopy Design Database

You can use the HardCopy Files Wizard to generate the complete set of deliverables required for migrating the design to a HardCopy device in a single click. The HardCopy Files Wizard asks questions related to the design and archives your design, settings, results, and database files for delivery to Altera. Your responses to the design details are stored in *<project name>*_**hardcopy_optimization***<project name>*.**hps.txt**.

You can generate the archive of the HardCopy design database only after compiling the design to a HardCopy Stratix device. The Quartus II Archive File is generated at the same directory level as the targeted project, either before or after optimization.

The Design Assistant automatically runs when the HardCopy Files Wizard is started.

Table 3–6 shows the archive directory structure and files collected by the HardCopy Files Wizard.

Table 3–6. HardCopy Stratix Design Files Collected by the HardCopy Files Wizard

<*project name*>**_hardcopy_optimization**
- <*project name*>**.flow.rpt**
- <*project name*>**.qpf**
- <*project name*>**.asm.rpt**
- <*project name*>**.blf**
- <*project name*>**.fit.rpt**
- <*project name*>**.gclk**
- <*project name*>**.hps.txt**
- <*project name*>**.macr**
- <*project name*>**.pin**
- <*project name*>**.qsf**
- <*project name*>**.sof**
- <*project name*>**.tan.rpt**

hardcopy
- <*project name*>**.apc**
- <*project name*>**_cksum.datasheet**
- <*project name*>**_cpld.datasheet**
- <*project name*>**_hcpy.vo**
- <*project name*>**_hcpy_v.sdo**
- <*project name*>**_pt_hcpy_v.tcl**
- <*project name*>**_rba_pt_hcpy_v.tcl**
- <*project name*>**_target.datasheet**
- <*project name*>**_violations.datasheet**

hardcopy_fpga_prototype
- fpga_<*project name*>**.asm.rpt**
- fpga_<*project name*>**.cmp.rcf**
- fpga_<*project name*>**.cmp.xml**
- fpga_<*project name*>**.db_info**
- fpga_<*project name*>**.fit.rpt**
- fpga_<*project name*>**.map.atm**
- fpga_<*project name*>**.map.rpt**
- fpga_<*project name*>**.pin**
- fpga_<*project name*>**.qsf**
- fpga_<*project name*>**.tan.rpt**
- fpga_<*project name*>**_cksum.datasheet**
- fpga_<*project name*>**_cpld.datasheet**
- fpga_<*project name*>**_hcpy.vo**
- fpga_<*project name*>**_hcpy_v.sdo**
- fpga_<*project name*>**_pt_hcpy_v.tcl**
- fpga_<*project name*>**_rba_pt_hcpy_v.tcl**
- fpga_<*project name*>**_target.datasheet**
- fpga_<*project name*>**_violations.datasheet**

db_export
- <*project name*>**.db_info**
- <*project name*>**.map.atm**
- <*project name*>**.map.hdbx**

After creating the migration database with the HardCopy Timing Optimization Wizard, you must compile the design before generating the project archive. You will receive an error if you create the archive before compiling the design.

Static Timing Analysis

In addition to performing timing analysis, the Quartus II software also provides all of the requisite netlists and Tcl scripts to perform static timing analysis (STA) using the Synopsys STA tool, PrimeTime. The following files, necessary for timing analysis with the PrimeTime tool, are generated by the HardCopy Files Wizard:

- <*project name*>**_hcpy.vo**—Verilog HDL output format
- <*project name*>**_hpcy_v.sdo**—Standard Delay Format Output File
- <*project name*>**_pt_hcpy_v.tcl**—Tcl script

These files are available in the <*project name*>**\hardcopy** directory. PrimeTime libraries for the HardCopy Stratix and Stratix devices are included with the Quartus II software.

Use the HardCopy Stratix libraries for PrimeTime to perform STA during timing analysis of designs targeted to HARDCOPY_FPGA_PROTOTYPE device.

For more information about static timing analysis, refer to the *Classic Timing Analyzer* and the *Synopsys PrimeTime Support* chapters in volume 3 of the *Quartus II Handbook*.

Early Power Estimation

You can use PowerPlay Early Power Estimation to estimate the amount of power your HardCopy Stratix or HardCopy APEX device will consume. This tool is available on the Altera web site. Using the Early Power Estimator requires some knowledge of your design resources and specifications, including:

- Target device and package
- Clock networks used in the design
- Resource usage for LEs, DSP blocks, PLL, and RAM blocks
- High speed differential interfaces (HSDI), general I/O power consumption requirements, and pin counts
- Environmental and thermal conditions

HardCopy Stratix Early Power Estimation

The PowerPlay Early Power Estimator provides an initial estimate of I_{CC} for any HardCopy Stratix device based on typical conditions. This calculation saves significant time and effort in gaining a quick understanding of the power requirements for the device. No stimulus vectors are necessary for power estimation, which is established by the clock frequency and toggle rate in each clock domain.

This calculation should only be used as an estimation of power, not as a specification. The actual I_{CC} should be verified during operation because this estimate is sensitive to the actual logic in the device and the environmental operating conditions.

For more information about simulation-based power estimation, refer to the *Power Estimation & Analysis* Section in volume 3 of the *Quartus II Handbook*.

On average, HardCopy Stratix devices are expected to consume 40% less power than the equivalent FPGA.

HardCopy APEX Early Power Estimation

The PowerPlay Early Power Estimator can be run from the Altera web site in the device support section (**http://www.altera.com/support/devices/dvs-index.html**). You cannot open this feature in the Quartus II software.

With the HardCopy APEX PowerPlay Early Power Estimator, you can estimate the power consumed by HardCopy APEX devices and design systems with the appropriate power budget. Refer to the web page for instructions on using the HardCopy APEX PowerPlay Early Power Estimator.

HardCopy APEX devices are generally expected to consume about 40% less power than the equivalent APEX 20KE or APEX 20KC FPGA devices.

Tcl Support for HardCopy Stratix

The Quartus II software also supports the HardCopy Stratix design flow at the command prompt using Tcl scripts.

For details on Quartus II support for Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Targeting Designs to HardCopy APEX Devices

Beginning with version 4.2, the Quartus II software supports targeting designs to HardCopy APEX device families. After compiling your design for one of the APEX 20KC or APEX 20KE FPGA devices supported by a HardCopy APEX device, run the HardCopy Files Wizard to generate the necessary set of files for HardCopy migration.

The HardCopy APEX device requires a different set of design files for migration than HardCopy Stratix. Table 3–7 shows the files collected for HardCopy APEX by the HardCopy Files Wizard.

Table 3–7. HardCopy APEX Files Collected by the HardCopy Files Wizard

<*project name*>**.tan.rpt**
<*project name*>**.asm.rpt**
<*project name*>**.fit.rpt**
<*project name*>**.hps.txt**
<*project name*>**.map.rpt**
<*project name*>**.pin**
<*project name*>**.sof**
<*project name*>**.qsf**
<*project name*>**_cksum.datasheet**
<*project name*>**_cpld.datasheet**
<*project name*>**_hcpy.vo**
<*project name*>**_hcpy_v.sdo**
<*project name*>**_pt_hcpy_v.tcl**
<*project name*>**_rba_pt_hcpy_v.tcl**
<*project name*>**_target.datasheet**
<*project name*>**_violations.datasheet**

Refer to "Generating the HardCopy Design Database" on page 3–50 for information about generating the complete set of deliverables required for migrating the design to a HardCopy APEX device. After you have successfully run the HardCopy Files Wizard, you can submit your design archive to Altera to implement of your design in a HardCopy device. You should contact Altera for more information about this process.

Conclusion

The methodology for designing HardCopy Stratix devices using the Quartus II software is the same as that for designing the Stratix FPGA equivalent. You can use the familiar Quartus II software tools and design flow, target designs to HardCopy Stratix devices, optimize designs for higher performance and lower power consumption than the Stratix FPGAs, and deliver the design database for migration to a HardCopy Stratix device. Compatible APEX FPGA designs can migrate to HardCopy APEX after compilation using the HardCopy Files Wizard to archive the design files. Submit the files to the HardCopy Design Center to complete the back-end migration.

Related Documents

For more information, refer to the following documentation:

- The *HardCopy Series Design Guidelines* chapter in volume 1 of the *HardCopy Series Handbook*
- The *HardCopy Series Back-End Timing Closure* chapter in volume 1 of the *HardCopy Series Handbook*

4. Engineering Change Management

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Introduction

A major benefit of programmable logic is that it accommodates changes to the system specification late in the design cycle. In a typical engineering project development cycle, the specification for the programmable logic portion is likely to change when engineering development begins or when integrating all system elements.

Last-minute design changes, commonly referred to as engineering change orders (ECOs), are defined as small changes to the functionality of a design, after the design has been fully compiled; that is, when synthesis and place-and-route are completed.

ECOs are usually intended to correct errors found in the programmable logic design during debugging, or to facilitate changes that are made to the design specification to compensate for design problems that are introduced while integrating components of your system design. As a project nears completion, a significant amount of time has been invested in maximizing performance and design verification; therefore, it is important that your ECO changes affect specific parts of your design and have minimal impact on unrelated parts of your design.

This chapter addresses the impact that ECOs have, and explains how to resolve these issues using the Quartus® II software.

Impact of Last Minute Design Changes

ECOs have an impact on the following areas of a system design:

- Performance
- Compile time
- Verification
- Documentation

Performance

When making a small change to the design functionality, the result can be a loss of previous design optimizations. Typical examples of design optimizations are floorplan optimizations and physical synthesis. Ideally, there should be a means to preserve previous design optimizations. This would focus future optimizations only to design areas where ECO changes occurred.

Compilation Time

In the traditional programmable logic design flow, a small change in the design necessarily results in a complete recompilation of the design; that is, synthesis and place-and-route. Making small changes to the design to reach the final implementation on a board can be a very long process. Ideally, to reach the desired functionality and to reach timing closure, a small change in functionality should result in reduced compilation time. You can achieve this by the incremental compilation feature, which uses the previous fit information on unchanged areas of the design.

Verification

After a design change, you must verify the impact of the change on your design. You can verify your design by performing timing analysis and simulation. You can choose to limit the verification to the area of the design impacted by the ECOs. To do this, run timing analysis on select paths and perform the simulation on gate level and timing simulation netlists.

Documentation

You must track changes to your project files. Tracking changes provides the ability to reproduce your results. Ideally, you can have multiple compilation revisions so that others can try the changes without corrupting the previous results.

ECO Support

You can apply ECOs at two stages in a typical design flow:

- HDL level
- Netlist level

Historically, in programmable logic designs, you would apply ECOs at the HDL level. The reason for this was the lack of tools for PLDs that could easily create ECOs and enable design sign-off at the netlist level.

ECO Support at the HDL Level

An ECO at the HDL level is a change to the design's Verilog HDL or VHDL source. This change may range from a single line to several lines of code modified within a module or entity. Typical examples of such modifications include:

- Changing the state encoding of a finite state machine
- Adding pipeline registers to improve design performance

- Duplicating the signal to reduce fan-out
- Adding a term to a conditional expression
- Changing the polarity of a register control signal

A few changes to the source code can produce many changes to the netlist produced by other EDA synthesis or tools such as the Quartus II software's integrated synthesis. During the synthesis process, the synthesis tools generally preserve the names of registers from the HDL source code, but automatically generate names for the combinational (look-up table level, or LUT level) nodes. This automatic name generation is necessary to accommodate the synthesis optimization performed on the HDL source to use the target device resources more efficiently.

A minor source code change can result in many changes to the names in the synthesis netlist. The changes in the synthesis netlist can be caused by the node names in the new netlist implementing a different functionality than in the previous netlist, or by implementing the same functionality as in the previous netlist, but have different names.

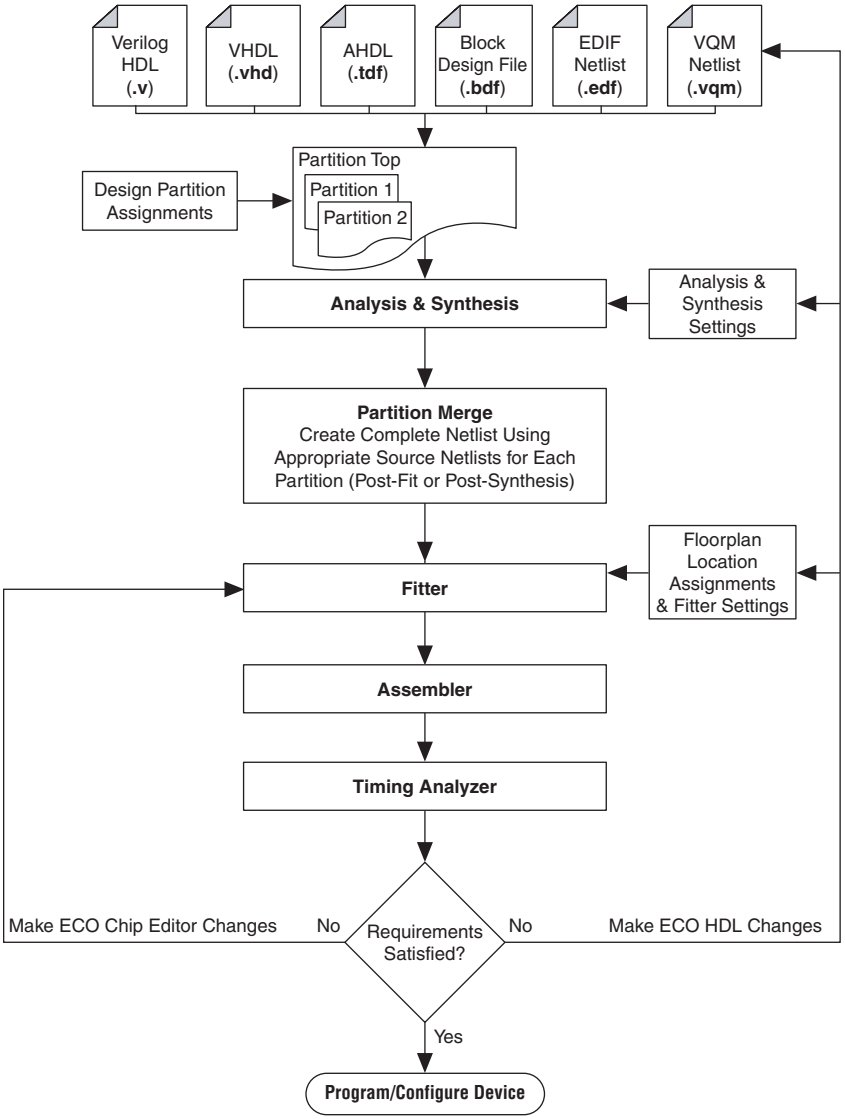
To leverage previous design optimizations and to reduce compilation time, there must be a way to perform incremental compilation on the modules with the new functionality to preserve the previous optimizations. The incremental compilation feature available in the Quartus II software provides a solution to this problem.

With Quartus II incremental compilation, you can preserve results and performance of unchanged logic in your design as you make ECOs elsewhere. The incremental compilation feature enables you to reduce design iteration time up to 70%, and reach timing closure more efficiently. Incremental compilation facilitates block-based design, and allows you to preserve performance for unchanged blocks of the design. You can also target optimization techniques, such as physical synthesis, to specific design blocks while leaving other blocks untouched.

A hierarchical design is flattened into a single netlist before logic synthesis and fitting; therefore, the entire design is recompiled every time the design changes. However, the incremental compilation feature allows you to partition a design along any of its hierarchical boundaries. The Quartus II software separately synthesizes and fits each individual hierarchical design partition. The Quartus II software combines or merges the design partitions to form a netlist for subsequent stages of the Quartus II compilation flow.

Figure 4–1 details the recommended design flow to support ECO changes at the HDL level.

Figure 4–1. Design Flow to Support ECO Changes



ECO Support at the Netlist Level

For some ECO changes, making changes at the netlist level can be faster than at the HDL level. This happens when you are debugging the design on silicon and need a very fast turnaround to generate a programming file for debugging the system.

A typical application occurs when you uncover a problem on the board and isolate the problem to the appropriate nodes or I/O cells on the PLD. You then need to be able to quickly correct the functionality of the offending logic cell or the properties of the I/O cell and generate a new programming file. In doing this, you can verify the operation of the change without having to modify the HDL and perform a synthesis and place-and-route operation. This minimizes the disruption to the board verification procedure.

If this quick fix works, you do not need to change the HDL source code and rerun place-and-route. You should have the option to:

- Document the change that has been made
- Easily recreate the steps taken to produce the changes to the design
- Generate EDA simulation netlists for verification of the design
- Perform timing analysis on the design

The Chip Editor feature of the Quartus II software provides these capabilities.

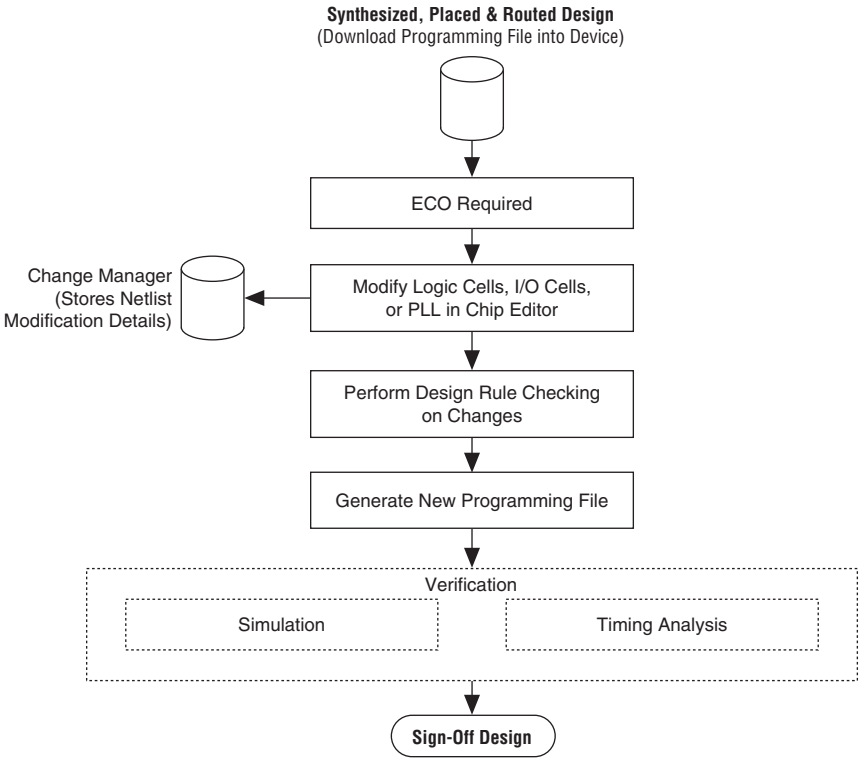
The Quartus II Chip Editor allows you to make functional changes to individual logic cells and to the I/O cell and phase-locked loop (PLL) parameters. These changes are stored in the Quartus II Change Manager log. This allows you to control the application of the changes, and generate a tool command language (Tcl) file.

The Tcl commands file recreates the changes on the original netlist and documents the project changes. This provides the ability to recreate the changes on the original design files without having to change the HDL source. You can regenerate an EDA simulation netlist for the modified design if it is necessary to perform a gate-level simulation of the modified design. If you should rerun timing analysis to sign-off the design, you can rerun timing analysis on the netlist containing the ECO changes.

For more information, refer to the *Design Analysis and Engineering Change Management with Chip Editor* chapter in volume 3 of the *Quartus II Handbook*.

Figure 4–2 shows the flow for ECO changes at the netlist level.

Figure 4–2. Design Flow for ECO Changes at the Netlist Level



Conclusion

Support for ECOs requires a combination of a modular design methodology and the appropriate software design tools.

The Quartus II software provides you with the software tools and the design methodology to perform successful ECOs at both the HDL and netlist level for programmable logic designs. This reduces the design cycle time and provides faster timing closure on designs that require last-minute changes.

Section II. Design Guidelines

Today's programmable logic device (PLD) applications have reached the complexity and performance requirements of ASICs. In the development of such complex system designs, good design practices have an enormous impact on your device's timing performance, logic utilization, and system reliability. Designs coded optimally will behave in a predictable and reliable manner, even when re-targeted to different device families or speed grades. This section presents design and coding style recommendations for Altera® devices.

This section includes the following chapters:

- Chapter 5, Design Recommendations for Altera Devices
- Chapter 6, Recommended HDL Coding Styles
- Chapter 7 moved to Volume 2

Revision History

The following table shows the revision history for Chapters 5 to 6.

Chapter(s)	Date / Version	Changes Made
5	May 2006 v6.0.0	Minor updates for the Quartus II version 6.0.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v.5.0.0	Chapter 5 was formerly Chapter 4 in version 4.2.
	Dec. 2004 v2.1	Updated for Quartus II software version 4.2: ● Chapter 5 was formerly Chapter 6 in version 4.1. ● General formatting and editing updates. ● Updated hardware requirements for the Quartus II Timing Analyzer. ● Added timing requirements and analysis details. ● Updated Design Guidelines. ● Added information about performing timing analysis on asynchronous ports. ● Added inferred latches information. ● Updated Delay Chains description. ● Updated figures, tables. ● Added Clocking Schemes information. ● Added details to Multiplexed Clocks details. ● Added clock gating details. ● Updated Hierarchical Design Partitioning to include synthesis and incremental synthesis. ● Added global routing information.
	June 2004 v.2.0	● Updates to tables, figures, coding examples. ● New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.
6	May 2006 v6.0.0	Updated for the Quartus II version 6.0: ● Added inferring Altera Megafunctions from HDL code information. ● Added coding guidelines for other logic structures.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v.5.0.0	Chapter 6 was formerly Chapter 5 in version 4.2
	Dec. 2004 v2.1	● Chapter 6 was formerly Chapter 7 in version 4.1. ● Updates to tables, figures. ● New functionality for Quartus II software 4.2.
	June 2004 v2.0	● Updates to tables, figures. ● Added and updated State Machines. ● Update to Verilog HDL for State Machines. ● New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.

Chapter(s)	Date / Version	Changes Made
7	October 2005 v5.1.0	• Chapter now resides in Volume 2, Section III, Chapter 9: Power Optimization
	August 2005 v.5.0.1	• Updates to tables, figures. • Added Standard Fir-Fitter Effort section. • Updated information.
	May 2005 v.5.0.0	Initial release.

5. Design Recommendations for Altera Devices

QII51006-6.0.0

Introduction

Today's FPGA applications have reached the complexity and performance requirements of ASICs. In the development of such complex system designs, good design practices have an enormous impact on your device's timing performance, logic utilization, and system reliability. Well-coded designs behave in a predictable and reliable manner even when re-targeted to different families or speed grades. Good design practices also aid in successful design migration between FPGA and HardCopy® or ASIC implementations for prototyping and production.

For optimal performance and reliability and faster time-to-market when designing with Altera® devices, you should:

- Understand the impact of synchronous design practices
- Follow recommended design techniques including hierarchical design partitioning
- Take advantage of the architectural features in the targeted device

For specific HDL coding examples and recommendations, including coding guidelines for targeting dedicated device hardware, such as memory and DSP blocks, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*. For information about migrating designs to HardCopy devices, refer to the *HardCopy Series Design Guidelines* chapter in the *HardCopy Series Handbook*.

Synchronous FPGA Design Practices

The first step in a good design methodology is to understand the implications of your design practices and techniques. This section outlines some of the benefits of optimal synchronous design practices and the hazards involved in other techniques. Good synchronous design practices can help you consistently meet your design goals. Problems with other design techniques can include reliance on propagation delays in a device, incomplete timing analysis, and possible glitches.

In a synchronous design, a clock signal triggers all events. As long as all of the registers' timing requirements are met, a synchronous design behaves in a predictable and reliable manner for all process, voltage, and temperature (PVT) conditions. You can easily target synchronous designs to different device families or speed grades. In addition, if you plan to migrate your design to a high-volume solution such as Altera HardCopy devices, or if you are prototyping an ASIC, then synchronous design practices help ensure successful migration.

Fundamentals of Synchronous Design

In a synchronous design, everything is related to the clock signal. On every active edge of the clock (usually the rising edge), the data inputs of registers are sampled and transferred to outputs. Following an active clock edge, the outputs of combinational logic feeding the data inputs of registers change values. This change triggers a period of instability due to propagation delays through the logic as the signals go through a number of transitions and finally settle to new values. Changes happening on data inputs of registers do not affect the values of their outputs until the next active clock edge.

Because the internal circuitry of registers isolates data outputs from inputs, instability in the combinational logic does not affect the operation of the design as long as the following timing requirements are met:

- Before an active clock edge, the data input has been stable for at least the setup time of the register
- After an active clock edge, the data input remains stable for at least the hold time of the register

When you specify all your clock frequencies and other timing requirements, the Quartus® II Timing Analyzer issues actual hardware requirements for the setup times (t_{SU}) and hold times (t_H) for every pin of your design. By meeting these external pin requirements and following synchronous design techniques, you ensure that you satisfy the setup and hold times for all registers within the Altera device.

To meet setup and hold time requirements on all input pins, any inputs to combinational logic that feeds a register should have a synchronous relationship with the clock of the register. If signals are asynchronous, you can register the signals at the input of the Altera device to help prevent a violation of the required setup and hold times.

When the setup or hold time of a register is violated, the output can be set to an intermediate voltage level between the high and low levels, called a metastable state. In this unstable state, small perturbations like noise in power rails can cause the register to assume either the high or low voltage level resulting in an unpredictable valid state. Various undesirable effects can occur, including increased propagation delays and incorrect output states. In some cases, the output can even oscillate between the two valid states for a relatively long time.

For details about timing requirements and analysis in the Quartus II software, refer to the *Classic Timing Analysis* or the *TimeQuest Timing Analysis* chapters in volume 3 of the *Quartus II Handbook*.

Hazards of Asynchronous Design

In the past, designers have often used asynchronous techniques such as ripple counters or pulse generators in programmable logic device (PLD) designs, enabling them to take "short cuts" to save device resources. Asynchronous design techniques have inherent problems such as relying on propagation delays in a device, which can result in incomplete timing constraints and possible glitches and spikes. Because today's FPGAs provide many high-performance logic gates, registers, and memory, resource and performance trade-offs have changed. Now it is more important to focus on design practices that help you meet design goals consistently than to save device resources using problematic asynchronous techniques.

Some asynchronous design structures rely on the relative propagation delays of signals to function correctly. In these cases, race conditions can arise where the order of signal changes can affect the output of the logic. PLD designs can have varying timing delays, depending on how the design is placed and routed in the device with each compilation. Therefore, it is almost impossible to determine the timing delay associated with a particular block of logic ahead of time. As devices become faster because of device process improvements, the delays in an asynchronous design may decrease, resulting in a design that does not function as expected. Specific examples are provided in "Design Guidelines" on page 5–4. Relying on a particular delay also makes asynchronous designs very difficult to migrate to different architectures, devices, or speed grades.

The timing of asynchronous design structures is often difficult or impossible to model with timing assignments and constraints. If you do not have complete or accurate timing constraints, the timing-driven algorithms used by your synthesis and place-and-route tools may not be able to perform the best optimizations, and reported results may not be complete.

Some asynchronous design structures can generate harmful glitches, which are pulses that are very short compared with clock periods. Most glitches are generated by combinational logic. When the inputs of combinational logic change, the outputs exhibit a number of glitches before they settle to their new values. These glitches can propagate through the combinational logic, leading to incorrect values on the outputs in asynchronous designs. In a synchronous design, glitches on the data inputs of registers are normal events that have no negative consequences because the data is not processed until the clock edge.

Design Guidelines

When designing with hardware description language (HDL) code, understanding how a synthesis tool interprets different HDL design techniques and what results to expect are important. Your design techniques can affect logic utilization and timing performance, as well as the design's reliability. This section discusses some basic design techniques that ensure optimal synthesis results for designs targeted to Altera devices while avoiding several common causes of unreliability and instability. Design your combinational logic carefully to avoid potential problems and pay attention to your clocking schemes so you can maintain synchronous functionality and avoid timing problems.

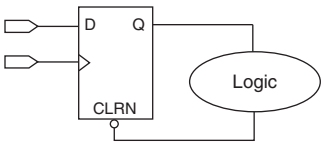
Combinational Logic Structures

Combinational logic structures consist of logic functions that depend only on the current state of the inputs. In Altera FPGAs, these functions are implemented in the look-up tables (LUTs) of the device's architecture, using either logic elements (LE) or adaptive logic modules (ALM). In some cases when combinational logic feeds registers, the register control signals can also be used to implement part of the logic function to save LUT resources. By following the recommendations in this section, you can improve the reliability of your combinational design.

Combinational Loops

Combinational loops are among the most common causes of instability and unreliability in digital designs, and should be avoided whenever possible. In a synchronous design, feedback loops should include registers. Combinational loops generally violate synchronous design principles by establishing a direct feedback loop that contains no registers. For example, a combinational loop occurs when the left-hand side of an arithmetic expression also appears on the right-hand side in HDL code. A combinational loop also occurs when you feed back the output of a register to an asynchronous pin of the same register through combinational logic, as shown in Figure 5–1.

Figure 5–1. Combinational Loop through Asynchronous Control Pin



To perform timing analysis in the Quartus II software on asynchronous ports such as the `clear` or `reset`, on the Assignments menu, click **Settings**. In the Settings dialog box, select **Timing Requirements & Option** and click **More Settings**. Turn on **Enable Recovery/Removal Analysis**.

Combinational loops are inherently high-risk design structures for the following reasons:

- Combinational loop behavior generally depends on the relative propagation delays through the logic involved in the loop. As discussed, propagation delays can change which means the behavior of the loop is unpredictable.
- Combinational loops can cause endless computation loops in many design tools. Most tools break open combinational loops to process the design. The various tools used in the design flow may open a given loop in a different manner, processing it in a way that is inconsistent with the original design intent.

Latches

A latch is a small combinational loop that holds the value of a signal until a new value is assigned. Latches can also be inferred from HDL code when you did not intend to use a latch. FPGA architectures are based on registers. In FPGA devices, latches actually use more logic resources and lead to lower performance than registers. This is different from other device architectures where latches may add less delay and can be implemented with less silicon area than registers.

Latches can cause various difficulties in the design. Although latches are memory elements, they are fundamentally different from registers. When a latch is in feed-through or transparent mode, there is a direct path between the data input and the output. Glitches on the data input can pass through the output. The timing for latches is also inherently ambiguous. For example, when analyzing a design with a D-latch, the software cannot determine whether you intended to transfer data to the output on the leading edge of the clock or on the trailing edge. In many cases, only the original designer knows the full intent of the design; therefore, another designer cannot easily modify the design or reuse the code.

In some cases, your synthesis tool can infer a latch that does not exhibit problems with glitches. Inferring the Altera `lpm_latch` function ensures that the implementation will be glitch-free in Altera architectures. Some third-party synthesis tools list the number of `lpm_latch` functions that are inferred. When using Quartus II integrated synthesis, these latches are reported in a section of the Compilation Report called **User-Specified**

and Inferred Latches. If a latch or combinational loop in your design is not listed in this report, it means that it was not inferred as a "safe" latch by the software and is not considered glitch-free.

However, even glitch-free latches may not be analyzed completely during timing analysis. The Quartus II software provides an option called **Analyze latches as synchronous elements** that allows you to treat latches as start and end points for timing analysis (a typical analysis performed in FPGA design tools). With this option turned on, latches are analyzed as registers (with an inverted clock). The Quartus II software does not perform cycle-borrowing analysis, such as that performed by third-party timing analysis tools like Synopsys PrimeTime.

In addition, latches have a limited support in formal verification tools. Therefore, it is especially important to ensure that you do not use latches when using formal verification.

Altera recommends avoiding using latches to ensure that you can completely analyze and verify the timing performance and reliability of your design.

Delay Chains

Delay chains occur when two or more consecutive nodes with a single fan-in and a single fan-out are used to cause delay. Inverters are often chained together to add delay. Delay chains are sometimes used to resolve race conditions created by other asynchronous design practices.

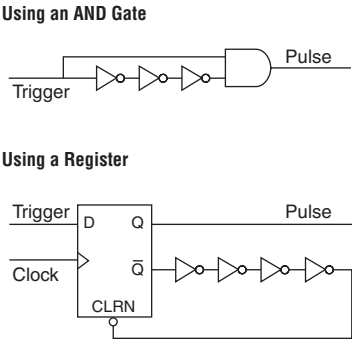
As described above, delays in PLD designs can change with each place-and-route cycle. Effects such as rise/fall time differences and on-chip variation mean that delay chains, especially those placed on clock paths, can cause significant problems in your design. See "Hazards of Asynchronous Design" on page 5–3 for examples of the kinds of problems that delay chains can cause. Avoid using delay chains to prevent these kind of problems.

In some ASIC designs, delays are used for buffering signals as they are routed around the device. This functionality is not needed in FPGA devices because the routing structure provides buffers throughout the device.

Pulse Generators & Multivibrators

Delay chains are sometimes used to generate either one pulse (pulse generators) or a series of pulses (multivibrators). There are two common methods for pulse generation, as shown in Figure 5–2. These techniques are purely asynchronous and therefore should be avoided.

Figure 5–2. Asynchronous Pulse Generators



In "Using an AND Gate" (Figure 5–2), a trigger signal feeds both inputs of a 2-input AND gate, but the design inverts or adds a delay chain to one of the inputs. The width of the pulse depends on the relative delays of the path that feeds the gate directly and the one that goes through the delay. This is the same mechanism responsible for the generation of glitches in combinational logic following a change of input values. This technique artificially increases the width of the glitch by using a delay chain.

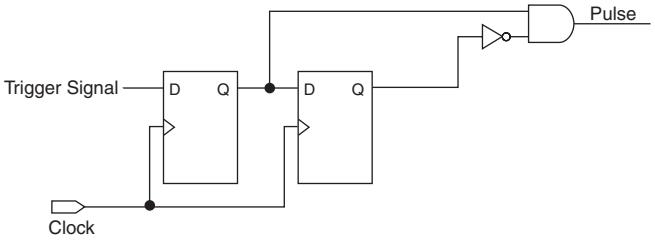
In "Using a Register" (Figure 5–2), a register's output drives the same register's asynchronous reset signal through a delay chain. The register resets itself asynchronously after a certain delay.

The width of pulses generated in this way are difficult for synthesis and place-and-route software to determine, set, or verify. The actual pulse width can only be determined after placement and routing, when routing and propagation delays are known. You cannot reliably determine the width of the pulse when creating HDL code, and it cannot be set by EDA tools. The pulse may not be wide enough for the application under all PVT conditions, and the pulse width changes if you change to a different device. In addition, static timing analysis cannot be used to verify the pulse width, so verification is very difficult.

Multivibrators use a "glitch generator" to create pulses, together with a combinational loop that turns the circuit into an oscillator. This creates additional problems because of the number of pulses involved. In addition, when the structures generate multiple pulses, they also create a new artificial clock in the design that has to be analyzed by the design tools.

When you need to use a pulse generator, use synchronous techniques, as shown in Figure 5–3.

Figure 5–3. Recommended Pulse-Generation Technique



In this design, the pulse width is always equal to the clock period. This pulse generator is predictable, can be verified with timing analysis, and is easily moved to other architectures, devices, or speed grades.

Clocking Schemes

Like combinational logic, clocking schemes have a large effect on your design's performance and reliability. Avoid using internally generated clocks where possible because they can cause functional and timing problems in the design. Clocks generated with combinational logic can introduce glitches that create functional problems, and the delay inherent in combinational logic can lead to timing problems. The following sections provide some specific examples and recommendations for avoiding these problems.

Specify all clock relationships in the Quartus II software to allow for the best timing-driven optimizations during fitting and to allow correct timing analysis. Use clock setting assignments on any derived or internal clocks to specify their relationship to the base clock.

Altera recommends using global device-wide, low-skew dedicated routing for all internally-generated clocks, instead of routing clocks on regular routing lines. See "Clock Network Resources" on page 5–16 for a detailed explanation.

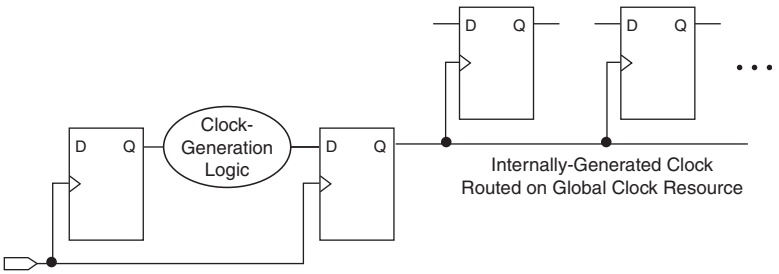
Avoid data transfers between different clocks wherever possible. If a data transfer between different clocks is needed, use FIFO circuitry. You can use the clock uncertainty features in the Quartus II software to compensate for the variable delays between clock domains. Consider setting a Clock Setup Uncertainty and Clock Hold Uncertainty value of 10% to 15% of the clock delay.

Internally Generated Clocks

If you use the output from combinational logic as a clock signal or as an asynchronous reset signal, you should expect to see glitches in your design. In a synchronous design, glitches on data inputs of registers are normal events that have no consequences. However, a glitch or a spike on the clock input (or an asynchronous input) to a register can have significant consequences. Narrow glitches can violate the register's minimum pulse width requirements. Setup and hold times may also be violated if the data input of the register is changing when a glitch reaches the clock input. Even if the design does not violate timing requirements, the register output can change value unexpectedly and cause functional hazards elsewhere in the design.

Because of these problems, always register the output of combinational logic before you use it as a clock signal. See Figure 5–4.

Figure 5–4. Recommended Clock-Generation Technique



Registering the output of combinational logic ensures that the glitches generated by the combinational logic are blocked at the data input of the register.

Divided Clocks

Designs often require clocks created by dividing a master clock. Most Altera FPGAs provide dedicated phase-locked loop (PLL) circuitry for clock division. Using dedicated PLL circuitry can help you to avoid many of the problems that can be introduced by asynchronous clock division logic.

When you need to use logic to divide a master clock, always use synchronous counters or state machines. In addition, create your design so that registers always directly generate divided clock signals, as

described in "Internally Generated Clocks" on page 5–9, and route the clock on global clock resources. To avoid glitches, you should not decode the outputs of a counter or a state machine to generate clock signals.

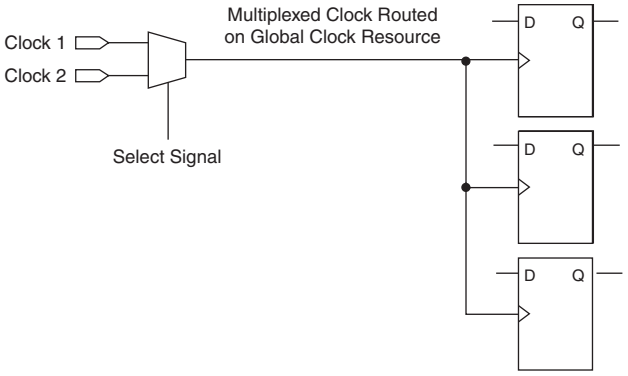
Ripple Counters

Altera recommends avoiding ripple counters in your design to simplify verification. In the past, FPGA designers implemented ripple counters to divide clocks by a power of two because the counters are easy to design and may use fewer gates than their synchronous counterparts. Ripple counters use cascaded registers, in which the output pin of each register feeds the clock pin of the register in the next stage. This cascading can cause problems because the counter creates a ripple clock at each stage. These ripple clocks have to be handled properly during timing analysis, which can be difficult and may require you to make complicated timing assignments in your synthesis and place-and-route tools.

Multiplexed Clocks

Clock multiplexing can be used to operate the same logic function with different clock sources. In these designs, multiplexing selects a clock source, as in Figure 5–5. For example, telecommunications applications that deal with multiple frequency standards often use multiplexed clocks.

Figure 5–5. Multiplexing Logic & Clock Sources



Adding multiplexing logic to the clock signal can create the problems addressed in the previous sections, but requirements for multiplexed clocks vary widely depending on the application. Clock multiplexing is acceptable when the clock signal uses global clock routing resources, if the following criteria are met:

- The clock multiplexing logic does not change after initial configuration
- The design uses multiplexing logic to select a clock for testing purposes
- Registers are always reset when the clock switches
- A temporarily incorrect response following clock switching has no negative consequences

If the design switches clocks in real time with no reset signal, and your design cannot tolerate a temporarily incorrect response, then you must use a synchronous design so that there are no timing violations on the registers, no glitches on clock signals, and no race conditions or other logical problems. By default, the Quartus II software optimizes and analyses all possible paths through the multiplexer and between both internal clocks that may come from the multiplexer. This may lead to more restrictive analysis than required if the multiplexer is always selecting one particular clock. If you do not need the more complete analysis, you can assign the output of the multiplexer as a base clock in the Quartus II software, so that all register-register paths are analyzed using that clock.

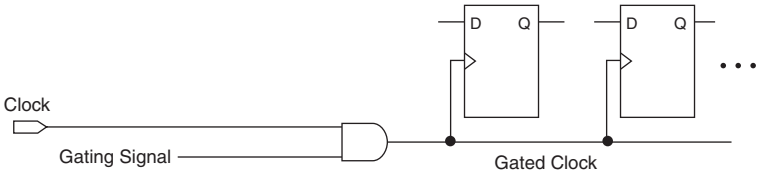
Altera recommends using dedicated hardware to perform clock multiplexing when it is available, instead of using multiplexing logic. For example, you can use the Clock Switchover feature of the PLL in the Stratix® series of devices, or the Clock Control Block in Stratix II and Cyclone™ II devices. These dedicated hardware blocks ensure that you use global low-skew routing lines and avoid any possible hold time problems on the device due to logic delay on the clock line.

Refer to the appropriate device data sheet or handbook for device-specific information about clocking structures.

Gated Clocks

Gated clocks turn a clock signal on and off using an enable signal that controls some sort of gating circuitry, as shown in Figure 5–6. When a clock is turned off, the corresponding clock domain is shut down and becomes functionally inactive.

Figure 5–6. Gated Clock



You can use gated clocks to reduce power consumption in some device architectures. When a clock is gated, both the clock network and the registers driven by it stop toggling, thereby eliminating their contributions to power consumption. However, gated clocks are not part of a synchronous scheme and therefore can significantly increase the effort required for design implementation and verification. Gated clocks contribute to clock skew and make device migration difficult. These clocks are also sensitive to glitches, which can cause design failure.

Altera recommends using dedicated hardware to perform clock gating rather than using multiplexing logic, if it is available in your target device. For example, you can use the clock control block in Stratix II and Cyclone II devices to shut down an entire clock network. Dedicated hardware blocks ensure that you use global routing with low skew and avoid any possible hold time problems on the device due to logic delay on the clock line.

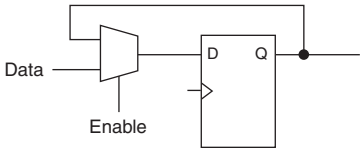
Refer to the appropriate device data sheet or handbook for device-specific information about clocking structures.

From a functional point of view, you can shut down a clock domain in a purely synchronous manner using a synchronous clock enable signal. However, when using a synchronous clock enable scheme, the clock network continues toggling. This practice does not reduce power consumption as much as gating the clock at the source does. In most cases, you should use a synchronous scheme such as those described in the "Synchronous Clock Enables" section. For improved power reduction when gating clocks with logic, refer to "Recommended Clock-Gating Method" on page 5–13.

Synchronous Clock Enables

To turn off a clock domain in a synchronous manner, use a synchronous clock enable signal. FPGAs efficiently support clock enable signals because there is a dedicated clock enable signal available on all device registers. This scheme does not reduce power consumption as much as gating the clock at the source because the clock network keeps toggling, but it will perform the same function as a gated clock by disabling a set of registers. Insert a multiplexer in front of the data input of every register to either load new data or copy the output of the register (Figure 5–7).

Figure 5–7. Synchronous Clock Enable

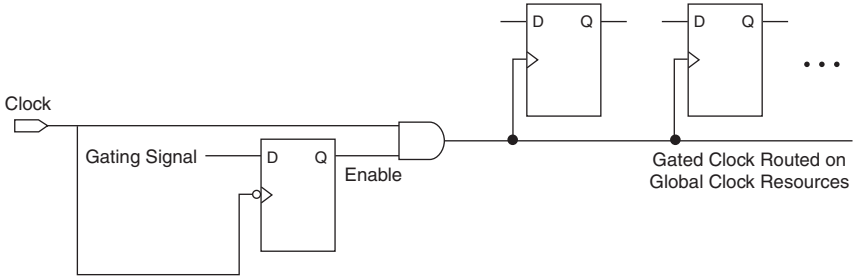


Recommended Clock-Gating Method

Only use gated clocks when your target application requires power reduction and when gated clocks are able to provide the required reduction in your device architecture. If you must use clocks gated by logic, implement these clocks using the robust clock-gating technique shown in Figure 5–8 and ensure that the gated clock signal uses dedicated global clock routing.

You can gate a clock signal at the source of the clock network, at each register, or somewhere in between. Because the clock network contributes to switching power consumption, gate the clock at the source whenever possible, so you can shut down the entire clock network instead of gating it further along the clock network at the registers.

Figure 5–8. Recommended Clock Gating Technique



In the technique shown in Figure 5–8, a register generates the enable signal to ensure that the signal is free of glitches and spikes. The register that generates the enable signal is triggered on the inactive edge of the clock to be gated (use the falling edge when gating a clock that is active on the rising edge, as shown in Figure 5–8). Using this technique, only one input of the gate that turns the clock on and off changes at a time that prevents any glitches or spikes on the output. Use an AND gate to gate a clock that is active on the rising edge. For a clock that is active on the falling edge, use an OR gate to gate the clock and register the enable command with a positive edge-triggered register.

When using this technique, pay attention to the duty cycle of the clock and the delay through the logic that generates the enable signal, because the enable signal must be generated in half the clock cycle. This situation might cause problems if the logic that generates the enable command is particularly complex, or if the duty cycle of the clock is severely unbalanced. However, careful management of the duty cycle and logic delay may be an acceptable solution when compared with problems created by other methods of gating clocks.

Ensure that you apply a clock setting to the gated clock in the Quartus II software. As shown in Figure 5–8, apply a clock setting to the output of the AND gate. Otherwise, the Timing Analyzer may analyze the circuit using the clock path through the register as the longest clock path and the path that skips the register as the shortest clock path, resulting in artificial clock skew.

Hierarchical Design Partitioning

A hierarchical design consists of multiple design blocks linked together in a hierarchy. When a design is partitioned hierarchically, you can compile, optimize and simulate the individual design blocks separately. You can use the incremental compilation or LogicLock™ design flows to follow a block-based design methodology where each block is placed and routed independently, then all blocks in the hierarchy are combined at the top level. Some synthesis tools have features to help you create separate netlist files or maintain separate parts of a netlist file for different parts of your design, to support block-based design techniques or incremental compilation.

For information about incremental compilation, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*. For more information about the LogicLock design methodology, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*. For more information about incremental synthesis flows in your synthesis tool, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II handbook*.

When using a hierarchical or incremental design methodology, consider how the design is partitioned to achieve good results.

Altera recommends the following practices for partitioning designs:

- Partition the design at functional boundaries.
- Minimize the I/O connections between different partitions.
- Register all inputs and outputs of each block. This makes logic synchronous and avoids glitches and avoids any delay penalty on signals that cross between partitions. Registering I/Os typically eliminates the need to specify timing requirements for signals that connect between different blocks.
- Do not use "glue logic" or connection logic between hierarchical blocks. When you preserve hierarchy boundaries, glue logic is not merged with hierarchical blocks. Your synthesis software may optimize glue logic separately, which can degrade synthesis results and is not efficient when used with the LogicLock design methodology.
- Remember that logic is not synthesized or optimized across partition boundaries, which means any constant values (signals set to GND, for example) will not be propagated across partitions.

- Do not use tri-state signals or bidirectional ports on hierarchical boundaries. If you use boundary tri-states in a lower-level block, synthesis pushes the tri-states through the hierarchy to the top-level to take advantage of the tri-state drivers on the output pins of Altera device. Because this requires optimizing through hierarchies, lower-level boundary tri-state signals have restrictions with block-level design methodologies.
- Limit clocks to one per block. Partitioning the design into clock domains makes synthesis and timing analysis easier.
- Place state machines in separate blocks to speed optimization and provide greater encoding control.
- Separate timing-critical functions from non-timing-critical functions.
- Limit the critical timing path to one hierarchical block. You can group the logic from several design blocks to ensure the critical path resides in one block.

For more guidelines for creating design partitions for Quartus II incremental compilation, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

Targeting Clock & Register-Control Architectural Features

In addition to following general design guidelines, it is important to code your design with the device architecture in mind. FPGAs provide device-wide clocks and register control signals that can improve performance.

Clock Network Resources

Altera FPGAs provide device-wide global clock routing resources and dedicated inputs. You should use the FPGA's low-skew, high-fan-out, dedicated routing where available. By assigning a clock input to one of these dedicated clock pins or using a Quartus II logic option to assign global routing, you can take advantage of the dedicated routing available for clock signals.

In ASIC design, balancing the clock delay as it is distributed across the device can be important. Because Altera FPGAs provides device-wide global clock routing resources and dedicated inputs, there is no need to manually balance delays on the clock network.

Altera recommends limiting the number of clocks in your design to the number of dedicated global clock resources available in your FPGA. Clocks feeding multiple locations that do not use global routing may exhibit clock skew across the device that could lead to timing problems. In addition, when you use combinational logic to generate an internal clock, it adds delays on the clock line. In some cases, delay on a clock line

can result in a clock skew greater than the data path length between two registers. If the clock skew is greater than the data delay, the timing parameters of the register (such as hold time requirements) are violated and the design will not function correctly.

Today's FPGAs offer increasing numbers of global clocks to address large designs with many clock domains. Many large FPGA devices provide dedicated global clock networks, regional clock networks, and dedicated fast regional clock networks. These clocks are typically organized into a hierarchical clock structure that allows many clocks in each device region with low skew and delay. There are typically a number of dedicated clock pins to drive either the global or regional clock networks and both PLL outputs and internal clocks can drive various clock networks.

To reduce the clock skew within a given clock domain and ensure that hold times are met within that clock domain, assign each clock signal to one of the global high-fan-out and low-skew clock networks in the FPGA device. Quartus II automatically uses global routing for high-fanout control signals, PLL outputs, and signals feeding the global clock pins on the device. You can make explicit **Global Signal** logic option settings. To make explicit **Global Signal** logic option settings, on the Assignment menu, click **Assignment Editor**. Use this option when it is necessary to force the software to use the global routing for particular signals.

To take full advantage of these routing resources, the sources of clock signals in a design (input clock pins or internally-generated clocks) should drive only the clock input ports of registers. In older Altera device families (such as FLEX® 10K and ACEX® 1K), if a clock signal feeds the data ports of a register, the signal may not be able to use the dedicated routing, which can lead to decreased performance and clock skew problems. In general, allowing clock signals to drive the data ports of registers is not considered synchronous design, and it can complicate timing analysis. It is not a recommended practice.

Reset Resources

ASIC designs may use local resets to avoid long routing delays on the signal. You should take advantage of the device-wide asynchronous reset pin available on most FPGAs to eliminate these problems. This reset signal provides low-skew routing across the device.

Register Control Signals

Avoid using an asynchronous load signal if the design's target device architecture does not include registers with dedicated circuitry for asynchronous loads. Also, avoid using both asynchronous clear and preset if the architecture provides only one of those control signals.

APEX™ devices, for example, directly support an asynchronous clear function, but not a preset or load function. When the target device does not directly support the signals, the place-and-route software must use combinational logic to implement the same functionality. In addition, if you use signals in a priority other than the inherent priority in the device architecture, combinational logic may be required to implement the desired control signals. The combinational logic is less efficient and can cause glitches and other problems; it is best to avoid these implementations.

For Verilog HDL and VHDL examples of registers with various control signals, and information on the inherent priority order of register control signals in Altera device architecture, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

Conclusion

Following the design practices outlined in this chapter can help you meet your design goals consistently. Asynchronous design techniques may result in incomplete timing analysis, may clause glitches on data signals, and may rely on propagation delays in a device leading to race conditions and unpredictable results. Taking advantage of the architectural features in your FPGA device can also improve your quality of results.

6. Recommended HDL Coding Styles

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Introduction

HDL coding style can have a significant effect on the quality of results that you achieve for programmable logic designs. Synthesis tools optimize HDL code for both logic utilization and performance. However, sometimes the best optimizations require human understanding of the design, and synthesis tools have no information about the purpose or intent of the design. You are often in the best position to improve your quality of results.

This chapter addresses HDL coding style recommendations to ensure optimal synthesis results when targeting Altera® devices, including the following sections:

- Using Altera Megafunctions
- Instantiating Altera Megafunctions in HDL Code
- Inferring Altera Megafunctions from HDL Code
- Device-Specific Coding Guidelines
- Coding Guidelines for Other Logic Structures

For additional guidelines on structuring your design, refer to the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

For style recommendations, options, or HDL attributes specific to your synthesis tool (including Quartus® II integrated synthesis and other third-party EDA tools), refer to the tool vendor's documentation or the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

Using Altera Megafunctions

Altera provides parameterizable megafunctions that are optimized for Altera device architectures. Using megafunctions instead of coding your own logic saves valuable design time. Additionally, the Altera-provided megafunctions may offer more efficient logic synthesis and device implementation. You can scale the megafunction's size and set various options by setting parameters. Megafunctions include the library of parameterized modules (LPM) and Altera device-specific megafunctions.

You must use megafunctions to access some Altera device-specific features, such as memory, DSP blocks, LVDS drivers, phase-locked loops (PLLs), transceivers, and double data rate input/output (DDIO) circuitry.

To use megafunctions in your HDL code, you can instantiate them as described in "Instantiating Altera Megafunctions in HDL Code" on page 6–3. Sometimes it is preferable to make your code independent of device family or vendor, and you do not want to instantiate megafunctions directly. In cases where you do not want to instantiate a megafunction, follow the guidelines and coding examples in "Inferring Altera Megafunctions from HDL Code" on page 6–6 to ensure your generic HDL code infers the appropriate Altera megafunction.

For some designs, generic HDL code can provide better results than instantiating a megafunction. Refer to the following general guidelines and examples that describe when to use standard HDL code and when to use megafunctions:

- For simple addition or subtraction functions, use the + or - symbol instead of an LPM function. Instantiating an LPM function for simple arithmetic operations can result in a less efficient result because the function is hard coded and the synthesis algorithms cannot take advantage of basic logic optimizations. For more complicated arithmetic logic such as synchronous loadable counters, LPM functions give you access to detailed architecture-specific functionality that is difficult to infer from HDL code.
- For simple multiplexers and decoders, use array notation (such as `out = data[sel]`) instead of an LPM function. Array notation works very well and has simple syntax. You can use the `LPM_MUX` function to take advantage of architectural features such as cascade chains in APEX™ series devices, but use the LPM function only if you want to force a specific implementation.
- Avoid division operations where possible. Division is an inherently slow operation. Many designers use multiplication creatively to produce division results. If you must divide, the `LPM_DIVIDE` function provides the best possible results.

Instantiating Altera Megafunctions in HDL Code

The following sections describe how to use megafunctions by instantiating them in your HDL code with the following methods:

- Instantiating Megafunctions Using the MegaWizard® Plug-In Manager—You can use the MegaWizard Plug-In Manager to parameterize the function and create a wrapper file.
- Creating a Clear Box Netlist File for Third-Party Synthesis Tools—You can optionally create a clear box body instead of a wrapper file.
- Instantiating Megafunctions Using the Port & Parameter Definition—You can instantiate the function directly in your HDL code.

Instantiating Megafunctions Using the MegaWizard Plug-In Manager

Use the MegaWizard Plug-In Manager as described in this section to create megafunctions in the Quartus II GUI that you can instantiate in your HDL code. The MegaWizard Plug-In Manager provides a graphical user interface to customize and parameterize megafunctions, and ensures that you set all megafunction parameters properly. When you finish setting parameters, you can specify which files you want to be generated. Depending on which language you choose, the MegaWizard Plug-In Manager instantiates the megafunction with the correct parameters and generates one of the following sets of files:

- AHDL Text Design File (**.tdf**) wrapper file and a sample instantiation template Text Design File (**_inst.tdf**).
- Verilog HDL (**.v**) wrapper file a sample instantiation template Verilog HDL file (**_inst.v**), and a black-box Verilog HDL module declaration.
- VHDL (**.vhd**) wrapper file and a sample instantiation template VHDL file (**_inst.vhd**).

You can instantiate the megafunction wrapper file in your design using the corresponding sample instantiation file. In addition, the MegaWizard Plug-In Manager also creates the following default files by default:

- Component Declaration File (**.cmp**) that can be used in VHDL Design Files
- ADHL Include File (**.inc**) that can be used in Text Design Files (**.tdf**) and as a reference for Verilog HDL design files

Refer to Table 6–1 for a list and description of files generated by the MegaWizard Plug-In Manager.

Table 6–1. MegaWizard Plug-In Manager Generated Files

File	Description
<*output file*>**.bsf**	Block Symbol File—Used in the Quartus II Block Design Files (**.bdf**).
<*output file*>**.cmp**	Component Declaration File—Used in VHDL designs.
<*output file*>**.inc**	ADHL Include File—Used in AHDL designs.
<*output file*>**.tdf** *(1)*	AHDL Wrapper File—Megafunction wrapper file for instantiation in an AHDL design.
<*output file*>**.vhd** *(2) (4)*	VHDL Wrapper File—Megafunction wrapper file, or clear box netlist file, for instantiation in a VHDL design.
<*output file*>**.v** *(3) (4)*	Verilog HDL Wrapper File—Megafunction wrapper file, or clear box netlist file, for instantiation in a Verilog HDL design.
<*output file*>**_bb.v** *(3)*	Black box Verilog HDL Module Declaration—Hollow-body module declaration that can be used in Verilog HDL designs to specify port directions when creating black boxes in third-party synthesis tools.
<*output file*>**_inst.tdf** *(1)*	Text Design File Instantiation Template—Sample AHDL instantiation of the subdesign in the megafunction wrapper file.
<*output file*>**_inst.vhd** *(2)*	VHDL Instantiation Template—Sample VHDL instantiation of the entity in the megafunction wrapper file.
<*output file*>**_inst.v** *(3)*	Verilog HDL Instantiation Template—Sample Verilog HDL instantiation of the module in the megafunction wrapper file.

Notes to Table 6–1:

(1) The MegaWizard Plug-In Manager generates this file only if you select AHDL output files.

(2) The MegaWizard Plug-In Manager generates this file only if you select VHDL output files.

(3) The MegaWizard Plug-In Manager generates this file only if you select Verilog HDL output files.

(4) A megafunction wrapper file is created by default for most megafunctions. To take advantage of the clear box feature, on the Tools menu, click **MegaWizard Plug-In Manager** and turn on **Generate clear box netlist file instead of a default wrapper file (for use with supported EDA synthesis tools only)**. For additional information about how to use the MegaWizard Plug-In Manager, refer to the Quartus II Help.

Creating a Clear Box Netlist File for Third-Party Synthesis Tools

When you use certain megafunctions with third-party synthesis tools, you can optionally create a clear box body instead of a wrapper file. The clear box body is a fully synthesized megafunction that you can use with certain third-party EDA synthesis tools. The netlist file that contains the megafunction clear box body provides your third-party synthesis tool with information about the architectural details used in the Quartus II software. This information enables certain synthesis tools to better report timing and resource utilization estimates. In addition, synthesis tools can use the timing information to focus timing-driven optimizations and improve the quality of results.

For information about clear box support in your synthesis tool, refer to the tool vendor's documentation or the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

To generate a clear box netlist, turn on **Generate clear box netlist file instead of a default wrapper file (for use with supported EDA synthesis tools only)** on the megafunction selection page 2a of the MegaWizard Plug-In Manager.

Note that not all megafunctions support clear box netlists. If you cannot create a clear box netlist for a particular megafunction, the option to generate the netlist is not shown on page 2a of the MegaWizard Plug-In Manager. Some megafunctions always use a clear box netlist file, in which case the option on page 2a cannot be turned off.

Instantiating Megafunctions Using the Port & Parameter Definition

You can instantiate the megafunction directly in your AHDL, Verilog HDL, or VHDL code by calling the megafunction and setting its parameters as you would any other subdesign, module, or component.

Refer to the specific megafunction in the Quartus II Help for a list of the megafunction ports and parameters. Quartus II Help also provides a sample VHDL component declaration and AHDL function prototype for each megafunction.

Altera strongly recommends that you use the MegaWizard Plug-In Manager for complex megafunctions such as PLLs, transceivers, and LVDS drivers. For details on using the MegaWizard Plug-In Manager, refer to "Instantiating Megafunctions Using the MegaWizard Plug-In Manager" on page 6–3.

Inferring Altera Megafunctions from HDL Code

Synthesis tools, including Quartus II integrated synthesis, recognize certain types of HDL code and automatically infer the appropriate megafunction. The synthesis tool uses the Altera megafunction code when compiling your design—even when you do not specifically instantiate the megafunction. Synthesis tools infer megafunctions to take advantage of logic that is optimized for Altera devices. The area and performance of such logic may be better than the results obtained by inferring generic logic from the same HDL code.

The following sections describe the types of logic that standard synthesis tools recognize and map to megafunctions. Synthesis software infers only the specific functions listed here. The software cannot infer other functions, such as PLLs, LVDS drivers, transceivers, or DDIO circuitry from HDL code because these functions cannot be fully or efficiently described in HDL code. In some cases, you can use synthesis tool options to turn off inference of certain megafunctions. The following sections describe how to infer the following megafunctions from generic HDL code:

- `lpm_mult`—Inferring Multipliers from HDL Code
- `altmult_accum` & `altmult_add`—Inferring Multiply-Accumulators & Multiply-Adders from HDL Code
- `altsyncram` & `lpm_ram_dp`—Inferring RAM Functions from HDL Code
- `lpm_rom`—Inferring ROM from HDL Code
- `altshift_taps`—Inferring Shift Registers from HDL Code

For synthesis tool features and options, refer to your synthesis tool documentation or the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

lpm_mult—Inferring Multipliers from HDL Code

To infer multiplier functions, synthesis tools look for multipliers and convert them to `lpm_mult` or `altmult_add` megafunctions, or may map them directly to multiplier device atoms. For devices with DSP blocks, the software can implement the function in a DSP block instead of logic, depending on device utilization. The Quartus II Fitter can also place input and output registers in DSP blocks (that is, perform register packing) to improve performance and area utilization.

For additional information about the DSP block and which functions it can implement, refer to the appropriate Altera device family handbook and The DSP Solution Center of the Altera web site at **www.altera.com**.

The following four code samples show Verilog HDL and VHDL examples for unsigned and signed multipliers that synthesis tools can infer as an `lpm_mult` or `altmult_add` megafunction. Each example fits into one DSP block 9-bit element. In addition, when register packing occurs, no extra logic cells for registers are required.

The `signed` declaration in Verilog HDL is a feature of the Verilog 2001 Standard.

Example 6–1. Verilog HDL Unsigned Multiplier

```
module unsigned_mult (out, a, b);
   output [15:0] out;
   input  [7:0] a;
   input  [7:0] b;
   assign out = a * b;
endmodule
```

Example 6–2. Verilog HDL Signed Multiplier with Input & Output Registers (Pipelining = 2)

```
module signed_mult (out, clk, a, b);
   output [15:0] out;
   input clk;
   input signed [7:0] a;
   input signed [7:0] b;

   reg signed [7:0] a_reg;
   reg signed [7:0] b_reg;
   reg signed [15:0] out;
   wire signed [15:0] mult_out;

   assign mult_out = a_reg * b_reg;

   always @ (posedge clk)
   begin
      a_reg <= a;
      b_reg <= b;
      out <= mult_out;
   end
endmodule
```

Example 6–3. VHDL Unsigned Multiplier with Input & Output Registers (Pipelining = 2)

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.all;

ENTITY unsigned_mult IS
   PORT (
      a: IN UNSIGNED (7 DOWNTO 0);
      b: IN UNSIGNED (7 DOWNTO 0);
      clk: IN STD_LOGIC;
      aclr: IN STD_LOGIC;
      result: OUT UNSIGNED (15 DOWNTO 0)
   );
END unsigned_mult;

ARCHITECTURE rtl OF unsigned_mult IS
   SIGNAL a_reg, b_reg: UNSIGNED (7 DOWNTO 0);
BEGIN
   PROCESS (clk, aclr)
   BEGIN
      IF (aclr ='1') THEN
         a_reg <= (OTHERS => '0');
         b_reg <= (OTHERS => '0');
         result <= (OTHERS => '0');
      ELSIF (clk'event AND clk = '1') THEN
         a_reg <= a;
         b_reg <= b;
         result <= a_reg * b_reg;
      END IF;
   END PROCESS;
END rtl;
```

Example 6–4. VHDL Signed Multiplier

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.all;

ENTITY signed_mult IS
   PORT (
      a: IN SIGNED (7 DOWNTO 0);
      b: IN SIGNED (7 DOWNTO 0);
      result: OUT SIGNED (15 DOWNTO 0)
   );
END signed_mult;

ARCHITECTURE rtl OF signed_mult IS
   SIGNAL a_int, b_int: SIGNED (7 downto 0);
   SIGNAL pdt_int: SIGNED (15 downto 0);
BEGIN
   a_int <= (a);
   b_int <= (b);
   pdt_int <= a_int * b_int;
   result <= pdt_int;
END rtl;
```

altmult_accum & altmult_add—Inferring Multiply-Accumulators & Multiply-Adders from HDL Code

Synthesis tools detect multiply-accumulators or multiply-adders and convert them to `altmult_accum` or `altmult_add` megafunctions, respectively. The Quartus II software then places these functions in DSP blocks during placement and routing.

Synthesis tools infer multiply-accumulator and multiply-adder functions only if the Altera device family has dedicated DSP blocks.

A multiply-accumulator consists of a multiplier feeding an addition operator. The addition operator feeds a set of registers that then feeds the second input to the addition operator. A multiply-adder consists of two to four multipliers feeding one or two levels of addition, subtraction, or addition/subtraction operators. Addition is always the second-level operator, if it is used. In addition to the multiply-accumulator and multiply-adder, the Quartus II Fitter also places input and output registers into the DSP blocks to pack registers and improve performance and area utilization.

The Verilog HDL and VHDL code samples shown in Examples 6–5 through 6–8 infer specific multiply-accumulators and multiply-adders.

Example 6–5. Verilog HDL Unsigned Multiply-Accumulator with Input, Output & Pipeline Registers (Latency = 3)

```
module unsig_altmult_accum (dataout, dataa, datab, clk, aclr, clken);
   input [7:0] dataa;
   input [7:0] datab;
   input clk;
   input aclr;
   input clken;
   output [31:0] dataout;
   reg [31:0] dataout;
   reg [7:0] dataa_reg;
   reg [7:0] datab_reg;
   reg [15:0] multa_reg;
   wire [15:0] multa;
   wire [31:0] adder_out;
   assign multa = dataa_reg * datab_reg;
   assign adder_out = multa_reg + dataout;
   always @ (posedge clk or posedge aclr)
   begin
      if (aclr)
      begin
         dataa_reg <= 0;
         datab_reg <= 0;
         multa_reg <= 0;
         dataout <= 0;
      end
      else if (clken)
      begin
         dataa_reg <= dataa;
         datab_reg <= datab;
         multa_reg <= multa;
         dataout <= adder_out;
      end
   end
endmodule
```

Example 6–6. Verilog HDL Signed Multiply-Adder (Latency = 0)

```
module sig_altmult_add (dataa, datab, datac, datad, result);
   input signed [15:0] dataa;
   input signed [15:0] datab;
   input signed [15:0] datac;
   input signed [15:0] datad;
   output [32:0] result;

   wire signed [31:0] mult0_result;
   wire signed [31:0] mult1_result;

   assign mult0_result = dataa * datab;
   assign mult1_result = datac * datad;
   assign result = (mult0_result + mult1_result);
endmodule
```

Example 6–7. VHDL Unsigned Multiply-Adder with Input, Output & Pipeline Registers (Latency = 3)

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.all;

ENTITY unsignedmult_add IS
   PORT (
      a: IN UNSIGNED (7 DOWNTO 0);
      b: IN UNSIGNED (7 DOWNTO 0);
      c: IN UNSIGNED (7 DOWNTO 0);
      d: IN UNSIGNED (7 DOWNTO 0);
      clk: IN STD_LOGIC;
      aclr: IN STD_LOGIC;
      result: OUT UNSIGNED (15 DOWNTO 0)
   );
END unsignedmult_add;

ARCHITECTURE rtl OF unsignedmult_add IS
   SIGNAL a_int, b_int, c_int, d_int: UNSIGNED (7 DOWNTO 0);
   SIGNAL pdt_int, pdt2_int: UNSIGNED (15 DOWNTO 0);
   SIGNAL result_int: UNSIGNED (15 DOWNTO 0);
BEGIN
   PROCESS (clk, aclr)
   BEGIN
      IF (aclr = '1') THEN
         a_int <= (OTHERS => '0');
         b_int <= (OTHERS => '0');
         c_int <= (OTHERS => '0');
         d_int <= (OTHERS => '0');
         pdt_int <= (OTHERS => '0');
         pdt2_int <= (OTHERS => '0');
         result_int <= (OTHERS => '0');

      ELSIF (clk'event AND clk = '1') THEN
         a_int <= a;
         b_int <= b;
         c_int <= c;
         d_int <= d;
         pdt_int <= a_int * b_int;
         pdt2_int <= c_int * d_int;
         result_int <= pdt_int + pdt2_int;
      END IF;
      END PROCESS;
   result <= result_int;
END rtl;
```

Example 6–8. VHDL Signed Multiply-Accumulator with Input, Output & Pipeline Registers (Latency = 3)

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.all;

ENTITY sig_altmult_accum IS
   PORT (
      a: IN SIGNED(7 DOWNTO 0);
      b: IN SIGNED (7 DOWNTO 0);
      clk: IN STD_LOGIC;
      accum_out: OUT SIGNED (15 DOWNTO 0)
   ) ;
END sig_altmult_accum;

ARCHITECTURE rtl OF sig_altmult_accum IS
   SIGNAL a_reg, b_reg: SIGNED (7 DOWNTO 0);
   SIGNAL pdt_reg: SIGNED (15 DOWNTO 0);
   SIGNAL adder_out: SIGNED (15 DOWNTO 0);
BEGIN
   PROCESS (clk)
   BEGIN
      IF (clk'event and clk = '1') THEN
         a_reg <= (a);
         b_reg <= (b);
            pdt_reg <= a_reg * b_reg;
         adder_out <= adder_out + pdt_reg;
      END IF;
     END process;
   accum_out <= (adder_out);
END rtl;
```

altsyncram & lpm_ram_dp—Inferring RAM Functions from HDL Code

To infer RAM functions, synthesis tools detect sets of registers and logic that can be replaced with the `altsyncram` or `lpm_ram_dp` megafunctions for device families that have dedicated RAM blocks.

Synthesis tools recognize single-port and simple dual-port (one read port and one write port) RAM blocks. Tools usually do not infer small RAM blocks because small RAM blocks typically can be implemented more efficiently by using the registers in regular logic.

If you are using Quartus II integrated synthesis, you can direct the software to infer RAM blocks for all sizes. On the Assignments menu, click **Settings**. In the **Category** list, click **Analysis & Synthesis Settings.** Click **More Settings**. Under **Existing Options Settings**, select the option **Allow Any RAM Size for Recognition**. Click the **Setting** arrow and select **ON**.

If your design contains a RAM block that your synthesis tool does not recognize and infer, the design might require a large amount of system memory that potentially can cause compilation problems.

Some synthesis tools provide options to control the implementation of inferred RAM blocks for Altera devices with TriMatrix™ memory blocks. For example, Quartus II integrated synthesis provides the ramstyle synthesis attribute to specify the type of memory block using the value "M512," "M4K," or "M-RAM," or to specify the use of regular logic instead of a dedicated memory block using the value "logic."

For information on synthesis attributes, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

When you are using a formal verification flow, Altera recommends that you create RAM blocks in separate entities or modules that only contain the RAM logic. In certain formal verification flows, for example, when using Quartus II integrated synthesis, the entity or module containing the inferred RAM is put into a black box automatically because formal verification tools do not support RAM blocks. The Quartus II software issues a warning message when this occurs. If the entity or module contains any additional logic outside the RAM block, this logic also must be treated as a black box for formal verification and therefore cannot be verified.

Dual-Clock Synchronous RAM

Altera's TriMatrix memory blocks are synchronous, so RAM designs that target architectures that contain these dedicated memory blocks must be synchronous to be mapped directly into the device architecture. Synchronous memories are supported in all Altera device families.

When simultaneous reading and writing to the same RAM address occurs, the TriMatrix memory blocks in Altera devices return undefined data values. This usually differs from the functionality of the original HDL design. If your design requires a given output when reading and writing to the same RAM address, direct your synthesis tool not to infer RAM blocks for dual-clock memories by disabling RAM inference for these memories.

For specific options to disable RAM inference in your synthesis tool, refer to your synthesis tool documentation or the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

The code samples shown in Examples 6–9 and 6–10 show Verilog HDL and VHDL code that infers dual-clock synchronous RAM.

Example 6–9. Verilog HDL Dual-Clock Synchronous RAM

```
module ram_dual (q, addr_in, addr_out, d, we, clk1, clk2);
   output [7:0] q;
   input [7:0] d;
   input [6:0] addr_in;
   input [6:0] addr_out;
   input we, clk1, clk2;

   reg [6:0] addr_out_reg;
   reg [7:0] q;
   reg [7:0] mem [127:0];

   always @ (posedge clk1)
   begin
      if (we)
         mem[addr_in] <= d;
   end

   always @ (posedge clk2) begin
      q <= mem[addr_out_reg];
      addr_out_reg <= addr_out;
   end
endmodule
```

Example 6–10. VHDL Dual-Clock Synchronous RAM

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY ram_dual IS
    PORT (
        clock1, clock2: IN STD_LOGIC;
        data: IN STD_LOGIC_VECTOR (3 DOWNTO 0);
        write_address: IN INTEGER RANGE 0 to 31;
        read_address: IN INTEGER RANGE 0 to 31;
        we: IN STD_LOGIC;
        q: OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
    );
END ram_dual;
ARCHITECTURE rtl OF ram_dual IS
    TYPE MEM IS ARRAY(0 TO 31) OF STD_LOGIC_VECTOR(3 DOWNTO 0);
    SIGNAL ram_block: MEM;
    SIGNAL read_address_reg : INTEGER RANGE 0 to 31;
BEGIN
    PROCESS (clock1)
    BEGIN
        IF (clock1'event AND clock1 = '1') THEN
            IF (we = '1') THEN
                ram_block(write_address) <= data;
            END IF;
        END IF;
    END PROCESS;
    PROCESS (clock2)
    BEGIN
        IF (clock2'event AND clock2 = '1') THEN
            q <= ram_block(read_address_reg);
            read_address_reg <= read_address;
        END IF;
    END PROCESS;
END rtl;
```

Single-Clock Synchronous RAM without Read-Through-Write Behavior

The code examples in this section show Verilog HDL and VHDL code that infers single-clock synchronous RAM. Altera's TriMatrix memory blocks are synchronous, so RAM designs targeting to architectures that contain these dedicated memory blocks must be synchronous to be mapped directly into the device architecture.

These examples also avoid read-through-write behavior, which is not directly supported in TriMatrix memory blocks. Altera recommends that you use this coding style as long as your design does not require RAM with read-through-write behavior, meaning your design does not require that a simultaneous read and write to the same RAM location read the new value that is currently being written to that RAM location.

In TriMatrix memory blocks, if you attempt to read and write from the same address in the same clock cycle, the read returns either the old data at the address or unknown data, depending on the memory mode and block type.

If you require RAM with read-through-write behavior, refer to the section "Single-Clock Synchronous RAM with Read-Through-Write Behavior" on page 6–17.

For additional information about the dedicated memory blocks in your specific device, refer to the appropriate Altera device family data sheet on the Altera web site at **www.altera.com**.

The RAM code samples shown in Examples 6–11 and 6–12 map directly into Altera TriMatrix memory.

Example 6–11. Verilog HDL Single-Clock Synchronous RAM Without Read-Through-Write Behavior

```
module ram_infer (q, a, d, we, clk);
   output reg [7:0] q;
   input [7:0] d;
   input [6:0] a;
   input we, clk;

   reg [7:0] mem [127:0];

   always @ (posedge clk) begin
      if (we)
         mem[a] <= d;
      q <= mem[a]; // q doesn't get d in this clock cycle
   end
endmodule
```

Example 6–12. VHDL Single-Clock Synchronous RAM Without Read-Through-Write Behavior

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY ram IS
   PORT (
      clock: IN STD_LOGIC;
      data: IN STD_LOGIC_VECTOR (2 DOWNTO 0);
      write_address: IN INTEGER RANGE 0 to 31;
      read_address: IN INTEGER RANGE 0 to 31;
      we: IN STD_LOGIC;
      q: OUT STD_LOGIC_VECTOR (2 DOWNTO 0)
   );
END ram;

ARCHITECTURE rtl OF ram IS
   TYPE MEM IS ARRAY(0 TO 31) OF STD_LOGIC_VECTOR(2 DOWNTO 0);
   SIGNAL ram_block: MEM;
BEGIN
   PROCESS (clock)
   BEGIN
      IF (clock'event AND clock = '1') THEN
         IF (we = '1') THEN
            ram_block(write_address) <= data;
         END IF;
         q <= ram_block(read_address);
            -- VHDL semantics imply that q doesn't get data
            -- in this clock cycle
      END IF;
   END PROCESS;
END rtl;
```

Single-Clock Synchronous RAM with Read-Through-Write Behavior

TriMatrix memory blocks do not support mixed-port read-through-write behavior. This means if you attempt to read and write from the same address in the same clock cycle, the read returns either the old data at the address or unknown data, depending on the memory mode and block type. However, you can describe a RAM block in HDL code in which a simultaneous read and write to the same location reads the new value that is currently being written to that RAM location. The following examples show code that infers this type of RAM logic. To implement this behavior in the target device, synthesis software adds bypass logic around the RAM block. This bypass logic increases the area utilization of the design and decreases the performance if the RAM block is part of the design's critical path.

The RAM examples shown in Examples 6–13 and 6–14 require bypass logic around the RAM block.

Example 6–13. Verilog HDL Single-Clock Synchronous RAM with Read-Through-Write Behavior

```
module ram_infer (q, a, d, we, clk);
    output [7:0] q;
    input [7:0] d;
    input [6:0] a;
    input we, clk;
reg [6:0] read_add;
    reg [7:0] mem [127:0];
always @ (posedge clk) begin
        if (we)
            mem[a] <= d;
        read_add <= a;
    end
assign q = mem[read_add];
endmodule
```

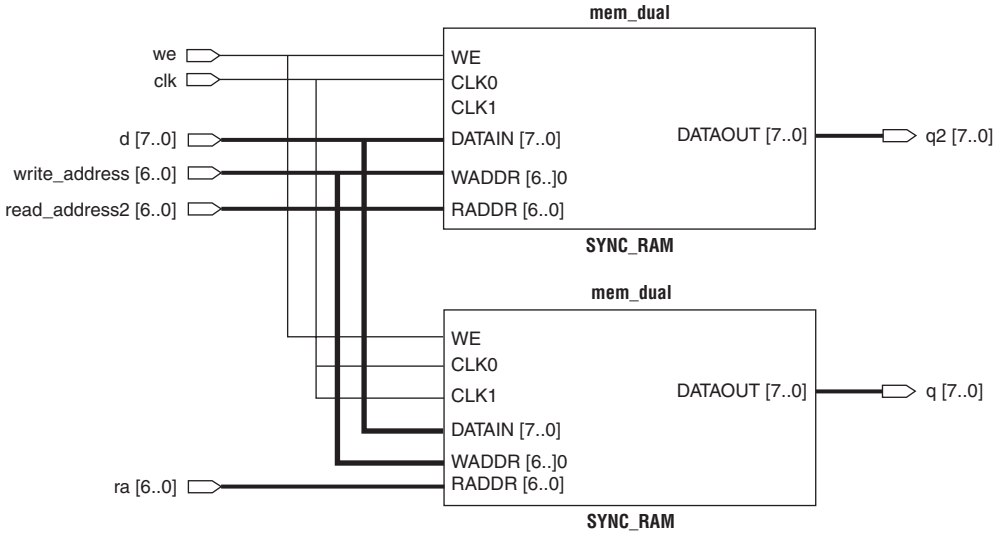
Example 6–14. VHDL Single-Clock Synchronous RAM with Read-Through-Write Behavior

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY ram IS
    PORT (
        clock: IN STD_LOGIC;
        data: IN STD_LOGIC_VECTOR (2 DOWNTO 0);
        write_address: IN INTEGER RANGE 0 to 31;
        read_address: IN INTEGER RANGE 0 to 31;
        we: IN STD_LOGIC;
        q: OUT STD_LOGIC_VECTOR (2 DOWNTO 0)
    );
END ram;

ARCHITECTURE rtl OF ram IS
    TYPE MEM IS ARRAY(0 TO 31) OF STD_LOGIC_VECTOR(2 DOWNTO 0);
    SIGNAL ram_block: MEM;
    SIGNAL read_address_reg: INTEGER RANGE 0 to 31;
BEGIN
    PROCESS (clock)
    BEGIN
        IF (clock'event AND clock = '1') THEN
            IF (we = '1') THEN
                ram_block(write_address) <= data;
            END IF;
            read_address_reg <= read_address;
        END IF;
    END PROCESS;
    q <= ram_block(read_address_reg);
END rtl;
```

Synchronous RAM with Two Read Addresses

Quartus II integrated synthesis can infer RAM blocks from RAM descriptions that have two read addresses and one write address. This type of RAM blocks can be implemented by duplicating the RAM block as shown in Figure 6–1. All inputs are duplicated for both RAM blocks except for the read address, which is individual for each block.

Figure 6–1. Block Diagram Showing Synchronous RAM with Two Read Addresses



The RAM code samples with two read addresses shown in Examples 6–15 and 6–16 are inferred by duplicating the RAM block.

Example 6–15. Verilog HDL Single-Clock Synchronous RAM with Two Read Addresses

```
module dual_ram_infer (q, q2, write_address, read_address, read_address2, d, we, clk);
      output reg [7:0] q;
      output reg [7:0] q2;
      input [7:0] d;
      input [6:0] write_address;
      input [6:0] read_address;
      input [6:0] read_address2;
      input we, clk;

      reg [7:0] mem [127:0];

      always @ (posedge clk) begin
            if (we)
                  mem[write_address] <= d;
            q <= mem[read_address];
            q2 <= mem[read_address2];
      end
endmodule
```

Example 6–16. VHDL Single-Clock Synchronous RAM with Two Read Addresses

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY dual_ram_infer IS
  PORT (
    clock: IN STD_LOGIC;
    data: IN STD_LOGIC_VECTOR (2 DOWNTO 0);
    write_address: IN INTEGER RANGE 0 to 31;
    read_address: IN INTEGER RANGE 0 to 31;
    read_address2: IN INTEGER RANGE 0 to 31;
    we: IN STD_LOGIC;
    q: OUT STD_LOGIC_VECTOR (2 DOWNTO 0);
    q2: OUT STD_LOGIC_VECTOR (2 DOWNTO 0)
    );
END dual_ram_infer;

ARCHITECTURE rtl OF dual_ram_infer IS
  TYPE MEM IS ARRAY(0 TO 31) OF STD_LOGIC_VECTOR(2 DOWNTO 0);
  SIGNAL ram_block: MEM;
BEGIN
  PROCESS (clock)
  BEGIN
    IF (clock'event AND clock = '1') THEN
      IF (we = '1') THEN
        ram_block(write_address) <= data;
      END IF;
      q <= ram_block(read_address);
      q2 <= ram_block(read_address2);
    END IF;
  END PROCESS;
END rtl;
```

Single-Clock Synchronous RAM with Asynchronous Read Address

The code samples shown in Examples 6–17 and 6–18 show Verilog HDL and VHDL code for RAM with asynchronous read addresses and registered outputs.

The implementation of the RAM code in the following examples varies depending on the dedicated RAM architecture of the device family. For example, implementing asynchronous read addresses in the APEX device series is straightforward because the RAM architecture in the APEX series supports asynchronous read addresses. However, read addresses in Stratix® devices and most newer device families must be registered. Therefore, you cannot directly implement the asynchronous RAM code in the following examples. To implement the asynchronous RAM in the Stratix series devices, for example, synthesis tools may move the output registers to the inputs of the RAM block so that the logic can be implemented using an `altsyncram` megafunction. If the read and write clocks are not the same, moving the output registers to the inputs of the RAM block can slightly change the functionality. Under these circumstances, the synthesis software issues a warning. If you are using Quartus II integrated synthesis, Quartus II Help explains the differences. These RAM examples may not map directly to the RAM block, depending on the device architecture.

Example 6–17. Verilog HDL Single-Clock Synchronous RAM with Asynchronous Read Address

```
module ram (clock, data, write_address, read_address, we, q);
    parameter ADDRESS_WIDTH = 4;
    parameter DATA_WIDTH    = 8;
    input clock;
    input [DATA_WIDTH-1:0] data;
    input [ADDRESS_WIDTH-1:0] write_address;
    input [ADDRESS_WIDTH-1:0] read_address;
    input we;
    output [DATA_WIDTH-1:0] q;

    reg [DATA_WIDTH-1:0] q;
    reg [DATA_WIDTH-1:0] ram_block [2**ADDRESS_WIDTH-1:0];
    always @ (posedge clock)

    begin
        if (we)
            ram_block[write_address] <= data;
        q <= ram_block[read_address];
    end
endmodule
```

Example 6–18. VHDL Single-Clock Synchronous RAM with Asynchronous Read Address

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY ram IS
    GENERIC (
        ADDRESS_WIDTH: integer := 4;
        DATA_WIDTH: integer := 8
    );
    PORT (
        clock: IN  std_logic;
        data: IN STD_LOGIC_VECTOR(DATA_WIDTH - 1 DOWNTO 0);
        write_address IN  STD_LOGIC_VECTOR (ADDRESS_WIDTH - 1 DOWNTO 0);
        read_address IN STD_LOGIC_VECTOR(ADDRESS_WIDTH - 1 DOWNTO 0);
        we: IN STD_LOGIC;
        q: OUT STD_LOGIC_VECTOR(DATA_WIDTH - 1 DOWNTO 0)
    );
END ram;

ARCHITECTURE rtl OF ram IS
    TYPE RAM IS ARRAY(0 TO 2 ** ADDRESS_WIDTH - 1) OF std_logic_vector(DATA_WIDTH - 1
DOWNTO 0);
    SIGNAL ram_block: RAM;
BEGIN
    PROCESS (clock)
    BEGIN
        IF (clock'event AND clock = '1') THEN
            IF (we = '1') THEN
                ram_block(TO_INTEGER(UNSIGNED(write_address))) <= data;
            END IF;
            q <= ram_block(TO_INTEGER(UNSIGNED(read_address)));
        END IF;
    END PROCESS;
END rtl;
```

Specifying Initial Memory Contents

Your synthesis tool may offer a way to specify the initial contents of an inferred memory. For example, Quartus II integrated synthesis supports a synthesis attribute called `ram_init_file` that allows you to specify a Memory Initialization File (**.mif**) for an inferred RAM block. In VHDL, you can also initialize the contents of an inferred memory by specifying a default value for the corresponding signal. Quartus II integrated synthesis automatically converts the default value into a MIF for the inferred RAM.

For information about the `ram_init_file` attribute, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*. For information about synthesis attributes in other synthesis tools, refer to the tool vendor's documentation.

lpm_rom—Inferring ROM from HDL Code

To infer ROM functions, synthesis tools detect sets of registers and logic that can be replaced with the `altsyncram` or `lpm_rom` megafunctions, depending on the target device family, only for device families that have dedicated memory blocks.

Because formal verification tools do not support ROM megafunctions, Quartus II integrated synthesis does not infer ROM megafunctions when a third-party formal verification tool is selected.

ROMs are inferred when a `case` statement exists in which a value is set to a constant for every choice in the case statement. Because small ROMs typically achieve the best performance when they are implemented using the registers in regular logic, each ROM function must meet a minimum size requirement to be inferred and placed into memory.

If you are using the Quartus II integrated synthesis, you can direct the software to infer ROM blocks for all sizes. On the Assignments menu, click **Settings**. In the **Category** list, click **Analysis & Synthesis Settings.** Click **More Settings**. Under **Existing Options Settings**, select the option **Allow Any ROM Size for Recognition**. Click the **Setting** arrow and select **ON**.

Some synthesis tools provide options to control the implementation of inferred ROM blocks for Altera devices with TriMatrix memory blocks. For example, Quartus II integrated synthesis provides the romstyle synthesis attribute to specify the type of memory block using the value "M512," "M4K," or "M-RAM," or to specify the use of regular logic instead of a dedicated memory block using the value "logic."

For information about synthesis attributes, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*. When you are using a formal verification flow, Altera recommends that you create ROM blocks in separate entities or modules that contain only the ROM logic because you may need to treat the entity and module as a black box during formal verification.

The Verilog HDL and VHDL code samples shown in Examples 6–19 and 6–20 infer synchronous ROM blocks. Depending on the device family's dedicated RAM architecture, the ROM logic may have to be synchronous; consult the device family handbook for details.

For device architectures with synchronous RAM blocks, such as the Stratix series devices and newer device families, either the address or the output has to be registered for ROM code to be inferred. When output registers are used, the registers are implemented using the input registers of the Stratix RAM block, but the functionality of the ROM is not changed. If you register the address, the power-up state of the inferred ROM can be different from the HDL design. In this scenario, the synthesis software generally issues a warning. The Quartus II Help explains the condition under which the functionality changes when you are using Quartus II integrated synthesis. These ROM code samples map directly to the Altera TriMatrix memory architecture.

Example 6–19. Verilog HDL Synchronous ROM

```
module sync_rom (clock, address, data_out);
    input clock;
    input [7:0] address;
    output [5:0] data_out;

    reg [5:0] data_out;

    always @ (posedge clock)
    begin
        case (address)
            8'b00000000: data_out = 6'b101111;
            8'b00000001: data_out = 6'b110110;
            ...
            8'b11111110: data_out = 6'b000001;
            8'b11111111: data_out = 6'b101010;
        endcase
    end
endmodule
```

Example 6–20. VHDL Synchronous ROM

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY sync_rom IS
    PORT (
        clock: IN STD_LOGIC;
        address: IN STD_LOGIC_VECTOR(7 downto 0);
        data_out: OUT STD_LOGIC_VECTOR(5 downto 0)
    );
END sync_rom;

ARCHITECTURE rtl OF sync_rom IS
BEGIN
PROCESS (clock)
    BEGIN
    IF rising_edge (clock) THEN
        CASE address IS
            WHEN "00000000" => data_out <= "101111";
            WHEN "00000001" => data_out <= "110110";
            ...
            WHEN "11111110" => data_out <= "000001";
            WHEN "11111111" => data_out <= "101010";
            WHEN OTHERS => data_out <= "101111";
        END CASE;
    END IF;
    END PROCESS;
END rtl;
```

altshift_taps—Inferring Shift Registers from HDL Code

To infer shift registers, synthesis tools detect a group of shift registers of the same length and convert them to an `altshift_taps` megafunction. To be detected, all the shift registers must have the following characteristics:

- Use the same clock and clock enable
- Do not have any other secondary signals
- Have equally spaced taps that are at least three registers apart

Because formal verification tools do not support shift register megafunctions, the Quartus II integrated synthesis does not infer the `altshift_taps` megafunction when a third-party formal verification tool is selected. You can select EDA tools for use with your Quartus II project on the **EDA Tool Settings** page of the **Settings** dialog box.

When you are using a formal verification flow, Altera recommends that you create shift register blocks in separate entities or modules containing only the shift register logic, because you may need to treat the entity or module as a black box during formal verification.

Synthesis software recognizes shift registers only for device families that have dedicated RAM blocks and the software uses certain guidelines to determine the best implementation. The following guidelines are followed in Quartus II integrated synthesis and also are generally followed by third-party EDA tools:

- For FLEX® 10K and ACEX® 1K devices, the software does not infer `altshift_taps` megafunctions because FLEX 10K and ACEX 1K devices have a relatively small amount of dedicated memory.
- For APEX 20K and APEX II devices, the software infers the `altshift_taps` megafunction only if the shift register has more than a total of 128 bits. Smaller shift registers typically do not benefit from implementation in dedicated memory.
- For Stratix and Cyclone™ series devices, the software determines whether to infer the `altshift_taps` megafunction based on the width of the registered bus (*W*), the length between each tap (*L*), and the number of taps (*N*).
  - If the registered bus width is one ($W = 1$), the software infers `altshift_taps` if the number of taps times the length between each tap is greater than or equal to 64 ($N \times L \geq 64$).
  - If the registered bus width is greater than one ($W > 1$), the software infers `altshift_taps` if the registered bus width times the number of taps times the length between each tap is greater than or equal to 32 ($W \times N \times L \geq 32$).

If the length between each tap (*L*) is not a power of two, the software uses more logic to decode the read and write counters. This situation occurs because for different sizes of shift registers, external decode logic that uses logic elements (LEs) or Adaptive Logic Modules (ALMs) is required to implement the function. This decode logic eliminates the performance and utilization advantages of implementing shift registers in memory.

The registers that the software maps to the `altshift_taps` megafunction and places in RAM are not available in a Verilog HDL or VHDL output file for simulation tools because their node names do not exist after synthesis.

The following examples infer shift registers:

- Verilog HDL Single-Bit Wide, 64-Bit Long Shift Register
- Verilog HDL 8-Bit Wide, 64-Bit Long Shift Register with Evenly Spaced Taps
- VHDL 8-Bit Wide, 64-Bit Long Shift Register with Evenly Spaced Taps

Verilog HDL Single-Bit Wide, 64-Bit Long Shift Register

The Verilog HDL code sample shown in Example 6–21 shows a simple, single-bit wide, 64-bit long shift register. The synthesis software implements the register ($W = 1$ and $M = 64$) in an `altshift_taps` megafunction for supported devices. If the length of the register is less than 64 bits, the software implements the shift register in logic.

Example 6–21. Verilog HDL Single-Bit Wide, 64-Bit Long Shift Register

```
module shift_1x64 (clk, shift, sr_in, sr_out);
    input clk, shift;
    input sr_in;
    output sr_out;

    reg [63:0] sr;

    always @ (posedge clk)
    begin
        if (shift == 1'b1)
        begin
            sr[63:1] <= sr[62:0];
            sr[0] <= sr_in;
        end
    end
    assign sr_out = sr[63];
endmodule
```

Verilog HDL 8-Bit Wide, 64-Bit Long Shift Register with Evenly Spaced Taps

The code samples shown in Examples 6–22 and 6–23 show Verilog HDL and VHDL 8-bit wide, 64-bit long shift register ($W > 1$ and $M = 64$) with evenly spaced taps at 15, 31, and 47. The synthesis software implements this function in a single `altshift_taps` megafunction and maps it to RAM in supported devices.

Example 6–22. Verilog HDL 8-Bit Wide, 64-Bit Long Shift Register with Evenly Spaced Taps

```
module shift_8x64_taps (clk, shift, sr_in, sr_out, sr_tap_one, sr_tap_two, sr_tap_three );
    input clk, shift;
    input [7:0] sr_in;
    output [7:0] sr_tap_one, sr_tap_two, sr_tap_three, sr_out;

    reg [7:0] sr [63:0];
    integer n;

    always @ (posedge clk)
    begin
        if (shift == 1'b1)
        begin
            for (n = 63; n>0; n = n-1)
            begin
                sr[n] <= sr[n-1];
            end
            sr[0] <= sr_in;
        end

    end
    assign sr_tap_one = sr[15];
    assign sr_tap_two = sr[31];
    assign sr_tap_three = sr[47];
    assign sr_out = sr[63];
endmodule
```

Example 6–23. VHDL 8-Bit Wide, 64-Bit Long Shift Register with Evenly Spaced Taps

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY shift_8x64_taps IS
    PORT (
        clk: IN STD_LOGIC;
        shift: IN STD_LOGIC;
        sr_in: IN STD_LOGIC_VECTOR(7 DOWNTO 0);
        sr_tap_one: OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
        sr_tap_two : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
        sr_tap_three: OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
        sr_out: OUT STD_LOGIC_VECTOR(7 DOWNTO 0)
    );
    END shift_8x64_taps;

ARCHITECTURE arch OF shift_8x64_taps IS
    SUBTYPE sr_width IS STD_LOGIC_VECTOR(7 DOWNTO 0);
    TYPE sr_length IS ARRAY (63 DOWNTO 0) OF sr_width;
    SIGNAL sr: sr_length;
BEGIN
    PROCESS (clk)
    BEGIN
        IF (clk'EVENT and clk = '1') THEN
            IF (shift = '1') THEN
                sr(63 DOWNTO 1) <= sr(62 DOWNTO 0);
                sr(0) <= sr_in;
            END IF;
        END IF;
    END PROCESS;
    sr_tap_one <= sr(15);
    sr_tap_two <= sr(31);
    sr_tap_three <= sr(47);
    sr_out <= sr(63);
END arch;
```

Device-Specific Coding Guidelines

This section provides device-specific coding recommendations for Altera device architectures. It is important to understand how synthesis tools map your HDL code into the target Altera device. Designing registers and specific logic structures to match the appropriate Altera device architecture can provide significant quality improvements in your design results.

Register Power-Up Values in Altera Devices

Registers in the device core always power up to a low (0) logic level on all Altera devices. However, there are ways to implement logic such that registers behave as if they were powering up to a high (1) logic level.

If you use a preset signal on a device that does not support presets in the register architecture, then your synthesis tool may convert the preset signal to a clear signal, which requires synthesis to perform an

optimization referred to as NOT gate push-back. NOT gate push-back adds an inverter to the input and the output of the register so that the reset and power-up conditions will appear to be high but the device operates as expected. In this case, your synthesis tool may issue a message informing you about the power-up condition. The register itself powers up low, but the register output is inverted so the signal that arrives at all destinations is high.

Due to these effects, if you specify a particular reset value (other than 0), you may cause your synthesis tool to use the asynchronous clear (`aclr`) signals available on the registers to implement the high bits with `NOT` gate push-back. In that case, the registers will look as though they power up to the specified reset value. You will see this behavior, for example, if your design targets FLEX 10KE or ACEX devices.

When a load signal is available in the device, your synthesis tools can implement a reset of 1 or 0 value by using an asynchronous load of 1 or 0. When the synthesis tool uses an asynchronous load signal, it is not performing `NOT` gate push-back, so the registers will power up to a 0 logic level.

For additional details, refer to the appropriate device family handbook or the appropriate handbook of the Altera web site at www.altera.com.

Designers typically use an explicit reset signal for the design, which forces all registers into their appropriate values after reset but not necessarily at power-up. You can create your design such that the asynchronous reset allows the board to operate in a safe condition and then you can bring up the design with the reset active. This is a good practice so you do not depend on the power-up conditions of the device.

You can make the your design more stable and avoid potential glitches by synchronizing external or combinational logic of the device architecture before you drive the asynchronous control ports of registers.

For additional information about good synchronous design practices, refer to the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

If you want to force a particular power-up condition for your design, use the synthesis options available in your synthesis tool. With Quartus II integrated synthesis, you can apply the **Power-Up Level** logic option. You can also apply the option with an `altera_attribute` assignment in your source code. Using this option forces synthesis to perform `NOT` gate push-back because synthesis tools cannot actually change the power-up states of core registers.

You can apply the Quartus II integrated synthesis **Power-Up Level** assignment to a specific register or to a design entity, module or subdesign. If you do so, every register in that block receives the value. Registers power up to 0 by default; therefore you can use this assignment to force all registers to power up to 1 using NOT gate push-back.

Be aware that using NOT gate push-back as a global assignment could slightly degrade the quality of results due to the number of inverters that are needed. In some situations, issues are caused by enable or secondary control logic inference. It may also be more difficult to migrate such a design to an ASIC or a HardCopy® device. You can simulate the power-up behavior in a functional simulation if you use initialization.

The **Power-Up Level** option and the altera_attribute are described in the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

In VHDL, some synthesis tools can also read the default values for registered signals and implement this behavior in the device. For example, Quartus II integrated synthesis converts VHDL default values for registered signals into Power-Up Level settings. That way, the synthesized behavior matches the power-up state of the HDL code during a functional simulation.

For example, the following code infers a register for q and sets its power-up level to high (while the reset value is 0):

```
SIGNAL q : STD_LOGIC := '1'; -- q has a default value of '1'

PROCESS (clk, reset)
BEGIN
   IF (reset = '1') THEN
      q <= '0';
   ELSIF (rising_edge(clk)) THEN
      q <= d;
   END IF;
END PROCESS;
```

Note that the Quartus II software, like most synthesis tools, does not synthesize Verilog HDL initial blocks. Therefore, the tool does not synthesize variables that are assigned values in initial blocks into power-up conditions.

Secondary Register Control Signals Such as Clear & Clock Enable

FPGA device architectures are based on registers also known as flipflops. The registers in Altera FPGAs provide a number of secondary control signals (such as clear and enable signals) that you can use to implement control logic for each register without using extra logic cells. Device families vary in their support for secondary signals, so consult the device family data sheet to verify which signals are available in your target device.

To make the most efficient use of the signals in the device, your HDL code should match the device architecture as closely as possible. The control signals have a certain priority due to the nature of the architecture, so your HDL code should follow that priority where possible.

Your synthesis tool can emulate any control signals using regular logic, so getting functionally correct results is always possible. However, if your design requirements are flexible in terms of which control signals are used and in what priority, match your design to the target device architecture to achieve the most efficient results. If the priority of the signals in your design is not the same as that of the target architecture, then extra logic may be required to implement the control signals. This extra logic uses additional device resources, and can cause additional delays for the control signals.

In addition, there are certain cases where using logic other than the dedicated control logic in the device architecture can have a larger impact. For example, the clock enable signal has priority over the synchronous reset or clear signal in the device architecture. The clock enable turns off the clock line in the logic array block (LAB), and the clear signal is synchronous. So in the device architecture, the synchronous clear takes effect only when a clock edge occurs. If you code a register with a synchronous clear signal that has priority over the clock enable signal, the software must emulate the clock enable functionality using data inputs to the registers. Because the signal does not use the clock enable port of a register, you cannot apply a Clock Enable Multicycle constraint. In this case, following the priority of signals available in the device is clearly the best choice for the priority of these control signals, and using a different priority causes unexpected results with an assignment to the clock enable signal.

The priority order for secondary control signals in Altera devices differs from the order for other vendors' devices. If your design requirements are flexible regarding priority, verify that the secondary control signals meet design performance requirements when migrating designs between FPGA vendors and try to match your target device architecture to achieve the best results.

The signal order is the same for all Altera device families, although as noted previously, not all device families provide every signal. The following priority order is observed:

1. Asynchronous Clear, `aclr`—highest priority
2. Preset, `pre`
3. Asynchronous Load, `aload`
4. Enable, `ena`
5. Synchronous Clear, `sclr`
6. Synchronous Load, `sload`
7. Data In, `data`—lowest priority

The following examples provide Verilog HDL and VHDL code that create a register with the `aclr`, `aload`, and `ena` control signals listed previously.

The **dff_all.v** does not have `adata` on the sensitivity list, but **dff_all.vhd** does. This is a limitation of the Verilog HDL language—there is no way to describe an asynchronous load signal (in which `q` toggles if `adata` toggles while `aload` is high). All synthesis tools should infer an `aload` signal from this construct despite this limitation. When they perform such inference, you may see information or warning messages from the synthesis tool.

Example 6–24. Verilog HDL D-Type Flipflop (Register) with ena, aclr & aload Control Signals

```
module dff_control(clk, aclr, aload, ena, data, adata, q);
    input clk, aclr, aload, ena, data, adata;
    output q;

    reg q;

    always @ (posedge clk or posedge aclr or posedge aload)
    begin
        if (aclr)
            q <= 1'b0;
        else if (aload)
            q <= adata;
        else
            if (ena)
                q <= data;
    end
endmodule
```

Example 6–25. VHDL D-Type Flipflop (Register) with ena, aclr & aload Control Signals

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY dff_control IS
    PORT (
      clk: IN STD_LOGIC;
      aclr: IN STD_LOGIC;
      aload: IN STD_LOGIC;
      adata: IN STD_LOGIC;
      ena: IN STD_LOGIC;
       data: IN STD_LOGIC;
      q: OUT STD_LOGIC
    );
END dff_control;

ARCHITECTURE rtl OF dff_control IS
BEGIN
    PROCESS (clk, aclr, aload, adata)
    BEGIN
        IF (aclr = '1') THEN
          q <= '0';
        ELSIF (aload = '1') THEN
          q <= adata;
        ELSE
            IF (clk = '1' AND clk'event) THEN
                IF (ena ='1') THEN
                q <= data;
                END IF;
            END IF;
        END IF;
    END PROCESS;
END rtl;
```

The preset signal is not available in many device families, because it is replaced with the more flexible aload signal, so the preset signal is not included in the examples.

Creating many registers with different sload and sclr signals can make packing the registers into LABs difficult for the Quartus II Fitter because the sclr and sload signals are LAB-wide signals. In addition, using the LAB-wide sload signal prevents the Fitter from packing registers using the quick feedback path in the device architecture, which means that some registers can not be packed with other logic.

Therefore, synthesis tools typically avoid using the sload or sclear signal if there is space in the look-up table (LUT). Using the LUT to implement the signals is always more flexible if it is available. Synthesis tools also typically restrict use of sload and sclr signals to certain functions such as arithmetic chains (counters), or wide multiplexers in which there are enough registers with common signals to allow good LAB packing. Because different device families offer different numbers of control signals, inference of these signals is also device-specific. For example, Stratix II devices have more flexibility than Stratix devices with respect to secondary control signals, so synthesis tools might infer more sload and sclr signals for Stratix II devices.

If you use these additional control signals, use them in the priority order that matches the device architecture. To achieve the most efficient results, ensure the sclr signal has a higher priority than the sload signal in the same way that aclr has higher priority than aload in the previous examples. Remember that the register signals are not inferred unless the design meets the conditions described previously. However, if your HDL described the desired behavior, the software will always implement logic with the correct functionality.

In Verilog HDL, the following code for sload and sclr could replace the q <= data statement in the Verilog HDL example shown in Example 6–24 (after adding the control signals to the module declaration).

Example 6–26. Verilog HDL sload & sclr

```
if (sclr)
    q <= 1'b0;
else if (sload)
    q <= sdata;
else
    q <= data;
```

In VHDL, the following code for sload and sclr could replace the q <= data; statement in the VHDL example shown in Example 6–25 (after adding the control signals to the entity declaration).

Example 6–27. VHDL sload & sclr

```
IF (sclr = '1') THEN
    q <= '0';
ELSIF (sload = '1') THEN
    q <= sdata;
ELSE
    q <= data;
```

Tri-State Signals

When you are targeting Altera devices, you should use tri-state signals only when they are attached to top-level bidirectional or output pins. Avoid lower level bidirectional pins, and avoid using the Z logic value unless it is driving an output or bidirectional pin.

Synthesis tools implement designs with internal tri-state signals correctly in Altera devices using multiplexer logic, but Altera does not recommend this coding practice.

In hierarchical block-based or incremental design flows, a hierarchical boundary cannot contain any bidirectional ports, unless the lower level bidirectional port is connected directly through the hierarchy to a top-level output pin without connecting to any other design logic. If you use boundary tri-states in a lower level block, synthesis software must push the tri-states through the hierarchy to the top-level to make use of the tri-state drivers on output pins of Altera devices. Because pushing tri-states requires optimizing through hierarchies, lower level tri-states are restricted with block-based design methodologies.

The code examples shown in Examples 6–28 and 6–29 show Verilog HDL and VHDL code that creates tri-state bidirectional signals.

Example 6–28. Verilog HDL Tri-State Signal

```
module tristate (myinput, myenable, mybidir);
    input myinput, myenable;
    inout mybidir;
    assign mybidir = (myenable ? myinput : 1'bZ);
endmodule
```

Example 6–29. VHDL Tri-State Signal

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;

ENTITY tristate IS
PORT (
   mybidir : INOUT STD_LOGIC;
   myinput : IN STD_LOGIC;
   myenable : IN STD_LOGIC
    );
END tristate;

ARCHITECTURE rtl OF tristate IS
BEGIN
    mybidir <= 'Z' WHEN (myenable = '0') ELSE myinput;
END rtl;
```

Adder Trees

Structuring adder trees appropriately to match your targeted Altera device architecture can result in significant performance and density improvements. A good example of an application using a large adder tree is a finite impulse response (FIR) correlator. Using a pipelined binary or ternary adder tree appropriately can greatly improve the quality of your results.

This section explains why coding recommendations are different for Altera 4-input LUT devices, and the 6-input LUT logic structures currently available only in Stratix II devices.

Architectures with 4-Input LUTs in Logic Elements

Architectures such as the Stratix series, Cyclone series, APEX series, and FLEX series devices contain 4-input LUTs as the standard combinational structure in the LE.

If your design can tolerate pipelining, the fastest way to add three numbers `A`, `B`, and `C` in devices that use 4-input lookup tables is to add `A + B`, register the output, and then add the registered output to `C`. Adding `A + B` takes one level of logic (one bit is added in one LE), so this runs at full clock speed. This can be extended to as many numbers as desired.

In the code sample shown in Example 6–30, five numbers A, B, C, D, and E are added. Adding five numbers in devices that use 4-input lookup tables requires four adders and three levels of registers for a total of 64 LEs (for 16-bit numbers).

Example 6–30. Verilog HDL Pipelined Binary Tree

```
module binary_adder_tree (A, B, C, D, E, CLK, OUT);
    parameter WIDTH = 16;
    input [WIDTH-1:0] A, B, C, D, E;
    input CLK;
    output [WIDTH-1:0] OUT;

    wire [WIDTH-1:0] sum1, sum2, sum3, sum4;
    reg [WIDTH-1:0] sumreg1, sumreg2, sumreg3, sumreg4;
    // Registers

    always @ (posedge CLK)
        begin
            sumreg1 <= sum1;
            sumreg2 <= sum2;
            sumreg3 <= sum3;
            sumreg4 <= sum4;
        end

    // 2-bit additions
    assign sum1 = A + B;
    assign sum2 = C + D;
    assign sum3 = sumreg1 + sumreg2;
    assign sum4 = sumreg3 + E;
    assign OUT = sumreg4;
endmodule
```

Architectures with 6-Input LUTs in Adaptive Logic Modules

Because the Stratix II architecture uses a 6-input LUT in its basic logic structure, Stratix II devices benefit from a different coding style from the previous example presented for 4-input LUTs. Specifically, Stratix II device ALMs can simultaneously add three bits. Therefore, the tree in the previous example must be two levels deep and contain just two add-by-three inputs instead of four add-by-two inputs.

Although the code in the previous example compiles successfully for Stratix II devices, the code is inefficient and does not take advantage of the 6-input adaptive look-up table (ALUT). By restructuring the tree as a ternary tree, the design becomes much more efficient, significantly improving density utilization. Therefore, when you are targeting Stratix II devices, large pipelined binary adder trees designed for 4-input LUT architectures should be rewritten to take advantage of the Stratix II device architecture.

Example 6–31 uses just 32 ALUTs in a Stratix II device—more than a 4:1 advantage over the number of LUTs in the prior example implemented in a Stratix device.

You cannot pack a Stratix II LAB full when using this type of coding style because of the number of LAB inputs. However, in a typical design, the Quartus II Fitter can pack other logic into each LAB to take advantage of the unused ALMs.

Example 6–31. Verilog HDL Pipelined Ternary Tree

```
module ternary_adder_tree (A, B, C, D, E, CLK, OUT);
    parameter WIDTH = 16;
    input [WIDTH-1:0] A, B, C, D, E;
    input CLK;
    output [WIDTH-1:0] OUT;

    wire [WIDTH-1:0] sum1, sum2;
    reg [WIDTH-1:0] sumreg1, sumreg2;
    // Registers

    always @ (posedge CLK)
        begin
            sumreg1 <= sum1;
            sumreg2 <= sum2;
        end

    // 3-bit additions
    assign sum1 = A + B + C;
    assign sum2 = sumreg1 + D + E;
    assign OUT = sumreg2;
endmodule
```

These examples show pipelined adders, but partitioning your addition operations can help you achieve better results in nonpipelined adders as well. If your design is not pipelined, a ternary tree provides much better performance than a binary tree. For example, depending on your synthesis tool, the HDL code `sum = (A + B + C) + (D + E)` is more likely to create the optimal implementation of a 3-input adder for `A + B + C` followed by a 3-input adder for `sum1 + D + E` than the code without the parenthesis. If you do not add the parenthesis, the synthesis tool may partition the addition in a way that is not optimal for the architecture.

Coding Guidelines for Other Logic Structures

This section provides coding guidelines for the following logic structures.

- Latches—Altera recommends that you not use latches if possible, but this section also includes guidelines for using latches successfully if they are required.
- State Machines—This section helps you ensure the best results when you use state machines.
- Multiplexers—This section addresses common problems and provides design guidelines to achieve optimal resource utilization for multiplexer designs.
- Cyclic Redundancy Check Functions—This section provides guidelines for getting good results when designing CRC functions.

Latches

A latch is a small combinational loop that holds the value of a signal until a new value is assigned.

Altera recommends that you design without the use of latches whenever possible.

For additional information about the issues involved in designing with latches and all combinational loops, refer to the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Latches can be inferred from HDL code when you did not intend to use a latch as detailed in "Unintentional Latch Generation". If you do intend to infer a latch, it is important to infer it correctly to guarantee correct device operation as detailed in "Inferring Latches Correctly" on page 6–42.

Unintentional Latch Generation

When you are designing combinational logic, certain coding styles can create an unintentional latch. For example, when `CASE` or `IF` statements do not cover all possible input conditions, latches may be required to hold the output if a new output value is not assigned. Check your synthesis tool messages for references to inferred latches. If your code unintentionally creates a latch, make code changes to remove the latch.

Latches have limited support in formal verification tools. Therefore, ensure that you do not infer latches unintentionally, for example, through an incomplete `CASE` statement, when you are using formal verification in your design flow.

The full_case attribute can be used in Verilog HDL designs to treat unspecified cases as don't care values (X). However, using the full_case attribute can cause simulation mismatches because this attribute is a synthesis-only attribute, so simulation tools still treat the unspecified cases as latches.

Refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook* for more information about using attributes in your synthesis tool. The *Quartus II Integrated Synthesis* chapter provides an example explaining possible simulation mismatches.

Omitting the final ELSE or WHEN OTHERS clause in an IF or CASE statement can also generate a latch. Don't care (X) assignments on the default conditions are useful in preventing latch generation. For the best logic optimization, assign the default CASE or final ELSE value to don't care (X) instead of a logic value.

The VHDL sample code shown in Example 6–32 prevents unintentional latches. Without the final ELSE clause, this code creates unintentional latches to cover the remaining combinations of the sel inputs. When you are targeting a Stratix device with this code, omitting the final ELSE condition can cause the synthesis software to use up to six LEs instead of the three it uses with the ELSE statement. Additionally, assigning the final ELSE value to 1 instead of assigning the ELSE statement to the value of X can result in slightly more LEs because the synthesis software cannot perform as much optimization when you specify a constant value compared to a don't care value.

Example 6–32. VHDL Code Preventing Unintentional Latch Creation

```
LIBRARY ieee;
USE IEEE.std_logic_1164.all;

ENTITY nolatch IS
    PORT (a,b,c: IN STD_LOGIC;
        sel: IN STD_LOGIC_VECTOR (4 DOWNTO 0);
        oput: OUT STD_LOGIC);
END nolatch;

ARCHITECTURE rtl OF nolatch IS
BEGIN
    PROCESS (a,b,c,sel) BEGIN
        IF sel = "00000" THEN
            oput <= a;
        ELSIF sel = "00001" THEN
            oput <= b;
        ELSIF sel = "00010" THEN
            oput <= c;
        ELSE              --- Prevents latch inference
            oput <= ''X'; --/
        END IF;
    END PROCESS;
END rtl;
```

Inferring Latches Correctly

Synthesis tools can infer a latch that does not exhibit the problems typically associated with combinational loops.

When using Quartus II integrated synthesis, latches that are inferred by the software are reported in the **User-Specified and Inferred Latches** section of the Compilation Report. This report indicates whether the latch is safe and free of timing hazards.

If a latch or combinational loop in your design is not listed in the **User-Specified and Inferred Latches** report, it means that it was not inferred as a safe latch by the software and is not considered glitch-free.

All combinational loops listed in the **Analysis & Synthesis Logic Cells Representing Combinational Loops** table in the **Compilation Report** are at risk of timing hazards. These entries indicate possible problems with your design that you should investigate. However, it is possible to have a correct design that includes combinational loops. For example, it is possible that the combinational loop cannot be sensitized. This can occur in cases where there is an electrical path in the hardware, but either the designer knows that the circuit will never encounter data that causes that path to be activated, or the surrounding logic is set up in a mutually exclusive manner that prevents that path from ever being sensitized, independent of the data input.

For macrocell-based devices such as MAX® 7000AE and MAX 3000A, all data (D-type) latches and set-reset (S-R) latches listed in the **Analysis & Synthesis User-Specified and Inferred Latches** table have an implementation free of timing hazards such as glitches. The implementation includes a cover term to ensure there is no glitching, and includes a single macrocell in the feedback loop.

For 4-input LUT-based devices such as Stratix devices, the Cyclone series, and MAX II devices, all latches in the **User-Specified and Inferred Latches** table with a single LUT in the feedback loop are free of timing hazards when a single input changes. Because of the hardware behavior of the LUT, the output does not glitch when a single input toggles between two values that are supposed to produce the same output value. For example, a D-type input toggling when the enable input is inactive, or a set input toggling when a reset input with higher priority is active. This hardware behavior of the LUT means that no cover term is needed for a loop around a single LUT. The Quartus II software uses a single LUT in the feedback loop whenever possible. A latch that has data, enable, set, and reset inputs in addition to the output fed back to the input cannot be implemented in a single 4-input LUT. If the Quartus II software cannot implement the latch with a single-LUT loop because there are too many inputs, then the **User-Specified and Inferred Latches** table indicates that the latch is not free of timing hazards.

For 6-input LUT-based devices such as Stratix II, the software can implement all latch inputs with a single adaptive look-up table (ALUT) in the combinational loop. Therefore, all latches in the **User-Specified and Inferred Latches** table are free of timing hazards when a single input changes.

To ensure hazard-free behavior, only one control input may change simultaneously. Changing two inputs simultaneously, such as deasserting set and reset at the same time, or changing data and enable at the same time, can produce incorrect behavior in any latch.

Quartus II integrated synthesis infers latches from `always` blocks in Verilog HDL and `process` statements in VHDL, but not from continuous assignments in Verilog HDL or concurrent signal assignments in VHDL. These rules are the same as for register inference. The software infers registers or flipflops only from always blocks and process statements. The following examples infer latches.

Verilog HDL Set-Reset Latch Example

The Verilog HDL code sample shown in Example 6–33 infers a S-R latch correctly in the Quartus II software.

Example 6–33. Verilog HDL Set-Reset Latch

```
module simple_latch (
   input SetTerm,
   input ResetTerm,
   output reg LatchOut
   );

   always @ (SetTerm or ResetTerm) begin
      if (SetTerm)
         LatchOut = 1'b1;
      else if (ResetTerm)
         LatchOut = 1'b0;
      end
endmodule
```

HDL Data Type Latch Example

The VHDL code sample shown in Example 6–34 infers a D-type latch correctly in the Quartus II software.

Example 6–34. HDL Data Type Latch

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.all;

ENTITY simple_latch IS
   PORT (
      enable, data    : IN STD_LOGIC;
      q               : OUT STD_LOGIC
   );
END simple_latch;

ARCHITECTURE rtl OF simple_latch IS
BEGIN

latch : PROCESS (enable, data)
   BEGIN
      IF (enable = '1') THEN
         q <= data;
      END IF;
   END PROCESS latch;
END rtl;
```

The following example shows a Verilog HDL continuous assignment that does not infer a latch in the Quartus II software. The behavior is similar to a latch, but it may not function correctly as a latch and its timing is not analyzed as a latch.

```
assign latch_out = en ? data : latch_out;
```

The Quartus II integrated synthesis also creates safe latches when possible for instantiations of the `lpm_latch` megafunction. Use this megafunction to create a latch with any combination of data, enable, set, and reset inputs. The same limitations apply for creating safe latches as for inferring latches from HDL code.

Inferring the Altera `lpm_latch` function in another synthesis tool ensures that the implementation will also be recognized as a latch in the Quartus II software. If a third-party synthesis tool implements a latch using the `lpm_latch` megafunction, then the Quartus II integrated synthesis lists the latch in the **User-Specified and Inferred Latches** table in the same way as it lists latches created in HDL source code. The coding style necessary to produce an `lpm_latch` implementation may depend on your synthesis tool. Some third-party synthesis tools list the number of `lpm_latch` functions that are inferred.

If a latch is listed by the Quartus II integrated synthesis in the **User-Specified and Inferred Latches** table, and is implemented by Analysis & Synthesis as a safe latch, then physical synthesis netlist optimizations in the Fitter maintain the hazard-free performance.

For LUT-based families, the Fitter uses global routing for control signals including signals that Analysis & Synthesis identifies as latch enables. In some cases the global insertion delay may decrease the timing performance. If necessary, you can turn off the Quartus II **Global Signal** logic option to manually prevent the use of global signals. Global latch enables are listed in the **Global & Other Fast Signals** table in the Compilation Report.

State Machines

Synthesis tools can recognize and encode Verilog HDL and VHDL state machines during synthesis. This section presents guidelines to ensure the best results when you use state machines. Ensuring that your synthesis tool recognizes a piece of code as a state machine allows the tool to recode the state variables to improve the quality of results, and allows the tool to use the known properties of state machines to optimize other parts of the design. When synthesis recognizes a state machine it is often able to improve the design area and performance.

To achieve the best results, synthesis tools often use one-hot encoding for FPGA devices and minimal-bit encoding for CPLD devices, although the choice of implementation can vary for different state machines and different devices. Refer to your synthesis tool documentation for specific ways to control the manner in which state machines are encoded.

For information about state machine encoding in Quartus II integrated synthesis, refer to the *State Machine Processing* section in the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook.*

To ensure proper recognition and inference of state machines and to improve the quality of results, Altera recommends that you observe the following guidelines, which apply to both Verilog HDL and VHDL:

- Assign default values to outputs derived from the state machine so that synthesis does not generate unwanted latches.
- Separate the state machine logic from all arithmetic functions and data paths, including assigning output values.
- If your design contains an operation that is used by more than one state, define the operation outside the state machine and cause the output logic of the state machine use this value.
- Use a simple asynchronous or synchronous reset to ensure a defined power-up state. If your state machine design contains more elaborate reset logic, such as both an asynchronous reset and an asynchronous load, the Quartus II software generates regular logic rather than inferring a state machine.

If a state machine enters an illegal state due to a problem with the device, the design will likely cease to function correctly until the next reset of the state machine. Synthesis tools do not provide for this situation by default. The same issue applies to any other registers if there is some kind of fault in the system. A `default` or `when others` clause does not affect this operation, assuming that your design never deliberately enters this state. Synthesis tools remove any logic generated by a default state if it is not reachable by normal state machine operation.

Some synthesis tools have an option to implement a safe state machine that inserts the default case if it does not exist and preserves the logic in the design to handle illegal states. If a state machine gets into an illegal state for any reason, it returns to the reset state on the next clock edge. Of course this option protects only state machines, and all other registers in the design are not protected this way.

For additional information about tool-specific options for implementing state machines, refer to the tool vendor's documentation or the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

The following two sections "Verilog HDL State Machines" and "VHDL State Machines" describe additional language-specific guidelines and coding examples.

Verilog HDL State Machines

To ensure proper recognition and inference of Verilog HDL state machines, observe the following additional Verilog HDL guidelines. Some of these guidelines may be specific to Quartus II integrated synthesis. Refer to your synthesis tool documentation for specific coding recommendations.

- If you are using the SystemVerilog standard, use enumerated types to describe state machines (as shown in the "SystemVerilog State Machine Coding Example" on page 6–49).
- Represent the states in a state machine with the `parameter` data types in Verilog-1995 and -2001 and use the parameters to make state assignments (as shown below in the "Verilog HDL State Machine Coding Example"). This implementation makes the state machine easier to read and reduces the risk of errors during coding.

  Altera recommends against the direct use of integer values for state variables such as `next_state < = 0`. However, using an integer does not prevent inference in the Quartus II software.

- No state machine is inferred in the Quartus II software if the state transition logic uses arithmetic similar to that shown in the following example:

```
case (state)
    0: begin
        if (ena) next_state <= state + 2;
        else next_state <= state + 1;
    end
    1: begin
    ...
endcase
```

- No state machine is inferred in the Quartus II software if the state variable is an output.

Verilog HDL State Machine Coding Example

The following module `verilog_fsm` is an example of a typical Verilog HDL state machine implementation.

This state machine has five states. The asynchronous reset sets the variable state to `state_0`. The sum of `in1` and `in2` is an output of the state machine in `state_1` and `state_2`. The difference (`in1 - in2`) is

also used in state_1 and state_2. The temporary variables tmp_out_0 and tmp_out_1 store the sum and the difference of in1 and in2. Using these temporary variables in the various states of the state machine ensures proper resource sharing between the mutually exclusive states.

Example 6–35. Verilog-2001 State Machine

```
module verilog_fsm (clk, reset, in_1, in_2, out);
    input clk;
    input reset;
    input [3:0] in_1;
    input [3:0] in_2;output [4:0] out;
    parameter state_0 = 3'b000;
    parameter state_1 = 3'b001;
    parameter state_2 = 3'b010;
    parameter state_3 = 3'b011;
    parameter state_4 = 3'b100;

    reg [4:0] tmp_out_0, tmp_out_1, tmp_out_2;
    reg [2:0] state, next_state;

    always @ (posedge clk or posedge reset)
    begin
        if (reset)
            state <= state_0;
        else
            state <= next_state;
    end
    always @ (state or in_1 or in_2)
    begin
        tmp_out_0 = in_1 + in_2;
        tmp_out_1 = in_1 - in_2;
        case (state)
            state_0: begin
               tmp_out_2 <= in_1 + 5'b00001;
               next_state <= state_1;
            end
            state_1: begin
                if (in_1 < in_2) begin
                    next_state <= state_2;
                    tmp_out_2 <= tmp_out_0;
                end
                else begin
                    next_state <= state_3;
                    tmp_out_2 <= tmp_out_1;
                end
            end
            state_2: begin
                tmp_out_2 <= tmp_out_0 - 5'b00001;
                next_state <= state_3;
            end
            state_3: begin
                tmp_out_2 <= tmp_out_1 + 5'b00001;
                next_state <= state_0;
            end
            state_4:begin
```

```
                tmp_out_2 <= in_2 + 5'b00001;
                next_state <= state_0;
            end
            default:begin
                tmp_out_2 <= 5'b00000;
                next_state <= state_0;
            end
        endcase
    end
    assign out = tmp_out_2;
endmodule
```

An equivalent implementation of this state machine can be achieved by using `‘define` instead of the `parameter` data type, as follows:

```
‘define state_0 3'b000
‘define state_1 3'b001
‘define state_2 3'b010
‘define state_3 3'b011
‘define state_4 3'b100
```

In this case, the `state` and `next_state` assignments are assigned a `‘state_x` instead of a `state_x`, as shown in the following example:

```
next_state <= ‘state_3;
```

Although the `‘define` construct is supported, Altera strongly recommends the use of the parameter data type because doing so preserves the state names throughout synthesis.

SystemVerilog State Machine Coding Example

The module `enum_fsm` shown in Example 6–36 is an example of a SystemVerilog state machine implementation that makes use of enumerated types. Altera recommends using this coding style to describe state machines in SystemVerilog.

In Quartus II integrated synthesis, the enumerated type that defines the states for the state machine must be of an unsigned integer type as shown in Example 6–36. If you do not specify the enumerated type as `int unsigned`, a signed `int` type is used by default. In this case, the Quartus II integrated synthesis synthesizes the design, but does not recognize or infer a state machine.

Example 6–36. SystemVerilog State Machine Using Enumerated Types

```
module enum_fsm (input clk, reset, input int data[3:0], output int o);

   enum int unsigned { S0 = 0, S1 = 2, S2 = 4, S3 = 8 } state, next_state;

   always_comb begin : next_state_logic
      next_state = S0;
      case(state)
        S0: next_state = S1;
        S1: next_state = S2;
        S2: next_state = S3;
        S3: next_state = S3;
      endcase
   end

   always_comb begin
      case(state)
         S0: o = data[3];
         S1: o = data[2];
         S2: o = data[1];
         S3: o = data[0];
      endcase
   end

   always_ff@(posedge clk or negedge reset) begin
      if(~reset)
         state <= S0;
      else
         state <= next_state;
   end
endmodule
```

VHDL State Machines

To ensure proper recognition and inference of VHDL state machines, represent the states in a state machine with enumerated types and use the corresponding types to make state assignments. This implementation makes the state machine easier to read and reduces the risk of errors during coding. If the state is not represented by an enumerated type, synthesis software (such as Quartus II integrated synthesis) does not recognize the state machine. Instead, the state machine is implemented as regular logic gates and registers and the state machine is not listed as a state machine in the **Analysis & Synthesis** section of the Compilation Report.

VHDL State Machine Coding Example

The following entity, `vhd1_fsm`, is an example of a typical VHDL state machine implementation.

This state machine has five states. The asynchronous reset sets the variable state to state_0. The sum of in1 and in2 is an output of the state machine in state_1 and state_2. The difference (in1 - in2) is also used in state_1 and state_2. The temporary variables tmp_out_0 and tmp_out_1 store the sum and the difference of in1 and in2. Using these temporary variables in the various states of the state machine ensures proper resource sharing between the mutually exclusive states.

Example 6–37. VHDL State Machine

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;

ENTITY vhdl_fsm IS
   PORT(
      clk: IN STD_LOGIC;
      reset: IN STD_LOGIC;
      in1: IN UNSIGNED(4 downto 0);
      in2: IN UNSIGNED(4 downto 0);
      out_1: OUT UNSIGNED(4 downto 0)
      );
END vhdl_fsm;

ARCHITECTURE rtl OF vhdl_fsm IS
   TYPE Tstate IS (state_0, state_1, state_2, state_3, state_4);
   SIGNAL state: Tstate;
   SIGNAL next_state: Tstate;
BEGIN
   PROCESS(clk, reset)
   BEGIN
         IF reset = '1' THEN
            state <=state_0;
      ELSIF rising_edge(clk) THEN
            state <= next_state;
      END IF;
   END PROCESS;
   PROCESS (state, in1, in2)
      VARIABLE tmp_out_0: UNSIGNED (4 downto 0);
      VARIABLE tmp_out_1: UNSIGNED (4 downto 0);
   BEGIN
      tmp_out_0 := in1 + in2;
      tmp_out_1 := in1 - in2;
      CASE state IS
         WHEN state_0 =>
            out_1 <= in1;
            next_state <= state_1;
         WHEN state_1 =>
            IF (in1 < in2) then
               next_state <= state_2;
               out_1 <= tmp_out_0;
            ELSE
               next_state <= state_3;
               out_1 <= tmp_out_1;
            END IF;
```

```
         WHEN state_2 =>
            IF (in1 < "0100") then
               out_1 <= tmp_out_0;
            ELSE
               out_1 <= tmp_out_1;
            END IF;
               next_state <= state_3;
         WHEN state_3 =>
               out_1 <= "11111";
               next_state <= state_4;
         WHEN state_4 =>
               out_1 <= in2;
               next_state <= state_0;
         WHEN OTHERS =>
               out_1 <= "00000";
               next_state <= state_0;
      END CASE;
   END PROCESS;
END rtl;
```

Multiplexers

Multiplexers form a large portion of the logic utilization in many FPGA designs. By optimizing your multiplexer logic, you ensure the most efficient implementation in your Altera device. This section addresses common problems and provides design guidelines to achieve optimal resource utilization for multiplexer designs. The section also describes various types of multiplexers, and how they are implemented in the 4-input LUT found in many FPGA architectures, such as Altera's Stratix devices.

Stratix II devices have 6-input LUTs and are not specifically addressed here. Although many of the principles and techniques for optimization are similar, device utilization differs in the Stratix II 6-input LUT devices, for example, Stratix II devices can implement wider multiplexers in one ALM than can be implemented in the 4-input LUT of an LE.

Multiplexer Types

This first subsection addresses how multiplexers are created from various types of HDL code. `CASE` statements, `IF` statements, and state machines are all common sources of multiplexer logic in designs. These HDL structures create different types of multiplexers including binary multiplexers, selector multiplexers, and priority multiplexers. Understanding how multiplexers are created from HDL code and how they might be implemented during synthesis is the first step towards optimizing multiplexer structures for best results.

Binary Multiplexers

Binary multiplexers select inputs based on binary-encoded selection bits. The following "Verilog HDL Binary-Encoded Case Statement" example shows Verilog HDL code describing a simple 4:1 binary multiplexer.

Example 6–38. Verilog HDL Binary-Encoded Case Statement

```
case (sel)
   2'b00: z = a;
   2'b01: z = b;
   2'b10: z = c;
   2'b11: z = d;
endcase
```

A 4:1 binary multiplexer is efficiently implemented by using two 4-input LUTs. Larger binary multiplexers can be constructed that use the 4:1 multiplexer; constructing an *N*-input multiplexer (*N*:1 multiplexer) from a tree of 4:1 multiplexers can result in a structure using as few as 0.66*(*N* - 1) LUTs.

Selector Multiplexers

Selector multiplexers have a separate select line for each data input. The select lines for the multiplexer are one-hot encoded. The following "Verilog HDL One-Hot-Encoded Case Statement" example shows a simple Verilog HDL code example describing a one-hot selector multiplexer.

Example 6–39. Verilog HDL One-Hot-Encoded Case Statement

```
case (sel)
   4'b0001: z = a;
   4'b0010: z = b;
   4'b0100: z = c;
   4'b1000: z = d;
   default: z = 1'bx;
endcase
```

Selector multiplexers are commonly built as a tree of AND and OR gates. Using this scheme, two inputs can be selected using two select lines in a single 4-input LUT that uses two AND gates and an OR gate. The outputs of these LUTs can be combined with a wide OR gate. An *N*-input selector multiplexer of this structure requires at least 0.66*(*N*-0.5) LUTs, which is just slightly worse than the best binary multiplexer.

Priority Multiplexers

In priority multiplexers, the select logic implies a priority. The options to select the correct item must be checked in a specific order based on signal priority. These structures commonly are created from IF, ELSE, WHEN,

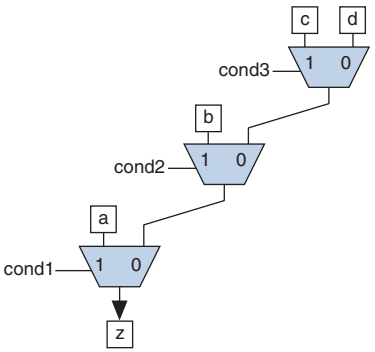
SELECT, or ? : statements in VHDL or Verilog HDL. The example VHDL code in the "VHDL IF Statement Implying Priority" section will probably result in the schematic implementation illustrated in Figure 6–2.

Example 6–40. VHDL IF Statement Implying Priority

```
IF cond1 THEN z <= a;
ELSIF cond2 THEN z <= b;
ELSIF cond3 THEN z <= c;
ELSE z <= d;
END IF;
```

The multiplexers shown in Figure 6–2 form a chain, evaluating each condition or select bit, one at a time.

Figure 6–2. Priority Multiplexer Implementation of an IF Statement



An *N*-input priority multiplexer uses a LUT for every 2:1 multiplexer in the chain, requiring *N*-1 LUTs. This chain of multiplexers generally increases delay because the critical path through the logic traverses every multiplexer in the chain.

To improve the timing delay through the multiplexer, avoid priority multiplexers if priority is not required. If the order of the choices is not important to the design, use a CASE statement to implement a binary or selector multiplexer instead of a priority multiplexer. If delay through the structure is important in a multiplexed design requiring priority, consider recoding the design to reduce the number of logic levels to minimize delay, especially along your critical paths.

Default or Others Case Assignment

To fully specify the cases in a CASE statement, include a DEFAULT (Verilog HDL) or OTHERS (VHDL) assignment. This assignment is especially important in one-hot encoding schemes where many combinations of the select lines are unused. Specifying a case for the unused select line combinations gives the synthesis tool information about how to synthesize these cases, and is required by the Verilog HDL and VHDL language specifications.

Some designs do not require that the outcome in the unused cases be considered, often because designers assume these cases will not occur. For these types of designs, you can choose any value for the DEFAULT or OTHERS assignment. However, be aware that the assignment value you choose can have a large effect on the logic utilization required to implement the design due to the different ways synthesis tools treat different values for the assignment, and how the synthesis tools use different speed and area optimizations.

In general, to obtain best results, explicitly define invalid CASE selections with a separate DEFAULT or OTHERS statement instead of combining the invalid cases with one of the defined cases.

If the value in the invalid cases is not important, specify those cases explicitly by assigning the X (don't care) logic value instead of choosing another value. This assignment allows your synthesis tool to perform the best area optimizations.

You can experiment with different DEFAULT or OTHERS assignments for your HDL design and your synthesis tool to test the effect they have on logic utilization in your design.

Implicit Defaults

The IF statements in Verilog HDL and VHDL can be a convenient way to specify conditions that do not easily lend themselves to a CASE-type approach. However, using IF statements can result in complicated multiplexer trees that are not easy for synthesis tools to optimize.

In particular, every IF statement has an implicit ELSE condition, even when it is not specified. These implicit defaults can cause additional complexity in a multiplexed design.

The following code in the "VHDL IF Statement with Implicit Defaults" example represents a multiplexer with four inputs (a, b, c, d) and one output (z).

Example 6–41. VHDL IF Statement with Implicit Defaults

```
IF cond1 THEN
   IF cond2 THEN
      z <= a;
   END IF;
ELSIF cond3 THEN
   IF cond4 THEN
      z <= b;
   ELSIF cond5 THEN
      z <= c;
   END IF;
ELSIF cond6 THEN
   z <= d;
END IF;
```

Although the code appears to implement a 4:1 multiplexer, each of the three separate IF statements in the code has an implicit ELSE condition that is not specified. Because the output values for the ELSE cases are not specified, the synthesis tool assumes the intent is to maintain the same output value for these cases.

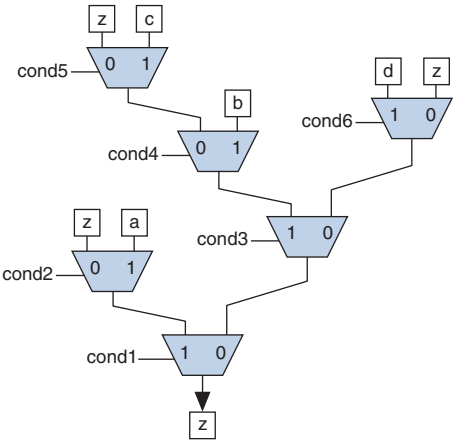
The code sample shown in Example 6–42 shows code with the same functionality as the code shown in Example 6–41, but specifies the ELSE cases explicitly.

Example 6–42. VHDL IF Statement with Default Conditions Explicitly Specified

```
IF cond1 THEN
   IF cond2 THEN
      z <= a;
   ELSE
      z <= z;
   END IF;
ELSIF cond3 THEN
   IF cond4 THEN
      z <= b;
   ELSIF cond5 THEN
      z <= c;
   ELSE
      z <= z;
   END IF;
ELSIF cond6 THEN
   z <= d;
ELSE
   z <= z;
END IF;
```

Figure 6–3 is a schematic representing the code in Example 6–42, which illustrates that the multiplexer logic is significantly more complicated than a basic 4:1 multiplexer, although there are only four inputs.

Figure 6–3. Multiplexer Implementation of an IF Statement with Implicit Defaults



There are several ways you can simplify the multiplexed logic and remove the unneeded defaults. The optimal method may be to recode the design so the logic takes the structure of a 4:1 `CASE` statement. Alternatively, if priority is important, you can restructure the code to deduce default cases and flatten the multiplexer. In this example, instead of `IF cond1 THEN IF cond2`, use `IF (cond1 AND cond2)` which performs the same function. In addition, examine whether the defaults are don't care cases. In this example, you can promote the last `ELSIF cond6` statement to an `ELSE` statement if no other valid cases can occur.

Avoid unnecessary default conditions in your multiplexer logic to reduce the complexity and logic utilization required to implement your design.

Degenerate Multiplexers

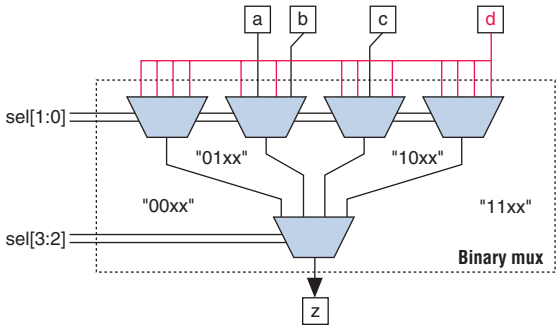
A degenerate multiplexer is a multiplexer in which not all of the possible cases are used for unique data inputs. The unneeded cases tend to contribute to inefficiency in the logic utilization for these multiplexers. You can recode degenerate multiplexers so they take advantage of the efficient logic utilization possible with full binary multiplexers.

The number of select lines in a binary multiplexer normally dictates the size of a multiplexer needed to implement the desired function. For example, the multiplexer structure represented in Figure 6–4 has four select lines capable of implementing a binary multiplexer with 16 inputs. However, the design does not use all 16 inputs, which makes this multiplexer a degenerate 16:1 multiplexer.

Example 6–43. VHDL CASE Statement Describing a Degenerate Multiplexer

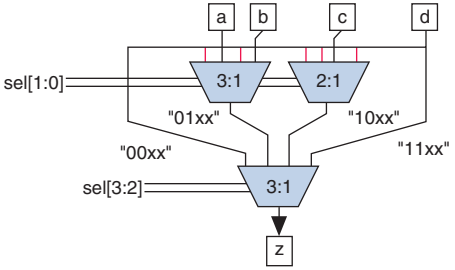
```
CASE sel[3:0] IS
   WHEN "0101" => z <= a;
   WHEN "0111" => z <= b;
   WHEN "1010" => z <= c;
   WHEN OTHERS => z <= d;
END CASE;
```

Figure 6–4. Binary Degenerate Multiplexer



In the example in Figure 6–4, the first and fourth multiplexers in the top level can easily be eliminated because all four inputs to each multiplexer are the same value, and the number of inputs to the other multiplexers can be reduced, as shown in Figure 6–5.

Figure 6–5. Optimized Version of the Degenerate Binary Multiplexer



Implementing this version of the multiplexer still requires at least five 4-input LUTs, two for each of the remaining 3:1 multiplexers and one for the 2:1 multiplexer. This design selects an output from only four inputs, a 4:1 binary multiplexer can be implemented optimally in two LUTs, so this degenerate multiplexer tree reduces the efficiency of the logic.

You can improve logic utilization of this structure by recoding the select lines to implement a full 4:1 binary multiplexer. The code sample shown in Example 6–44 shows a recoder design that translates the original select lines into a signal z_sel with binary encoding.

Example 6–44. VHDL Recoder Design for Degenerate Binary Multiplexer

```
CASE sel[3:0] IS
   WHEN "0101" => z_sel <= "00";
   WHEN "0111" => z_sel <= "01";
   WHEN "1010" => z_sel <= "10";
   WHEN OTHERS => z_sel <= "11";
END CASE;
```

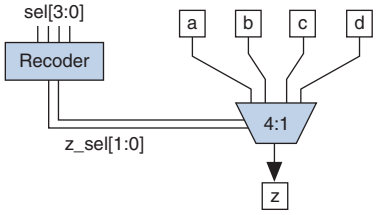
The code sample shown in Example 6–45 shows you how to implement the full binary multiplexer.

Example 6–45. VHDL 4:1 Binary Multiplexer Design

```
CASE z_sel[1:0] IS
   WHEN "00" => z <= a;
   WHEN "01" => z <= b;
   WHEN "10" => z <= c;
   WHEN "11" => z <= d;
END CASE;
```

Use the new z_sel control signal from the recoder design to control the 4:1 binary multiplexer that chooses between the four inputs a, b, c, and d, as illustrated in Figure 6–6. The complexity of the select lines is handled in the recoder design, and the data multiplexing is performed with simple binary select lines enabling the most efficient implementation.

Figure 6–6. Binary Multiplexer with Recorder



The design for the recoder can be implemented in two LUTs and the efficient 4:1 binary multiplexer uses two LUTs, for a total of four LUTs. The original degenerate multiplexer required five LUTs, so the recoded version uses 20% less logic than the original.

You can often improve the logic utilization of multiplexers by recoding the select lines into full binary cases. Although logic is required to perform the encoding, the overall logic utilization is often improved.

Buses of Multiplexers

The inputs to multiplexers are often data input buses in which the same multiplexer function is performed on a set of data input buses. In these cases, any inefficiency in the multiplexer is multiplied by the number of bits in the bus. The issues described in the previous sections become even more important for wide multiplexer buses.

For example, the recoding of select lines into full binary cases detailed in the previous section can often be used in multiplexed buses. Recoding the select lines may need to be completed only once for all the multiplexers in the bus. By sharing the recoder logic among all the bits in the bus, you can greatly improve the logic efficiency of a bus of multiplexers.

The degenerate multiplexer in the previous section requires five LUTs to implement. If the inputs and output are 32 bits wide, the function could require 32 × 5 or 160 LUTs for the whole bus. The recoder design uses only two LUTs, and the select lines only need to be recoded once for the entire bus. The binary 4:1 multiplexer requires two LEs per bit of the bus. The total logic utilization for the recoded version could be 2 + (2 x 32) or 66 LUTs for the whole bus, compared to 160 LUTs for the original version. The logic savings become more important with wide multiplexer buses.

Using techniques to optimize degenerate multiplexers, removing unneeded implicit defaults, and choosing the optimal `DEFAULT` or `OTHERS` case can play an important role when optimizing buses of multiplexers.

Quartus II Software Option for Multiplexer Restructuring

Quartus II integrated synthesis provides the **Restructure Multiplexers** logic option that extracts and optimizes buses of multiplexers during synthesis. In certain situations, this option automatically performs some of the recoding functions described without changing the HDL code in your design. This option is on by default, when the Optimization technique is set to **Balanced** (the default for most device families) or set to **Area**.

For details, refer to the *Restructure Multiplexers* subsection in the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

Cyclic Redundancy Check Functions

Cyclic redundancy check (CRC) computations are used heavily by communications protocols and storage devices to detect any corruption of the data. These functions are highly effective; there is a very low probability that corrupted data can pass a 32-bit CRC check.

CRC functions typically use wide XOR gates to compare the data. The way that synthesis tools flatten and factor these XOR gates to implement the logic in FPGA LUTs can greatly impact the area and performance results for the design. XOR gates have a cancellation property which creates an exceptionally large number of reasonable factoring combinations, so synthesis tools can not always choose the best result by default.

The 6-input ALUT in Stratix II devices has a significant advantage over 4-input LUTs for these designs. When properly synthesized, CRC processing designs can run at high speeds in Stratix II devices.

The following guidelines will help you improve the quality of results for CRC designs in Altera devices.

If Performance is Important, Optimize for Speed

Synthesis tools flatten XOR gates to minimize area and depth of levels of logic. Synthesis tools such as Quartus II integrated synthesis target area optimization by default for these logic structures. Therefore, for more focus on depth reduction, set the synthesis optimization technique to speed.

Note that flattening for depth sometimes causes a significant increase in area.

Use Separate CRC Blocks Instead of Cascaded Stages

Some designers optimize their CRC designs to use cascaded stages, for example 4 stages of 8 bits. In such designs, intermediate calculations are used as needed (such as the calculations after 8, 24, or 32 bits) depending on the data width. This design is not optimal in FPGA devices. The XOR cancellations that can be performed in CRC designs mean that the function does not require all the intermediate calculations to determine the final result. Therefore forcing the use of intermediate calculations increases the area required to implement the function, as well as increasing the logic depth because of the cascading. It is typically better to create full separate CRC blocks for each data width that you need in the design, then multiplex them together to choose the appropriate mode at a given time.

Use Separate CRC Blocks Instead of Allowing Blocks to Merge

Synthesis tools often attempt to optimize CRC designs by sharing resources and extracting duplicates in usually two different CRC blocks because of the factoring options in the XOR logic. As addressed previously, the CRC logic allows significant reductions but this works best when each CRC function is optimized separately. Check for duplicate extraction behavior if you have different CRC functions that are driven by common data signals or that feed the same destination signals.

If you are having problems with quality of results and you see that two CRC functions are sharing logic, ensure that the blocks are synthesized independently using one of the following methodologies:

- Synthesize each CRC block as a separate project and then write a separate VQM or EDIF netlist file for each.
  - To create a VQM file using Quartus II integrated synthesis, on the Processing menu click **Start**, then click **Start VQM Writer**.
- Define each CRC block as a separate design partition in an incremental compilation design flow.
  - For details, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.
- Use synthesis options to preserve the hierarchical boundary of the CRC block.
  - On the Assignments menu, click **Assignment Editor**. Set **Preserve Hierarchical Boundary** to **Firm**.

Take Advantage of Latency if Available

If your design can use more than one cycle to implement the CRC functionality, adding registers and retiming the design can help reduce area, improve performance and reduce power utilization. If your synthesis tool offers a retiming feature (such as the Quartus II software **Perform gate-level register retiming** option), you can insert an extra bank of registers at the input and allow the retiming feature to move the registers for better results. You can also build the CRC unit half as wide and alternate between halves of the data in each clock cycle.

Save Power by Disabling CRC Blocks When Not in Use

CRC designs are heavy consumers of dynamic power because the logic toggles whenever there is a change in the design. To save power, use clock enables to disable the CRC function for every clock cycle that the logic is not needed. Some designs don't check the CRC results for a few clock cycles while other logic is performed. It is valuable to disable the CRC function even for this short amount of time.

Use the Device Synchronous Load (sload) Signal to Initialize

The data in many CRC designs must be initialized to `1`'s before operation. If your target device supports the use of the `sload` signal, you should use it to set all the registers in your design to `1`'s before operation. To enable use of the `sload` signal, follow the coding guidelines presented in the "Secondary Register Control Signals Such as Clear & Clock Enable" on page 6–32 section. You can check the register equations in the Timing Closure Floorplan or the Chip Editor to ensure that the signal was used as expected.

If you must force a register implementation using an `sload` signal, you can use low-level device primitives as described in the *Introduction to Low-Level Primitives Design User Guide*.

Conclusion

Because coding style and megafunction implementation can have such large effects on your design performance, it is important to match the coding style to the device architecture from the very beginning of the design process. To improve design performance and area utilization, take advantage of advanced device features, such as memory and DSP blocks, as well as the logic architecture of the targeted Altera device by following the coding recommendations presented in this chapter.

For additional optimization recommendations, refer to the *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Section III. Synthesis

As programmable logic devices (PLDs) become more complex and require increased performance, advanced design synthesis has become an important part of the design flow. In the Quartus® II software you can use the Analysis & Synthesis module of the Compiler to analyze your design files and create the project database. You can also use other EDA synthesis tools to synthesize your designs, and then generate EDIF netlist files or VQM files that can be used with the Quartus II software. This section explains the options that are available for each of these flows, and how they are supported in the Quartus II, version 6.0 software.

This section includes the following chapters:

The previously documented chapter, *Synopsys FPGA Compiler II BLIS & Quartus II LogicLock™ Design Flow*, has been removed from the Quartus II Handbook version 5.1.

Revision History

The table below shows the revision history for Chapter 7 to 12.

Chapter(s)	Date / Version	Changes Made
7	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Added language support. • Added Quartus II Synthesis options. • Added information on setting other Quartus II options in HDL source code.
	December 2005 v5.1.1	Minor typographic update.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 7 was formerly Chapter 8 in version 5.0.
	May 2005 v5.0.0	• Chapter 8 was formerly Chapter 6 in version 4.2. • Updated information. • Updated figures. • Restructured information. • Renamed sections. • New functionality for Quartus II software 5.0.
	Dec. 2004 v3.0	• Chapter 7 was formerly Chapter 8 in version 4.1. • Added documentation of incremental synthesis feature • New functionality for Quartus II software version 4.2
	June 2004 v2.0	• Updates to tables, figures. • New functionality for Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
8	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Updated cross probling information. • Added NativeLink® integration information. • Added Synplify design flow support. • Added Altera megafunction guidelines and architecture-specific features.
	December 2005 v5.1.1	Minor typographic update.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 8 was formerly chapter 9 in version 5.0.
	May 2005 v5.0.0	Chapter 9 was formerly chapter 7 in version 4.2.
	Dec. 2004 v2.1	• Chapter 8 was formerly Chapter 9 in version 4.1. • Updated information. • New functionality for Quartus II software version 4.2. • Updated figure 8-1.
	June 2004 v2.0	• Updates to tables, figures. • New functionality for Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.

Chapter(s)	Date / Version	Changes Made
9	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 9 was formerly Chapter 10 in version 5.0.
	May 2005 v5.0.0	Chapter 10 was formerly chapter 8 in version 4.2.
	Dec. 2004 v2.1	• Chapter 9 was formerly Chapter 10 in version 4.1. • Updates to tables and figures. • New functionality for Quartus II software version 4.2.
	June 2004 v2.0	• Updates to tables and figures. • New functionality for Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
10	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 10 was formerly chapter 11 in version 5.0.
	May 2005 v5.0.0	Chapter 11 was formerly chapter 9 in version 4.2.
	Dec. 2004 v2.1	• Chapter 10 was formerly Chapter 11 in version 4.1. • Updated information. • New functionality in Quartus II software version 4.2. • Updated tables and figures.
	June 2004 v2.0	• Updates to tables, and figures. • New functionality for Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
11	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 11 was formerly chapter 13 in version 5.0.
	May 2005 v5.0.0	Chapter 13 was formerly chapter 11 in version 4.2.
	Dec. 2004 v1.1	• Chapter 12 was formerly Chapter 13 in version 4.1. • Updated information. • New functionary for Quartus II software version 4.2. • Moved figure 12-3 within the chapter.
	June 2004 v1.0	Initial release.

Chapter(s)	Date / Version	Changes Made
12	May 2006 v6.0.0	Name changed to *Analyzing Designs with the Quartus II Netlist Viewers*. Updated for the Quartus II software version 6.0.0: • Updated GUI information.
	December 2005, v5.1.1	Updated for version 5.1, including viewing inside device atoms, filter on bus index, display timing path in the RTL Viewer, state machine access from Tools menu, locate from state machines, and state encoding table.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 12 was formerly chapter 14 in version 5.0.
	May 2005 v5.0.0	Chapter 14 was formerly chapter 12 in version 4.2.
	Dec. 2004 v2.1	• Chapter 13 was formerly Chapter 14 in version 4.1. • Updates to tables and figures. • New functionality for Quartus II software version 4.2.
	June 2004 v 2.0	• Updates to tables, and figures. • New functionality for Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.

7. Quartus II Integrated Synthesis

QII51008-6.0.0

Introduction

As programmable logic designs become more complex and require increased performance, advanced synthesis has become an important part of the design flow. The Quartus® II software includes advanced integrated synthesis that fully supports VHDL and Verilog HDL, as well as Altera®-specific design entry languages, and provides options to control the synthesis process. With this synthesis support, the Quartus II software provides a complete, easy-to-use solution.

This chapter documents the design flow and language support in the Quartus II software. It explains how to improve and control your Quartus II synthesis results with incremental synthesis. Additionally, you can improve synthesis results with Quartus II synthesis options and by controlling the inference of architecture-specific megafunctions. This chapter also explains some of the node-naming conventions used during synthesis to help you better understand your synthesized design, and the messages issued during synthesis to improve your HDL code. Scripting techniques for applying all the options and settings described are also provided.

This chapter contains the following sections:

- Design Flow
- Language Support
- Incremental Synthesis
- Quartus II Synthesis Options
- Setting Other Quartus II Options in Your HDL Source Code
- Analyzing Synthesis Results
- VHDL & Verilog HDL Messages
- Node-Naming Conventions in Quartus II Integrated Synthesis
- Scripting Support

Design Flow

The Quartus II Analysis & Synthesis process includes Quartus II integrated synthesis, which fully supports the Verilog HDL and VHDL languages as well as Altera-specific languages (refer to "Language Support" on page 7–5 for details), and supports a subset of the SystemVerilog language. This stage of the compilation flow performs logic synthesis to optimize design logic, and performs technology mapping to implement the design logic using device resources such as logic elements (LEs) or adaptive logic modules (ALMs). This stage also generates the single project database that integrates all the design files in a project (including any netlists from third-party synthesis tools).

You can use the Analysis & Synthesis stage of the Quartus II compilation to perform any of the following levels of analysis and synthesis:

- **Analyze Current File**—Parse the current design source file to check for syntax errors. This command does not report on many semantic errors that require further design synthesis. On the Processing menu, click **Analyze Current File**.
- **Analysis & Elaboration**—Check a design for syntax and semantic errors and perform elaboration. On the Processing menu, click **Start**, and then click **Start Analysis & Elaboration**.
- **Analysis & Synthesis**—Perform complete analysis and synthesis on a design, including technology mapping. On the Processing menu, point to **Start**, and then click **Start Analysis & Synthesis**. This is the most commonly used command and is part of the full compilation flow.

The Quartus II design and compilation flow using Quartus II integrated synthesis is made up of the following steps:

1. Create a project in the Quartus II software, and specify the general project information, including the top-level design entity name.
2. Create design files in the Quartus II software or with a text editor.
3. Add all design files to your Quartus II project using the **Files** page of the Settings dialog box.
4. Specify compiler settings that control the compilation and optimization of the design during synthesis and fitting. For synthesis settings, refer to "Quartus II Synthesis Options" on page 7–20.
5. Compile the design in the Quartus II software. To synthesize the design, on the Processing menu, point to Start, and click **Start Analysis & Synthesis**.

On the Processing menu, click **Start Compilation** to run a complete compilation flow including placement, routing, creation of a programming file, and timing analysis.

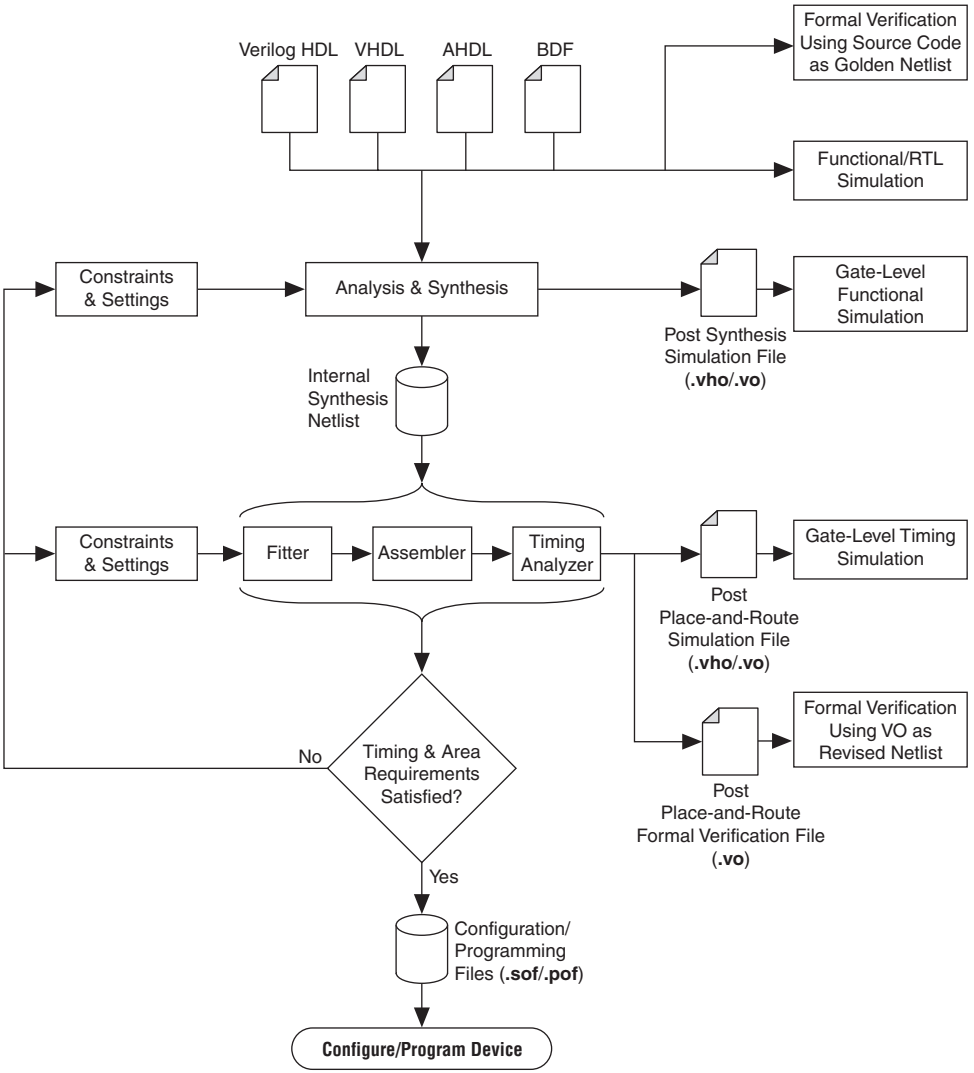
6. After obtaining synthesis and place-and-route results that meet your needs, program the Altera device.

The software provides netlists that allow you to perform functional simulation and gate-level timing simulation in the Quartus II simulator or a third-party simulator, perform timing analysis in a third-party timing analysis tool in addition to the TimeQuest or Classic Timing Analyzer, and/or perform formal verification in a third-party formal verification tool. The Quartus II software also provides many additional analysis and debugging features.

For more information about creating a project, compilation flow, and other features in the Quartus II software, refer to the Quartus II Help. For an overall summary of Quartus II features, refer to the *Introduction to Quartus II Manual*.

Figure 7–1 shows the basic design flow using Quartus II integrated synthesis.

Figure 7–1. Quartus II Design Flow Using Quartus II Integrated Synthesis



Language Support

This section explains the Quartus II software's integrated synthesis support for HDL and schematic design entry. You can mix all supported languages, and netlists generated by third-party synthesis tools, in a single Quartus II project.

Verilog HDL Support

The Quartus II Compiler's analysis and synthesis module supports the following Verilog HDL standards:

- Verilog-1995 (IEEE Standard 1364-1995)
- Verilog-2001 (IEEE Standard 1364-2001)
- SystemVerilog-2005 (IEEE Standard 1800-2005) (only certain constructs are supported)

Refer to the subsections that follow for more info about language support.

For complete information about specific syntax features and language constructs, refer to the Quartus II Help.

To specify a default Verilog HDL version for all files, perform the following steps:

1. On the Assignments menu, click **Settings**.
2. In the Settings dialog box, under Category, expand **Analysis & Synthesis Settings**, and select **Verilog HDL Input**, then click **OK**.
3. On the **Verilog HDL Input** page, under **Verilog version**, select the appropriate Verilog version, then click **OK**.

You can also specify the Verilog HDL version for each design file using a synthesis directive. For details, refer to "Specifying Verilog & VHDL Versions for Each Design File" on page 7–24.

The Quartus II Compiler uses the Verilog-2001 standard by default.

The Verilog HDL code samples provided in this document follow the Verilog-2001 standard unless otherwise specified.

The Quartus II software support for Verilog HDL is case-sensitive in accordance with the Verilog HDL standard.

The Quartus II software supports the `include` compiler directive to include files with absolute paths (with either "/" or "\" as the separator), or relative paths (relative to project root or current file location). When

searching for a relative path, the Quartus II software first searches relative to the project directory. If the software cannot find the file, it then searches relative to the directory location of the file.

Verilog-2001 Support

The Quartus II software does not support Verilog-2001 libraries and configurations.

SystemVerilog Support

The Quartus II software supports the following SystemVerilog constructs:

- Built-in data types `logic`, `bit`, `byte`, `shortint`, `longint`, `int`
- Enumeration data types using `enum` (no support for enum methods)
- Structure data types using `struct`
- Unpacked and packed arrays (no support for packed arrays with more than one dimension)
- User-defined types using `typedef` (no support for global typedefs or forward type declarations)
- Coding constructs `always_comb`, `always_latch`, `always_ff`
- Assignment operators +=, -=, *=, /=, %=, &=, |=, ^=, <<=, >>=, <<<=, and >>>=
- Increment ++ and decrement --
- Assignment patterns (no support for patterns that specify default, member name, or type)
- Keywords `unique` and `priority` in case statements
- Default values for function/task arguments

Designs written to comply with the Verilog-2001 standard may not compile successfully using the SystemVerilog setting because the SystemVerilog standard adds a number of new reserved keywords. For a list of reserved words in each language standard, refer to the Quartus II Help.

Verilog HDL Macros

The Quartus II software supports the compiler directive `` `define ``, in accordance with the Verilog HDL standard. The Quartus II software also provides an equivalent Verilog HDL macro that you can turn on or off via the GUI or from the command line.

Specifying a Verilog Macro in the GUI
To specify a macro in the GUI, on the Assignments menu, click **Settings**. Under **Category**, expand **Analysis & Synthesis Settings** and click **Verilog HDL Input**. Under **Verilog HDL macro**, type the macro name in the **Setting** box, and click **Add**.

Specifying a Verilog Macro on the Command Line
Type the command shown in Example 7–1 at the command prompt to specify a Verilog macro.

Example 7–1. Command Syntax for Specifying a Verilog Macro

```
quartus_map <Design name> --verilog_macro= "<Macro Name>=<Macro Setting>" ↵
```

For example, the command in Example 7–2 has the same effect as specifying `` `define a=2 `` in the Verilog HDL source code:

Example 7–2. Specifying a Verilog Macro a = 2

```
quartus_map my_design --verilog_macro="a=2" ↵
```

To specify multiple macros, you can repeat the option more than once, as in Example 7–3:

Example 7–3. Specifying Verilog Macros a = 2 & a = 3

```
quartus_map my_design --verilog_macro="a=2" --verilog_macro="b=3" ↵
```

VHDL Support

The Quartus II Compiler's analysis and synthesis module supports the following VHDL standards:

- VHDL 1987 (IEEE Standard 1076-1987)
- VHDL 1993 (IEEE Standard 1076-1993)

For information about specific syntax features and language constructs, refer to the Quartus II Help.

To specify a default VHDL version for all files, perform the following steps:

1. On the Assignments menu, click **Settings**.

2. In the Settings dialog box, under Category, expand **Analysis & Synthesis Settings**, and select **VHDL Input**, then click **OK**.

3. On the **VHDL Input** page, under **VHDL version**, select the appropriate version, then click **OK**.

4. You can also specify the VHDL version for each design file using a synthesis directive.

For details, refer to "Specifying Verilog & VHDL Versions for Each Design File" on page 7–24. The Quartus II Compiler uses the VHDL 1993 standard by default.

The VHDL code samples provided in this document follow the VHDL 1993 standard.

VHDL Libraries

The Quartus II software includes the standard IEEE libraries and a number of vendor-specific VHDL libraries. You can also create custom VHDL libraries to store your own VHDL design units.

The **IEEE** library includes the standard VHDL packages `std_logic_1164`, `numeric_std`, `numeric_bit`, and `math_real`. The **STD** library is part of the VHDL language standard and includes packages `standard` (included in every project by default) and `textio`. For compatibility with older designs, the Quartus II software also supports the following vendor-specific packages and libraries:

- Synopsys packages such as `std_logic_arith` and `std_logic_unsigned` in the **IEEE** library
- Mentor Graphics® packages such as `std_logic_arith` in the **ARITHMETIC** library
- Altera primitive packages `altera_primitives_components` (for primitives such as `GLOBAL` and `DFFE`) and `maxplus2` (for legacy support of MAX+PLUS® II primitives) in the **ALTERA** library
- Altera megafunction packages `altera_mf_components` and `stratixgx_mf_components` in the **ALTERA_MF** library (for Altera-specific megafunctions including LCELL), and `lpm_components` in the **LPM** library for library of parameterized modules (LPM) functions.

For a complete listing of library and package support, refer to the Quartus II Help.

Beginning with the Quartus II software version 5.1, you should import component declarations for Altera primitives such as `GLOBAL` and `DFFE` from the `altera_primitives_components` package and not the `altera_mf_components` package.

To ensure that the software reads all associated project files, add each VHDL file to your Quartus II project. To add files to your project, on the Project menu, click **Add/Remove Files In Project**.

Beginning in the Quartus II software version 5.1, VHDL design files can be added to the project in any order.

By default, the Quartus II software compiles all VHDL files into the work library. If a VHDL file refers to a library that does not exist, or if the library does not contain a referenced design unit, then the software searches the work library. This default behavior allows the Quartus II software to compile most VHDL designs with minimal setup.

To compile your VHDL design files into specific libraries, you can specify a destination library for each design file in one of the following ways:

- In the **Settings** dialog box
- In the Quartus II Settings File (**.qsf**)
- With a Tcl command
- In the VHDL file itself, with a synthesis directive

When the Quartus II Compiler analyzes the file, it stores the analyzed design units in the file's destination library.

A VHDL design cannot contain two or more entities with the same name, even if they are compiled into separate custom libraries.

Specifying a Destination Library Name in the Settings Dialog Box
To specify a library name for one of your VHDL files:

1. From the Assignments menu, choose **Settings**.
2. On the **Files** page of the **Settings** dialog box, specify the library name in the **File Name** list.
3. Click **Properties**.
4. In the **File Properties** dialog box, from the **Type** list, select **VHDL File**.

5. Type the desired library name in the **Library** field.

6. Click **OK**.

Specifying a Destination Library Name in the Quartus II Settings File or Using Tcl

You can specify the VHDL library name with the `-library` option to the `VHDL_FILE` assignment in the Quartus II Setting File or with Tcl commands.

For example, the following Quartus II Settings File or Tcl assignment specifies that the Quartus II software analyze **my_file.vhd** and store its contents (design units) in the VHDL library **my_lib**.

Example 7–4. Specifying a Destination Library Name

```
set_global_assignment VHDL_FILE my_file.vhd –library my_lib
```

For more information about Tcl scripting, refer to "Scripting Support" on page 7–70.

Specifying a Destination Library Name in Your VHDL File

You can use the `library` synthesis directive to specify a library name in your VHDL source file. This directive takes a single string argument: the name of the destination library. Specify the `library` directive in a VHDL comment prior to the context clause for a primary design unit (that is, a package declaration, an entity declaration, or a configuration), using one of the supported keywords for synthesis directives, that is, `altera`, `synthesis`, `pragma`, `synopsys`, or `exemplar`.

For more information about specifying synthesis directives, refer to "Synthesis Directives" on page 7–24.

The `library` directive overrides the default library destination **work**, the library setting specified for the current file through the **Settings** dialog box, an existing Quartus II Settings File setting, setting made through the Tcl interface, or any prior `library` directive in the current file. The directive remains effective until the end of the file or the next `library` synthesis directive.

Example 7–5 uses the `library` synthesis directive to create a library called **my_lib** that contains the design unit `my_entity`.

Example 7–5. Using the library Synthesis Directive

```
-- synthesis library my_lib
library ieee;
use ieee.std_logic_1164.all;
entity my_entity(...)
end entity my_entity;
```

You can specify a single destination library for all the design units in a given source file by specifying the library name in the the **Settings** dialog box, editing the Quartus II Settings File, or using the Tcl interface. Using the `library` directive to change the destination VHDL library within a source file gives you the option to organizing the design units in a single file into different libraries, rather than just a single library.

The Quartus II software gives an error if you use the library directive within a design unit.

AHDL Support

The Quartus II Compiler's analysis and synthesis module fully supports the Altera Hardware Description Language (AHDL).

AHDL designs use Text Design Files (**.tdf**). You can import AHDL Include Files (**.inc**) into a Text Design File with an AHDL `include` statement. Altera provides AHDL Include Files for all megafunctions shipped with the Quartus II software.

For information about specific syntax features and language constructs, refer to the Quartus II Help.

The AHDL language does not support the synthesis directives or attributes described in this chapter.

Schematic Design Entry Support

The Quartus II Compiler's analysis and synthesis module fully supports Block Design Files (**.bdf**) for schematic design entry.

Use the Quartus II software's Block Editor to create and edit Block Design Files and open Graphic Design Files (**.gdf**) imported from the MAX+PLUS II software. Use the Symbol Editor to create and edit Block Symbol Files (**.bsf**) and open MAX+PLUS II Symbol Files (**.sym**). You can

read and edit these legacy MAX+PLUS II formats with the Quartus II Block and Symbol Editors; however, the Quartus II software saves them as BDF or BSF files.

For information about creating and editing schematic designs, refer to the Quartus II Help.

Schematic entry methods do not support the synthesis directives or attributes described in this chapter.

Incremental Synthesis

The incremental synthesis feature in the Quartus II software manages a design hierarchy for incremental design by allowing you to divide the design into multiple partitions. Incremental synthesis ensures that when a design is compiled, only those partitions of the design that have been updated will be resynthesized, reducing synthesis time and runtime memory usage. You can change and resynthesize a design partition without affecting other design partitions, which means that node names are maintained during synthesis for all registered and combinational nodes in unchanged partitions.

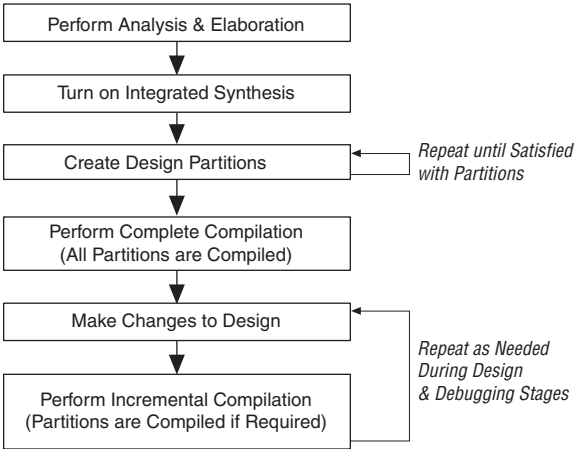
Conventionally, a hierarchical design is flattened into a single netlist of logic gates before logic synthesis and technology mapping. However, incremental synthesis allows you to partition a hierarchical design along any of its hierarchical boundaries. The individual hierarchical partitions are synthesized and mapped separately by the Quartus II software. The hierarchical partitions are then combined—or merged—to form a flattened netlist for further stages of the Quartus II compilation flow, including fitting. The mapped netlist for each partition is stored by the Quartus II software. Therefore, if the source code for one partition changes during the design cycle, only the partition that changed is resynthesized during the next compilation of the design.

You can use incremental synthesis by itself, or use a full incremental compilation flow in which you also preserve the placement and potentially routing information for unchanged partitions.

This chapter describes incremental synthesis only. For information about the full incremental compilation flow, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

The flow chart in Figure 7–2 shows the steps in the incremental synthesis flow.

Figure 7–2. Summary of Design Flow Using Quartus II Incremental Synthesis Flow

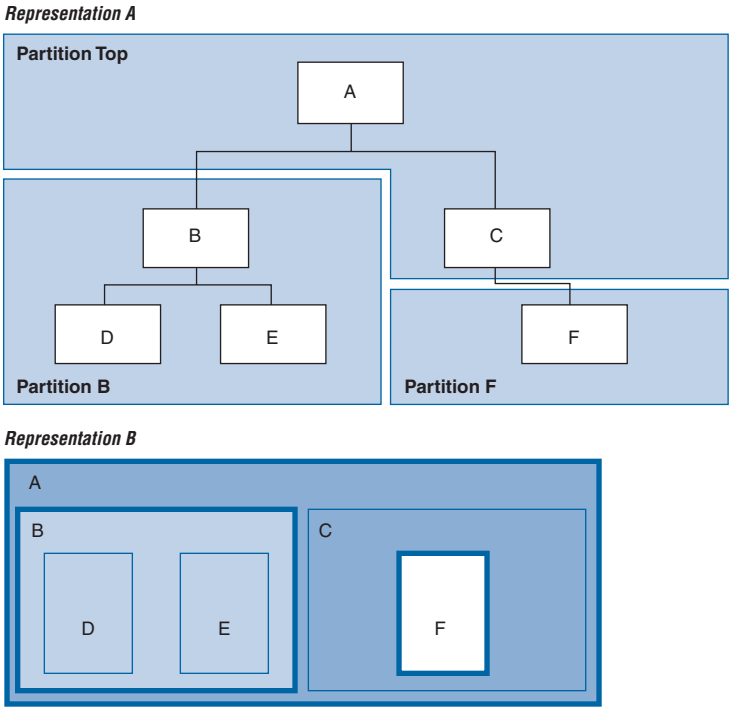


Partitions for Incremental Synthesis

A partition represents a portion of the design that you want to synthesize incrementally. Partitions must be bounded by hierarchical boundaries, and therefore, cannot be a portion of the logic within a hierarchical block. When a partition is declared, every hierarchical block within that partition becomes part of the same partition. You can create new partitions for hierarchical blocks within an existing partition, in which case the blocks designates as a new partition are no longer part of the higher-level partition.

In Figure 7–3, hierarchical entities B and F form partitions in the complete design, which is made up of entities A, B, C, D, E, and F. The shaded boxes in Representation A indicate design partitions in a "tree" representation of the hierarchy. In Representation B, the lower-level entities are represented inside of higher-level entities, and the partitions are illustrated with different colored shading. The top-level partition Top automatically contains the top-level entity in the design, and any logic that is not defined as part of another partition. The design file for the top-level may be just a wrapper for the hierarchical entities below it, or it may contain its own logic. In this example, the partition for top-level entity A also includes the logic in one of its lower-level entities, C. Because entity F is contained in its own partition, it is not treated as part of the top-level partition. Another separate partition, B, contains the logic in entities B, D, and E.

Figure 7–3. Partitions in a Hierarchical Design



Partitions for Preserving Hierarchical Boundaries

Use partitions if you need to preserve hierarchical boundaries through the synthesis process. For example, if you are performing formal verification, you must use partitions to ensure that no optimizations occur across specific design hierarchies.

Follow the steps described in the next section, "Preparing a Design for Incremental Synthesis" on page 7–15, if you need to set up your design to preserve hierarchical boundaries during Quartus II synthesis. If desired, you can use partitions with full incremental compilation (instead of incremental synthesis only) to preserve boundaries throughout the entire compilation process.

Beginning with the Quartus II software version 6.0, Altera recommends using Design Partition assignments instead of the Preserve Hierarchical Boundary logic option, which may be removed in future versions of the Quartus II software.

Preparing a Design for Incremental Synthesis

To set up your design with partitions for incremental synthesis, identify the design partitions and turn on incremental synthesis using the following steps:

1. On the Processing menu, point to Start and click **Start Analysis & Elaboration** to elaborate the design, or perform any compilation flow that includes this step. This allows the Quartus II software to identify your design's hierarchy.

2. Identify the partitions in your design by applying the `PARTITION_HIERARCHY` assignment to the appropriate instances. You can do this using the list of instances under **Compilation Hierarchy** in the **Project Navigator**. Right-click on an instance in the **Project Navigator** and click **Set as Design Partition**.

   An incremental compilation icon appears next to each instance that is set as a partition.

3. On Assignments menu, click **Settings**. The **Settings** dialog box appears.

4. On the **Compilation Process Settings** page of the **Settings** dialog box, select **Incremental synthesis only** in the **Incremental compilation** section.

   When you specify your first partition, a dialog box appears asking whether you wish to enable incremental compilation. Click **Incremental synthesis only** to turn on incremental synthesis.

To remove an existing `PARTITION_HIERARCHY` assignment with the GUI, right-click the instance in the **Project Navigator** and select **Set as Design Partition** to turn off the option.

Synthesizing a Design Using Incremental Synthesis

Once incremental synthesis is enabled, it becomes the default compilation procedure under normal circumstances, that is, when you click **Start Compilation** from the Processing menu, or when you select **Start Compilation** in the toolbar.

During compilation, the software synthesizes each partition separately, and then merges the partitions to create a flattened netlist for further stages of the Quartus II compilation flow, including fitting.

For subsequent iterations of analysis and synthesis, the Quartus II software uses an internal checksum calculation to determine whether the file should be resynthesized. The software checks the contents of the source file, as well as the values of the synthesis and netlist optimization settings.

When you are using the full incremental compilation flow, changes in settings do not trigger automatic resynthesis of the design when you specify that you want to use an existing netlist. For more information about the differences between full incremental compilation and incremental synthesis, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

The Quartus II software resynthesizes only those partitions that contain changed source code, or changes to synthesis or netlist optimization settings. If you modify a file in the top-level partition, but none of the lower-level partitions are affected, the Quartus II software only resynthesizes the top-level partition.

The software always maintains the synthesis results for unchanged partitions, and merges newly synthesized partitions with unchanged partitions.

Synthesizing Using the Synthesis & Merge Commands

If you compile your design using the individual compilation steps available from the Start submenu of the Processing menu or by selecting **Compilation Tool** from the Tools menu, use the separate synthesis and merge commands.

Once incremental synthesis is enabled, on the Processing menu, point to **Start** and click **Start Analysis & Synthesis** to separately synthesize each partition. You must then merge the partitions to create a flattened netlist for further stages of the Quartus II compilation flow, including fitting. On the Processing menu, point to **Start** and click **Start Partition Merge**. After each incremental iteration of analysis and synthesis, merge the newly synthesized partitions with the unchanged partitions.

Forcing Complete Resynthesis

Because the incremental synthesis flow identifies changes to source code and assignments and resynthesizes only the partitions that have changed, you usually do not have to completely resynthesize all of your source files.

If you want to force complete resynthesis, from the **Incremental compilation** section of the **Compilation Process** page of the **Settings** dialog box, select **Off**. Then resynthesize your entire design, and turn on **Incremental synthesis only** again (if desired). Alternately, to save the extra synthesis run, you can make a small change and save at least one file in each design partition, so that the Quartus II software detects the changes and resynthesizes each partition on the next analysis and synthesis.

Considerations & Restrictions When Using Incremental Synthesis

To use incremental synthesis effectively, there are some issues to consider when planning your design's structure. Additionally, there are restrictions when using incremental synthesis with other Quartus II features. This section provides information about the following considerations and restrictions:

- Hierarchical considerations
- Restrictions on megafunction partitions
- Resource balancing
- Back-annotating node locations using the Altera LogicLock™ design methodology
- SignalTap® II logic analyzer

Hierarchical Considerations

When planning a design, keep in mind the size and scope of each partition, and how likely it is that different parts of your design will change as your design develops.

For guidelines about design hierarchical partitioning, refer to the *Hierarchical Design Partitioning* section of the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Observe the following important hierarchical design considerations:

- Register all inputs and outputs of each block. This helps avoid any delay penalty on signals that cross partition boundaries.

While this can be difficult in practice, greater adherence to this principle results in less timing degradation and area increase when using incremental flows. Registering lessens the need for the cross-partition optimizations that are prevented by partitioning.

- Do not use tri-state signals or bidirectional ports on hierarchical boundaries unless they are directly connected to top-level pins. If you use boundary tri-states in a lower-level block, synthesis pushes the tri-states through the hierarchy to the top-level to take advantage of the tri-state drivers on the output pins of the device. Because this requires optimizing through hierarchies, lower-level boundary tri-state signals are restricted with a block-level or incremental design methodology.

  Using incremental synthesis, internal tri-states are supported only when all the destination logic is contained in the same partition, in which case analysis and synthesis implements the internal tri-state signals using multiplexing logic. For bidirectional ports that feed a bidirectional pin at the top level, all the logic that forms the bidirectional I/O cell must reside in the same partition.

- Remember that logic is not synthesized, or optimized, across partition boundaries, which means any constant value (e.g., signals set to GND) will not be propagated across partitions.

Restrictions on Megafunction Partitions

The Quartus II software does not support partitions for megafunction instantiations. If you use the MegaWizard® Plug-In Manager to customize a megafunction variation, the MegaWizard-generated wrapper file instantiates the megafunction. You can create a partition for the MegaWizard-generated megafunction custom variation wrapper file.

The Quartus II software does not support the creation of a partition for inferred megafunctions (that is, in which the software uses a megafunction to implement logic in your design). If you have a module or entity for the logic that is inferred, you can create a partition for that hierarchy level in the design.

The Quartus II software does not support creation of a partition for any Quartus II internal hierarchy that is dynamically-generated during compilation to implement the contents of a megafunction.

Resource Balancing

You may have to do some manual resource balancing across partitions. When using incremental synthesis, each partition is synthesized separately, with no data about the resources used in other partitions. This means device resources could be overused in the individual partitions during synthesis, and thus the design may not fit in the target device when the partitions are merged.

For example, in the regular synthesis flow, when DSP blocks or RAM blocks are overused, the Quartus II Compiler can perform resource balancing and convert some of the logic into regular logic cells, for example, LEs or adaptive logic modules (ALMs). Without data about resources used in other partitions, it is possible for the logic in each separate partition to maximize the use of a particular device resource such that the design does not fit once all the partitions are merged. In this case, you may be able to manually balance the resources by using the Quartus II synthesis options to control inference of megafunctions that use the DSP or RAM blocks.

Refer to "Megafunction Inference Control" on page 7–40 for more information about resource balancing. You can also use the MegaWizard Plug-In Manager to customize your RAM or DSP megafunctions to use regular logic instead of the dedicated hardware blocks.

For more tips on resource balancing and reducing resource utilization, refer to the appropriate section of the *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Preserving Compilation Results

Altera recommends using full incremental compilation for top-down and bottom-up compilation flows where you wish to preserve placement and routing information and the performance of unchanged parts of your design. The full incremental compilation feature also allows you to export and import lower-level design files to enable team-based design flows or design flows where you need to optimize different blocks separately.

For more information about preserving results and exporting or importing design blocks using full incremental compilation, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

OpenCore Plus MegaCore Functions

The circuitry involved in providing OpenCore® Plus MegaCore® functions is currently incompatible with incremental synthesis and full incremental compilation.

Quartus II Synthesis Options

The Quartus II software offers a number of options to help you control the synthesis process and achieve the optimal results for your design. The "Setting Synthesis Options" on page 7–21 section describes the synthesis settings dialog box where you can set the most common global settings and options, and defines three types of synthesis options: Quartus II logic options, synthesis attributes, and synthesis directives. The other subsections describe the following common synthesis options in the Quartus II software, and provide HDL examples of how to use each option where applicable:

- Specifying Verilog & VHDL Versions for Each Design File
- Optimization Technique
- Speed Optimization Technique for Clock Domains
- PowerPlay Power Optimization
- State Machine Processing
- Manually Specifying State Assignments Using the syn_encoding Attribute
- Manually Specifying Enumerated Types Using the enum_encoding Attribute
- Preserve Hierarchical Boundary
- Restructure Multiplexers
- Power-Up Level
- Power-Up Don't Care
- Remove Duplicate Logic
- Remove Duplicate Registers
- Remove Redundant Logic Cells
- Preserve Registers
- Noprune Synthesis Attribute/Preserve Fanout Free Node
- Keep Combinational Node/Implement as Output of Logic Cell
- Maximum Fan-Out
- Megafunction Inference Control
- RAM Style & ROM Style—for Inferred Memory
- RAM Initialization File—for Inferred Memory
- Multiplier Style—for Inferred Multipliers
- Full Case
- Parallel Case
- Translate Off & On
- Ignore Translate Off
- Read Comments as HDL

For information about using other Quartus II synthesis attributes to make pin-related assignments and set other entity options (available only as logic options) in your Verilog HDL or VHDL code, refer to "Setting Other Quartus II Options in Your HDL Source Code" on page 7–52.

Setting Synthesis Options

You can set synthesis options in the **Settings** dialog box, or with logic options in the Quartus II software, or you can use synthesis attributes and directives within the HDL source code.

Analysis & Synthesis Page of the Settings Dialog Box

On the Assignments menu, click **Settings** to open the **Settings** dialog box. The **Analysis & Synthesis Settings** page allows you to set global synthesis options that apply to the entire project. These options are described in later subsections.

Quartus II Logic Options

Quartus II logic options control many aspects of the synthesis and place-and-route process. To set logic options in the Quartus II graphical user interface, on the Tools menu, click **Assignment Editor**. You can also use a corresponding Tcl command. Quartus II logic options allow you to set instance or node-specific assignments without editing the source HDL code. Logic options can be used with all design entry languages supported by the Quartus II software.

Synthesis Attributes

The Quartus II software supports synthesis attributes for Verilog HDL and VHDL, also commonly called pragmas. These attributes are not standard Verilog HDL or VHDL commands. They are used only by synthesis tools to control the synthesis process in a particular manner. Attributes always apply to a specific design element, and are applied in the HDL source code. Some synthesis attributes are also available as Quartus II logic options via the Quartus II user interface or with Tcl. Each attribute description in this chapter indicates whether there is a corresponding setting or logic option that can be set in the user interface; some attributes can be specified only with HDL synthesis attributes. Attributes specified in your HDL code are not visible in the user interface or in the Quartus II Settings File. Assignments or settings made through the Quartus II user interface, the Quartus II Settings File, or the Tcl interface take precedence over assignments or settings made with synthesis attributes in your HDL code.

The Verilog-2001, SystemVerilog, and VHDL language definitions provide specific syntax for specifying attributes. However in Verilog-1995 HDL, you must embed attribute assignments in comments. You can enter attributes in your code using the syntax in Examples 7–6, 7–7, and 7–8, where <*attribute*>, <*attribute type*>, <*value*>, <*object*>, and <*object type*> are variables, and the entry in brackets is optional. The examples in this chapter demonstrate each syntax form.

Verilog HDL is case-sensitive, therefore, synthesis attributes are also case sensitive.

Example 7–6. Synthesis Attributes in Verilog-1995 HDL

```
// synthesis <attribute> [ = <value> ]
                    or
/* synthesis <attribute> [ = <value> ] */
```

Verilog-1995 comment-embedded attributes as shown in Example 7–6 must be used as a suffix to (that is, placed after) the declaration of an item and must appear before the semicolon when one is required.

You cannot use the open one-line comment in Verilog HDL when a semicolon is required at the end of the line because it is not clear to which HDL element the attribute applies. For example, you cannot make an attribute assignment such as `reg r; // synthesis` <*attribute*> because the attribute could be read as part of the next line.

To apply multiple attributes to the same instance, separate the attributes with spaces, as follows:

`//synthesis` <*attribute1*> [= <*value*>] <*attribute2*> [= <*value*>]

For example, to set the `maxfan` attribute to `16` (Refer to "Maximum Fan-Out" on page 7–39 for details) and set the `preserve` attribute (Refer to "Preserve Registers" on page 7–36 for details) on a register called `my_reg`, use the following syntax:

```
reg my_reg /* synthesis maxfan = 16 preserve */;
```

In addition to the `synthesis` keyword as shown above, the keywords `pragma`, `synopsys`, and `exemplar` are supported for compatibility with other synthesis tools. The keyword `altera` is also supported, which allows you to add synthesis attributes that will be recognized only by Quartus II integrated synthesis and not by other tools that recognize the same synthesis attribute.

Because formal verification tools do not recognize the `exemplar`, `pragma`, and `altera` keywords, avoid using these attribute keywords when using formal verification.

Example 7–7. Synthesis Attributes in Verilog-2001 & SystemVerilog

```
(* <attribute> [ = <value> ] *)
```

Verilog-2001 attributes as shown in Example 7–7 must be used as a prefix to (that is, placed before) a declaration, module item, statement, or port connection, and used as a suffix to (that is, placed after) an operator or a Verilog HDL function name in an expression.

Because formal verification tools do not recognize the syntax, the Verilog-2001 attribute syntax is not supported when using formal verification.

To apply multiple attributes to the same instance, separate the attributes with commas, as shown in the following example:

(* *<attribute1>* [= *<value1>*], *<attribute2>* [= *<value2>*] *)

For example, to set the `maxfan` attribute to `16` (Refer to"Maximum Fan-Out" on page 7–39 for details) and set the `preserve` attribute (Refer to "Preserve Registers" on page 7–36 for details) on a register called `my_reg`, use the following syntax:

```
(* preserve, maxfan = 16 *) reg my_reg;
```

Example 7–8. Synthesis Attributes in VHDL

```
attribute <attribute> : <attribute type> ;
attribute <attribute> of <object> : <object type> is <value>;
```

VHDL attributes, as shown in Example 7–8, declare the attribute type and then apply it to a specific object. For VHDL designs, all supported synthesis attributes are declared in the `altera_syn_attributes` package in the Altera library. You can call this library from your VHDL code to declare the synthesis attributes, as follows:

```
LIBRARY altera;
USE altera.altera_syn_attributes.all;
```

Synthesis Directives

The Quartus II software supports synthesis directives, also commonly called compiler directives or pragmas. You can include synthesis directives in Verilog HDL or VHDL code as comments. These directives are not standard Verilog HDL or VHDL commands; however, synthesis tools use them to control the synthesis process in a particular manner. Other tools such as simulators ignore these directives and treat them as comments.

You can enter synthesis directives in your code using the following syntax shown in Examples 7–9 and 7–10, where <*directive*> and <*value*> are variables, and the entry in brackets is optional. The examples in this chapter demonstrate each syntax form.

Verilog HDL is case-sensitive, therefore, all synthesis directives are also case sensitive.

Example 7–9. Synthesis Directives in Verilog HDL

```
// synthesis <directive> [ =<value> ]
                    or
/* synthesis <directive> [ =<value> ] */
```

Example 7–10. Synthesis Directives in VHDL

```
-- synthesis <directive> [ =<value> ]
```

In addition to the `synthesis` keyword shown above, the `pragma`, `synopsys`, and `exemplar` keywords are supported in both Verilog HDL and VHDL for compatibility with other synthesis tools. The keyword `altera` is also supported, which allows you to add synthesis directives that will be recognized only by Quartus II integrated synthesis and not by other tools that recognize the same synthesis directive.

Because formal verification tools ignore keywords `exemplar`, `pragma`, and `altera`, avoid using these directive keywords when you are using formal verification to prevent mismatches with the Quartus II results.

Specifying Verilog & VHDL Versions for Each Design File

Your design may require you to override the default Verilog HDL or VHDL input versions (specified in the **Settings** dialog box) for some design files. This situation can occur when you want to take advantage of the features in a newer standard. If your Quartus II project contains older

design files that declare objects with these new keywords, you must use the VERILOG_INPUT_VERSION or VHDL_INPUT_VERSION synthesis directive in these files to override the default language version.

To control the language version used to process a specific file, use the following synthesis directives.

Example 7–11. Verilog HDL Design Files

```
// synthesis VERILOG_INPUT_VERSION <language version>
```

The variable <*language version*> takes one of the following values:

- VERILOG_1995
- VERILOG_2001
- SYSTEMVERILOG_2005

Example 7–12. VHDL Design Files

```
--synthesis VHDL_INPUT_VERSION <language version>
```

The variable <*language version*> takes one of the following values:

- VHDL87
- VHDL93

When the software reads a VERILOG_INPUT_VERSION or VHDL_INPUT_VERSION synthesis directive, it changes the current language version as specified until the end of the file, or until it reaches the next VERILOG_INPUT_VERSION or VHDL_INPUT_VERSION directive.

You cannot change the language version in the middle of a Verilog module or VHDL design unit.

Optimization Technique

The **Optimization Technique** logic option specifies the goal for logic optimization during compilation, that is, whether to attempt to achieve maximum speed performance or minimum area usage, or a balance between the two. Table 7–1 lists the settings for this logic option, which you can apply only to a design entity. You can also set this logic option for your whole project on the **Analysis & Synthesis Settings** page in the **Settings** dialog box.

Table 7–1. Optimization Technique Settings

Setting	Description
Area	The Compiler makes the design as small as possible to minimize resource usage
Speed	The Compiler chooses a design implementation that has the fastest f_{MAX}
Balanced *(1)*	The Compiler maps part of the design for area and part for speed, providing better area utilization than optimizing for speed, with only a slightly slower f_{MAX} than optimizing for speed

Note to Table 7–1:
(1) Balanced optimization technique is not supported for all device families.

The default setting varies by device family, and is generally optimized for the best area/speed trade-off. Results are design-dependent and vary depending on which device family you use.

Speed Optimization Technique for Clock Domains

The **Speed Optimization Technique for Clock Domains** logic option specifies that all combinational logic in or between the specified clock domain(s) is optimized for speed.

When this option is set on a particular clock signal, all the logic in this clock domain is optimized for speed during synthesis. The remainder of the design in other clock domains is synthesized with the project-wide **Optimization Technique** that is set in the **Analysis & Synthesis Settings**. The option can also be set from one clock to another clock signal, in which case the logic in paths from registers the first clock domain to registers in the second clock domain are synthesized for speed. The advantage of using this option over the project-wide setting to optimize for speed is that there is less penalty to the area of the design, because a smaller part of the circuit is optimized for speed. This may also have a positive effect on the clock speed. This option also has an advantage over setting the **Optimization Technique** on a design entity, because that option forces the hierarchical blocks to be synthesized separately. Doing so may increase area and decrease performance due to the lack of optimizations across hierarchies. The **Speed Optimization Technique for Clock**

Domains option does not treat hierarchical entities separately, and can optimize across hierarchical boundaries for logic within the same clock domain.

This option is useful if you have one or more clock domains that do not meet your timing requirements. When there are failing paths within a clock domain, the option can be set on the clock of that clock domain. When there are failing paths between clock domains, the option can be set from one clock domain to the other one.

This option is available for the following device families:

- Stratix® II
- Stratix II GX
- Stratix
- Stratix GX
- Cyclone™ II
- Cyclone
- HardCopy® II
- HardCopy Stratix
- MAX® II

PowerPlay Power Optimization

This logic option controls the power-driven compilation setting of Analysis & Synthesis and determines how aggressively Analysis & Synthesis optimizes the design for power. On the Assignments menu, click **Settings**, under **Category**, click **Analysis & Synthesis Settings**, this displays the **Analysis & Synthesis Settings** page. The following three settings are available for the PowerPlay power optimization option:

- **Off**—Analysis & Synthesis does not perform any power optimizations.
- **Normal Compilation**—Analysis & Synthesis performs power optimizations, without reducing design performance.
- **Extra Effort**—Analysis & Synthesis performs additional power optimizations which may reduce design performance.

State Machine Processing

This logic option specifies the processing style used to compile a state machine. Table 7–2 lists the settings for this logic option, which you can apply to a state machine name or to a design entity containing a state machine. You can also set this option for your whole project on the **Analysis & Synthesis Settings** page in the **Settings** dialog box.

Table 7–2. State Machine Processing Settings

Setting	Description
Auto (Default)	Allows the Compiler to choose what it determines to be the best encoding for the state machine
Minimal Bits	Uses the least number of bits to encode the state machine
One-Hot	Encodes the state machine in the one-hot style
User-Encoded	Encodes the state machine in the manner specified by the user

The default state machine encoding, which is Auto, uses one-hot encoding for FPGA devices and minimal-bits encoding for CPLDs. These settings achieve the best results on average, but another encoding style might be more appropriate for your design, so this option allows you to control the state machine encoding.

Refer to the *Recommended HDL Coding Styles* chapter in the *Quartus II Handbook* for guidelines to ensure that your state machine is inferred and encoded correctly.

If the State Machine Processing logic option is set to **User-Encoded** in a Verilog HDL design, then the software uses the original design values for the state constants. For example, a Verilog HDL design can contain a declaration such as the following:

```
parameter S0 = 4'b1010, S1 = 4'b0101, ...
```

If the software infers states `S0, S1,...` it uses the encoding `4'b1010, 4'b0101,...`

To assign your own state encoding with the **User-Encoded State Machine Processing option** in a VHDL design, you must apply specific binary encoding to the elements of an enumerated type because enumeration literals have no numeric values in VHDL. Use the `syn_encoding` synthesis attribute to apply your encoding values. Refer to "Manually Specifying State Assignments Using the syn_encoding Attribute" on page 7–29.

Manually Specifying State Assignments Using the syn_encoding Attribute

The Quartus II software infers state machines from enumerated types and automatically assigns state encoding based on "State Machine Processing" on page 7–28. However, in standard VHDL code, you cannot specify user encoding in the state machine description because enumeration literals have no numeric values in VHDL.

To assign your own state encoding for the **User-Encoded State Machine Processing** setting, you must use the `syn_encoding` synthesis attribute to apply specific binary encodings to the elements of an enumerated type.

In Example 7–13, the `syn_encoding` attribute associates a binary encoding with the states in the enumerated type `count_state`. In this example, the states are encoded with the following values: zero = "11", one = "01", two = "10", three = "00".

Example 7–13. Example of the syn_encoding VHDL Attribute

```
ARCHITECTURE rtl OF my_fsm IS
TYPE count_state is (zero, one, two, three);
ATTRIBUTE syn_encoding : STRING;
ATTRIBUTE syn_encoding OF count_state : TYPE IS "11 01 10 00";
SIGNAL present_state, next_state : count_state;
BEGIN
```

Manually Specifying Enumerated Types Using the enum_encoding Attribute

By default, the Quartus II software one-hot encodes all user-defined Enumerated Types. With the `enum_encoding` attribute, you can specify the logic encoding for an Enumerated Type and override the default `one-hot` encoding to improve the logic efficiency.

If an Enumerated Type represents the states of a state machine, using the `enum_encoding` attribute to specify a manual state encoding prevents the Compiler from recognizing state machines based on the Enumerated Type. Instead, the Compiler processes these state machines as "regular" logic using the encoding specified by the attribute, and they are not listed as state machines in the Report window for the project. If you wish to control the encoding for a recognized state machine, use the State Machine Processing logic option and the `syn_encoding synthesis` attribute.

To use the enum_encoding attribute in a VHDL design file, associate the attribute with the Enumeration Type whose encoding you want to control. The enum_encoding attribute must follow the Enumeration Type Definition but precede its use. In addition, the attribute value must be a string literal that specifies either an arbitrary user encoding or an encoding style of "default", "sequential", "gray", or "one-hot".

An arbitrary user encoding consists of a space-delimited list of encodings. The list must contain as many encodings as there are enumeration literals in your Enumeration Type. In addition, the encodings must all have the same length, and each encoding must consist solely of values from the std_ulogic type declared by the std_logic_1164 package in the IEEE library. In the code fragment of Example 7–14, the enum_encoding attribute specifies an arbitrary user encoding for the Enumeration Type fruit.

Example 7–14. Specifying an Arbitrary User Encoding for Enumerated Type

```
type fruit is (apple, orange, pear, mango);
attribute enum_encoding : string;
attribute enum_encoding of fruit : type is "11 01 10 00";
```

In this example, the enumeration literals are encoded as:

```
apple   = "11"
orange  = "01"
pear    = "10"
mango   = "00"
```

Sometimes you may wish to specify an encoding style, rather than a manual user encoding, especially when the Enumeration Type has a large number of enumeration literals. The Quartus II software can implement Enumeration Types with four different encoding styles:

- "default"—Use an encoding based on the number of enumeration literals in the Enumeration Type. If there are fewer than 5 literals, use the "sequential" encoding. If there are more than five but fewer than 50 literals, use a "one-hot" encoding. Otherwise, use a "gray" encoding.
- "sequential"—Use a binary encoding in which the first enumeration literal in the Enumeration Type has encoding 0, the second 1, and so on.
- "gray"—Use an encoding in which the encodings for adjacent enumeration literals differ by exactly one bit.
- "one-hot"—The default encoding style requiring *N* bits, where *N* is the number of enumeration literals in the Enumeration Type.

Observe that in Example 7–14, the `enum_encoding` attribute manually specified a gray encoding for the Enumeration Type `fruit`. This example could be written more concisely by specifying the `"gray"` encoding style instead of a manual encoding, as shown in Example 7–15.

Example 7–15. Specifying the "gray" Encoding Style or Enumeration Type

```
type fruit is (apple, orange, pear, mango);
attribute enum_encoding : string;
attribute enum_encoding of fruit : type is "gray";
```

Preserve Hierarchical Boundary

This logic option allows you to preserve the hierarchical boundaries between design entities. Beginning with the Quartus II software version 6.0, Altera recommends using design partitions with incremental synthesis or full incremental compilation instead of using the **Preserve Hierarchical Boundary** logic option.

The **Preserve Hierarchical Boundary** logic option may be removed in future versions of the Quartus II software.

Refer to "Partitions for Preserving Hierarchical Boundaries" on page 7–14 for details about using design partitions.

Restructure Multiplexers

This option specifies whether the Quartus II software should extract and optimize buses of multiplexers during synthesis.

This option is useful if your design contains buses of fragmented multiplexers. This option restructures multiplexers more efficiently for area, allowing the design to implement multiplexers with a reduced number of LEs or ALMs. This option is available for Stratix II, Stratix, Stratix GX, Cyclone II, Cyclone, and MAX II devices.

The **Restructure Multiplexers** option works on entire trees of multiplexers. Multiplexers may arise in different parts of the design through Verilog HDL or VHDL constructs such as the "`if`," "`case`," or "`?:`" statements. When multiplexers from one part of the design feed multiplexers in another part of the design, trees of multiplexers are formed. Multiplexer buses occur most often as a result of multiplexing together vectors in Verilog HDL, or `STD_LOGIC_VECTOR` signals in VHDL. The **Restructure Multiplexers** option identifies buses of multiplexer trees that have a similar structure. When it is turned on, the

Restructure Multiplexers option optimizes the structure of each multiplexer bus for the target device to reduce the overall amount of logic used in the design.

Results of the multiplexer optimizations are design dependent, but area reductions as high as 20% are possible. The option may negatively affect your design's f_{MAX}.

Table 7–3 lists the settings for the logic option, which you can apply only to a design entity. You can also specify this option on the **Analysis & Synthesis Settings** page in the **Settings** dialog box for your whole project.

Table 7–3. Restructure Multiplexers Settings

Setting	Description
On	Enables multiplexer restructuring to minimize your design area. This setting may reduce the f_{MAX}.
Off	Disables multiplexer restructuring to avoid possible reductions in f_{MAX}.
Auto (Default)	Allows the Compiler to determine whether to enable the option based on your other Quartus II synthesis settings. The option is On when the **Optimization Technique** option is set to **Area** or **Balanced**, and Off when the **Optimization Technique** option is **Speed**. (Note that since the default Optimization Technique is Balanced for many device families including Stratix and Stratix II devices, this option is turned on by default for those families.)

After you have compiled your design, you can view multiplexer restructuring information in the **Multiplexer Restructuring Statistics** report in the **Multiplexer Statistics** folder under **Analysis & Synthesis Optimization Results** in the **Analysis & Synthesis** section of the **Compilation Report**. Table 7–4 describes the information that is listed in the **Multiplexer Restructuring Statistics** report table for each bus of multiplexers.

Table 7–4. Multiplexer Information in the Multiplexer Restructuring Statistics Report (Part 1 of 2)

Heading	Description
Multiplexer Inputs	The number of different choices that are multiplexed together.
Bus Width	The width of the bus in bits.
Baseline Area	An estimate of how many logic cells are needed to implement the bus of multiplexers (before any multiplexer restructuring takes place). This estimate can be used to identify any large multiplexers in the design.
Area if Restructured	An estimate of how many logic cells are needed to implement the bus of multiplexers if **Multiplexer Restructuring** is applied.

Table 7–4. Multiplexer Information in the Multiplexer Restructuring Statistics Report (Part 2 of 2)

Heading	Description
Saving if Restructured	An estimate of how many logic cells are saved if **Multiplexer Restructuring** is applied.
Registered	An indication of whether registers are present on the multiplexer outputs. **Multiplexer Restructuring** uses the secondary control signals of a register (such as synchronous clear and synchronous-load) to further reduce the amount of logic needed to implement the bus of multiplexers.
Example Multiplexer Output	The name of one of the multiplexers' outputs. This name can help determine where in the design the multiplexer bus originated.

For more information about optimizing for multiplexers, refer to the *Multiplexers* section of the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Power-Up Level

This logic option causes a register (flip-flop) to power up with the specified logic level, either **High** (1) or **Low** (0). Registers in the device core hardware power up to 0 in all Altera devices. For the register to power up with a logic level **High** specified using this option, the Compiler performs an optimization referred to as NOT-gate push back on the register. NOT-gate push back adds an inverter to the input and the output of the register so that the reset and power-up conditions will appear to be high and the device operates as expected. The register itself actually still powers up low, but the register output is inverted so the signal arriving at all destinations is high.

This option supports wildcard characters, and you can apply this option to any register or to a pin with the logic configurations described in the following list:

- If this option is turned on for an input pin, the option is transferred automatically to the register that is driven by the pin if the following conditions are present:
  - There is no logic, other than inversion, between the pin and the register
  - The input pin drives the data input of the register
  - The input pin does not fan out to any other logic

- If this option is turned on for an output or bidirectional pin, it is transferred automatically to the register that feeds the pin, if the following conditions are present:
  - There is no logic, other than inversion, between the register and the pin
  - The register does not fan out to any other logic

For VHDL, Quartus II integrated synthesis also reads default values for registered signals defined in the VHDL code and converts the default values into Power-Up Level settings. That way, the synthesized behavior matches the power-up state of the VHDL code during a functional simulation. The Quartus II software, like most synthesis tools, does not synthesize variables that are assigned values in Verilog HDL initial blocks into power-up conditions. Initial blocks are generally not synthesized.

For more information about `NOT` gate push-back, the power-up states for Altera devices, and how power-up level is affected by set and reset control signals, refer to *Recommended HDL Coding Styles* in volume 1 of the *Quartus II Handbook*.

Power-Up Don't Care

This logic option causes registers to power up with the logic level most appropriate for the design. This option allows the Compiler to change the power-up condition of a register to, for example, minimize your design's area usage. This option is turned on by default.

For example, a register may have its `D` input tied to `VCC`. If you turn this option off, the register powers up low even though it goes high at the first clock signal. If you turn this option on, the Compiler sets the power-up value of the register to high and, therefore, can eliminate the register and connect the output of the register to `VCC`. If the Compiler performs this type of optimization, it issues a message indicating it is doing so.

This project-wide option does not apply to registers that have the **Power-Up Level** logic option set to either **High** or **Low**.

Remove Duplicate Logic

If you turn on this logic option, the Compiler removes logic that is identical to other logic in the design. If two functions generate the same logic, the Compiler removes the second one, and the first one fans out to the second one's destinations. Additionally, if the deleted logic function has different logic option assignments, the Compiler ignores them. This option is turned on by default.

When turned on, this option also removes all duplicate registers in the same way as does the **Remove Duplicate Registers** option. If you do not want the Compiler to remove certain registers when this option is turned on, turn off the **Remove Duplicate Registers** option for those registers. For more details, refer to Table 7–5.

Even if you turn this option on, the Compiler does not remove duplicate logic that you inserted deliberately. If a function's output feeds an LCELL buffer, the Compiler always treats it as a unique signal and the **Remove Duplicate Logic** option does not apply (that is, the Compiler does not remove an LCELL buffer if you turn on this option).

Remove Duplicate Registers

If you turn on this logic option, the Compiler removes registers that are identical to another register. If two registers generate the same logic, the Compiler removes the second one, and the first one fans out to the second one's destinations. Also, if the deleted register has different logic option assignments, the Compiler ignores them. This option is turned on by default.

The Compiler recognizes this option only if you turned on the **Remove Duplicate Logic** option. When turned on, the **Remove Duplicate Logic** option also removes duplicate registers. Therefore, you should use this option only if you want to prevent the Compiler from removing duplicate registers that you have used deliberately. That is, you should use this option only with the **Off** setting. Refer to Table 7–5. You can apply this option to an individual register or a design entity that contains registers.

Table 7–5. Settings for Remove Duplicate Logic & Remove Duplicate Registers

Remove Duplicate Logic Setting	Remove Duplicate Registers Setting	Description
On (Default)	On (Default)	Removes logic (including registers) if it is identical to other logic in the design.
On	Off	Preserves all registers for which the **Remove Duplicate Registers** option is turned off. Removes logic (including any other registers) if it is identical to other logic in the design.
Off	On or Off	Preserves duplicate logic and registers.

Remove Redundant Logic Cells

This logic option removes redundant LCELL primitives or WYSIWYG cells. If you turn on this option, the Compiler optimizes a circuit for area and speed. The project-wide option is turned off by default.

Preserve Registers

This attribute and logic option direct the Compiler not to minimize or remove a specified register during synthesis optimizations or register netlist optimizations.Optimizations can eliminate redundant registers and registers with constant drivers; this option prevents a register from being reduced to a constant or merged with a duplicate register. This option can preserve a register so you can observe it during simulation or with the SignalTap II logic analyzer. Additionally, it can preserve registers if you are creating a preliminary version of the design in which secondary signals are not specified. You can also use the attribute to preserve a duplicate of an I/O register so that one copy can be placed in an I/O cell and the second can be placed in the core. By default, the software may remove one of the two duplicate registers in this case; the `preserve` attribute can be added to both registers to prevent this.

This option cannot preserve registers that have no fan-out. To prevent the removal of registers with no fanout, refer to "Noprune Synthesis Attribute/Preserve Fanout Free Node" on page 7–37.

The `Preserve Registers` attribute prevents a register from being inferred as a state machine.

You can set the **Preserve Registers** logic option in the Quartus II GUI or you can set the `preserve` attribute in your HDL code as shown in Example 7–16, 7–17, and 7–18. In the examples, the `my_reg` register is preserved.

In addition to `preserve`, the Quartus II software supports the `syn_preserve` attribute name for compatibility with other synthesis tools.

Example 7–16. Verilog HDL Example of a preserve Attribute

```
reg my_reg /* synthesis preserve = 1 */;
```

Example 7–17. Verilog-2001 Example of a syn_preserve Attribute

```
(* syn_preserve = 1 *) reg my_reg;
```

The `" = 1"` after the `"preserve"` in Example 7–16 and Example 7–17 is optional, because the assignment uses a default value of `1` when it is specified.

Example 7–18. VHDL Example of a preserve Attribute

```
signal my_reg : stdlogic;
attribute preserve : boolean;
attribute preserve of my_reg : signal is true;
```

Noprune Synthesis Attribute/Preserve Fanout Free Node

This synthesis attribute and corresponding logic option direct the Compiler to preserve a fanout free register through the entire compilation flow. This is different from the Preserve Registers option, which prevents a register from being reduced to a constant or merged with a duplicate register. Standard synthesis optimizations remove nodes that do not directly or indirectly feed a top-level output pin. This option can retain a register so you can observe it in the Simulator or the SignalTap II logic analyzer. Additionally, it can retain registers if you are creating a preliminary version of the design in which the registers' fanout logic is not specified.

You can set the **Preserve Fanout Free Node logic** option in the Quartus II GUI, or you can set the `noprune` attribute in your HDL code as shown in Example 7–19, Example 7–20, and Example 7–21. In these examples, the `my_reg` register is preserved.

You must use the `noprune` attribute instead of the logic option if the register has no immediate fanout in its module or entity. If you do not use the synthesis attribute, registers with no fanout are removed (or "pruned") during analysis and elaboration before the logic synthesis stage applies any logic options. If the register has no fanout in the full design, but has fanout within its module or entity, then you can use the logic option to retain the register through compilation.

The attribute name `syn_noprune` is supported for compatibility with other synthesis tools.

Example 7–19. Verilog HDL Example of a noprune Attribute

```
reg my_reg /* synthesis noprune = 1 */;
```

Example 7–20. Verilog-2001 Example of a noprune Attribute

```
(* noprune = 1 *) reg my_reg;
```

Example 7–21. VHDL Example of a noprune Attribute

```
signal my_reg : stdlogic;
attribute noprune: boolean;
attribute noprune of my_reg : signal is true;
```

Keep Combinational Node/Implement as Output of Logic Cell

This synthesis attribute and corresponding logic option direct the Compiler to keep a wire or combinational node through logic synthesis minimizations and netlist optimizations. A wire that has a `keep` attribute or a node that has the **Implement as Output of Logic Cell** logic option applied becomes the output of a logic cell in the final synthesis netlist, and the name of the logic cell will be the same as the name of the wire or node. You can use this directive to make combinational nodes visible to the SignalTap II logic analyzer.

The option cannot keep nodes that have no fan-out. Node names cannot be maintained for wires with tri-state drivers, or if the signal feeds a top-level pin of the same name (in this case the node name is changed to a name such as <*net name*>`~reg0`).

You can set the **Implement as Output of Logic Cell** logic option in the Quartus II GUI, or you can set the `keep` attribute in your HDL code as shown in Example 7–22, Example 7–23, and Example 7–24. In these examples, the Compiler maintains the node name `my_wire`.

In addition to `keep`, the Quartus II software supports the `syn_keep` attribute name for compatibility with other synthesis tools.

Example 7–22. Verilog HDL Example of a keep Attribute

```
wire my_wire /* synthesis keep = 1 */;
```

Example 7–23. Verilog-2001 Example of a keep Attribute

```
(* keep = 1 *) wire my_wire;
```

Example 7–24. VHDL Example of a syn_keep Attribute

```
signal my_wire: bit;
attribute syn_keep: boolean;
attribute syn_keep of my_wire: signal is true;
```

Maximum Fan-Out

This attribute and logic option directs the Compiler to control the number of destinations fed by a node. The Compiler duplicates a node and splits its fan-out until the individual fan-out of each copy falls below the maximum fan-out restriction. You can apply this option to a register or a logic cell buffer. You can also use this option to reduce the load of critical signals, which can improve performance. You can use this option to instruct the Compiler to duplicate (or replicate) a register that feeds nodes in different locations on the target device. Duplicating the register may allow the Fitter to place these new registers closer to their destination logic, minimizing routing delay.

This option is available for all devices supported in the Quartus II software except MAX® 3000, MAX 7000, FLEX 10K®, ACEX® 1K, and Mercury™ devices. The maximum fan-out constraint is honored as long as the following conditions are met:

- The node is not part of a cascade, carry, or register cascade chain
- The node does not feed itself
- The node feeds other logic cells, DSP blocks, RAM blocks and/or pins through data, address, clock enable, etc, but not through any asynchronous control ports (such as asynchronous clear)

The software does not create duplicate nodes in these cases either because there is no clear way to duplicate the node, or, in the third condition above where asynchronous control signals are involved, to avoid the possible situation that small differences in timing could produce functional differences in the implementation. If the constraint cannot be applied because one of these conditions is not met, the Quartus II software issues a message indicating that it ignored maximum fan-out assignment.

If you have enabled any of the Quartus II netlist optimizations that affect registers, add the `preserve` attribute to any registers to which you have set a `maxfan` attribute. The `preserve` attribute ensures that the registers are not affected by any of the netlist optimization algorithms such as register retiming.

For details about netlist optimizations, refer to the *Netlist Optimization & Physical Synthesis* chapter in volume 2 of the *Quartus II Handbook*.

You can set the **Maximum Fan-Out** logic option in the Quartus II GUI, and this option supports wildcard characters. You can also set the `maxfan` attribute in your HDL code as shown in Example 7–25, 7–26, and 7–27. In these examples, the Compiler duplicates the `clk_gen` register, so its fan-out is not greater than 50.

In addition to `maxfan`, the Quartus II software supports the `syn_maxfan` attribute name for compatibility with other synthesis tools.

Example 7–25. Verilog HDL Example of a syn_maxfan Attribute

```
reg clk_gen /* synthesis syn_maxfan = 50 */;
```

Example 7–26. Verilog-2001 Example of a maxfan Attribute

```
(* maxfan = 50 *) reg clk_gen;
```

Example 7–27. VHDL Example of a maxfan Attribute

```
signal clk_gen : stdlogic;
attribute maxfan : signal ;
attribute maxfan of clk_gen : signal is 50;
```

Megafunction Inference Control

The Quartus II Compiler automatically recognizes certain types of HDL code and infers the appropriate megafunction The software uses the Altera megafunction code when compiling your design even when you do not specifically instantiate the megafunction. The software infers megafunctions to take advantage of logic that is optimized for Altera devices. The area and performance of such logic may be better than the results obtained by inferring generic logic from the same HDL code.

Additionally, you must use megafunctions to access certain architecture-specific features, such as RAM, digital signal processing (DSP) blocks, and shift registers, that generally provide improved performance compared with basic logic elements.

For details on coding style recommendations when targeting megafunctions in Altera devices, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

The Quartus II software provides options to control the inference of certain types of megafunctions, as described in the following sub-sections.

Multiply-Accumulators & Multiply-Adders

Use the **Auto DSP Block Replacement** logic option to control DSP block inference for multiply-accumulations and multiply-adders. This option is turned on by default. To disable inference, turn off this option for your

whole project on the **Analysis & Synthesis Settings** page of the **Settings** dialog box, or disable the option for a specific block with the **Assignment Editor**.

Any registers that the software maps to the `altmult_accum` and `altmult_add` megafunctions and places in DSP blocks are not available in the Simulator because their node names do not exist after synthesis.

Shift Registers

Use the **Auto Shift Register Replacement** logic option to control shift register inference. This option is turned on by default. To disable inference, turn off this option for your whole project on the **Analysis & Synthesis Settings** page of the **Settings** dialog box, or for a specific block with the **Assignment Editor**. The software may not infer small shift registers because small shift registers typically do not benefit from implementation in dedicated memory. However, you can use the **Allow Any Shift Register Size for Recognition** logic option to instruct synthesis to infer a shift register even when its size is considered too small.

The registers that the software maps to the `altshift_taps` megafunction and places in RAM are not available in the Simulator because their node names do not exist after synthesis.

The **Auto Shift Register Replacement** logic option is turned off automatically when a formal verification tool is selected in the EDA Tool Settings. The software issues a warning and lists shift registers that would have been inferred if no formal verification tool was selected in the compilation report. To allow the use of a megafunction for the shift register in the formal verification flow, you can either instantiate a shift register explicitly using the MegaWizard Plug-in Manager or black-box the shift register in a separate entity/module.

RAM & ROM

Use the **Auto RAM Replacement** and **Auto ROM Replacement** logic options to control RAM and ROM inference, respectively. These options are turned on by default. To disable inference, turn off the appropriate option for your whole project on the **Analysis & Synthesis Settings** page of the **Settings** dialog box, or disable the option for a specific block with the **Assignment Editor**.

The software may not infer very small RAM or ROM blocks because very small memory blocks can typically be implemented more efficiently by using the registers in the logic. However, you can use the **Allow Any RAM Size for Recognition** and **Allow Any ROM Size for Recognition** logic options to instruct synthesis to infer a memory block even when its size is considered too small.

The **Auto ROM Replacement** logic option is automatically turned off when a formal verification tool is selected in the **EDA Tool Settings** page. A warning is issued and a report panel lists ROMs that would have been inferred if no formal verification tool was selected. To allow the use of a megafunction for the shift register in the formal verification flow, you can either instantiate a ROM explicitly using the MegaWizard Plug-in Manager or create a black box the ROM in a separate entity/module.

Although formal verification tools do not support inferred RAM blocks, because of the importance of inferring RAM in many designs, the **Auto RAM Replacement** logic option remains on when a formal verification tool is selected in the **EDA Tool Settings** page. The Quartus II software automatically black boxes any module or entity that contains a RAM block that is inferred. The software issues a warning and lists the black box that is created in the compilation report. This block box allows formal verification tools to proceed; however, the entire module or entity containing the RAM cannot be verified in the tool. Altera recommends explicitly instantiating RAM blocks in separate modules or entities so that as much logic as possible can be verified by the formal verification tool.

RAM Style & ROM Style—for Inferred Memory

These attributes specify the implementation for an inferred RAM or ROM block. You can specify the type of TriMatrix™ embedded memory block to be used, or specify the use of standard logic cells (LEs or ALMs). The attributes are supported only for device families with TriMatrix embedded memory blocks.

The `ramstyle` and `romstyle` attributes take a single string value. The values "M512", "M4K", and "M-RAM" indicates the type of memory block to use for the inferred RAM or ROM. The value "logic" indicates that the RAM or ROM should be implement in regular logic rather than dedicated memory blocks. You can set the attribute on a module or entity, in which case it specifies the default implementation style for all inferred memory blocks in the immediate hierarchy. You can also set the attribute on a specific signal (VHDL) or variable (Verilog HDL) declaration, in which case it specifies the preferred implementation style for that specific memory, overriding the default implementation style.

If you specify a value of "logic", the memory still appears as a RAM or ROM block in the RTL Viewer, but it is converted to regular logic during a later synthesis step.

In addition to `ramstyle` and `romstyle`, the Quartus II software supports the `syn_ramstyle` attribute name for compatibility with other synthesis tools.

Example 7–28, 7–29, and 7–30 specify that all memory in the module or entity `my_memory_blocks` should be implemented using a specific type of block.

Example 7–28. Verilog-1995 Example of Applying a romstyle Attribute to a Module Declaration

```
module my_memory_blocks (...) /* synthesis romstyle = "M4K" */
```

Example 7–29. Verilog-2001 Example of Applying a ramstyle Attribute to a Module Declaration

```
 (* ramstyle = "M512" *) module my_memory_blocks (...);
```

Example 7–30. VHDL Example of Applying a romstyle Attribute to an Architecture

```
architecture rtl of my_ my_memory_blocks is
attribute romstyle : string;
attribute romstyle of rtl : architecture is "M-RAM";
begin
```

Example 7–31, 7–32, and 7–33 specify that the inferred memory `my_ram` or `my_rom` should be implemented using regular logic instead of a TriMatrix memory block.

Example 7–31. Verilog-1995 Example of Applying a syn_ramstyle Attribute to a Variable Declaration

```
reg [0:7] my_ram[0:63] /* synthesis syn_ramstyle = "logic" */;
```

Example 7–32. Verilog-2001 Example of Applying a romstyle Attribute to a Variable Declaration

```
(* romstyle = "logic" *) reg [0:7] my_rom[0:63];
```

Example 7–33. VHDL Example of Applying a ramstyle Attribute to a Variable Declaration

```
type memory_t is array (0 to 63) of std_logic_vector (0 to 7);
signal my_ram : memory_t;
attribute ramstyle : string;
attribute ramstyle of my_ram : signal is "logic";
```

RAM Initialization File—for Inferred Memory

The `ram_init_file` attribute specifies the initial contents of an inferred memory in the form of a Memory Initialization File (**.mif**). The attribute takes a string value containing the name of the RAM initialization file.

Example 7–34. Verilog-1995 Example of Applying a ram_init_file Attribute

```
reg [7:0] mem[0:255] /* synthesis ram_init_file
= " my_init_file.mif" */;
```

Example 7–35. Verilog-2001 Example of Applying a ram_init_file Attribute

```
(* ram_init_file = "my_init_file.mif" *) reg [7:0] mem[0:255];
```

Example 7–36. VHDL Example of Applying a ram_init_file Attribute

```
type mem_t is array(0 to 255) of unsigned(7 downto 0);
signal ram : mem_t;
attribute ram_init_file : string;
attribute ram_init_file of ram :
signal is "my_init_file.mif";
```

In VHDL, you can also initialize the contents of an inferred memory by specifying a default value for the corresponding signal. Quartus II integrated synthesis automatically converts the default value into a MIF for the inferred RAM.

Multiplier Style—for Inferred Multipliers

The `multstyle` attribute specifies the implementation style for multiplication operations (`*`) in your HDL source code. You can use this attribute to specify whether you prefer the Compiler to implement a multiplication operation in general logic or dedicated hardware, if available in the target device.

Specifying a `multstyle` of `"dsp"` does not guarantee that the Quartus II software can implement a multiplication in dedicated DSP hardware. The final implementation depends, among other things, on the availability of dedicated hardware in the target device, the size of the operands, and whether or not one or both operands are constant.

The `multstyle` attribute takes a string value of `"logic"` or `"dsp,"` indicating a preferred implementation in logic or in dedicated hardware, respectively. In Verilog HDL, apply the attribute to a module declaration,

a variable declaration, or a specific binary expression containing the * operator. In VHDL, apply the synthesis attribute to a signal, variable, entity, or architecture.

In addition to `multstyle`, the Quartus II software supports the `syn_multstyle` attribute name for compatibility with other synthesis tools.

When applied to a Verilog HDL module declaration, the attribute specifies the default implementation style for all instances of the * operator in the module. For example, in the following code examples, the `multstyle` attribute directs the Quartus II software to implement all multiplications inside module `my_module` in dedicated multiplication hardware.

Example 7–37. Verilog-1995 Example of Applying a multstyle Attribute to a Module Declaration

```
module my_module (...) /* synthesis multstyle = "dsp" */;
```

Example 7–38. Verilog-2001 Example of Applying a multstyle Attribute to a Module Declaration

```
(* multstyle = "dsp" *) module my_module(...);
```

When applied to a Verilog HDL variable declaration, the attribute specifies the implementation style to be used for a multiplication operator whose result is directly assigned to the variable. It overrides the `multstyle` attribute associated with the enclosing module, if present. For example, in Example 7–39 and 7–40, the `multstyle` attribute applied to variable `result` directs the Quartus II software to implement `a * b` in general logic rather than dedicated hardware.

Example 7–39. Verilog-2001 Example of Applying a multstyle Attribute to a Variable Declaration

```
wire [8:0] a, b;
(* multstyle = "logic" *) wire [17:0] result;
assign result = a * b;  //Multiplication must be
                        //directly assigned to result
```

Example 7–40. Verilog-1995 Example of Applying a multstyle Attribute to a Variable Declaration

```
wire [8:0] a, b;
wire [17:0] result /* synthesis multstyle = "logic" */;
assign result = a * b;  //Multiplication must be
                        //directly assigned to result
```

When applied directly to a binary expression containing the * operator, the attribute specifies the implementation style for that specific operator alone and overrides any multstyle attribute associated with target variable or enclosing module. For example, in Example 7–41, the multstyle attribute indicates that a * b should be implemented in dedicated hardware.

Example 7–41. Verilog-2001 Example of Applying a multstyle Attribute to a Binary Expression

```
wire [8:0] a, b;
wire [17:0] result;
assign result = a * (* multstyle = "dsp" *) b;
```

You can not use Verilog-1995 attribute syntax to apply the multstyle attribute to a binary expression.

When applied to a VHDL entity or architecture, the attribute specifies the default implementation style for all instances of the * operator in the entity or architecture. For example, in Example 7–42, the multstyle attribute directs the Quartus II software to use dedicated hardware, if possible, for all multiplications inside architecture rtl of entity my_entity.

Example 7–42. VHDL Example of Applying a multstyle Attribute to an Architecture

```
architecture rtl of my_entity is
       attribute multstyle : string;
       attribute multstyle of rtl : architecture is "dsp";
begin
```

When applied to a VHDL signal or variable, the attribute specifies the implementation style to be used for all instances of the * operator whose result is directly assigned to the signal or variable. It overrides the multstyle attribute associated with the enclosing entity or architecture, if present. For example, in Example 7–43, the multstyle attribute associated with signal result directs the Quartus II software to implement a * b in general logic rather than dedicated hardware.

Example 7–43. VHDL Example of Applying a multstyle Attribute to a Signal or Variable

```
signal a, b : unsigned(8 downto 0);
signal result : unsigned(17 downto 0);

attribute multstyle : string;
attribute multstyle of result : signal is "logic";
result <= a * b;
```

Full Case

A Verilog HDL case statement is considered full when its case items cover all possible binary values of the case expression or when a default case statement is present. A `full_case` attribute attached to a case statement header that is not full forces the unspecified states to be treated as a "don't care" value. VHDL case statements must be full, so the attribute does not apply to VHDL.

Using this attribute on a case statement that is not full avoids the latch inference problems discussed in the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Latches have limited support in formal verification tools. It is important to ensure that you do not infer latches unintentionally, e.g. through an incomplete case statement, when using formal verification. Formal verification tools do support the `full_case` synthesis attribute (with limited support for attribute syntax, as described in "Synthesis Attributes" on page 7–21).

When you are using the `full_case` attribute, there is a potential cause for a simulation mismatch between Verilog HDL functional and post-Quartus II simulation because unknown case statement cases may still function like latches during functional simulation. For example, a simulation mismatch may occur with the code in the following example when `sel` is `2'b11` because a functional HDL simulation output behaves like a latch while the Quartus II simulation output behaves like "don't care."

Altera recommends making the case statement "full" in your regular HDL code, instead of using the `full_case` attribute.

The case statement in Example 7–44 is not full because not all binary values for `sel` are specified. Because the `full_case` attribute is used, synthesis treats the output as "don't care" when the `sel` input is `2'b11`.

Example 7–44. Verilog HDL Example of a full_case Attribute

```
module full_case (a, sel, y);
    input [3:0] a;
    input [1:0] sel;
    output y;
    reg y;
    always @ (a or sel)
    case (sel) // synthesis full_case
        2'b00: y=a[0];
        2'b01: y=a[1];
        2'b10: y=a[2];
        endcase
endmodule
```

Verilog-2001 syntax also accepts the statements in Example 7–45 in the `case` header instead of the comment form shown in Example 7–44.

Example 7–45. Verilog-2001 Syntax for the full_case Attribute

```
(* full_case *) case (sel)
```

Parallel Case

The `parallel_case` attribute indicates that a Verilog HDL case statement should be considered parallel, that is, only one case item can be matched at a time. Case items in Verilog HDL case statements may overlap. To resolve multiple matching case items, the Verilog HDL language defines a priority relationship among case items in which the case statement always executes the first case item that matches the case expression value. By default, the Quartus II software implements the extra logic required to satisfy this priority relationship.

Attaching a `parallel_case` attribute to a case statement's header allows the Quartus II software to consider its case items as inherently parallel, that is, at most one case item matches the case expression value. Parallel case items reduce the complexity of the generated logic.

In VHDL, the individual choices in a case statement may not overlap, so they are always parallel and this attribute does not apply.

Use this attribute only when the `case` statement is truly parallel. If you use the attribute in any other situation, the generated logic will not match the functional simulation behavior of the Verilog HDL.

Altera recommends that you avoid using the parallel_case attribute, due to the possibility of introducing mismatches between Verilog HDL functional and post-Quartus II simulation.

If you specify the supported Verilog HDL version as SystemVerilog-2005 for your design, you can use the SystemVerilog keyword unique to achieve the same result as the parallel_case directive without causing simulation mismatches.

The following example shows a casez statement with overlapping case items. In functional HDL simulation, the three case items have a priority order that depends on the bits in sel. For example, sel[2] takes priority over sel[1] which takes priority over sel[0]. However the synthesized design may simulate differently because the parallel_case attribute eliminates this priority order. If more than one bit of sel is high, then more than one output (a, b, or c) is high as well, a situation that cannot occur in functional HDL simulation.

Example 7–46. Verilog HDL Example of a parallel_case Attribute

```
                    module parallel_case (sel, a, b, c);
   input [2:0] sel;
   output a, b, c;
   reg a, b, c;
   always @ (sel)
   begin
      {a, b, c} = 3'b0;
      casez (sel) // synthesis parallel_case
         3'b1??: a = 1'b1;
         3'b?1?: b = 1'b1;
         3'b??1: c = 1'b1;
      endcase
   end
endmodule
```

Verilog-2001 syntax also accepts the statements as shown in Example 7–47 in the case (or casez) header instead of the comment form as shown in Example 7–46.

Example 7–47. Verilog-2001 Syntax

```
(* parallel_case *) casez (sel)
```

Translate Off & On

The `translate_off` and `translate_on` synthesis directives indicate whether the Quartus II software or a third-party synthesis tool should compile a portion of HDL code that is not relevant for synthesis. The `translate_off` directive marks the beginning of code that the synthesis tool should ignore; the `translate_on` directive indicates that synthesis should resume. A common use of these directives is to indicate a portion of code that is intended for simulation only. The synthesis tool reads synthesis-specific directives and processes them during synthesis; however, third-party simulation tools read the directives as comments and ignore them. Example 7–48 and Example 7–49 show these directives.

Example 7–48. Verilog HDL Example of Translate Off & On

```
// synthesis translate_off
parameter tpd = 2;    // Delay for simulation
#tpd;
// synthesis translate_on
```

Example 7–49. VHDL Example of Translate Off & On

```
-- synthesis translate_off
use std.textio.all;
-- synthesis translate_on
```

If you wish to ignore a portion of code in Quartus II integrated synthesis only, you can use the Altera-specific attribute keyword `altera`. For example, use the `// altera translate_off` and `// altera translate_on` directives to direct Quartus II integrated synthesis to ignore a portion of code that is intended only for other synthesis tools.

Ignore Translate Off

The **Ignore Translate Off** logic option directs Quartus II integrated synthesis to ignore the `translate_off` and `translate_on` attributes described in the previous section. This allows you to compile code that was previously intended to be ignored by third-party synthesis tools, for example megafunction declarations that were treated as black boxes in other tools but can be compiled in the Quartus II software. To set the **Ignore Translate Off** logic option, click **More Settings** on the **Analysis & Synthesis Settings** page of the **Settings** dialog box.

Read Comments as HDL

The read_comments_as_HDL synthesis directive indicates that the Quartus II software should compile a portion of HDL code that is commented out. This directive allows you to comment out portions of HDL source code that are not relevant for simulation, while instructing the Quartus II software to read and synthesize that same source code. Setting the read_comments_as_HDL directive to on marks the beginning of commented code that the synthesis tool should read; setting the read_comments_as_HDL directive to off indicates the end of the code.

You can use this directive with translate_off and translate_on to create one HDL source file that includes both a megafunction instantiation for synthesis and a behavioral description for simulation.

Because formal verification tools do not recognize the read_comments_as_HDL directive, it is not supported when you are using formal verification.

In Example 7–50 and 7–51, the commented code enclosed by read_comments_as_HDL is visible to the Quartus II Compiler and is synthesized.

Because synthesis directives are case-sensitive in Verilog HDL, you must match the case of the directive, as shown below.

Example 7–50. Verilog HDL Example of Read Comments as HDL

```
// synthesis read_comments_as_HDL on
// my_rom lpm_rom (.address (address),
//                 .data    (data));
// synthesis read_comments_as_HDL off
```

Example 7–51. VHDL Example of Read Comments as HDL

```
-- synthesis read_comments_as_HDL on
-- my_rom : entity lpm_rom
--   port map (
--    address => address,
--    data    => data,      );
-- synthesis read_comments_as_HDL off
```

Setting Other Quartus II Options in Your HDL Source Code

This section describes Quartus II synthesis attributes that can be used to set other Quartus II options and settings in your HDL source code. The attributes described in the "chip_pin" and "Use I/O Flip-Flops" sections can help you make pin-related assignments in your HDL code, and the attribute described in the "Altera Attribute" section can be used to make any other Quartus II option or setting assignments in your HDL code. Assignments made with these synthesis attributes take precedence over assignments made through the Quartus II user interface, the Quartus II Settings File, or the Tcl interface.

Use I/O Flip-Flops

This attribute directs the Quartus II software to implement input, output, and output enable flip-flops (or registers) in I/O cells that have fast, direct connections to an I/O pin, when possible. Applying the `useioff` synthesis attribute can improve I/O performance by minimizing setup, clock-to-output, and clock-to-output enable times. This synthesis attribute is supported using the **Fast Input Register**, **Fast Output Register**, and **Fast Output Enable Register** logic options that can also be set in the **Assignment Editor**.

For more information about which device families support fast input, output, and output enable registers, refer to the device family data sheet, device handbook, or the Quartus II Help.

The `useioff` synthesis attribute takes a Boolean value and can only be applied to the port declarations of a top-level Verilog HDL module or VHDL entity (it is ignored if applied elsewhere). Setting the value to `1` (Verilog HDL) or `TRUE` (VHDL) instructs the Quartus II software to pack registers into I/O cells. Setting the value to 0 (Verilog HDL) or `FALSE` (VHDL) prevents register packing into I/O cells.

In Example 7–52 and 7–53, the `useioff` synthesis attribute directs the Quartus II software to implement the registers `a_reg`, `b_reg`, and `o_reg` in the I/O cells corresponding to the ports `a`, `b`, and `o` respectively.

Example 7–52. Verilog HDL Example of a useioff Attribute

```
module top_level(clk, a, b, o);
       input clk;
       input [1:0] a, b /* synthesis useioff = 1 */;
       output [2:0] o /* synthesis useioff = 1 */;
       reg [1:0] a_reg, b_reg;
       reg [2:0] o_reg;
       always @ (posedge clk)
       begin
           a_reg <= a;
           b_reg <= b;
           o_reg <= a_reg + b_reg;
       end
       assign o = o_reg;
endmodule
```

Verilog-2001 syntax also accepts the type of statements shown in Example 7–53 and 7–54 instead of the comment form shown in Example 7–52.

Example 7–53. Verilog-2001 Syntax for a useioff Attribute

```
(* useioff = 1 *)   input [1:0] a, b;
(* useioff = 1 *)   output [2:0] o;
```

Example 7–54. VHDL with a useioff Attribute

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity top_level is
   port (
      clk  : in  std_logic;
      a, b : in  unsigned(1 downto 0);
      o    : out unsigned(1 downto 0));
   attribute useioff : boolean;
   attribute useioff of a : signal is true;
   attribute useioff of b : signal is true;
   attribute useioff of o : signal is true;
end top_level;
architecture rtl of top_level is
   signal o_reg, a_reg, b_reg : unsigned(1 downto 0);
begin
   process(clk)
   begin
      a_reg <= a;
      b_reg <= b;
      o_reg <= a_reg + b_reg;
   end process;
   o <= o_reg;
end rtl;
```

Altera Attribute

This attribute enables you to apply Quartus II options and assignments to an object (entity, instance, or net) in your HDL source code. With `altera_attribute`, you can control synthesis options from your HDL source even when the options lack a specific HDL synthesis attribute (such as many of the logic options presented earlier in this chapter). You can also use this attribute to pass entity-level settings and assignments to phases of the Compiler flow beyond Analysis & Synthesis, such as Fitting.

Assignments and settings made with the Altera Attribute take precedence over assignments and settings made through the Quartus II user interface, the Quartus II Settings File, or the Tcl interface.

The syntax for setting this attribute in HDL is the same as the syntax for other synthesis attributes, as shown in "Synthesis Attributes" on page 7–21.

The attribute value is a single string containing a list of Quartus II Settings File variable assignments separated by semicolons, as shown in the following example:

```
-name <variable_1> <value_1>;-name <variable_2> <value_2>[;...]
```

If the Quartus II option or assignment includes a target, source, and/or section tag, use the following syntax for each Quartus II Settings File variable assignment.

```
-from <source> -to <target> -section_id <section>
-name <variable> <value>
```

The syntax for the full attribute value, including the optional target, source, and section tags for two different Quartus II Settings File assignments is shown in the following example:

```
"[-from <source_1>] [-to <target_1>] [-section_id
<section_1>] -name <variable_1> <value_1>; [-from <source_2>]
[-to <target_2>] [-section_id <section_2>] -name <variable_2>
<value_2>"
```

If a variable's assigned value is a string of text, you must use escaped quotes around the value, as in the following examples (using non-existent variable and value terms):

Verilog HDL

```
"VARIABLE_NAME \"STRING_VALUE\""
```

VHDL

```
"VARIABLE_NAME ""STRING_VALUE"""
```

To find the Quartus II Settings File variable name or value corresponding to a specific Quartus II option or assignment, you can make the option setting or assignment in the Quartus II user interface and then note the changes in the Quartus II Settings File. You can also refer to the *Quartus II Settings File Reference Manual* which documents all variable names.

Example 7–55, 7–56, and 7–57 use `altera_attribute` to set the power-up level of an inferred register. Note that for inferred instances, you cannot apply the attribute to the instance directly so you should apply the attribute to one of the instance's output nets. The Quartus II software moves the attribute to the inferred instance automatically.

Example 7–55. Verilog-1995 Example of Applying Altera Attribute to an Instance

```
reg my_reg /* synthesis altera_attribute = "-name POWER_UP_LEVEL HIGH" */;
```

Example 7–56. Verilog-2001 Example of Applying Altera Attribute to an Instance

```
(* altera_attribute = "-name POWER_UP_LEVEL HIGH" *) reg my_reg;
```

Example 7–57. VHDL Example of Applying Altera Attribute to an Instance

```
signal my_reg : std_logic;
attribute altera_attribute : string;
attribute altera_attribute of my_reg: signal is "-name POWER_UP_LEVEL
HIGH";
```

Example 7–58, 7–59, and 7–60 use the `altera_attribute` to disable the **Auto Shift Register Replacement** synthesis option for an entity. To apply the Altera Attribute to a VHDL entity, you must set the attribute on its architecture rather than on the entity itself.

Example 7–58. Verilog-1995 Example of Applying Altera Attribute to an Entity

```
module my_entity(…) /* synthesis altera_attribute = "-name
AUTO_SHIFT_REGISTER_RECOGNITION OFF" */;
```

Example 7–59. Verilog-2001 Example of Applying Altera Attribute to an Entity

```
(* altera_attribute = "-name AUTO_SHIFT_REGISTER_RECOGNITION OFF" *)
module my_entity(…) ;
```

Example 7–60. VHDL Example of Applying Altera Attribute to an Entity

```
entity my_entity is
-- Declare generics and ports
end my_entity;
architecture rtl of my_entity is
     attribute altera_attribute : string;
     -- Attribute set on architecture, not entity
     attribute altera_attribute of rtl: architecture is "-name
AUTO_SHIFT_REGISTER_RECOGNITION OFF";
begin
   -- The architecture body
end rtl;
```

You can also use altera_attribute for more complex assignments involving more than one instance. In Example 7–61, 7–62, and 7–63 the altera_attribute is used to cut all timing paths from reg1 to reg2, equivalent to this Tcl or QSF command:

```
set_instance_assignment -name CUT ON -from reg1 -to
reg2
```

Example 7–61. Verilog-1995 Example of Applying Altera Attribute with -to

```
reg reg2;
reg reg1 /* synthesis altera_attribute = "-name CUT ON -to reg2" */;
```

Example 7–62. Verilog-2001 Example of Applying Altera Attribute with -to

```
reg reg2;
(* altera_attribute = "-name CUT ON -to reg2" *) reg reg1;
```

Example 7–63. VHDL Example of Applying Altera Attribute with -to

```
signal reg1, reg2 : std_logic;
attribute altera_attribute: string;
attribute altera_attribute of reg1 : signal is "-name CUT ON -to reg2";
```

You may specify either the -to option or the -from option in a single altera_attribute; integrated synthesis automatically sets the remaining option to the target of the altera_attribute. You may also specify wildcards for either option. For example, if you specify "*" for the -to option instead of reg2 in these examples, the Quartus II software cuts all timing paths from reg1 to every other register in this design entity.

The altera_attribute can be used only for entity-level settings, and the assignments (including wildcards) apply only to the current entity.

chip_pin

This attribute enables you to assign pins to the ports of an entity or module in your HDL source. You may only assign pins to single-bit or one-dimensional bus ports in your design.

For single-bit ports, the value of the `chip_pin` attribute is the name of the pin on the target device, as specified by the device's pin table.

In addition to `chip_pin`, the Quartus II software supports the `altera_chip_pin_lc` attribute name for compatibility with other synthesis tools. When using this attribute in other synthesis tools, some older device families require an "@" symbol in front of each pin assignment. In the Quartus II software, the "@" is optional.

Example 7–64, 7–65, and 7–66 show different ways of assigning input pin `my_pin1` to Pin C1 and `my_pin2` to Pin 4 on a different target device.

Example 7–64. Verilog-1995 Examples of Applying Chip Pin to a Single Pin

```
input my_pin1 /* synthesis chip_pin = "C1" */;
input my_pin2 /* synthesis altera_chip_pin_lc = "@4" */;
```

Example 7–65. Verilog-2001 Example of Applying Chip Pin to a Single Pin

```
(* chip_pin = "C1" *) input my_pin1;
(* altera_chip_pin_lc = "@4" *) input my_pin2;
```

Example 7–66. VHDL Example of Applying Chip Pin to a Single Pin

```
entity my_entity is
     port(my_pin1: in std_logic; my_pin2: in std_logic;…);
end my_entity;
attribute chip_pin : string;
attribute altera_chip_pin_lc : string;
attribute chip_pin of my_pin1 : signal is "C1";
attribute altera_chip_pin_lc of my_pin2 : signal is "@4"
```

For bus I/O ports, the value of the chip pin attribute is a comma-delimited list of pin assignments. The order in which you declare the port's range determines the mapping of assignments to individual bits in the port. To leave a particular bit unassigned, simply leave its corresponding pin assignment blank.

Example 7–67 assigns `my_pin[2]` to `Pin_4`, `my_pin[1]` to `Pin_5`, and `my_pin[0]` to `Pin_6`.

Example 7–67. Verilog-1995 Example of Applying Chip Pin to a Bus of Pins

```
input [2:0]  my_pin /* synthesis chip_pin = "4, 5, 6" */;
```

Example 7–68 reverses the order of the signals in the bus, assigning `my_pin[0]` to `Pin_4` and `my_pin[2]` to `Pin_6` but leaves `my_pin[1]` unassigned.

Example 7–68. Verilog-1995 Example of Applying Chip Pin to Part of a Bus

```
input [0:2]  my_pin /* synthesis chip_pin = "4, ,6" */;
```

Example 7–69 assigns `my_pin[2]` to Pin `4` and `my_pin[0]` to Pin `6`, but leaves `my_pin[1]` unassigned.

Example 7–69. VHDL Example of Applying Chip Pin to Part of a Bus of Pins

```
entity my_entity is
     port(my_pin: in std_logic_vector(2 downto 0);…);
end my_entity;

attribute chip_pin of my_pin: signal is "4, , 6";
```

Analyzing Synthesis Results

After you have performed synthesis, you can check your synthesis results in the following locations:

- Messages
- Analysis & Synthesis Section of Compilation Report
- Project Navigator

Messages

The messages that appear during Analysis & Synthesis describe many of the optimizations that the software performs during the synthesis stage, and provide information about how the design is interpreted. You should always check the messages to analyze critical warnings and warnings, because these messages may relate to important design problems. It is also useful to read the Information messages to get more information about how the software processes your design.

Analysis & Synthesis Section of Compilation Report

The Compilation Report, which provides a summary of results for the project, appears after a successful compilation, or you can choose it from the Processing menu. After Analysis & Synthesis, before the Fitter begins, the Summary information provides a summary of utilization based on synthesis data, before fitter optimizations have occurred. Synthesis-specific information is listed in the Analysis & Synthesis section.

There are various report sections under Analysis & Synthesis, including a list of the source files read for the project, the resource utilization by entity after synthesis, and information about state machines, latches, optimization results, and parameter settings.

For more information about each report section, refer to the Quartus II Help.

Project Navigator

The Hierarchy tab of the Project Navigator provides a summary of resource information about the entities in the project. After Analysis & Synthesis, before the Fitter begins, the Project Navigator provides a summary of utilization based on synthesis data, before Fitter optimizations have occurred.

If you hold your mouse pointer over one of the entities in the Hierarchy tab, a tooltip that shows parameter information for each instance.

VHDL & Verilog HDL Messages

The Quartus II software issues a variety of messages when it is analyzing and elaborating the Verilog HDL and VHDL files in your design. These HDL messages help you identify potential problems early in the design process.

HDL Message Types

HDL messages fall into three categories: Info, Warning, and Error.

- **Info message**—Lists a property of your design.
- **Warning message**—Indicates a potential problem in your design. Potential problems come from a variety of sources, including typos, inappropriate design practices, or the functional limitations of your target device. Though HDL warning messages do not always identify actual problems, you should always investigate code that generates an HDL warning. Otherwise, the synthesized behavior of your design might not match your original intent or its simulated behavior.
- **Error message**—Indicates an actual problem with your design. Your HDL code may be invalid due to a syntax or semantic error, or it may not be synthesizable as written. Consult the Help associated with any HDL error messages for assistance in removing the error from your design.

In Example 7–70, the sensitivity list contains multiple copies of the variable `i`. While the Verilog HDL language does not prohibit duplicate entries in a sensitivity list, it is clear that this design has a typo: Variable `j` should be listed on the sensitivity list to avoid a possible simulation/synthesis mismatch.

Example 7–70. Generating an HDL Warning Message

```
//dup.v
module dup(input i, input j, output reg o);
always @ (i)
    o = i & j;
endmodule
```

When processing this HDL code, the Quartus II software generates the following warning message:

```
Warning: (10276) Verilog HDL sensitivity list warning
at dup.v(2): sensitivity list contains multiple
entries for "i".
```

In Verilog HDL, variable names are case-sensitive, so the variables my_reg and MY_REG in Example 7–71 are two different variables. However, declaring variables whose names only differ in case may confuse some users, especially those users who use VHDL, where variables are not case-sensitive.

Example 7–71. Generating HDL Info Messages

```
// namecase.v
module namecase (input i, output o);
    reg my_reg;
    reg MY_REG;
    assign o = i;
endmodule
```

When processing this HDL code, the Quartus II software generates the following informational message:

```
Info: (10281) Verilog HDL information at
namecase.v(3): variable name "MY_REG" and variable
name "my_reg" should not differ only in case.
```

In addition, the Quartus II software generates additional HDL info messages to inform you that neither my_reg or MY_REG are used in this small design:

```
Info: (10035) Verilog HDL or VHDL information at
namecase.v(3): object "my_reg" declared but not used
Info: (10035) Verilog HDL or VHDL information at
namecase.v(4): object "MY_REG" declared but not used
```

Controlling the Display of HDL Messages

The Quartus II software allows you to control how many HDL messages you see during the analysis and elaboration of your design files. You can set the HDL Message Level to enable or disable groups of HDL messages, or you can enable or disable specific messages.

For more information about synthesis directives and their syntax, refer to "Synthesis Directives" on page 7–24.

These options are in addition to the general message suppression options in the Quartus II software. For more information about suppressing other messages, refer to the *Quartus II Project Management* chapter in volume 2 of the *Quartus II Handbook*.

Setting the HDL Message Level

The HDL Message Level specifies the types of messages that the Quartus II software displays when it is analyzing and elaborating your design files. Table 7–6 details the information about the HDL message levels.

Table 7–6. HDL Info Message Level

Level	Purpose	Description
Level1	Displays high-severity messages only	If you want to see only those HDL messages that identify likely problems with your design, select **Level1**. When **Level1** is selected, the Quartus II software will only issue a message if there is a high probability that it points an actual problem with your design.
Level2	Displays high-severity and medium-severity messages	If you want to see additional HDL messages that identify possible problems with your design, select **Level2**. This is the default setting.
Level3	Displays all messages, including low-severity message	If you want to see all HDL info and warning messages, select **Level3**. This level includes extra "LINT" messages that suggest changes to improve the style of your HDL code or make it easier to understand.

You should address all issues reported at the **Level1** setting. The default HDL message level is **Level2**.

To set the HDL Message Level in the user interface, on the Assignments menu, click **Settings**; under Category, click **Analysis & Synthesis Settings**. Set the HDL Message Level.

You can override this default setting in a source file with the `message_level synthesis` directive, which takes the values **level1**, **level2**, and **level3**, as shown in Example 7–72 and 7–73.

Example 7–72. Verilog HDL Examples of message_level Directive

```
// altera message_level level1
                    or
/* altera message_level level3 */
```

Example 7–73. VHDL Example of message_level Directive

```
-- altera message_level level2
```

A message_level synthesis directive remains effective until the end of a file or until the next message_level directive. In VHDL, you can use the message_level synthesis directive to set the HDL Message Level for entities and architectures, but not for other design units. An HDL Message Level for an entity applies to its architectures, unless overridden by another message_level directive. In Verilog HDL, you can use the message_level directive to set the HDL Message Level for a module.

Enabling or Disabling Specific HDL Messages

You can enable or disable a specific HDL info or warning message with its Message ID, which is displayed in parentheses at the beginning of the message. Enabling or disabling a specific message overrides its HDL Message Level.

To disable specific HDL messages in the GUI, from the Settings menu, select **Analysis & Synthesis Settings** and click the **Advanced** button next to the HDL Message Level setting. In the Advanced Message Settings dialog box, add the Message IDs you wish to enable or disable.

To enable or disable specific HDL messages in your HDL, use the message_on and message_off synthesis directives. Both directives take a space-separated list of Message IDs. You can enable or disable messages with these synthesis directives immediately before Verilog HDL modules, VHDL entities, or VHDL architectures. You cannot enable or disable a message in the middle of an HDL construct.

A message enabled or disabled via a message_on or message_off synthesis directive overrides its HDL Message Level or any message_level synthesis directive. The message will remain disabled until the end of the source file or until its status is changed by another message_on or message_off directive.

Example 7–74. Verilog HDL message_off Directive for Message with ID 10000

```
// altera message_off 10000
```

or

```
/* altera message_off 10000 */
```

Example 7–75. VHDL message_off Directive for Message with ID 10000

```
-- altera message_off 10000
```

Node-Naming Conventions in Quartus II Integrated Synthesis

Being able to find the logic node names after synthesis can be useful during verification or while debugging a design. This section provides an overview of the conventions used by the Quartus II software when it names the nodes created from your HDL design. The section focuses on the conventions for Verilog HDL and VHDL code, but AHDL and BDFs are discussed when appropriate.

Whenever possible, as described in this section, Quartus II integrated synthesis uses wire or signal names from your source code to name nodes such as LEs or ALMs. Some nodes, such as registers, have predictable names that typically do not change when a design is resynthesized. The names of other nodes, particularly LEs or ALMs that contain only combinational logic, can change due to logic optimizations that the software performs.

Synthesis netlist optimizations also change node names because nodes are changed, combined, and duplicated to optimize the design.

For more information about the type of optimizations performed by synthesis netlist optimizations, refer to *Netlist Optimizations & Physical Synthesis* in volume 2 of the *Quartus II handbook*.

The Quartus II Fitter can also change node names after synthesis. For example when the Fitter uses register packing to pack a register into an I/O element, or when logic is modified by physical synthesis.

Hierarchical Node-Naming Conventions

To make each name in the design unique, the Quartus II software adds the hierarchy path to the beginning of each name. The "|" separator is used to indicate a level of hierarchy. For each instance in the hierarchy, the software adds the entity name and the instance name of that entity, using the ":" separator between each entity name and its instance name. For example, if a design instantiates entity `A` with the name `my_A_inst`, the hierarchy path of that entity would be `A:my_A_inst`. The full name of any node is obtained by starting with the hierarchical instance path; followed by a "|", and ending with the node name inside that entity, using the following convention:

<entity 0>:*<instance_name 0>*|*<entity 1>*:
<instance_name 1>|...|*<instance_name n>*

For example, if entity A contains a register (DFF atom) called `my_dff`, its full hierarchy name would be `A:my_A_inst|my_dff`.

You can turn off the **Display Entity Name for Node Name** option on the **Compilation Process Settings** page of the **Settings** dialog box to instruct the Compiler to generate node names that do not contain the name for each level of the hierarchy. With this option on, the node names use the following convention:

<instance_name 0>|<instance_name 1>|...|<instance_name n>

Node-Naming Conventions for Registers (DFF or D Flip-Flop Atoms)

In Verilog HDL and VHDL, inferred registers are named after the `reg` or `signal` connected to the output.

For example, the following is a description of a register in Verilog HDL that creates a DFF primitive called `my_dff_out`:

Example 7–76. Verilog HDL Register

```
wire dff_in, my_dff_out, clk;

always @ (posedge clk)
  my_dff_out <= dff_in;
```

Similarly, Example 7–77 is a description of a register in VHDL that creates a DFF primitive called `my_dff_out`.

Example 7–77. VHDL Register

```
signal dff_in, my_dff_out, clk;
process (clk)
  begin
  if (rising_edge(clk)) then
    my_dff_out <= dff_in;
  end if;
end process;
```

In AHDL designs, DFF registers are declared explicitly rather than inferred, so the software uses the user-declared name for the register.

For schematic designs using BDF, all elements are given a name when they are instantiated in the design, so the software uses the user-defined name for the register or DFF.

In the special case that a wire or signal (such as `my_dff_out` in the above examples) is also an output pin of your top-level design, the Quartus II software cannot use that name for the register (e.g., cannot use

my_dff_out) because the software requires that all logic and I/O cells have unique names. In this case, the Quartus II integrated synthesis appends ~reg0 to the register name.

For example, the Verilog HDL code in Example 7–78 produces a register called q~reg0:

Example 7–78. Verilog HDL Register Feeding Output Pin

```
module my_dff (input clk, input d, output q);
  always @ (posedge clk)
    q <= d;
endmodule
```

This situation occurs only for registers driving top-level pins. If a register drives a port of a lower level of the hierarchy, then the port is removed during hierarchy flattening and the register retains its original name, in this case, q.

Register Changes During Synthesis

On some occasions, you may not be able to find registers that you expect to see in the synthesis netlist. Registers may be removed by logic optimization, or their names may be changed due to synthesis optimization. Common optimizations include inference of a state machine, counter, adder-subtractor, or shift register from registers and surrounding logic. Other common register changes occur when registers are packed into dedicated hardware on the FPGA such as a DSP block or a RAM block.

This section describes the device features that affect register names:

- State machines
- Inferred adder-subtractors, shift registers, memory, and DSP functions
- Input and output registers of RAM and DSP blocks

State Machines

If a state machine is inferred from your HDL code, then the registers that represent the states will be mapped into a new set of registers that implement the state machine. Most commonly, the software converts the state machine into a one-hot form where each state is represented by one register. In this case for Verilog HDL or VHDL designs, the registers are named according to the name of the state register and the states, where possible.

For example, consider a Verilog HDL state machine where the states are `parameter state0 = 1, state1 = 2, state2 = 3`, and where the state machine register is declared as `reg [1:0] my_fsm`. In this example, the three one-hot state registers are named `my_fsm.state0`, `my_fsm.state1`, and `my_fsm.state2`.

In AHDL, state machines are explicitly specified with a machine name. State machine registers are given synthesized names based on the state machine name but not the state names. For example, if a state machine is called `my_fsm` and has four state bits, they may be synthesized with names such as `my_fsm~12`, `my_fsm~13`, `my_fsm~14`, and `my_fsm~15`.

Inferred Adder-Subtractors, Shift Registers, Memory & DSP Functions

The Quartus II software infers megafunctions from Verilog HDL and VHDL code for logic that forms adder-subtractors, shift registers, RAM, ROM, and arithmetic functions that can be placed in DSP blocks.

For information about inferring megafunctions, refer to the *Recommended HDL Coding Styles* chapter in the *Quartus II Handbook*.

Because adder-subtractors are part of a megafunction instead of generic logic, the combinational logic exists in the design with different names. For shift registers, memory, and DSP functions, the registers and logic are typically implemented inside the dedicated RAM or DSP blocks in the device. Thus, the registers are not visible as separate LEs or ALMs.

Input & Output Registers of RAM & DSP Blocks

Registers can be packed into the input registers and output registers of RAM and DSP blocks, so that they are not visible as separate registers in LEs or ALMs.

For information about packing registers into RAM and DSP megafunctions, refer to the *Recommended HDL Coding Styles* chapter in the *Quartus II Handbook*.

Node-Naming Conventions for Combinational Logic Cells

Whenever possible for Verilog HDL, VHDL, and AHDL code, the Quartus II software uses wire names that are the targets of assignments, but may change the node names due to synthesis optimizations.

For example, consider the Verilog HDL code in Example 7–79. Quartus II integrated synthesis uses the names `c`, `d`, `e`, and `f` for the combinational logic cells that are produced.

Example 7–79. Naming Nodes for Combinational Logic Cells in Verilog HDL

```
wire c;
reg d, e, f;

assign c = a | b;
always @ (a or b)
    d = a & b;
always @ (a or b) begin : my_label
    e = a ^ b;
end

always @ (a or b)
    f = ~(a | b);
```

For schematic designs using BDF, all elements are given a name when they are instantiated in the design and the software uses the user-defined name when possible.

If logic cells, such as those created in the above example, are packed with registers in device architectures such as the Stratix and Cyclone device families, those names may not appear in the netlist after fitting. In other devices such as the Stratix II and Cyclone II device families, the register and combinational nodes are kept separate throughout the compilation, so these names are more often maintained through fitting.

When logic optimizations occur during synthesis, it is not always possible to retain the initial names as described above. In some cases, synthesized names will be used, which are the wire names with a tilde (~) and a number appended. For example, if a complex expression is assigned to a wire `w` and that expression generates several logic cells, those cells may have names such as `w`, `w~1`, `w~2`, and so on. Sometimes the original wire name `w` is removed, and an arbitrary name such as `rtl~123` is created. It is a goal of Quartus II integrated synthesis to retain user names whenever possible. Any node name ending with ~<*number*> is a name created during synthesis, which may change if the design is

changed and re-synthesized. Knowing these naming conventions can help you understand your post-synthesis results and make it easier to debug your design or make assignments.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The *Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

You can specify many of the options described in this section either on an instance, or global level, or both.

Use the following Tcl command to make a global assignment:

```
set_global_assignment -name <QSF Variable Name> <Value>
```

Use the following Tcl command to make an instance assignment:

```
set_instance_assignment -name <QSF Variable Name> <Value>\
-to <Instance Name>
```

Quartus II Synthesis Options

Table 7–7 lists the Quartus II Settings File variable names and applicable values for the settings discussed in this chapter. The Quartus II Settings File variable name is used in the Tcl assignment to make the setting along with the appropriate value. The *Type* column indicates whether the setting is supported as a Global setting, or an Instance setting, or both.

Table 7–7. Quartus II Synthesis Options (Part 1 of 2)

Setting Name	Quartus II Settings File Variable	Values	Type
Allow Any RAM Size for Recognition	ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION	ON, OFF	Global, Instance
Allow Any ROM Size for Recognition	ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION	ON, OFF	Global, Instance
Allow Any Shift Register Size for Recognition	ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION	ON, OFF	Global, Instance
Auto DSP Block Replacement	AUTO_DSP_RECOGNITION	ON, OFF	Global, Instance
Auto RAM Replacement	AUTO_RAM_RECOGNITION	ON, OFF	Global, Instance
Auto ROM Replacement	AUTO_ROM_RECOGNITION	ON, OFF	Global, Instance
Auto Shift-Register Replacement	AUTO_SHIFT_REGISTER_RECOGNITION	ON, OFF	Global, Instance
Fast Input Register	FAST_INPUT_REGISTER	ON, OFF	Instance
Fast Output Enable Register	FAST_OUTPUT_ENABLE_REGISTER	ON, OFF	Instance
Fast Output Register	FAST_OUTPUT_REGISTER	ON, OFF	Instance
Implement as Output of Logic Cell	IMPLEMENT_AS_OUTPUT_OF_LOGIC_CELL	ON, OFF	Instance
Maximum Fan-Out	MAX_FANOUT	*<Maximum Fan-Out Value>*	Instance
Optimization Technique	*<device family>*_OPTIMIZATION_TECHNIQUE	Area, Speed, Balanced	Global, Instance
PowerPlay Power Optimization	OPTIMIZE_POWER_DURING_SYNTHESIS	"NORMAL COMPILATION", "EXTRA EFFORT", OFF	Global, Instance
Power-Up Don't Care	ALLOW_POWER_UP_DONT_CARE	ON, OFF	Global

Table 7–7. Quartus II Synthesis Options (Part 2 of 2)

Setting Name	Quartus II Settings File Variable	Values	Type
Power-Up Level	POWER_UP_LEVEL	HIGH, LOW	Instance
Preserve Hierarchical Boundary	PRESERVE_HIERARCHICAL_BOUNDARY	Off, Relaxed, Firm	Instance
Preserve Registers	PRESERVE_REGISTER	ON, OFF	Instance
Remove Duplicate Logic	REMOVE_DUPLICATE_LOGIC	ON, OFF	Global, Instance
Remove Duplicate Registers	REMOVE_DUPLICATE_REGISTERS	ON, OFF	Global, Instance
Remove Redundant Logic Cells	REMOVE_REDUNDANT_LOGIC_CELLS	ON, OFF	Global
Restructure Multiplexers	MUX_RESTRUCTURE	On, Off, Auto	Global, Instance
Speed Optimization Technique for Clock Domains	SYNTH_CRITICAL_CLOCK	ON, OFF	Instance
State Machine Processing	STATE_MACHINE_PROCESSING	AUTO, "MINIMAL BITS", "ONE HOT", "USER-ENCODED"	Global, Instance

Assigning a Pin

Use the following Tcl command to assign a signal to a pin or device location.

```
set_location_assignment -to <signal name> <location>
```

For example,

```
set_location_assignment -to data_input Pin_A3
```

Valid locations are pin location names. Some device families also support edge and I/O bank locations. Edge locations are EDGE_BOTTOM, EDGE_LEFT, EDGE_TOP, and EDGE_RIGHT. I/O bank locations include IOBANK_1 to IOBANK_n, where n is the number of I/O banks in a particular device.

Preparing a Design for Incremental Synthesis

To set up your design for incremental synthesis, identify design partitions and enable incremental synthesis.

Creating Design Partitions

To create a partition, use the following command:

```
set_instance_assignment -name PARTITION_HIERARCHY \
<file name> -to <destination> -section_id <partition name>
```

The <*destination*> should be the entity's short hierarchy path. A short hierarchy path is the full hierarchy path without the top-level name, for example: "`ram:ram_unit|altsyncram:altsyncram_component`" (with quotation marks). For the top-level partition, you can use the pipe (|) symbol to represent the top-level entity.

For more information about hierarchical naming conventions, refer to "Node-Naming Conventions in Quartus II Integrated Synthesis" on page 7–65.

The <*partition name*> is the user-designated partition name, which must be unique and less than 1024 characters long. The name can consist only of alpha-numeric characters, as well as pipe (|), colon (:) and underscore (_) characters. Altera recommends enclosing the name in double quotation marks (" ").

The <*file name*> is the name used for internally generated netlists files during incremental compilation. Netlists are named automatically by the Quartus II software based on the instance name if you create the partition in the user interface. If you are using Tcl to create your partitions, you must assign a custom file name that is unique across all partitions. For the top-level partition, the specified file name is ignored, and you can use any dummy value. To ensure the names are safe and platform independent, file names must be unique regardless of case. For example, if a partition uses the file name `my_file`, no other partition can use the file name `MY_FILE`. For simplicity, Altera recommends that you base each file name on the corresponding instance name for the partition.

The software stores all netlists in the **db** compilation database directory.

Enabling Incremental Synthesis

Turn on incremental synthesis using the following Tcl command:

```
set_global_assignment -name INCREMENTAL_COMPILATION \
INCREMENTAL_SYNTHESIS
```

Synthesizing a Design Using Incremental Synthesis

Once incremental synthesis is turned on in the Quartus II Settings File file, or through a Tcl command, incremental synthesis automatically occurs when you compile using the `execute_flow -compile` command for the **quartus_sh** compiler executable.

Synthesizing Using the Synthesis & Merge Commands
Use the separate synthesis and merge commands if you compile your design using the individual compiler executables (e.g., **quartus_map** and **quartus_fit**) instead of using the `execute_flow -compile` command for the **quartus_sh** compiler executable.

To enable incremental synthesis when using the **quartus_map** executable, perform the following two steps:

1. Type the following command at a command prompt:

```
quartus_map --incremental compilation=incremental_synthesis ↵
```

This command enables the flow in the project, so subsequent synthesis runs can be performed with the `quartus_map` command without the incremental compilation option.

2. Merge the synthesized partitions to create a flattened netlist for further stages of the Quartus II compilation flow, including fitting. Type the following command at a system command prompt:

```
quartus_cdb --merge ↵
```

Conclusion

The Quartus II software includes complete Verilog HDL and VHDL language support, as well as support for Altera-specific languages, making it an easy-to-use, standalone solution for Altera designs. You can use the synthesis options available in the software to help you improve your synthesis results, giving you more control over the way your design is synthesized.

8. Synplicity Synplify & Synplify Pro Support

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Introduction

As programmable logic device (PLD) designs become more complex and require increased performance, advanced synthesis has become an important part of the design flow. This chapter documents support for the Synplicity Synplify and Synplify Pro software in the Quartus® II software, as well as key design flows, methodologies, and techniques for achieving good results in Altera® devices, including the following topics:

- General design flow with the Synplify and Quartus II software
- Synplify software optimization strategies, including timing-driven compilation settings, optimization options, and Altera-specific attributes
- Exporting designs and constraints to the Quartus II software using NativeLink® integration
- Guidelines for Altera megafunctions and library of parameterized module (LPM) functions, instantiating them in a clear- or black-box flow with the MegaWizard® Plug-In Manager, and tips for inferring them from hardware description language (HDL) code
- Incremental compilation and block-based design, including the Synplify Pro software MultiPoint flow

The content in this chapter applies to both the Synplify and Synplify Pro software unless otherwise specified.

This chapter assumes that you have set up, licensed, and are familiar with the Synplify or Synplify Pro software.

For more information about obtaining, licensing, and using the Synplify software, refer to the Synplicity web site at **www.synplicity.com**.

Design Flow

A Quartus II software design flow using the Synplify software consists of the following steps:

1. Create Verilog HDL or VHDL design files in the Quartus II software, Synplify software, or a text editor.
2. Set up a project in the Synplify software and add the HDL design files for synthesis.
3. Select a target device and add timing constraints and compiler directives to optimize the design during synthesis.

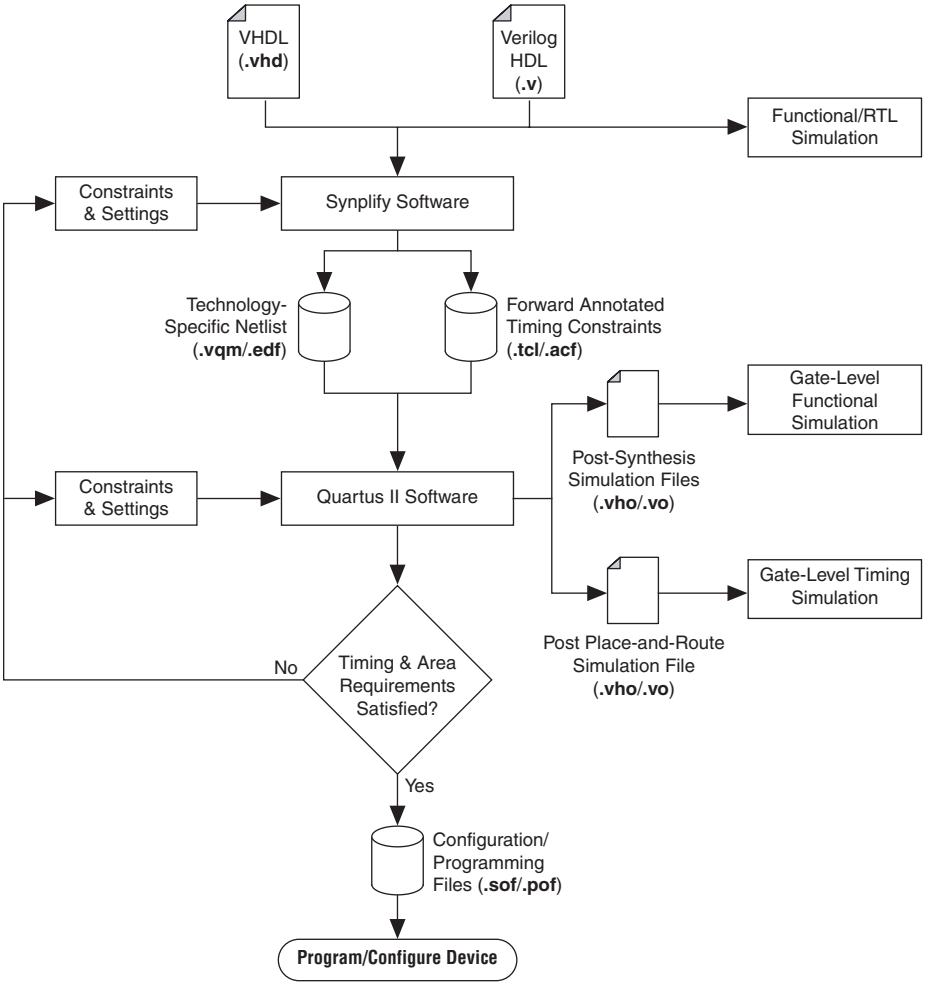
4. Synthesize the design in the Synplify software.

5. Create a Quartus II project and import the technology-specific netlist and the tool command language (Tcl) constraint file generated by the Synplify software into the Quartus II software for placement and routing, and for performance evaluation.

6. After obtaining place-and-route results that meet your needs, configure or program the Altera device.

Figure 8–1 shows the recommended design flow when using the Synplify and the Quartus II software.

Figure 8–1. Recommended Design Flow



The Synplify and Synplify Pro software support both VHDL and Verilog HDL source files. The Synplify Pro software also supports mixed synthesis, allowing a combination of VHDL and Verilog HDL source files.

Specify timing constraints and attributes for the design in a Synplify Constraints File (**.sdc**) with the SCOPE editor in the Synplify software or directly in the HDL source file. Compiler directives can also be defined in the HDL source file. Many of these constraints are forward-annotated in the Tcl file for Quartus II software use. You can save all project options and included files in a Synplify Project file (**.prj**).

The HDL Analyst that is included in the Synplify software is a graphical tool for generating schematic views of the technology-independent register transfer level (RTL) view netlist (**.srs**) and technology-view netlist (**.srm**) files. You can use the Synplify HDL Analyst to visually analyze and debug your design. The HDL Analyst supports cross probing between the RTL and Technology views, the HDL source code, and the Finite State Machine (FSM) viewer. Refer to "FSM Compiler" on page 8–9.

A separate license file is required to enable the HDL Analyst in the Synplify software. The Synplify Pro software includes the HDL Analyst.

Once synthesis is complete, import the electronic design interchange format (EDIF) or Verilog Quartus Mapping (VQM) netlist to the Quartus II software for place-and-route. You can use the Tcl file generated by the Synplify software to forward-annotate your constraints, and optionally to set up your project in the Quartus II software.

If the area and timing requirements are satisfied, use the files generated by the Quartus II software to program or configure the Altera device. As shown in Figure 8–1, if your area or timing requirements are not met, you can change the constraints in the Synplify software or the Quartus II software and repeat the synthesis. Repeat the process until the area and timing requirements are met.

While you can perform simulation at various points in the process, final timing analysis should be performed after placement and routing is complete. Formal verification may also be performed at various stages of the design process.

For more information about how the Synplify software supports formal verification, refer to the *Formal Verification* section in volume 3 of the *Quartus II Handbook*.

You can also use other options and techniques in the Quartus II software to meet area and timing requirements. One such option is called WYSIWYG Primitive Resynthesis, which can perform optimizations on your VQM netlist within the Quartus II software.

For information about netlist optimizations, refer to the *Netlist Optimizations & Physical Synthesis* chapter in volume 2 of the *Quartus II Handbook*.

In some cases, you may be required to modify the source code if area and timing requirements cannot be met using options in the Synplify and Quartus II software.

After synthesis, the Synplify software produces several intermediate and output files. Table 8–1 lists these file types.

Table 8–1. Synplify Intermediate & Output Files

File Extensions	File Description
.srs	Technology-independent RTL netlist that can be read only by the Synplify software
.srm	Technology view netlist
.srr *(1)*	Synthesis Report file
.edf/.vqm *(2)*	Technology-specific netlist in electronic design interchange format (EDIF) or VQM file format
.acf/.tcl *(3)*	Forward-annotated constraints file containing constraints and assignments

Notes to Table 8–1:

(1) This report file includes performance estimates that are often based on pre-place-and-route information. Use the f_{MAX} reported by the Quartus II software after place-and-route, because it is the only reliable source of timing information. This report file includes post-synthesis device resource utilization statistics that may inaccurately predict resource usage after place-and-route. The Synplify software does not account for black box functions nor for logic usage reduction achieved through register packing performed by the Quartus II software. Register packing combines a single register and look-up table (LUT) into a single logic cell, reducing the logic cell utilization below the Synplify software estimate. Use the device utilization reported by the Quartus II software after place-and-route.

(2) An EDIF output file (**.edf**) is created only for ACEX® 1K, FLEX® 10K, FLEX 10KA, FLEX 10KE, FLEX 6000, FLEX 8000, MAX® 7000, MAX 9000, and MAX 3000 devices. A VQM file is created for all other Altera device families.

(3) An Assignment and Configuration File (**.acf**) file is created only for ACEX 1K, FLEX 10K, FLEX 10KA, FLEX 10KE, FLEX 6000, FLEX 8000, MAX 7000, MAX 9000, and MAX 3000 devices. The ACF is generated for backward compatibility with the MAX+PLUS® II software. A Tcl file for the Quartus II software is created for all devices, and also contains Tcl commands to create a Quartus II project and, if applicable, the MAX+PLUS® II assignments are imported from the ACF file.

Output Netlist File Name & Result Format

Specify the output netlist directory location and name by performing the following steps:

1. On the Project menu, click **Implementation Options**.
2. Click the **Implementation Results** tab.

3. In the **Results Directory** box, type your output netlist file directory location.

4. In the **Result File Name** box, type your output netlist file name.

By default, directory and file name are set to the project implementation directory and the top-level design module or entity name.

The **Result Format** and **Quartus version** options are also available on the **Implementation Results** tab. The **Result Format** list specifies an EDIF or VQM netlist depending on your device family. The software creates an EDIF output netlist file only for ACEX 1K, FLEX 10K, FLEX 10KA, FLEX 10KE, FLEX 6000, FLEX 8000, MAX 7000, MAX 9000, and MAX 3000 devices. For other Altera devices, the software generates a VQM-formatted netlist.

Beginning with the Synplify software version 8.4, select the version of the Quartus II software that you are using in the **Quartus version** list. This option ensures that the netlist is compatible with the software version and supports the newest features. Altera recommends using the latest version of the Quartus II software whenever possible. If your Quartus II software is newer than the versions available in the **Quartus version** list, check if there is a newer version of the Synplify software available that supports the current Quartus II software version. Otherwise, choose the latest version in the list for the best compatibility.

Synplify Optimization Strategies

As designs become more complex and require increased performance, using different optimization strategies has become important. Combining Synplify software constraints with VHDL and Verilog HDL coding techniques and Quartus II software options can help you obtain the required results.

For additional design and optimization techniques, refer to the *Design Recommendations for Altera Devices* chapter in volume 1 and the *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

The Synplify software offers many constraints and optimization techniques to improve your design's performance. The Synplify Pro software adds some additional techniques that are not supported in the basic Synplify software. Wherever this document describes Synplify support, this includes both the basic Synplify and the Synplify Pro software; Synplify Pro-only features are labeled as such. This section provides an overview of some of the techniques you can use to help improve the quality of your results.

For more information about applying the attributes discussed in this section, refer to the *Tasks & Tips* chapter of the *Synplify Software User Guide*.

Implementations in Synplify Pro

In the Synplify Pro software, on the Project menu, click **New Implementation** to create different synthesis results without overwriting the others. For each implementation, specify the target device, synthesis options, and constraint files. Each implementation generates its own subdirectory that contains all the resulting files, including VQM and Tcl files, from a compilation of the particular implementation. You can then compare the results of the different implementations to find the optimal set of synthesis options and constraints for a design.

Timing-Driven Synthesis Settings

The Synplify software supports timing-driven synthesis through user-assigned timing constraints to optimize the performance of the design. The Synplify software optimizes the design to attempt to meet these constraints.

The Quartus II NativeLink feature allows timing constraints that are applied in the Synplify software to be forward-annotated for the Quartus II software using a Tcl script file for timing-driven place and route. Refer to "Passing Constraints to the Quartus II Software" for more details about how constraints such as clock frequencies, false paths, and multicycle paths are forward-annotated. This section explains some of the important timing constraints in the Synplify software.

The Synplify Synthesis Report File (**.srr**) contains timing reports of estimated place-and-route delays. The Quartus II software can perform further optimizations on a post-synthesis netlist from third-party synthesis tools. In addition, designs may contain black boxes or IP functions that have not been optimized by the third-party synthesis software. Actual timing results are obtained only after the design has gone through full placement and routing in the Quartus II software. For these reasons, the Quartus II post place-and-route timing reports provide a more accurate representation of the design. The statistics in these reports should be used to evaluate design performance.

Clock Frequencies

For single-clock designs, specify a global frequency when using the push-button flow. While this flow is simple and provides good results, often it does not meet the performance requirements for more advanced

designs. You can use timing constraints, compiler directives, and other attributes to help optimize the performance of a design. You can enter these attributes and directives directly in the HDL code. Alternatively, you can enter attributes (not directives) into an SDC file with the SCOPE editor in the Synplify software.

Use the SCOPE editor to set global frequency requirements for the entire design and individual clock settings. Use the **Clocks** tab in the SCOPE editor to specify frequency (or period), rise times, fall times, duty cycle, and other settings. Assigning individual clock settings, rather than over-constraining the global frequency, helps the Quartus II software and the Synplify software achieve the fastest clock frequency for the overall design. The `define_clock` attribute assigns clock constraints.

Multiple Clock Domains

The Synplify software can perform timing analysis on unrelated clock domains. Each clock group is a different clock domain and is treated as unrelated to the clocks in all other clock groups. All the clocks in a single clock group are assumed to be related and the Synplify software automatically calculates the relationship between the clocks. You can assign clocks to a new clock group, or put related clocks in the same clock group by using the **Clocks** tab in the SCOPE editor or with the `define_clock` attribute.

Input/Output Delays

Specify the input and output delays for the ports of a design in the **Input/Output** tab of the SCOPE editor or with the `define_input_delay` and `define_output_delay` attributes. The Synplify software does not allow you to assign the t_{CO} and t_{SU} values directly to inputs and outputs. However, a t_{CO} value can be inferred by setting an external output delay, and a t_{SU} value can be inferred by setting an external input delay. The following equations illustrate the relationship between t_{CO}/t_{SU} and the input/output delays:

(1) t_{CO} = clock period – external output delay

(2) t_{SU} = clock period – external input delay

When the `syn_forward_io_constraints` attribute is set to 1, the Synplify software passes the external input and output delays to the Quartus II software using NativeLink integration. The Quartus II software then uses the external delays to calculate the maximum system frequency.

Multicycle Paths

Specify any multicycle paths in the design in the **Multi-Cycle Paths** tab of the SCOPE editor or with the `define_multicycle_path` attribute. A multicycle path is a path that requires more than one clock cycle to propagate. It is important to specify which paths are multicycle to avoid having the Quartus II and the Synplify compilers work excessively on a non-critical path. Not specifying these paths can also result in an inaccurate critical path being reported during timing analysis.

False Paths

False paths are paths that should not be considered during timing analysis or which should be assigned low (or no) priority during optimization. Some examples of false paths are slow asynchronous resets and test logic added to the design. Set these paths in the **False Paths** tab of the SCOPE editor. Use the `define_false_path` attribute.

FSM Compiler

If the FSM Compiler is turned on, the compiler automatically detects state machines in a design. The compiler can then extract and optimize the state machine. The FSM Compiler analyzes the state machine and decides to implement sequential, gray, or one-hot encoding based on the number of states. It also performs unused-state analysis, optimization of unreachable states, and minimization of transition logic.

If the FSM Compiler is turned off, the compiler does not infer state machines. The state machines are implemented as coded in the HDL code. Thus, if the coding style for the state machine was sequential, then the implementation is also sequential. If the FSM Compiler is turned on, the compiler infers the state machines. The implementation is based on the number of states regardless of the coding style in the HDL code.

You can use the `syn_state_machine` complier directive to specify or prevent a state machine from being extracted and optimized. To override the default encoding of the FSM Compiler, use the `syn_encoding` directive.

The values for the syn_encoding directive are shown in Table 8–2.

Table 8–2. syn_encoding Directive Values

Value	Description
Sequential	Generates state machines with the fewest possible flip-flops. Sequential, also called binary, state machines are useful for area-critical designs when timing is not the primary concern.
Gray	Generates state machines where only one flip-flop changes during each transition. Gray-encoded state machines tend to be free of glitches.
One-hot	Generates state machines containing one flip-flop for each state. One-hot state machines typically provide the best performance and shortest clock-to-output delays. However, one-hot implementations are usually larger than binary implementations.
Safe	Generates extra control logic to force the state machine to the reset state if an invalid state is reached. The safe value can be used in conjunction with the other three values, which results in the state machine being implemented with the requested encoding scheme and the generation of the reset logic.

Example 8–1 shows sample VHDL code for applying the syn_encoding directive.

Example 8–1. VHDL Code for syn_encoding

```
SIGNAL current_state : STD_LOGIC_VECTOR(7 DOWNTO 0);
ATTRIBUTE syn_encoding : STRING;
ATTRIBUTE syn_encoding OF current_state : SIGNAL IS "sequential";
```

The default is to optimize state machine logic for speed and area, but this is potentially undesirable for critical systems. The safe value generates extra control logic to force the state machine to the reset state if an invalid state is reached.

FSM Explorer in Synplify Pro

The Synplify Pro software can use the FSM Explorer to automatically explore different encoding styles for a state machine, and then implement the best encoding based on the overall design constraints. The FSM Explorer uses the FSM Compiler to identify and extract state machines from a design. However, unlike the FSM Compiler which chooses the encoding style based on the number of states, the FSM Explorer tries several different encoding styles before choosing a specific one. The trade-off is that the compilation requires more time to perform the analysis of the state machine, but finds an optimal encoding scheme for the state machine.

Optimization Attributes & Options

The following sections list other attributes and options that you can modify in the Synplify software to improve your design performance.

Retiming in Synplify Pro

The Synplify Pro software can retime a design, which can improve the timing performance of sequential circuits by moving registers (register balancing) across combinational elements. Be aware that retimed registers incur name changes. To retime your design, turn on the **Retiming** option in the **Device** tab in the **Implementation Options** section, or use the `syn_allow_retiming` attribute.

Maximum Fan-Out

When your design has critical path nets with high fan-outs, you can use the `syn_maxfan` attribute to control the fan-out of the net. Setting this attribute for a specific net results in the replication of the driver of the net to reduce the overall fan-out. The `syn_maxfan` attribute takes an integer value and applies it to inputs or registers. (The `syn_maxfan` attribute cannot be used to duplicate control signals, and the minimum allowed value of the attribute is 4.) Using this attribute may result in increased logic resource utilization, thus putting a strain on routing resources and leading to long compile times and difficult fitting.

If you need to duplicate an output register or output enable register, you can create a register for each output pin by using the `syn_useioff` attribute (refer to "Register Packing").

Preserving Nets

During synthesis, the compiler maintains ports, registers, and instantiated components. However, some nets may not be maintained in order to create an optimized circuit. Applying the `syn_keep` directive overrides the optimization of the compiler and preserves the net during synthesis. The `syn_keep` directive takes a Boolean value and can be applied to wires (Verilog HDL) and signals (VHDL). Setting the value to **true** preserves the net through synthesis.

Register Packing

Altera devices allow for the packing of registers into I/O cells. Altera recommends allowing the Quartus II software to make the I/O register assignments. However, it is possible to control register packing with the `syn_useioff` attribute. The `syn_useioff` attribute takes a Boolean value and can be applied to ports or entire modules. Setting the value to **1** instructs the compiler to pack the register into an I/O cell. Setting the value to **0** prevents register packing in both the Synplify and Quartus II software.

Resource Sharing

The Synplify software uses resource sharing techniques during synthesis by default to reduce area. Turning off the **Resource Sharing** option on the **Options** tab of the **Implementation Options** dialog box can improve performance results for some designs. If you turn off this option, be sure to check the results to determine if it helps the timing performance, and if it does not help, then you should leave it on.

Preserving Hierarchy

The Synplify software performs cross-boundary optimization by default. This results in the flattening of the design to allow optimization. Use the `syn_hier` attribute to over-ride the default compiler settings. The `syn_hier` attribute takes a string value and applies it to modules and/or architectures. Setting the value to **hard** maintains the boundaries of a module and/or architecture, and prevents cross-boundary optimization.

By default, the Synplify software generates a hierarchical VQM file. To flatten the file, set the `syn_netlist_hierarchy` attribute equal to "0".

Register Input & Output Delays

The advanced options called `define_reg_input_delay` and `define_reg_output_delay` can speed up paths feeding a register or coming from a register by a specific number of nanoseconds. The Synplify software attempts to meet the global clock frequency goals for a design as well as the individual clock frequency goals (set with `define_clock`). You can use these attributes to add delay to paths feeding into/out of registers to further constrain critical paths.

These options are useful in closing timing when your design does not meet timing goals because the routing delay after placement and routing exceeds the delay predicted by the Synplify software. Rerun synthesis using this option, specifying the actual routing delay (from place-and-route results) so that the tool can meet the required clock frequency.

In the SCOPE constraint editor, use the registers panel with the following entries:

- Register—Specifies the name of the register. If you have initialized a compiled design, you can choose the name from the list.
- Type—Specifies whether the delay is an input or output delay.
- Route—Shrinks the effective period for the constrained registers by the specified value without affecting the clock period that is forward-annotated to the Quartus II software.

Use the following Tcl command syntax to specify an input or output register delay in nanoseconds.

Example 8–2. Specifying an Input or Output Register Delay Using Tcl Command Syntax

```
define_reg_input_delay {<Register>}  -route <delay in ns>
define_reg_output_delay {<Register>} -route <delay in ns>
```

syn_direct_enable

This attribute controls the assignment of a clock-enable net to the dedicated enable pin of a register. Using this attribute, you can direct the Synplify mapper to use a particular net as the only clock enable when the design has multiple clock enable candidates.

You can also use this attribute as a compiler directive to infer registers with clock enables. To do so, enter the `syn_direct_enable` directive in your source code, not the SCOPE spreadsheet.

The `syn_direct_enable` data type is Boolean. A value of **1** or **true** enables net assignment to the clock-enable pin. The syntax for Verilog HDL is shown below:

```
object /* synthesis syn_direct_enable = 1 */ ;
```

Standard I/O Pad

For certain Altera devices and the equivalent device I/O standard, you can specify the I/O standard type to use for the I/O pad in the design using the **I/O Standard** panel in the Synplify SCOPE editor.

Example 8–3 shows the Synplify SDC syntax for the **define_io_standard** constraint, in which the `delay_type` must be either `input_delay` or `output_delay`.

Example 8–3. Synplify SDC Syntax for the define_io_standard Constraint

```
define_io_standard [-disable|-enable] {<objectName>} -delay_type \
[input_delay|output_delay] <columnTclName>{<value>} \
[<columnTclName>{<value>}...]
```

For details about supported I/O standards, refer to *Altera I/O Standards* in the *Synplify Reference Manual*.

Altera-Specific Attributes

The following attributes are for use with specific Altera device features. These attributes are forward-annotated to the Quartus II project and are used during the place-and-route process.

altera_chip_pin_lc

Use this attribute to make pin assignments. This attribute takes a string value and applies it to inputs and outputs.

This attribute is not supported for any of the MAX series devices. In the SCOPE editor, select the attribute **altera_chip_pin_lc** and set the value to a pin number or a list of pin numbers.

Example 8–4 shows VHDL code for making location assignments to ACEX 1K and FLEX 10KE devices.

The "@" is used to specify pin locations for ACEX 1K and FLEX 10KE devices. For these devices the pin location assignments are written to the output EDIF.

Example 8–4. Making Location Assignments to ACEX 1K & FLEX 10KE Devices, VHDL

```
ENTITY sample (data_in : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
   data_out: OUT STD_LOGIC_VECTOR (3 DOWNTO 0));
ATTRIBUTE altera_chip_pin_lc : STRING;
ATTRIBUTE altera_chip_pin_lc OF data_out : SIGNAL IS "@14, @5,@16, @15";
```

Example 8–5 shows VHDL code for making location assignments for other Altera devices. The pin location assignments for these devices are written to the output Tcl script.

Example 8–5. Making Location Assignments to Other Devices, VHDL

```
ENTITY sample (data_in : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
   data_out: OUT STD_LOGIC_VECTOR (3 DOWNTO 0));
ATTRIBUTE altera_chip_pin_lc : STRING;
ATTRIBUTE altera_chip_pin_lc OF data_out : SIGNAL IS "14, 5, 16,
   15";
```

The `data_out` signal is a 4-bit signal; `data_out[3]` is assigned to pin 14 and `data_out[0]` is assigned to pin 15.

altera_implement_in_esb or altera_implement_in_eab

You can use these attributes to implement logic in either embedded system blocks (ESBs) or embedded array blocks (EABs) rather than in logic resources to improve area utilization. The modules selected for such implementation cannot have feedback paths, and either all or none of the I/Os must be registered. This attribute takes a boolean value and can be applied to instances. (This option is applicable for devices with ESBs/EABs only. For example, the Stratix® family of devices is not supported by this option. This attribute is ignored for designs targeting devices that do not have ESBs or EABs.)

altera_io_powerup

You can use this attribute to define the power-up value of an I/O register that has no set or reset. This attribute takes a string value (**high | low**) and applies it to ports that have I/O registers.

altera_io_opendrain

Use this attribute to specify open-drain mode I/O ports. This attribute takes a boolean value and applies it to outputs or bidirectional ports for devices that support open-drain mode.

Exporting Designs to the Quartus II Software Using NativeLink Integration

The NativeLink feature in the Quartus II software facilitates the seamless transfer of information between the Quartus II software and EDA tools, and allows you to run other EDA design entry or synthesis, simulation, and timing analysis tools automatically from within the Quartus II software. After a design is synthesized in the Synplify software, a VQM (or EDIF) file and Tcl files are used to import the design into the Quartus II software for place-and-route. You can run the Quartus II software from within the Synplify software or as a standalone application. Once you have imported the design into the Quartus II software, you can specify different options to further optimize the design.

When you are using NativeLink integration, the path to your project must not contain white space. The Synplify software uses Tcl scripts to communicate with the Quartus II software, and the Tcl language does not accept arguments with white space in the path.

You can use NativeLink integration to integrate the Synplify software and Quartus II software with a single GUI for both the synthesis and place-and-route operations. NativeLink integration allows you to run the Quartus II software from within the Synplify software GUI or to run the Synplify software from within the Quartus II software GUI.

Running the Quartus II Software from within the Synplify Software

To use the Quartus II software from within the Synplify software, you must first verify that the `QUARTUS_ROOTDIR` environment variable contains the Quartus II software installation directory. This environment variable is required to use the Synplify and Quartus II software together.

Under each Implementation in the Synplify software, you can create a place-and-route implementation called **pr**_<*number*> **(Altera Place & Route)**. You can create new place and route implementations using the **New P&R** button in the GUI. To run the Quartus II software in command-line mode after each synthesis run, use the text box to turn on the place-and-route implementation. The results of the place and route are written to a log file in the **pr**_<*number*> directory under the current implementation directory.

You can also use the commands in the Quartus II menu to run the Quartus II software at any time following a successful completion of synthesis. Use one of the following commands from the **Quartus II** submenu under the Options menu in the Synplify software:

- **Launch Quartus**—Opens the Quartus II software GUI and creates a Quartus II project with the synthesized output file, forward-annotated timing constraints, and pin assignments. You can use this to configure options for the project and execute any Quartus II commands.
- **Run Background Compile**—Runs the Quartus II software in command-line mode with the project settings from the synthesis run. The results of the place-and-route are written to a log file.

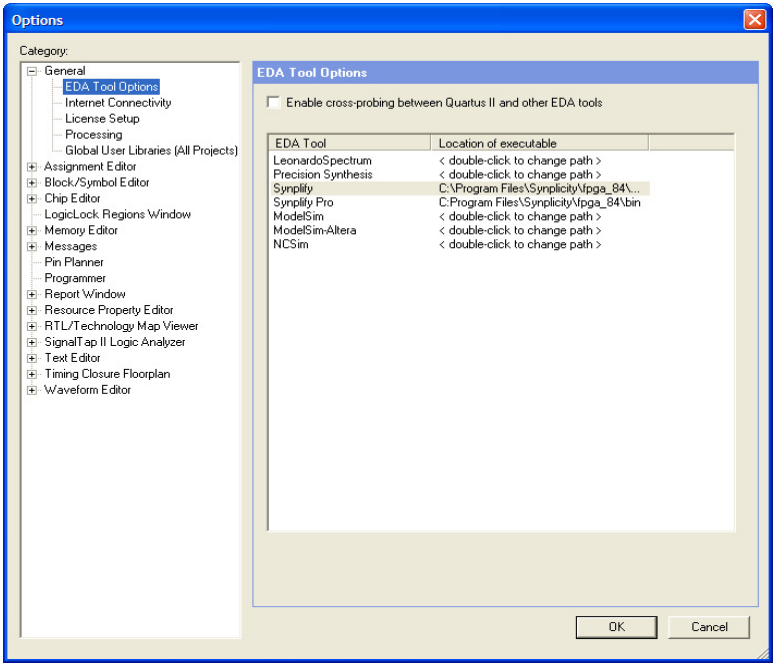
The <*project_name*>**_cons.tcl** file is used to set up the Quartus II project and calls the <*project_name*>**.tcl** file to pass constraints from the Synplify software to the Quartus II software. The <*project_name*>**.tcl** file contains device, timing, and location assignments.

Using the Quartus II Software to Launch the Synplify Software

You can set up the Quartus II software to run the Synplify software for synthesis using NativeLink integration. This feature allows you to use the Synplify software to synthesize a design as part of a normal compilation in the Quartus II software.

To set up Synplify in Quartus II, on the Tools menu, click **Options**. In the **Options** window, click **EDA Tool Options** and specify the path of Synplify software, as shown in Figure 8–2.

Figure 8–2. Specifying the Path to the Synplify Software



For detailed information about using NativeLink integration with the Synplify software, refer to the Quartus II Help.

Running the Synplify software with NativeLink integration requires a floating network license (as opposed to a node-locked single-PC license), because batch mode compilation is supported only with floating licenses.

Running the Quartus II Software Manually Using the Synplify-Generated Tcl Script

You can also use the Quartus II software separately from the Synplify software. To run the Tcl script generated by the Synplify software to set up your project, perform the following steps:

1. Ensure the VQM and Tcl files are located in the same directory (they should both be located in the implementation directory by default).

2. In the Quartus II software, on the View menu, point to **Utility Windows** and click **Tcl Console**. The Quartus II Tcl Console opens.

3. At the Tcl Console command prompt, type:

```
source <path>/<project name>_cons.tcl ↵
```

Passing Constraints to the Quartus II Software

This section describes how Synplify constraints are converted to the equivalent Quartus II assignments and are forward-annotated to the Quartus II software with Tcl commands.

Default or Global Clock Frequency

Use the following Synplify command to set the Synplify default or global clock frequency that applies to the entire project:

```
set_option -frequency <frequency>
```

The <*frequency*> is specified in MHz. If a global frequency is not specified, the software uses the default global clock frequency of 1 MHz.

The `set_option` Synplify constraint is passed to the Quartus II software with the following command:

```
set_global_assignment -name FMAX_REQUIREMENT
<frequency> MHz
```

If a frequency is not specified in the Quartus II software, the software uses the default global clock frequency of 1 GHz.

Individual Clocks & Frequencies

You can specify clock frequencies for individual clocks with the following Synplify commands:

Example 8–6. Specifying Clock Frequencies for Individual Clocks

```
define_clock -name {<clock_name>} -freq <frequency> -clockgroup <clock_group>
-rise <rise_time> -fall <fall_time>
define_clock -name {<clock_name>} -period <period> -clockgroup <clock_group>
-rise <rise_time> -fall <fall_time>
```

Table 8–3 shows the command arguments.

Table 8–3. Command Arguments

Argument	Description
`-name`	The <*clock_name*> specifies a design port name or a register output signal name, and, after synthesis, corresponds to a <*mapped_clock_name*>.
`-freq` *(1)*	The <*frequency*> is specified in MHz.
`-period` *(2)*	The <*period*> is specified in ns.
`-clockgroup`	If the <*clock_group*> is not specified, it defaults to `default_clkgroup`. Synplify assumes all clocks belonging to the same clock group are related. If you do not specify a clock group, the clock belongs to the default clock group. Therefore, if you do not specify any clock groups, all the clocks are considered related by default in the software.
`-rise` `-fall`	The <*rise_time*> and <*fall_time*> specify a non-default duty cycle. By default, the Synplify synthesis tool assumes that the clock is a 50% duty cycle clock, with the rising edge at 0 and the falling edge at period/2. If you have another duty clock cycle, you can specify the appropriate **Rise At** and **Fall At** values.

Notes to Table 8–3:

(1) When the <*frequency*> is specified, the Synplify software uses <*fall_time*> and <*frequency*> to calculate the `duty_cycle` with the following formula: `duty_cycle` = (<*fall_time*> – <*rise_time*>) × <*frequency*> ÷ 10.

(2) When the <*period*> is specified, the Synplify software uses <*fall_time*> and <*period*> to calculate the `duty_cycle` with the following formula: `duty_cycle` = 100 × (<*fall_time*> – <*rise_time*>) ÷ <*period*>.

The equivalent Quartus II commands depend on how the clock groups are defined. In the Quartus II software, clocks that belong to the same or related clock settings are considered related clocks. Clocks assigned to unrelated clock settings are unrelated clocks. There is a one-to-one correspondence between each Quartus II clock setting and a Synplify clock group.

The following sections describe only the frequency constraints. You can use the corresponding constraints for period.

Virtual Clocks

The Quartus II software supports virtual clocks. If you use the virtual clock setting in Synplify, the setting is mapped to a constraint in the Quartus II software.

Route Delay Option

The `-route` option in Synplify clock constraints is designed for use for synthesis only if you do not meet timing goals because the routing delay after placement and routing exceeds the delay predicted by the Synplify software. This constraint does not have to be forward annotated to the Quartus II software.

Global Signals

The Synplify software automatically promotes clock signals to global routing lines and passes **Global Signal** assignments to the Quartus II software. The assignments ensure that the same global routing constraints are applied during placement and routing.

Note that the signals promoted to global routing can be different than the ones that the Quartus II software promotes to global routing by default. Synplify promotes only clock signals and not other control signals such as reset or enable. By default, without constraints from the Synplify software, the Quartus II software promotes control signals to global routing if they have high fan-out.

Multiple Clocks in Different Clock Groups

You can specify clock frequencies for multiple clocks with the Synplify commands shown in Example 8–7.

Example 8–7. Specifying Clock Frequencies for Multiple Clocks

```
define_clock -name {<clock_name1>} -freq <frequency1> \
-clockgroup <clock_group1> -rise <rise_time1> -fall <fall_time1>

define_clock -name {<clock_name2>} -freq <frequency2> \
-clockgroup <clock_group2> -rise <rise_time2> -fall <fall_time2>
```

<clock_group1> and *<clock_group2>* are unique names defined in the Synplify software for base clock settings in the Quartus II software.

If the clock <*rise_time*> is zero ("0"), multiple separate clocks are passed to the Quartus II software with the commands shown in Example 8–8:

Example 8–8. Quartus II Assignments for Multiple Clocks if the Clock Rise Time is Zero

```
create_base_clock -fmax <frequency1>MHz -duty_cycle <duty_cycle1> \
-target mapped_clock_name1 <base_clock_setting1>

create_base_clock -fmax <frequency2>MHz -duty_cycle <duty_cycle2> \
-target mapped_clock_name2 <base_clock_setting2>
```

If the clock <*rise_time*> is non-zero, multiple separate clocks are passed to the Quartus II software with the following commands shown in Example 8–9:

Example 8–9. Quartus II Assignments for Multiple Clocks if the Clock Rise Time is Not Zero

```
create_base_clock -fmax <frequency1>MHz -duty_cycle <duty cycle1> \
-no_target <base clock setting1>

create_base_clock -fmax <frequency2>MHz -duty_cycle <duty cycle2> \
-no_target <base clock setting2>

create_relative_clock -base_clock <base clock setting1> -offset <rise time1>ns \
-duty_cycle <duty cycle1> -multiply <multiply by> -divide <divide by> \
-target <mapped clock name1> <derived clock setting1>

create_relative_clock -base_clock <base clock setting2> -offset <rise time2>ns \
-duty_cycle <duty cycle2> -multiply <multiply by> -divide <divide by> \
-target <mapped clock name2> <derived clock_setting2>
```

Multiple Clocks with Different Frequencies in the Same Clock Group

You can specify multiple clocks with relative clock settings in the same clock group in Synplify with different frequencies with the commands shown in Example 8–10:

Example 8–10. Specifying Multiple Clocks with Different Frequencies in the Same Clock Group

```
define_clock -name {<clock_name1>} -freq <frequency1> -clockgroup <clock_group1> \
-rise <rise_time1> -fall <fall_time1>

define_clock -name {<clock_name2>} -freq <frequency2> -clockgroup <clock_group1> \
-rise <rise_time2> -fall <fall_time2>
```

When you specify clocks with different frequencies in the same clock group, the software calculates the <*multiply_by*> and the <*divide_by*> factors for relative clock settings from <*frequency1*> and <*frequency2*> in the clock group settings.

If the clock <*rise_time*> is zero ("0"), multiple clocks with relative clock settings in the same clock group with different frequencies are passed to the Quartus II software with the commands shown in Example 8–11:

Example 8–11. Quartus II Assignments for Multiple Clocks with Different Frequencies in the Same Clock Group, if the Clock Rise Time is Zero

```
create_base_clock -fmax <frequency1>MHz -duty_cycle <duty_cycle1> \
-target <mapped_clock_name1> <base_clock_setting1>

create_relative_clock -base_clock <base_clock_setting1> \
-duty_cycle <duty_cycle2> -multiply <multiply_by> -divide <divide_by> \
-target <mapped_clock_name2> <derived_clock_setting2>
```

Inter-Clock Relationships—Delays & False Paths between Clocks

You can set a clock-to-clock delay constraint in Synplify with the commands in Example 8–12.

Example 8–12. Specifying Clock-to-Clock Delay Constraints

```
define_clock_delay -fall <clock_name1> -rise <clock_name2> <delay_value>
define_clock_delay -rise <clock_name1> -fall <clock_name2> <delay_value>
define_clock_delay -rise <clock_name1> -rise <clock_name2> <delay_value>
define_clock_delay -fall <clock_name1> -fall <clock_name2> <delay_value>
```

If <*delay_value*> is set to `false`, these constraints in Synplify indicate a false path between the two clocks. If all four rise/fall clock-edge pairs are specified in the Synplify software, the Synplify constraints are mapped to the following constraint in the Quartus II software:

```
set_timing_cut_assignment -from <clock_name1> \
-to <clock_name2>
```

If all four clock-edge pairs are not specified in Synplify, the constraint cannot be mapped to a constraint in the Quartus II software.

If <*delay_value*> is set to a value other than `false`, these constraints in Synplify is not mapped to a constraint in the Quartus II software. The Quartus II software does not support clock-edge to clock-edge delay constraints.

False Paths

You can specify the false path constraint in Synplify with the command shown below.

```
define_false_path -from <sig_name1> -to <sig_name2>
```

The signals <*sig_name1*> and <*sig_name1*> can be design port names or register instance names.

The **define_false_path** constraint in Synplify is mapped to the constraint in the Quartus II software, as shown below.

```
set_timing_cut_assignment -from <sig_name1> \
-to <sig_name2>
```

Synplify can identify pairs of signal sets such that every member of the cross-product of these two sets is a valid false path constraint. Signal groups can be defined in the Quartus II software with the commands shown below.

```
timegroup -add_member sig_name1_i <sig_group1>
```
(for every signal in <*sig_group1*>)

```
timegroup -add_member sig_name2_i <sig_group2>
```
(for every signal in <*sig_group2*>)

```
set_timing_cut_assignment -from <sig_group1> \
-to <sig_group2>
```

If the signals <*sig_name1*> or <*sig_name2*> represent multiple signals such as a wildcard, group, or bus, the constraints you can expand appropriately for representation in the Quartus II software. The Quartus II software supports wildcard signal names, and signal groups for timing assignments. The Quartus II software does not support bus notation, such as **A[7:4]**.

False Path from a Signal

You can specify a false path constraint from a signal in Synplify with the following command:

```
define_false_path -from <sig_name>
```

The Quartus II software does not support "from-only" path specifications. You must also include a "to-path" specification. However, you can specify a wildcard for the `-to` signal. This constraint in Synplify is mapped to the following constraint in the Quartus II software:

```
set_timing_cut_assignment -from <sig_name> -to {*}
```

False Path to a Signal
You can specify a false path constraint to a signal in Synplify with the following command:

```
define_false_path -to <sig_name>
```

The Quartus II software does not support **to-only** path specifications. You must include a **from-path** specification." However, you can specify a wildcard for the `-from` signal. This constraint in Synplify is mapped to the following constraint in the Quartus II software:

```
set_timing_cut_assignment -from {*} -to <sig_name>
```

False Path Through a Signal
You can specify a false path constraint through a signal in Synplify with the following command:

```
define_false_path -from <sig_name1> -to <sig_name2> \
-through <sig_name3>
```

The Quartus II software does not currently support false paths with a "through path" specification. Any constraint in Synplify with a `-through` specification is not mapped to a constraint in the Quartus II software.

Multicycle Paths

You can specify a multicycle path constraint in Synplify with the following command:

```
define_multicycle_path -from <sig_name1> \
-to <sig_name2> <clock_cycles>
```

This constraint in Synplify is mapped to the following constraint in the Quartus II software:

```
set_multicycle_assignment -from <sig_name1> \
-to <sig_name2> <clock_cycles>
```

If the signals <*sig_name1*> or <*sig_name2*> represent multiple signals such as a wildcard, group, or bus, the constraints can be appropriately expanded for representation in the Quartus II software as described in "False Paths" on page 8–9.

<*clock_cycles*> is the number of clock cycles for the multicycle path.

Multicycle Path from a Signal
You can specify a multicycle path constraint from a signal in Synplify with the following command:

```
define_multicycle_path -from <sig_name> <clock_cycles>
```

This constraint is mapped using a wildcard for the `-to` value in the Quartus II software, similar to the false path constraints:

```
set_multicycle_assignment -from <sig_name> \
-to {*} <clock_cycles>
```

Multicycle Path to a Signal
You can specify a multicycle path constraint to a signal in Synplify with the following command:

```
define_multicycle_path -to <sig_name> <clock_cycles>
```

This constraint is mapped using a wildcard for the `-from` value in the Quartus II software, similar to the false path constraints:

```
set_multicycle_assignment -from {*} <sig_name> \
<clock_cycles>
```

Multicycle Path Through a Signal
You can specify a multicycle path constraint through a signal in Synplify using the following command:

```
define_multicycle_path -from <sig_name1> -to <sig_name2> \
-through <sig_name3> <clock_cycles>
```

The Quartus II software does not currently support multicycle paths with a **through path** specification. Any constraint in Synplify with a `-through` specification is not mapped to a constraint in the Quartus II software.

Maximum Path Delays

You can specify the maximum path delay relationships between signals in Synplify with the following command:

```
define_path_delay -from <sig_name1> -to <sig_name2> \
-max <delay_value>
```

This constraint in Synplify is mapped to the following constraint in the Quartus II software:

```
set_instance_assignment -from <sig_name1> \
-to <sig_name2> -name SETUP_RELATIONSHIP <delay_value>ns
```

The Quartus II software does not support signal groups or bus notation, and supports only register names for this constraint.

Maximum Path Delay from a Signal
You can specify the maximum path delay constraint from a signal in Synplify with the following command:

```
define_path_delay -from <sig_name> -max <delay_value>
```

This constraint is mapped using a wildcard for the `-to` value in the Quartus II software, similar to false path constraints:

```
set_instance_assignment -from <sig_name> -to {*} \
-name SETUP_RELATIONSHIP <delay_value>ns
```

Maximum Path Delay to a Signal
You can specify the maximum path delay constraint to a signal in Synplify with the following command:

```
define_path_delay -to <sig_name> -max <delay_value>
```

This constraint is mapped using a wildcard for the `-from` value in the Quartus II software, similar to the false path constraints.

```
set_instance_assignment -from {*}<sig_name> \
-to <sig_name> -name SETUP_RELATIONSHIP <delay_value>ns
```

Maximum Path Delay through a Signal
You can specify the maximum path delay constraint through a signal in Synplify with the following command:

```
define_path_delay -from <sig_name1> -to <sig_name2> \
-through <sig_name3> -max <delay_value>
```

The Quartus II software does not currently support maximum path delay constraints with a "through path" specification. Any constraint in Synplify with a `-through` specification is not mapped to a constraint in the Quartus II software.

Register Input & Output Delays
These register input delay and register output delay constraints in Synplify are for use in synthesis only, and therefore are not forward-annotated to the Quartus II software.

Default External Input Delay
You can specify the default input delay constraint in Synplify with the following command:

```
define_input_delay -default <delay_value>
```

This constraint is mapped to the following constraint in the Quartus II software:

```
set_input_delay -clock {*} <delay_value> {*}
```

Port-Specific External Input Delay
You can specify a port-specific input delay constraint in Synplify with the following command:

```
define_input_delay <input_port_name> <delay_value> \
-ref <clock_name>:<clock_edge>
```

The <*clock_edge*> can be set to `r` (rising edge) or `f` (falling edge).

When the clock edge is `r` (rising edge), this constraint is mapped to the following constraint in the Quartus II software:

```
set_input_delay -clock <clock_name> <delay_value> \
<input_port_name>
```

When the clock_edge is `f` (falling edge), this constraint is not mapped to a constraint in the Quartus II software. The Quartus II software does not support the specification of input delays with respect to the falling edge of the clock.

Default External Output Delay
You can specify the default output delay constraint in Synplify with the following command:

```
define_output_delay -default <delay_value>
```

This constraint is mapped to the following constraint in the Quartus II software:

```
set_output_delay -clock {*} <delay_value> {*}
```

Port-Specific External Output Delay
You can specify a port-specific input delay constraint in Synplify with the following command:

```
define_output_delay <output_port_name> <delay_value> \
-ref <clock_name>:<clock_edge>
```

The <*clock_edge*> can be set to `r` (rising edge) or `f` (falling edge). When the clock edge is `r` (rising edge), this constraint is mapped to the following constraint in the Quartus II software:

```
set_output_delay -clock <clock_name> <delay_value> \
<output_port_name>
```

When the clock_edge is `f` (falling edge), this constraint is not mapped to a constraint in the Quartus II software. The Quartus II software does not support the specification of output delays with respect to the falling edge of the clock.

Guidelines for Altera Megafunctions & Architecture-Specific Features

Altera provides parameterizable megafunctions including the LPMs, device-specific Altera megafunctions, intellectual property (IP) available as Altera MegaCore® functions, and IP available through the Altera Megafunction Partners Program (AMPP℠). You can use megafunctions by instantiating them in your HDL code or inferring them from generic HDL code.

If you want to instantiate a megafunction in your HDL code, you can do so by using the MegaWizard Plug-In Manager to parameterize the function or instantiating the function using the port and parameter definition. The MegaWizard Plug-In Manager provides a graphical interface within the Quartus II software for customizing and parameterizing any available megafunction for the design. "Instantiating Altera Megafunctions Using the MegaWizard Plug-In Manager" on page 8–30 describes the MegaWizard Plug-In Manager flow with the Synplify software.

For more information about specific Altera megafunctions, refer to the Quartus II Help. For more information about IP functions, refer to the appropriate IP documentation.

The Synplify software also automatically recognizes certain types of HDL code and infers the appropriate megafunction when a megafunction provides optimal results. The Synplify software provides options to control inference of certain types of megafunctions, as described in "Inferring Altera Megafunctions from HDL Code" on page 8–35.

For a detailed discussion about instantiating versus inferring megafunctions, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*. The *Recommended HDL Coding Styles* chapter also provides details on using the MegaWizard Plug-In Manager in the Quartus II software and explains the files generated by the wizard, as well as providing coding style recommendations and HDL examples for inferring megafunctions in Altera devices.

Instantiating Altera Megafunctions Using the MegaWizard Plug-In Manager

When you use the MegaWizard Plug-In Manager to set up and parameterize a megafunction, the MegaWizard Plug-In Manager creates a VHDL or Verilog HDL wrapper file that instantiates the megafunction (a black box methodology). Some megafunctions also support the generation of a fully synthesizeable netlist for improved results with EDA synthesis tools such as Synplify (a clear box methodology). Clear- and black-box methodologies are described in the following sections.

Clear Box Methodology

You can use the MegaWizard Plug-In Manager to generate a fully synthesizeable netlist. This flow is referred to as a clear box methodology because the Synplify software can "see" into the megafunction file. The clear box feature enables the synthesis tool to report more accurate timing estimates and resource utilization, and to take better advantage of timing driven optimization than a black box methodology.

For certain megafunctions, the clear box feature is enabled by turning the **Generate clear box netlist file instead of a default wrapper file (for use with supported EDA synthesis tools only)** option on in the MegaWizard Plug-In Manager. If the option does not appear, then clear box models are not supported for the selected megafunction. The Synplify software supports clear box models for Stratix and Cyclone™ devices. Turning this option on causes the Quartus II MegaWizard Plug-In Manager to generate a synthesizeable clear box netlist instead of the megafunction wrapper file described in "Black Box Methodology" on page 8–31.

Using MegaWizard Plug-In Manager-Generated Verilog HDL Files for Clear Box Megafunction Instantiation

If you turn on the <*output file*>**_inst.v** option on the last page of the wizard, the MegaWizard Plug-In Manager generates a Verilog HDL instantiation template file for use in your Synplify design. This file can help you instantiate the megafunction clear box netlist file, <*output file*>**.v**, in your top-level design. Include the megafunction clear-box netlist file in your Synplify Project. Also include the **stratix.v** library file from the

lib/altera directory of the Synplify installation directory; this file provides the port and parameter definitions of the clear box primitives. Finally, include the megafunction clear box netlist file, <*output file*>**.v**, along with your Synplify-generated VQM netlist in your Quartus II project.

The Synplify software reads the clear box description for the `alt_pll` megafunction and writes the netlist for the phase-locked loop (PLL) into the resulting VQM output netlist. Therefore, for `alt_pll` instantiations, do not include the megafunction clear box netlist file <*output file*>**.v** in your Quartus II project. Reading the PLL function allows the Synplify software to interpret the multiplication and division factors in the PLL instantiation to make the correct timing assignment.

Using MegaWizard Plug-In Manager-Generated VHDL Files for Clear Box Megafunction Instantiation

If you check the <*output file*>**.cmp** and <*output file*>**_inst.vhd** options on the last page of the wizard, the MegaWizard Plug-In Manager generates a VHDL Component declaration file and a VHDL Instantiation template file for use in your design. These files help to instantiate the megafunction clear box netlist file, <*output file*>**.vhd**, in your top-level design. Include the megafunction clear box netlist file in your Synplify Project. Finally, include the megafunction clear box netlist file, <*output file*>**.vhd**, along with your Synplify-generated VQM netlist in your Quartus II project.

The Synplify software reads the clear box description for the `alt_pll` megafunction and writes the netlist for the PLL into the resulting VQM output netlist. Therefore, for `alt_pll` instantiations, do not include the megafunction clear box netlist file <*output file*>**.vhd** in your Quartus II project. Reading the PLL function allows the Synplify software to interpret the multiplication and division factors in the PLL instantiation to make the correct timing assignment.

Black Box Methodology

Using the MegaWizard Plug-In Manager-generated wrapper file is referred to as a black-box methodology because the megafunction is treated as a black box in the Synplify software. The black box wrapper file is generated by default in the MegaWizard Plug-In Manager and is available for all megafunctions.

The black box methodology does not allow the synthesis tool any visibility into the function module and therefore does not take full advantage of the synthesis tool's timing driven optimization. For better timing optimization, especially if the black box does not have registered

inputs and outputs, add timing models to black boxes. Refer to "Other Synplify Software Attributes for Creating Black Boxes" on page 8–34 for details.

Using MegaWizard Plug-In Manager-Generated Verilog HDL Files for Black Box Megafunction Instantiation

If you check the <*output file*>**_inst.v** and <*output file*>**_bb.v** options on the last page of the wizard, the MegaWizard Plug-In Manager generates a Verilog HDL instantiation template file and a hollow-body black-box module declaration for use in your Synplify design. The instantiation template file helps to instantiate the megafunction variation wrapper file, <*output file*>**.v**, in your top-level design. Do not include the megafunction variation wrapper file in your Synplify Project, but add it, with your Synplify-generated VQM netlist, to your Quartus II project. Add the hollow-body black-box module declaration <*output file*>**_bb.v** to your Synplify Project to describe the port connections of the black box.

You can use the `syn_black_box` compiler directive to declare a module as a black box. The top-level design files must contain the megafunction port mapping and hollow-body module declaration, as described above. You can apply the `syn_black_box` directive to the module declaration in the top-level file or a separate file included in the project (such as the <*output file*>**_bb.v** file) to instruct the Synplify software that this is a black box. The software compiles successfully without this directive, but reports an additional warning message. Using this directive allows you to add other directives as discussed in "Other Synplify Software Attributes for Creating Black Boxes" on page 8–34.

Example 8–13 shows a sample top-level file that instantiates **verilogCount.v**, which is a customized variation of the `lpm_counter` generated by the MegaWizard Plug-In Manager.

Example 8–13. Top-Level Verilog HDL Code with Black Box Instantiation of lpm_counter

```
module topCounter (clk, count);
    input clk;
    output[7:0]  count;
    verilogCounter verilogCounter_inst (
        .clock ( clk ),
        .q ( count )
);
endmodule
// Module declaration found in verilogCounter_bb.v
// The following attribute is added to create a
// black box for this module.
module verilogCounter (
    clock,
    q) /* synthesis syn_black_box */;
    input clock;
    output[7:0]  q;
endmodule
```

Using MegaWizard Plug-In Manager-Generated VHDL Files for Black Box Megafunction Instantiation

If you check the <*output file*>**.cmp** and <*output file*>**_inst.vhd** options on the last page of the wizard, the MegaWizard Plug-In Manager generates a VHDL component declaration file and a VHDL instantiation template file for use in your Synplify design. These files can help you instantiate the megafunction variation wrapper file, <*output file*>**.vhd**, in your top-level design. Do not include the megafunction variation wrapper file in your Synplify Project, but add it, along with your Synplify-generated VQM netlist, to your Quartus II project.

You can use the `syn_black_box` compiler directive to declare a component as a black box. The top-level design files must contain the megafunction variation component declaration and port mapping, as described above. Apply the `syn_black_box` directive to the component declaration in the top-level file. The software compiles successfully without this directive, but reports an additional warning message. Using this directive allows you to add other directives such as the ones in the "Other Synplify Software Attributes for Creating Black Boxes" section.

Example 8–14 shows a sample top-level file that instantiates **vhdlCount.vhd**, which is a customized variation of the lpm_counter generated by the MegaWizard Plug-In Manager.

Example 8–14. Top-level VHDL Code with Black Box Instantiation of lpm_counter

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY testCounter IS
    PORT
    (
        clk: IN STD_LOGIC ;
        count: OUT STD_LOGIC_VECTOR (7 DOWNTO 0)
    );
    END testCounter;
ARCHITECTURE top OF testCounter IS
component vhdlCount
    PORT (
        clock: IN STD_LOGIC ;
        q: OUT STD_LOGIC_VECTOR (7 DOWNTO 0)
    );
end component;
attribute syn_black_box : boolean;
attribute syn_black_box of vhdlCount: component is true;
BEGIN
    vhdlCount_inst : vhdlCount PORT MAP (
        clock => clk,
        q => count
    );
END top;
```

Other Synplify Software Attributes for Creating Black Boxes

The black box methodology does not allow the synthesis tool any visibility into the function module. Thus, it does not take full advantage of the synthesis tool's timing-driven optimization. For better timing optimization, especially if the black box does not have registered inputs and outputs, add timing models to black boxes. This can be done with a "gray box" methodology by adding the `syn_tpd`, `syn_tsu`, and `syn_tco` attributes. Refer to Example 8–15 for a Verilog HDL example.

Example 8–15. Verilog HDL Example

```
module ram32x4(z,d,addr,we,clk);
/* synthesis syn_black_box syn_tco1="clk->z[3:0]=4.0"
    syn_tpd1="addr[3:0]->z[3:0]=8.0"
    syn_tsu1="addr[3:0]->clk=2.0"
    syn_tsu2="we->clk=3.0" */
output[3:0]z;
input[3:0]d;
input[3:0]addr;
input we
input clk
endmodule
```

The following additional attributes are supported by the Synplify software to communicate details about the characteristics of the black box module within the HDL code:

- `syn_resources`—Specifies the resources used in a particular black box
- `black_box_pad_pin`—Prevents mapping to I/O cells
- `black_box_tri_pin`—Indicates a tri-stated signal

For more information about applying these attributes, refer to the *Tasks & Tips* chapter of the *Synplify User Guide*.

Inferring Altera Megafunctions from HDL Code

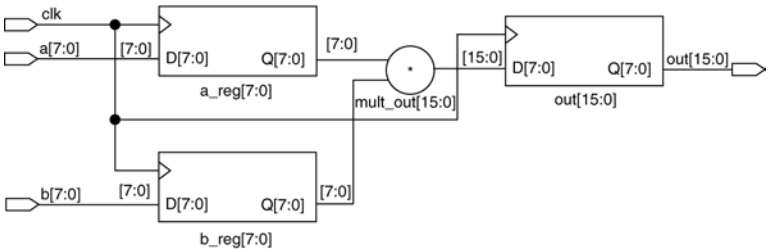
The Synplify software uses Behavior Extraction Synthesis Technology (BEST) algorithms to infer high-level structures such as RAMs, ROMs, operators, FSMs, and so forth. It then keeps the structures abstract for as long as possible in the synthesis process. This allows the use of technology-specific resources to implement these structures by inferring the appropriate Altera megafunction when a megafunction provides optimal results. The following sections outline some of the Synplify-specific details when inferring Altera megafunctions. The Synplify software provides options to control inference of certain types of megafunctions, which is also described in the following sections.

For coding style recommendations and examples for inferring megafunctions in Altera devices, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

Inferring Multipliers

Figure 8–3 shows the RTL view of an unsigned 8×8 multiplier with two pipeline stages after synthesis as seen in HDL Analyst in the Synplify software. This multiplier is converted into an `lpm_mult` megafunction. For devices with DSP blocks, the software may implement the `lpm_mult` function in a DSP block instead of logic elements (LEs), depending on device utilization.

Figure 8–3. HDL Analyst View of lpm_mult Megafunction (Unsigned 8×8 Multiplier with Pipeline=2)



Resource Balancing

While mapping multipliers to DSP blocks, the Synplify software performs resource balancing for optimum performance.

Altera devices have a fixed number of DSP blocks, which include a fixed number of embedded multipliers. If the design uses more multipliers than are available, the Synplify software automatically maps the extra multipliers to logic (logic elements (LEs), or adaptive logic modules (ALMs)).

If a design uses more multipliers than are available in the DSP blocks, the Synplify software maps the multipliers in the critical paths to DSP blocks. Next, any wide multipliers, which may or may not be in the critical paths, are mapped to DSP blocks. Smaller multipliers and multipliers that are not in the critical paths may then be implemented in logic (LEs or ALMs). This ensures that the design fits successfully in the device.

Controlling the Inferring of DSP Blocks

Multipliers can be implemented in DSP blocks or in logic in Altera devices that contain DSP blocks. You can control this implementation through attribute settings in the Synplify software.

Signal Level Attribute

You can control the implementation of individual multipliers by using the `syn_multstyle` attribute as shown below:

```
<signal_name> /* synthesis syn_multstyle = "logic" */
```

where *signal_name* is the name of the signal.

This setting applies to wires only; it cannot be applied to registers.

Table 8–4 shows the values for the signal level attribute in the Synplify software that controls the implementation of the multipliers in the DSP blocks or LEs.

Table 8–4. Attribute Settings for DSP Block in the Synplify Software

Attribute Name	Value	Description
syn_multstyle	lpm_mult	LPM Function inferred and multipliers implemented in DSP block
syn_multstyle	logic	LPM function not inferred and multipliers implemented LEs by the Synplify software

The following examples show simple Verilog HDL and VHDL code using the syn_multstyle attribute.

Example 8–16. Signal Attributes for Controlling DSP Block Inference in Verilog HDL Code

```
module mult(a,b,c,r,en);

input [7:0] a,b;
output [15:0] r;
input [15:0] c;
input en;
wire [15:0] temp /* synthesis syn_multstyle="logic" */;

assign temp = a*b;
assign r = en ? temp : c;
endmodule
```

Example 8–17. Signal Attributes for Controlling DSP Block Inference in VHDL Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity onereg is port (
    r  : out std_logic_vector(15 downto 0);
    en : in std_logic;
    a  : in std_logic_vector(7 downto 0);
    b  : in std_logic_vector(7 downto 0);
    c  : in std_logic_vector(15 downto 0)
    );
end onereg;

architecture beh of onereg is
signal temp : std_logic_vector(15 downto 0);
attribute syn_multstyle : string;
attribute syn_multstyle of temp : signal is "logic";

begin
temp <= a * b;
    r <= temp when en='1' else c;
end beh;
```

Inferring RAM

Follow the guidelines below for the Synplify software to successfully infer RAM in a design:

- The address line must be at least 2 bits wide.
- Resets on the memory are not supported. Refer to the device family documentation for information about whether read and write ports must be synchronous.
- Some Verilog HDL statements with blocking assignments may not be mapped to RAM blocks, so avoid blocking statements when modeling RAMs in Verilog HDL.

For certain device families, the `syn_ramstyle` attribute specifies the implementation to use for an inferred RAM. You can apply `syn_ramstyle` globally, to a module, or to a RAM instance, to specify `registers` or `block_ram` values. To turn off RAM inference, set the attribute value to `registers`.

When inferring RAM for certain Altera device families, the Synplify software generates additional bypass logic. This logic is generated to resolve a half-cycle read/write behavior difference between the RTL and post-synthesis simulations. The RTL simulation shows the memory being updated on the positive edge of the clock, and the post-synthesis

simulation shows the memory being updated on the negative edge. To eliminate the bypass logic, the output of the RAM must be registered. By adding this register, the output of the RAM is seen after a full clock cycle, by which time the update has occurred; thus, eliminating the need for the bypass logic.

For Stratix II, Stratix, Cyclone II, and Cyclone series devices, you can disable the creation of glue logic by setting the `syn_ramstyle` value to `no_rw_check`. Use `syn_ramstyle` with a value of `no_rw_check` to disable the creation of glue logic in dual-port mode.

Example 8–18 shows sample VHDL code for inferring dual-port RAM.

Example 8–18. VHDL Code for Inferred Dual-Port RAM

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_signed.all;

ENTITY dualport_ram IS
PORT ( data_out: OUT STD_LOGIC_VECTOR (7 DOWNTO 0);
    data_in: IN STD_LOGIC_VECTOR (7 DOWNTO 0);
    wr_addr, rd_addr: IN STD_LOGIC_VECTOR (6 DOWNTO 0);
    we: IN STD_LOGIC;
    clk: IN STD_LOGIC);
END dualport_ram;

ARCHITECTURE ram_infer OF dualport_ram IS
TYPE Mem_Type IS ARRAY (127 DOWNTO 0) OF STD_LOGIC_VECTOR (7 DOWNTO 0);
SIGNAL mem: Mem_Type;
SIGNAL addr_reg: STD_LOGIC_VECTOR (6 DOWNTO 0);

BEGIN
    data_out <= mem (CONV_INTEGER(rd_addr));
    PROCESS (clk, we, data_in) BEGIN
        IF (clk='1' AND clk'EVENT) THEN
            IF (we='1') THEN
            mem(CONV_INTEGER(wr_addr)) <= data_in;
            END IF;
        END IF;
    END PROCESS;
END ram_infer;
```

Example 8–19 shows an example of the VHDL code preventing bypass logic for inferring dual-port RAM. The extra latency behavior stems from the inferring methodology and is not required when instantiating a megafunction.

Example 8–19. VHDL Code for Inferred Dual-Port RAM Preventing Bypass Logic

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_signed.all;

ENTITY dualport_ram IS
PORT ( data_out: OUT STD_LOGIC_VECTOR (7 DOWNTO 0);
    data_in : IN STD_LOGIC_VECTOR (7 DOWNTO 0);
    wr_addr, rd_addr : IN STD_LOGIC_VECTOR (6 DOWNTO 0);
    we : IN STD_LOGIC;
    clk : IN STD_LOGIC);
END dualport_ram;

ARCHITECTURE ram_infer OF dualport_ram IS
TYPE Mem_Type IS ARRAY (127 DOWNTO 0) OF STD_LOGIC_VECTOR (7 DOWNTO 0);
SIGNAL mem : Mem_Type;
SIGNAL addr_reg : STD_LOGIC_VECTOR (6 DOWNTO 0);
SIGNAL tmp_out : STD_LOGIC_VECTOR(7 DOWNTO 0); --output register

BEGIN
    tmp_out <= mem (CONV_INTEGER(rd_addr));
    PROCESS (clk, we, data_in) BEGIN
        IF (clk='1' AND clk'EVENT) THEN
            IF (we='1') THEN
            mem(CONV_INTEGER(wr_addr)) <= data_in;
            END IF;
            data_out <= tmp_out; --registers output preventing
                                 -- bypass logic generation.
        END IF;
    END PROCESS;
END ram_infer;
```

Inferring ROM

Follow the guidelines below for the Synplify software to successfully infer ROM in a design:

- The address line must be at least 2 bits wide.
- ROM must be at least half full.
- A CASE or IF statement must make 16 or more assignments using constant values of the same width.

Inferring Shift Registers

The software infers shift registers for sequential shift components so that they can be placed in dedicated memory blocks in supported device architectures using the `altshift_taps` megafunction.

If it is required, set the implementation style with the `syn_srlstyle` attribute. If you do not want the components automatically mapped to shift registers, set the value to `registers`. You can set the value globally or on individual modules or registers.

For some designs, turning off shift register inference can improve the design performance.

Incremental Compilation & Block-Based Design

As designs become more complex and designers work in teams, a block-based hierarchical or incremental design flow is often an effective design approach. In an incremental compilation flow, you can make changes to part of the design while maintaining the placement and performance of unchanged parts of the design. Design iterations are made dramatically faster by focusing new compilations on a particular design partitions and merging results with previous compilation results of other partitions. In a bottom-up or team-based approach, you can perform optimization on individual subblocks and then preserve the results before you integrate the blocks into a final design and optimize it at the top level.

MultiPoint synthesis, which is available for certain device technologies in the Synplify Pro software, provides an automated block-based incremental synthesis flow. The MultiPoint feature manages a design hierarchy to let you design incrementally and synthesize designs that take too long for top-down synthesis of the entire project. MultiPoint synthesis allows different netlist files to be created for different sections of a design hierarchy, and supports Quartus II incremental compilation and LogicLock™ design methodologies. It also ensures that only those sections of a design that have been updated are resynthesized when the design is compiled, reducing synthesis run time and preserving the results for the unchanged blocks. You can change and resynthesize one section of a design without affecting other sections of the design.

You can also partition your design and create different netlist files manually with the Synplify software (basic Synplify and Synplify Pro) by creating a separate project for the logic in each partition of the design. Creating different netlist files for each partition of the design means that each partition is independent of the others. When synthesizing the entire project, only portions of a design that have been updated have to be

resynthesized when you compile the design. You can make changes and resynthesize one partition of a design to create a new netlist file without affecting the synthesis results and placement of other partitions.

Hierarchical design methodologies can improve the efficiency of your design process, providing better design reuse opportunities and fewer integration problems when working in a team environment. When you use these incremental synthesis methodologies, you can take advantage of the incremental compilation and methodologies in the Quartus II software. You can perform placement and routing on only the changed partitions of the design, reducing place-and-route time and preserving your fitting results. Following the guidelines in this section can help you achieve good results with these methodologies.

The following list shows the general top-down compilation flow when using these features of the Quartus II software:

1. Create Verilog HDL or VHDL design files as in the regular design flow.
2. Determine which hierarchical blocks are to be treated as separate partitions in your design.
3. Set up your design using the MultiPoint feature or separate projects so that a separate netlist file is created for each partition of the design.
4. If using separate projects, disable I/O pad insertion in the implementations for lower-level partitions.
5. Compile and technology-map each partition in the Synplify Pro or Synplify software, making constraints as you would in the regular design flow.
6. Import the VQM or EDIF netlist and the Tcl file for each partition into the Quartus II software and set up the Quartus II project(s) to use incremental compilation.
7. Compile your design in the Quartus II software and preserve the compilation results using the post-fit netlist in incremental compilation.
8. When you make design or synthesis optimization changes to part of your design, resynthesize only the changed partition to generate new netlist and Tcl file. Do not regenerate netlist files for the unchanged partitions.

9. Import the new netlist and Tcl file into the Quartus II software and recompile the design in the Quartus II software using incremental compilation.

For more information about creating partitions and using the incremental compilation in the Quartus II software, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*. For more information about using the LogicLock feature in the Quartus II software, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

Hierarchy & Design Considerations with Multiple VQM Files

To ensure the proper functioning of the synthesis flow, you can create separate netlist files only for modules and entities. In addition, each module or entity should have its own design file. If two different modules are in the same design file but are defined as being part of different partitions, you cannot maintain incremental compilation since both partitions would have to be recompiled when you change one of the modules.

Altera recommends that you register all inputs and outputs of each partition. This makes logic synchronous and avoids any delay penalty on signals that cross partition boundaries.

If you use boundary tri-states in a lower-level block, the Synplify software pushes (or "bubbles") the tri-states through the hierarchy to the top level to make use of the tri-state drivers on output pins of Altera devices. Because bubbling tri-states requires optimizing through hierarchies, lower-level tri-states are not supported with a block-based compilation methodology. You should use tri-state drivers only at the external output pins of the device and in the top-level block in the hierarchy.

For more tips on design partitioning, refer to the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Creating a Design with Separate Netlist Files

The first stage of a hierarchical or incremental design flow is to ensure that different parts of your design do not affect each other. Ensure that you have separate netlists for each partition in your design so that you can take advantage of the incremental compilation and LogicLock design flows in the Quartus II software. If the whole design is in one netlist file, changes in one partition affect other partitions because of possible node name changes when you resynthesize the design.

You can generate multiple VQM files either by using the MultiPoint synthesis flow and LogicLock attributes in the Synplify Pro software, or by manually creating separate Synplify projects and creating a black box for each block that you want to be considered as a separate design partition.

In the MultiPoint synthesis flow (Synplify Pro only), you create multiple VQMs from one easy-to-manage top-level synthesis project. By using the manual black box method (Synplify or Synplify Pro), you have multiple synthesis projects, which may be required for certain team-based or bottom-up designs where a single top-level project is not desired.

Once you have created multiple VQM files using one of these two methods, you need to create the appropriate Quartus II projects to place-and-route the design.

Creating a Design with Multiple VQM Files Using Synplify Pro MultiPoint Synthesis

This section describes how to generate multiple VQM files using the Synplify Pro MultiPoint synthesis flow. You must first set up your compile points, constraint files, and Synplify Pro options, then apply Altera-specific attributes to write multiple VQM files and create LogicLock region assignments.

Set Compile Points & Create Constraint Files

The MultiPoint flow lets you segment a design into smaller synthesis units, called Compile Points. The synthesis software treats each Compile Point as a partition for incremental mapping, which allows you to isolate and work on individual Compile Point modules as independent segments of the larger design without impacting other design modules. A design can have any number of Compile Points, and Compile Points can be nested. The top-level module is always treated as a Compile Point.

Compile Points are optimized in isolation from their parent, which can be another Compile Point or a top-level design. Each block created with a Compile Point is unaffected by critical paths or constraints on its parent or other blocks. A Compile Point is independent, with its own individual constraints. During synthesis, any Compile Points that have not yet been synthesized are synthesized before the top level. Nested Compile Points are synthesized before the parent Compile Points in which they are contained. When you apply the appropriate Synplify Pro LogicLock constraints to a Compile Point module, then a separate netlist is created for that Compile Point, isolating that logic from any other logic in the design.

Figure 8–6 on page 8–52 shows an example of a design hierarchy that can be split into multiple partitions. The top-level block of each partition can be synthesized as a separate Compile Point.

In this case, modules A, B, and F are Compile Points. The top-level Compile Point consists of the top-level block in the design (that is, block A in this example), including the logic that is not defined under another Compile Point. In this example, the design for top-level Compile Point A also includes the logic in one of its subblocks, C. Because block F is defined as its own Compile Point, it is not treated as part of the top-level Compile Point A. Another separate Compile Point B contains the logic in blocks B, D, and E. One netlist is created for the top-level module A and submodule C, another netlist is created for B and its submodules D and E, while a third netlist is created for F.

Apply Compile Points to the module or architecture in the Synplify Pro SCOPE spreadsheet or in the SDC file. You cannot set a Compile Point in the Verilog HDL or VHDL source code. You can set the constraints manually using Tcl or by editing the SDC file. You can also use the GUI which provides two methods, manual or automated, as shown below.

Defining Compile Points Using Tcl or SDC
To set Compile Points using Tcl or an SDC file, use the `define_compile_point` command, as shown in Example 8–20.

Example 8–20. The define_compile_point Command

```
define_compile_point [-disable] [-comment <comment>] <objname> \
[-type <compile point type>]
```

In the syntax statement above, *objname* represents any module in the design. Currently, `locked` is the only Compile Point type supported.

Each Compile Point has a set of constraint files that begin with the `define_current_design` command to set up the SCOPE environment.

```
define_current_design {<my_module>}
```

Manually Defining Compile Points from the GUI

The manual method requires you to separately create constraint files for the top-level and the lower-level Compile Points. To use the manual method:

1. From the top level, select the **Compile Points** tab in the SCOPE spreadsheet.
2. Select the modules that you want to define as Compile Points.

   Currently, locked Compile Points are the only type supported. All Compile Points must be defined from the top level because the **Compile Points** tab is not available in the SCOPE spreadsheet from lower level modules.
3. Manually create a constraint file for each module.

To ensure that changes to a Compile Point do not affect the top-level parent module, disable the **Update Compile Point Timing Data** option on the **Implementation Options** dialog box. If this option is enabled, updates to a child module can impact the top-level module.

Automatically Defining Compile Points from the GUI

When you use the automated process, the lower-level constraint file is created automatically. This eliminates the manual step necessary to do to set up each Compile Point. To use the automated method, perform the following steps:

1. On the File menu, select **New**. Click to create a new **Constraint File**, or click the **SCOPE** icon in the tool bar.
2. From the **Select File Type** tab of the **Create a New SCOPE File** dialog box, select **Compile Point**.
3. Select the module you want to designate as a Compile Point. The software automatically sets the Compile Points in the top-level constraint file and creates a lower-level constraint file for each Compile Point.

To ensure that changes to a Compile Point do not affect the top-level parent module, disable the **Update Compile Point Timing Data** option on the **Implementation Options** dialog box. If this option is enabled, updates to a child module can impact the top-level module.

When using Compile Points with the incremental compilation or LogicLock design flow, keep the following restrictions in mind:

- To use Compile Points effectively, you must provide timing constraints (timing budgeting) for each Compile Point; the more accurate the constraints, the better your results are. Constraints are not automatically budgeted, so manual time budgeting is essential. Altera recommends that you register all inputs and outputs of each partition. This avoids any logic delay penalty on signals that cross partition boundaries.
- When using the Synplify Pro attribute `syn_useioff` to pack registers in the I/O Elements (IOEs) of Altera devices, these registers must be in the top-level module, not a lower level. Otherwise, you must allow the Quartus II software to perform I/O register packing instead of the `syn_useioff` attribute. You can use the **Fast Input Register** or **Fast Output Register** options, or set I/O timing constraints and turn on **Optimize I/O cell register placement for timing** on the **Fitter Settings** page of the **Settings** dialog box in the Quartus II software.
- There is no incremental synthesis support for top-level logic; any logic in the top-level is resynthesized during every compilation in the Synplify Pro software.

For more information about Compile Points, refer to the *Synplify Pro User Guide and Reference Manual* on the Synplicity web site at **www.synplicity.com/literature/index.html**.

Apply the LogicLock Attributes

To instruct the Synplify Pro software to create a separate VQM netlist file for each Compile Point, you must indicate that the Compile Point is being used with LogicLock regions in the incremental compilation or LogicLock design methodology. Since separate netlist files are required for incremental compilation, you must use the LogicLock attributes if you plan to use the incremental compilation feature in the Quartus II software. When you apply the appropriate LogicLock attributes, the Synplify Pro software also writes out Tcl commands for the Quartus II software to create a LogicLock region for each netlist.

LogicLock regions in the Quartus II software have size and location properties. The region's size is defined by the height and width of the rectangular area. If the region is specified as auto-size, then the Quartus II software determines the appropriate size to fit the logic assigned to the region. When you specify the size, you must include enough device resources to accommodate the assigned logic. The location of a region is defined by its origin, which is the position of its bottom-left corner or top-left corner, depending on the target device family. In the Quartus II

software, this location can be specified as locked or floating. If the location is floating, the Quartus II software determines the location during its optimization process.

Floating locations are the only type currently supported in the Synplify Pro software.

When you use incremental compilation in the Quartus II software, you should lock down the size and location of the region in the Quartus II software after the first compilation to achieve the best quality of results.

Table 8–5 shows the valid combinations of the LogicLock attributes.

Table 8–5. LogicLock Location & Size Properties

altera_logiclock_location Attribute	altera_logiclock_size Attribute	Description
Floating	Auto	The most flexible type of LogicLock constraint. Allows the Quartus II software to choose appropriate region size and location.
Floating	Fixed	Assumes size of LogicLock constraint area is already optimal in existing Quartus II project.

You can apply these attributes to the top-level constraint file or to the individual constraint files for each lower-level Compile Point. You can use the **Attribute** tab of the SCOPE spreadsheet to set attributes.

Synplify Pro offers another attribute, `syn_allowed_resources`, which restricts the number of resources for a given module. You can apply the `syn_allowed_resources` attribute to any Compile Point view.

For specific information regarding these attributes, refer to the Synplify Pro online help or reference manual.

Creating a Quartus II Project for Multiple VQM Files

During compilation, the Synplify Pro software creates a <*top-level project*>**.tcl** file that provides the Quartus II software with the appropriate constraints and LogicLock assignments, creating a region for each VQM file along with the information to set up a Quartus II project.

The Tcl file contains the following commands for each LogicLock region. Example 8–21 is for module `A` (instance `u1`) in the project named `top` where the region name `cpll_1` was selected by Synplify Pro for the Compile Point.

Example 8–21. Commands for Each LogicLock Region in a Tcl File

```
set_global_assignment -section_id{taps_region} -name{LL_AUTO_SIZE}{ON}
set_global_assignment -section_id{taps_region} -name{LL_STATE}{FLOATING}
set_instance_assignment -section_id{taps_region} -to{|taps:u1} \
-name{LL_MEMBER_OF} {taps_region}
```

These commands create a LogicLock region with Auto Size and Floating Origin properties. This flexible LogicLock region allows the Quartus II Compiler to select the size and location of the region.

For more information about Tcl commands, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

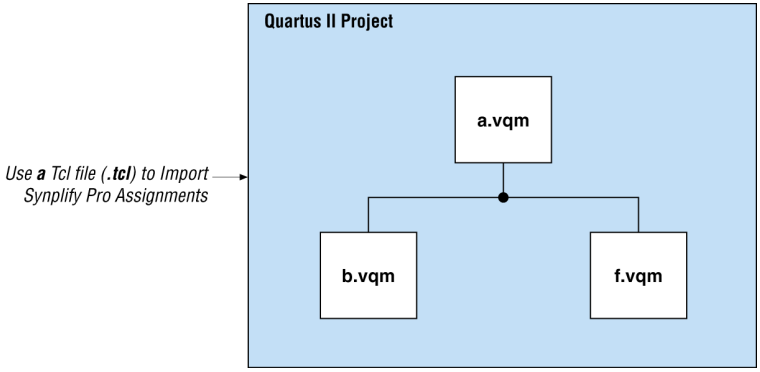
Depending on your design methodology, you can create one Quartus II project for all netlists (a top-down placement and routing flow) or a separate Quartus II project for each netlist (a bottom-up placement and routing flow). In a top-down incremental compilation design flow, you create design partition assignments and LogicLock floorplan location assignments for each partition in the design within a single Quartus II project. This methodology allows for the best quality of results and performance preservation during incremental changes to your design. You may require a bottom-up design flow if each partition must be optimized separately, such as in certain team-based design flows. To perform a bottom-up compilation in the Quartus II software, create separate Quartus II projects and import each design partition into a top-level design using the incremental compilation export and import features to maintain placement results.

The following sections describe how to create the Quartus II projects for these two design flows.

Creating a Single Quartus II Project for a Top-Down Incremental Compilation Flow

Use the <*top-level project*>**.tcl** file that contains the Synplify Pro assignments for all partitions within the project. This method allows you to import all the partitions into one Quartus II project and optimize all modules within the project at once, taking advantage of the performance preservation and compilation-time reduction incremental compilation offers. Figure 8–4 shows a visual representation of the design flow for the example design in Figure 8–6.

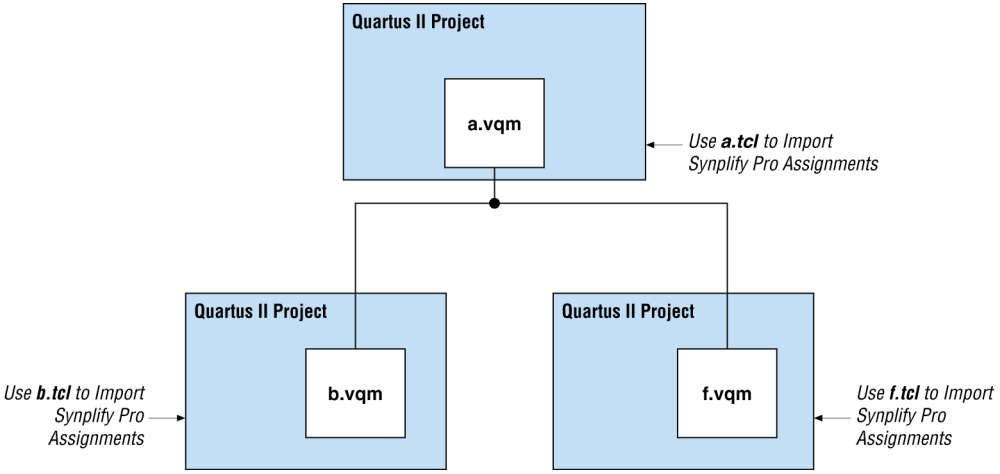
Figure 8–4. Design Flow Using Multiple VQM Files with One Quartus II Project



Creating Multiple Quartus II Projects for a Bottom-Up LogicLock Design Flow

Generate multiple Quartus II projects, one for each partition and netlist in the design. Each designer in the project can optimize their partition separately within the Quartus II software and export the placement for their partitions. Figure 8–5 shows a visual representation of the design flow for the example design in Figure 8–6. The optimized sub-designs can be brought into one top-level Quartus II project using incremental compilation.

Figure 8–5. Design Flow Using Multiple VQM Files with Multiple Quartus II Projects



Generating a Design with Multiple VQM Files Using Black Boxes

This section describes how to manually generate multiple VQM files using black boxes. This manual flow is supported in versions of the Synplify software that do not include the MultiPoint Synthesis feature.

Manually Creating Multiple VQM Files Using Black Boxes

To create multiple VQM files manually in the Synplify software, create a separate project for each low-level module and the top-level design that you want to maintain as a separate VQM file. Implement black box instantiations of lower-level partitions in your top-level project. When synthesizing the projects for the lower-level modules, perform the following steps.

1. In the **Implementation Options** dialog box, turn on **Disable I/O Insertion** for the target technology.
2. Read the HDL files for the modules.

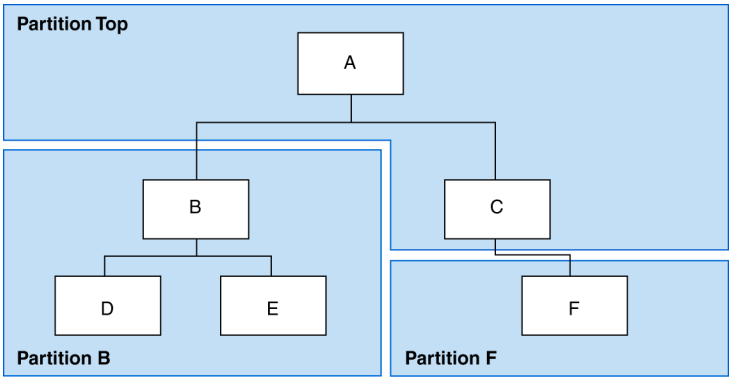
   Modules may include black box instantiations of lower-level modules that are also maintained as separate VQM files.
3. Add constraints with the SCOPE constraint editor.
4. Enter the clock frequency to ensure that the sub-design is correctly optimized.
5. In the **Attributes** tab, set **syn_netlist_hierarchy** to **0**.

When synthesizing the top-level design project, perform the following steps:

1. Turn off **Disable I/O Insertion** for the target technology.
2. Read the HDL files for top-level designs.
3. Create black boxes using lower-level modules in the top-level design.
4. Add constraints with the SCOPE constraint editor.
5. Enter the clock frequency to ensure that the design is correctly optimized.
6. In the **Attributes** tab, set **syn_netlist_hierarchy** to **0**.

The following sections describe an example of black box implementation to create separate VQM files. Figure 8–6 shows an example of a design hierarchy that is split up into multiple partitions.

Figure 8–6. Partitions in a Hierarchical Design



In Figure 8–6, the partition top contains the top-level block in the design (block A) and the logic that is not defined as part of another partition. In this example, the partition for top-level block A also includes the logic in one of its subblocks, C. Because block F is contained in its own partition, it is not treated as part of the top-level partition A. Another separate partition, B, contains the logic in blocks B, D, and E. In a team-based design, different engineers may work on the logic in different partitions. One netlist is created for the top-level module A and its submodule C, another netlist is created for B and its submodules D and E, while a third netlist is created for F. To create multiple VQM files for this design, follow these steps:

1. Generate a VQM file for module B. Use **B.v/.vhd**, **D.v/.vhd**, and **E.v/.vhd** as the source files.

2. Generate a VQM file for module F. Use **F.v/.vhd** as the source files.

3. Generate a top-level VQM file for module A. Use **A.v/.vhd** and **C.v/.vhd** as the source files. Ensure that you use black box modules B and F, which were optimized separately in the previous steps.

Creating Black Boxes in Verilog HDL

Any design block that is not defined in the project or included in the list of files to be read for a project are treated as a black box by the software. Use the `syn_black_box` attribute to indicate that you intend to create a black box for the given module. In Verilog HDL, you must provide an empty module declaration for the module that is treated as a black box.

Example 8–22 shows an example of the **A.v** top-level file. Follow the same procedure below for lower-level files which also contain a black box for any module beneath the current level hierarchy.

Example 8–22. Verilog HDL Black Box for Top-Level File A.v

```
module A (data_in, clk, e, ld, data_out);
    input data_in, clk, e, ld;
    output [15:0] data_out;

    wire [15:0] cnt_out;

    B U1 (.data_in (data_in),.clk(clk), .ld (ld),.data_out(cnt_out));
    F U2 (.d(cnt_out), .clk(clk), .e(e), .q(data_out));

    // Any other code in A.v goes here.

endmodule

// Empty Module Declarations of Sub-Blocks B and F follow here.
// These module declarations (including ports) are required for black
boxes.

module B (data_in, clk, ld, data_out) /* synthesis syn_black_box */ ;
    input data_in, clk, ld;
    output [15:0] data_out;
endmodule

module F (d, clk, e, q) / *synthesis syn_black_box */ ;
    input [15:0] d;
    input clk, e;
    output [15:0] q;
endmodule
```

Creating Black Boxes in VHDL

Any design block that is not defined in the project or included in the list of files to be read for a project are treated as a black box by the software. Use the `syn_black_box` attribute to indicate that you intend to treat the given component as a black box. In VHDL, you need a component declaration for the black box just like any other block in the design.

Although VHDL is not case-sensitive, VQM (a subset of Verilog HDL) is case-sensitive. Entity names and their port declarations are forwarded to the VQM. Black box names and port declarations are also passed to the VQM. To prevent case-based mismatches between VQM, use the same capitalization for black box and entity declarations in VHDL designs.

Example 8–23 shows an example of the **A.vhd** top-level file. Follow this same procedure for any lower-level files that contain a black box for any block beneath the current level of hierarchy.

Example 8–23. VHDL Black Box for Top-Level File A.vhd

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
LIBRARY synplify;
use synplify.attributes.all;

ENTITY A IS
PORT ( data_in : IN INTEGER RANGE 0 TO 15;
   clk, e, ld : IN STD_LOGIC;
   data_out : OUT INTEGER RANGE 0 TO 15 );
END A;

ARCHITECTURE a_arch OF A IS

COMPONENT B PORT(
   data_in : IN INTEGER RANGE 0 TO 15;
   clk, ld : IN STD_LOGIC;
   d_out : OUT INTEGER RANGE 0 TO 15 );
END COMPONENT;

COMPONENT F PORT(
   d : IN INTEGER RANGE 0 TO 15;
   clk, e: IN STD_LOGIC;
   q : OUT INTEGER RANGE 0 TO 15 );
END COMPONENT;

attribute syn_black_box of B: component is true;
attribute syn_black_box of F: component is true;

-- Other component declarations in A.vhd go here
```

```
signal cnt_out : INTEGER RANGE 0 TO 15;

BEGIN

U1 : B
PORT MAP (
    data_in => data_in,
    clk => clk,
    ld => ld,
    d_out => cnt_out );

U2 : F
PORT MAP (
    d => cnt_out,
    clk => clk,
    e => e,
    q => data_out );

-- Any other code in A.vhd goes here

END a_arch;
```

After you have completed the steps described in this section, you have a netlist file for each partition of the design. These files are ready for use with incremental compilation in the Quartus II software.

Creating a Quartus II Project for Multiple VQM Files

The Synplify software creates a Tcl file for each VQM file, that provide the Quartus II software with the appropriate constraints and information to set up a project. For details on using the Tcl script generated by the Synplify software to set up your Quartus II project and pass your constraints, refer to "Running the Quartus II Software Manually Using the Synplify-Generated Tcl Script" on page 8–18.

Depending on your design methodology, you can create one Quartus II project for all netlists (a top-down placement and routing flow) or a separate Quartus II project for each netlist (a bottom-up placement and routing flow). In a top-down incremental compilation design flow, you create design partition assignments and LogicLock floorplan location assignments for each partition in the design within a single Quartus II project. This methodology allows for the best quality of results and performance preservation during incremental changes to your design. You may require a bottom-up design flow where each partition must be optimized separately, such as in certain team-based design flows. To perform a bottom-up compilation in the Quartus II software, create

separate Quartus II projects and import each design partition into a top-level design using the incremental compilation export and import features to maintain placement results.

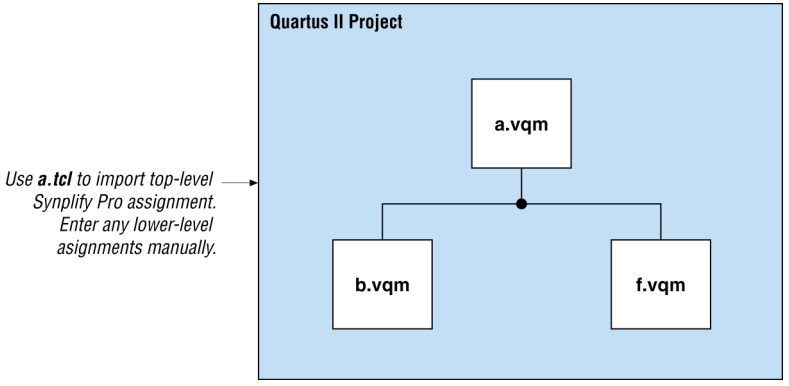
The following sections describe how to create the Quartus II projects for these two design flows.

Creating Compile Points in Single Quartus II Project for a Top-Down Incremental Compilation Flow

Use the <*top-level project*>**.tcl** file that contains the Synplify assignments for the top-level design. This method allows you to import all the partitions into one Quartus II project and optimize all modules within the project at once, taking advantage of the performance preservation and compilation time reduction offered by incremental compilation. Figure 8–7 shows a visual representation of the design flow for the example design in Figure 8–6.

All the constraints from the top-level project will be passed to the Quartus II software in the top-level Tcl file, but any constraints made in the lower-level projects within the Synplify software is not forward-annotated. Enter these constraints manually in your Quartus II project.

Figure 8–7. Design Flow Using Multiple VQM Files with One Quartus II Project

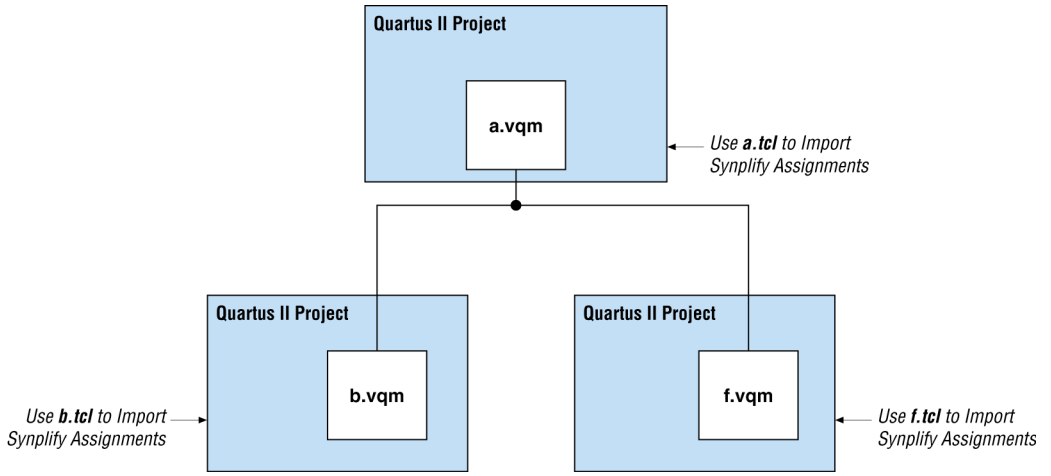


Creating Multiple Quartus II Projects for a Bottom-Up Design Flow

Use the Tcl file that is created for each VQM file by the Synplify software for each Synplify Project. This method generates multiple Quartus II projects, one for each block in the design. Each designer in the project can optimize their block separately within the Quartus II software and export the placement of their blocks. Figure 8–8 on page 8–57 shows a visual representation of the design flow for the example in Figure 8–6 on

page 8–52. Designers should create a LogicLock region for each block; the top-level designer should then import all the blocks and assignments into the top-level project. This method allows each block in the design to be treated separately; each block can then be imported into one top-level project.

Figure 8–8. Design Flow Using Multiple Synplify Projects & Multiple Quartus II Projects



Conclusion

Advanced synthesis is an important part of the design flow. Taking advantage of the Synplicity Synplify and Quartus II design flows allows you to control how your design files are prepared for the Quartus II place-and-route process, as well as improve performance and optimize a design for use with Altera devices. Several of the methodologies outlined in this chapter can help optimize a design to achieve performance goals and save design time.

9. Mentor Graphics Precision RTL Synthesis Support

QII51011-6.0.0

Introduction

As programmable logic device (PLD) designs become more complex and require increased performance, advanced synthesis has become an important part of the design flow. This chapter documents support for the Mentor Graphics® Precision RTL Synthesis software in the Quartus® II software design flow, as well as key design methodologies and techniques for improving your results for Altera® devices. This chapter includes the following sections:

- General design flow with the Precision RTL Synthesis software and the Quartus II software
- Creating a project and compiling the design
- Setting constraints to achieve optimal results
- Synthesizing the design and evaluating the results
- Exporting designs to the Quartus II software using NativeLink® integration
- Guidelines for Altera megafunctions and the library of parameterized modules (LPM) functions, instantiating them in a clear-box or black-box flow using the MegaWizard® Plug-In manager, and tips for inferring them from HDL code
- Incremental compilation and block-based design

This chapter assumes that you have installed and licensed the Precision RTL Synthesis software and the Quartus II software.

To obtain and license the Precision RTL Synthesis software, refer to the Mentor Graphics web site at **www.mentor.com**. To install and run the Precision RTL Synthesis software and to set up your work environment, refer to the *Precision RTL Synthesis User's Manual* in the Precision Manuals Bookcase in the Help menu.

Design Flow

The basic steps in a Quartus II design flow using the Precision RTL Synthesis software are as follows:

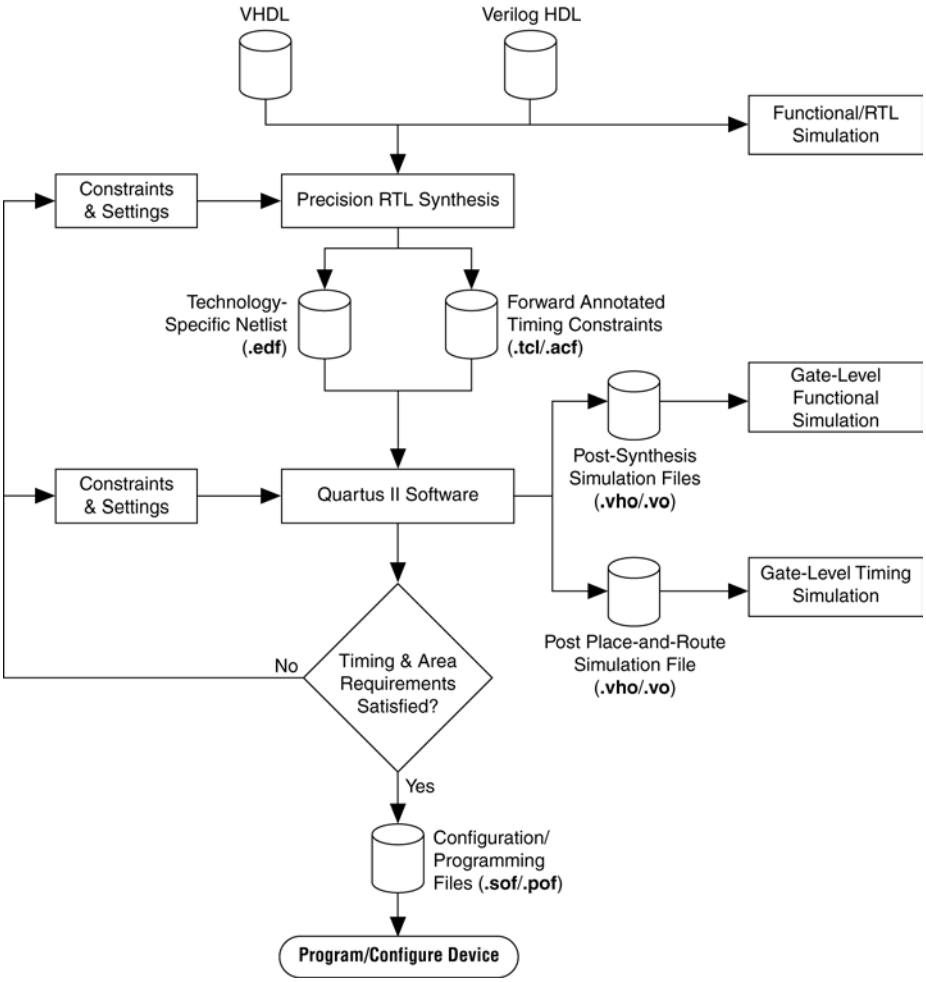
1. Create Verilog HDL or VHDL design files in the Quartus II design software, the Precision RTL Synthesis software, or with a text editor.
2. Create a project in the Precision RTL Synthesis software that contains the HDL files for your design, select your target device, and set global constraints. For best results when using Altera megafunctions, Mentor Graphics recommends using the clear box option which enables synthesis to report more accurate resource utilization and timing estimates. Refer to "Clear-Box Methodology" on page 9–20 for details.
3. Compile the project in the Precision RTL Synthesis software.
4. Add specific timing constraints, optimization attributes, and compiler directives to optimize the design during synthesis.

   For best results, Mentor Graphics recommends specifying constraints that are as close as possible to actual operating requirements. Properly setting clock and I/O constraints, assigning clock domains, and indicating false and multicycle paths guide the synthesis algorithms more accurately toward a suitable solution in the shortest synthesis time.
5. Synthesize the project in the Precision RTL Synthesis software. With the design analysis capabilities and cross-probing of Precision RTL Synthesis software, you can identify and improve circuit area and performance issues using pre-layout timing estimates.
6. Create a Quartus II project and import the technology-specific EDIF (**.edf**) netlist and the tool command language (**.tcl**) file generated by the Precision RTL Synthesis software into the Quartus II software for placement and routing, and for performance evaluation using actual post-layout timing data.
7. After obtaining place-and-route results that meet your needs, configure or program the Altera device.

These steps are described in detail throughout this chapter. Figure 9–1 shows the Quartus II design flow using Precision RTL Synthesis as described in the steps above.

Figure 9–1. Design Flow Using the Precision RTL Synthesis Software & Quartus II Software



If your area or timing requirements are not met, you can change the constraints and resynthesize the design in the Precision RTL Synthesis software, or you can change constraints to optimize the design during place and route in the Quartus II software. Repeat the process until the area and timing requirements are met (Figure 9–1).

You can use other options and techniques in the Quartus II software to meet area and timing requirements. One such option is the **WYSIWYG Primitive Resynthesis** option, which can perform optimizations on your EDIF netlist in the Quartus II software.

For information about netlist optimizations, refer to the *Netlist Optimizations and Physical Synthesis* chapter in volume 2 of the *Quartus II Handbook*. For more recommendations on how to optimize your design, refer to the *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

While simulation and analysis can be performed at various points in the design process, final timing analysis should be performed after placement and routing is complete.

During the synthesis process, the Precision RTL Synthesis software produces several intermediate and output files. Table 9–1 lists these files with a short description of each file type.

Table 9–1. Precision RTL Synthesis Software Intermediate & Output Files

File Extension(s)	File Description
.sdc	Design constraints file in Synopsys Design Constraints File
.psp	Precision RTL Synthesis Software Project File
.xdb	Mentor Graphics Design Database File
.rep *(1)*	Synthesis Area & Timing Report File
.edf	Technology-specific netlist in electronic design interchange format (EDIF)
.acf/**.tcl** *(2)*	Forward-annotated constraints file containing constraints and assignments

Notes to Table 9–1:

(1) The timing report file includes performance estimates that are based on preplace-and-route information. Use the f_{MAX} reported by the Quartus II software after place-and-route for accurate post-place-and-route timing information. The area report file includes post-synthesis device resource utilization statistics that may differ from the resource usage after place-and-route due to black-boxes or further optimizations performed during placement and routing. Use the device utilization reported by the Quartus II software after place-and-route for final resource utilization results. See *"Synthesizing the Design & Evaluating the Results" on page 9–11* for details.

(2) An Assignment & Configuration File (**.acf**) file is created only for ACEX® 1K, FLEX® 10K, FLEX 10KA, FLEX 6000, FLEX 8000, MAX® 7000, MAX 9000, and MAX 3000 devices. The Assignment & Configuration File is generated for backward compatibility with the MAX+PLUS® II software. A Tcl file for the Quartus II software is created for all devices, which also contains Tcl commands to create and compile a Quartus II project.

Creating a Project & Compiling the Design

After creating your design files, create a project in the Precision RTL Synthesis software that contains the basic settings for compiling the design.

Creating a Project

Set up your design files as follows:

1. In the Precision RTL Synthesis software, click the **New Project** icon in the Design Bar on the left side of the GUI.
2. Set the **Project Name** and the **Project Folder**. The implementation name of the design corresponds to this project name.
3. Add input files to the project with the **Add Input Files** icon in the Design Bar. Precision RTL Synthesis software automatically detects the top-level module/entity of the design. It uses the top-level module/entity to name the current implementation directory, logs, reports, and netlist files.
4. In the Design Bar, click the **Setup Design** icon.
5. To specify a target device family, expand the Altera entry, and choose the target device and speed grade.
6. If desired, set a global design frequency and/or default input and output delays. This constrains all clock paths and all I/O pins in your design. Modify the settings for individual paths or pins that do not require such a setting. All timing constraints are forward-annotated to the Quartus II software using Tcl scripts.

To generate additional netlist files (for example, an HDL netlist for simulation), on the Tools menu, point to **Set Options > Output** and click **Additional Output Netlist**. The Precision RTL Synthesis software generates a separate file for each selected type of file: EDIF, Verilog HDL, and VHDL.

Compiling the Design

To compile the design into a technology-independent implementation, click the **Compile** icon in the Design Bar.

Setting Constraints

In the next steps, you set constraints and map the design to technology-specific cells. The Precision RTL Synthesis software maps the design by default to the fastest possible implementation that meets your timing constraints. To accomplish this, you must specify timing requirements for the automatically determined clock sources. With this information, the Precision RTL Synthesis software performs static timing analysis to determine the location of the critical timing paths. The Precision RTL Synthesis software achieves the best results for your design when you set as many realistic constraints as possible. Ensure to set constraints for timing, mapping, false paths, multicycle paths, and others that control the structure of the implemented design.

Mentor Graphics recommends creating a Synopsys Design Constraint file (**.sdc**) and adding this file to the Constraint Files section of the Project Files list. You can create this file with a text editor or use the Precision RTL Synthesis software to generate one automatically for you on the first synthesis run. To create an initial constraint file manually, set constraints on design objects (such as clocks, design blocks, or pins) in the Design Hierarchy browser. By default, the Precision RTL Synthesis software saves all timing constraints and attributes in two files: **precision_rtl.sdc** and **precision_tech.sdc**. The **precision_rtl.sdc** file contains constraints set on the RTL-level database (after compilation) and **precision_tech.sdc** file contains constraints set on the gate-level database (after synthesis) located in the current implementation directory.

You can also enter constraints at the command line. After adding constraints at the command line, update the SDC file with the **update constraint file** command.

You can add constraints that change infrequently directly to the HDL source files with HDL attributes or pragmas.

For more details and examples, refer to the Attributes chapter in the *Precision Synthesis Reference Manual* in the Precision Manual Bookcase in the Help menu.

Setting Timing Constraints

Timing constraints, based on the industry-standard Synopsys Design Constraint file format, help the Precision RTL Synthesis software to deliver optimal results. Missing timing constraints can result in incomplete timing analysis and may prevent timing errors from being detected. Precision RTL Synthesis software provides constraint analysis prior to synthesis to ensure that designs are fully and accurately constrained. All timing constraints are forward-annotated to the Quartus II software using Tcl scripts.

Because the Synopsys Design Constraint file format requires that timing constraints must be set relative to defined clocks, you must specify your clock constraints before applying any other timing constraints.

You also can use multicycle path and false path assignments to relax requirements or exclude nodes from timing requirements. Doing so can improve area utilization and allow the software optimizations to focus on the most critical parts of the design.

For details about the syntax of Synopsys Design Constraint commands, refer to the *Precision RTL Synthesis Users Manual* and the *Precision Synthesis Reference Manual* available in the Precision Manual Bookcase in the Help menu.

Setting Mapping Constraints

Mapping constraints affect how your design is mapped into the target Altera device. You can set mapping constraints in the user interface, in HDL code, or with the **set_attribute** command in the constraint file.

Assigning Pin Numbers & I/O Settings

The Precision RTL Synthesis software supports assigning device pin numbers, I/O standards, drive strengths, and slew-rate settings to top-level ports of the design. You can set these timing constraints with the **set_attribute** command, the GUI, or by specifying synthesis attributes in your HDL code. These constraints are written into the Tcl file that is read by the Quartus II software during place-and-route and do not affect synthesis.

You can use the **set_attribute** command in the Synopsys Design Constraint file to specify pin number constraints, I/O standards, drive strengths, and slow slew-rate settings. Table 9–2 outlines the format to use for entries in the Synopsys Design Constraint file.

Table 9–2. Constraint File Settings

Constraint	Entry Format for Synopsys Design Constraint File
Pin number	`set_attribute -name PIN_NUMBER -value "<pin number>" -port <port name>`
I/O standard	`set_attribute -name IOSTANDARD -value "<I/O Standard>" -port <port name>`
Drive strength	`set_attribute -name DRIVE -value "<drive strength in mA>" -port <port name>`
Slew rate	`set_attribute -name SLEW -value "TRUE | FALSE" -port <port name>`

You can also specify these options in the GUI. To specify a pin number or other I/O setting in the Precision RTL Synthesis GUI, follow these steps:

1. After compiling the design, expand the **Ports** entry in the Design Hierarchy Browser.
2. Under **Ports,** expand the **Inputs** or **Outputs** entry.

    You also can assign I/O settings by right-clicking the pin in the Schematic Viewer.

3. Right-click the desired pin name and select the **Set Input Constraints** option under **Inputs** or **Set Output Constraints** option under **Outputs**.
4. Enter the desired pin number on the Altera device in the **Pin Number** box (**Port Constraints** dialog box).
5. Select the I/O standard from the **IO_STANDARD** list.
6. For output pins, you can also select a drive strength setting and slew rate setting using the **DRIVE** and **SLOWSLEW** lists.

You also can use synthesis attributes or pragmas in your HDL code to make these assignments. The following code samples show you how to make a pin assignment in your HDL code.

Example 9–1. Verilog HDL Pin Assignment

```
//pragma attribute clk pin_number P10;
```

Example 9–2. VHDL Pin Assignment

```
attribute pin_number : string
attribute pin_number of clk : signal is “P10”;
```

You can use the same syntax to assign the I/O standard using the attribute `IOSTANDARD`, drive strength using the attribute `DRIVE`, and slew rate using the attribute `SLEW`.

 For more details about attributes and how to set them in your HDL code, refer to the *Precision Synthesis Reference Manual*.

Assigning I/O Registers

The Precision RTL Synthesis software performs timing-driven I/O register mapping by default. It moves registers into an I/O element (IOE) when it does not negatively impact the register-to-register performance of your design, based on the timing constraints.

You can force a register to the device's IOE using the Complex I/O constraint. This option does not apply if you turn off I/O pad insertion. Refer to "Disabling I/O Pad Insertion" for more information.

To force an I/O register into the device's IOE using the GUI, follow these steps:

1. After compiling the design, expand the **Ports** entry in the Design Hierarchy browser.
2. Under **Ports**, expand the **Inputs** or **Outputs** entry, as desired.
3. Under **Inputs** or **Outputs**, right-click the desired pin name and select **Force Register into IO**.

You also can make the assignment by right-clicking on the pin in the Schematic Viewer.

For Stratix® II, Cyclone™ II, MAX® II, Stratix, and Cyclone families of devices, the Precision RTL Synthesis software can move an internal register to an I/O register without any restrictions on design hierarchy.

For more mature devices, the Precision RTL Synthesis software can move an internal register to an I/O register only when the register exists in the top level of the hierarchy. If the register is buried in the hierarchy, you must flatten the hierarchy so that the buried registers are moved to the top level of the design.

Disabling I/O Pad Insertion

The Precision RTL Synthesis software assigns I/O pad atoms (device primitives used to represent the I/O pins and I/O registers used) to all ports in the top level of a design by default. In certain situations, you may not want the software to add I/O pads to all I/O pins in the design. The Quartus II software can compile a design without I/O pads; however, including I/O pads provides the Precision RTL Synthesis software with the most information about the top-level pins in the design.

Preventing the Precision RTL Synthesis Software from Adding I/O Pads

If you are compiling a subdesign as a separate project, I/O pins cannot be primary inputs or outputs of the device and therefore should not have an I/O pad associated with them. To prevent the Precision RTL Synthesis software from adding I/O pads, perform the following steps:

1. On the Tools menu, click **Set Options**.
2. On the **Optimization** page of the **Options** dialog box, turn off **Add IO Pads**, then click **Apply**.

This procedure adds the following command to the project file:

```
setup_design -addio=false
```

Preventing the Precision RTL Synthesis Software from Adding an I/O Pad on an Individual Pin

To prevent I/O pad insertion on an individual pin when you are using a black box, such as Double Data Rate (DDR) or a Phase-Locked Loop (PLL), at the external ports of the design, follow these steps:

1. After compiling the design, in the Design Hierarchy browser, expand the **Ports** entry by clicking the +.
2. Under **Ports**, expand the **Inputs** or **Outputs** entry.
3. Under **Inputs** or **Outputs**, right-click the desired pin name and click **Set Input Constraints**.
4. In the **Port Constraints** dialog box for the selected pin name, turn off **Insert Pad**.

You also can make the assignment by right-clicking on the pin in the Schematic Viewer or by attaching the `nopad` attribute to the port in the HDL source code.

Controlling Fan-Out on Data Nets

Fan-out is defined as the number of nodes driven by an instance or top-level port. High fan-out nets can have significant delays which can result in an unroutable net. On a critical path, high fan-out nets can cause larger delay in a single net segment which can result in the timing constraints not being met. To prevent this behavior, each device family has a global fan-out value set in the Precision RTL Synthesis software

library. In addition, the Quartus II software automatically routes high fan-out signals on global routing lines in the Altera device whenever possible.

To eliminate routability and timing issues associated with high fan-out nets, the Precision RTL Synthesis software also allows you to override the library default value on a global or individual net basis. You can override the library value by setting a `max_fanout` attribute on the net.

Synthesizing the Design & Evaluating the Results

To synthesize the design for the target device, click on the **Synthesize** icon in the Precision RTL Synthesis Design Bar. During synthesis, the Precision RTL Synthesis software optimizes the compiled design, then writes out netlists and reports to the implementation subdirectory of your working directory after the implementation is saved, using the naming convention:

<*project name*>_impl_<*number*>

After synthesis is complete, you can evaluate the results in terms of area and timing. The *Precision RTL Synthesis User's Manual* on the Mentor Graphics web site describes different results that can be evaluated in the software.

There are several schematic viewers available in the Precision RTL Synthesis software: RTL schematic, Technology-mapped schematic, and Critical Path schematic. These analysis tools allow you to quickly and easily isolate the source of timing or area issues, and to make additional constraint or code changes, if needed, to optimize the design.

Obtaining Accurate Logic Utilization & Timing Analysis Reports

Historically, designers have relied on post-synthesis logic utilization and timing reports to determine how much logic their design requires, how big a device they need, and how fast the design will run. However, today's FPGA devices provide a wide variety of advanced features in addition to basic registers and look-up tables. The Quartus II software has advanced algorithms to take advantage of these features, as well as optimization techniques to both increase performance and reduce the amount of logic required for a given design. In addition, designs may contain black boxes and functions that take advantage of specific device features. Because of these advances, synthesis tool reports provide post-synthesis area and timing estimates, but the place-and-route software should be used to obtain final logic utilization and timing reports.

Exporting Designs to the Quartus II Software Using NativeLink Integration

The NativeLink feature in the Quartus II software facilitates the seamless transfer of information between the Quartus II software and EDA tools, which allows you to run other EDA design entry/synthesis, simulation, and timing analysis tools automatically from within the Quartus II software.

After a design is synthesized in the Precision RTL Synthesis software, the technology-mapped design is written to the current implementation directory as an EDIF netlist file, along with a Quartus II Project Configuration File and a Place-and-Route Constraints File, written as Tcl scripts. You can use the Project Configuration script, <*project name*>**.tcl**, to create and compile a Quartus II project for your EDIF netlist. This script makes basic project assignments, such as assigning the target device specified in the Precision RTL Synthesis software, and makes timing assignments. For many devices, the Project Configuration script calls the place-and-route constraints script, <*project name*>**_pnr_constraints.tcl**, to make your timing constraints.

Running the Quartus II Software from within the Precision RTL Software

Precision RTL Synthesis software also has a built-in place-and-route environment that allows you to run the Quartus II Fitter and view the results in the Precision RTL Synthesis GUI. This feature is useful when performing an initial compilation of your design to view post-place-and-route timing and device utilization results, but not all the advanced Quartus II options that control the compilation process are available.

After you specify an Altera device as the target, set the Quartus II options. On the Tools menu, click **Set Options**. On the **Integrated Place and Route** page, specify the path to the Quartus II executables in the **Path to Quartus II installation** box.

To automate the place-and-route process, click the **Run Quartus** icon in the **Quartus II** window of the Precision RTL Synthesis Toolbar. The Quartus II software uses the current implementation directory as the Quartus II project directory and runs a full compilation in the background (that is, no user interface appears).

Two primary Precision RTL Synthesis software commands control the place-and-route process. Place-and-route options are set by the **setup_place_and_route** command. The process is started with the **place_and_route** command.

Precision RTL Synthesis software versions 2004a and later support using individual Quartus II executables, such as analysis and synthesis (**quartus_map**), Fitter (**quartus_fit**), and Timing Analyzer (**quartus_tan**), for improved runtime and memory utilization during place and route. This flow is referred to as the **Quartus II Modular** flow option in Precision RTL Synthesis software and is compatible with Quartus II software versions beginning with version 4.0. By default, the Precision RTL Synthesis software generates this Quartus II Project Configuration File (Tcl file) for Stratix II, Stratix, Stratix GX, MAX II, Cyclone II, and Cyclone device families. When using this flow, all timing constraints that you set during synthesis are exported to the Quartus II place-and-route constraints file (<*project name*>**_pnr_constraints.tcl**).

For other device families, Precision RTL Synthesis software uses the **Quartus II** flow option, which enables the Quartus II compilation flow that existed in Precision RTL Synthesis software versions earlier than 2004a. The Quartus II Project Configuration File (Tcl file) written when using the **Quartus II** flow option includes supported timing constraints that you specified during synthesis. This Tcl file is compatible with all versions of the Quartus II software; however, the format and timing constraints do not take full advantage of the features in the Quartus II software introduced with version 4.0.

To force the use of a particular flow when it is not the default for a certain device family, use the following command to set up the integrated place-and-route flow:

```
setup_place_and_route -flow "<Altera Place-and-Route flow>"
```

Depending on the device family, you can use one of the following flow options in the command above:

- `Quartus II Modular`
- `Quartus II`
- `MAX+PLUS II`

For example, for the Stratix II or MAX II device families (which were not supported in Quartus II software versions earlier than 4.0), you can use only the **Quartus II Modular** flow. For the Stratix device family you can use either the **Quartus II Modular** or **Quartus II** flows. The FLEX 8000 device family, which is not supported in the Quartus II software, is supported only by the **MAX+PLUS II** flow.

After the design is compiled in the Quartus II software from within the Precision RTL Synthesis software, you can invoke the Quartus II GUI manually and then open the project using the generated Quartus II project file. You can view reports, run analysis tools, specify options, and run the various processing flows available in the Quartus II software.

Running the Quartus II Software Manually Using the Precision RTL Synthesis-Generated Tcl Script

You can use the Quartus II software separately from the Precision RTL Synthesis software. To run the Tcl script generated by the Precision RTL Synthesis software to set up your project and start a full compilation, perform the following steps:

1. Ensure the EDIF and Tcl files are located in the same directory (they should both be located in the implementation directory by default).
2. In the Quartus II software, on the View menu, point to Utility Windows and click **Tcl Console**.
3. At the Tcl Console command prompt, type the command:

   `source <path>/<project name>.tcl ↵`

4. On the File menu, click **Open Project**. Browse to the project name, and click **Open**.
5. Compile the project in the Quartus II software.

Using Quartus II Software to Launch the Precision RTL Synthesis Software

Using NativeLink integration, you can set up the Quartus II software to run the Precision RTL Synthesis software. This feature allows you to use the Precision RTL Synthesis software to synthesize a design as part of a normal compilation.

For detailed information about using NativeLink integration with the Precision RTL Synthesis software, go to *Specifying EDA Tool Settings* in the Quartus II Help index.

Passing Constraints to the Quartus II Software

The place-and-route constraints script forward-annotates timing constraints that you made in the Precision RTL Synthesis software. This integration allows you to enter these constraints once in the Precision RTL Synthesis software, and then pass them automatically to the Quartus II software.

The following constraints are translated by the Precision RTL Synthesis software:

- `create_clock`
- `set_input_delay`
- `set_output_delay`
- `set_false_path`
- `set_multicycle_path`

create_clock

You can specify a clock in the Precision RTL Synthesis software as shown in Example 9–3.

Example 9–3. Specifying a Clock using create_clock

```
create_clock -name <clock_name> -period <period in ns> -waveform {<edge_list>} -domain
<ClockDomain> <pin>
```

The period is always in units of ns. If no clock domain is specified, the clock belongs to a default clock domain `main`. All clocks in the same clock domain are treated as synchronous (that is, related) clocks. If no <*clock_name*> is provided, the default name `virtual_default` is used. The <*edge_list*> sets the rise and fall edges of the clock signal over an entire clock period. The first value in the list is a rising transition, typically the first rising transition after time zero. The waveform can contain any even number of alternating edges, and the edges listed should alternate between rising and falling. The position of any edge can be equal to or greater than zero but must be equal to or less than the clock period. If `-waveform` <*edge_list*> is not specified, but `-period` <*period_value*> is specified, the default waveform has a rising edge of 0.0 and a falling edge of <*period_value*>/2.

The Precision RTL Synthesis software passes the clock definitions to the Quartus II software with the `create_base_clock` command.

The following list describes some differences in the clock properties supported by the Precision RTL Synthesis software and the Quartus II software:

- The Quartus II software supports only clock waveforms with two edges in a clock cycle. If the Precision RTL Synthesis software finds a multi-edge clock, it passes to the Quartus II software and issues an error message.
- Clocks in the same clock -`domain` are annotated with the `create_relative_clock` command to create related clocks in the Quartus II software.
- The Quartus II software assumes the first clock edge to be at time 0.0. If the Precision RTL Synthesis software waveform has a first transition at a time different than time zero (0.0), the Precision RTL Synthesis software creates a base clock without any target, then uses this to create a relative clock with an offset set to the first clock edge.

set_input_delay

This port-specific input delay constraint is specified in the Precision RTL Synthesis software as shown in Example 9–4.

Example 9–4. Specifying set_input_delay

```
set_input_delay <delay_value port_pin_list> -clock <clock_name> -rise
-fall -add_delay
```

This constraint is mapped to the `set_input_delay` setting in the Quartus II software.

When the reference clock <*clock_name*> is not specified, all clocks are assumed to be the reference clocks for this assignment. The input pin name for the assignment can be an input pin name of a time group. The software can use the option `clock_fall` to specify delay relative to the falling edge of the clock.

Although the Precision RTL Synthesis software allows you to set input delays on pins inside the design, these constraints are not sent to the Quartus II software, and a message is displayed.

set_output_delay

This port-specific output delay constraint is specified in the Precision RTL Synthesis software as shown in Example 9–5.

Example 9–5. Using the set_output_delay Constraint

```
set_output_delay <delay_value> <port_pin_list> -clock <clock_name> -rise -fall
-add_delay
```

This constraint is mapped to the `set_output_delay` setting in the Quartus II software.

When the reference clock <*clock_name*> is not specified, all clocks are assumed to be the reference clocks for this assignment. The output pin name for the assignment can be an output pin name of a time group.

Although the Precision RTL Synthesis software allows you to set output delays on pins inside the design, these constraints are not sent to the Quartus II software, and a message is displayed.

set_false_path

The false path constraint is specified in the Precision RTL Synthesis software as shown in Example 9–6.

Example 9–6. Using the set_false_path Constraint

```
set_false_path -to <to_node_list> -from <from_node_list> -reset_path
```

The node lists can be a list of clocks, ports, instances, and pins. Multiple elements in the list can be represented using wildcards such as "*" and "?."

This setting in the Precision RTL Synthesis software is mapped to a `set_timing_cut_assignment` setting in the Quartus II software.

The node lists for this assignment represents top-level ports and/or nets connected to instances (end points of timing assignments). The node lists can contain wildcards. The Quartus II software does not support bus notation such as A[7:4] in the node lists.

The Quartus II software does not support any `setup`, `hold`, `rise`, or `fall` options for this assignment.

The Quartus II software does not support false paths with the `through` path specification. Any setting in the Precision RTL Synthesis software with a `-through` specification cannot be mapped to a setting in the Quartus II software.

If you use the `from` or `to` option without using both options, the Precision RTL Synthesis command is converted to a Quartus II command using wildcards. Table 9–3 lists these `set_false_path` constraints in the Precision RTL Synthesis software and the Quartus II software equivalent.

Table 9–3. set_false_path Constraints

Precision RTL Synthesis Assignment	Quartus II Equivalent
set_false_path -from <*from_node_list*>	set_timing_cut_assignment -to {*} -from <*node_list*>
set_false_path -to <*to_node_list*>	set_timing_cut_assignmet -to <*node_list*> -from {*}

set_multicycle_path

This multi-cycle path constraint is specified in the Precision RTL Synthesis software as shown in Example 9–7.

Example 9–7. Using the set_multicycle_path Constraint

```
set_multicycle_path <multiplier_value> [-start] [-end] -to <to_node_list> -from
<from_node_list> -reset_path
```

The node lists can contain clocks, ports, instances, and pins. Multiple elements in the list can be represented using wildcards such as "`*`" and "`?`." Paths without multicycle path definitions are identical to paths with multipliers of 1. To add one additional cycle to the datapath, use a multiplier value of 2. The option `start` is to indicate that source clock cycles should be considered for the multiplier. The option `end` is to indicate that destination clock cycles should be considered for the multiplier. The default is to reference the end clock.

This setting in Precision RTL Synthesis software is mapped to a `set_multicycle_assignment` setting in the Quartus II software.

The node lists represent top-level ports and/or nets connected to instances (end points of timing assignments). The node lists can contain wildcards; the Quartus II software automatically expands all wildcards. The Quartus II software does not support bus notation as A[7:4] in the node list.

If you use the `from` or `to` option without using both options, the Precision RTL Synthesis command is converted to a Quartus II command using wildcards. Table 9–4 lists the `set_multicycle_path` constraints in the Precision RTL Synthesis software and the Quartus II software equivalent

Table 9–4. set_multicycle_path Constraints

Precision RTL Synthesis Assignment	Quartus II Equivalent
set_multicycle_path -from <*from_node_list*> <*value*>	set_multicycle_assignment -to {*} -from <*node_list*> <*value*>
set_multicycle_path -to <*to_node_list*> <*value*>	set_multicycle_assignmet -to <*node_list*> -from {*} <*value*>

The Quartus II software does not support the `rise` or `fall` options on this assignment.

The Quartus II software does not support multicycle path with a `through` path specification. Any setting in Precision RTL Synthesis software with a `-through` specification cannot be mapped to a setting in the Quartus II software.

Megafunctions & Architecture-Specific Features

Altera provides parameterizable megafunctions including LPM, device-specific Altera megafunctions, intellectual property (IP) available as Altera MegaCore functions, and IP available through the Altera Megafunction Partners Program (AMPP^{SM}). You can use megafunctions by instantiating them in your HDL code or inferring them from generic HDL code.

For more details about specific Altera megafunctions, refer to the Quartus II Help. For more information about IP functions, consult the appropriate IP documentation.

If you want to instantiate a megafunction in your HDL code, you can use the MegaWizard Plug-In Manager to parameterize the function or you can instantiate the function using the port and parameter definition. The MegaWizard Plug-In Manager provides a graphical interface for customizing and parameterizing any available megafunction for the design. The "Instantiating Altera Megafunctions Using the MegaWizard Plug-In Manager" section describes the MegaWizard flow with the Precision RTL Synthesis software.

The Precision RTL Synthesis software automatically recognizes certain types of HDL code and infers the appropriate megafunction when a megafunction will provide optimal results. The Precision RTL Synthesis

software also provides options to control inference of certain types of megafunctions, as described in the "Inferring Altera Megafunctions from HDL Code" section.

For a detailed information about instantiating versus inferring megafunctions, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*. This chapter also provides details about using the MegaWizard Plug-In Manager in the Quartus II software and explains the files generated by the wizard. In addition, the chapter provides coding style recommendations and examples for inferring megafunctions in Altera devices.

Instantiating Altera Megafunctions Using the MegaWizard Plug-In Manager

When you use the MegaWizard Plug-In Manager to set up and parameterize a megafunction and to create a custom megafunction variation, the MegaWizard creates either a VHDL or Verilog HDL wrapper file. This file instantiates the megafunction (a black-box methodology) or, for some megafunctions, generates a fully synthesizeable netlist for improved results using EDA synthesis tools such as the Precision RTL Synthesis software (a clear-box methodology).

Clear-Box Methodology

You can use the MegaWizard Plug-In Manager to generate a fully synthesizable netlist. This flow is referred to as a clear-box methodology because the Precision RTL Synthesis software can "see" into the megafunction file. The clear box feature enables the synthesis tool to report more accurate resource utilization and timing estimates, taking better advantage of timing driven optimization.

This clear-box feature of the MegaWizard Plug-In Manager is turned on by choosing the **Generate clear box body (for EDA tools only)** in the **MegaWizard Plug-In Manager** for certain megafunctions. If the option does not appear, then clear box models are not supported for the selected megafunction. Turning on this option causes the MegaWizard Plug-In Manager to generate a synthesizable clear box netlist instead of the megafunction wrapper file described in the "Black-Box Methodology" section.

Using MegaWizard-Generated Verilog HDL Files for Clear Box Megafunction Instantiation

The MegaWizard Plug-In Manager generates a Verilog HDL instantiation template file <*output*>**_inst.v** for use in your Precision RTL Synthesis design. This file can help you instantiate the megafunction clear box netlist file, <*output file*>**.v**, in your top-level design. Include the megafunction clear box netlist file in your Precision RTL Synthesis project and the information gets passed to the Quartus II software in the Precision RTL Synthesis-generated EDIF output file.

Using MegaWizard-Generated VHDL Files for Clear Box Megafunction Instantiation

The MegaWizard Plug-In Manager generates a VHDL Component declaration file <***output file***>**.cmp** and a VHDL Instantiation template file <***output file***>**_inst.vhd** for use in your design. These files help to instantiate the megafunction clear box netlist file, <***output file***>.**vhd**, in your top-level design. Include the megafunction clear box netlist file in your Precision RTL Synthesis project and the information gets passed to the Quartus II software in the Precision RTL Synthesis-generated EDIF output file.

Black-Box Methodology

Using the MegaWizard Plug-In Manager-generated wrapper file is referred to as a black-box methodology because the megafunction is treated as a black box in the Precision RTL Synthesis software. The black-box wrapper file is generated by default in the MegaWizard Plug-In Manager and is available for all megafunctions.

The black-box methodology does not allow the synthesis tool any visibility into the function module and so does not take full advantage of the synthesis tool's timing driven optimization.

Using MegaWizard Plug-In Manager-Generated Verilog HDL Files for Black-Box Megafunction Instantiation

The MegaWizard Plug-In Manager generates a Verilog HDL instantiation template file <***output file***>**_inst.v** and a hollow-body black-box module declaration <***output file***>**_bb.v** for use in your Precision RTL Synthesis design. The instantiation template file helps to instantiate the megafunction variation wrapper file, <***output file***>**.v**, in your top-level design. Add the hollow-body black-box module declaration <***output file***>**_bb.v** to your Precision RTL Synthesis project to describe the port connections of the black box.

You do not have to include the megafunction variation wrapper file <*output file*>**.v** in your Precision RTL Synthesis project, but you must add it to your Quartus II project along with your Precision RTL synthesis-generated EDIF netlist. Alternately, you can include the file in your Precision project and then right-click on the file in the input file list, and select **Properties**. In the input file properties dialog, turn on **Exclude file from Compile Phase** and click **OK**. When this option is on, the Precision RTL Synthesis software does not compile this file and the tool makes a copy of the file in the appropriate directory so that the Quartus II software can compile the design during placement and routing.

Using MegaWizard Plug-In Manager-Generated VHDL Files for Black-Box Megafunction Instantiation

The MegaWizard Plug-In Manager generates a VHDL Component declaration file <*output file*>**.cmp** and a VHDL Instantiation template file <*output file*>**_inst.vhd** for use in your Precision RTL Synthesis design. These files can help you instantiate the megafunction variation wrapper file, <*output file*>.**vhd**, in your top-level design.

You do not have to include the megafunction variation wrapper file, <*output file*>.**vhd**, in your Precision RTL synthesis project, but you must add it to your Quartus II project with your Precision RTL synthesis-generated EDIF netlist. Alternately, you can include the file in your Precision project and then right-click on the file in the input file list, and select **Properties**. In the input file properties dialog, turn on **Exclude file from Compile Phase** and click **OK**. When this option is on, the Precision RTL Synthesis software does not compile this file and the tool makes a copy of the file in the appropriate directory so that the Quartus II software can compile the design during placement and routing.

Inferring Altera Megafunctions from HDL Code

The Precision RTL Synthesis software automatically recognizes certain types of HDL code and maps arithmetic and relational operators, and memory (RAM and ROM), to efficient technology-specific implementations. This allows for the use of technology-specific resources to implement these structures by inferring the appropriate Altera megafunction when a megafunction will provide optimal results. In some cases, the Precision RTL Synthesis software has options that you can use to disable or control inference.

For coding style recommendations and examples for inferring megafunctions in Altera devices, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*, and the *Precision Synthesis Style Guide* in the Precision RTL Synthesis Manuals Bookcase in the Help menu.

Multipliers

The Precision RTL Synthesis software detects multipliers in HDL code and maps them directly to device atoms to implement the multiplier in the appropriate type of logic. The Precision RTL Synthesis software also allows you to control the device resources that are used to implement individual multipliers, as described in the following section.

Controlling DSP Block Inference for Multipliers

By default, the Precision RTL Synthesis software uses DSP blocks available in the Stratix series of devices to implement multipliers. The default setting is **AUTO**, to allow Precision RTL Synthesis software the flexibility to choose between logic look-up tables (LUTs) and DSP blocks, depending on the size of the multiplier. You can use the Precision RTL Synthesis GUI or HDL attributes to direct the mapping to only logic elements or to only DSP blocks. The options for multiplier mapping in the Precision RTL Synthesis software are shown in Table 9–5.

Table 9–5. Options for DEDICATED_MULT Parameter to Control Multiplier Implementation in Precision RTL Synthesis

Value	Description
ON	Use only DSP blocks to implement multipliers, regardless of the size of the multiplier.
OFF	Use only logic (LUTs) to implement multipliers.
AUTO	Use logic (LUTs) and DSP blocks to implement multipliers depending on the size of the multipliers.

Using the GUI

Perform the following steps to set the **Use Dedicated Multiplier** option in the Precision RTL Synthesis GUI:

1. Compile the design.
2. In the Design Hierarchy browser, right-click the operator for the desired multiplier and click **Use Dedicated Multiplier**.

Using Attributes

To control the implementation of a multiplier in your HDL code, use the dedicated_mult attribute with the appropriate value from Table 9–5 as shown in Example 9–8 and Example 9–9.

Example 9–8. Setting the dedicated_mult Attribute in Verilog HDL

```
//synthesis attribute <signal name> dedicated_mult <value>
```

Example 9–9. Setting the dedicated_mult Attribute in VHDL

```
ATTRIBUTE dedicated_mult: STRING;
ATTRIBUTE dedicated_mult OF <signal name>: SIGNAL IS <value>;
```

The dedicated_mult attribute can be applied to signals and wires; it does not work when applied to a register. This attribute can be applied only to simple multiplier code such as a = b * c.

Some signals for which dedicated_mult attribute is set may be synthesized away by the Precision RTL Synthesis software because of design optimization. In such cases, if you want to force the implementation, you should preserve the signal by setting the preserve_signal attribute to TRUE as shown in Example 9–10.

Example 9–10. Setting the preserve_signal Attribute in Verilog HDL

```
//synthesis attribute <signal name> preserve_signal TRUE
```

Example 9–11. Setting the preserve_signal Attribute in VHDL

```
ATTRIBUTE preserve_signal: BOOLEAN;
ATTRIBUTE preserve_signal OF <signal name>: SIGNAL IS TRUE;
```

Example 9–12 and Example 9–13 are examples in Verilog HDL and VHDL of using the dedicated_mult attribute to implement the given multiplier in regular logic in the Quartus II software.

Example 9–12. Verilog HDL Multiplier Implemented in Logic

```
module unsigned_mult (result, a, b);
    output [15:0] result;
    input [7:0] a;
    input [7:0] b;
    assign result = a * b; //synthesis attribute result dedicated_mult OFF
endmodule
```

Example 9–13. VHDL Multiplier Implemented in Logic

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY unsigned_mult IS
    PORT(
        a: IN std_logic_vector (7 DOWNTO 0);
        b: IN std_logic_vector (7 DOWNTO 0);
        result: OUT std_logic_vector (15 DOWNTO 0));
ATTRIBUTE dedicated_mult: STRING;
END unsigned_mult;

ARCHITECTURE rtl OF unsigned_mult IS
    SIGNAL a_int, b_int: UNSIGNED (7 downto 0);
    SIGNAL pdt_int:  UNSIGNED (15 downto 0);
ATTRIBUTE dedicated_mult OF pdt_int: SIGNAL IS "OFF";
BEGIN
    a_int <= UNSIGNED (a);
    b_int <= UNSIGNED (b);
    pdt_int <= a_int * b_int;
    result <= std_logic_vector(pdt_int);
END rtl;
```

Multiplier-Accumulators & Multiplier-Adders

The Precision RTL Synthesis software detects multiply-accumulators or multiply-adders in HDL code and infers an `altmult_accum` or `altmult_add` megafunction so that the logic can be placed in DSP blocks, or maps directly to device atoms to implement the multiplier in the appropriate type of logic.

The Precision RTL Synthesis software supports inference for these functions only if the target device family has dedicated DSP blocks.

The Precision RTL Synthesis software also allows you to control the device resources used to implement multiply-accumulators or multiply-adders in your project or in a particular module. Refer to the **"Controlling DSP Block Inference" on page 9–26** section for more information.

For more information about DSP blocks in Altera devices, refer to the appropriate Altera device family handbook and device-specific documentation. For details about which functions a given DSP block can implement, refer to the DSP Solutions Center on the Altera web site.

For more information about inferring Multiply-Accumulator and Multiply-Adder megafunctions in HDL code, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*, and the *Precision Synthesis Style Guide* in the Precision RTL Synthesis Manuals Bookcase in the Help menu.

Controlling DSP Block Inference

By default the Precision RTL Synthesis software infers the `altmult_add` or `altmult_accum` megafunction as appropriate for your design. These megafunctions allow the Quartus II software the flexibility to choose regular logic or DSP blocks depending on the device utilization and the size of the function.

You can use the `extract_mac` attribute to prevent the inference of an `altumult_add` or `altmult_accum` megafunction in a certain module or entity. The options for this attribute are shown in Table 9–6.

Table 9–6. Options for EXTRACT_MAC Attribute Controlling DSP Implementation

Value	Description
TRUE	The `altmult_add` or `altmult_accum` megafunction is inferred
FALSE	The `altmult_add` or `altmult_accum` megafunction is not inferred

To control inference, use the `extract_mac` attribute with the appropriate value from Table 9–6 in your HDL code as shown in Example 9–14 and Example 9–15.

Example 9–14. Setting the extract_mac Attribute in Verilog HDL

```
//synthesis attribute <module name> extract_mac <value>
```

Example 9–15. Setting the extract_mac Attribute in VHDL

```
ATTRIBUTE extract_mac: BOOLEAN;
ATTRIBUTE extract_mac OF <entity name>: ENTITY IS <value>;
```

To control the implementation of the multiplier portion of a multiply-accumulator or multiply-adder, you must use the `dedicated_mult` attribute as described in the "Controlling DSP Block Inference" section. See that section for syntax details.

Example 9–16 and Example 9–17 use the `extract_mac`, `dedicated_mult`, and `preserve_signal` attributes (in Verilog HDL and VHDL) to implement the given DSP function in logic in the Quartus II software.

Example 9–16. Use of extract_mac, dedicated_mult & preserve_signal in Verilog HDL

```
module unsig_altmult_accum1 (dataout, dataa, datab, clk, aclr, clken);
    input [7:0] dataa, datab;
    input clk, aclr, clken;
    output     [31:0] dataout;

    reg        [31:0] dataout;
    wire       [15:0] multa;
    wire       [31:0] adder_out;

    assign multa = dataa * datab;

    //synthesis attribute multa preserve_signal TRUE
    //synthesis attribute multa dedicated_mult OFF
    assign adder_out = multa + dataout;

    always @ (posedge clk or posedge aclr)
    begin
        if (aclr)
        dataout <= 0;
    else if (clken)
        dataout <= adder_out;
    end

    //synthesis attribute unsig_altmult_accum1 extract_mac FALSE
endmodule
```

Example 9–17. Use of extract_mac, dedicated_mult, and preserve_signal in VHDL

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.std_logic_signed.all;

ENTITY signedmult_add IS
    PORT(
        a, b, c, d: IN STD_LOGIC_VECTOR (7 DOWNTO 0);
        result: OUT STD_LOGIC_VECTOR (15 DOWNTO 0)
    );
    ATTRIBUTE preserve_signal: BOOLEAN;
    ATTRIBUTE dedicated_mult: STRING;
    ATTRIBUTE extract_mac: BOOLEAN;
    ATTRIBUTE extract_mac OF signedmult_add: ENTITY IS FALSE;
END signedmult_add;
```

```
ARCHITECTURE rtl OF signedmult_add IS
    SIGNAL a_int, b_int, c_int, d_int : signed (7 DOWNTO 0);
    SIGNAL pdt_int, pdt2_int : signed (15 DOWNTO 0);
    SIGNAL result_int: signed (15 DOWNTO 0);

    ATTRIBUTE preserve_signal OF pdt_int: SIGNAL IS TRUE;
    ATTRIBUTE dedicated_mult OF pdt_int: SIGNAL IS "OFF";
    ATTRIBUTE preserve_signal OF pdt2_int: SIGNAL IS TRUE;
    ATTRIBUTE dedicated_mult OF pdt2_int: SIGNAL IS "OFF";

BEGIN
    a_int <= signed (a);
    b_int <= signed (b);
    c_int <= signed (c);
    d_int <= signed (d);
    pdt_int <= a_int * b_int;
    pdt2_int <= c_int * d_int;
    result_int <= pdt_int + pdt2_int;
    result <= STD_LOGIC_VECTOR(result_int);
END rtl;
```

RAM & ROM

The Precision RTL Synthesis software detects memory structures in HDL code and converts them to an operator that infers an `altsyncram` or `lpm_ram_dp` megafunction, depending on the device family. The software then places these functions in memory blocks.

The software supports inference for these functions only if the target device family has dedicated memory blocks.

For more information about inferring RAM and ROM megafunctions in HDL code, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*, and the *Precision Synthesis Style Guide* in the Precision RTL Synthesis Manuals Bookcase in the Help menu.

Incremental Compilation & Block-Based Design

As designs become more complex and designers work in teams, a block-based hierarchical or incremental design flow is often an effective design approach. In an incremental compilation flow, you can make changes to part of the design while maintaining the placement and performance of unchanged parts of the design. Design iterations can be made dramatically faster by focusing new compilations on particular design partitions and merging results with the results of previous compilations of other partitions. In a bottom-up or team-based approach, you can perform optimization on individual blocks and then integrate them into a final design and optimize it at the top level.

Using the Precision RTL Synthesis software, you can create different netlist files for different partitions of a design hierarchy. Doing this makes each partition independent of the others for either a top-down or a bottom-up incremental compilation or LogicLock design flow. In either case, only the portions of a design that have been updated must be recompiled during design iterations. You can make changes and resynthesize one partition in a design to create a new netlist without affecting the synthesis results or fitting of other partitions. The following steps show the general top-down compilation flow when using these features of the Quartus II software:

1. Create Verilog HDL or VHDL design files as you do in the regular design flow.
2. Determine which hierarchical blocks you want to treat as separate partitions in your design.
3. Create a project with multiple implementations (or create multiple projects) in the Precision RTL Synthesis software, one for each partition in the design.
4. Disable I/O pad insertion in the implementations for lower-level partitions.
5. Compile and synthesize each implementation or each project in the Precision RTL Synthesis software, and make constraints as in the regular design flow.
6. Import the EDIF netlist and the Tcl file for each partition into the Quartus II software and set up the Quartus II project(s) to use the incremental compilation or LogicLock methodology.
7. Compile your design in the Quartus II software and preserve the compilation results using the post-fit netlist type in incremental compilation or back-annotation in the LogicLock methodology.
8. When you make design or synthesis optimization changes to part of your design, resynthesize only the changed partition to generate the new EDIF netlist and Tcl file. Do not resynthesize the implementations or projects for the unchanged partitions.
9. Import the new EDIF netlist and Tcl file into the Quartus II software and recompile the design in the Quartus II software using the incremental compilation or LogicLock methodology.

For more information about creating partitions and using the incremental compilation in the Quartus II software, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*. For more information about using the LogicLock feature in the Quartus II software, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

Hierarchy & Design Considerations

To ensure the proper functioning of the synthesis flow, you can create separate partitions only for modules, entities, or existing netlist files. In addition, each module or entity must have its own design file. If two different modules are in the same design file but are defined as being part of different partitions, you cannot maintain incremental synthesis because both regions must be recompiled when you change one of the modules.

Altera recommends that you register all inputs and outputs of each partition. This makes logic synchronous and avoids any delay penalty on signals that cross partition boundaries.

If you use boundary tri-states in a lower level block, the Precision RTL Synthesis software pushes the tri-states through the hierarchy to the top level to make use of the tri-state drivers on output pins of Altera devices. Because pushing tri-states requires optimizing through hierarchies, lower level tri-states are not supported with a block-based compilation methodology. You should use tri-state drivers only at the external output pins of the device and in the top-level block in the hierarchy.

For more tips on design partitioning, refer to the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Creating a Design with Separate Netlist Files

The first step in a hierarchical or incremental design flow is to ensure that different parts of your design do not affect each other. Ensure that you have separate netlists for each partition in your design so that you can take advantage of the incremental compilation and LogicLock design flows in the Quartus II software. If the whole design is in one netlist file, changes in one partition affect other partitions because of possible node name changes when you resynthesize the design.

You can create different implementations for each partition in your Precision RTL project, which allows you to switch between partitions without leaving the current project file, or you can create a separate project for each partition if you need separate projects for a bottom-up or team-based design flow.

Create a separate implementation or a separate project for each lower level module and for the top-level design that you want to maintain as a separate EDIF netlist file. Implement black-box instantiations of lower level modules in your top-level implementation or project.

For more information about managing implementations and projects, refer to the *Precision RTL Synthesis User's Manual* in the Precision Manuals Bookcase in the Help menu.

When synthesizing the implementations for lower level modules, perform these steps:

1. Turn off **Add IO Pads** on the **Optimization** page under **Set Options** (Tools menu).
2. Read the HDL files for the modules.

   Modules may include black-box instantiations of lower level modules that are also maintained as separate EDIF files.

3. Add constraints for all partitions in the design.

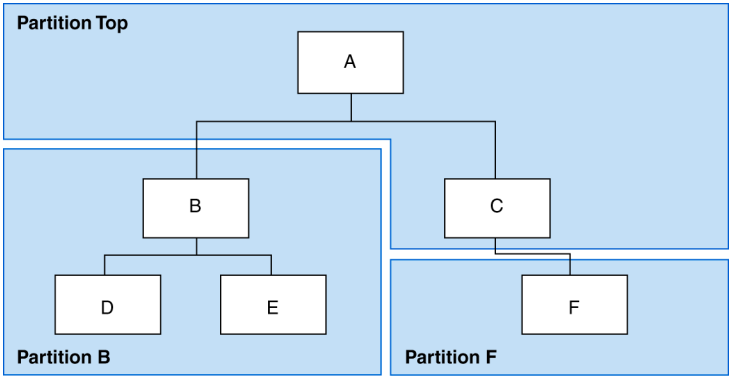
When synthesizing the top-level design implementation, perform these steps:

1. Read the HDL files for top-level designs.
2. Create black boxes for lower level modules in the top-level design.
3. Add constraints.

In a top-down incremental compilation flow, constraints made on lower level modules are not passed to the Quartus II software. Ensure that appropriate constraints are made in the top-level Precision RTL Synthesis project, or in the Quartus II project.

The following sections describe an example of implementing black boxes to create separate EDIF netlists. Figure 9–2 shows an example of a design hierarchy separated into various partitions.

Figure 9–2. Partitions in a Hierarchical Design



In Figure 9–2, the top-level partition contains the top-level block in the design (block A) and the logic that is not defined as part of another partition. In this example, the partition for top-level block A also includes the logic in the C subblock. Because block F is contained in its own partition, it is not treated as part of the top-level partition A. Another separate partition, B, contains the logic in blocks B, D, and E. In a team-based design, different engineers may work on the logic in different partitions. One netlist is created for the top-level module A and its submodule C, another netlist is created for B and its submodules D and E, while a third netlist is created for F. To create multiple EDIF netlist files for this design, follow these steps:

1. Generate an EDIF file for module B. Use **B.v/.vhd**, **D.v/.vhd**, and **E.v/.vhd** as the source files.

2. Generate an EDIF file for module F. Use **F.v/.vhd** as the source file.

3. Generate a top-level EDIF file for module A. Use **A.v/.vhd** and **C.v/.vhd** as the source files. Ensure that you create black boxes for modules B and F, which were optimized separately in the previous steps.

Creating Black Boxes in Verilog HDL

Any design block that is not defined in the project or included in the list of files to be read for a project is treated as a black box by the software. In Verilog HDL, you must provide an empty module declaration for any module that is treated as a black box.

A black-box example for top-level file **A.v** follows. Use this same procedure for any lower level files, which also contain a black box for any module beneath the current level of hierarchy.

Example 9–18. Verilog HDL Black Box for Top-Level File A.v

```
module A (data_in, clk, e, ld, data_out);
    input data_in, clk, e, ld;
    output [15:0] data_out;

    wire [15:0] cnt_out;

    B U1 (.data_in (data_in),.clk(clk), .ld (ld),.data_out(cnt_out));
    F U2 (.d(cnt_out), .clk(clk), .e(e), .q(data_out));

// Any other code in A.v goes here.
endmodule

// Empty Module Declarations of Sub-Blocks B and F follow here.
// These module declarations (including ports) are required for black
// boxes.

module B (data_in, clk, ld, data_out);
    input data_in, clk, ld;
    output [15:0] data_out;
endmodule

module F (d, clk, e, q);
    input [15:0] d;
    input clk, e;
    output [15:0] q;
endmodule
```

Creating Black Boxes in VHDL

Any design block that is not defined in the project or included in the list of files to be read for a project is treated as a black box by the software. In VHDL, you need a component declaration for the black box just like any other block in the design.

A black box for the top-level file **A.vhd** is shown in the following example. Follow this same procedure for any lower level files that also contain a black box or for any block beneath the current level of hierarchy.

Example 9–19. VHDL Black Box for Top-Level File A.vhd

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY A IS
PORT ( data_in : IN INTEGER RANGE 0 TO 15;
    clk, e, ld : IN STD_LOGIC;
    data_out : OUT INTEGER RANGE 0 TO 15);
END A;

ARCHITECTURE a_arch OF A IS
COMPONENT B PORT(
    data_in : IN INTEGER RANGE 0 TO 15;
    clk, ld : IN STD_LOGIC;
    d_out : OUT INTEGER RANGE 0 TO 15);
END COMPONENT;

COMPONENT F PORT(
    d : IN INTEGER RANGE 0 TO 15;
    clk, e: IN STD_LOGIC;
    q : OUT INTEGER RANGE 0 TO 15);
END COMPONENT;

-- Other component declarations in A.vhd go here

signal cnt_out : INTEGER RANGE 0 TO 15;

BEGIN
U1 : B
PORT MAP (
    data_in => data_in,
    clk => clk,
    ld => ld,
    d_out => cnt_out);

U2 : F
PORT MAP (
    d => cnt_out,
    clk => clk,
    e => e,
    q => data_out);

-- Any other code in A.vhd goes here

END a_arch;
```

After you complete the steps outlined in this section, you have different EDIF netlist files for each partition of the design. These files are ready for use in the incremental compilation or LogicLock design methodologies in the Quartus II software.

Creating Quartus II Projects for Multiple EDIF Files

The Precision RTL Synthesis software creates a Tcl file for each EDIF file, and provides the Quartus II software with the appropriate constraints and information to set up a project. For details about using the Tcl script generated by the Precision RTL software to set up your Quartus II project and to pass your top-level constraints, refer to *"Running the Quartus II Software Manually Using the Precision RTL Synthesis-Generated Tcl Script" on page 9–14*.

Depending on your design methodology, you can create one Quartus II project for all EDIF netlists (a top-down flow), or a separate Quartus II project for each EDIF netlist (a bottom-up flow). In a top-down compilation design flow, you create design partition assignments and floorplan location assignments for each partition in the design within a single Quartus II project. This methodology provides the best quality of results and performance preservation during incremental changes to your design. You may need to use a bottom-up design flow when each partition must be optimized separately, such as in certain team-based design flows.

To perform a bottom-up compilation in the Quartus II software, create separate Quartus II projects and import each design partition into a top-level design using the incremental compilation export and import features to maintain placement results. Alternately, you can use the LogicLock design methodology to import each lower-level partition and maintain placement results.

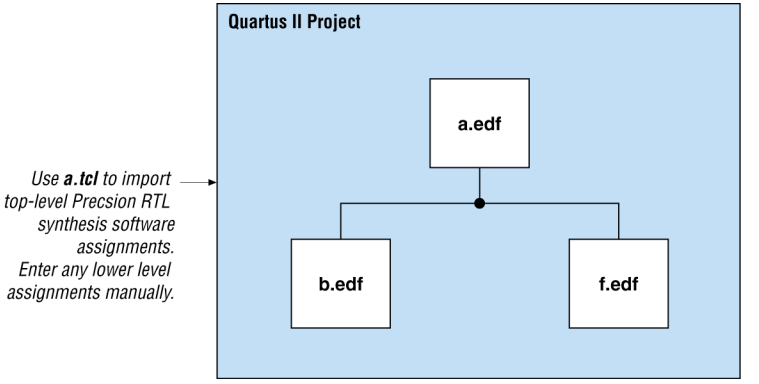
The following sections describe how to create the Quartus II projects for these two design flows.

Creating a Single Quartus II Project for a Top-Down Incremental Compilation Flow

Use the <*top-level project*>**.tcl** file generated for the top-level partition to create your Quartus II project and import all the netlists into this one Quartus II project for an incremental compilation flow. You can optimize all partitions within the single Quartus II project and take advantage of the performance preservation and compilation time reduction that incremental compilation provides. Figure 9–3 shows the design flow for the example design in Figure 9–2.

All the constraints from the top-level implementation are passed to the Quartus II software in the top-level Tcl file, but any constraints made only in the lower level implementations within the Precision RTL Synthesis software are not forward-annotated. Enter these constraints manually in your Quartus II project.

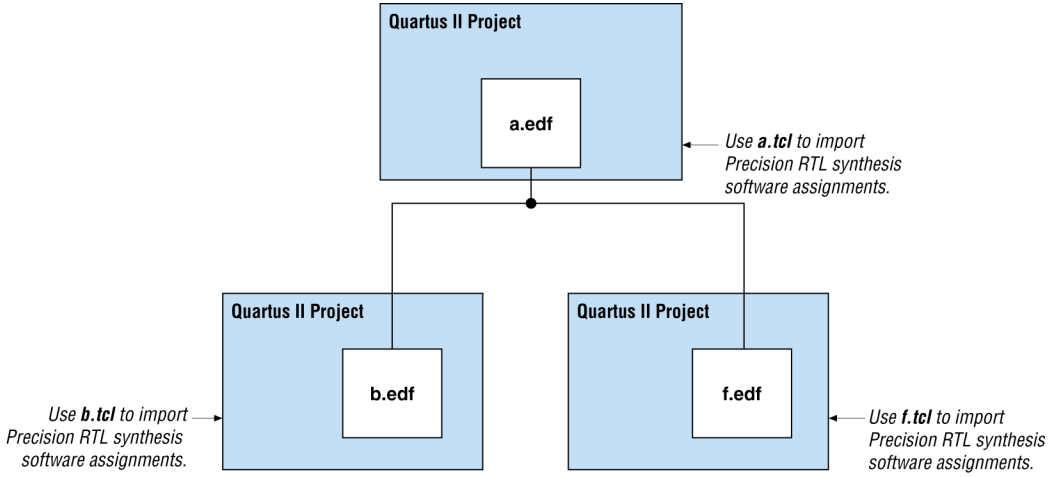
Figure 9–3. Design Flow Using Multiple EDIF Files with One Quartus II Project



Creating Multiple Quartus II Projects for a Bottom-Up Flow

Use the Tcl files generated by the Precision RTL Synthesis software for each Precision RTL Synthesis software implementation or project to generate multiple Quartus II projects, one for each partition in the design. Each designer in the project can optimize their block separately in the Quartus II software and export the placement of their blocks using the incremental compilation or LogicLock design methodology. Designers should create a LogicLock region for each block; the top-level designer should then import all the blocks and assignments into the top-level project. Figures 9–4 shows the design flow for the example design in Figure 9–2.

Figure 9–4. Design Flow: Using Multiple EDIF Files with Multiple Quartus II Projects



Conclusion

Advanced synthesis is an important part of the design flow. The Mentor Graphics Precision RTL Synthesis software and Quartus II design flow allows you to control how to prepare your design files for the Quartus II place-and-route process. This allows you to improve performance and optimize a design for use with Altera devices. Several of the methodologies outlined in this chapter can help you optimize a design to achieve performance goals and save design time.

10. Mentor Graphics LeonardoSpectrum Support

QII51010-6.0.0

Introduction

As programmable logic devices (PLDs) become more complex and require increased performance, advanced synthesis has become an important part of the design flow. Combining HDL coding techniques, Mentor Graphics LeonardoSpectrum™ software constraints, and Quartus® II options provide the performance increase needed for today's system-on-a-programmable-chip (SOPC) designs.

The LeonardoSpectrum software is a mature synthesis tool supporting legacy devices and many current devices. The LeonardoSpectrum software version 2005b supports the Stratix® II, Stratix, Stratix GX, Cyclone™ II, Cyclone, MAX® II, MAX series, APEX™ series, FLEX® series, and ACEX® series device families. Altera® recommends using the advanced Precision Synthesis software for new designs in new device families.

For more information about Precision RTL Synthesis, refer to the *Mentor Graphics Precision RTL Synthesis Support* chapter in volume 1 of the *Quartus II Handbook*.

This chapter documents key design methodologies and techniques for achieving better performance in Altera devices using the LeonardoSpectrum and Quartus II design flow.

This chapter assumes that you have set up, licensed, and are familiar with the LeonardoSpectrum software.

To obtain and license the LeonardoSpectrum software, refer to the Mentor Graphics web site at **www.mentor.com**. For information about installing the LeonardoSpectrum software and setting up your working environment, refer to the *LeonardoSpectrum Installation Guide* and the *LeonardoSpectrum User's Manual*.

Design Flow

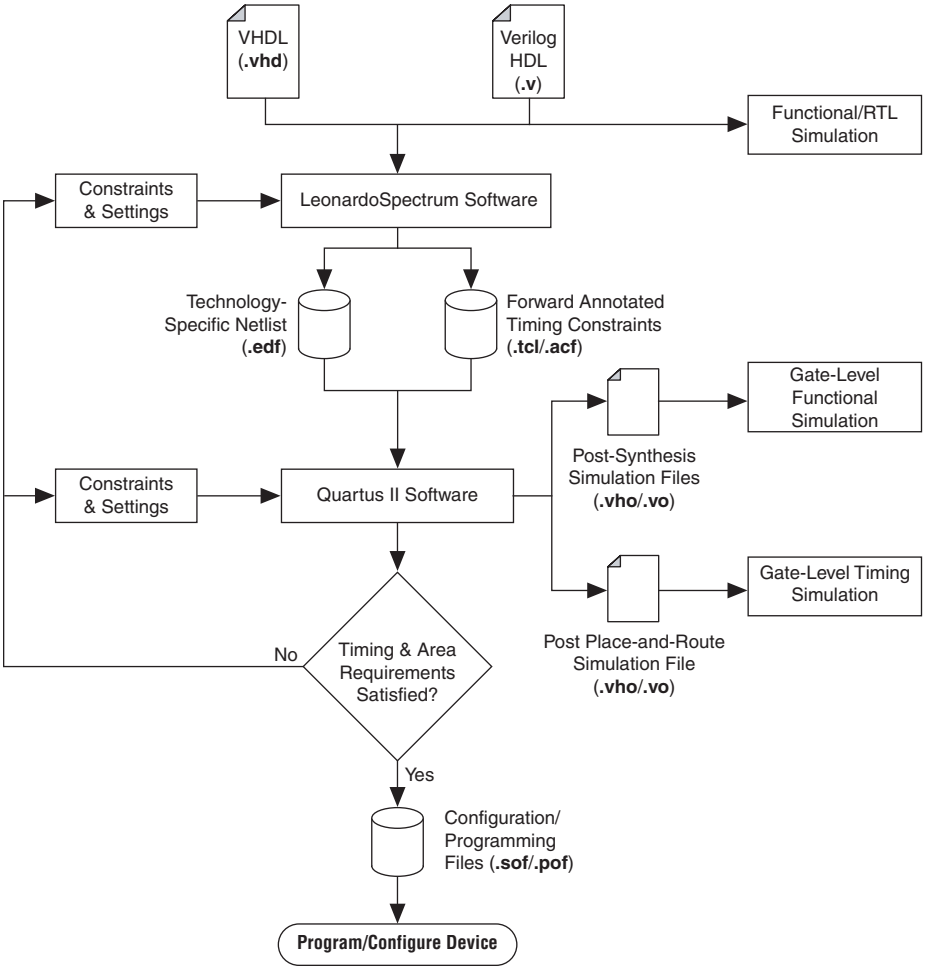
Following are the basic steps in a LeonardoSpectrum-Quartus II design flow:

1. Create Verilog HDL or VHDL design files in the LeonardoSpectrum software or a text editor.
2. Import the Verilog HDL or VHDL design files into the LeonardoSpectrum software for synthesis.
3. Select a target device and add timing constraints and compiler directives to help optimize the design during synthesis.
4. Synthesize the project in the LeonardoSpectrum software.
5. Create a Quartus II project and import the technology-specific EDIF Input File (.**edf**) netlist and the Tcl Script File (.**tcl**) generated by the LeonardoSpectrum software into the Quartus II software for placement and routing, and for performance evaluation.
6. After obtaining place-and-route results that meet your needs, configure or program the Altera device.

Figure 10–1 shows the recommended design flow using the LeonardoSpectrum and Quartus II software.

If your area and timing requirements are satisfied, use the programming files generated from the Quartus II software to program or configure the Altera device. As shown in Figure 10–1, if the area or timing requirements are not met, change the constraints in the LeonardoSpectrum software and re-run the synthesis. Repeat the process until the area and timing requirements are met. You can also use other Quartus II software options and techniques to meet the area and timing requirements.

Figure 10–1. Recommended Design Flow Using LeonardoSpectrum & Quartus II Software



The LeonardoSpectrum software supports both VHDL and Verilog HDL source files. With the appropriate license, it also supports mixed synthesis, allowing a combination of VHDL and Verilog HDL source files.

After synthesis, the LeonardoSpectrum software produces several intermediate and output files. Table 10–1 lists these file extensions with a short description of each file.

Table 10–1. LeonardoSpectrum Intermediate & Output Files

File Extension(s)	File Description
.xdb	Technology-independent register transfer level (RTL) netlist file that can only be read by the LeonardoSpectrum software.
.edf	Technology-specific output netlist in electronic design interchange format (EDIF).
.acf/**.tcl** *(1)*	Forward-annotated constraint file containing constraints and assignments.

Note to Table 10–1:

(1) An assignment and configuration (**.acf**) file is created only for ACEX 1K, FLEX series, and MAX series devices. The assignment and configuration file is generated for backward compatibility with the MAX+PLUS® II software. A Tcl Script File (**.tcl**) is generated for the Quartus II software which also contains Tcl commands to create a Quartus II project.

Altera recommends that you do not use project directory names that include spaces. Some file operations in the LeonardoSpectrum software do not work correctly if the path name contains spaces.

Specify timing constraints and compiler directives for the design in the LeonardoSpectrum software, or in a constraint file (**.ctr**). Many of these constraints are forward-annotated in the Tcl file for use by the Quartus II software.

The LeonardoInsight™ Schematic Viewer is an add-on graphical tool for schematic views of the technology-independent RTL netlist (**.xdb**) and the technology-specific gate-level results. You can use the Schematic Viewer to visually analyze and debug the design. It also supports cross probing between the RTL and gate-level schematics, the design browser, and the source code in the HDLInventor™ text editor.

Optimization Strategies

You can configure most general settings in the **Quick Setup** tab in the LeonardoSpectrum user interface. Other Flow tabs provide additional options, and some Flow tabs include multiple Power tabs (at the bottom of the screen) with still more options. Advanced optimization options in the LeonardoSpectrum software include timing-driven synthesis, encoding style, resource sharing, and mapping I/O registers.

Timing-Driven Synthesis

The LeonardoSpectrum software supports timing-driven synthesis through user-assigned timing constraints to optimize the performance of the design. Setting constraints in the LeonardoSpectrum software are straightforward. Constraints such as clock frequency can be specified globally or for individual clock signals. The following sections describe how to set the various types of timing constraints in the LeonardoSpectrum software.

The timing constraints described in the "Global Power Tab" section are set in the **Constraints** Flow tab. In this tab, there are Power tabs at the bottom, such as **Global** and **Clock**, for setting various constraints.

Global Power Tab

The **Global** tab is the default Power tab in the **Constraints** Flow tab. Specify the global clock frequency here. The **Clock Frequency** on the **Quick Setup** tab is equivalent to the **Registers to Registers** delay setting. You can also specify the following: **Input Ports to Registers**, **Registers to Output Ports**, and **Inputs to Outputs** delays that correspond to global t_{SU}, t_{CO}, and t_{PD} requirements, respectively, in the Quartus II software. The timing diagram on this tab reflects the settings you have made.

Clock Power Tab

You can set various constraints for each clock in your design. First, select the clock name in the **Clock(s)** window. The clock names appear after the design is read from the **Input** Flow tab. Configure settings for that particular clock and click **Apply**. If necessary, you can also set the **Duty Cycle** to a value other than the default 50%. The timing diagram shows these settings.

If a clock has an **Offset** from the main clock, which is considered to be time "`0`", this constraint corresponds to the `OFFSET_FROM_BASE_CLOCK` setting in the Quartus II software.

You can specify the pin number for the clock input pin in the **Pin Location** field. This pin number is passed to the Quartus II software for place-and-route, but does not affect synthesis in the LeonardoSpectrum software.

Input & Output Power Tabs

Configure settings for individual input or output pins in the **Input** and **Output** tabs. First, select a name in the **Input Ports** or **Output Ports** window. The names appear after the design is read from the **Input** Flow tab. Then make the setting for that pin as described below.

The **Arrival Time** setting indicates that the input signal arrives a specified time after the rising clock edge (time "0"). This setting constrains the path from the pin to the first register by including the arrival time in the total delay, and corresponds to the `EXTERNAL_INPUT_DELAY` assignment in the Quartus II software.

The **Required Time** setting indicates the maximum delay after time "0" that the output signal should arrive at the output pin. This setting directly constrains the register to output delay, and corresponds with the `EXTERNAL_OUTPUT_DELAY` assignment in the Quartus II software.

Specify the pin number for the I/O pin in the **Pin Location** field. This pin number is passed to the Quartus II software for place-and-route, but does not affect synthesis in the LeonardoSpectrum software.

Other Constraints

The following sections describe other constraints that can be set with the LeonardoSpectrum user interface.

Encoding Style

The LeonardoSpectrum software encodes state machines during the synthesis process. To improve performance when coding state machines, separate state machine logic from all arithmetic functions and data paths. Once encoded, a design cannot be re-encoded later in the optimization process. You must follow a particular VHDL or Verilog HDL coding style for the LeonardoSpectrum software to identify the state machine.

Table 10–2 shows the state machine encoding styles supported by the LeonardoSpectrum software.

Table 10–2. State Machine Encoding Styles in the LeonardoSpectrum Software

Style	Description
Binary	Generates state machines with the fewest possible flipflops. Binary state machines are useful for area-critical designs when timing is not the primary concern.
Gray	Generates state machines where only one flipflop changes during each transition. Gray-encoded state machines tend to be glitchless.
One-hot	Generates state machines containing one flipflop for each state. One-hot state machines provide the best performance and shortest clock-to-output delays. However, one-hot implementations are usually larger than binary implementations.
Random	Generates state machines using random state machine encoding. Only use random state machine encoding when no other implementation achieves the desired results.
Auto (default)	Implements binary or one-hot encoding, depending on the size of enumerated types in the state machine.

The **Encoding Style** setting is created in the **Input** Flow tab. It instructs the software to use a particular state machine encoding style for all state machines. The default **Auto** selection implements binary or one-hot encoding, depending on the size of enumerated types in the state machine.

To ensure proper recognition and improve performance when coding state machines, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook* for design guidelines.

Resource Sharing

You can also enable the **Resource Sharing** setting in the **Input** Flow tab. This setting allows optimization to reduce device resources. You should generally leave this setting turned on.

Mapping I/O Registers

The **Map I/O Registers** option is located in the **Technology** Flow tab. The **Map I/O Registers** option applies to Altera FPGAs containing I/O cells (IOCs) or I/O elements (IOE). If the option is turned on, input or output registers are moved into the device's I/O cells for faster setup or clock-to-output times.

Timing Analysis with the Leonardo-Spectrum Software

The LeonardoSpectrum software reports successful synthesis with an information message in the **Transcript** or **Information** window. Estimated device usage and timing results are reported in the Device Utilization section of this window. Figure 10–2 shows an example of a LeonardoSpectrum compilation report.

Figure 10–2. LeonardoSpectrum Compilation Report

```
************************************************
Device Utilization for EP20K200EQC208
************************************************
Resource                 Used    Avail    Utilization
-------------------------------------------------------
IOs                      22      136       16.18%
LCs                      114     8320       1.37%
Memory Bits              0       106496     0.00%


-------------------------------------------------
                         Clock Frequency Report

        Clock                 : Frequency
      ------------------------------------


        clk                   : 52.2 MHz
        clk2                  : 149.5 MHz

                         Critical Path Report
```

The LeonardoSpectrum software estimates the timing results based on timing models. The LeonardoSpectrum software has no information about how the design is placed and routed in the Quartus II software, so it cannot report accurate routing delays. Additionally, if the design includes any black-boxed Altera-specific functions, the LeonardoSpectrum software does not report timing information for these functions.

Final timing results are generated by the Quartus II software and are reported separately in the **Transcript** or **Information** window if the **Run Integrated Place and Route** option is turned on. Refer to "Integration with the Quartus II Software" on page 10–10 for more information.

Exporting Designs Using NativeLink Integration

You can use NativeLink® integration to integrate the LeonardoSpectrum software and the Quartus II software with a single GUI for both the synthesis and place-and-route operations. NativeLink integration allows you to run the Quartus II software from within the LeonardoSpectrum software GUI, or to run the LeonardoSpectrum software from within the Quartus II software GUI for device families supported in the Quartus II software.

Generating Netlist Files

The LeonardoSpectrum software generates an EDIF netlist file readable as an input file in the Quartus II software for place-and-route. Select the EDIF file option name in the **Output** Flow tab. The EDIF netlist is also generated if the **Auto** option is turned on in the **Output** Flow tab.

Including Design Files for Black-Boxed Modules

If the design has black-boxed megafunctions, be sure to include the MegaWizard® Plug-In Manager-generated custom megafunction variation design file in the Quartus II project directory, or add it to the list of project files for place-and-route.

Passing Constraints with Scripts

The LeonardoSpectrum software can write out a Tcl file called <***project name***>**.tcl**. This file contains commands to create a Quartus II project along with constraints and other assignments. To output a Tcl script, turn on the **Write Vendor Constraint Files** option in the **Output** Flow tab.

To create and compile a Quartus II project using the Tcl file generated from the LeonardoSpectrum software, perform the following steps in the Quartus II software:

1. Place the EDIF netlist files and Tcl scripts in the same directory.
2. On the View menu, point to Utility, and click **Tcl Console** to open the Quartus II Tcl Console.
3. Type `source` <*path*>/<*project name*>`.tcl` ↵, at a **Tcl Console** command prompt.
4. On the File menu, click **Open Project** to open the new project. On the Processing menu, click **Start Compilation**.

Integration with the Quartus II Software

The **Place And Route** section in the **Quick Setup** tab allows you to launch the Quartus II software from within the LeonardoSpectrum software. Turn on the **Run Integrated Place and Route** option to start the compilation using the Quartus II software to show the fitting and performance results. You can also run the place-and-route software by turning on the **Run Quartus** option on the **Physical** Flow tab and clicking **Run PR**.

To use integrated place-and-route software, on the Options menu, point to Place and Route Path and click **Tools**, and specify the location of the Quartus II software executable file (browse to <*Quartus II software installation directory*>**/bin)**.

Guidelines for Altera Megafunctions & LPM Functions

Altera provides parameterizable megafunctions ranging from simple arithmetic units, such as adders and counters, to advanced phase-locked loop (PLL) blocks, multipliers, and memory structures. These functions are performance-optimized for Altera devices. Megafunctions include the library of parameterized modules (LPM), device-specific megafunctions such as PLLs, LVDS, and digital signal processing (DSP) blocks, intellectual property (IP) available as Altera MegaCore® functions, and IP available through the Altera Megafunction Partners Program (AMPP^{sm}).

Some IP cores require that you synthesize them in the LeonardoSpectrum software. Refer to the user guide for the specific IP.

There are two methods for handling megafunctions in the LeonardoSpectrum software: inference and instantiation.

The LeonardoSpectrum software supports inferring some of the Altera megafunctions, such as multipliers, DSP functions, and RAM and ROM blocks. The LeonardoSpectrum software supports all Altera megafunctions through instantiation.

Instantiating Altera Megafunctions

There are two methods of instantiating Altera megafunctions in the LeonardoSpectrum software. The first and least common method is to directly instantiate the megafunction in the Verilog HDL or VHDL code. The second method, to maintain target technology awareness, is to use the MegaWizard Plug-In Manager in the Quartus II software to setup and parameterize a megafunction variation. The megafunction wizard creates a wrapper file that instantiates the megafunction. The advantage of using the megafunction wizard in place of the instantiation method is the

megafunction wizard properly sets all the parameters and you do not need the library support required in the direct instantiation method. This is referred to as the black box methodology.

Altera recommends using the megafunction wizard to ensure that the ports and parameters are set correctly.

When directly instantiating megafunctions, see the Quartus II Help for a list of the ports and parameters.

Inferring Altera Memory Elements

The LeonardoSpectrum software can infer memory blocks from Verilog HDL or VHDL code. When the LeonardoSpectrum software detects a RAM or ROM from the style of the RTL code at a technology-independent level, it then maps the element to a generic module in the RTL database. During the technology-mapping phase of synthesis, the LeonardoSpectrum software maps the generic module to the most optimal primitive memory cells, or Altera megafunction, for the target Altera technology.

For more information about inferring RAM and ROM megafunctions, including examples of VHDL and Verilog HDL code, see the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

Inferring RAM

The LeonardoSpectrum software supports RAM inference for various device families. The restrictions for the LeonardoSpectrum software to successfully infer RAM in a design are listed below:

- The write process must be synchronous
- The read process can be asynchronous or synchronous depending on the target Altera architecture
- Resets on the memory are not supported

Table 10–3 shows a summary of the minimum memory sizes and minimum address widths for inferring RAM in various device families.

To disable RAM inference, set the `extract_ram` and `infer_ram` variables to "false." On the Tools menu, click **Variable Editor** to enter the value "false" when synthesizing in the user interface with the Advanced Flow tabs, or add the commands `set extract_ram false` and `set infer_ram false` to your synthesis script.

Table 10–3. Inferring RAM Summary

	Stratix II, Stratix, Stratix GX & Cyclone Series	APEX Series, Excalibur & Mercury	FLEX 10KE & ACEX 1K
RAM primitive	`altsyncram`	`altdpram`	`altdpram`
Minimum RAM size	2 bits	64 bits	128 bits
Minimum address width	1 bit	4 bits	5 bits

Inferring ROM

You can implement ROM behavior in HDL source code with `CASE` statements or specify the ROM as a table. The LeonardoSpectrum software infers both synchronous and asynchronous ROM depending on the target Altera device. For example, memory for the Stratix series devices must be synchronous to be inferred.

To disable ROM inference, set the `extract_rom` variable to "false." To enter the value "false" when synthesizing in the user interface with the **Advanced Flow** tabs, on the Tools menu, click **Variable Editor**, or add the commands `set extract_rom false` to your synthesis script.

Inferring Multipliers & DSP Functions

Some Altera devices include dedicated DSP blocks optimized for DSP applications. The following Altera megafunctions are used with DSP block modes:

- `lpm_mult`
- `altmult_accum`
- `altmult_add`

You can instantiate these megafunctions in the design or have the LeonardoSpectrum software infer the appropriate megafunction by recognizing a multiplier, multiplier-accumulator (MAC), or multiplier-adder in the design. The Quartus II software maps the functions to the DSP blocks in the device during place-and-route.

For more information about inferring multipliers and DSP functions, including examples of VHDL and Verilog HDL code, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of *The Quartus II Handbook*.

Simple Multipliers

The `lpm_mult` megafunction implements the DSP block in the simple multiplier mode. The following functionality is supported in this mode:

- The DSP block includes registers for the input and output stages, and an intermediate pipeline stage
- Signed and unsigned arithmetic is supported

Multiplier Accumulators

The `altmult_accum` megafunction implements the DSP block in the multiply-accumulator mode. The following functionality is supported in this mode:

- The DSP block includes registers for the input and output stages, and an intermediate pipeline stage
- The output registers are required for the accumulator
- The input and pipeline registers are optional
- Signed and unsigned arithmetic is supported

If the design requires input registers to be used as shift registers, use the black-boxing method to instantiate the `altmult_accum` megafunction.

Multiplier Adders

The LeonardoSpectrum software can infer multiplier adders and map them to either the two-multiplier adder mode or the four-multiplier adder mode of the DSP blocks. The LeonardoSpectrum software maps the HDL code to the correct `altmult_add` function.

The following functionality is supported in these modes:

- The DSP block includes registers for the input and output stages and an intermediate pipeline stage
- Signed and unsigned arithmetic is supported, but support for the Verilog HDL "signed" construct is limited

Controlling DSP Block Inference

In devices that include dedicated DSP blocks, multipliers, multiply-accumulators, and multiply-adders can be implemented either in DSP blocks or in logic. You can control this implementation through attribute settings in the LeonardoSpectrum software.

As shown in Table 10–4, attribute settings in the LeonardoSpectrum software control the implementation of the multipliers in DSP blocks or logic at the signal block (or module), and project level.

Table 10–4. Attribute Settings for DSP Blocks in the LeonardoSpectrum Software *Note (1)*

Level	Attribute Name	Value	Description
Global	extract_mac *(2)*	TRUE	All multipliers in the project mapped to DSP blocks.
		FALSE	All multipliers in the project mapped to logic.
Module	extract_mac *(3)*	TRUE	Multipliers inside the specified module mapped to DSP blocks.
		FALSE	Multipliers inside the specified module mapped to logic.
Signal	dedicated_mult	ON	LPM inferred and multipliers implemented in DSP block.
		OFF	LPM inferred, but multipliers implemented in logic by the Quartus II software.
		LCELL	LPM not inferred, and multipliers implemented in logic by the LeonardoSpectrum software.
		AUTO	LPM inferred, but the Quartus II software automatically maps the multipliers to either logic or DSP blocks based on the Quartus II software place-and-route.

Notes to Table 10–4:

(1) The extract_mac attribute takes precedence over the dedicated_mult attribute.
(2) For devices with DSP blocks, the extract_mac attribute is set to "true" by default for the entire project.
(3) For devices with DSP blocks, the extract_mac attribute is set to "true" by default for all modules.

Global Attribute

You can set the global attribute extract_mac to control the implementation of multipliers in DSP blocks for the entire project. You can set this attribute using the script interface. The script command is:

```
set extract_mac <value>
```

Module Level Attributes

You can control the implementation of multipliers inside a module or component by setting attributes in the Verilog HDL source code. The attribute used is extract_mac. Setting this attribute for a module affects only the multipliers inside that module. The command is:

```
//synthesis attribute <module name> extract_mac <value>
```

The Verilog HDL and VHDL codes samples shown in Examples 10–1 and 10–2 show how to use the `extract_mac` attribute.

Example 10–1. Using Module Level Attributes in Verilog HDL Code

```
module mult_add ( dataa, datab, datac, datad, result);
//synthesis attribute mult_add extract_mac FALSE
// Port Declaration
input [15:0] dataa;
input [15:0] datab;
input [15:0] datac;
input [15:0] datad;

output [32:0] result;

// Wire Declaration
wire [31:0] mult0_result;
wire [31:0] mult1_result;

// Implementation
// Each of these can go into one of the 4 mults in a
// DSP block
assign mult0_result = dataa * `signed datab;
//synthesis attribute mult0_result preserve_signal TRUE

assign mult1_result = datac * datad;

// This adder can go into the one-level adder in a DSP
// block
assign result = (mult0_result + mult1_result);

endmodule
```

Example 10–2. Using Module Level Attributes in VHDL Code

```
library ieee ;
USE ieee.std_logic_1164.all;

USE ieee.std_logic_arith.all;

entity mult_acc is
   generic (size : integer := 4) ;
   port (
      a: in std_logic_vector (size-1 downto 0) ;
      b: in std_logic_vector (size-1 downto 0) ;
      clk : in std_logic;
        accum_out: inout std_logic_vector (2*size downto 0)
   ) ;
   attribute extract_mac : boolean;
   attribute extract_mac of mult_acc : entity is FALSE;
end mult_acc;

architecture synthesis of mult_acc is
    signal a_int, b_int : signed (size-1 downto 0);
    signal pdt_int : signed (2*size-1 downto 0);
    signal adder_out : signed (2*size downto 0);

begin
    a_int <= signed (a);
    b_int <= signed (b);
    pdt_int <= a_int * b_int;
    adder_out <= pdt_int + signed(accum_out);
    process (clk)
    begin
       if (clk'event and clk = '1') then
          accum_out <= std_logic_vector (adder_out);
       end if;
    end process;
end synthesis ;
```

Signal Level Attributes

You can control the implementation of individual `lpm_mult` multipliers by using the `dedicated_mult` attribute as shown below:

```
//synthesis attribute <signal_name> dedicated_mult <value>
```

The `dedicated_mult` attribute is only applicable to signals or wires; it is not applicable to registers.

Table 10–5 shows the supported values for the `dedicated_mult` attribute.

Table 10–5. Values for the dedicated_mult Attribute

Value	Description
ON	LPM inferred and multipliers implemented in DSP block.
OFF	LPM inferred and multipliers synthesized, implemented in logic, and optimized by the Quartus II software. *(1)*
LCELL	LPM not inferred and multipliers synthesized, implemented in logic, and optimized by the LeonardoSpectrum software. *(1)*
AUTO	LPM inferred but the Quartus II software maps the multipliers automatically to either the DSP block or logic based on resource availability.

Note to Table 10–5:

(1) Although both dedicated_mult=OFF and dedicated_mult=LCELLS result in logic implementations, the optimized results in these two cases may differ.

Some signals for which the `dedicated_mult` attribute is set may get synthesized away by the LeonardoSpectrum software due to design optimization. In such cases, if you want to force the implementation, the signal is preserved from being synthesized away by setting the `preserve_signal` attribute to "true."

The `extract_mac` attribute must be set to "false" for the module or project level when using the `dedicated_mult` attribute.

Examples 10–3 and 10–4 are samples of Verilog HDL and VHDL codes, respectively, using the `dedicated_mult` attribute.

Example 10–3. Signal Attributes for Controlling DSP Block Inference in Verilog HDL Code

```
module  mult (AX, AY, BX, BY, m, n, o, p);
input [7:0] AX, AY, BX, BY;
output [15:0] m, n, o, p;
wire [15:0] m_i = AX * AY; // synthesis attribute m_i dedicated_mult ON
// synthesis attribute m_i preserve_signal TRUE
//Note that the preserve_signal attribute prevents
// signal m_i from getting synthesized away
wire [15:0] n_i = BX * BY; // synthesis attribute n_i dedicated_mult OFF
wire [15:0] o_i = AX * BY; // synthesis attribute o_i dedicated_mult AUTO
wire [15:0] p_i = BX * AY; // synthesis attribute p_i dedicated_mult LCELL
// since n_i , o_i , p_i  signals are not preserved,
// they may be synthesized away based on the design
assign m = m_i;
assign n = n_i;
assign o = o_i;
assign p = p_i;
endmodule
```

Example 10–4. Signal Attributes for Controlling DSP Block Inference in VHDL Code

```
library ieee ;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.std_logic_unsigned.all;
USE ieee.std_logic_signed.all;

ENTITY mult is
PORT( AX,AY,BX,BY: IN
    std_logic_vector (17 DOWNTO 0);
m,n,o,p: OUT
    std_logic_vector (35 DOWNTO 0));
attribute dedicated_mult: string;
attribute preserve_signal : boolean
END mult;
ARCHITECTURE struct of mult is

signal m_i, n_i, o_i, p_i : unsigned (35 downto 0);
attribute dedicated_mult of m_i:signal is "ON";
attribute dedicated_mult of n_i:signal is "OFF";
attribute dedicated_mult of o_i:signal is "AUTO";
attribute dedicated_mult of p_i:signal is "LCELL";

begin

m_i <= unsigned (AX) * unsigned (AY);
n_i <= unsigned (BX) * unsigned (BY);
o_i <= unsigned (AX) * unsigned (BY);
p_i <= unsigned (BX) * unsigned (AY);

m <= std_logic_vector(m_i);
n <= std_logic_vector(n_i);
o <= std_logic_vector(o_i);
p <= std_logic_vector(p_i);
end struct;
```

Guidelines for Using DSP Blocks

In addition to the guidelines mentioned earlier in this section, use the following guidelines while designing with DSP blocks in the LeonardoSpectrum software:

- To access all the control signals for the DSP block, such as `sign A`, `sign B`, and `dynamic addnsub`, use the black-boxing technique.
- While performing signed operations, ensure that the specified data width of the output port matches the data width of the expected result. Otherwise, the sign bit may be lost or data may be incorrect because the sign is not extended.
  For example, if the data widths of input `A` and `B` are `width_a` and `width_b`, respectively, then the maximum data width of the result can be (`width_a` + `width_b` +2) for the four-multipliers adder mode. Thus, the data width of the output port should be less than or equal to (`width_a` + `width_b` +2).
- While using the accumulator, the data width of the output port should be equal to or greater than (`width_a` + `width_b`). The maximum width of the accumulator can be (`width_a` + `width_b` + 16). Accumulators wider than this are implemented in logic.
- If the design uses more multipliers than are available in a particular device, you may get a no fit error in the Quartus II software. In such cases, use the attribute settings in the LeonardoSpectrum software to control the mapping of multipliers in your design to DSP blocks or logic.

Block-Based Design with the Quartus II Software

The incremental compilation and LogicLock™ block-based design flows enable users to design, optimize, and lock down a design one section at a time. You can independently create and implement each logic module into a hierarchical or team-based design. With this method, you can preserve the performance of each module during system integration and have more control over placement of your design. To maximize the benefits of the incremental compilation or LogicLock design methodology in the Quartus II software, you can partition a new design into a hierarchy of netlist files during synthesis in the LeonardoSpectrum software.

The LeonardoSpectrum software allows you to create different netlist files for different sections of a design hierarchy. Different netlist files mean that each section is independent of the others. When synthesizing the entire project, only portions of a design that have been updated have to be re-synthesized when you compile the design. You can make changes, optimize, and re-synthesize your section of a design without affecting other sections.

For more information about incremental compilation, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*. For more information about the LogicLock feature, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook.*

Hierarchy & Design Considerations

You must plan your design's structure and partitioning carefully to use incremental compilation and LogicLock features effectively. Optimal hierarchical design practices include partitioning the blocks at functional boundaries, registering the boundaries of each block, minimizing the I/O between each block, separating timing-critical blocks, and keeping the critical path within one hierarchical block.

For more recommendations for hierarchical design partitioning, refer to the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook.*

To ensure the proper functioning of the synthesis tool, you can apply the LogicLock option in the LeonardoSpectrum software only to modules, entities, or netlist files. In addition, each module or entity should have its own design file. If two different modules are in the same design file but are defined as being part of different regions, it is difficult to maintain incremental synthesis since both regions would have to be recompiled when you change one of the modules or entities.

If you use boundary tri-states in a lower-level block, the LeonardoSpectrum software pushes (or "bubbles") the tri-states through the hierarchy to the top-level to take advantage of the tri-state drivers on the output pins of the Altera device. Because bubbling tri-states requires optimizing through hierarchies, lower-level tri-states are not supported with a block-level design methodology. You should use tri-state drivers only at the external output pins of the device and in the top-level block in the hierarchy.

If the hierarchy is flattened during synthesis, logic is optimized across boundaries, preventing you from making LogicLock assignments to the flattened blocks. Altera recommends preserving the hierarchy when compiling the design. In the **Optimize** command of your script, use the **Hierarchy Preserve** command or in the user interface select **Preserve** in the **Hierarchy** section on the **Optimize** Flow tab.

If you are compiling your design with a script, you can use an alternative method for preventing optimization across boundaries. In this case, use the **Auto** hierarchy setting and set the `auto_dissolve` attribute to false on the instances or views that you want to preserve (that is, the modules with LogicLock assignments) using the following syntax:

```
set_attribute -name auto_dissolve -value false
    .work.<block1>.INTERFACE
```

This alternative method flattens your design according to the `auto_dissolve` limits, but does not optimize across boundaries where you apply the attribute as described.

For more details on LeonardoSpectrum attributes and hierarchy levels, refer to the LeonardoSpectrum documentation in the Help menu.

Creating a Design with Multiple EDIF Files

The first stage of a hierarchical design flow is to generate multiple EDIF files, enabling you to take advantage of the incremental compilation flows in the Quartus II software. If the whole design is in one EDIF file, changes in one block affect other blocks because of possible node name changes. You can generate multiple EDIF files either by using the LogicLock option in the LeonardoSpectrum software, or by manually black boxing each block that you want to be part of a LogicLock region.

Once you have created multiple EDIF files using one of these methods, you must create the appropriate Quartus II project(s) to place-and-route the design.

Generating Multiple EDIF Files Using the LogicLock Option

This section describes how to generate multiple EDIF files using the LogicLock option in the LeonardoSpectrum software. When synthesizing a top-level design that includes LogicLock regions, use the following general steps:

1. Read in the Verilog HDL or VHDL source files.
2. Add LogicLock constraints.
3. Optimize and write output netlist files, or choose **Run** Flow.

To set the correct constraints and compile the design, use the following steps in the LeonardoSpectrum software:

1. Switch to the **Advanced** Flow tab instead of the **Quick Setup** tab (Tools menu).
2. Set the target technology and speed grade for the device on the **Technology** Flow tab.
3. Open the input source files on the **Input** Flow tab.
4. Click **Read** on the **Input** Flow tab to read the source files but not begin optimization.
5. Select the **Module** Power tab located at the bottom of the **Constraints** Flow tab.
6. Click on a module to be placed in a LogicLock region in the **Modules** section.
7. Turn on the **LogicLock** option.
8. Type the desired LogicLock region name in the text field under the **LogicLock** option.
9. Click **Apply**.
10. Repeat steps 6-9 for any other modules that you want to place in LogicLock regions.

In some cases, you are prompted to save your LogicLock and other non-global constraints in a Constraints File (**.ctr**) when you click anywhere off the **Constraints** Flow tab. The default name is <*project name*>**.ctr**. This file is added to your **Input** file list, and must be manually included later if you recreate the project.

The command written into the LeonardoSpectrum Information or Transcript Window is the Tcl command that gets written into the CTR file. The format of the "path" for the module specified in the command should be work.<*module*>.**INTERFACE**. To ensure that you don't see an optimized version of the module, do not perform a **Run Flow** on the **Quick Setup** tab prior to setting LogicLock constraints. Always use the **Read** command, as described in step 4.

11. Continue making any other settings as required on the **Constraints** tab.

12. Select **Preserve** in the **Hierarchy** section on the **Optimize** tab to ensure that the hierarchy names are not flattened during optimization.

13. Continue making any other settings as required on the **Optimize** tab.

14. Run your synthesis flow using each Flow tab, or click **Run Flow**.

Synthesis creates an EDIF file for each module that has a LogicLock assignment in the **Constraints** Flow tab. You can now use these files with the incremental compilation flows in the Quartus II software.

You might occasionally see multiple EDIF files and LogicLock commands for the same module. An "unfolded" version of a module is created when you instantiate a module more than once and the boundary conditions of the instances are different. For example, if you apply a constant to one instance of the block, it might be optimized to eliminate unneeded logic. In this case, the LeonardoSpectrum software must create a separate module for each instantiation (unfolding). If this unfolding occurs, you see more than one EDIF file, and each EDIF file has a LogicLock assignment to the same LogicLock region. When you import the EDIF files to the Quartus II software, the EDIF files created from the module are placed in different LogicLock regions. Any optimizations performed in the Quartus II software using the LogicLock methodology must be performed separately for each EDIF netlist.

Creating a Quartus II Project for Multiple EDIF Files Including LogicLock Regions

The LeonardoSpectrum software creates Tcl files that provide the Quartus II software with the appropriate LogicLock assignments, creating a region for each EDIF file along with the information to set up a Quartus II project.

The Tcl file contains the commands shown in Example 10–5 for each LogicLock region. This example is for module `taps` where the name `taps_region` was typed as the LogicLock region name in the **Constraints** Flow tab in the LeonardoSpectrum software.

Example 10–5. Tcl File for Module Taps with taps_region as LogicLock Region Name

```
project add_assignment {taps} {taps_region} {} {}
    {LL_AUTO_SIZE} {ON}
project add_assignment {taps} {taps_region} {} {}
    {LL_STATE} {FLOATING}
project add_assignment {taps} {taps_region} {} {}
    {LL_MEMBER_OF} {taps_region}
```

These commands create a LogicLock region with Auto-Size and Floating-Origin properties. This flexible LogicLock region allows the Quartus II Compiler to select the size and location of the region.

For more information about Tcl commands, refer to the *TCL Scripting* chapter in volume 2 of the *Quartus II Handbook*.

You can use the following methods to import the EDIF file and corresponding Tcl file into the Quartus II software:

- Use the Tcl file that is created for each EDIF file by the LeonardoSpectrum software. This method allows you to generate multiple Quartus II projects, one for each block in the design. Each designer in the project can optimize their block separately in the Quartus II software and preserve their results. Altera recommends this method for bottom-up incremental and hierarchical design methodologies because it allows each block in the design to be treated separately. Each block can be brought into one top-level project with the import function.

  or

- Use the <*top-level project*>**.tcl** file that contains the assignments for all blocks in the project. This method allows the top-level designer to import all the blocks into one Quartus II project. You can optimize all modules in the project at once in a top-down design flow. If additional optimization is required for individual blocks, each designer can use their EDIF file to create a separate project at that time. You would then have to add new assignments to the top-level project using the import function.

In both methods, you can use the following steps to create the Quartus II project, import the appropriate LogicLock assignments, and compile the design:

1. Place the EDIF and Tcl files in the same directory.
2. On the View menu, point to Utility Windows and click **Tcl Console** to open the Quartus II **Tcl Console**.

3. Type `source <path>/<project name>.tcl ↵`.

4. To open the new completed project, on the File menu, click **Open Project**. Browse to and select the project name, and click **Open**.

For more information about importing design using incremental compilation, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*. For more information about importing LogicLock assignments, see the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

Generating Multiple EDIF Files Using Black Boxes

This section describes how to manually generate multiple EDIF files using the black-boxing technique. The manual flow, described below, was supported in older versions of the LeonardoSpectrum software. The manual flow is discussed here because some designers want more control over the project for each submodule.

To create multiple EDIF files in the LeonardoSpectrum software, create a separate project for each module and top-level design that you want to maintain as a separate EDIF file. Implement black-box instantiations of lower-level modules in your top-level project.

When synthesizing the projects for the lower-level modules and the top-level design, use the following general guidelines.

For lower-level modules:

- Turn off **Map IO Registers** for the target technology on the **Technology** Flow tab.
- Read the HDL files for the modules. Modules may include black-box instantiations of lower-level modules that are also maintained as separate EDIF files.
- Add constraints.
- Turn off **Add I/O Pads** on the **Optimize** Flow tab.

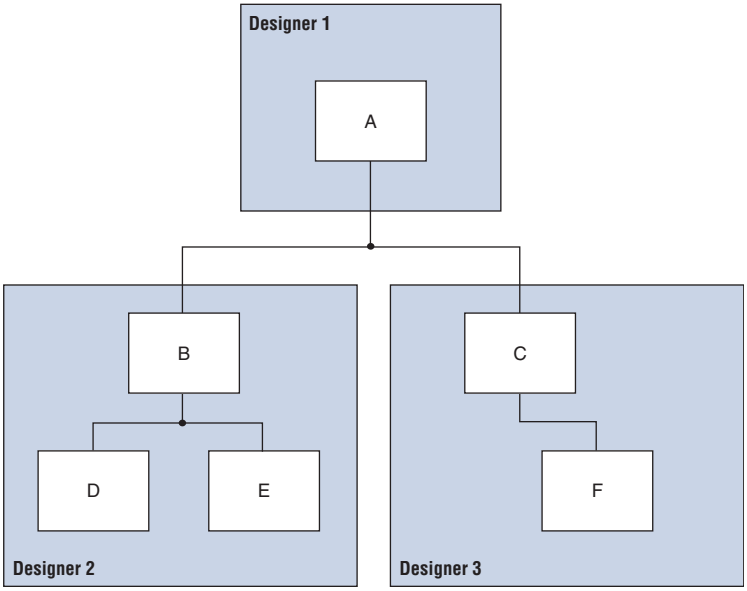
For the top-level design:

- Turn on **Map IO Registers** if you want to implement input and/or output registers in the IOEs for the target technology on the **Technology** Flow tab.
- Read the HDL files for the top-level design.
  - Black-box lower-level modules in the top-level design
- Add constraints (clock settings should be made at this time).

The following sections describe examples of black-box modules in a block-based and team-based design flow.

In Figure 10–3, the top-level design A is assigned to one engineer (designer 1), while two-engineers work on the lower levels of the design. Designer 2 works on B and its submodules D and E, while designer 3 works on C and its submodule F.

Figure 10–3. Block-Based & Team-Based Design Example



One netlist is created for the top-level module A, another netlist is created for B and its submodules D and E, while another netlist is created for C and its submodule F. To create multiple EDIF files, perform the following steps:

1. Generate an EDIF file for module C. Use **C.v** and **F.v** as the source files.
2. Generate an EDIF file for module B. Use **B.v**, **D.v**, and **E.v** as the source files.
3. Generate a top-level EDIF file **A.v** for module A. Ensure that your black-box modules B and C were optimized separately in steps 1 and 2.

Black Boxing in Verilog HDL

Any design block that is not defined in the project, or included in the list of files to be read for a project, is treated as a black box by the software. In Verilog HDL, you must also provide an empty module declaration for the module that you plan to treat as a black box.

Example 10–6 shows an example of the **A.v** top-level file. If any of your lower-level files also contain a black-boxed lower-level file in the next level of hierarchy, follow the same procedure.

Example 10–6. Verilog HDL Top-Level File Black-Boxing Example

```
module A (data_in,clk,e,ld,data_out);
    input data_in, clk, e, ld;
    output [15:0] data_out;

    reg [15:0] cnt_out;
    reg [15:0] reg_a_out;

    B U1 ( .data_in (data_in),.clk (clk), .e(e), .ld (ld),
           .data_out(cnt_out) );

    C U2 ( .d(cnt_out), .clk (clk), .e(e), .q (reg_out));
    // Any other code in A.v goes here.

endmodule

// Empty Module Declarations of Sub-Blocks B and C follow here.
// These module declarations (including ports) are required for blackboxing.

module B (data_in,e,ld,data_out );
    input data_in, clk, e, ld;
    output [15:0] data_out;
endmodule

module C (d,clk,e,q );
    input d, clk, e;
    output [15:0] q;
endmodule
```

Previous versions of the LeonardoSpectrum software required an attribute statement `//exemplar attribute U1 NOOPT TRUE`, which instructs the software to treat the instance `U1` as a black box. This attribute is no longer required, although it is still supported in the software.

Black Boxing in VHDL

Any design block that is not defined in the project, or included in the list of files to be read for a project, is treated as a black box by the software. In VHDL, you need a component declaration for the black box which is normal for any other block in the design.

Example 10–7 shows an example of the **A.vhd** top-level file. If any of your lower-level files also contain a black-boxed lower-level file in the next level of hierarchy, follow the same procedure.

Example 10–7. VHDL Top-Level File Black-Boxing Example

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY A IS
PORT ( data_in : IN INTEGER RANGE 0 TO 15;
    clk : IN STD_LOGIC;
    e : IN STD_LOGIC;
    ld : IN STD_LOGIC;
    data_out : OUT INTEGER RANGE 0 TO 15
);
END A;

ARCHITECTURE a_arch OF A IS

COMPONENT B PORT(
    data_in : IN INTEGER RANGE 0 TO 15;
    clk : IN STD_LOGIC;
    e : IN STD_LOGIC;
    ld : IN STD_LOGIC;
    data_out : OUT INTEGER RANGE 0 TO 15
);
END COMPONENT;

COMPONENT C PORT(
    d : IN INTEGER RANGE 0 TO 15;
    clk : IN STD_LOGIC;
    e : IN STD_LOGIC;
    q : OUT INTEGER RANGE 0 TO 15
);
END COMPONENT;

-- Other component declarations in A.vhd go here

signal cnt_out : INTEGER RANGE 0 TO 15;
signal reg_a_out : INTEGER RANGE 0 TO 15;
BEGIN
CNT : C
PORT MAP (
    data_in => data_in,
    clk => clk,
    e => e,
    ld => ld,
    data_out => cnt_out
);

REG_A : D
PORT MAP (
    d => cnt_out,
    clk => clk,
    e => e,
    q => reg_a_out
);

-- Any other code in A.vhd goes here

END a_arch;
```

Previous versions of the LeonardoSpectrum software required the attribute statement `noopt of C: component is TRUE`, which instructed the software to treat the component C as a black box. This attribute is no longer required, although it is still supported in the software.

After you have completed the steps outlined in this section, you have a different EDIF netlist file for each block of code. You can now use these files for incremental compilation flows in the Quartus II software.

Creating a Quartus II Project for Multiple EDIF Files

The LeonardoSpectrum software creates a Tcl file for each EDIF file, which provides the Quartus II software with the information to set up a project.

As in the previous section, there are two different methods for bringing each EDIF and corresponding Tcl file into the Quartus II software:

- Use the Tcl file that is created for each EDIF file by the LeonardoSpectrum software. This method generates multiple Quartus II projects, one for each block in the design. Each designer in the project can optimize their block separately in the Quartus II software and preserve their results. Designers should create a LogicLock region for each block; the top-level designer should then import all the blocks and assignments into the top-level project. Altera recommends this method for bottom-up incremental and hierarchical design methodology because it allows each block in the design to be treated separately; each block can be imported into one top-level project.

  or

- Use the <*top-level project*>**.tcl** file that contains the information to set up the top-level project. This method allows the top-level designer to create LogicLock regions for each block and bring all the blocks into one Quartus II project. Designers can optimize all modules in the project at once in a top-down design flow. If additional optimization is required for individual blocks, each designer can take their EDIF file and create a separate Quartus II project at that time. New assignments would then have to be added to the top-level project manually or through the import function.

For more information about importing designs using incremental compilation, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*. For more information about importing LogicLock regions, refer to the *LogicLock Design Methodology* chapter in the volume 2 of the *Quartus II Handbook*.

In both methods, you can use the following steps to create the Quartus II project and compile the design:

1. Place the EDIF and Tcl files in the same directory.
2. On the View menu, point to Utility Windows and click **Tcl Console**. The Quartus II **Tcl Console** is shown.
3. At a Tcl prompt, type `source` <*path*>/<*project name*>`.tcl` ↵.
4. On the File menu, click **Open Project**. In the **New Project** window, browse to and select the project name. Click **Open**.
5. To create LogicLock assignments, on the Assignments menu, click **LogicLock Regions Window**.
6. On the Processing menu, click **Start Compilation**.

Incremental Synthesis Flow

If you make changes to one or more submodules, you can manually create new projects in the LeonardoSpectrum software to generate a new EDIF netlist file when there are changes to the source files. Alternatively, you can use incremental synthesis to generate a new netlist for the changed submodule(s). To perform incremental synthesis in the LeonardoSpectrum software, use the script described in this section to reoptimize and generate a new EDIF netlist for only the affected modules using the LeonardoSpectrum top-level project. This method applies only when you are using the **LogicLock** option in the LeonardoSpectrum software.

Modifications Required for the LogicLock_Incremental.tcl Script File

There are three sets of entries in the file that must be modified before beginning incremental synthesis. The variables in the Tcl file are surrounded by angle brackets (< >).

1. Add the list of source files that are included in the project. You can enter the full path to the file or just the file name if the files are located in the working directory.

2. Indicate which modules in the design have changed. These modules are the EDIF files that are regenerated by the LeonardoSpectrum software. These modules contain a LogicLock assignment in the original compilation.

   Obtain the LeonardoSpectrum software path for each module by looking at the CTR file that contains the LogicLock assignments from the original project. Each LogicLock assignment is applied to a particular module in the design.

3. Enter the target device family using the appropriate device keyword. The device keyword is written into the **Transcript** or **Information** window when you select a target Technology and click **Load Library** or **Apply** on the **Technology Flow** tab in the graphical user interface.

Example 10–8 shows the **LogicLock_Incremental.tcl** file for the incremental synthesis flow. You must modify the Tcl file before you can use it for your project.

Example 10–8. LogicLock_Interface.tcl Script File for Incremental Synthesis

```
################################################
#### LogicLock Incremental Synthesis Flow ####
################################################

## You must indicate which modules have changed (based on the source files
## that have changed) and provide the complete path to each module

## You must also specify the list of design files and the target Altera
## technology being used

# Read the design source files.
read <list of design files separated by spaces (such as block1.v block2.v)>

# Get the list of modified modules in bottom-up "depth first search" order
# where the lower-level blocks are listed first (these should be modules
# that had LogicLock assignments and separate EDIF netlist files in the
# first pass and had their source code modified)

set list_of_modified_modules {.work.<block2>.INTERFACE .work.<block1>.INTERFACE}

foreach module $list_of_modified_modules {
    set err_rc [regexp {\.(.*)\.(.*)\.(.*)} $module unused lib module_name arch]
    present_design $module

    # Run optimization, preserving hierarchy. You must specify a technology.
    optimize -ta <technology> -hierarchy preserve

    # Ensure that the lower-level module is not optimized again when
    # optimizing higher-level modules.
    dont_touch $module
}

foreach module $list_of_modified_modules {
    set err_rc [regexp {\.(.*)\.(.*)\.(.*)} $module unused lib module_name arch]
    present_design $module
    undont_touch $module
    auto_write $module_name.edf
    # Ensure that the lower-level module is not written out in the EDIF file
    # of the higher-level module.
    noopt $module
}
```

Running the Tcl Script File in LeonardoSpectrum

Once you have modified the Tcl script, as described in the "Modifications Required for the LogicLock_Incremental.tcl Script File" on page 10–31, you can compile your design using the script.

You can run the script in batch mode at the command line prompt using the following command:

```
spectrum -file <Tcl_file> ↵
```

To run the script from the interface, on the File menu, click **Run Script**, then browse to your Tcl file and click **Open**.

The LogicLock incremental design flow uses module-based design to help you preserve performance of modules and have control over placement. By tagging the modules that require separate EDIF files, you can make multiple EDIF files for use with the Quartus II software from a single LeonardoSpectrum software project.

Conclusion

Advanced synthesis is an important part of the design flow. Taking advantage of the Mentor Graphics LeonardoSpectrum software and the Quartus II design flow allows you to control how your design files are prepared for the Quartus II place-and-route process, as well as to improve performance and optimize a design for use with Altera devices. The methodologies outlined in this chapter can help optimize a design to achieve performance goals and save design time.

11. Synopsys Design Compiler FPGA Support

QII51014-6.0.0

Introduction

Programmable logic device (PLD) designs have reached the complexity and performance requirements of ASIC designs. As a result, advanced synthesis has taken on a more important role in the design process. This chapter documents the usage and design flow of the Synopsys Design Compiler FPGA (DC FPGA) synthesis software with Altera® devices and Quartus® II software. DC FPGA supports Stratix® II, Stratix, Stratix GX, Cyclone™ II, and Cyclone devices.

This chapter assumes that you have set up and licensed the DC FPGA software and Altera Quartus II software.

This chapter is primarily intended for ASIC designers experienced with the Design Compiler (DC) software who are now developing PLD designs, and experienced PLD designers who would like an introduction to the Synopsys DC FPGA software.

To obtain the DC FPGA software, libraries, and instructions on general product usage, go to the Synopsys web site at **http://solvnet.synopsys.com/retrieve/012889.html**

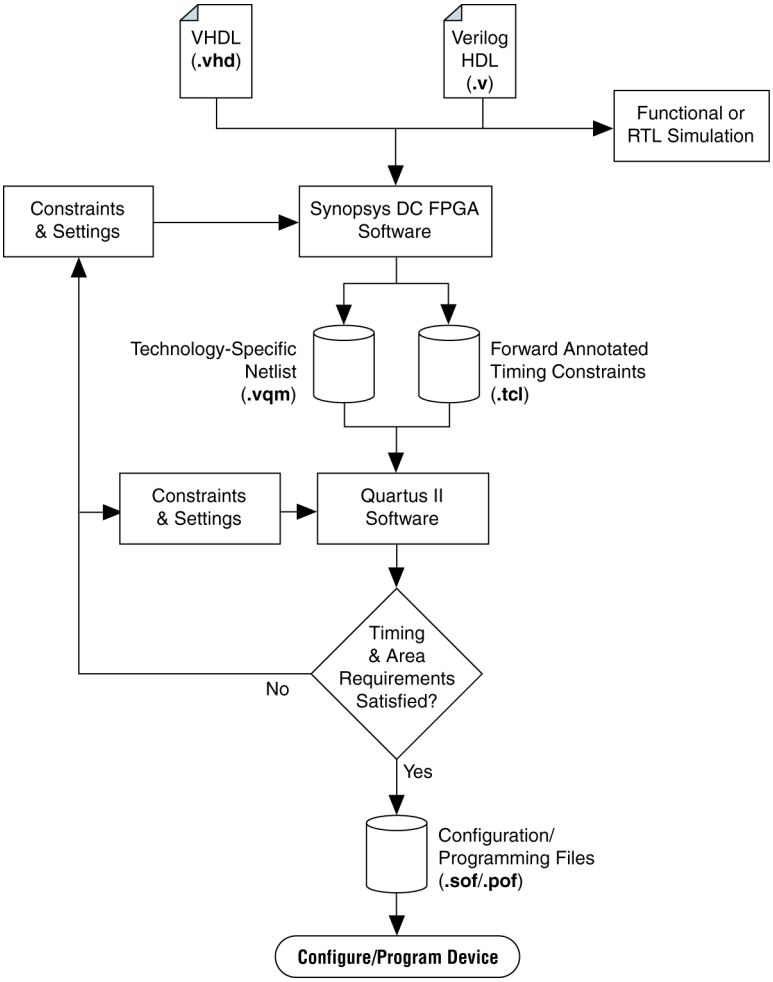
The following areas are covered in this chapter:

- General design flow with the DC FPGA software and the Quartus II software
- Initialization procedure using the **.synopsys_dc.setup** file for targeting Altera devices
- Using Altera megafunctions with the DC FPGA software
- Reading design files into the DC FPGA software
- Applying synthesis and timing constraints
- Reporting and saving design information
- Exporting designs to the Quartus II software

Design Flow Using the DC FPGA Software & the Quartus II Software

A high-level overview of the recommended design flow for using the DC FPGA software with the Quartus II software is shown in Figure 11–1.

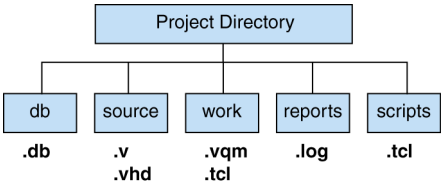
Figure 11–1. Design Flow Using the DC FPGA Software & the Quartus II Software



Setup of the DC FPGA Software Environment for Altera Device Families

Altera recommends that you organize your project directory with several subdirectories. A recommended project hierarchy is shown in Figure 11–2.

Figure 11–2. Project Hierarchy



To use the DC FPGA software to synthesize HDL designs for use with the Quartus II software, the required settings should be included in your **.synopsys_dc.setup** initialization file. This file is used to define global variables and direct the DC FPGA software to the proper libraries used for synthesis, as well as set internal assignments for synthesizing designs for Altera devices.

The **.synopsys_dc.setup** file can reside in any one of three locations and be read by the DC FPGA software. The DC FPGA software automatically reads the **.synopsys_dc.setup** file at startup in the following order of precedence:

1. Current directory where you run the DC FPGA software shell.
2. Home directory.
3. The DC FPGA software installation directory.

The DC FPGA software has vendor-specific setup files for each of the Altera logic families in the installation directory. These vendor-specific setup files are found where you have installed the libraries (<*dcfpga_rootdir*>**/libraries/fpga/altera**) and are named in the form **synopsys_dc_**<*logic family*>**.setup**. For example, if you want to use the default setup for synthesizing an Altera Stratix device, you must link to or copy the **synopsys_dc_stratix.setup** to your home or current directory and rename the file **.synopsys_dc.setup**.

Synopsys recommends using the vendor-specific setup files provided with each release of the DC FPGA software to ensure that you have all the correct settings and obtain the best quality results.

Example 11–1 contains the recommended synthesis settings for the Stratix II device architecture.

Example 11–1. Recommended Synthesis Settings for Stratix II Device Architecture

```
# Setup file for Altera Stratixii
# TCL style setup file but will work for original DC shell as well
# Need to define the root location of the libraries by chaning the variable
$dcfpga_lib_path

set dcfpga_lib_path "<dcfpga_rootdir>/libraries/fpga/altera"


set search_path ". $dcfpga_lib_path $dcfpga_lib_path/STRATIXII $search_path"
set target_library "stratixii.db"
set synthetic_library "tmg.sldb altera_mf.sldb lpm.sldb"
set link_library "* stratixii.db tmg.sldb altera_mf.sldb lpm.sldb stratixii_mf.sldb"

set_fpga_defaults altera_stratixii
```

After generating your **.synopsys_dc.setup** file, run the DC FPGA software in either the Tcl shell or in the Design Compiler software shell without Tcl support. Run the DC FPGA software shell at a command prompt by typing `fpga_shell-t` or `fpga_shell -tcl` for the Tcl shell version of the DC FPGA software. Run the non-Tcl version of the DC FPGA software with the `fpga_shell` command. Altera recommends using the Tcl shell for all of your synthesis work.

If you have created a Tcl synthesis script for use in the DC FPGA software and wish to run it immediately at startup, you can start the DC FPGA software shell and run the script with the command shown in the example below:

`fpga_shell-t -f` *<path>/<script filename>*`.tcl` ↵

Otherwise, you can run your scripts at any time at the `fpga_shell-t>` prompt with the `source` command. An example is shown below:

`source` *<path>/<script filename>*`.tcl` ↵

Megafunctions & Architecture-Specific Features

Altera provides parameterized megafunctions including library of parameterized modules (LPMs), device-specific Altera megafunctions, intellectual property (IP) available as Altera MegaCore® functions, and IP available through the Altera Megafunction Partners Program (AMPP). You can use megafunctions by instantiating them in your HDL code, or by inferring them from your HDL code during synthesis in the DC FPGA software.

For more details on specific Altera megafunctions, refer to the Quartus II Help.

The DC FPGA software automatically recognizes certain types of HDL code and infers the appropriate megafunction when a megafunction provides optimal results. The DC FPGA software also provides options to control inference of certain types of megafunctions, as described in the section "Instantiating Altera Megafunctions Using the MegaWizard Plug-In Manager" on page 11–6.

For a detailed discussion about instantiating versus inferring megafunctions, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*. This chapter also provides details about using the MegaWizard® Plug-In Manager in the Quartus II software and explains the files generated by the wizard. In addition, the chapter provides coding style recommendations and examples for inferring megafunctions in Altera devices.

If you instantiate a megafunction in your HDL code, you can use the MegaWizard Plug-In Manager to parameterize the function, or you can instantiate the function using the port and parameter definition. The MegaWizard Plug-In Manager provides a graphical interface in the Quartus II software for customizing and parameterizing megafunctions. "Instantiating Altera Megafunctions Using the MegaWizard Plug-In Manager" on page 11–6 describes the MegaWizard Plug-In Manager flow with the DC FPGA synthesis software.

Instantiating Altera Megafunctions Using the MegaWizard Plug-In Manager

When you use the MegaWizard Plug-In Manager to set up and parameterize a megafunction, the MegaWizard Plug-In Manager creates a VHDL or Verilog HDL wrapper file that instantiates the megafunction (a black box methodology). The MegaWizard can also generate a fully elaborated netlist that is read by EDA synthesis tools, such as the DC FPGA (a clear box methodology). Both clear box and black box methodologies are described in the following sections.

Clear Box Methodology

You can use the MegaWizard Plug-In Manager to generate a fully synthesizeable netlist. This flow is referred to as a clear box methodology because starting in V-2005.06, the DC FPGA software can look into the megafunction file. The clear box feature enables the synthesis tool to report more accurate timing estimates and resource utilization, while taking a better advantage of timing driven optimization than a black box methodology.

This clear box feature is enabled by turning on the **Generate clear box netlist file instead of a default wrapper file (for use with supported EDA synthesis tools only)** option in the MegaWizard Plug-In Manager for certain megafunctions. DC FPGA supports clear box megafunctions for `altmult_add`, `almult_accum`, `altsyncram` and `altshift_taps`. If the option does not appear, then clear box models are not supported for the selected megafunction.

The library declarations in the MegaWizard generated VHDL output files need to be manually commented out to work properly with the DC FPGA.

Reading Megafunction Wizard-Generated Synthesizable Clear Box Netlist Files for Megafunction Instantiation

The DC FPGA software analyzes and elaborates the Megafunction Wizard-generated Verilog HDL <*output file*>**.v** or VHDL <*output file*>**.vhd** netlist that contains the parameters needed by the Quartus II software to properly configure and instantiate your megafunction. Analyze the clear box netlist files along with the rest of the RTL files during synthesis in DC FPGA. The resulting netlist contains all the primitives that are part of the clear box netlist. There is no need to put the clear box netlist file in your Quartus II project along with your DC FPGA generated netlist file.

Using the clear box Megafunction Wizard-generated netlist files provides the DC FPGA software an understanding of their timing arcs and resource usage. The DC FPGA software uses timing information to optimize the surrounding circuits and resource data to better manage the overall resource usage for the whole design. The DC FPGA software takes the clear box netlist timing and area data into account when reporting the timing and resource utilization for the device.

Advanced Clear Box Support for the Direct-Instantiated or Inferred Clear Box Megafunctions

The DC FPGA provides advanced clear box support that enables a clear box implementation for the direct-instantiated or inferred megafunctions in your design. This methodology allows the DC FPGA to obtain the most accurate interface timing and area data for the megafunctions. Therefore, synthesis optimization is more effective, and timing and area reports are more accurate.

The following describes the setup and usage model for this advanced clear box support.

Design Compiler FPGA Setup

The advanced clear box flow will be enabled in the DC FPGA only when the **clearbox.sldb** synthetic library is added to the `synthetic_library` variable. For example:

```
set synthetic_library [concat clearbox.sldb $synthetic_library]
set link_library [concat clearbox.sldb $link_library]
```

Specify the path to the clear box loader (executable) in one of the following ways:

- Set the `synlib_cbx_exec_path` variable to the absolute path of the clear box loader before the compile command:
  `set synlib_cbx_exec_path` <*Quartus II installation directory /bin/clearbox*>
- Set the UNIX environment variable `CLEARBOX_EXEC_PATH` to the absolute path of the clear box loader. For example:
  `setenv CLEARBOX_EXEC_PATH` <*Quartus II installation directory /bin/clearbox*>

By default, the advance clear box flow is turned off. To enable the clear box advanced flow, add the following to your DC FPGA script. Set it before the compile command:

```
set fpga_altera_clearbox_for_user_cells true
```

UNIX Environment Setting

For the DC FPGA to work with the clear box loader, the following setting is necessary for the LD_LIBRARY_PATH environment variable. Assume the QuartusII_Path used below is set to the Quartus II installation directory.

On a Linux platform:

```
setenv LD_LIBRARY_PATH QuartusII_Path/linux:$LD_LIBRARY_PATH
```

On a Solaris platform:

```
setenv LD_LIBRARY_PATH QuartusII_Path/solaris:$LD_LIBRARY_PATH
```

Error Message

The only error message that you might encounter when trying to enable the advanced clear box flow is: DCFPGA_UEGI-1

The DC FPGA reports this error when one of the following situations occurs:

- It cannot find the clear box loader path. For example, the defined path is incorrect.
- The Loader is not found in the specified path.
- The Loader specified is not executable.

Sample Design Compiler FPGA Clear Box Setup Script

The TCL script shown in Example 11–2 is a DC FPGA clear box setup script. Use it before compiling the design in DC FPGA.

Example 11–2. Sample Clear Box Setup Script

```
set QuartusII_Path /tools/altera/qii51
set_unix_variable CLEARBOX_EXEC_PATH $QuartusII_Path/bin/clearbox
set old_llp [get_unix_variable LD_LIBRARY_PATH]
set platform [sh uname]

if { $platform == "Linux" } {
    set_unix_variable LD_LIBRARY_PATH $QuartusII_Path/linux: old_llp
} else {
    # Assume, if not linux, it is solaris
    set_unix_variable LD_LIBRARY_PATH $QuartusII_Path/solaris: old_llp

set synthetic_library [concat clearbox.sldb $synthetic_library]
set link_library [concat clearbox.sldb $link_library]

set fpga_altera_clearbox_for_user_cells true
```

Black Box Methodology

Using the MegaWizard Plug-In Manager-generated wrapper file is referred to as a black box methodology because the megafunction is treated as a black box in the DCFPGA software. The black box wrapper file is generated by default in the MegaWizard Plug-In Manager and is available for all megafunctions. The black box methodology does not allow the synthesis tool any visibility into the function module and therefore, does not take full advantage of the synthesis tool's timing driven optimization.

There are two ways of instantiating Megafunction Wizard-generated functions in your design hierarchy loaded in the DC FPGA software. You can instantiate and compile the Verilog HDL or VHDL variation wrapper file description of your megafunction in the DC FPGA software, or you can instantiate a black box that just describes the ports of your megafunction variation wrapper file.

The library declarations in the MegaWizard generated VHDL output files need to be manually commented out to work properly with the DC FPGA.

Reading Megafunction Wizard-generated Variation Wrapper Files

The DC FPGA software has the ability to analyze and elaborate the Megafunction Wizard-generated Verilog HDL <*output file*>**.v** or VHDL <*output file*>**.vhd** netlist that contains the parameters needed by the Quartus II software to properly configure and instantiate your megafunction. The DC FPGA software may take advantage of this variation wrapper file during the optimization of your design to reduce area utilization and improve path delays. DC FPGA also supports altpll in a non-black box flow (that is, the DC FPGA can automatically derive PLL output clocks when the user has specified only the PLL input clock).

Using the megafunction variation wrapper file <*output file*>**.v** or <*output file*>**.vhd** in the DC FPGA software synthesis provides good synthesis results for area estimates, but actual timing results are best predicted after place-and-route inside the Quartus II software. However, reading the megafunction variation wrapper allows the DC FPGA software to provide better synthesis estimates over a black box methodology.

Using Megafunction Wizard-Generated Variation Wrapper Files in a Black Box Methodology

Instantiating the megafunction wizard-generated wrapper file without reading it in the DC FPGA software is referred to as a black box methodology because the megafunction is treated as an unknown container in the DC FPGA software.

The black box methodology does not allow synthesis software to have any visibility into the module, thereby not taking full advantage of the timing driven optimization of the DC FPGA software and preventing the software from estimating logic resources for the black box design.

Using Megafunction Wizard-Generated Verilog HDL Files for Black Box Megafunction Instantiation

By default, the MegaWizard Plug-In Manager generates the Verilog HDL instantiation template file <*output file*>**_inst.v** and the black box module declaration <*output_file*>**_bb.v** for use in your design in the DC FPGA software. The instantiation template file helps to instantiate the megafunction variation wrapper file, <*output file*>**.v**, in your top-level design. Do not include the megafunction variation wrapper file in the DC FPGA software project if you are following the black box methodology. Instead, add the wrapper file and your generated Verilog Quartus Mapping (**.vqm**) netlist in your Quartus II project. Add the hollow body black box module declaration <*output file*>**_bb.v** to your linked design files in the DC FPGA software to describe the port connections of the black box.

Using Megafunction Wizard-Generated VHDL Files for Black Box Megafunction Instantiation

By default, the MegaWizard Plug-In Manager generates a VHDL component declaration file <*output file*>**.cmp** and a VHDL instantiation template file <*output file*>**_inst.vhd** for use in your design. These files can help you instantiate the megafunction variation wrapper file, <*output file*>**.vhd**, in your top-level design. Do not include the megafunction variation wrapper file in the DC FPGA software project. Instead, add the wrapper file and your generated Verilog Quartus Mapping netlist in your Quartus II project.

The DC FPGA software supports direct instantiation of all LPMs and megafunctions. For a complete list of all LPMs and Megafunctions, refer to the following two files in your Quartus II installation directory:

- <Quartus II installation directory> **/libraries/vhdl/lpm/lpm_pack.vhd**
- <Quartus II installation directory> **/libraries/vhdl/altera_mf/altera_mf_components.vhd**

DC FPGA supports direct instantiation of LPMs and megafunctions only. These macro functions include all Altera IP cores and all components listed in:

<***Quartus II installation directory***>**/libraries/vhdl/altera_mf_components.vhd** or **stratixgx_mf_components.vhd**.

The following example is the usage model using the **mypll** for direct instantiation:

1. During synthesis in DC FPGA, analyze the variation file **mypll.[v|vhd]** along with the rest of the RTL files.

2. During place-and-route in the Quartus II software, simply run the self-contained Verilog Quartus Mapping File. You do not need to put the variation file in the Verilog Quartus Mapping directory.

The benefit of using the direct instantiation method is that the DC FPGA is able to utilize the available clock enable pins of the LPMs and megafunctions during the automatic gated-clock conversion process.

Inferring Altera Megafunctions from HDL Code

The DC FPGA software automatically recognizes certain types of HDL code, and maps digital signal processing (DSP) functions and memory (RAM and ROM) to efficient, technology-specific implementations. This allows the use of technology-specific resources to implement these structures by inferring the appropriate Altera megafunction when it provides optimal results.

For coding style recommendations and examples for inferring megafunctions in Altera devices, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

Depending on the coding style, if you do not adhere to these recommended HDL coding style guidelines, it is possible that the DC FPGA software and Quartus II software will not take advantage of the high performance DSP blocks and RAMs, and may instead

implement your logic using regular logic elements (LEs). This causes your logic to consume more area in your device and may adversely affect your design performance. Altera device families do not all share the same resources, so your HDL coding style may cause your logic to be implemented differently in each family. For example, Stratix devices contain dedicated DSP blocks which Cyclone devices lack. In a Cyclone device, multipliers are implemented in LEs.

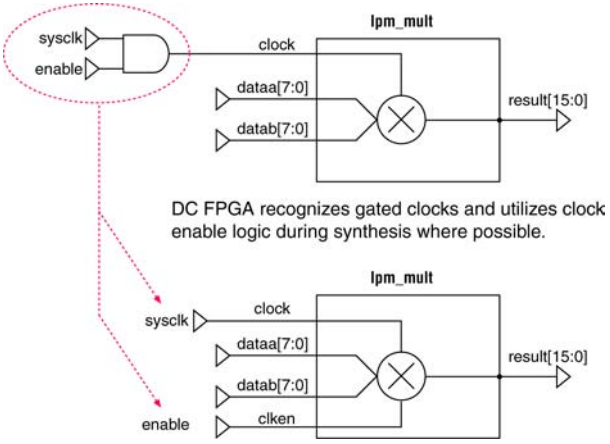
Example 11–3 shows Verilog HDL code that infers a two-port RAM that can be synthesized into an M512 RAM block of a Stratix device.

Example 11–3. Verilog HDL Code Inferring a Two-Port RAM

```
module example_ram (clk, we, rd_addr, wr_addr, data_in, data_out);
input clk, we;
input [15:0] data_in;
output [15:0] data_out;
input [7:0] rd_addr;
input [7:0] wr_addr;
reg [15:0] ram_data [7:0];
reg [15:0] data_out_reg;
always @ (posedge clk)
begin
if (we)
        ram_data[wr_addr] <= data_in;
data_out_reg <= ram_data[rd_addr];
end
assign data_out = data_out_reg;
endmodule
```

One of the strengths of the DC FPGA software is its gated clock conversion feature. Inferring megafunctions in HDL takes advantage of this feature. For gated clocks or clock enables designed outside of LPMs, Altera-specific megafunctions, and registers, the DC FPGA software merges the gated clock functions into these design elements using dedicated clock enable functionality during synthesis. The DC FPGA software reconfigures the megafunction block or register to synthesize the clock enable control logic. This can save area in your design and improve your design performance by reducing the gated clock path delay and the amount of logic used to implement the design. An illustration of this kind of gated clock optimization is shown in Figure 11–3.

Figure 11–3. Gated Clock Optimization



The DC FPGA software does not perform gated clock optimization on instantiated black box megafunctions or on instantiated megafunction variation wrapper file. The DC FPGA software performs gated clock optimization only on synthesizable inferred megafunctions.

Reading Design Files into the DC FPGA Software

The process of reading design files into the DC FPGA software is a two-step process where the DC FPGA software analyzes your HDL design for syntax errors, then elaborates the specified design. The elaboration process finds analyzed designs and instantiates them in the elaborated design's hierarchy. You must identify which supported language the files are written in when reading designs into the DC FPGA software. The supported HDL languages are listed in Table 11–1.

Table 11–1. Supported Design File Formats

Format	Description	Keyword	Extension
Verilog HDL (Synopsys Presto HDL)	Verilog hardware description language	verilog	.v
VHDL	VHSIC hardware description language	vhdl	.vhd
.db	Synopsys internal database format *(1)*	db	.db
EDIF	Electronic design interchange format	edif	.edf

Note to Table 11–1:
(1) The Design Compiler DB format file requires additional license keys.

To set most of the required synthesis settings to generate an optimal netlist, use the following command:

```
set_fpga_defaults <architecture_name>
```

For example:

```
set_fpga_defaults altera_stratixii
```

Use the following commands to analyze and elaborate HDL designs in the DC FPGA software:

```
analyze -f <verilog|vhdl> <design file> ↵
```

```
elaborate <design name> ↵
```

Once a design is analyzed, it is stored in a Synopsys library format file in your working directory for reuse. You need to re-analyze the design only when you change the source HDL file. Elaboration is performed after you have analyzed all of the subdesigns below your current design.

Another way to read your design is by using the `read_file` command. This can be used to read in gate-level netlists that are already mapped to a specific technology. The `read_file` command performs analysis and elaboration on Verilog HDL and VHDL designs that are written in register transfer level (RTL) format. The difference between the `read_file` command and the analyze and elaborate combination is that the `read_file` command elaborates every design read, which is unnecessary. Only the top-level design must be elaborated. The `read_file` command is useful if you have a previously synthesized block of logic that you want to re-use in your design.

To use the `read_file` command for a specific language, type the following command:

```
read_file -f <verilog|vhdl|db|edif> <design file> ↵
```

You can also read files in specific languages using the `read_verilog`, `read_vhdl`, `read_db`, and `read_edif` commands.

Once you have read all of your design files, specify the design you want to focus your work on with the `current_design` command. This is usually the top module or entity in your design that you wish to compile up to. To use this command, type the following:

```
current_design <design name> ↵
```

You then need to build your design from all of the analyzed HDL files with the link command. To use this command, type the following:

```
link ↵
```

After linking your designs successfully in the DC FPGA software, you should specify the constraints you are applying to your design. In the DC FPGA software, you have the capability of loading multiple levels of hierarchy and synthesizing specific blocks in a bottom-up synthesis methodology, or you can synthesize the entire design from the top-level module in a top-down synthesis methodology.

You can switch the current focus of the DC FPGA software between the designs loaded by using the `current_design` command. This changes your current focus onto the design specified, and all subsequent constraints and commands will apply to that design.

If you have read Quartus II megafunction wizard-generated designs or third-party IP into the DC FPGA software, you can instruct the DC FPGA software not to synthesize the IP. Use the `set_dont_touch` constraint and apply it to each module of your design that you do not want synthesized. To use this command, type the following:

```
set_dont_touch <design name> ↵
```

Using the `set_dont_touch` command can be helpful in a bottom-up synthesis methodology, where you optimize designs at the lower levels of your hierarchy first and do not allow the DC FPGA software to resynthesize them later during the top-level integration. However, depending on the design's HDL coding, you might want to allow top-level resynthesis to get further area reduction and improved path delays. For best results, Altera recommends following the top-down synthesis methodology and not using the `set_dont_touch` command on lower level designs.

Selecting a Target Device

If you do not select an Altera device, the DC FPGA software, by default, synthesizes for the fastest speed grade of the logic family library that is loaded in your **.synopsys_dc.setup** file. If you are targeting a specific device of an Altera family, you must have the correct library linked, then specify the device for synthesis with the `set_fpga_target_device` command**.** To use this command, type the following:

```
set_fpga_target_device <device name> ↵
```

You can have the DC FPGA software produce a list of all available devices in the linked library by adding the `-show_all` option to the `set_fpga_target_device` command. An example of this list of devices for the Stratix II library is shown in Example 11–4.

Example 11–4. List of Available Devices in the Linked Library Using the -show_all Option

```
Loading db file '/dc_fpga/libraries/fpga/altera/STRATIXII/stratixii.db'

  Valid device names are:

Part              Pins      FFs    Speed Grades
-----------------------------------------------
AUTO *            0         0        FASTEST
EP2S15F484        484       12480    C4
EP2S15F672        672       12480    C4
EP2S30F484        484       27104    C4
EP2S30F672        672       27104    C4
EP2S60F484        484       48352    C4
EP2S60F672        672       48352    C4
EP2S60F1020       1020      48352    C4
EP2S90F1020       1020      72768    C4
EP2S90F1508       1508      72768    C4
EP2S130F1020      1020      106032   C4
EP2S130F1508      1508      106032   C4
EP2S180F1020      1020      143520   C4
EP2S180F1508      1508      143520   C4

  * Default part
```

For example, if you want to target the C4 speed grade device of the Stratix II EP2S60F672 device, apply the following constraint:

```
set_fpga_target_device EP2S60F672C4
```

Timing & Synthesis Constraints

You must create timing and synthesis constraints for your design for the DC FPGA software to optimize your design performance. The timing constraints specify your desired clocks and their characteristics, input and output delays, and timing exceptions such as false paths and multi-cycle paths. The synthesis constraints define the device, the type of I/O buffers that should be used for top-level ports, and the maximum register fan-out threshold before buffer insertion is performed. Synopsys Design Constraints (SDCs) are Tcl-format commands that are widely used in many EDA software applications. The DC FPGA software supports the same SDC commands that the full version of the Design Compiler software supports. However, certain constraints that are used in ASIC synthesis are not applicable to programmable logic synthesis, so the DC FPGA software ignores them.

The DC FPGA software supports the following constraints:

- `create_clock`
- `set_max_delay`
- `set_propagated_clock`
- `set_input_delay`
- `set_output_delay`
- `set_multicycle_path`
- `set_false_path`
- `set_disable_timing`
- `set_fpga_resource_limit`
- `set_register_max_fanout`
- `set_max_fanout`
- `set_fpga_target_device`

For the syntax and full usage of these commands, refer to the *Synopsys DC FPGA User Guide*.

For synthesis with the DC FPGA software, minimum timing analysis is not necessary, as it primarily looks at setup timing optimization to achieve the fastest clock frequency for your design. Altera recommends adding additional minimum timing constraints to your design inside the Quartus II software.

The DC FPGA forward annotates all the clock, timing exceptions, and I/O delay constraints to Quartus II when the `write_par_constraint` command is used in the DC FPGA. For more information about this command, refer to "Exporting Designs to the Quartus II Software" on page 11–22. Since the Quartus II software does not support the `through` option for the timing exception constraints, the DC FPGA does not forward annotate constraints that use the `through` option.

In the DC FPGA software, timing constraints applied to inferred RAM, ROM, shift registers, and DSP MAC functions are obeyed. However, these constraints are not forward-annotated to the Quartus II software because these functions are inferred to Altera megafunctions. The Quartus II software does not support timing constraints applied to megafunctions. The workaround is to run the Verilog Quartus Mapping/EDIF netlist through analysis and synthesis in the Quartus II software (**quartus_map**). All megafunctions expand to atom primitives. These atom primitives can be processed by the Quartus II software. You can then apply constraints to the internal atoms of the megafunctions.

The timing reports generated from the DC FPGA software are preliminary estimates of the path delays in your design, and accurate timing is reported only after place-and-route is performed with the Quartus II software.

The DC FPGA software also performs cross-hierarchical boundary optimization. Altera recommends running this command before a compilation:

```
ungroup -small 500 ↵
```

This allows the DC FPGA software to potentially improve area reduction and performance improvement by ungrouping smaller blocks of logic in your design hierarchy and combining functions.

Compilation & Synthesis

After applying timing and synthesis constraints, you can begin the compilation and synthesis process. The `compile` command runs this process within the DC FPGA software. To run a compilation, at the shell prompt type:

```
compile ↵
```

The compilation process performs two kinds of optimization:

- Architectural optimization focuses on the HDL description and performs high-level synthesis tasks such as sharing resources and sub-expressions, selecting Synopsys Design Ware implementations, and re-ordering operators.
- Gate-level optimization works on the generic netlist created by logic synthesis and works to improve the mapping efficiency to save area and improve performance by minimizing path delays.

Compilation can be done using a top-down synthesis methodology or a bottom-up synthesis methodology. The top-down synthesis methodology involves a single compilation of your entire design with the focus on the top module or entity of your design. The bottom-up synthesis methodology involves incremental compilation of major blocks in your design hierarchy and top-level integration and optimization. Either methodology can be applied when synthesizing for Altera devices. For best results, Altera recommends following the top-down synthesis methodology.

An example synthesis script that reads the design, applies timing constraints, reports results, saves the synthesized netlist file in the Verilog Quartus Mapping File format, and creates the Tcl scripts to work with the

Quartus II software is shown in Example 11–5. It uses the command write_fpga, which is described in "write_fpga Command" on page 11–22.

Example 11–5. Sample Synthesis Script

```
# Setup output directories
set outdir ./design
file delete -force $outdir
file mkdir $outdir
set rptdir ./report
file delete -force $rptdir
file mkdir $rptdir
#  Enable Presto compiler for VHDL design files
#  set hdlin_enable_presto_for_vhdl TRUE
# Setup libraries
define_design_lib work-path .$outdir/work
file mkdir $outdir/work
analyze -format verilog ./source/mult_box.v
analyze -format verilog ./source/mult_ram.v
analyze -format verilog ./source/top_module.v
elaborate top_module
link
current_design top_module
create_clock -period 5 [get_ports clk]
set_input_delay -max 2 -clock clk [get_ports {data_in_* mode_in}]
set_input_delay -min 0.5 -clock clk [get_ports {data_in_* mode_in}]
set_output_delay -max 2 -clock clk [get_ports {data_out ram_data_out_port} ]
set_output_delay -min 0.5 -clock clk [get_ports {data_out ram_data_out_port} ]
set_false_path -from [get_ports reset]
ungroup -small 500
compile
report_timing > $rptdir/top_module.log
report_fpga > $rptdir/top_module_fpga.log
write_fpga $outdir
quit
```

Reporting Design Information

After compilation is complete, the DC FPGA software reports information about your design. You can specify which kinds of reports you want generated with the reporting commands shown in Table 11–2.

Table 11–2. Reporting Commands

Object	Command	Description
Design	report_design	Reports design characteristics
	report_area	Reports design size and object counts
	report_hierarchy	Reports design hierarchy
	report_resources	Reports resource implementations
	report_fpga	Reports FPGA resource utilization statistics for the design
Instances	report_cell	Displays information about instances
References	report_reference	Displays information about references
Ports	report_port	Displays information about ports
	report_bus	Displays information about bused ports
Nets	report_net	Reports net characteristics
	report_bus	Reports bused net characteristics
Clocks	report_clock	Displays information about clocks
Timing	report_timing	Checks the timing of the design
	report_constraint	Checks the design constraints
	check_timing	Checks for unconstrained timing paths and clock-gating logic
	report_design	Shows operating conditions, timing ranges, internal input and output, and disabled timing arcs
	report_port	Shows unconstrained input and output ports and port loading
	report_timing_requirements	Shows all timing exceptions set on the design
	report_clock	Checks the clock definition and clock skew information
	derive_clocks	Checks internal clock and unused registers
	report_path_group	Shows all timing path groups in the design
Cell Attributes	get_cells	Shows all cell instances that have a specific attribute

For more information about the usage of these commands, refer to the *Synopsys DC FPGA User Guide*.

The DC FPGA software only provides preliminary estimates of your design's timing delays because the timing of your design cannot be accurately predicted until the Quartus II software has placed and routed your design.

Saving Synthesis Results

After synthesis, the technology-mapped design can be saved to a file in one of the following four formats: Verilog HDL, VHDL, Synopsys internal DB, or EDIF.

The Quartus II software accepts an EDIF netlist or Verilog Quartus Mapping netlist synthesized from the DC FPGA software. The default output netlist from the DC FPGA software is Verilog Quartus Mapping. The Verilog Quartus Mapping File format follows a subset of Verilog HDL rules. You can use the same Verilog Quartus Mapping netlist format with the Quartus II software and formal verification.

Use the `write` command to save your design work. The syntax for this command is shown in Example 11–6.

Example 11–6. Syntax Using the write Command

```
write -format <verilog|db|edif> -output <file name> <design list>
[-hierarchy] ↵
```

The `-hierarchy` option causes the DC FPGA software to write all the designs within the hierarchy of the current design. The DC FPGA default flow to interface with Quartus II software uses the Verilog Quartus Mapping netlist.

To generate a Verilog Quartus Mapping netlist, set the required settings using the commands shown in Example 11–7.

Example 11–7. Generating a Verilog Quartus Mapping Netlist

```
define_name_rules ALTERA -remove_internal_net_bus
change_names -rules ALTERA -hier
change_names –rules verilog –hier
write -format verilog -hier -o <design_top>.vqm
```

The Synopsys internal DB format is useful when you have synthesized your design and want to reuse it later in the DC FPGA software. The DB file contains your constraints and synthesized design netlist, and loads into the DC FPGA software faster than Verilog HDL or VHDL designs.

You can also write out your design constraints in Tcl format for export to the Quartus II software with the `write_par_constraint` command or by using the write_fpga command. These commands are explained in "Exporting Designs to the Quartus II Software".

Exporting Designs to the Quartus II Software

The DC FPGA software can create two Tcl scripts that start the Quartus II software, create your initial design project, apply the exported timing constraints, and compile your design in the Quartus II software.

You can generate the two Tcl scripts by using write and `write_par_constraint` command together, or by using the `write_fpga` command alone.

write_fpga Command

The recommended method to export all of the place-and-route files from the DC FPGA software is to use the `write_fpga` command. This command is used after the compile. Example 11–8 shows how the `write_fpga` command is used.

Example 11–8. Using the write_fpga Command after Compile

```
compile
write_fpga <outputdir>
```

The `write _fpga` command will do the following in one step:

Example 11–9. Using the write_fpga Command to Generate All Files

```
write -hier -f db -o $outputdir/top_module.db
write –hier –f edif –o $outputdir/top_module.edf
define_name_rules ALTERA -remove_internal_net_bus
change_names -rules ALTERA -hier
change_names –rules verilog –hier
write -format verilog -hier -o <design_top>.vqm
write_par_constraint $outputdir/top_module_quartus_setup.tcl
```

When you use the `write_fpga` command, it generates all files in the current work directory or in the directory you specify (entering an output directory is optional) and generates the output files based on the current design file name.

write & write_par_constraint Commands

The `write` command is used to generate a post synthesis netlist for place-and-route and formal verification. You should use a Verilog Quartus Mapping formatting netlist to work with the Quartus II software, beginning with the DC FPGA software, version 2005.09. Example 11–10 uses the write and write_par_constraint commands to generate the Verilog Quartus Mapping File and Tcl scripts:

Example 11–10. Using the write & write_par_constraint Commands

```
define_name_rules ALTERA -remove_internal_net_bus
change_names -rules ALTERA -hier
change_names –rules verilog –hier
write -format verilog -hier -o <design_top>.vqm
```

Tcl scripts that start the Quartus II software and forward annotate the timing constraints can be generated using the write_par_constraint command.

`write_par_constraint` <*user-specified file name*>`.tcl` ↵

This command generates both Tcl scripts in one operation. The first Tcl script has the name you specify in the `write_par_constraint` command. This script creates and compiles your Quartus II project. The second script is automatically generated and named <*top_module*>_const**.tcl** by default and contains your exported timing constraints from the DC FPGA software. This constraint file is sourced by the <*user-specified file name*>**.tcl** script and applies the timing constraints used in the DC FPGA software to your project in the Quartus II software.

For example, if your design is called **dma_controller**, and you run the command, `write_par_constraint run_quartus.tcl`, the DC FPGA software produces two Tcl scripts called `run_quartus.tcl` and `dma_controller_const.tcl`.

Using Tcl Scripts with Quartus II Software

To use this Tcl script in the Quartus II Tcl shell, type the following command at a command prompt:

`quartus_sh -t` <*user-specified file name*>`.tcl` ↵

To run this Tcl script in the Quartus II software GUI, type the following command at the Quartus II Tcl console prompt:

`source` <*user-specified file name*>`.tcl` ↵

The ability to run scripts in the Tcl console is useful when performing an initial compilation of your design to view post place-and-route timing and device utilization results, but the advanced Quartus II options that control the compilation process are not available.

To create a Quartus II project without performing compilation automatically, remove these lines from the script:

```
load_package flow
execute_flow -compile
```

Example 11–11. An Example Script

```
###############################################################################
# Generated by DC FPGA X-2005.09 on Wed Aug 10 04:20:01 2005
#
# Description: This TCL script is generated by DC FPGA using
#              write_par_constraint command. It is used to create a new Quartus
#              II project, specify timing constraint assignments in Quartus II,
#              and run quartus_map, quartus_fit, quartus_tan, & quartus_asm.
#
# Usage:  To execute this TCL script in batch mode: quartus_sh -t turboTop.tcl
#         To execute this TCL script in Quartus II GUI: source turboTop.tcl
#
#
#************    WARNING    **********    WARNING    ***************************
#
# Please ensure the P&R netlist name is represented correctly in this tcl file.
# You may need to change the file_name variable to match your actual netlist
# name.
#
###############################################################################

# Set the file_name and  project_name variable
set file_name turboTop.vqm
set project_name turboTop

# Close the project if open
if [is_project_open] {
   project_close
}

# Create a new project
project_new -overwrite -family STRATIXII -part EP2S30F484C3 $project_name

# Make global assignments
set_global_assignment -name TOP_LEVEL_ENTITY $project_name

###############################################################################
# if you are using Verilog P&R netlist, please comment out EDIF assignment
# and uncomment the VERILOG assignment below.

#set_global_assignment -name EDIF_FILE $file_name
set_global_assignment -name  VQM_FILE $file_name
###############################################################################
```

```
set_global_assignment -name ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP ON
#set_global_assignment -name ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP OFF
set_global_assignment -name EDA_DESIGN_ENTRY_SYNTHESIS_TOOL -value "Design Compiler FPGA"
set_global_assignment -name EDA_INPUT_VCC_NAME -value VDD -section_id
eda_design_synthesis
set_global_assignment -name EDA_INPUT_GND_NAME -value GND -section_id
eda_design_synthesis
set_global_assignment -name EDA_LMF_FILE -value dc_fpga.lmf -section_id
eda_design_synthesis
set_global_assignment -name VERILOG_LMF_FILE dc_fpga.lmf
set_global_assignment -name FITTER_EFFORT "STANDARD FIT"

# Source in the design timing constraint file
source $project_name\_cons.tcl

# The following runs quartus_map, quartus_fit, quartus_tan, & quartus_asm
load_package flow
execute_flow -compile
project_close
```

After synthesis in the DC FPGA software, the technology-mapped design is written to the current project directory as an Verilog Quartus Mapping netlist file. The project configuration script (<*user-specified file name*>**.tcl**) is used to create and compile a Quartus II project containing your Verilog Quartus Mapping netlist. The example script makes basic project assignments such as assigning the target device as specified in the DC FPGA software. The project configuration script calls the place-and-route constraints script to make your timing constraints. The place-and-route constraints script (<*top module*>_const**.tcl**) forward-annotates the timing constraints that you made in the DC FPGA software, including false path assignments, multi-cycle assignments, timing groups, and related clocks. This integration means that you need to enter these constraints only once, in the DC FPGA software, and they are passed automatically to the Quartus II software.

Place & Route with the Quartus II Software

After you have created your Quartus II project and successfully loaded your Verilog Quartus Mapping netlist into the Quartus II project, you can use the Quartus II software to perform place-and-route. The Synopsys DC FPGA software uses only worst case timing delays and constraints, and does not optimize minimum timing requirements. Altera recommends that you add minimum timing constraints and perform minimum timing analysis in the Quartus II software.

For more information about these advance features, area optimization, and timing closure, refer to the *Quartus II Handbook*.

You can use the Quartus II software to obtain accurate prediction of post-conversion f_{MAX} performance and power consumption characteristics when migrating from a high-density FPGA to a cost-optimized, high-volume structured ASIC such as a HardCopy Stratix device.

The Quartus II software place-and-route algorithms can use register packing, register retiming, automatic logic duplication, and what-you-see-is-what-you-get (WYSIWYG) primitive re-synthesis technologies to increase logic utilization in your device and to deliver superior f_{MAX} performance at extremely high logic utilization.

For more information, refer to the *Quartus II Support for HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook.*

Formality Software Support

Beginning with version 4.2, the Quartus II software interfaces with the Formality software from Synopsys. Formality software verifies logic equivalency between the RTL and DC FPGA post-synthesis netlist, and between the DC FPGA post-synthesis netlist and the Quartus II post-place-and-route netlist. A synthesized verilog netlist generated by the DC FPGA is required to use with formality flow. Formality supports Stratix II, Stratix and Stratix GX device families.

For more information about how to set the required synthesis settings to generate a valid formal verification netlist and to use the Formality software for equivalence checking, refer to the *Synopsys Formality Support* chapter in volume 3 of the *Quartus II Handbook*.

Conclusion

Large FPGA designs require advanced synthesis of their HDL code. Taking advantage of the Synopsys DC FPGA software and the Quartus II software allows you to develop high-performance designs while occupying as little programmable logic resources as possible. The DC FPGA software and Quartus II software combination is an excellent solution for the high density designs using Altera FPGA devices.

12. Analyzing Designs with Quartus II Netlist Viewers

QII51013-6.0.0

Introduction

As FPGA designs grow in size and complexity, the ability to analyze how your synthesis tool interprets your design becomes critical. With today's advanced designs, often several design engineers are involved in coding and synthesizing different design blocks, making it difficult to analyze and debug the design. The Quartus® II RTL Viewer, State Machine Viewer, and Technology Map Viewer provide powerful ways to view your initial and fully mapped synthesis results during the debugging, optimization, or the constraint entry process.

The first section in this chapter, "When to Use Viewers: Analyzing Design Problems" describes examples of using the viewers to analyze your design at various stages of the design cycle. The following sections provide an introduction to the Quartus II design flow using the netlist viewers, an overview of each viewer, and an explanation of the user interface. The next sections describe the following activities:

- How to navigate and filter schematics
- How to probe to and from other windows within the Quartus II software
- How to view a timing path from the Timing Analyzer report

The final section "Debugging HDL Code with the State Machine Viewer" on page 12–45 provides a detailed example that uses the viewer to analyze a design and quickly resolve a design problem.

When to Use Viewers: Analyzing Design Problems

You can use the netlist viewer to analyze your design to see how it was interpreted by the Quartus II software. This section provides simple examples of how to use the RTL, State Machine, and Technology Map Viewers to analyze problems encountered in the design process.

For more explanation about how the netlist viewers display your design, refer to the following sections:

- Quartus II Design Flow with the Netlist Viewers
- RTL Viewer Overview
- State Machine Viewer Overview
- Technology Map Viewer Overview

To see the user interface for the netlist viewers, refer to "Introduction to the User Interface" on page 12–7.

Using the RTL Viewer is a good way to view your initial synthesis results to determine whether you have created the desired logic, and that the logic and connections have been interpreted correctly by the software. You can use the RTL Viewer and the State Machine Viewer to visually check your design before simulation or other verification processes. Catching design errors at this early stage of the design process can save you valuable time.

If you see unexpected behavior during verification, this is another good opportunity to use the RTL Viewer to trace through the netlist and ensure that the connections and the logic in your design are as expected. You can also use the State Machine Viewer to view state machine transitions and transition equations. Viewing the design can help you find and analyze the source of design problems. If your design looks correct in the RTL Viewer, you know to focus your analysis on later stages of the design process and investigate potential timing violations or issues in the verification flow itself.

You can use the Technology Map viewer to look at the results at the end of synthesis by running the viewer after performing Analysis & Synthesis, or the results after placement and routing by running the viewer after running the Fitter.

In addition, you can use the RTL Viewer or Technology Map Viewer to locate the source of a particular signal, which can help you debug your design. Use the navigation techniques described in this chapter to search easily through the design. You can trace back from a point of interest to find the source of the signal and ensure the connections are as expected.

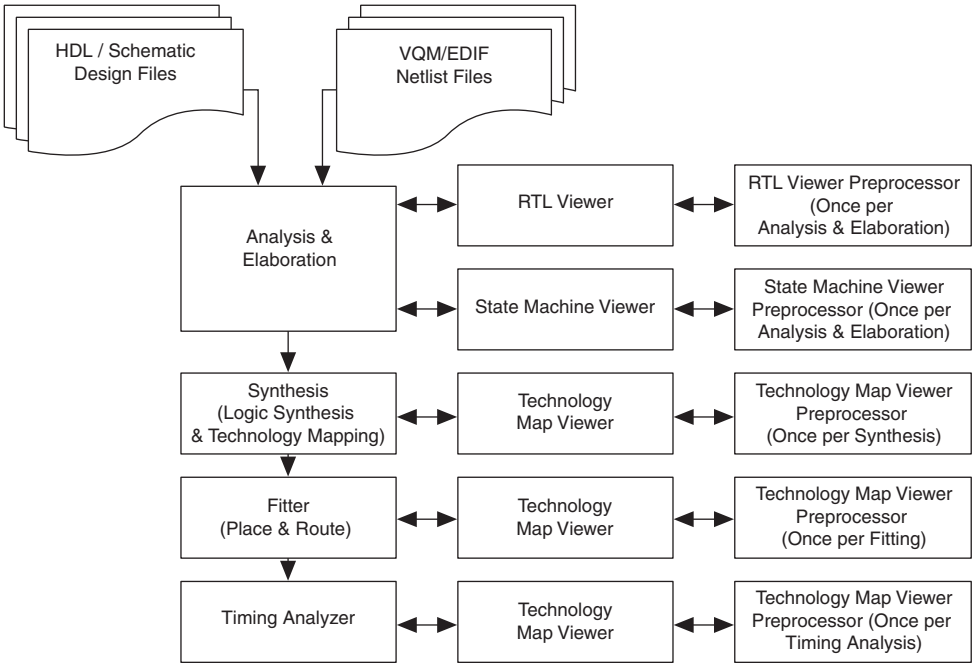
You also can use the Technology Map Viewer to help you locate post-synthesis nodes in your netlist and make assignments when optimizing your design. This functionality can be useful, for example, when making a multicycle clock timing assignment between two registers in your design. You can start at an I/O port and trace forward or backwards through the design and through levels of hierarchy to find nodes that interest you, or to locate a specific register by visually inspecting the schematic.

The RTL Viewer, State Machine Viewer, and Technology Map Viewer can be used in many other ways throughout the design, debugging, and optimization stages. Viewing the design netlist is a powerful way to analyze design problems. This chapter shows how you can use the various features of the netlist viewers to increase your productivity when analyzing a design.

Quartus II Design Flow with the Netlist Viewers

The first time you open one of the netlist viewers after compiling the design, a preprocessor stage runs automatically before the viewer opens. If you close the viewer and open it again later without recompiling the design, the viewer opens immediately without performing the preprocessing stage. Figure 12–1 shows how the netlist viewers fit into the basic Quartus II design flow.

Figure 12–1. Quartus II Design Flow Including the RTL Viewer & Technology Map Viewer



Each viewer requires that your design has been compiled with the minimum compilation stage listed below before the viewer can run the preprocessor and open the design.

- To open the RTL Viewer or State Machine Viewer, you must first perform at least **Analysis & Elaboration**.
- To open the Technology Map Viewer, you must first perform at least **Analysis & Synthesis**.

If you open one of the viewers without first compiling the design with the appropriate minimum compilation stage, the viewer does not appear. Instead, the Quartus II software issues an error message instructing you to run the necessary compilation stage and restart the viewer.

Both viewers display the results of the last successful compilation. Therefore, if you make a design change that causes an error during Analysis & Elaboration, you cannot view the netlist for the new design files, but you can still see the results from the last successfully compiled version of the design files. If you receive an error during compilation and you have not yet successfully run the appropriate compilation stage for your project, the viewer cannot be displayed; in this case, the Quartus II software issues an error message when you try to open the viewer.

If the viewer window is open when you start a new compilation, the viewer closes automatically. You must open the viewer again to view the new design netlist after compilation completes successfully.

RTL Viewer Overview

The Quartus II RTL Viewer allows you to view a register transfer level (RTL) graphical representation of your Quartus II integrated synthesis results or your third-party netlist file within the Quartus II software.

You can view results after Analysis & Elaboration when your design uses any supported Quartus II design entry method, including Verilog HDL Design files (**.v**), VHDL (**.vhd**), AHDL Text Design Files (**.tdf**), schematic Block Design Files (**.bdf),** or schematic Graphic Design Files (**.gdf)** imported from the MAX+PLUS® II software. You can also view the hierarchy of atom primitives (such as device logic cells and I/O ports) when your design uses a synthesis tool to generate a Verilog Quartus Mapping File (**.vqm**) or Electronic Design Interchange Format (**.edf**) netlist file. Refer to Figure 12–1, "Quartus II Design Flow Including the RTL Viewer & Technology Map Viewer" for a flow diagram.

The Quartus II RTL Viewer displays a schematic view of the design netlist after analysis and elaboration or netlist extraction is performed by the Quartus II software, but before technology mapping and any synthesis or fitter optimization algorithms occur. This view is not the final design structure because optimizations have not yet occurred. This view most closely represents your original source design. If you synthesized your design using the Quartus II integrated synthesis, this view shows how the Quartus II software interpreted your design files. If you are using a third-party synthesis tool, this view shows the netlist written by your synthesis tool.

When displaying your design, the RTL Viewer optimizes the netlist to maximize readability in the following ways:

- Logic with no fan-out (its outputs are unconnected) and logic with no fan-in (its inputs are unconnected) are removed from the display.
- Default connections such as VCC and GND are not shown.
- Pins, nets, wires, module ports, and certain logic are grouped into buses where appropriate.
- Constant bus connections are grouped.
- Values are displayed in hexadecimal format.
- NOT gates are converted to bubble inversion symbols in the schematic.
- Chains of equivalent combinational gates are merged into a single gate, for example, a 2-input AND gate feeding a 2-input AND gate is converted to a single 3-input AND gate.
- State machine logic is converted into a state diagram, state transition table and state encoding table which are displayed in the State Machine Viewer.

To run the RTL Viewer for a Quartus II project, first analyze the design to generate an RTL netlist. To analyze the design and generate an RTL netlist, on the Processing menu, point to Start and click **Start Analysis & Elaboration**. You can also perform a full compilation or any process that includes the initial Analysis & Elaboration stage of the Quartus II compilation flow.

To run the viewer, on the Tools menu, point to Netlist Viewers and click **RTL Viewer**, or select **RTL Viewer** from the **Applications** toolbar.

The **Applications** toolbar does not display by default in the Quartus II user interface. To add the toolbar, on the Tools menu, click **Customize**. On the **Customize** dialog box, click the **Toolbars** tab under **Toolbars**, and turn on **Applications**. Click **Close**.

State Machine Viewer Overview

The State Machine Viewer presents a high-level view of finite state machines in your design. The State Machine Viewer provides a graphical representation of the states and their related transitions, as well as a state transition table that displays the condition equation for each of the state transitions, and encoding information for each state.

To run the State Machine Viewer, on the Tools menu, point to Netlist Viewers and click **State Machine Viewer**. To open the State Machine Viewer for a particular state machine, double-click the state machine instance in the RTL Viewer, or right-click the state machine instance, and click **Hierarchy Down**.

Technology Map Viewer Overview

The Quartus II Technology Map Viewer provides a technology-specific, graphical representation of your design after Analysis & Synthesis or the Fitter has mapped your design into the target device. The Technology Map Viewer shows the hierarchy of atom primitives (such as device logic cells and I/O ports) in your design. For supported families, you can also view the internal registers and look-up tables inside logic cell (LCELL) and registers in I/O atom primitives. Refer to "Viewing Contents of Atom Primitives in the Technology Map Viewer" on page 12–21 for details.

Where possible, the port names of each hierarchy are maintained throughout synthesis. However, port names may change or be removed from the design. For example, if a port is unconnected or driven by `GND` or VCC, it is removed during synthesis. When a port name is changed, the port is assigned a related user logic name in the design, or a generic port name such as `IN1` or `OUT1`.

You can view your Quartus II technology-mapped results after synthesis, fitting, or timing analysis. To run the Technology Map Viewer for a Quartus II project, on the Processing menu, point to Start and click **Start Analysis & Synthesis** to first synthesize and map the design to the target technology. You also can perform a full compilation, or any process that includes the synthesis stage in the compilation flow.

If you have completed the Fitter stage, the Technology Map Viewer shows the changes made to your netlist by the Fitter, such as physical synthesis optimizations. If you have completed the Timing Analysis stage, you can locate timing paths from the Timing Analyzer report in the Technology Map Viewer (refer to "Viewing a Timing Path" on page 12–37 for details). Refer to Figure 12–1 for a flow diagram.

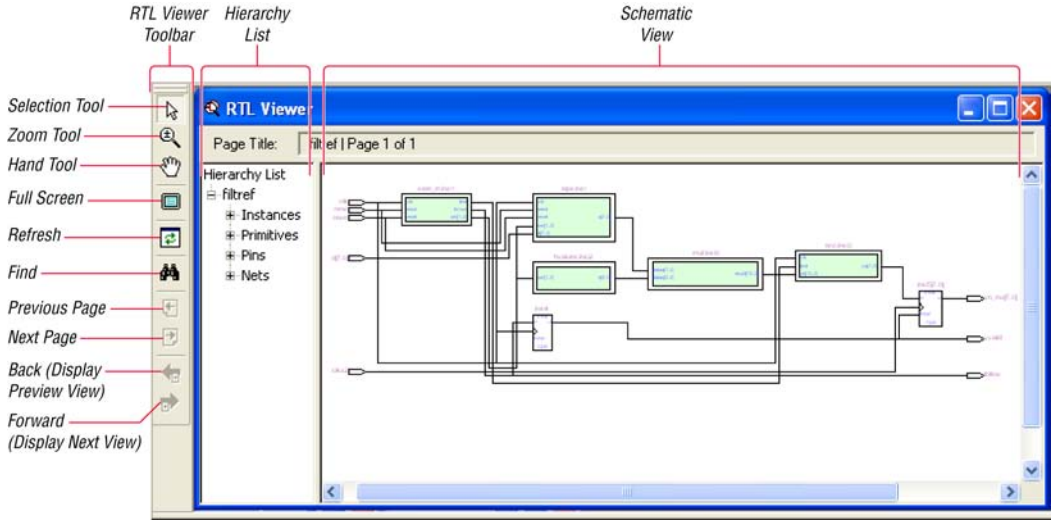
To run the viewer, on the Tools menu, point to Netlist Viewers and click **Technology Map Viewer**, or select **Technology Map Viewer** from the **Applications** toolbar.

Introduction to the User Interface

The RTL Viewer window and Technology Map Viewer window each consist of two main parts: the schematic view and the hierarchy list. Figure 12–2 shows the RTL Viewer window and indicates these two parts. Both viewers also contain a toolbar that gives you tools to use in the schematic view.

You can have only one RTL Viewer and one Technology Map Viewer window open at a time, although each window can show multiple pages. The window for each viewer has characteristics similar to other "child" windows in the Quartus II software; it can be resized and moved, minimized or maximized, tiled or cascaded, and moved in front of or behind other windows.

Figure 12–2. RTL Viewer Window & RTL Toolbar



Schematic View

The schematic view is shown on the right side of the RTL Viewer and Technology Map Viewer. It contains a schematic representing the design logic in the netlist. This is the main screen for viewing your gate-level netlist in the RTL Viewer and your technology-mapped netlist in the Technology Map Viewer.

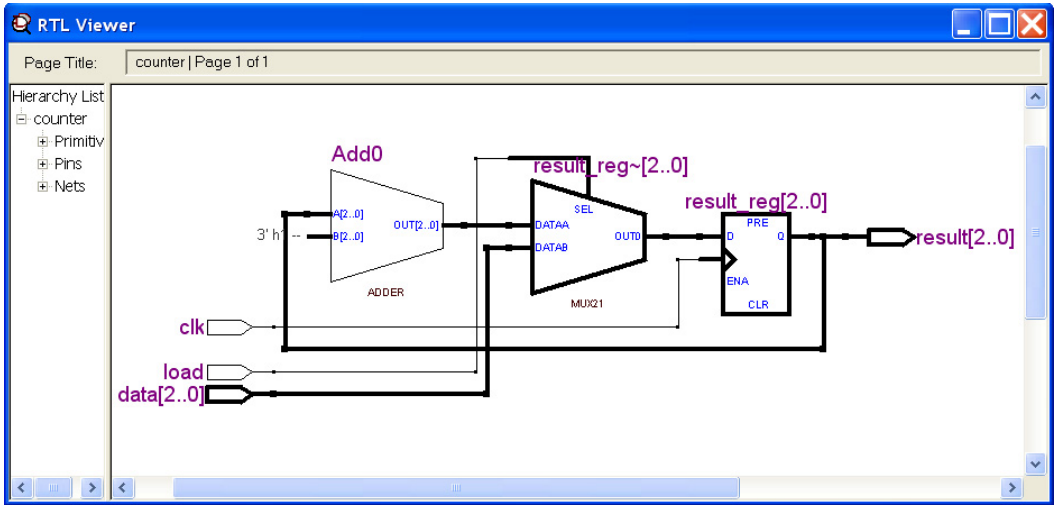
Schematic Symbols

The symbols for nodes in the schematic represent elements of your design netlist. These elements include input and output ports, registers, logic gates, Altera primitives, high-level operators, and hierarchical instances.

Figure 12–3 shows an example of an RTL Viewer schematic for a 3-bit synchronous loadable counter. The "Code Sample for Counter Schematic Shown in Figure 12–3" section shows the Verilog HDL code that produced this schematic. In this example, there are multiplexers and a group of registers (Table 12–1) in a bus along with an ADDER operator (Table 12–3) inferred by the counting function in the HDL code.

The schematic displays wire connections between nodes with a thin black line, and bus connections with a thick black line (Figure 12–3).

Figure 12–3. Example Schematic Diagram in the RTL Viewer



Example 12–1. Code Sample for Counter Schematic Shown in Figure 12–3

```
module counter (input [2:0] data, input clk, input load, output [2:0] result);
    reg [2:0] result_reg;
    always @ (posedge clk)
        if (load)
            result_reg <= data;
        else
            result_reg <= result_reg + 1;
    assign result = result_reg;
endmodule
```

Figure 12–4 shows a portion of the corresponding Technology Map Viewer schematic with a compiled design that targets a Stratix® device. In this schematic, you can see the LCELL (logic cell) device-specific primitives that represent the counter function, labeled with their post-synthesis node names. The REGOUT port represents the output of the register in the LCELL, and the COMBOUT port represents the output of the combinational logic in the look-up table (LUT) of the LCELL. The hexadecimal number in parentheses below each LCELL primitive represents the LUT mask, which is a hexadecimal representation of the logic function of the LCELL.

Figure 12–4. Example Schematic Diagram in the Technology Map Viewer

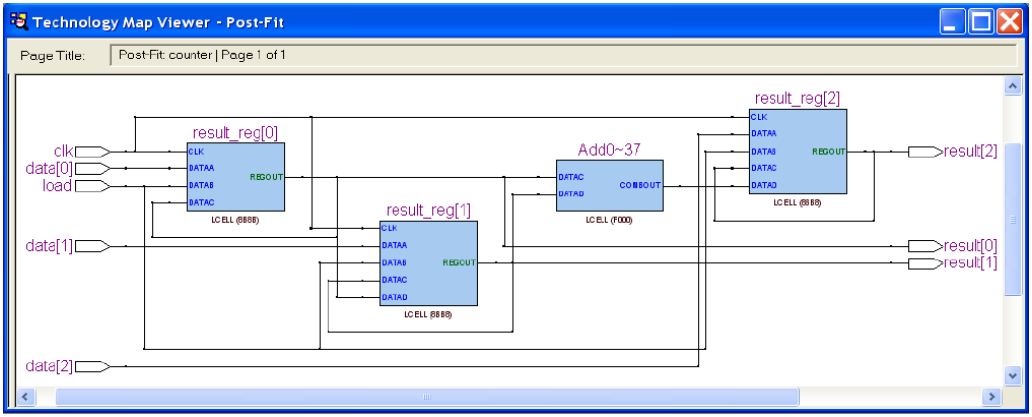


Table 12–1 lists and describes the primitives and basic symbols that you can display in the schematic view of the RTL Viewer and Technology Map Viewer. Table 12–3 on page 12–13 lists and describes the additional higher level operator symbols used in the RTL Viewer schematic view.

The logic gates and operator primitives appear only in the RTL Viewer. Logic in the Technology Map Viewer is represented by atom primitives such as LCELL.

Table 12–1. Symbols in the Schematic View (Part 1 of 3)

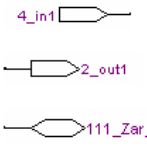
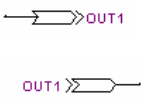
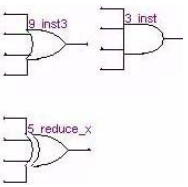
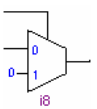
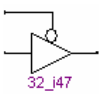
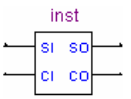
Symbol	Description
I/O Ports 	An input, output, or bidirectional port in the current level of hierarchy. A device input, output, or bidirectional pin when viewing the top-level hierarchy. The symbol can represent a bus. Only one wire is connected to the bidirectional symbol, representing both the input and the output paths. Input symbols appear on the left-most side of the schematic, while output and bidirectional symbols appear on the right-most side of the schematic.
I/O Connectors 	An input or output connector, representing a net that comes from another page of the same hierarchy (refer to "Partitioning the Schematic into Pages" on page 12–24). To go to the page that contains the source or the destination, right-click on the net and choose the page from the menu (refer to "Following Nets across Schematic Pages" on page 12–25).
Hierarchy Port Connect 	A connector representing a port relationship between two different hierarchies. A connector indicates that a path passes through a port connector in a different level of hierarchy.
OR, AND, XOR Gates 	An OR, AND, or XOR gate primitive (the number of ports can vary). A small circle (bubble symbol) on an input or output indicates that the port is inverted.
MUX 	A multiplexer (MUX) primitive with a selector port that selects between port 0 and port 1. A MUX with more than two inputs is displayed as an operator (refer to "Operator Symbols in the RTL Viewer Schematic View" on page 12–13).
BUFFER 	A buffer primitive. The figure shows the tri-state buffer, with an inverted output enable port. Other buffers without an enable port include LCELL, SOFT, CARRY, and GLOBAL. The NOT gate and EXP expander buffers use this symbol without an enable port and with an inverted output port.
CARRY_SUM 	A CARRY_SUM buffer primitive, where SI represents SUM IN, SO represents SUM OUT, CI represents CARRY IN, and CO represents the CARRY OUT port of the buffer.

Table 12–1. Symbols in the Schematic View (Part 2 of 3)

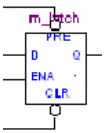
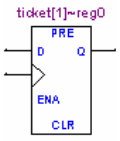
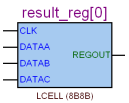
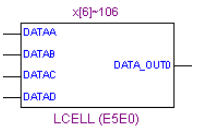
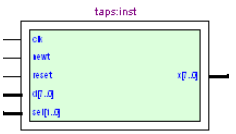
Symbol	Description
LATCH 	A latch primitive with D data input, EN enable input, Q data output, and PRE preset and CLR clear ports.
DFFE/DFFEA/DFFAES 	A DFFE (data flipflop with enable) primitive, with the same ports as a latch and a clock trigger. The other flipflop primitives are similar: DFFEA (data flipflop with enable and asynchronous load) primitive with additional ALOAD asynchronous load and ADATA data signals, and DFFEAS (data flipflop with enable and both synchronous and asynchronous load) which has ASDATA as the secondary data port.
Atom Primitive 	Primitives are low-level nodes that cannot be expanded to any lower hierarchy. The symbol displays the port names, the primitive type, and its name. The blue shading indicates an atom primitive in the Technology Map Viewer which allows you to view the internal details of the primitive. Refer to "Viewing Contents of Atom Primitives in the Technology Map Viewer" on page 12–21 for details.
Other Primitive 	Any primitive that does not fall into the categories above. Primitives are low-level nodes that cannot be expanded to any lower hierarchy. The symbol displays the port names, the primitive or operator type, and its name. The figure shows an LCELL WYSIWYG primitive, with DATAA to DATAD and COMBOUT port connections. This type of LCELL primitive would be found in the Technology Map Viewer for technology-specific atom primitives when the contents of the atom primitive cannot be viewed. The RTL Viewer contains similar primitives if the source design was a VQM or EDIF netlist.
Instance 	An instance in the design that does not correspond to a primitive or operator (generally a user-defined hierarchy block), indicated by the double outline and green shading. The symbol displays the instance name. To open the schematic for the lower level hierarchy, right-click and choose the appropriate command (refer to "Traversing & Viewing the Design Hierarchy" on page 12–20).

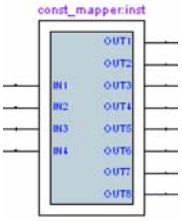
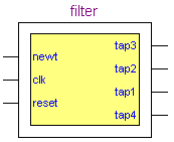
Table 12–1. Symbols in the Schematic View (Part 3 of 3)	
Symbol	**Description**
Encrypted Instance 	A user-defined encrypted instance in the design, indicated by the double outline and gray shading. The symbol displays the instance name. You cannot open the schematic for the lower level hierarchy, because the source design is encrypted.
State Machine Instance 	A finite state machine instance in the design, indicated by the double outline and yellow shading. Double-clicking this instance opens the State Machine Viewer. Refer to"State Machine Viewer" on page 12–17 for more details.

Table 12–2 lists and describes the symbol used only in the State Machine Viewer.

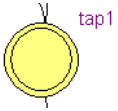
Table 12–2. Symbol Available only in the State Machine Viewer	
Symbol	**Description**
State Node 	The node representing a state in a finite state machine. State transitions are indicated with arcs between state nodes. The double circle border indicates the state connects to logic outside the state machine, while a single circle border indicates the state node does not feed outside logic.

Table 12–3 lists and describes the additional higher level operator symbols used in the RTL Viewer schematic view.

Table 12–3. Operator Symbols in the RTL Viewer Schematic View (Part 1 of 2)

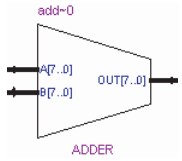
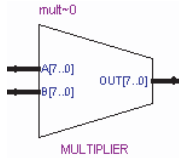
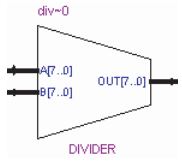
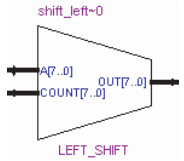
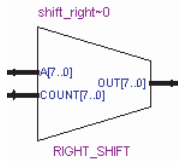
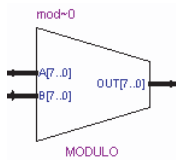
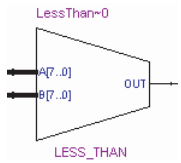
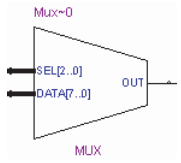
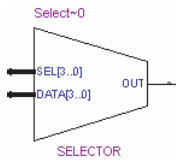
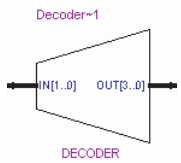
Symbol	Description
	An adder operator: `OUT = A + B`
	A multiplier operator: `OUT = A × B`
	A divider operator: `OUT = A / B`
	A left shift operator: `OUT = (A << COUNT)`
	A right shift operator: `OUT = (A >> COUNT)`
	A modulo operator: `OUT = (A % B)`

Table 12–3. Operator Symbols in the RTL Viewer Schematic View (Part 2 of 2)

Symbol	Description
	A less than comparator: `OUT = (A <= B : A < B)`
	A multiplexer: `OUT = DATA [SEL]` The data range size is $2^{\text{sel range size}}$
	A multiplexer with one-hot select input, and more than two input signals.
	A binary number decoder: `OUT` = (binary_number (`IN`) == x) for x=0 to $x=2^{(n+1)} - 1$

Selecting an Item in the Schematic View

To select an item in the schematic view, ensure that the **Selection Tool** is enabled in the viewer toolbar (this tool is enabled by default). Click on an item in the schematic view to highlight it in red.

Select multiple items by pressing the Shift or Ctrl key while selecting with your mouse. You also can select all nodes in a region by selecting a rectangular box area with your mouse cursor when the **Selection Tool** is enabled. To select nodes in a box, move your mouse to one corner of the area you want to select, click the mouse button, and drag the mouse to the opposite corner of the box, then release the mouse button. By default, creating a box like this highlights and selects all nodes in the selected area (instances, primitives, and pins), but not the nets. The **Viewer Options** dialog box provides an option to select nets. To include nets, right-click in the schematic and click **Viewer Options**. In the **Net Selection** section, turn on the **Select entire net when segment is selected** option.

Items selected in the schematic view are automatically selected in the hierarchy list (refer to the "Hierarchy List" on page 12–15). The list expands automatically if required to show the selected entry. However, the list does not collapse automatically when entries are not being used or are deselected.

When you select a hierarchy box, node, or port in the schematic view, the item is highlighted in red but none of the connecting nets are highlighted. When you select a net (wire or bus) in the schematic view, all connected nets are highlighted in red. The selected nets are highlighted across all hierarchy levels and pages. Net selection can be useful when navigating a netlist because you see the net highlighted when you traverse between hierarchy levels or pages.

In some cases, when you select a net that connects to nets in other levels of the hierarchy, these connected nets also are highlighted in the current hierarchy. If you prefer that these nets are not highlighted, use the **Viewer Options** dialog box option to highlight a net only if the net is in the current hierarchy. Right-click in the schematic, and click **Viewer Options**. In the **Net Selection** section, turn on the **Limit selections to current hierarchy** option.

Moving & Panning in the Schematic View

When the schematic view page is larger than the portion currently displayed, you can use the scroll bars at the bottom and right side of the schematic view to see other areas of the page.

You can also use the Hand Tool to "grab" the schematic page and drag it in any direction. Enable the Hand Tool with the toolbar button. Click and drag to move around the schematic view without using the scroll bars.

Hierarchy List

The hierarchy list is displayed on the left side of the viewer window. The hierarchy list displays the entire netlist in a "tree" format based on the hierarchical levels of the design. Using the hierarchy list, you can traverse through the design hierarchy to view the logic schematic for each level. You also can select an element in the hierarchy list that you want to see highlighted in the schematic view.

Nodes inside atom primitives are not listed in the hierarchy list.

For each module in the design hierarchy, the hierarchy list displays the the applicable elements listed in Table 12–4. Click the + icon to expand an element.

Table 12–4. Hierarchy List Elements

Elements	Description
Instances	Modules or instances in the design that can be expanded to lower hierarchy levels.
State Machines	State machine instances in the design that can be viewed in the State Machine Viewer.
Primitives	Low-level nodes that cannot be expanded to any lower hierarchy level. These include registers and gates that you can view in the RTL Viewer when using Quartus II integrated synthesis, or logic cell atoms in the Technology Map Viewer or in the RTL Viewer when using a VQM or EDIF from third-party synthesis software. In the Technology Map Viewer, you can view the internal implementation of certain atom primitives, but you can not traverse into a lower level of hierarchy.
Pins	The I/O ports in the current level of hierarchy. • Pins are device I/O pins when viewing the top hierarchy level, and are I/O ports of the design when viewing the lower levels. • When a pin represents a bus or an array of pins, expand the pin entry in the list view to see individual pin names.
Nets	Nets or wires connecting the nodes. When a net represents a bus or array of nets, expand the net entry in the tree to see individual net names.

Selecting an Item in the Hierarchy List

When you click any item in the hierarchy list, the viewer performs the following actions:

- Searches for the item in the currently viewed pages, and displays the page containing the selected item in the schematic view if it is not currently displayed. (If you are currently viewing a filtered netlist, for example, the relevant page within the filtered netlist is displayed.)
- If the selected item is not found in the currently viewed pages, the entire design netlist is searched, and the item is displayed in a default view.
- Highlights the selected item in red in the schematic view.

When you double-click an instance in the hierarchy list, the viewer displays the underlying implementation of the instance.

You can select multiple items by pressing the Shift or Ctrl key while selecting with your mouse. When you right-click an item in the hierarchy list, you can navigate in the schematic view using the **Filter** and **Locate** commands. Refer to "Filtering in the Schematic View" on page 12–27 and "Probing to Source Design File & Other Quartus II Windows" on page 12–35 for more information.

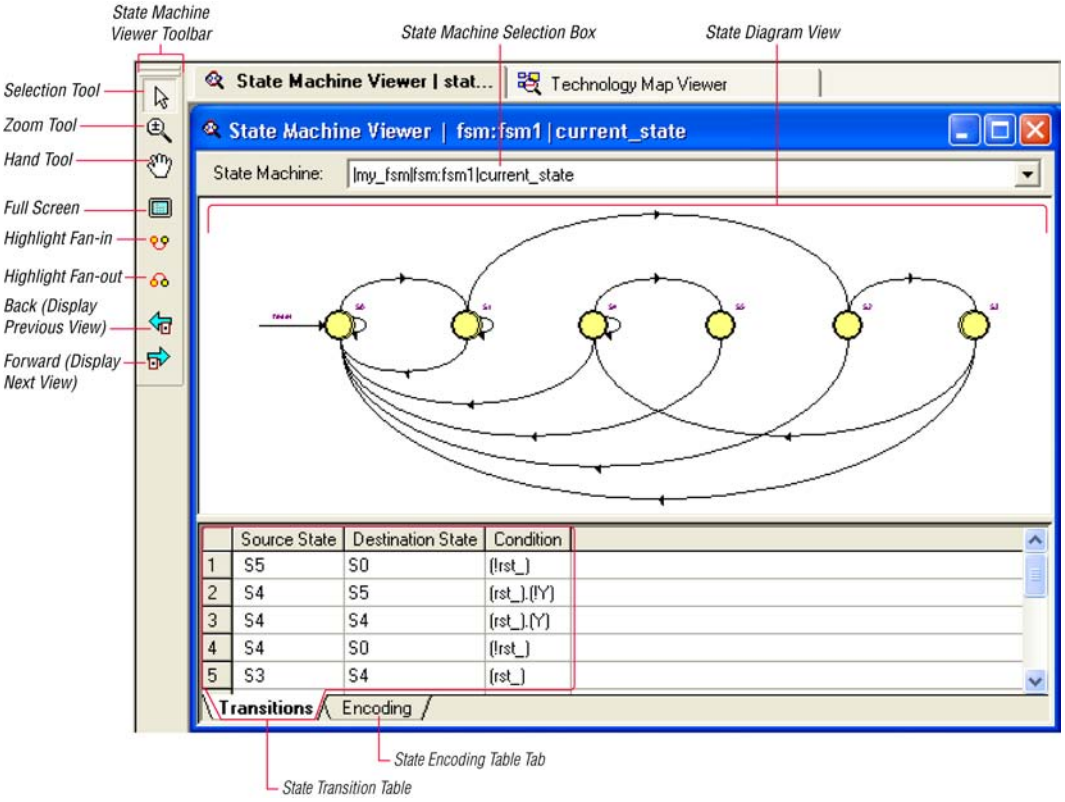
State Machine Viewer

The State Machine Viewer displays a graphical representation of the state machines in your design. You can open the State Machine Viewer in any of the following ways:

- On the Tools menu, point to Netlist Viewers, and click **State Machine Viewer**
- Double-click on a state machine instance in the RTL Viewer
- Right-click on a state machine instance in the RTL Viewer, and click **Hierarchy Down**
- Select a state machine instance in the RTL Viewer, and on the Project menu, point to Hierarchy and click **Down**

Table 12–5 shows an example of the State Machine Viewer for a simple state machine. The State Machine toolbar on the left side of the viewer provides tools you can use in the state diagram view.

Figure 12–5. State Machine in the State Machine Viewer



State Diagram View

The state diagram view is shown at the top of the State Machine Viewer window. It contains a diagram of the states and state transitions.

The nodes that represent each state are arranged horizontally in the state diagram view with the initial state, that is, the state node that receives the reset signal, in the left-most position. Nodes that connect to logic outside of the state machine instance are represented by a double circle. The state transition is represented by an arc with an arrow pointing in the direction of the transition.

When you select a node in the state diagram view, if you turn on the **Highlight Fan-in** or **Highlight Fan-out** command from the View menu or the State Machine Viewer toolbar, the respective fan-in or fan-out transitions from the node are highlighted in red.

An encrypted block with a state machine displays encoding information in the state encoding table, but does not display a state transition diagram or table.

State Transition Table

The state transition table on the **Transitions** tab at the bottom of the State Machine Viewer window displays the condition equation for each state transition. Each transition (each arc in the state diagram view) is represented by a row in the table. The table has the following three columns:

- **Source State**—the name of the source state for the transition
- **Destination State**—the name of the destination state for the transition
- **Condition**—the condition equation that causes the transition from source state to destination state

To easily see all the transitions to and from each state name, click the appropriate column heading to sort on that column.

The text in each column is left aligned by default; to change the alignment and more easily see the relevant part of the text in the table, right-click in the column, and click **Align Right**. To change back to left alignment, choose **Align Left**.

You can click in any cell in the table to select it. To select all cells, right-click in the cell and click **Select All**; or, on the Edit menu, click **Select All**. To copy selected cells to the clipboard, right-click the cells and click **Copy Table**; or, on the Edit menu, point to Copy and click **Copy Table**. You can paste the table into any text editor as tab-separated columns.

State Encoding Table

The state encoding table on the **Encoding** tab at the bottom of the State Machine Viewer window displays the encoding information for each state transition.

To view state encoding information in the State Machine Viewer, you must have synthesized your design using **Start Analysis & Synthesis**. If you have only elaborated your design using **Start Analysis & Elaboration**, the encoding information is not displayed.

Selecting an Item in the State Machine Viewer

Each state node and transition in the State Machine Viewer can be selected and highlighted. To select a state transition, click the arc that represents the transition.

When you select a state node and/or transition arc in the state diagram view, the matching state node and/or equation conditions in the state transition table are highlighted; conversely, when you select a state node and/or equation condition in the state transition table, the corresponding state node and/or transition arc is highlighted in the state diagram view.

Switching between State Machines

A design may contain multiple state machines. To choose which state machine to view, use the **State Machine selection** box located at the top of the State Machine Viewer. Click in the drop-down box and select the desired state machine.

Navigating the Schematic View

The previous sections provided an overview of the user interface for each netlist viewer, and how to select an item in each viewer. This section describes ways to navigate through the pages and hierarchy levels in the schematic view of the RTL Viewer and Technology Map Viewer.

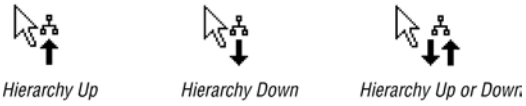
Traversing & Viewing the Design Hierarchy

You can open different hierarchy levels in the schematic view using the hierarchy list (refer to "Hierarchy List" on page 12–15), or the **Hierarchy Up** and **Hierarchy Down** commands in the schematic view.

Use the **Hierarchy Down** command to go down into, or expand an instance's hierarchy, and open a lower level schematic showing the internal logic of the instance. Use the **Hierarchy Up** command to go up in hierarchy, or collapse a lower level hierarchy, and open the parent higher level hierarchy. When the **Selection Tool** is selected, the appropriate option is available when your mouse pointer is located over an area of the schematic view that has a corresponding lower or higher level hierarchy.

The mouse pointer changes as it moves over different areas of the schematic to indicate whether you can move up, down, or both up and down in the hierarchy (Figure 12–6). To open the next hierarchy level, right-click in that area of the schematic, and click **Hierarchy Down** or **Hierarchy Up**, as appropriate, or double-click in that area of the schematic.

Figure 12–6. Mouse Pointers Indicate How to Traverse Hierarchy



Flattening the Design Hierarchy

You can flatten the design hierarchy to see the design without hierarchical boundaries. To flatten the hierarchy from the current level and all the lower level hierarchies of the current design hierarchy, right-click in the schematic, and click **Flatten Netlist**. To flatten the entire design, choose this command from the top-level schematic of the design.

Viewing the Contents of a Design Hierarchy within the Current Schematic

You can use the **Display Content** and **Hide Content** commands to show or hide a lower hierarchy level for a specific instance within the schematic for the current hierarchy level.

To display the lower hierarchy netlist of an instance on the same schematic as the remaining logic in the currently viewed netlist, right-click the selected instance, and click **Display Content**.

To hide all of the lower hierarchy logic of a hierarchy box into a closed instance, right-click the selected instance, and click **Hide Content**.

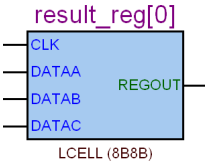
Viewing Contents of Atom Primitives in the Technology Map Viewer

In the Technology Map Viewer, you can view the contents of certain device atom primitives to see their underlying implementation details. For logic cell (`LCELL`) atoms in Stratix, Cyclone™, and MAX® II devices, you can view the look-up tables (LUT), registers, and logic gates. For I/O atoms in Stratix II, Cyclone II, Stratix, Cyclone, and HardCopy® II devices, you can view the registers and logic gates.

In addition, you can view the implementation of RAM and DSP blocks in certain devices. You can view the implementation of RAM blocks in Stratix II, Stratix II GX, Stratix, Stratix GX, Cyclone II, and Cyclone devices. You can view the implementation of DSP blocks only in Stratix and Stratix GX series of devices.

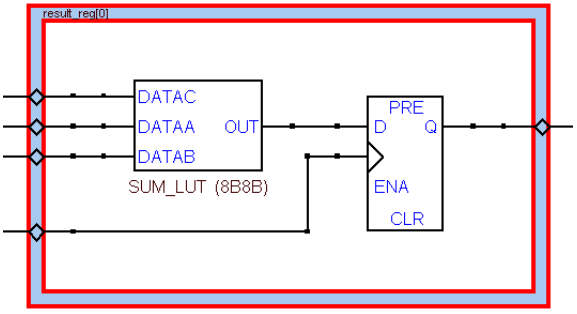
If you can view the contents of an atom instance, it is colored blue in the schematic view (Figure 12–7).

Figure 12–7. Instance that Can Be Expanded to View Internal Contents



To view the contents of one or more atom primitive instances, select the desired atom instance(s). Right-click the selected instance and click **Display Content**. Figure 12–8 shows an expanded version of the instance in Figure 12–7.

Figure 12–8. Internal Contents of the Atom Instance in Figure 12–7.



To hide the contents (and revert to the compact format), select and right-click the atom instance(s), and click **Hide Content**.

In the schematic view, the internal details within an atom instance can not be selected as individual nodes. Any mouse action on any of the internal details is treated as a mouse action on the atom instance.

Zooming & Magnification

You can control the magnification of your schematic with the View menu, the **Zoom Tool** in the toolbar, or the Ctrl key and mouse wheel button, as described in this section.

The **Fit in Window**, **Fit Selection in Window**, **Zoom In**, **Zoom Out**, and **Zoom** commands are available from the View menu, by right-clicking in the schematic view and selecting **Zoom,** or from the **Zoom** toolbar. To enable the zoom toolbar, on the Tools menu, click **Customize**. Click the **Toolbars** tab and click **Zoom** to enable the toolbar.

By default, the viewer displays most pages sized to fit in the window. If the schematic page is very large, the schematic is displayed at the minimum zoom level, and the view is centered on the first node. Select **Zoom In** to see the image at a larger size, and select **Zoom Out** to see the image (when the entire image is not displayed) at a smaller size. The **Zoom** command allows you to specify a magnification percentage (where 100% is considered the normal size for the schematic symbols). The **Fit Selection in Window** command zooms in on the selected nodes in a schematic to fit within the window. Use the **Selection Tool** to select one or more nodes (instances, primitives, pins, and nets), then select **Fit Selection in Window** to enlarge the area covered by the selection. This feature is helpful when you want to see a particular element in a large schematic. After you select a node, you can easily zoom in to view the particular node.

You also can use the **Zoom Tool** on the viewer toolbar to control magnification in the schematic view. When you select the **Zoom Tool** in the toolbar, clicking on the schematic zooms in and centers the view on the location you clicked. Right-click on the schematic (or press the Shift key or the Ctrl key and click) to zoom out and center the view on the location you clicked. When you select the **Zoom Tool**, you also can zoom in to a certain portion of the schematic by selecting a rectangular box area with your mouse cursor. The schematic is enlarged to show the selected area. To change the minimum and the maximum zoom level, on the Tools menu, click **Options**. In the **Options** dialog box, in the **Category** list, select **RTL/Technology Map Viewer**, and set the desired minimum and maximum zoom level.

By default, the viewers maintain the zoom level when filtering on the schematic (refer to "Filtering in the Schematic View" on page 12–27). To change the behavior so that the zoom level is always reset to "Fit in Window," on the Tools menu, click **Options**. In the **Category** list, select **RTL/Technology Map Viewer**, and turn off **Maintain zoom level**.

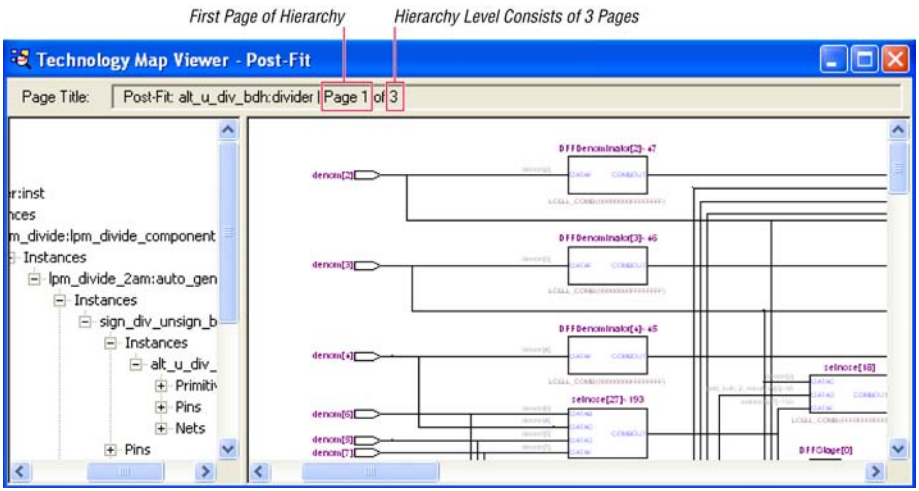
Partitioning the Schematic into Pages

For large design hierarchies, the RTL Viewer and Technology Map Viewer partition your netlist into multiple pages in the schematic view. To control how much of the design can be seen on each page, on the Tools menu, click **Options**. In the **Category** list, select **RTL/Technology Map Viewer**, and set the desired options under **Display Settings**.

The **Nodes per page** option specifies the number of nodes per partitioned page. The default value is 50 nodes; the range is 1 to 1,000 nodes. The **Ports per page** option specifies the number of ports (or pins) per partitioned page. The default value is 1,000 ports/pins; the range is 1 to 2,000 ports/pins. The viewers partition your design into a new page if either the node number or the port number exceeds the limit you have specified. You may occasionally see the number of ports exceed the limit, depending on the configuration of nodes on the page.

When a hierarchy level is partitioned into multiple pages, the title bar for the schematic window indicates which page is displayed and how many total pages exist for this level of hierarchy (shown in the format: Page <*current page number*> of <*total number of pages*>) as shown in Figure 12–9.

Figure 12–9. RTL Viewer Title Bars Indicating Page Number Information



When you change the number of nodes or ports per page, the change applies only to new pages that are shown or opened in the viewer. To refresh the current page so that it displays the changed number of nodes or ports, click the **Refresh** button in the toolbar.

Moving between Schematic Pages

To move to another schematic page, on the View menu, click **Previous Page** or **Next Page**, or click the **Previous Page** icon or the **Next Page** icon in the viewer toolbar.

To go to a particular page of the schematic, on the Edit menu, click **Go To**, or right-click in the schematic view, and click **Go To**. In the **Page** list, select the desired page number.

Moving Back & Forward through Schematic Pages

To return to the previous view after changing the page view, click **Back** on the View menu, or click the **Back** icon on the viewer toolbar. To go to the next view, click **Forward** on the View menu, or click the **Forward** icon on the viewer toolbar.

You can go **Forward** only if you have not made any changes to the view since going **Back**. Use **Back** and **Forward** to switch between page views. These commands do not undo an action such as selecting a node.

Following Nets across Schematic Pages

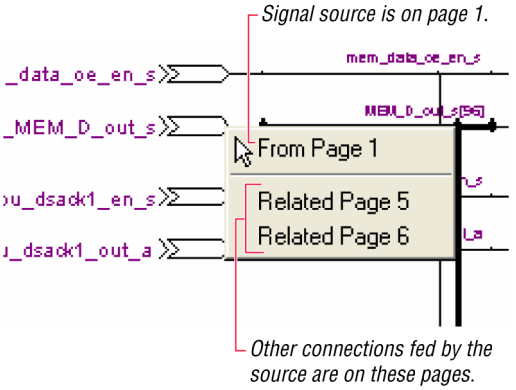
Input and output connectors indicate nodes that connect across pages of the same hierarchy. Right-click on a connector to display a menu of commands that trace the net through the pages of the hierarchy.

After you right-click to follow a connector port, the viewer opens a new page, which centers the view on the particular source or destination net using the same zoom factor used by the previous page. To trace a specific net to the new page of the hierarchy, Altera recommends that you first select the desired net, which highlights it in red, before you right-click to traverse pages.

Input Connectors

Figure 12–10 shows an example of the menu that appears when you right-click an input connector. The **From** command opens the page containing the source of the signal. The **Related** commands, if applicable, open the specified page containing another connection fed by the same source.

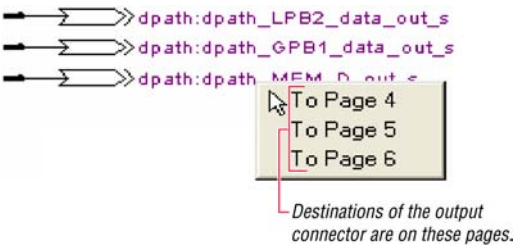
Figure 12–10. Input Connector Right Button Pop-Up Menu



Output Connectors

Figure 12–11 shows an example of the menu that appears when you right-click an output connector. The **To** command opens the specified page that contains a destination of the signal.

Figure 12–11. Output Connector Right Button Pop-Up Menu



Go to Net Driver

To locate the source of a particular net in the schematic view, select the net to highlight it, right-click the selected net, point to Go to Net Driver, and click **Current page**, **Current hierarchy**, or **Across hierarchies**. Refer to Table 12–5.

Table 12–5. Go to Net Driver Commands

Command	Action
Current page	Locates the source or driver on the current page of the schematic only.
Current hierarchy	Locates the source within the current level of hierarchy, even if the source is located on another page of the netlist schematic.
Across hierarchies	Locates the source across hierarchies until the software reaches the source at the top hierarchy level.

The schematic view opens the correct page of the schematic if needed, and adjusts the centering of the page so that you can see the net source. The schematic shows the default page for the net driver. The view is an unfiltered view, so no filtering results are kept.

Filtering in the Schematic View

Filtering allows you to filter out nodes and nets in your netlist to view only a logic path that interests you.

Filter your netlist by selecting hierarchy boxes, nodes, ports of a node, net, or states in a state machine that are part of the path you want to see. The following filter commands are available:

- **Sources**—Displays the sources of the selection
- **Destinations**—Displays the destinations of the selection
- **Sources & Destinations**—Displays both the sources and destinations of the selection
- **Selected Nodes and Nets**—Displays only the selected nodes and nets with the connections between them
- **Between Selected Nodes**—Displays nodes and connections in the path between the selected nodes
- **Bus Index**—Displays the sources or destinations for one or more indices of an output or input bus port

Select a hierarchy box, node, port, net, or state node, right-click in the window, point to Filter and click the appropriate filter command. The viewer generates a new page showing the netlist that remains after filtering.

When filtering in a state diagram in the State Machine Viewer, sources and destinations refer to the previous and next transition states or paths between transition states in the state diagram. The transition table and encoding table also reflect the filtering.

You can go back to the netlist page before it was filtered using the **Back** command, described in "Moving Back & Forward through Schematic Pages" on page 12–25.

When viewing a filtered netlist, clicking an item in the hierarchy list causes the schematic view to display an unfiltered view of the appropriate hierarchy level. You cannot use the hierarchy list to select items or navigate in a filtered netlist.

Filter Sources Command

To filter out all but the source of the selected item, right click the item, point to Filter and click **Sources**. The selected object type determines what is displayed, as outlined in Table 12–6 below, and shown in Figure 12–12 on page 12–29.

Table 12–6. Selected Objects Determine Filter Sources Display

Selected Object	Result Shown in Filtered Page
Node or hierarchy box	Shows all the sources of the node's input ports. For an example, refer to Figure 12–12 on page 12–29.
Net	Shows the sources that feed the net.
Input port of a node	Shows only the input source nodes that feed this port.
Output port of a node	Shows only the selected node.
State node in a state machine	Shows the states that feed the selected state (previous transition states).

Filter Destinations Command

To filter out all but the destinations of the selected node or port displayed as outlined in Table 12–7 below, and shown in Figure 12–12 on page 12–29, right-click the node or port, point to Filter, and click **Destinations**.

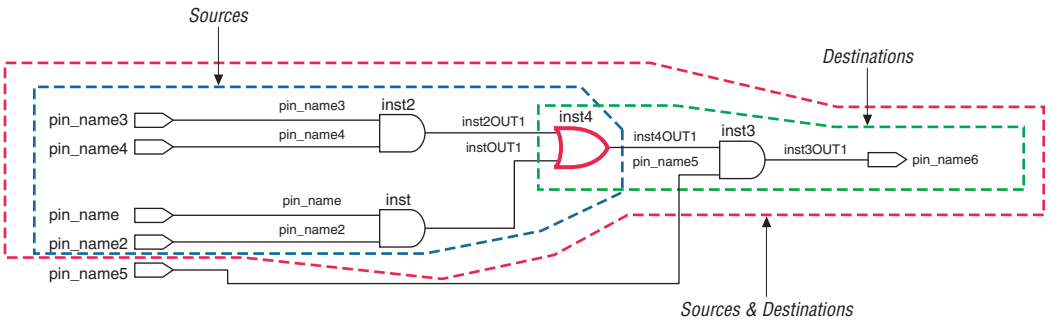
Table 12–7. Selected Objects Determine Filter Destinations Display

Selected Object	Result Shown in Filtered Page
Node or hierarchy box	Shows all the destinations of the node's output ports. For an example, refer to Figure 12–12 on page 12–29.
Net	Shows the destinations fed by the net.
Input port of a node	Shows only the selected node.
Output port of a node	Shows only the fan-out destination nodes fed by this port.
State node in a state machine	Shows the states that are fed by the selected states (next transition states).

Filter Sources & Destinations Command

The **Sources & Destinations** command is a combination of the **Sources** and **Destinations** filtering commands, in which the filtered page shows both the sources and the destinations of the selected item. To select this option, right-click on the desired object, point to Filter, and click **Sources & Destinations**. For an example, refer to Figure 12–12.

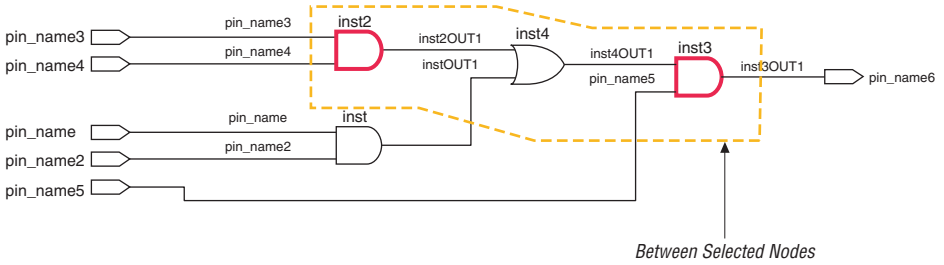
Figure 12–12. Sources, Destinations & Sources & Destinations Filtering for inst4



Filter between Selected Nodes Command

To show the nodes in the path between two or more selected nodes or hierarchy boxes, right-click, point to Filter, and click **Between Selected Nodes**. For this option, selecting a port of a node is the same as selecting the node. For an example, refer to Figure 12–13.

Figure 12–13. Between Selected Nodes Filtering Between inst2 & inst3



Filter Selected Nodes & Nets Command

To create a filtered page that shows only the selected nodes and/or nets and, if applicable, the connections between the selected nodes and/or nets, right-click, point to Filter, and click **Selected Nodes & Nets**. Figure 12–14 shows a schematic with some nodes selected.

Figure 12–14. Using Selected Nodes & Nets to Select Nodes

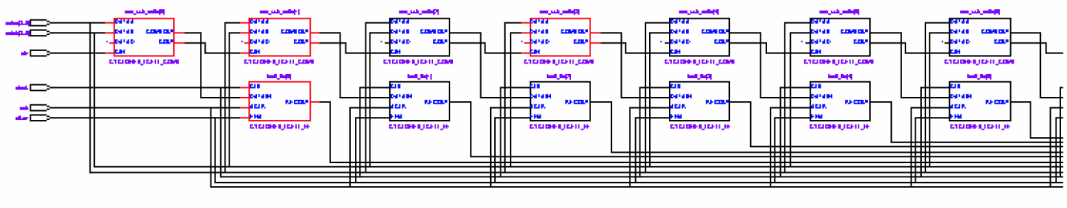
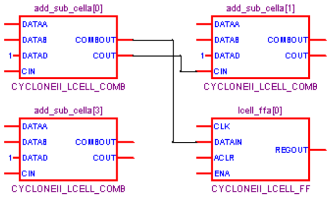


Figure 12–15 shows the schematic after filtering has been performed. If you select a net, the filtered page shows the immediate sources and destinations of the selected net.

Figure 12–15. Selected Nodes & Nets Filtering on Figure 12–14 Schematic



Filter Bus Index Command

To show the path related to a specific index of a bus input or output port in the RTL Viewer, right-click the port, point to Filter, and click **Bus Index**. The **Select Bus Index** dialog box allows you to select the indices of interest.

Filter Command Processing

The options to control filtering are available in the **Filtering** section of the **RTL/Technology Map Viewer Options** dialog box. Right-click in the schematic, and click **Viewer Options** to open the dialog box.

For all the filtering commands, the viewer stops tracing through the netlist to obtain the filtered netlist when it reaches one of the following objects:

- A pin
- A specified number of filtering levels, counting from the selected node or port; the default value is 3

  Specify the **Number of filtering** levels in the **Filtering** section of the **RTL/Technology Map Viewer Options** dialog box. The default value is 3 to ensure optimal processing time when performing filtering, but you can specify a value from 1 to 100.

- A register (optional; turned on by default)

  Turn the **Stop filtering at register** option on or off in the **Filtering** section of the **RTL/Technology Map Viewer Options** dialog box. Right-click in the schematic and click **Viewer Options** to open the dialog box.

By default, the filtered schematic shows all possible connection between the nodes shown in the schematic. To remove the nodes and connections that are not directly part of the path that was traced to generate a filtered netlist, turn off the **Shows all connections between nodes** option in the **Filtering** section of the **RTL/Technology Map Viewer Option**s dialog box.

Filtering Across Hierarchies

The filtering commands display nodes in all hierarchies by default. When the filtered path passes through levels of hierarchy on the same schematic page, green hierarchy boxes group the logic and show the hierarchy boundaries. A diamond symbol appears on the border that represents the port relationship between two different hierarchies (Figure 12–16 on page 12–33 and Figure 12–17 on page 12–33).

The **RTL/Technology Map Viewer Options** dialog box provides an option to control filtering if you prefer to filter only within the current hierarchy. Right-click in the schematic, and click **Viewer Options**. In the **Filtering** section, turn off the **Filter across hierarchy** option.

To disable the box hierarchy display, on the Tools menu, click **Options**. In the Category list, select **RTL/Technology Map Viewer**, and turn off **Show box hierarchy**.

Netlists of the same hierarchy that are displayed over more than one page are not grouped with a box. Filtering and expanding on a blue atom primitive does not trace the underlying netlist even when **Filter across hierarchy** is enabled.

Figures 12–16 and 12–17 show examples of filtering across hierarchical boundaries. Figure 12–17 shows an example after the **Sources** filter has been applied to an input port of the `taps` instance, where the input port of the lower level hierarchical block connects directly to an input pin of the design. The name of the instance is indicated within the green border and appears as a tooltip when you move your mouse pointer over the instance.

Figure 12–16. Filtering Across Hierarchical Boundaries, Small Example

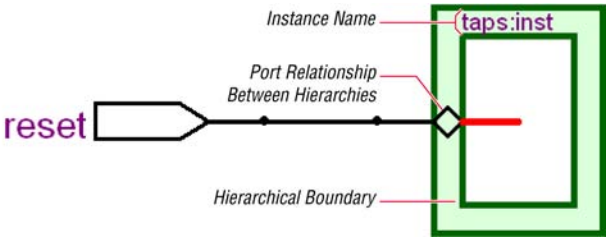
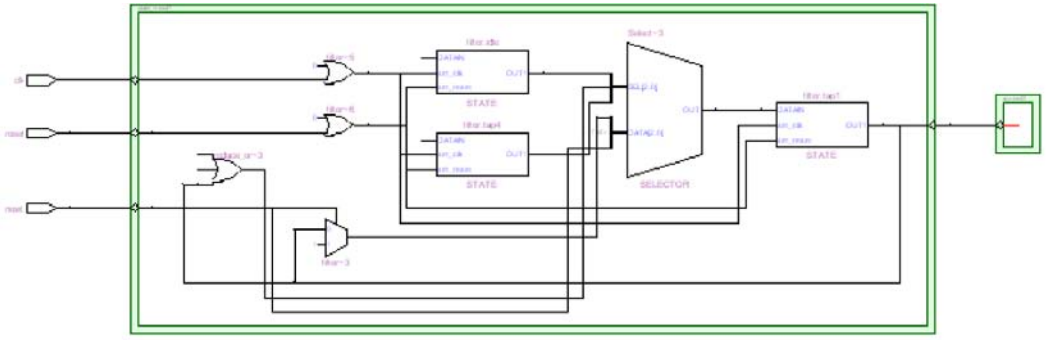


Figure 12–17 shows a larger example after the **Sources** filter that has been applied to an input port of an instance, in which the source comes from input pins that are fed through another level of hierarchy.

Figure 12–17. Filtering Across Hierarchical Boundaries, Large Example



Sources command applied to an input port of an instance in which the source comes from input pins that are fed through another level of hierarchy.

Expanding a Filtered Netlist

After a netlist is filtered, there may be ports whose connections are not displayed because they are not part of the main path through the netlist. Two expansion features, immediate expansion and the **Expand** command, allow you to add the fan-out or fan-in signals of these ports to the schematic display of a filtered netlist.

You can immediately expand any port whose connections are not displayed by double-clicking that port in the filtered schematic. When you do so, one level of logic is expanded.

To expand more than one level of logic, right-click the port and click the **Expand** command. This command expands logic from the selected port by the amount specified in the **Viewer Options**. To set these options, right-click in the schematic view, and click **Viewer Options**. In the Expansion section, set the **Number of expansion levels** option to specify the number of levels to expand (the default value is 3 and the range is 1 to 100 levels). You also can set the **Stop expanding at register** option (which is turned on by default) to specify whether to stop netlist expansion when a register is reached.

You can select multiple nodes to expand when using the **Expand** command. If you select ports that are located on multiple schematic pages, only the ports on the currently viewed page are shown in the expanded schematic.

In the State Machine Viewer, the **Expand** command has the following three options:

- **Sources**—Displays the states that feed the selected states (previous transition states).
- **Destinations**—Displays the states that are fed by the selected states (next transition states).
- **Sources & Destinations**—Displays both the previous and next transition states.

The state transition table and state encoding table also reflect the changes to the filtering.

The expansion feature works across hierarchical boundaries if the filtered page containing the port to be expanded was generated with the **Filter across hierarchy** option turned on (refer to "Filtering in the Schematic View" on page 12–27 for details on this option). When viewing timing paths in the Technology Map Viewer, the **Expand** command always works across hierarchical boundaries because filtering across hierarchy is always turned on for these schematics (Refer to "Viewing a Timing Path" on page 12–37 for details on these schematics).

Reducing a Filtered Netlist

In some cases, removing logic from a filtered schematic or state diagram makes the schematic view easier to read or minimizes distracting logic that you do not need to see on the schematic.

To reduce elements in the filtered schematic or state diagram view, right-click the node or nodes you want to remove and click **Reduce**.

Probing to Source Design File & Other Quartus II Windows

The RTL, Technology Map, and State Machine Viewers let you cross-probe from the viewer to the source design file and to various other windows within the Quartus II software. You can select one or more hierarchy boxes, nodes, nets, state nodes, or state transition arcs that interest you in the viewer and locate the corresponding items in another applicable Quartus II software window. You then can view and make changes or assignments in the appropriate editor or floorplan.

To locate an item from the viewer in another window, right-click the items of interest in the schematic or state diagram view, point to Locate, and click the appropriate command. The following commands are available:

- **Locate in Assignment Editor**
- **Locate in Pin Planner**
- **Locate in Timing Closure Floorplan**
- **Locate in Chip Editor**
- **Locate in Resource Property Editor**
- **Locate in RTL Viewer**
- **Locate in Technology Map Viewer**
- **Locate in Design File**

The options available for locating depend on the type of node and whether it exists after placement and routing. If a command is enabled in the menu, then it is available for the selected node. You can use the **Locate in Assignment Editor** command for all nodes, but assignments may be ignored during placement and routing if they are applied to nodes that do not exist after synthesis.

The viewer automatically opens another window for the appropriate editor or floorplan, and highlights the selected node or net in the newly opened window. You can switch back to the viewer by selecting it in the Window menu or by closing, minimizing, or moving the new window.

Probing to the Viewers from Other Quartus II Windows

You can cross-probe to the RTL Viewer and Technology Map Viewer from other windows within the Quartus II software. You can select one or more nodes or nets in another window and locate them in one of the viewers.

You can locate nodes between the RTL, State Machine, and Technology Map Viewers, and you can locate nodes in the RTL Viewer or Technology Map Viewer from the following Quartus II software windows:

- Project Navigator
- Timing Closure Floorplan
- Chip Editor
- Resource Property Editor
- Node Finder
- Assignment Editor
- Messages Window
- Compilation Report

To locate elements in the viewer from another Quartus II window, select the node or nodes in the appropriate window; for example, select an entity in the **Entity** list on the **Hierarchy** tab in the Project Navigator, or select nodes in the **Timing Closure Floorplan**, or select node names in the **From** or **To** column in the Assignment Editor. Then, right-click the selected object, point to Locate, and click **Locate in RTL Viewer** or **Locate in Technology Map Viewer**. After you choose this command, the viewer window opens, or is brought to the foreground if the viewer window is already open.

The first time the window opens after a compilation, the preprocessor stage runs before the viewer window opens.

The viewer shows the selected nodes and, if applicable, the connections between the nodes. The display is similar to what you see if you right-click the object, point to Filter, and click **Selected Nodes & Nets** using **Filter Across Hierarchy**. If the nodes cannot be found in the viewer, a message box displays the message: “Can’t find message location.”

Viewing a Timing Path

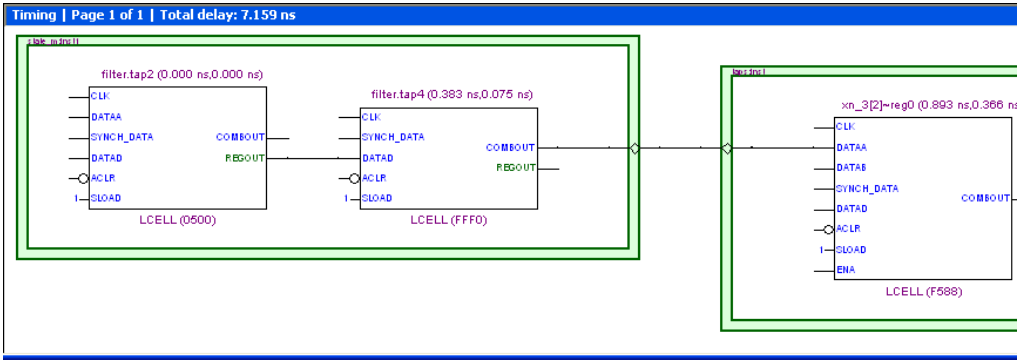
You can cross-probe from the Timing Analysis section of the Compilation Report to see a visual representation of a timing path listed by the Timing Analyzer.

To take advantage of this feature, you must first successfully complete a full compilation of your design, including the Timing Analyzer stage. To access the **Timing Analyzer** report which contains the timing results for your design, on the Processing menu, click **Compilation Report**. To view a path listed in any of the detailed reports for **Clock Setup:** <*clock name*>, **tsu**, **tco**, **tpd**, or other timing parameters. When you select a detailed report, the timing information is listed in a table format on the right side of the Compilation Report; each row of the table represents a timing path in the design. To view a particular timing path in the Technology Map Viewer, right-click the appropriate row in the table, point to Locate, and click **Locate in Technology Map Viewer** or **Locate in RTL Viewer**.

In the Technology Map Viewer, the schematic page displays the nodes along the timing path with a summary of the total delay, as well as timing data representing the interconnect (IC) and cell delays associated with each node. The delay for each node is shown in the following format: <*post-synthesis node name*> (<*IC delay*> ns, <*cell delay*> ns).

Figure 12–18 shows a portion of a timing path represented in the Technology Map Viewer. The total delay for the entire path going through a number of levels of logic (only three are shown in Figure 12–18) is 7.159 ns. The delays are indicated for each level of logic, for example, the interconnect or IC delay to the first `LCELL` primitive is 0.383 ns, and the cell delay through the `LCELL` is 0.075 ns. When the timing path passes through a level of hierarchy, green hierarchy boxes group the logic and show the hierarchical boundaries. A diamond symbol on the border indicates the path passes between two different hierarchies.

Figure 12–18. Timing Path Schematic in the Technology Map Viewer



In the RTL Viewer, the schematic page displays the nodes in the path(s) between the source and destination registers with a summary of the total delay.

The RTL Viewer netlist is based on an initial stage of synthesis, so the post-fitting nodes may not exist in the RTL Viewer netlist. Therefore, the internal delay numbers are not displayed in the RTL Viewer as they are in the Technology Map Viewer, and the timing path may not be displayed exactly as it appears in the timing analysis report. If there are multiple paths between the source and destination registers, the RTL Viewer might display more than just the timing path. There are also some cases when the path cannot be displayed, such as paths through state machines, encrypted intellectual property (IP), or registers that are created during the fitter process. In cases where the timing path displayed in the RTL Viewer might not be the correct path, the compiler issues messages.

Other Features in the Schematic Viewer

This section describes other features in the schematic view that enhance usability and help you analyze your design.

Tooltips

A tooltip is displayed whenever the mouse pointer is held over an element in the schematic. The tooltip contains useful information about a node, net, input port, and output port. Table 12–8 lists the information contained in the tooltip for each type of node.

The tooltip information for an instance (the first row in Table 12–8) includes a list of the primitives found within that level of hierarchy, and the number of each primitive contained in the current instance. The number includes all hierarchical blocks below the current instance in the hierarchy. This information lets you estimate the size and complexity of a hierarchical block without navigating into the block.

The tooltip information for atom primitives in the Technology Map Viewer (the second row of Table 12–8) shows the equation for the design atom. The equations are an expanded version of the equations you can view in the Equations window in the Timing Closure Floorplan. Advanced users can use these equations to analyze the design implementation in detail.

For details on understanding equations, refer to the Quartus II Help.

To copy tooltips into the clipboard for use in other applications, right-click the desired node or netlist, and click **Copy Tooltip**.

To turn off tooltips or change the duration of time that a tooltip is displayed in the view, on the Tools menu, click **Options**. In the Category list, select **RTL/Technology Map Viewer** and set the desired options under **Tooltip settings**.

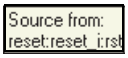
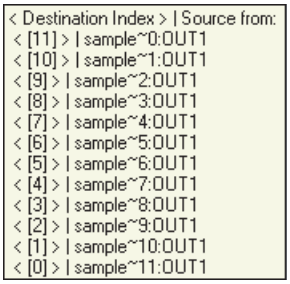
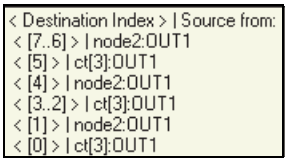
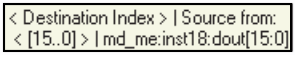
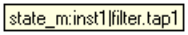
The **Show names in tooltip for** option specifies the number of seconds to display the names of assigned nodes and pins in a tooltip when the pointer is over the assigned nodes and pins. Selecting **Unlimited** displays the tooltip as long as the pointer remains over the node or pin. Selecting **0** turns off tooltips. The default value is 5 seconds.

The **Delay showing tooltip for** option specifies the number of seconds you must hold the mouse pointer over assigned nodes and pins before the tooltip displays the names of the assigned nodes and pins. Selecting **0** displays the tooltip immediately when the pointer is over an assigned node or pin. Selecting **Unlimited** prevents tooltips from being displayed. The default value is 1 second.

Table 12–8. Tooltip Information (Part 1 of 2)

Description & Tooltip Format	Example Tooltips
Instance Format: <*instance name*>, <*instance type*> <*primitive type*>, <*number of primitives*>... <*primitive type*>, <*number of primitives*>	taps:inst, INST DFF 32 OPERATOR(SELECTOR) 8 OPERATOR(DECODER) 1
Atom Primitive Format: <*instance name*>, <*primitive name*> (<*LUT Mask Value*>) {(`r` | `c` <*Register or Combinational equation*>)} ... An `r` (as in the first example) represents the equation for a register, and a `c` (as in the second example) represents the equation for combinational logic.	inst5[3], LCELL (0000) <r> inst5[3] = DFFEAS((GND), GLOBAL(CLK), VCC, , ENA, SYNCH_DATA, , , VCC) CLK = clkx2 ENA = inst4 SYNCH_DATA = result[7] acc:inst3|ynm[2]~133, LCELL (00F0) <c> ynm[2]~133 = DATAC & !DATAD DATAC = result[2] DATAD = filter.tap1
Primitive Format:<*primitive name*>, <*primitive type*>	clocks:inst7|Mux~1, OPER (MUX) md_me:inst18|data[3..3], DFFE
Pin Format: <*pin name*>, <*pin type*>	pc_clock, INPUT Test_probe, OUTPUT
Connector Format: <*connector name*>	inst4_CLK
Net Format: <*net name*>, `fan-out` = <*number of fan-out signals*>	state_m:inst1:decoder_node[2][0], fan-out = 1

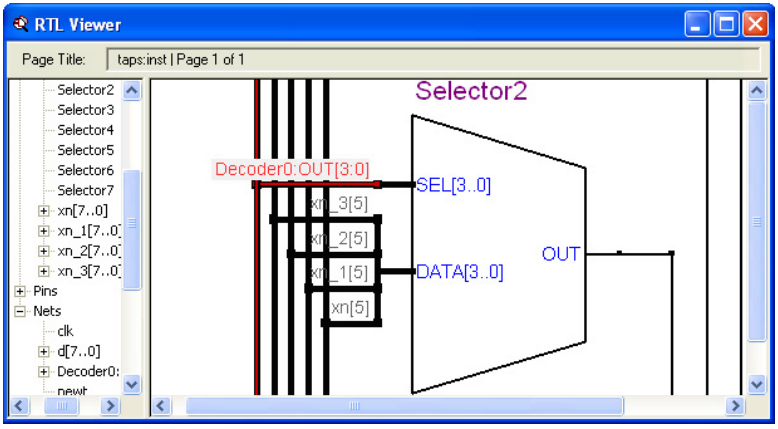
Table 12–8. Tooltip Information (Part 2 of 2)

Description & Tooltip Format	Example Tooltips
Output port Format: `fan-out` = <*number of fan-out signals*>	
Input Port The information displayed depends on the type of the source net. The examples of the tooltips shown represent the following type of source net: *(1)* Single net *(2)* Individual nets, part of the same bus net *(3)* Combination of different bus nets *(4)* Constant inputs *(5)* Combination of single net and constant input *(6)* Bus net Source from refers to the source net name that connects to the input port. Destination Index refers to the bit(s) at the destination input port to which the source net is connected (not applicable for single nets).	 *(1)*  *(2)*  *(3)*  *(4)*  *(5)*  *(6)*
State Machine Node Format: <*node name*>	
State Machine Transition Arc This information is displayed when you hold your mouse over the arc representing the transition between two states. Format: (<*equation for transition between states*>)	

Rollover

You can highlight an element and view its name in your schematic using the rollover feature. When you place your mouse pointer over an object, the object is highlighted and the name is displayed, helping you to analyze your schematic diagram. This feature is enabled by default in the netlist viewers. To turn off the Rollover feature, on the Tools menu, click **Options**. In the **Options** dialog box, in the **Category** list, select **RTL/Technology Map Viewer** and turn off **Enable Rollover**.

Figure 12–19. Rollover in the RTL Viewer & Technology Map Viewer



The Properties Dialog Box

You can view the properties of an instance or a primitive using the Properties Dialog box. To view the properties of an instance or a primitive in the RTL Viewer or the Technology Map Viewer, right-click the node and click **Properties**.

The Properties dialog box contains the following information about the selected node:

- The parameter values of an instance.
- The active level of the port (for example, active high or active low). An active low port is denoted with an exclamation mark "!".
- The port's constant value (for example, VCC or GND). Table 12–9 describes the possible value of a port.

Table 12–9. Possible Port Values

Value	Description
VCC	The port is not connected and has VCC value (tied to VCC)
GND	The port is not connected and has GND value (tied to GND)
--	The port is connected and has value (other than VCC or GND)
Unconnected	The port is not connected and has no value (hanging)

Displaying Net Names

To see names of all the nets displayed in your schematic, on the Assignments menu, click **Options**. In the Category list, select **RTL/Technology Map Viewer** and turn on **Show Net Name** under **Display Settings**. This option is disabled by default. If you turn on this option, the schematic view refreshes automatically to display the net names.

Displaying Node Names

Nodes in some designs have long names that overlap the ports of other symbols in the schematic. To remove the node names from the schematic, on the Tools menu, click **Options**. In the **Category** list, select **RTL/Technology Map Viewer** and turn off **Show node name** under **Display Settings**. This option is turned on by default.

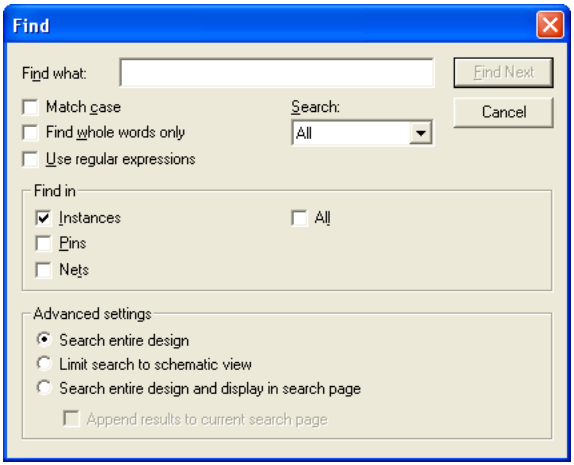
Full Screen View

To set the viewer window to fill the whole screen, on the View menu, click **Full Screen**, or click the **Full Screen** icon in the viewer toolbar, or press Ctrl+Alt+Space. The keyboard shortcut toggles the full screen. To return to the standard screen view after viewing the full screen, press Ctrl+Alt+Space again.

Find Command

To open the **Find** dialog box shown in Figure 12–20, on the Edit menu, click **Find**, or click the **Find** icon in the viewer toolbar, or right-click in the schematic view, and click **Find**.

Figure 12–20. Find Dialog Box



Select **Up** in the Search list to search from the current hierarchy to upper (parent) hierarchies. Select **Down** to search from the current hierarchy to lower (child) hierarchies. You can choose to search only instances (nodes) in the design, or to also search pins and nets. By default, only instances are searched.

When you click **Find**, the viewer selects and highlights the first item found, opens the appropriate page of the schematic, if necessary, and centers the page so that the node is seen in the viewable area (but does not zoom in to the node). To find the next matching node, click **Find Next**.

You can use the options in the **Advanced settings** section to control the scope of the results found during a search and how they are displayed in the viewer. The default selection, **Search entire design**, searches for the item in all design elements across the entire design. To search only in the pages of the currently displayed netlist, such as a schematic showing filtering results, choose **Limit search to schematic view**.

To display the results in a new page, select **Search entire design and display in search page**. This command searches all design elements across the entire design, and displays the results on a separate page dedicated to search results. You can also append new search results to an

existing search page with the **Append results to current search page** command. The appended items appear in the same relative position as they do in the full schematic. You can use this to find and select two objects that are not on the same page and display them on the same page after performing the **Find** command.

Refer to "Finding Nodes in the RTL Viewer & Technology Map Viewer" in the Quartus II Help for more details on using the **Find** dialog box.

Exporting & Copying a Schematic Image

You can export the RTL Viewer or Technology Map Viewer schematic view in JPEG File Interchange Format (**.jpg**) or Windows Bitmap (**.bmp**) file format, which allows you to include the schematic in project documentation or share it with other project members. To export the schematic view, on the File menu, click **Export**. In the **Export** dialog box, type a file name and location, and select the desired file type. The default file name is based on the current instance name and the default file type is JPEG Interchange Format (**.jpg**). However, for pages that use filtering, expanding, or reducing operations, the default name is **Filter**<*number of export operation*>.<*file extension*>.

You can choose to copy the whole image or copy only a portion of the image. To copy the full image, on the Edit menu, point to Copy and click **Full Image**. To copy a portion of the image when using a Windows-based platform, on the Edit menu, point to Copy and click **Partial Image**. The cursor changes to indicate that you can draw a box shape. Drag the cursor around the portion of the schematic you want to copy. When you release the mouse button, the partial image is copied to the clipboard.

Occasionally, due to the design size and objects selected, an image is too large to copy to the clipboard. In this case, the Quartus II software displays an error message.

To export or copy a schematic that is too large to copy in one piece, first split the design into multiple pages to export or to copy smaller portions of the design. For information about how to control how much of your design is shown on each schematic page, refer to "Partitioning the Schematic into Pages" on page 12–24. As an alterative, use the Partial Image feature to copy a portion of the image.

The **Copy** feature is not available on UNIX platforms.

Printing

To print your schematic page, on the File menu, click **Print**. You can print each schematic page onto one full page, or you can print the highlighted parts of your schematic onto one page with the **Selection** option. Refer to "Partitioning the Schematic into Pages" on page 12–24 to control how much of your design is shown on each schematic page.

Before printing, you can modify the page orientation. On the File menu, click **Page Setup**. Change the page orientation from **Portrait** to **Landscape**, or to the setting that best fits your design. You also can adjust the page margins in the **Page Setup** dialog box.

The hierarchy list in the viewers and the table view of the State Machine Viewer cannot be printed. You can use the State Machine Viewer **Copy** command to copy the table to a text editor and print from the text editor.

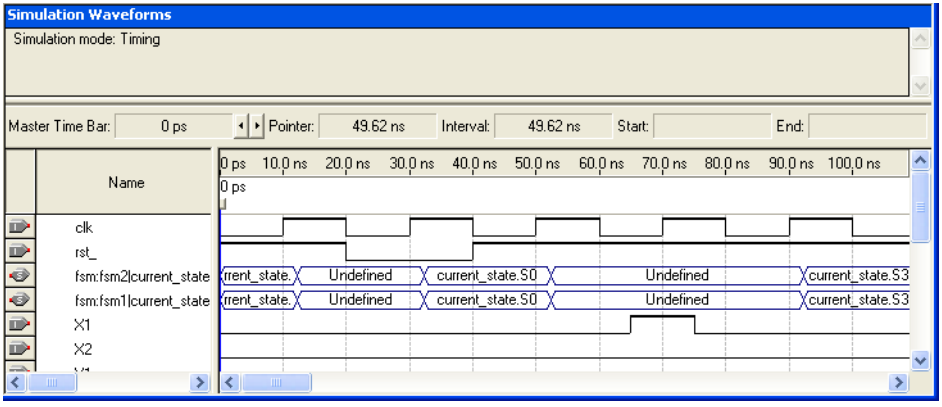
Debugging HDL Code with the State Machine Viewer

This section provides an example of using the State Machine Viewer to help debug HDL code. This example shows you how you can use the various features in the netlist viewers to help solve design problems.

Simulation of State Machine Gives Unexpected Results

The section presents a design scenario in which you compiled your design and performed a simulation in the Quartus II Simulator. The simulation result is shown in Figure 12–21 and has unexpected undefined states.

Figure 12–21. Simulation Result Showing Undefined States



To analyze the state machine design in the State Machine Viewer, follow these steps:

1. Open the State Machine Viewer for the state machine of interest. You can do this in one of the following ways:

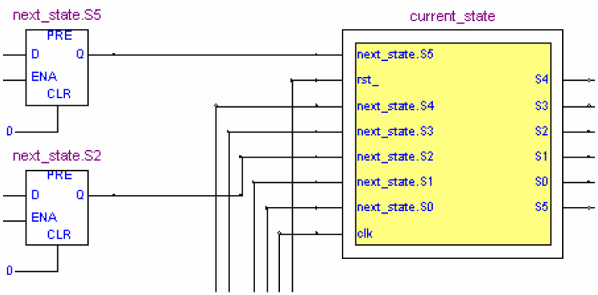
2. On the Tools menu, point to Netlist Viewers, and click **State Machine Viewer**. In the State Machine selection box, choose the state machine that you want to view.

   or

   On the Tools menu, point to Netlist Viewers, and click **RTL Viewer**. Browse to the hierarchy block that contains the state machine definition and double-click the yellow state machine instance to open the State Machine Viewer (Figure 12–24).You can open the State Machine Viewer using either of two methods:

   - In the schematic view, double-click an instance in the hierarchy to open the lower level hierarchy. You can traverse through the schematic hierarchy in this way to open the schematic page that contains the state machine (Figure 12–22).

Figure 12–22. State Machine Instance in RTL Viewer Schematic View



   or

   - In the hierarchy list, click the **+** symbol next to **Instances** to open a list of the instances in that hierarchy level of the design. You can traverse down the hierarchy tree in this way to find the instance that contains the state machine. Click on the name of the state machine in the **State Machines** folder (Figure 12–23) to open the appropriate schematic in the schematic view (Figure 12–22).

Figure 12–23. State Machine Instance in RTL Viewer Hierarchy List

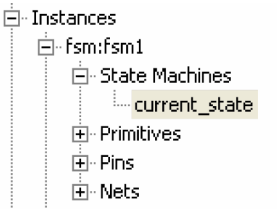
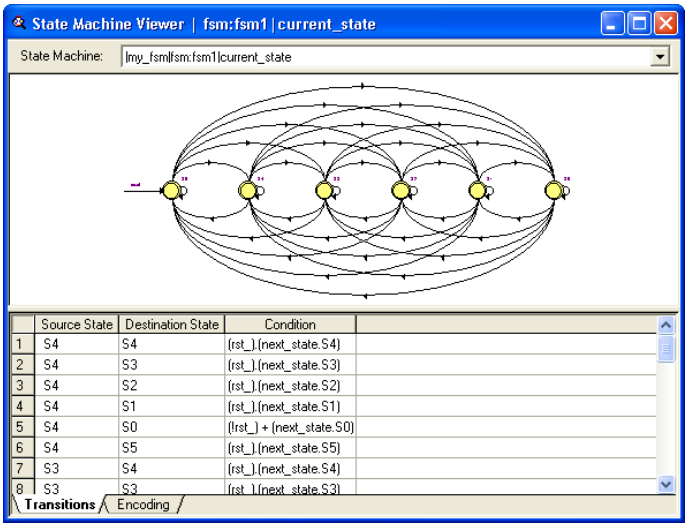


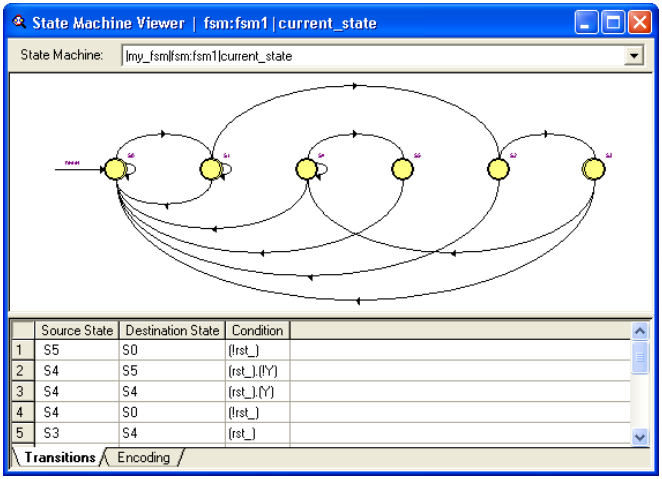
Figure 12–24. State Machine Viewer Showing Incorrect Transitions



3. You can now analyze this state machine instance using the state machine diagram, transition table, and encoding table. You can clearly see something is wrong with the state machine because there are transitions between every state. Upon inspecting the state machine behavior, you can determine that in this scenario, the designer forgot to create default assignments for the next state (that is, `next_state = current_state` if the conditions are not met).

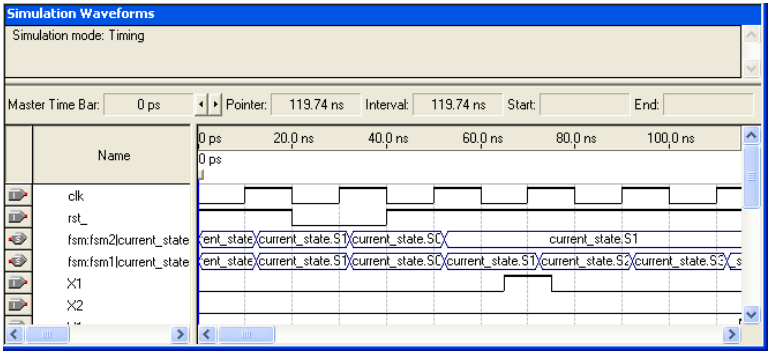
4. After fixing the error in the HDL code, recompile the design and repeat steps 1-3 to view the new state machine diagram and transition table shown in Figure 12–25 to check that the state transitions are now occurring correctly.

Figure 12–25. State Machine Viewer Showing Correct Transitions



5. Perform a new simulation, as shown in Figure 12–26, and ensure that the state machine now performs as expected.

Figure 12–26. Simulation Result Showing Correct States



Conclusion

The Quartus II RTL Viewer, State Machine Viewer, and Technology Map Viewer allow you to explore and analyze your initial synthesis netlist, post-synthesis netlist, or post-fitting and physical synthesis netlist. The viewers provide a number of features in the hierarchy list and schematic view to help you trace through your netlist and find specific hierarchies or nodes of interest. These capabilities can help you debug, optimize, or constrain your design to increase your productivity.

Quartus II Version 6.0 Handbook

Volume 2: Design Implementation & Optimization

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QII5V2-6.0

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Chapter Revision Dates

The chapters in this book, *Quartus II Handbook, Volume 2*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Assignment Editor
Revised: *May 2006*
Part number: *QII52001-6.0.0*

Chapter 2. Command-Line Scripting
Revised: *May 2006*
Part number: *QII52002-6.0.0*

Chapter 3. Tcl Scripting
Revised: *May 2006*
Part number: *QII52003-6.0.0*

Chapter 4. Quartus II Project Management
Revised: *May 2006*
Part number: *QII52012-6.0.0*

Chapter 5. I/O Management
Revised: *May 2006*
Part number: *QII52013-6.0.0*

Chapter 6. Mentor Graphics PCB Design Tools Support
Revised: *May 2006*
Part number: *QII52015-6.0.0*

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Revised: *May 2006*
Part number: *QII52014-6.0.0*

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Revised: *May 2006*
Part number: *QII52005-6.0.0*

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Revised: *May 2006*
Part number: *QII51016-6.0.0*

Chapter 10. Timing Closure Floorplan
Revised: *May 2006*
Part number: *QII52006-6.0.0*

Chapter 11. Netlist Optimizations & Physical Synthesis
Revised: *May 2006*
Part number: *QII52007-6.0.0*

Chapter 12. Design Space Explorer
Revised: *May 2006*
Part number: *QII52008-6.0.0*

Chapter 13. LogicLock Design Methodology
Revised: *May 2006*
Part number: *QII52009-6.0.0*

Chapter 14. Synplicity Amplify Physical Synthesis Support
Revised: *May 2006*
Part number: *QII52011-6.0.0*

About this Handbook

This handbook provides comprehensive information about the Altera® Quartus®II design software, version 6.0.

How to Contact Altera

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Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	altera.com/mysupport/
	(800) 800-EPLD (3753) (7:00 a.m. to 5:00 p.m. Pacific Time)	(408) 544-7000 *(1)* (7:00 a.m. to 5:00 p.m. Pacific Time)
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com *(1)*	literature@altera.com *(1)*
Non-technical customer service	(800) 767-3753	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)
FTP site	ftp.altera.com	ftp.altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Third-Party Software Product Information

Third-party software products described in this handbook are not Altera products, are licensed by Altera from third parties, and are subject to change without notice. Updates to these third-party software products may not be concurrent with Quartus II software releases. Altera has assumed responsibility for the selection of such third-party software products and its use in the Quartus II 6.0 software release. To the extent that the software products described in this handbook are derived from third-party software, no third party warrants the software, assumes any liability regarding use of the software, or undertakes to furnish you any support or information relating to the software. EXCEPT AS EXPRESSLY SET FORTH IN THE APPLICABLE ALTERA PROGRAM LICENSE SUBSCRIPTION AGREEMENT UNDER WHICH THIS SOFTWARE WAS PROVDED TO YOU, ALTERA AND THIRD-PARTY LICENSORS DISCLAIM ALL WARRANTIES WITH RESPECT TO THE USE OF SUCH THIRD-PARTY SOFTWARE CODE OR DOCUMENTATION IN THE SOFTWARE, INCLUDING, WITHOUT LIMITATION, ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND NONINFRINGEMENT. For more information, including the latest available version of specific third-party software products, refer to the documentation for the software in question.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section I. Scripting & Constraint Entry

As a result of the increasing complexity of today's FPGA designs and the demand for higher performance, designers must make a large number of complex timing and logic constraints to meet their performance requirements. Once you have created a project and your design, you can use the Quartus® II software Assignment Editor and Floorplan Editor to specify your initial design constraints, such as pin assignments, device options, logic options, and timing constraints.

This section describes how to take advantage of these components of the Quartus II software, how to take advantage of Quartus II modular executables, and how to develop and run tool command language (Tcl) scripts to perform a wide range of functions.

This section includes the following chapters:

Revision History

The table below shows the revision history for Chapters 1, 2, 3, and 4.

Chapter(s)	Date / Version	Changes Made
1	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0. • Added Classic Timing Analyzer and TimeQuest Timing Analyzer information.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.0.
	May 2005 v5.0.0	• Updated for the Quartus II software version 5.0.0. • General formatting and editing updates. • Updated 2 graphics and references to reflect changes in the Quartus II software version 5.0.0
	Dec. 2004 v2.1	• Updated for Quartus II software version 4.2: • General formatting and editing updates. • Updated information about refreshing the Assignment Editor. • Updated figures. • Added information about how to make selections to the Assignment Editor window. • Added Time Groups reference. • Reworded description of Customizable Columns. • Added new section Creating Pin Locations Using the Assignment Editor. • Added new description to Exporting & Importing Assignments.
	June 2004 v2.0	• Updates to tables, figures. • New functionality in the Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
2	May 2006 v6.0.0	Added the TimeQuest timing analyzer feature.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.0.
	May 2005 v5.0.0	Updated for the Quartus II software version 5.0.0.
	Dec. 2004 v2.1	• Updates to tables and figures. • New functionality in the Quartus II software version 4.2.
	June 2004 v2.0	• Updates to tables and figures. • New functionality in the Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.

Chapter(s)	Date / Version	Changes Made
3	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0. • Reorganized content. • Added the TimeQuest timing analyzer feature.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.0.
	August 2005 v5.0.1	Minor text changes.
	May 2005 v5.0.0	Updated for the Quartus II software version 5.0.0.
	Dec. 2004 v2.1	• Updates to tables and figures. • New functionality in the Quartus II software version 4.2.
	Aug. 2004 v2.1	• Minor typographical corrections • Enhancements to example scripts.
	June 2004 v2.0	• Updates to tables, figures. • New functionality in the Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
4	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.0.
	May 2005 v5.0.0	Updated for the Quartus II software version 5.0.0.
	Dec. 2004 v1.1	Updated for Quartus II software version 4.2: • General formatting and editing updates. • Added new figures. • Added new introduction to To Delete a Revision That is a Design's Current Revision. • Added new section To Delete a Revision That is not a Design's Current Revision. • Updated figures. • Added new information about displaying assignments for multiple revisions. • Updated Archive a Project. • Updated Restore an Archived Project. • Version-Compatible Databases describes migration to Quartus II software version 4.2. • Corrected Tcl commands.
	June 2004 v1.0	Initial release.

1. Assignment Editor

QII52001-6.0.0

Introduction

The complexity of today's FPGA designs is compounded by the increasing density and associated pin counts of current FPGAs. It requires that you make a large number of pin assignments that include the pin locations and I/O standards to successfully implement a complex design in the latest generation of FPGAs.

To facilitate the process of entering these assignments, Altera® has developed an intuitive, spreadsheet interface called the Assignment Editor. The Assignment Editor is designed to make the process of creating, changing, and managing a large number of assignments as easy as possible.

This chapter discusses the following topics:

- Using the Assignment Editor
- Assignment Editor Features
- Assigning Pin Locations Using the Assignment Editor
- Creating Timing Constraints Using the Assignment Editor
- Exporting & Importing Assignments

Using the Assignment Editor

You can use the Assignment Editor throughout the design cycle. Before board layout begins, you can make pin assignments with the Assignment Editor. Throughout the design cycle, use the Assignment Editor to help achieve your design performance requirements by making timing assignments. You can also use the Assignment Editor to view, filter, and sort assignments based on node names or assignment type.

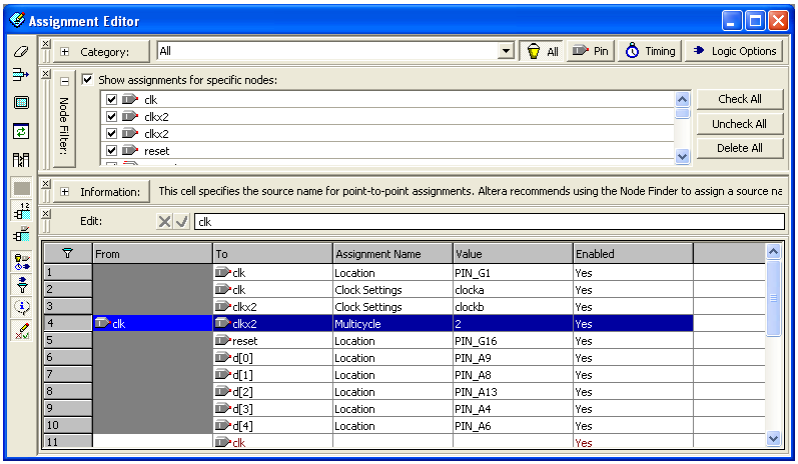
The Assignment Editor is a resizable window. This scalability makes it easy to view or edit your assignments right next to your design files. To open the Assignment Editor, click the **Assignment Editor** icon in the toolbar, or on the Assignments menu, click **Assignment Editor**.

You can also launch the Assignment Editor by pressing Ctrl+Shift+A.

Category, Node Filter, Information & Edit Bars

The Assignment Editor window is divided into four bars and a spreadsheet (Figure 1–1).

Figure 1–1. The Assignment Editor Window



You can hide all four bars in the View menu if desired, and you can collapse the **Category**, **Node Filter**, and **Information** bars. Table 1–1 provides a brief description of each bar.

Table 1–1. Assignment Editor Bar Descriptions

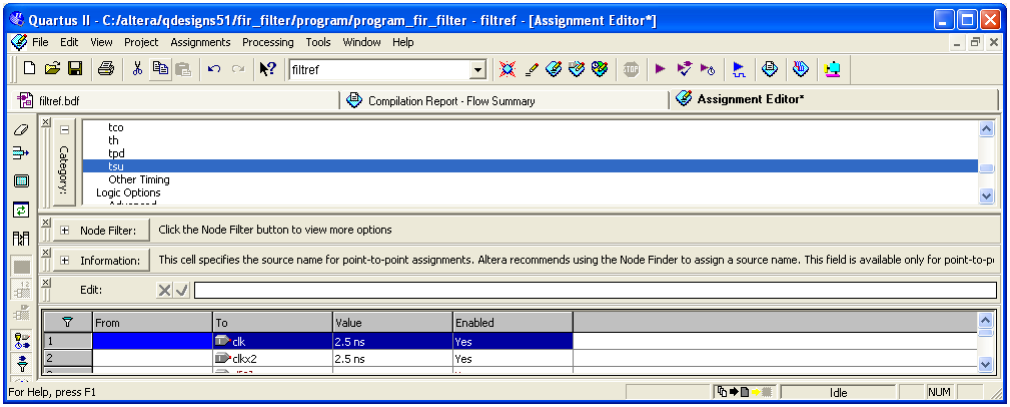
Bar Name	Description
Category	Lists the type of available assignments.
Node Filter	Lists a selection of design nodes to be viewed or assigned.
Information	Displays a description of the currently selected cell.
Edit	Allows you to edit the text in the currently selected cell(s).

Category Bar

The **Category** bar lists all assignment categories available for the selected device. You can use the **Category** bar to select a particular assignment type and to filter out all other assignments. Selecting an assignment category from the **Category** list changes the spreadsheet to show only applicable options and values. To search for a particular type of assignment, use the **Category** bar to filter out all other assignments.

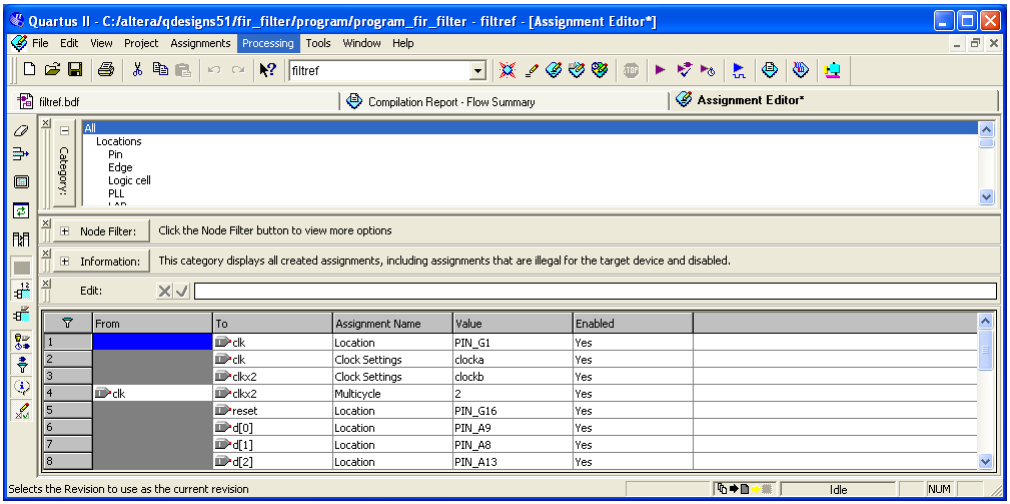
To view all t_{SU} assignments in your project, select **tsu** in the **Category** list (Figure 1–2).

Figure 1–2. t_{SU} Selected in the Category List



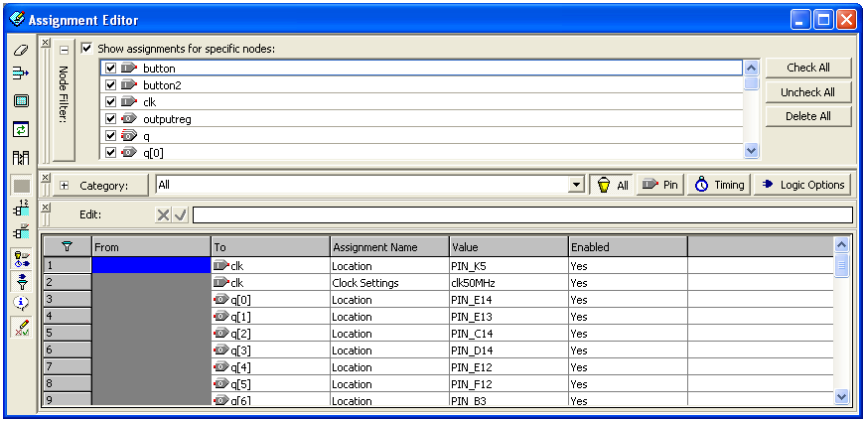
If you select **All** in the **Category** bar (Figure 1–3), the Assignment Editor displays all assignments.

Figure 1–3. All Selected in the Category List



When you collapse the **Category** bar, four shortcut buttons are displayed allowing you to select from various preset categories (Figure 1–4).

Figure 1–4. Category Bar



Use the **Pin** category to create pin location assignments. The **Pin** category displays additional information about each FPGA pin including its I/O Bank number, VREF group number, corresponding pad number, and primary and secondary functions.

When entering a pin number, the Assignment Editor auto completes the pin number. For example, instead of typing `Pin_AA3`, you can type `AA3` and let the Assignment Editor auto complete the pin number to `Pin_AA3`. You can also choose a pin location from the pins list by double clicking the cell in the location column. All occupied pin locations are shown in italics.

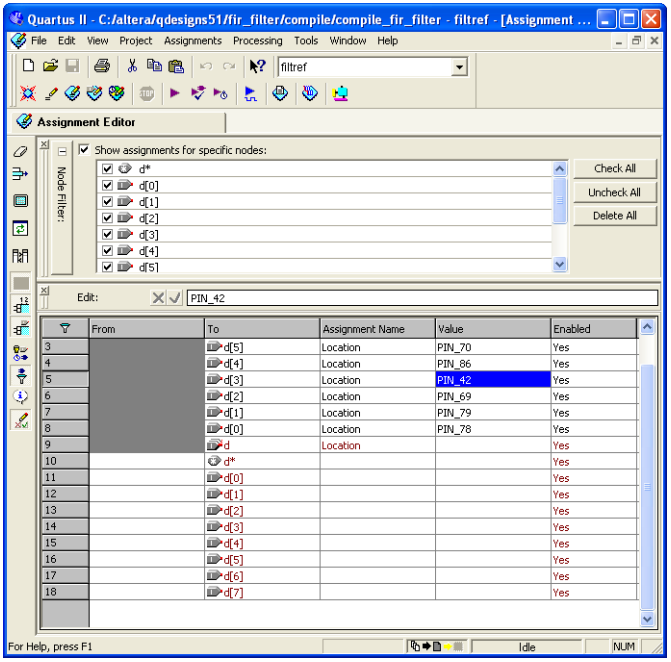
Node Filter Bar

When **Show assignments for specific nodes** is turned on, the spreadsheet shows only assignments for nodes matching the selected node name filters in the **Node Filter** bar. You can selectively enable individual node name filters listed in the **Node Filter** bar. You can create a new node name filter by selecting a node name with the Node Finder or typing a new node name filter. The Assignment Editor automatically inserts a spreadsheet row and pre-populates the **To** field with the node name filter. You can easily add an assignment to the matching nodes by entering it in the new row. Rows with incomplete assignments are shown in dark red. When you choose **Save** on the File menu, and there are incomplete assignments, a prompt gives you the choice to save and lose incomplete assignments, or cancel the save.

As shown in Figure 1–5, when all the bits of the d input bus are enabled in the **Node Filter** bar, all unrelated assignments are filtered out.

In the **Node Filter** bar, selecting a d input bus only highlights the row. If you want to enable the bus, you must turn on the bus.

Figure 1–5. Using the Node Filter Bar in the Assignment Editor



Information Bar

The **Information** bar provides a brief description of the currently selected cell and what information you should enter into the cell. For example, the **Information** bar describes if it is correct to enter a node name, or a number value into a cell. If the selected cell is a logic option, then the **Information** bar shows a description of that option.

For more information on logic options, refer to the Quartus® II Help.

Edit Bar

The **Edit** bar is an efficient way to enter a value into one or more spreadsheet cells.

To change the contents of multiple cells at the same time, select the cells in the spreadsheet (Figure 1–6), then type the new value into the **Edit** box in the **Edit** bar, and click **Accept** (Figure 1–7).

Figure 1–6. Edit Bar Selection

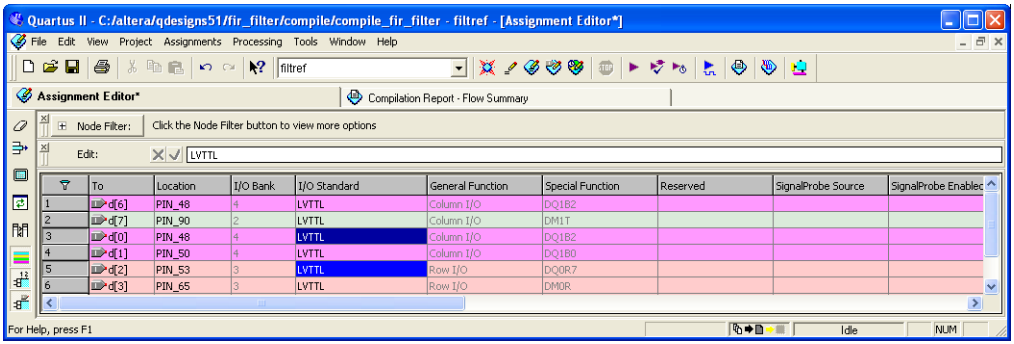
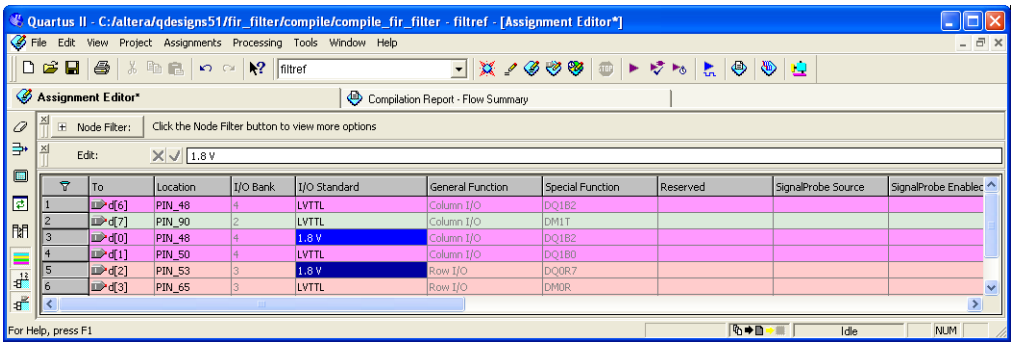


Figure 1–7. Edit Bar Change



Viewing & Saving Assignments in the Assignment Editor

Although the Assignment Editor is the most common method of entering and modifying assignments, there are other methods you can use to make and edit assignments. For this reason, you can refresh the Assignment Editor after you add, remove, or change an assignment outside the Assignment Editor.

By default, all assignments made in the Quartus II software are first stored into memory, then to the Quartus II Setting File (**.qsf**) on the disk after you start a processing task, or if you save or close your project. Saving assignments to memory avoids reading and writing to your disk drive and improves the performance of the software.

After making assignments in the Assignment Editor, on the File menu, click **Save** to save your assignments and update the Quartus II Settings File outside the Assignment Editor.

Starting with the Quartus II software version 5.1, you can force all assignments to be written to a disk drive. This is performed by turning off **Update assignments to disk during design processing only** in the **Processing** page of the **Options** settings dialog box on the Tools menu.

For more information on how the Quartus II software writes to the Quartus II Settings File, refer to the *Quartus II Project Management* chapter in volume 2 of the *Quartus II Handbook*.

You can refresh the Assignment Editor window by clicking **Refresh** from the View menu. If you make an assignment in the Quartus II software, such as in the Tcl console or in the Pin Planner, the Assignment Editor reloads the new assignments from memory. If you directly modify the Quartus II Settings File outside the Assignment Editor, click **Refresh** on the View menu to view the assignments.

If the Quartus II Settings File is edited while the project is open, go to the File menu and click **Save Project** to ensure that you are editing the latest Quartus II Settings File.

Each time the Assignment Editor is refreshed, the following message displays in the Message window:

```
Info: Assignments reloaded -- assignments updated outside Assignment Editor
```

Assignment Editor Features

You can open the Assignment Editor from many locations in the Quartus II software, including the Text Editor, the Node Finder, the Timing Closure Floorplan, the Pin Planner, the Compilation Report, and the Messages window. For example, you can highlight a node name in your design file and open the Assignment Editor with the node name populated.

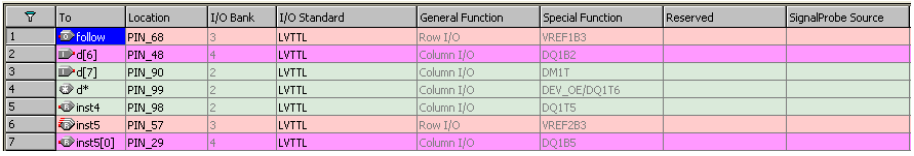
You can also open other windows from the Assignment Editor. From a node listed in the Assignment Editor spreadsheet, you can locate the node in any of the following windows: Pin Planner, Timing Closure Floorplan, Chip Editor, Block Editor, or Text Editor.

Using the Enhanced Spreadsheet Interface

One of the key features of the Assignment Editor is the spreadsheet interface. With the spreadsheet interface, you can sort columns, use pull-down list boxes, and copy and paste multiple cells into the Assignment Editor. As you enter an assignment, the font color of the row changes to indicate the status of the assignment. Refer to "Dynamic Syntax Checking" on page 1–9 for more information.

There are many ways to select or enter nodes into the spreadsheet including: the Node Finder, the Node Filter bar, the Edit bar, or by directly typing the node name into the cell in the spreadsheet. A node type icon is shown beside each node name and node name filter to identify its type. The node type icon identifies the entry as an input, output, bidirectional pin, a register, combinational logic, or an assignment group (Figure 1–8). The node type icon appears as an asterisk for node names and node name filters that use a wildcard character (* or ?).

Figure 1–8. Node Type Icon Displayed Beside Each Node Name in the Spreadsheet



	To	Location	I/O Bank	I/O Standard	General Function	Special Function	Reserved	SignalProbe Source
1	follow	PIN_68	3	LVTTL	Row I/O	VREF1B3		
2	d[6]	PIN_48	4	LVTTL	Column I/O	DQ1B2		
3	d[7]	PIN_90	2	LVTTL	Column I/O	DM1T		
4	d*	PIN_99	2	LVTTL	Column I/O	DEV_OE/DQ1T6		
5	inst4	PIN_98	2	LVTTL	Column I/O	DQ1T5		
6	inst5	PIN_57	3	LVTTL	Row I/O	VREF2B3		
7	inst5[0]	PIN_29	4	LVTTL	Column I/O	DQ1B5		

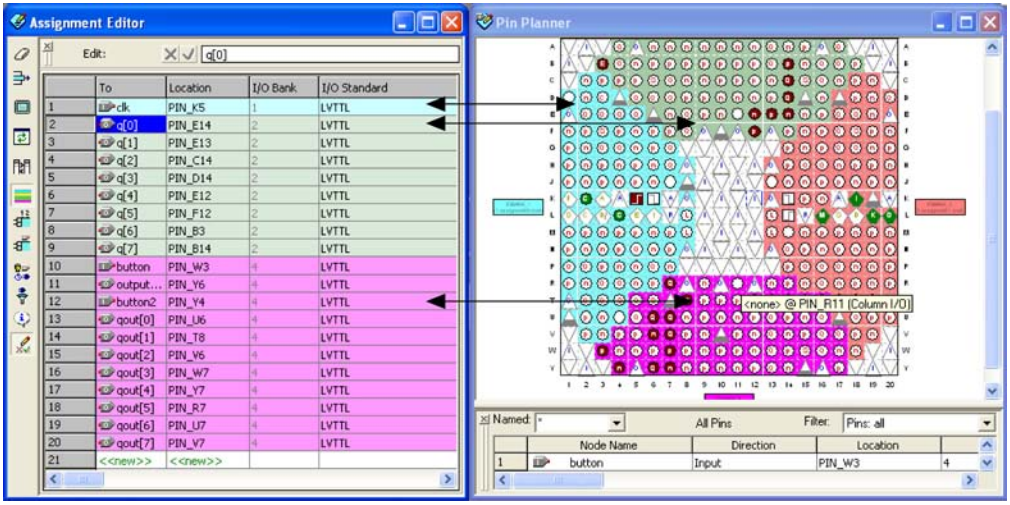
The Assignment Editor supports wildcards in the following types of assignments:

- All timing assignments
- Point-to-point global signal assignments (applicable to Stratix® II and Stratix devices)
- Point-to-point or pad-to-core delay chain assignments
- All assignments that support wild cards are shown in the drop list under the Assignment Name column of the Assignment Editor with "(Accepts wildcards/groups)" displayed beside it

The spreadsheet also supports customizable columns that allow you to show, hide, and arrange columns. For more information, refer to "Customizable Columns" on page 1–12.

When making pin location assignments, the background color of the cells coordinates with the color of the I/O bank shown in the Pin Planner (Figure 1–9).

Figure 1–9. Spreadsheet-Like Interface



Dynamic Syntax Checking

As you enter your assignments, the Assignment Editor performs simple legality and syntax checks. This checking is not as thorough as the checks performed during compilation, but it rejects incorrect settings. For example, the Assignment Editor does not allow assignment of a pin name to a no-connect pin. In this case, the assignment is not accepted and you must enter a different pin location.

The color of the text in each row indicates if the assignment is incomplete, incorrect, or disabled (Table 1–2). To customize the colors in the Assignment Editor, on the Tools menu, click **Options**.

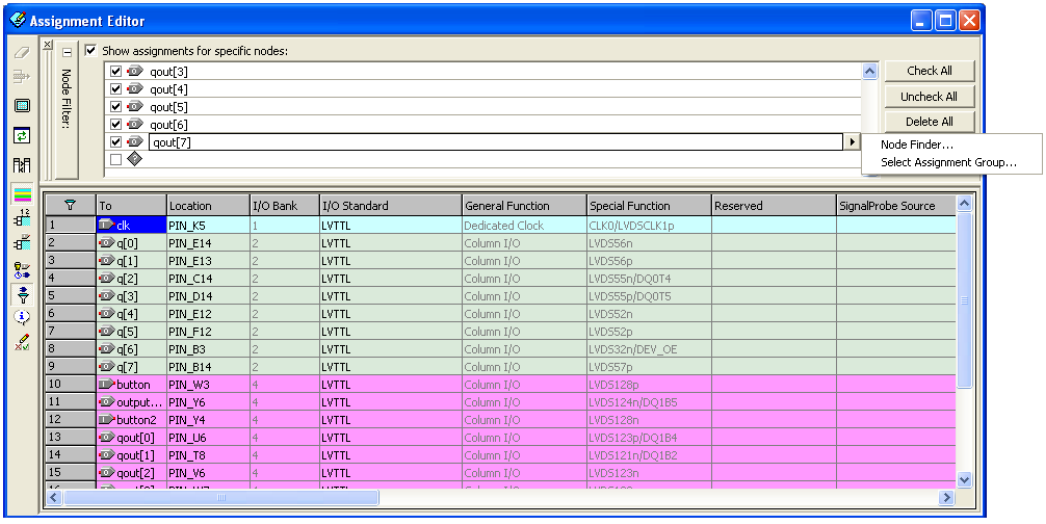
Table 1–2. Description of the Text Color in the Spreadsheet

Text Color	Description
Green	A new assignment can be created.
Yellow	The assignment contains warnings, such as an unknown node name.
Dark Red	The assignment is incomplete.
Bright Red	The assignment has an error, such as an illegal value.
Light Gray	The assignment is disabled.

Node Filter Bar

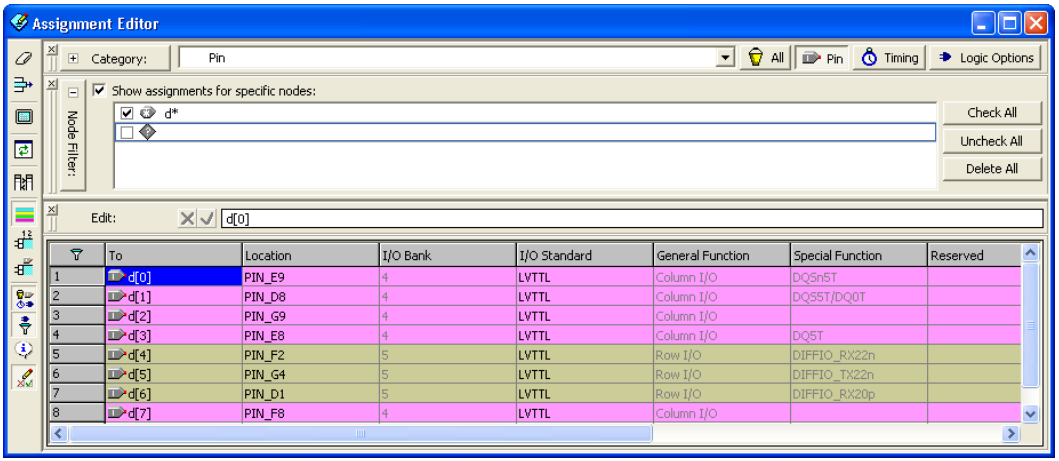
The **Node Filter** bar provides flexibility in how you view and make your settings. The **Node Filter** bar contains a list of node filters. To create a new entry, use the **Node Finder** or manually type the node name. Double-click an empty row in the **Node Filter** list, click on the **arrow**, and click **Node Finder** (Figure 1–10) to open the **Node Finder** dialog box.

Figure 1–10. Node Finder Option



In the **Node Filter** bar, you can turn each filter on or off. To turn off the **Node Filter** bar, turn off **Show assignments for specific nodes**. The wildcards (* and ?) are used to filter for a selection of all the design nodes with one entry in the Node Filter. For example, you can enter `d*` into the **Node Filter** list to view all assignments for `d[0]`, `d[1]`, `d[2]`, and `d[3]` (Figure 1–11).

Figure 1–11. Using the Node Filter Bar with Wildcards



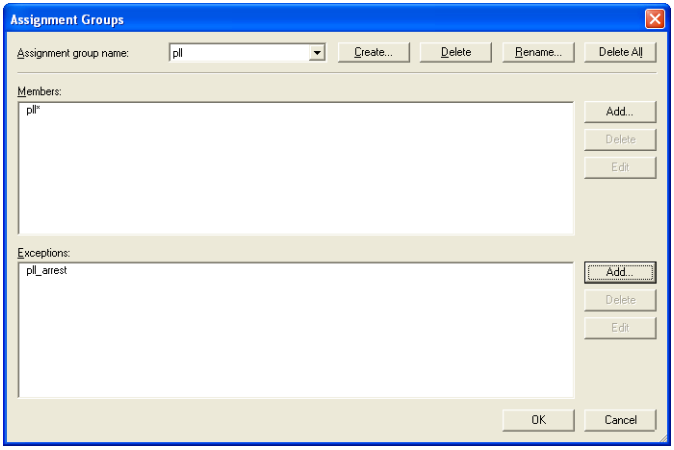
Using Assignment Groups

An assignment group is a collection of design nodes grouped together and represented as a single unit for the purpose of making assignments to the collection. Using assignment groups with the Assignment Editor provides the flexibility required for making complex fitting or timing assignments to a large number of nodes.

To create an assignment group, on the Assignments menu, click **Assignment (Time) Groups.** The **Assignment Groups** dialog box is shown. You can add or delete members of each assignment group with wild cards in the Node Finder (Figure 1–12).

For more information on using Assignment Groups for timing analysis, refer to the *Classic Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Figure 1–12. Assignment Groups Dialog Box



There are cases when wildcards are not flexible enough to select a large number of nodes that have similar node names. You can use assignment groups to combine wildcards, which select a large number of nodes, and use exceptions to remove nodes that you did not intend to select. Although settings may not always display correctly when you have wildcards or assignment groups, the fitter always recognizes assignments created with wildcards and assignment groups when the design is compiled.

Customizable Columns

To provide more control over the display of information in the spreadsheet, the Assignment Editor supports customizable columns.

You can move columns, sort them in ascending or descending order, show or hide individual columns, and align the content of the column left, center, or right for improved readability.

When the Quartus II software starts for the first time, you see a pre-selected set of columns. For example, when the Quartus II software is first started, the Comment column is hidden. To show or hide any of the available columns, on the View menu, click **Customize Columns**. When you restart the Quartus II software, your column settings are maintained.

Depending on the category selected, there are many different hidden columns you can display. For example, with the Pins category selected, there are many columns that are not shown by default, such as VREF group, pad number, output pin load, toggle rate, timing requirements, and fast input and output register options.

You can use the Comments column to document the purpose of a pin or to explain why you applied a timing or logic constraint. You can use the Enabled column to disable any assignment without deleting it. This feature is useful when performing multiple compilations with different timing constraints or logic optimizations.

Even though you can make many pin-related assignments with the **Pin** category selected, only the pin location assignment is disabled when you disable a row using the Enabled column.

Tcl Interface

Whether you use the Assignment Editor or another feature to create your design assignments, you can export them to a Tcl file. You can then use the Tcl file to reapply the settings or to archive your assignments. On the File menu, click **Export** to export your assignments (currently displayed in the spreadsheet of the Assignment Editor) to a Tcl script.

On the Project menu, click **Generate TCL File for Project** to generate a Tcl script file that sets up your design and applies all the assignments.

In addition, as you use the Assignment Editor to enter assignments, the equivalent Tcl commands are shown in the System Message window. You can reference these Tcl commands to create customized Tcl scripts (Figure 1–13). To copy a Tcl command from the Messages window, right-click the message and click **Copy**.

Figure 1–13. Equivalent Tcl Commands Displayed in the Messages Window

For more information on Tcl scripting with the Quartus II software, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Assigning Pin Locations Using the Assignment Editor

There are two methods for making pin assignments with the Assignment Editor. The first approach involves choosing a design node name for each device pin location. It is important to understand the properties of each pin on the FPGA device before you assign a design node to the location. For example, when following pin placement guidelines, you need to know which I/O bank or VREF group each pin belongs to.

On the Assignments menu, click **Assignment Editor**. To view all pin numbers in the targeted package, click the **Pin** category. On the View menu, click **Show All Assignable Pin Numbers**. You can customize the columns shown in the Assignment Editor to display property information about each pin including their pad numbers, as well as primary and secondary functions.

For more information on pin placement guidelines, refer to the *Selectable I/O Standards* chapters in the appropriate device handbook.

The second approach involves choosing a pin location for each pin in your design. To view all pin numbers in the targeted package, open the **Assignment Editor**, click the **Pin** category, and on the View menu, click **Show All Known Pin Names**. For each pin name, select a pin location.

For more information about creating pin assignments, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Creating Timing Constraints Using the Assignment Editor

Accurate timing constraints guide the place-and-route engine in the Quartus II software to help optimize your design into the FPGA. After completing a place-and-route, perform a static timing analysis using the classic timing analyzer or the TimeQuest timing analyzer to analyze slack and critical paths in your design.

If you are using the Classic Timing Analyzer, create timing constraints using the Assignment Editor. On the Assignments menu, click **Assignment Editor**. In the **Category** list, select **Timing**, and make timing assignments in the spreadsheet section of the Assignment Editor.

For more information on the Classic Timing Analyzer, refer to the *Classic Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

If you are using the TimeQuest Timing Analyzer, the TimeQuest Timing Analyzer uses timing assignments from a Synopsys Design Constraint (**.sdc**) file.

For information on converting the timing assignments in your Quartus Settings File to an Synopsys Design Constraint file, refer to the *Switching to the TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Exporting & Importing Assignments

Designs that use the LogicLock™ hierarchal design methodology use the **Import Assignment** command to import assignments into the current project. You can also use the **Export Assignments** command to save all the assignments in your project to a file to be used for archiving or to transfer assignments from one project to another.

On the Assignments menu, click **Export Assignments** or **Import Assignments** to do the following:

- Export your Quartus II assignments to a Quartus II Settings File.
- Import assignments from a Quartus II Entity Settings File (**.esf**), a MAX+PLUS® II Assignment and Configuration File (**.acf**), or a Comma Separated Value (**.csv**) file.

In addition to the **Export Assignments** and **Import Assignments** dialog boxes, the **Export** command on the File menu allows you to export your assignments to a Tcl Script (**.tcl**) file.

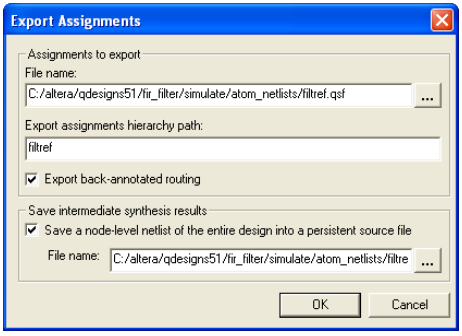
When applicable, the **Export** command exports the contents of the active window in the Quartus II software to another file format.

You can use these file formats for many different aspects of your project. For example, you can use a Comma Separated Value file for documentation purposes, or to transfer pin-related information to board layout tools. The Tcl file makes it easy to apply assignments in a scripted design flow. The LogicLock design flow uses the Quartus II Settings File to transfer your LogicLock region settings.

Exporting Assignments

You can use the **Export Assignments** dialog box to export your Quartus II software assignments into a Quartus II Settings File, generate a node-level netlist file, and export back-annotated routing information as a Routing Constraints File (**.rcf**) (Figure 1–14).

Figure 1–14. Export Assignments Dialog Box



On the Assignments menu, click **Export Assignments** to open the **Export Assignments** dialog box. The LogicLock design flow also uses this dialog box to export LogicLock regions.

For more information on using the **Export Assignments** dialog box to export LogicLock regions, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

On the File menu, click **Export** to export all assignments to a Tcl file or export a set of assignments to a Comma Separated Value file. When you export assignments to a Tcl file, only user-created assignments are written to the Tcl script file; default assignments are not exported.

When assignments are exported to a Comma Separated Value file, only the assignments displayed in the current view of the Assignment Editor are exported.

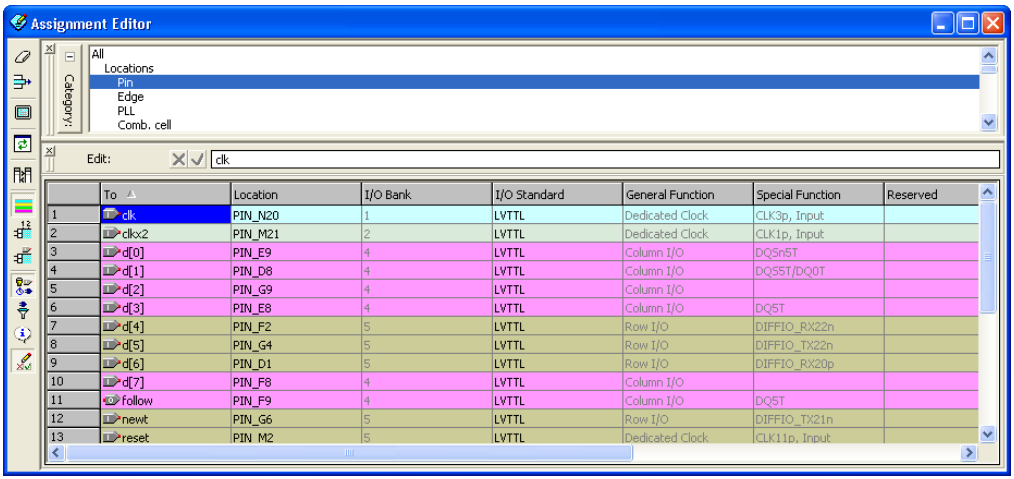
Exporting Pin Assignments

To export your pin assignments to a Comma Separated Value file, you can open the Assignment Editor and select **Pin** from the Category bar. The **Pin** category displays detailed properties about each pin similar to that of the device pin-out files in addition to the pin name and pin number. On the File menu, click **Export**, and select **Comma Separated Value File** from the **Save as type** list.

The first uncommented row of the Comma Separated Value file is a list of the column headings displayed in the Assignment Editor separated by commas. Each row below the header row represents the rows in the spreadsheet of the Assignment Editor (Figure 1–15). On the View menu, click **Customize Columns** to add and remove columns that are displayed in the spreadsheet. You can view and make edits to the Comma Separated Value file with Excel or other spreadsheet tools. If you intend to import the Comma Separated Value file back into the Quartus II software, the column headings must remain unedited and in the same order.

For more information on exporting pin assignments, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Figure 1–15. Assignment Editor With Category Set to Pin



The following code is an example of an exported Comma Separated Value file from the Assignment Editor:

```
# Note: The column header names should not be changed if you wish to import this .csv file
# into the Quartus II software.

To,Location,I/O Bank,I/O Standard,General Function,Special Function,Reserved,Enabled
clk,PIN_N20,1,LVTTL,Dedicated Clock,"CLK3p, Input",,Yes
clkx2,PIN_M21,2,LVTTL,Dedicated Clock,"CLK1p, Input",,Yes
d[0],PIN_E9,4,LVTTL,Column I/O,DQSn5T,,Yes
d[1],PIN_D8,4,LVTTL,Column I/O,DQS5T/DQ0T,,Yes
d[2],PIN_G9,4,LVTTL,Column I/O,,,Yes
d[3],PIN_E8,4,LVTTL,Column I/O,DQ5T,,Yes
d[4],PIN_F2,5,LVTTL,Row I/O,DIFFIO_RX22n,,Yes
d[5],PIN_G4,5,LVTTL,Row I/O,DIFFIO_TX22n,,Yes
d[6],PIN_D1,5,LVTTL,Row I/O,DIFFIO_RX20p,,Yes
```

```
d[7],PIN_F8,4,LVTTL,Column I/O,,,Yes
```

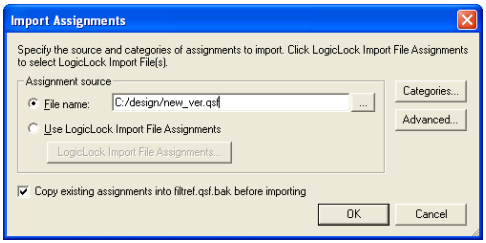
Importing Assignments

The **Import Assignments** dialog box allows you to import Quartus II assignments from a Quartus II Settings File, a Quartus II Entity Settings File, a MAX+PLUS II Assignment Configuration File, or a Comma Separated Value (Figure 1–16).

To import assignments from any of the supported assignment files, perform the following steps:

1. On the Assignments menu, click **Import Assignments**. The **Import Assignments** dialog box is shown (Figure 1–16).

Figure 1–16. Import Assignments Dialog Box



2. In the **File name** text-entry box, type the file name, or browse to the assignment file. The **Select File** dialog box is shown.
3. In the **Select File** dialog box**,** select the file, and click **Open**.
4. Click **OK**.

When you import a Comma Separated Value file, the first uncommented row of the file must be in the exact format as it was when exported.

When using the LogicLock™ flow methodology to import assignments, perform the following steps:

1. On the Assignments menu, click **Import Assignments**. The **Import Assignments** dialog box appears (Figure 1–16).
2. Turn on **Use LogicLock Import File Assignments,** and click **LogicLock Import File Assignments**.

3. When the **LogicLock Import File Assignments** dialog box opens, select the assignments to import and click **OK**.

For more information on using the **Import Assignments** dialog box to import LogicLock regions, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

You can create a backup copy of your assignments before importing new assignments by turning on the **Copy existing assignments into <*revision name*>.qsf.bak before importing** option.

When importing assignments from a file, you can choose which assignment categories to import by following these steps:

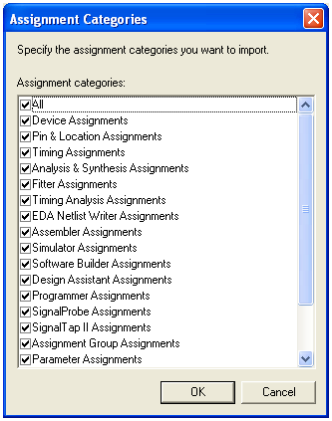
1. Click **Categories** in the **Import Assignments** dialog box.

2. Turn on the categories you want to import from the **Assignment categories** list (Figure 1–17).

To select specific types of assignments to import, click **Advanced** in the **Import Assignments** dialog box. The **Advanced Import Settings** dialog box appears. You can choose to import instance, entity, or global assignments, and select various assignment types to import.

For more information on these options, refer to the Quartus II Help.

Figure 1–17. Assignment Categories Dialog Box



Conclusion

As FPGAs continue to increase in density and pin count, it is essential to be able to quickly create and view design assignments. The Assignment Editor provides an intuitive and effective way of making assignments. With the spreadsheet interface and the **Category, Node Filter, Information**, and **Edit** bars, the Assignment Editor provides an efficient assignment entry solution for FPGA designers.

2. Command-Line Scripting

QII52002-6.0.0

Introduction

FPGA design software that easily integrates into your design flow saves time and improves productivity. The Altera® Quartus® II software provides you with a command-line executable for each step of the FPGA design flow to make the design process customizable and flexible.

The benefits provided by command-line executables include:

- Command-line control over each step of the design flow
- Easy integration with scripted design flows including makefiles
- Reduced memory requirements
- Improved performance

The command-line executables are also completely compatible with the Quartus II GUI, allowing you to use the exact combination of tools that you prefer.

This chapter describes how to take advantage of Quartus II command-line executables, and provides several examples of scripts that automate different segments of the FPGA design flow.

The Benefits of Command-Line Executables

The Quartus II command-line executables provide command-line control over each step of the design flow. Each executable includes options to control commonly used software settings. Each executable also provides detailed, built-in help describing its function, available options, and settings.

Command-line executables allow for easy integration with scripted design flows. It is simple to create scripts in any language with a series of commands. These scripts can be batch-processed, allowing for integration with distributed computing in server farms. You can also integrate the Quartus II command-line executables in makefile-based design flows. All of these features enhance the ease of integration between the Quartus II software and other EDA synthesis, simulation, and verification software.

Command-line executables add integration and scripting flexibility without sacrificing the ease-of-use of the Quartus II GUI. You can use the Quartus II GUI and command-line executables at different stages in the design flow. For example, you might use the Quartus II GUI to edit the

floorplan for the design, use the command-line executables to perform place-and-route, and return to the Quartus II GUI to perform debugging with the Chip Editor.

Command-line executables reduce the amount of memory required during each step in the design flow. Because each executable targets only one step in the design flow, it is relatively compact, both in file size and the amount of memory used when running. This memory reduction improves performance, and is particularly beneficial in design environments where computer networks or workstations are heavily used with reduced memory.

Introductory Example

The following introduction to design flow with command-line executables shows how to create a project, fit the design, perform timing analysis, and generate programming files.

The tutorial design included with the Quartus II software is used to demonstrate this functionality. If installed, the tutorial design is found in the <*Quartus II directory*>**/qdesigns/tutorial** directory.

Before making changes, copy the tutorial directory and type the four commands shown in Example 2–1 at a command prompt in the new project directory:

The <*Quartus II directory*>**/bin** directory must be in your `PATH` environment variable.

Example 2–1. Introductory Example

```
quartus_map filtref --source=filtref.bdf --family=CYCLONE ↵
quartus_fit filtref --part=EP1C12Q240C6 --fmax=80MHz --tsu=8ns ↵
quartus_asm filtref ↵
quartus_tan filtref ↵
```

The **quartus_map filtref --source=filtref.bdf --family=CYCLONE** command creates a new Quartus II project called **filtref** with the **filtref.bdf** file as the top-level file. It targets the Cyclone™ device family and performs logic synthesis and technology mapping on the design files.

The **quartus_fit filtref --part=EP1C12Q240C6 --fmax=80MHz --tsu=8ns** command performs fitting on the **filtref** project. This command specifies an EP1C12Q240C6 device and the fitter attempts to meet a global f_{MAX} requirement of 80 MHz and a global t_{SU} requirement of 8 ns.

The **quartus_asm filtref** command creates programming files for the **filtref** project.

The **quartus_tan filtref** command performs timing analysis on the **filtref** project to determine whether the design meets the timing requirements that were specified to the **quartus_fit** executable.

You can put the four commands from Example 2–1 into a batch file or script file, and run them. For example, you can create a simple UNIX shell script called **compile.sh**, which includes the code shown in Example 2–2.

Example 2–2. UNIX Shell Script: compile.sh

```
#!/bin/sh
PROJECT=filtref
TOP_LEVEL_FILE=filtref.bdf
FAMILY=Cyclone
PART=EP1C12Q240C6
FMAX=80MHz
quartus_map $PROJECT --source=$TOP_LEVEL_FILE --family=$FAMILY
quartus_fit $PROJECT --part=$PART --fmax=$FMAX
quartus_asm $PROJECT
quartus_tan $PROJECT
```

Edit the script as necessary and compile your project.

Command-Line Executables

Table 2–1 details the command-line executables and their respective descriptions.

Table 2–1. Quartus II Command-Line Executables & Descriptions (Part 1 of 4)

Executable	Description
Analysis & Synthesis quartus_map	Quartus II Analysis & Synthesis builds a single project database that integrates all the design files in a design entity or project hierarchy, performs logic synthesis to minimize the logic of the design, and performs technology mapping to implement the design logic using device resources such as logic elements.
Fitter quartus_fit	The Quartus II Fitter performs place-and-route by fitting the logic of a design into a device. The Fitter selects appropriate interconnection paths, pin assignments, and logic cell assignments. Quartus II Analysis & Synthesis must be run successfully before running the Fitter.

Table 2–1. Quartus II Command-Line Executables & Descriptions (Part 2 of 4)

Executable	Description
Assembler quartus_asm	The Quartus II Assembler generates a device programming image, in the form of one or more of the following from a successful fit (that is, place-and-route). ● Programmer Object Files (**.pof**) ● SRAM Object Files (**.sof**) ● Hexadecimal (Intel-Format) Output Files (**.hexout**) ● Tabular Text Files (**.ttf**) ● Raw Binary Files (**.rbf**) The **.pof** and **.sof** files are then processed by the Quartus II Programmer and downloaded to the device with the MasterBlaster™ or the ByteBlaster™ II download cable, or the Altera Programming Unit (APU). The Hexadecimal (Intel-Format) Output Files, Tabular Text Files, and Raw Binary Files can be used by other programming hardware manufacturers that provide support for Altera devices. The Quartus II Fitter must be run successfully before running the Assembler.
Classic Timing Analyzer quartus_tan	The Quartus II Classic Timing Analyzer computes delays for the given design and device, and annotates them on the netlist. Then, the Classic Timing Analyzer performs timing analysis, allowing you to analyze the performance of all logic in your design. The **quartus_tan** executable includes Tcl support. Quartus II Analysis & Synthesis or the Fitter must be run successfully before running the Classic Timing Analyzer.
TimeQuest Timing Analyzer quartus_sta	The Quartus II TimeQuest Timing Analyzer computes delays for the given design and device, and annotates them on the netlist. Then, the TimeQuest Timing Analyzer performs timing analysis, allowing you to analyze the performance of all logic in your design. The **quartus_sta** executable includes Tcl support and SDC support. Quartus II Analysis & Synthesis or the Fitter must be run successfully before running the TimeQuest Timing Analyzer.
Design Assistant quartus_drc	The Quartus II Design Assistant checks the reliability of a design based on a set of design rules. The Design Assistant is especially useful for checking the reliability of a design before converting the design for HardCopy® devices. The Design Assistant supports designs that target any Altera device supported by the Quartus II software, except MAX® 3000 and MAX 7000 devices. Quartus II Analysis & Synthesis or the Fitter must be run successfully before running the Design Assistant.
Compiler Database Interface quartus_cdb	The Quartus II Compiler Database Interface generates incremental netlists for use with LogicLock™ back-annotation, or back-annotates device and resource assignments to preserve the fit for future compilations. The **quartus_cdb** executable includes Tcl support. Analysis & Synthesis must be run successfully before running the Compiler Database Interface.

Table 2–1. Quartus II Command-Line Executables & Descriptions (Part 3 of 4)

Executable	Description
EDA Netlist Writer quartus_eda	The Quartus II EDA Netlist Writer generates netlist and other output files for use with other EDA tools. Analysis & Synthesis, the Fitter, or Timing Analyzer must be run successfully before running the EDA Netlist Writer, depending on the arguments used.
Simulator quartus_sim	The Quartus II Simulator tests and debugs the logical operation and internal timing of the design entities in a project. The Simulator can perform two types of simulation: functional simulation and timing simulation. The **quartus_sim** executable includes Tcl support. Quartus II Analysis & Synthesis must be run successfully before running a functional simulation. The Timing Analyzer must be run successfully before running a timing simulation.
Power Analyzer quartus_pow	The Quartus II PowerPlay Power Analyzer estimates the thermal dynamic power and the thermal static power consumed by the design. For newer families such as Stratix® II and MAX II, the power drawn from each power supply is also estimated. Quartus II Analysis & Synthesis or the Fitter must be run successfully before running the PowerPlay Power Analyzer.
Programmer quartus_pgm	The Quartus II Programmer programs Altera devices. The Programmer uses one of the supported file formats: • Programmer Object Files (**.pof**) • SRAM Object Files (**.sof**) • Jam File (**.jam**) • Jam Byte-Code File (**.jbc**) Make sure you specify a valid programming mode, programming cable, and operation for a specified device.
Convert Programming File quartus_cpf	The Quartus II Convert Programming File module converts one programing file format to a different possible format. Make sure you specify valid options and an input programming file to generate the new requested programming file format.
Quartus Shell quartus_sh	The Quartus II Shell acts as a simple Quartus II Tcl interpreter. The Shell has a smaller memory footprint than the other command-line executables that support Tcl. The Shell may be started as an interactive Tcl interpreter (shell), used to run a Tcl script, or used as a quick Tcl command evaluator, evaluating the remaining command-line arguments as one or more Tcl commands.

Table 2–1. Quartus II Command-Line Executables & Descriptions (Part 4 of 4)

Executable	Description
TimeQuest Timing Analyzer GUI quartus_staw	This executable opens the TimeQuest Timing Analyzer GUI. This is helpful because you don't have to open the entire Quartus II GUI for certain operations.
Programmer GUI quartus_pgmw	This executable opens up the programmer—a GUI to the quartus_pgm executable. This is helpful because users don't have to open the entire Quartus II GUI for certain operations

Command-Line Scripting Help

Help on command-line executables is available through different methods. You can access help built in to the executables with command-line options. You can use the Quartus II Command-Line and Tcl API Help browser for an easy graphical view of the help information. Additionally, you can refer to the *Scripting Reference Manual* on the Quartus II literature page on Altera's website, which has the same information in PDF format.

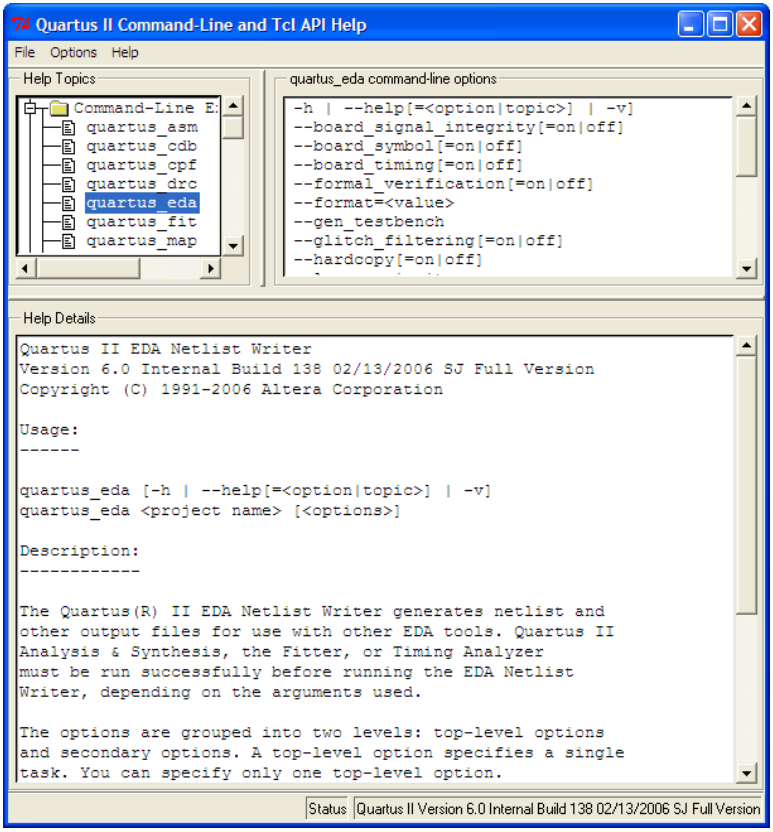
To use the Quartus II Command-Line and Tcl API Help browser, type the following:

```
quartus_sh --qhelp ↵
```

This command starts the Quartus II Command-Line and Tcl API Help browser, a viewer for information about the Quartus II Command-Line executables and Tcl API (Figure 2–1).

Use the `-h` option with any of the Quartus II Command-Line executables to get a description and list of supported options. Use the `--help=<option name>` option for detailed information about each option.

Figure 2–1. Quartus II Command-Line & Tcl API Help Browser



Command-Line Option Details

Command-line options are provided for many common global project settings and performing common tasks. You can use either of two methods to make assignments to an individual entity. If the project exists, open the project in the Quartus II GUI, change the assignment, and close the project. The changed assignment is updated in the Quartus II Settings File. Any command-line executables that are run after this update use the updated assignment. Refer to "Option Precedence" on page 2–8 for more

information. You can also make assignments using the Quartus II Tcl scripting API. If you want to completely script the creation of a Quartus II project, choose this method.

Refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Scripting information for all Quartus II project settings and assignments is located in the *QSF Reference Manual*.

Option Precedence

If you use command-line executables, you should be aware of the precedence of various project assignments and how to control the precedence. Assignments for a particular project exist in the Quartus II Settings File for the project. Assignments for a project can also be made with command-line options, as described earlier in this document. Project assignments are reflected in compiler database files that hold intermediate compilation results and reflect assignments made in the previous project compilation.

All command-line options override any conflicting assignments found in the Quartus II Settings File or the compiler database files. There are two command-line options to specify whether Quartus II Settings File or compiler database files take precedence for any assignments not specified as command-line options.

Any assignment not specified as a command-line option or found in the Quartus II Settings File or compiler database file is set to its default value.

The file precedence command-line options are `--read_settings_files` and `--write_settings_files`.

By default, the `--read_settings_files` and `--write_settings_files` options are turned on. Turning on the `--read_settings_files` option causes a command-line executable to read assignments from the Quartus II Settings File instead of from the compiler database files. Turning on the `--write_settings_files` option causes a command-line executable to update the Quartus II Settings File to reflect any specified options, as happens when closing a project in the Quartus II GUI.

Table 2–2 lists the precedence for reading assignments depending on the value of the `--read_settings_files` option.

Table 2–2. Precedence for Reading Assignments

Option Specified	Precedence for Reading Assignments
--read_settings_files = `on` (default)	1. Command-line options 2. Quartus II Settings File 3. Project database (**db** directory, if it exists) 4. Quartus II software defaults
--read_settings_files = `off`	1. Command-line options 2. Project database (**db** directory, if it exists) 3. Quartus II software defaults

Table 2–3 lists the locations to which assignments are written, depending on the value of the `--write_settings_files` command-line option.

Table 2–3. Location for Writing Assignments

Option Specified	Location for Writing Assignments
--write_settings_files = `on` (Default)	Quartus II Settings File and compiler database
--write_settings_files = `off`	Compiler database

Example 2–3 assumes that a project named **fir_filter** exists, and that the analysis and synthesis step has been performed (using the **quartus_map** executable).

Example 2–3. Write Settings Files

```
quartus_fit fir_filter --fmax=80MHz ↵
quartus_tan fir_filter ↵
quartus_tan fir_filter --fmax=100MHz --tao=timing_result-100.tao
    --write_settings_files=off ↵
```

The first command, **quartus_fit fir_filter --fmax=80MHz**, runs the **quartus_fit** executable and specifies a global f_{MAX} requirement of 80 MHz.

The second command, **quartus_tan fir_filter**, runs Quartus II timing analysis for the results of the previous fit.

The third command reruns Quartus II timing analysis with a global f_{MAX} requirement of 100 MHz and saves the result in a file called **timing_result-100.tao**. By specifying the `--write_settings_files=off` option, the command-line executable does not update the Quartus II Settings File to reflect the changed f_{MAX} requirement. The compiler database files reflect the changed f_{MAX} requirement. If the `--write_settings_files=off` option is not specified, the command-line executable updates the Quartus II Settings File to reflect the 100-MHz global f_{MAX} requirement.

Use the options `--read_settings_files=off` and `--write_settings_files=off` (where appropriate) to optimize the way that the Quartus II software reads and updates settings files. Example 2–4 shows how to avoid unnecessary reading and writing.

Example 2–4. Avoiding Unnecessary Reading & Writing

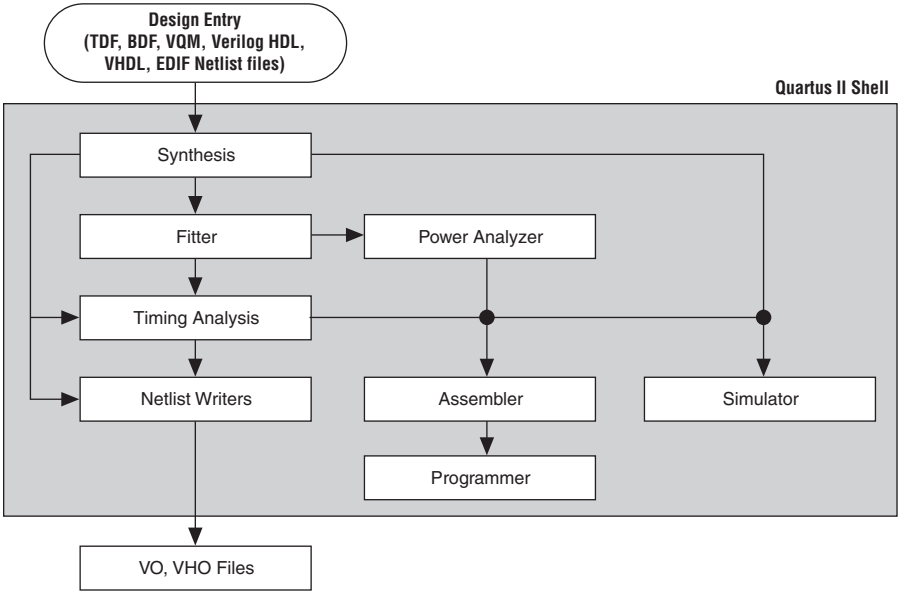
```
quartus_map filtref --source=filtref
    --part=ep1s10f780c5 ↵
quartus_fit filtref --fmax=100MHz
    --read_settings_files=off ↵
quartus_tan filtref --read_settings_files=off
    --write_settings_files=off ↵
quartus_asm filtref --read_settings_files=off
    --write_settings_files=off ↵
```

The **quartus_tan** and **quartus_asm** executables do not read or write settings files because they do not change any settings in the project.

Design Flow

Figure 2–2 shows a typical design flow.

Figure 2–2. Typical Design Flow



Compilation with quartus_sh --flow

Use the **quartus_sh** executable with the `--flow` option to perform a complete compilation flow with a single command. (For information about specialized flows, type `quartus_sh --help=flow` ↵ at a command prompt.) The `--flow` option supports the smart recompile feature and efficiently sets command-line arguments for each executable in the flow.

If you used the **quartus_cmd** executable to perform command-line compilations in earlier versions of the Quartus II software, you should use the `quartus_sh --flow` command beginning with the Quartus II software version 3.0.

The following example runs compilation, timing analysis, and programming file generation with a single command:

```
quartus_sh --flow compile filtref ↵
```

Text-Based Report Files

Each command-line executable creates a text report file when it is run. These files report success or failure, and contain information about the processing performed by the executable.

Report file names contain the revision name and the short-form name of the executable that generated the report file: <*revision*>.<*executable*>**.rpt**. For example, using the **quartus_fit** executable to place and route a project with the revision name **design_top** generates a report file named **design_top.fit.rpt**. Similarly, using the **quartus_tan** executable to perform timing analysis on a project with the revision name **fir_filter** generates a report file named **fir_filter.tan.rpt**.

As an alternative to parsing text-based report files, you can use the Tcl package called **::quartus::report**. For more information about this package, refer to "Command-Line Scripting Help" on page 2–6.

You can use Quartus II command-line executables in scripts that control a design flow that uses other software in addition to the Quartus II software. For example, if your design flow uses other synthesis or simulation software, and you can run the other software at a system command prompt, you can include it in a single script. The Quartus II command-line executables include options for common global project settings and operations, but you must use a Tcl script or the Quartus II GUI to set up a new project and apply individual constraints, such as pin location assignments and timing requirements. Command-line executables are very useful for working with existing projects, for making common global settings, and for performing common operations. For more flexibility in a flow, use a Tcl script, which makes it easier to pass data between different stages of the design flow and have more control during the flow.

For more information about Tcl scripts, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*, or the *Quartus II Scripting Reference Manual*.

For example, your script could run other synthesis software, then place-and-route the design in the Quartus II software, then generate output netlists for other simulation software. Example 2–5 shows how to do this with a UNIX shell script for a design that targets a Cyclone II device.

Example 2–5. Script for End-to-End Flow

```
#!/bin/sh
# Run synthesis first.
# This example assumes you use Synplify software
synplify -batch synthesize.tcl

# If your Quartus II project exists already, you can just
# recompile the design.
# You can also use the script described in a later example to
# create a new project from scratch
quartus_sh --flow compile myproject

# Use the quartus_tan executable to do best and worst case
# timing analysis
quartus_tan myproject --tao=worst_case
quartus_tan myproject --fast_model --tao=best_case

# Use the quartus_eda executable to write out a gate-level
# Verilog simulation netlist for ModelSim
quartus_eda my_project --simulation --tool=modelsim
 --format=verilog

# Perform the simulation with the ModelSim software
vlib cycloneii_ver
vlog -work cycloneii_ver c:/quartusii/eda/sim_lib/cycloneii_atoms.v
vlib work
vlog -work work my_project.vo
vsim -L cycloneii_ver -t 1ps work.my_project
```

Makefile Implementation

You can also use the Quartus II command-line executables in conjunction with the **make** utility to automatically update files when other files they depend on change. The file dependencies and commands used to update files are specified in a text file called a makefile.

To facilitate easier development of efficient makefiles, the following "smart action" scripting command is provided with the Quartus II software:

```
quartus_sh --determine_smart_action ↵
```

Because assignments for a Quartus II project are stored in the Quartus II Settings File (**.qsf**), including it in every rule results in unnecessary processing steps. For example, updating a setting related to programming file generation (which requires re-running only **quartus_asm**) modifies the Quartus II Settings File, requiring a complete recompilation if the Quartus II Settings File is included in every rule.

The smart action command determines the earliest command-line executable in the compilation flow that must be run based on the current Quartus II Settings File, and generates a change file corresponding to that executable. For a given command-line executable named **quartus_**<*executable*>, the change file is named with the format <*executable*>**.chg**. For example, if **quartus_map** must be re-run, the smart action command creates or updates a file named **map.chg**. Thus, rather than including the Quartus II Settings File in each makefile rule, include only the appropriate change file.

Example 2–6 uses change files and the smart action command. You can copy and modify it for your own use. A copy of this example is included in the help for the makefile option, which is available by typing:

```
quartus_sh --help=makefiles ↵
```

Example 2–6. Sample Makefile

```
###################################################################
# Project Configuration:
#
# Specify the name of the design (project), the Quartus II Settings
# File (.qsf), and the list of source files used.
###################################################################

PROJECT = chiptrip
SOURCE_FILES = auto_max.v chiptrip.v speed_ch.v tick_cnt.v time_cnt.v
ASSIGNMENT_FILES = chiptrip.qpf chiptrip.qsf

###################################################################
# Main Targets
#
# all: build everything
# clean: remove output files and database
###################################################################

all: smart.log $(PROJECT).asm.rpt $(PROJECT).tan.rpt

clean:
    rm -rf *.rpt *.chg smart.log *.htm *.eqn *.pin *.sof *.pof db

map: smart.log $(PROJECT).map.rpt
fit: smart.log $(PROJECT).fit.rpt
asm: smart.log $(PROJECT).asm.rpt
tan: smart.log $(PROJECT).tan.rpt
smart: smart.log

###################################################################
# Executable Configuration
###################################################################

MAP_ARGS = --family=Stratix
FIT_ARGS = --part=EP1S20F484C6
ASM_ARGS =
TAN_ARGS =

###################################################################
# Target implementations
###################################################################

STAMP = echo done >

$(PROJECT).map.rpt: map.chg $(SOURCE_FILES)
    quartus_map $(MAP_ARGS) $(PROJECT)
    $(STAMP) fit.chg

$(PROJECT).fit.rpt: fit.chg $(PROJECT).map.rpt
    quartus_fit $(FIT_ARGS) $(PROJECT)
```

```
    $(STAMP) asm.chg
    $(STAMP) tan.chg

$(PROJECT).asm.rpt: asm.chg $(PROJECT).fit.rpt
    quartus_asm $(ASM_ARGS) $(PROJECT)

$(PROJECT).tan.rpt: tan.chg $(PROJECT).fit.rpt
    quartus_tan $(TAN_ARGS) $(PROJECT)

smart.log: $(ASSIGNMENT_FILES)
    quartus_sh --determine_smart_action $(PROJECT) > smart.log

######################################################################
# Project initialization
######################################################################

$(ASSIGNMENT_FILES):
    quartus_sh --prepare $(PROJECT)

map.chg:
    $(STAMP) map.chg
fit.chg:
    $(STAMP) fit.chg
tan.chg:
    $(STAMP) tan.chg
asm.chg:
    $(STAMP) asm.chg
```

A Tcl script is provided with the Quartus II software to create or modify files that can be specified as dependencies in the make rules, assisting you in makefile development. Complete information about this Tcl script and how to integrate it with makefiles is available by running the following command:

```
quartus_sh --help=determine_smart_action ↵
```

Command-Line Scripting Examples

This section of the chapter presents various examples of command-line executable use.

Create a Project & Apply Constraints

The command-line executables include options for common global project settings and commands. To apply constraints such as pin locations and timing assignments, run a Tcl script with the constraints in it. You can write a Tcl constraint file from scratch, or generate one for an existing project. From the Project menu, click **Generate Tcl File for Project**.

Example 2–7 creates a project with a Tcl script and applies project constraints using the tutorial design files in the <*Quartus II installation directory*>**/qdesigns/tutorial/** directory:

Example 2–7. Tcl Script to Create Project & Apply Constraints

```
project_new filtref -overwrite
# Assign family, device, and top-level file
set_global_assignment -name FAMILY Cyclone
set_global_assignment -name DEVICE EP1C12Q240C6
set_global_assignment -name BDF_FILE filtref.bdf
# Assign pins
set_location_assignment -to clk Pin_28
set_location_assignment -to clkx2 Pin_29
set_location_assignment -to d[0] Pin_139
set_location_assignment -to d[1] Pin_140
# Other pin assignments could follow
# Create timing assignments
create_base_clock -fmax "100 MHz" -target clk clocka
create_relative_clock -base_clock clocka -divide 2 \
    -offset "500 ps" -target clkx2 clockb
set_multicycle_assignment -from clk -to clkx2 2
# Other timing assignments could follow
project_close
```

Save the script in a file called **setup_proj.tcl** and type the commands illustrated in Example 2–8 at a command prompt to create the design, apply constraints, compile the design, and perform fast-corner and slow-corner timing analysis. Timing analysis results are saved in two files.

Example 2–8. Script to Create & Compile a Project

```
quartus_sh -t setup_proj.tcl ↵
quartus_map filtref ↵
quartus_fit filtref ↵
quartus_asm filtref ↵
quartus_tan filtref --fast_model --tao=min.tao
    --export_settings=off ↵
    quartus_tan filtref --tao=max.tao
    --export_settings=off ↵
```

You can use the following two commands to create the design, apply constraints, and compile the design:

```
quartus_sh -t setup_proj.tcl ↵
quartus_sh --flow compile filtref ↵
```

The **quartus_sh --flow compile** command performs a full compilation, and is equivalent to clicking the **Start Compilation** button in the toolbar.

Check Design File Syntax

The UNIX shell script example shown in Example 2–9 assumes that the Quartus II software **fir_filter** tutorial project exists in the current directory. (You can find the **fir_filter** project in the <*Quartus II directory*>**/qdesigns/fir_filter** directory unless the Quartus II software tutorial files are not installed.)

The `--analyze_file` option performs a syntax check on each file. The script checks the exit code of the **quartus_map** executable to determine whether there is an error during the syntax check. Files with syntax errors are added to the `FILES_WITH_ERRORS` variable, and when all files are checked, the script prints a message indicating syntax errors. When options are not specified, the executable uses the project database values. If not specified in the project database, the executable uses the Quartus II software default values. For example, the **fir_filter** project is set to target the Cyclone device family, so it is not necessary to specify the `--family` option.

Example 2–9. Shell Script to Check Design File Syntax

```
#!/bin/sh
FILES_WITH_ERRORS=""
# Iterate over each file with a .bdf or .v extension
for filename in `ls *.bdf *.v`
do
  # Perform a syntax check on the specified file
    quartus_map fir_filter --analyze_file=$filename
  # If the exit code is non-zero, the file has a syntax error
    if [ $? -ne 0 ]
    then
       FILES_WITH_ERRORS="$FILES_WITH_ERRORS $filename"
    fi
done
if [ -z "$FILES_WITH_ERRORS" ]
then
    echo "All files passed the syntax check"
    exit 0
else
    echo "There were syntax errors in the following file(s)"
    echo $FILES_WITH_ERRORS
    exit 1
fi
```

Create a Project & Synthesize a Netlist Using Netlist Optimizations

This example creates a new Quartus II project with a file **top.edf** as the top-level entity. The `--enable_register_retiming=on` and `--enable_wysiwyg_resynthesis=on` options allow the technology mapper to optimize the design using gate-level register retiming and technology remapping.

For more details about register retiming, WYSIWYG primitive resynthesis, and other netlist optimization options, refer to the Quartus II Help.

The `--part` option tells the technology mapper to target an EP20K600EBC652-1X device. To create the project and synthesize it using the netlist optimizations described above, type the command shown in Example 2–10 at a command prompt.

Example 2–10. Creating a Project & Synthesizing a Netlist Using Netlist Optimizations

```
quartus_map top --source=top.edf --enable_register_retiming=on
    --enable_wysiwyg_resynthesis=on --part=EP20K600EBC652-1X ↵
```

Archive & Restore Projects

You can archive or restore a Quartus II project with a single command. This makes it easy to take snapshots of projects when you use batch files or shell scripts for compilation and project management. Use the `--archive` or `--restore` options for **quartus_sh** as appropriate. Type the command shown in Example 2–11 at a system command prompt to archive your project.

Example 2–11. Archiving a Project

```
quartus_sh --archive <project name> ↵
```

The archive file is automatically named <*project name*>.**qar**. If you want to use a different name, rename the archive after it has been created. This command overwrites any existing archive with the same name.

To restore a project archive, type the command shown in Example 2–12 at a system command prompt:

Example 2–12. Restoring a Project Archive

```
quartus_sh --restore <archive name> ↵
```

The command restores the project archive to the current directory and overwrites existing files.

Perform I/O Assignment Analysis

You can perform I/O assignment analysis with a single command. I/O assignment analysis checks pin assignments to ensure they do not violate board layout guidelines. I/O assignment analysis does not require a complete place and route, so it is a quick way to ensure your pin assignments are correct. The command shown in Example 2–13 performs I/O assignment analysis for the specified project and revision.

Example 2–13. Performing I/O Assignment Analysis

```
quartus_fit --check_ios <project name> --rev=<revision name> ↵
```

Update Memory Contents without Recompiling

You can use two simple commands to update the contents of memory blocks in your design without recompiling. Use the **quartus_cdb** executable with the `--update_mif` option to update memory contents from Memory Initialization Files or Hexadecimal (Intel-Format) Files. Then re-run the assembler with the **quartus_asm** executable to regenerate the SOF, POF, and any other programming files.

Example 2–14 shows these two commands:

Example 2–14. Commands to Update Memory Contents without Recompiling

```
quartus_cdb --update_mif <project name> [--rev=<revision name>]↵
quartus_asm <project name> [--rev=<revision name>]↵
```

Example 2–15 shows the commands for a DOS batch file for this example. You can paste the following lines into a DOS batch file called **update_memory.bat**.

Example 2–15. Batch file to Update Memory Contents without Recompiling

```
quartus_cdb --update_mif %1 --rev=%2
quartus_asm %1 --rev=%2
```

Type the following command at a system command prompt:

```
update_memory.bat <project name> <revision name> ↵
```

Fit a Design as Quickly as Possible

This example assumes that a project called **top** exists in the current directory, and that the name of the top-level entity is **top**. The `--effort=fast` option causes the Fitter to use the fast fit algorithm to increase compilation speed, possibly at the expense of reduced f_{MAX} performance. The `--one_fit_attempt=on` option restricts the Fitter to only one fitting attempt for the design.

To attempt to fit the project called **top** as quickly as possible, type command shown in Example 2–16 at a command prompt.

Example 2–16. Fitting a Project Quickly

```
quartus_fit top --effort=fast --one_fit_attempt=on ↵
```

Fit a Design Using Multiple Seeds

This shell script example assumes that the Quartus II software tutorial project called **fir_filter** exists in the current directory (defined in the file **fir_filter.qpf**). If the tutorial files are installed on your system, this project exists in the <*Quartus II directory*>**/qdesigns**<*quartus_version_number*>**/fir_filter** directory. Because the top-level entity in the project does not have the same name as the project, you must specify the revision name for the top-level entity with the `--rev` option. The `--seed` option specifies the seeds to use for fitting.

A seed is a parameter that affects the random initial placement of the Quartus II Fitter. Varying the seed can result in better performance for some designs.

After each fitting attempt, the script creates new directories for the results of each fitting attempt and copies the complete project to the new directory so that the results are available for viewing and debugging after the script has completed.

Example 2–17 is designed for use on UNIX systems using **sh** (the shell).

Example 2–17. Shell Script to Fit a Design Using Multiple Seeds

```
#!/bin/sh
ERROR_SEEDS=""
quartus_map fir_filter --rev=filtref
# Iterate over a number of seeds
for seed in 1 2 3 4 5
do
echo "Starting fit with seed=$seed"
# Perform a fitting attempt with the specified seed
        quartus_fit fir_filter --seed=$seed --rev=filtref
# If the exit-code is non-zero, the fitting attempt was
# successful, so copy the project to a new directory
        if [ $? -eq 0 ]
        then
          mkdir ../fir_filter-seed_$seed
          mkdir ../fir_filter-seed_$seed/db
          cp * ../fir_filter-seed_$seed
          cp db/* ../fir_filter-seed_$seed/db
        else
          ERROR_SEEDS="$ERROR_SEEDS $seed"
        fi
done
if [ -z "$ERROR_SEEDS" ]
then
        echo "Seed sweeping was successful"
        exit 0
else
        echo "There were errors with the following seed(s)"
        echo $ERROR_SEEDS
        exit 1
fi
```

Use the Design Space Explorer included with the Quartus II software (DSE) script (by typing `quartus_sh --dse` ↵ at a command prompt) to improve design performance by performing automated seed sweeping.

For more information about the DSE, type `quartus_sh --help=dse` ↵ at the command prompt, or refer to the *Design Space Explorer* chapter in volume 2 of the *Quartus II Handbook*, or see the Quartus II Help.

The QFlow Script

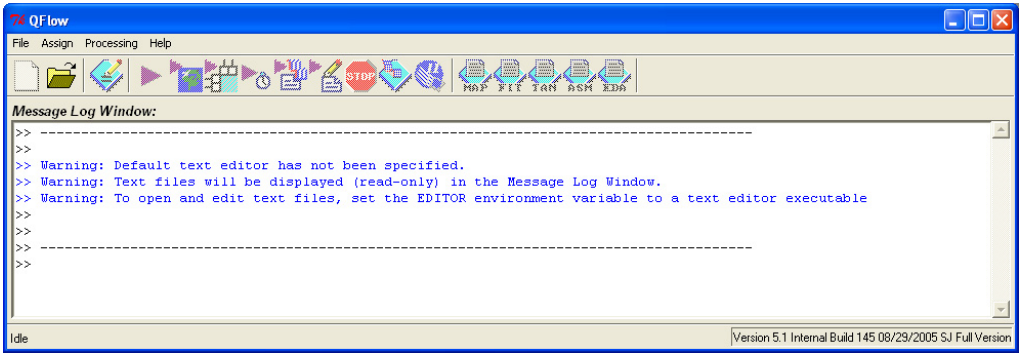
A Tcl/Tk-based graphical interface called QFlow is included with the command-line executables. You can use the QFlow interface to open projects, launch some of the command-line executables, view report files, and make some global project assignments. The QFlow interface can run the following command-line executables:

- **quartus_map** (Analysis & Synthesis)
- **quartus_fit** (Fitter)
- **quartus_tan** (Timing Analysis)
- **quartus_asm** (Assembler)
- **quartus_eda** (EDA Netlist Writer)

To view floorplans or perform other GUI-intensive tasks, launch the Quartus II software.

Start QFlow by typing the following command at a command prompt: `quartus_sh -g` ↵ . Figure 2–3 shows the QFlow interface.

Figure 2–3. QFlow Interface



The QFlow script is located in the <*Quartus II directory*>**/common/tcl/apps/qflow/** directory.

3. Tcl Scripting

QII52003-6.0.0

Introduction

Developing and running tool command language (Tcl) scripts to control the Altera® Quartus® II software allows you to perform a wide range of functions, such as compiling a design or writing procedures to automate common tasks.

You can use Tcl scripts to manage a Quartus II project, make assignments, define design constraints, make device assignments, run compilations, perform timing analysis, import LogicLock™ region assignments, use the Quartus II Chip Editor, and access reports. You can automate your Quartus II assignments using Tcl scripts so that you do not have to create them individually. Tcl scripts also facilitate project or assignment migration. For example, when using the same prototype or development board for different projects, you can automate reassignment of pin locations in each new project. The Quartus II software can also generate a Tcl script based on all the current assignments in the project, which aids in switching assignments to another project.

The Quartus II software Tcl commands follow the EDA industry Tcl application programming interface (API) standards for using command-line options to specify arguments. This simplifies learning and using Tcl commands. If you encounter an error using a command argument, the Tcl interpreter gives help information showing correct usage.

This chapter includes sample Tcl scripts for automating the Quartus II software. You can modify these example scripts for use with your own designs. You can find more Tcl scripts in the Design Examples section of the Support area of Altera's website.

What is Tcl?

Tcl (pronounced tickle) is a popular scripting language that is similar to many shell scripting and high-level programming languages. It provides support for control structures, variables, network socket access, and APIs. Tcl is the EDA industry-standard scripting language used by Synopsys, Mentor Graphics®, Synplicity, and Altera software. It allows you to create custom commands and works seamlessly across most development platforms. For a list of recommended literature on Tcl, refer to "References" on page 3–50.

You can create your own procedures by writing scripts containing basic Tcl commands, user-defined procedures, and Quartus II API functions. You can then automate your design flow, run the Quartus II software in batch mode, or execute the individual Tcl commands interactively in the Quartus II Tcl interactive shell.

If you're unfamiliar with Tcl scripting, or are a Tcl beginner, refer to the "Tcl Scripting Basics" on page 3–42 for an introduction to Tcl scripting.

The Quartus II software, beginning with version 4.1, supports Tcl/Tk version 8.4, supplied by the Tcl DeveloperXchange at **tcl.activestate.com**.

Quartus II Tcl Packages

The Quartus II Tcl commands are grouped in packages by function. Table 3–1 describes each Tcl package.

Table 3–1. Tcl Packages

Package Name	Package Description
advanced_timing	Traverse the timing netlist and get information about timing nodes
backannotate	Back annotate assignments
chip_editor	Identify and modify resource usage and routing with the Chip Editor
database_manager	Manage version-compatible database files
device	Get device and family information from the device database
flow	Compile a project, run command-line executables and other common flows
insystem_memory_edit	Read and edit memory contents in Altera devices
jtag	Control the jtag chain
logic_analyzer_interface	Query and modify the logic analyzer interface output pin state
logiclock	Create and manage LogicLock regions
misc	Perform miscellaneous tasks
project	Create and manage projects and revisions, make any project assignments including timing assignments
report	Get information from report tables, create custom reports
sdc	Specifies constraints and exceptions to the TimeQuest Analyzer
simulator	Configure and perform simulations
sta	Contains the set of Tcl functions for obtaining advanced information from the TimeQuest Timing Analyzer
stp	Run the SignalTap® II logic analyzer
timing	Annotate timing netlist with delay information, compute and report timing paths
timing_assignment	Contains the set of Tcl functions for making project-wide timing assignments, including clock assignments; all Tcl commands designed to process Classic Timing Analyzer assignments have been moved to this package
timing_report	List timing paths

By default, only the minimum number of packages is loaded automatically with each Quartus II executable. This keeps the memory requirement for each executable as low as possible. Because the minimum number of packages is automatically loaded, you must load other packages before you can run commands in those packages.

Table 3–2 lists the Quartus II Tcl packages available with Quartus II executables and indicates whether a package is loaded by default (●) or is available to be loaded as necessary (◓). A clear circle (○) means that the package is not available in that executable.

Table 3–2. Tcl Package Availability by Quartus II Executable (Part 1 of 2)

Packages	Quartus II Executable						
	Quartus_sh	Quartus_tan	Quartus_cdb	Quartus_sim	Quartus_stp	Quartus_sta	Tcl Console
advanced_timing	○	◓	○	○	○	○	○
backannotate	○	○	◓	○	○	○	◓
chip_editor	○	○	◓	○	○	○	○
device	●	◓	●	●	○	●	◓
flow	◓	◓	◓	◓	○	◓	◓
insystem_memory_edit	○	○	○	○	●	○	○
jtag	○	○	○	○	●	○	○
logic_analyzer_ interface	○	○	○	○	●	○	○
logiclock	○	◓	◓	○	○	○	◓
misc	●	●	●	●	●	●	●
old_api	○	○	○	○	○	○	●
project	●	●	●	●	●	●	●
report	◓	◓	◓	●	○	●	◓
sdc	○	○	○	○	○	●	○
simulator	○	○	○	●	○	○	○
sta	○	○	○	○	○	●	○
stp	○	○	○	○	●	○	○

Table 3–2. Tcl Package Availability by Quartus II Executable (Part 2 of 2)

Packages	Quartus II Executable						
	Quartus_sh	Quartus_tan	Quartus_cdb	Quartus_sim	Quartus_stp	Quartus_sta	Tcl Console
timing	○	●	○	○	○	○	○
timing_assignment	●	●	●	●	●	○	○
timing_report	○	◓	○	○	●	○	●

Notes to Table 3–2:

(1) A dark circle (●) indicates that the package is loaded automatically.

(2) A half-circle (◓) means that the package is available but not loaded automatically.

(3) A white circle (○) means that the package is not available for that executable.

Because different packages are available in different executables, you must run your scripts with executables that include the packages you use in the scripts. For example, if you use commands in the **timing** package, you must use the **quartus_tan** executable to run the script because the **quartus_tan** executable is the only one with support for the **timing** package.

Loading Packages

To load a Quartus II Tcl package, use the **load_package** command as follows:

```
load_package [-version <version number>] <package name>
```

This command is similar to the **package require** Tcl command (described in Table 3–3 on page 3–7), but you can easily alternate between different versions of a Quartus II Tcl package with the **load_package** command.

For additional information about these and other Quartus II command-line executables, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Quartus II Tcl API Help

Access the Quartus II Tcl API Help reference by typing the following command at a system command prompt:

```
quartus_sh --qhelp ↵
```

This command runs the Quartus II Command-Line and Tcl API help browser, which documents all commands and options in the Quartus II Tcl API. It includes detailed descriptions and examples for each command.

In addition, the information in the Tcl API help is available in the *Quartus II Scripting Reference Manual*, which is available in PDF on the Quartus II Literature page on the Altera web site.

Quartus II Tcl help allows easy access to information about the Quartus II Tcl commands. To access the help information, type `help` at a Tcl prompt, as shown in Example 3–1.

Example 3–1. Help Output

```
tcl> help
---------------------------------------------------------------------------

----------------------------------
Available Quartus II Tcl Packages:
----------------------------------

Loaded                          Not Loaded
-----------------------------   ----------------------
::quartus::misc                 ::quartus::device
::quartus::old_api              ::quartus::backannotate
::quartus::project              ::quartus::flow
::quartus::timing_assignment    ::quartus::logiclock
::quartus::timing_report        ::quartus::report


* Type "help -tcl"
  to get an overview on Quartus II Tcl usages.
```

Using the `-tcl` option with `help` displays an introduction to the Quartus II Tcl API that focuses on how to get help for Tcl commands (short help and long help) and Tcl packages.

The Tcl API help is also available in Quartus II online help. Search for the command or package name to find details about that command or package.

Table 3–3 summarizes the help options available in the Tcl environment.

Table 3–3. Help Options Available in the Quartus II Tcl Environment (Part 1 of 2)

Help Command	Description
`help`	To view a list of available Quartus II Tcl packages, loaded and not loaded.
`help -tcl`	To view a list of commands used to load Tcl packages and access command-line help.
`help -pkg` <*package_name*> `[-version` <*version number*>`]`	To view help for a specified Quartus II package that includes the list of available Tcl commands. For convenience, you can omit the `::quartus::` package prefix, and type `help -pkg` <*package name*> ↵. If you do not specify the `-version` option, help for the currently loaded package is displayed by default. If the package for which you want help is not loaded, help for the latest version of the package is displayed by default. Examples: `help -pkg ::quartus::p` ↵ `help -pkg ::quartus::project` ↵ `help -pkg project rhelp -pkg project -version 1.0` ↵
<*command_name*> `-h` or <*command_name*> `-help`	To view short help for a Quartus II Tcl command for which the package is loaded. Examples: `project_open -h` ↵ `project_open -help` ↵
`package require ::quartus::`<*package name*> `[`<*version*>`]`	To load a Quartus II Tcl package with the specified version. If <*version*> is not specified, the latest version of the package is loaded by default. Example: `package require ::quartus::project 1.0` ↵ This command is similar to the **load_package** command. The advantage of using **load_package** is that you can alternate freely between different versions of the same package. Type <*package name*> `[-version` <*version number*>`]` ↵ to load a Quartus II Tcl package with the specified version. If the `-version` option is not specified, the latest version of the package is loaded by default. Example: `load_package ::quartus::project -version 1.0` ↵

Table 3–3. Help Options Available in the Quartus II Tcl Environment (Part 2 of 2)

Help Command	Description
`help -cmd` <*command name*> `[-version` <*version number*>`]` *or* <*command name*> `-long_help`	To view long help for a Quartus II Tcl command. Only <*command name*> `-long_help` requires that the associated Tcl package is loaded. If you do not specify the `-version` option, help for the currently loaded package is displayed by default. If the package for which you want help is not loaded, help for the latest version of the package is displayed by default. Examples: `project_open -long_help` ↵ `help -cmd project_open` ↵ `help -cmd project_open -version 1.0` ↵
`help -examples`	To view examples of Quartus II Tcl usage.
`help -quartus`	To view help on the predefined global Tcl array that can be accessed to view information about the Quartus II executable that is currently running.
`quartus_sh --qhelp`	To launch the Tk viewer for Quartus II command-line help and display help for the command-line executables and Tcl API packages. For more information about this utility, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Executables Supporting Tcl

Some of the Quartus II command-line executables support Tcl scripting (refer to Table 3–4). Each executable supports different sets of Tcl packages. Refer to Table 3–4 to determine the appropriate executable to run your script.

Table 3–4. Command-line Executables Supporting Tcl Scripting

Executable Name	Executable Description
quartus_sh	The Quartus II Shell is a simple Tcl scripting shell, useful for making assignments, general reporting, and compiling.
quartus_tan	Use the Quartus II Classic Timing Analyzer to perform simple timing reporting and advanced timing analysis.
quartus_cdb	The Quartus II Compiler Database supports back annotation, LogicLock region operations, and Chip Editor functions.
quartus_sim	The Quartus II Simulator supports the automation of design simulation.
quartus_sta	The TimeQuest Timing Analyzer supports SDC terminology for constraint entry and reporting.
quartus_stp	The Quartus II SignalTap II executable supports in-system debugging tools.

The **quartus_tan** and **quartus_cdb** executables support supersets of the packages supported by the **quartus_sh** executable. Use the **quartus_sh** executable if you run Tcl scripts with only project management and assignment commands, or if you need a Quartus II command-line executable with a small memory footprint.

For more information about these command-line executables, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Command-Line Options: -t, -s & --tcl_eval

Table 3–5 lists three command-line options you can use with executables that support Tcl.

Table 3–5. Command-Line Options Supporting Tcl Scripting

Command-Line Option	Description
`-t` <*script file*> [<*script args*>]	Run the specified Tcl script with optional arguments.
`-s`	Open the executable in the interactive Tcl shell mode.
`--tcl_eval` <*tcl command*>	Evaluate the remaining command-line arguments as Tcl commands. For example, the following command displays help for the project package: `quartus_sh --tcl_eval help -pkg project`

Run a Tcl Script

Running an executable with the `-t` option runs the specified Tcl script. You can also specify arguments to the script. Access the arguments through the `argv` variable, or use a package such as **cmdline**, which supports arguments of the following form:

-<argument name> <argument value>

The **cmdline** package is included in the <*Quartus II directory*>**/common/tcl/packages** directory.

For example, to run a script called **myscript.tcl** with one argument, `Stratix`, type the following command at a system command prompt:

```
quartus_sh -t myscript.tcl Stratix ↵
```

Beginning with version 4.1, the Quartus II software supports the `argv` variable. In previous software versions, script arguments are accessed in the `quartus(args)` global variable.

Refer to "Accessing Command-Line Arguments" on page 3–36 for more information.

Interactive Shell Mode

Running an executable with the `-s` option starts an interactive Tcl shell that displays a `tcl>` prompt. For example, type `quartus_tan -s` ↵ at a system command prompt to open the Classic timing analyzer

executable in interactive shell mode. Commands you type in the Tcl shell are interpreted when you press **Enter**. You can run a Tcl script in the interactive shell with the following command:

```
source <script name> ↵
```

If a command is not recognized by the shell, it is assumed to be an external command and executed with the **exec** command.

Evaluate as Tcl

Running an executable with the `--tcl_eval` option causes the executable to immediately evaluate the remaining command-line arguments as Tcl commands. This can be useful if you want to run simple Tcl commands from other scripting languages.

For example, the following command runs the Tcl command that prints out the commands available in the **project** package.

```
quartus_sh --tcl_eval help -pkg project ↵
```

Using the Quartus II Tcl Console Window

You can run Tcl commands directly in the Quartus II Tcl Console window. On the View menu, click **Utility Windows**. By default, the Tcl Console window is docked in the bottom-right corner of the Quartus II GUI. Everything typed in the Tcl Console is interpreted by the Quartus II Tcl shell.

The **Quartus II Tcl Console** window supports the Tcl API used in the Quartus II software version 3.0 and earlier for backward compatibility with older designs and EDA tools.

Tcl messages appear in the **System** tab (Messages window). Errors and messages written to `stdout` and `stderr` also are shown in the Quartus II Tcl Console window.

Note that you can do limited timing analysis in the Tcl console in the Quartus II GUI. With the **timing_report** package, you can use the **list_path** command to get details on paths listed in the timing report. However, if you want to get information about timing paths that are not listed in the timing report, you must use the **quartus_tan** executable in shell mode or run a script that reports on the paths in which you are interested.

If your design uses the TimeQuest timing Analyzer, you should perform scripted timing analysis in the TimeQuest Tcl console.

As Table 3–2 shows, the Tcl console in the Quartus II GUI does not include support for every package, so you cannot run scripts that use commands in packages that are not supported.

End-to-End Design Flows

You can use Tcl scripts to control all aspects of the design flow, including controlling other software if it includes a scripting interface.

Typically, EDA tools include their own script interpreters that extend core language functionality with tool-specific commands. For example, the Quartus II Tcl interpreter supports all core Tcl commands, and adds numerous commands specific to the Quartus II software. You can include commands in one Tcl script to run another script, which allows you to combine or chain together scripts to control different tools. Because scripts for different tools must be executed with different Tcl interpreters, it is difficult to pass information between the scripts unless one script writes information into a file and another script reads it.

Within the Quartus II software, you can perform many different operations in a design flow (such as synthesis, fitting, and timing analysis) from a single script, making it easy to maintain global state information and pass data between the operations. However, there are some limitations on the operations you can perform in a single script due to the various packages supported by each executable. For example, you cannot write a single script that performs simulation with commands in the **simulator** package while using commands in the **advanced_timing** package; those two packages are not available in the same executable. In a case where you wanted to include Tcl simulation and advanced timing analysis commands, you must write two scripts.

There are no limitations on running flows from any executable. Flows include operations found in the Start section of the Processing menu in the Quartus II GUI, and are also documented with the **execute_flow** Tcl command. If you can make settings in the Quartus II software and run a flow to get your desired result, you can make the same settings and run the same flow in any command-line executable.

To revisit the example with simulation and timing analysis, you could write one script that includes settings that configure a simulation, with settings that configure timing analysis. Then, run the simulation and timing analysis flows with the **execute_flow** command.

Configuring a simulation includes specifying settings such as name and location of the stimulus file, the duration of the simulation, whether to perform glitch detection or not, and more. Configuring timing analysis includes specifying settings such as the required clock frequency, the number of paths to report, and which timing model to use. You can make the settings, then run the flows with the **execute_flow** command, in any Quartus II command-line executable.

Creating Projects & Making Assignments

One benefit of the Tcl scripting API is that it is easy to create a script that makes all the assignments for an existing project. You can use the script at any time to restore your project settings to a known state. From the Project menu, click **Generate Tcl File for Project** to automatically generate a Tcl file with all of your assignments. You can source this file to recreate your project, and you can edit the file to add other commands, such as compiling the design. The file is a good starting point to learn about project management commands and assignment commands.

Refer to "Interactive Shell Mode" on page 3–10 for information about sourcing a script. Scripting information for all Quartus II project settings and assignments is located in the *QSF Reference Manual*.

Example 3–2 shows how to create a project, make assignments, and compile the project. It uses the **fir_filter** tutorial design files.

Example 3–2. Create & Compile a Project

```
load_package flow

# Create the project and overwrite any settings
# files that exist
project_new fir_filter -revision filtref -overwrite
# Set the device, the name of the top-level BDF,
# and the name of the top level entity
set_global_assignment -name FAMILY Cyclone
set_global_assignment -name DEVICE EP1C6F256C6
set_global_assignment -name BDF_FILE filtref.bdf
set_global_assignment -name TOP_LEVEL_ENTITY filtref
# Add other pin assignments here
set_location_assignment -to clk Pin_G1
# Create a base clock and a derived clock
create_base_clock -fmax "100 MHz" -target clk clocka
create_relative_clock -base_clock clocka -divide 2 \
    -offset "500 ps" -target clkx2 clockb
# Create a multicycle assignment of 2 between
# the two clock domains in the design.
set_multicycle_assignment -from clk -to clkx2 2
execute_flow -compile
project_close
```

The assignments created or modified while a project is open are not committed to the Quartus II settings files unless you explicitly call **export_assignments** or **project_close** (unless `-dont_export_assignments` is specified). In some cases, such as when running **execute_flow**, the Quartus II software automatically commits the changes.

HardCopy Device Design

For information about using a scripted design flow for HardCopy II designs, refer to the *Script-Based Design Flow for HardCopy Devices* chapter of the *HardCopy Handbook*. It contains sample scripts and recommendations to make your HardCopy II design flow easy.

A separate chapter in the *HardCopy Handbook* called *Timing Constraints for HardCopy II* also contains information about script-based design for HardCopy II devices, with an emphasis on timing constraints.

EDA Tool Assignments

You can target EDA tools for a project in the Quartus II software in Tcl with the **set_global_assignment** Tcl command. To use the default tool settings for each EDA tool, you need only specify the EDA tool to be used. The EDA interfaces available for the Quartus II software cover design

entry, simulation, timing analysis, and board design tools. More advanced EDA tools such as those for formal verification and resynthesis are supported by their own global assignment.

By default, the EDA interface options are set to <none>. Table 3–6 lists the EDA interface options available in the Quartus II software. Enclose interface assignment options that contain spaces in quotation marks.

Table 3–6. EDA Interface Options in the Quartus II Software (Part 1 of 2)

Option	Acceptable Values
Design Entry (EDA_DESIGN_ENTRY_SYNTHESIS_TOOL)	• Design Architect • Design Compiler • FPGA Compiler • FPGA Compiler II • FPGA Compiler II Altera Edition • FPGA Express • LeonardoSpectrum™ • LeonardoSpectrum-Altera (Level 1) • Synplify • Synplify Pro • ViewDraw • Precision Synthesis • Custom
Simulation (EDA_SIMULATION_TOOL)	• ModelSim (VHDL output from the Quartus II software) • ModelSim (Verilog HDL output from the Quartus II software) • ModelSim-Altera (VHDL output from the Quartus II software) • ModelSim-Altera (Verilog HDL output from the Quartus II software) • SpeedWave • VCS • Verilog-XL • VSS • NC-Verilog (Verilog HDL output from the Quartus II software) • NC-VHDL (VHDL output from the Quartus II software) • Scirocco (VHDL output from the Quartus II software) • Custom Verilog HDL • Custom VHDL
Timing Analysis (EDA_TIMING_ANALYSIS_TOOL)	• PrimeTime (VHDL output from the Quartus II software) • PrimeTime (Verilog HDL output from the Quartus II software) • Stamp (board model) • Custom Verilog HDL • Custom VHDL

Table 3–6. EDA Interface Options in the Quartus II Software (Part 2 of 2)

Option	Acceptable Values
Board level tools (EDA_BOARD_DESIGN_TOOL)	• Signal Integrity (IBIS) • Symbol Generation (ViewDraw)
Formal Verification (EDA_FORMAL_VERIFICATION_TOOL)	• Conformal LEC
Resynthesis (EDA_RESYNTHESIS_TOOL)	• PALACE • Amplify

For example, to generate an NC-Sim Verilog simulation output file, EDA_SIMULATION_TOOL should be set to target NC-Sim Verilog as the desired output, as shown in Example 3–3.

Example 3–3.

```
set_global_assignment -name eda_simulation_tool \
"NcSim (Verilog HDL output from Quartus II)"
```

For information about using third-party simulation tools, refer to volume 3 of the *Quartus II Handbook*.

Example 3–4 shows compilation of the `fir_filter` design files, generating a VHDL Output (**.vho**) file output for NC-Sim Verilog simulation.

Example 3–4. Simple Design with .vho Output

```
# This script works with the quartus_sh executable
# Set the project name to filtref
set project_name filtref

# Open the Project. If it does not already exist, create it
if [catch {project_open $project_name}] {project_new \ $project_name}

# Set Family
set_global_assignment -name family APEX 20KE

# Set Device
set_global_assignment -name device ep20k100eqc208-1

# Optimize for speed
set_global_assignment -name optimization_technique speed

# Turn-on Fastfit fitter option to reduce compile times
set_global_assignment -name fast_fit_compilation on

# Generate a NC-Sim Verilog simulation Netlist
set_global_assignment -name eda_simulation_tool "NcSim\
(Verilog HDL output from Quartus II)"

# Create an FMAX=50MHz assignment called clk1 to pin clk
create_base_clock -fmax 50MHz -target clk clk1

# Create a pin assignment on pin clk
set_location -to clk Pin_134

# Compilation option 1
# Always write the assignments to the constraint files before
# doing a system call. Else, stand-alone files will not pick up
# the assignments
#export_assignments
#qexec quartus_map <project_name>
#qexec quartus_fit <project_name>
#qexec quartus_asm <project_name>
#qexec quartus_tan <project_name>
#qexec quartus_eda <project_name>

# Compilation option 2 (better)
# Using the ::quartus::flow package, and execute_flow command will
# export_assignments automatically and be equivalent to the steps
# outlined in compilation option 1
load_package flow
execute_flow -compile
```

```
# Close Project
project_close
```

Custom options are available to target other EDA tools. For custom EDA configurations, you can change the individual EDA interface options by making additional assignments.

For a complete list of each EDA setting line available, refer to the Quartus II Help.

Using LogicLock Regions

You can use Tcl commands to work with LogicLock™ regions. The following examples show how to export and import LogicLock regions for use in other designs. The examples use the files in the LogicLock tutorial design.

For additional information about the LogicLock design methodology, see the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

To compile a design and export LogicLock regions, follow these steps:

1. Create a project and add assignments.
2. Assign virtual pins.
3. Create a LogicLock region.
4. Assign a design entity to the region.
5. Compile the project.
6. Back-annotate the region.
7. Export the region.

Example 3–5 shows a script that creates a project called **lockmult**, and makes all the required assignments to compile the project. Next, the script compiles the project, back-annotates the design, and exports the LogicLock region. The script uses a procedure called **assign_virtual_pins**, which is described after the example. Use the **quartus_cdb** executable to run this script.

Example 3–5. LogicLock Export Script

```
load_package flow
load_package logiclock
load_package backannotate

project_new lockmult -overwrite
set_global_assignment -name BDF_FILE pipemult.bdf
set_global_assignment -name FAMILY Cyclone
set_global_assignment -name DEVICE EP1C6F256C6
set_global_assignment -name TOP_LEVEL_ENTITY pipemult

# These two assignments cause the Quartus II software
# to generate a VQM file for the logic in the LogicLock
# region. The VQM file is imported into the top-level
# design.
set_global_assignment -name \
   LOGICLOCK_INCREMENTAL_COMPILE_FILE pipemult.vqm
set_global_assignment -name \
   LOGICLOCK_INCREMENTAL_COMPILE_ASSIGNMENT ON

create_base_clock -fmax 200MHz -target clk clk_200
assign_virtual_pins { clk }
#Prepare LogicLock data structures before
#LogicLock-related commands.
initialize_logiclock

# Create a region named lockmult and assign pipemult
# to it.
# The region is auto-sized and floating.
set_logiclock -region lockmult -auto_size true \
-floating true
set_logiclock_contents -region lockmult -to pipemult
execute_flow -compile

# Back annotate the LogicLock Region and export a QSF
logiclock_back_annotate -region lockmult -lock
logiclock_export -file_name pipemult.qsf


uninitialize_logiclock
project_close
```

The **assign_virtual_pins** command is a procedure that makes virtual pin assignments to all bottom-level design pins, except for signals specified as arguments to the procedure. The procedure is defined in Example 3–6.

Example 3–6. assign_virtual_pins Procedure

```
proc assign_virtual_pins { skips } {

   # Analysis and elaboration must be run first to get the pin names
   execute_flow -analysis_and_elaboration

   # Get all pin names as a collection.

   set name_ids [get_names -filter * -node_type pin]
   foreach_in_collection name_id $name_ids {
      # Get the hierarchical path name of the pin.
      set hname [get_name_info -info full_path $name_id]
      #Skip the virtual pin assignment if the
      #pin is in the list of signals to be skipped.
      if {[lsearch -exact $skips $hname] == -1} {
         post_message "Setting VIRTUAL_PIN on $hname"
         set_instance_assignment -to $hname -name VIRTUAL_PIN ON
      } else {
         post_message "Skipping VIRTUAL_PIN for $hname"
      }
   }
}
```

When the script runs, it generates a netlist file named **pipemult.vqm**, and a Quartus II Settings File named **pipemult.qsf**, which contains the back-annotated assignments. You can then import the LogicLock region in another design. This example uses the top-level design in the **topmult** directory.

To import it four times in the top-level LogicLock tutorial design, follow these steps:

1. Create the top-level project.
2. Add assignments.
3. Elaborate the design.
4. Import the LogicLock constraints.
5. Compile the project.

Example 3–7 shows a script that demonstrates the previous steps.

Example 3–7. LogicLock Import Script

```
load_package flow
load_package logiclock

project_new topmult -overwrite
set_global_assignment -name BDF_FILE topmult.bdf
set_global_assignment -name VQM_FILE pipemult.vqm
set_global_assignment -name FAMILY Cyclone
set_global_assignment -name DEVICE EP1C6F256C6
create_base_clock -fmax 200MHz -target clk clk_200

# The LogicLock region will be used four times
# in the top-level design. These assignments
# specify that the back-annotated assignments in
# the QSF will be applied to the four entities
# in the top-level design.
set_instance_assignment -name LL_IMPORT_FILE pipemult.qsf \
    -to pipemult:inst
set_instance_assignment -name LL_IMPORT_FILE pipemult.qsf \
    -to pipemult:inst1
set_instance_assignment -name LL_IMPORT_FILE pipemult.qsf \
    -to pipemult:inst2
set_instance_assignment -name LL_IMPORT_FILE pipemult.qsf \
    -to pipemult:inst3

execute_flow -analysis_and_elaboration
initialize_logiclock
logiclock_import
uninitialize_logiclock
execute_flow -compile
project_close
```

For additional information about the LogicLock design methodology, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

Compiling Designs

You can run the Quartus II command-line executables from Tcl scripts. Use the included **flow** package to run various Quartus II compilation flows, or run each executable directly.

The flow Package

The **flow** package includes two commands for running Quartus II command-line executables, either individually or together in standard compilation sequence. The **execute_module** command allows you to run

an individual Quartus II command-line executable. The **execute_flow** command allows you to run some or all of the modules in commonly-used combinations.

Altera recommends using the **flow** package instead of using system calls to run compiler executables.

Another way to run a Quartus II command-line executable from the Tcl environment is by using the **qexec** Tcl command, a Quartus II implementation of the Tcl **exec** command. For example, to run the Quartus II technology mapper on a given project, type:

```
qexec "quartus_map <project_name>" ↵
```

When you use the **qexec** command to compile a design, assignments made in the Tcl script (or from the Tcl shell) are not exported to the project database and settings file before compilation. Use the **export_assignments** command or compile the project with commands in the **flow** package to ensure assignments are exported to the project database and settings file.

You should use the **qexec** command to make system calls.

You can also run executables directly in a Tcl shell, using the same syntax as at the system command prompt. For example, to run the Quartus II technology mapper on a given project, type the following at the Tcl shell prompt:

```
quartus_map <project_name> ↵
```

Reporting

Once compilation finishes, it is sometimes necessary to extract information from the report to evaluate the results. For example, you may need to know how many device resources the design uses, or whether it meets your performance requirements. The Quartus II Tcl API provides easy access to report data so you don't have to write scripts to parse the text report files.

Use the commands that access report data one row at a time, or one cell at a time. If you know the exact cell or cells you want to access, use the **get_report_panel_data** command and specify the row and column names (or *x* and *y* coordinates) and the name of the appropriate report panel. You may often search for data in a report panel. To do this, use a loop that reads the report one row at a time with the **get_report_panel_row** command.

Column headings in report panels are in row 0. If you use a loop that reads the report one row at a time, you can start with row 1 to skip the row with column headings. The **get_number_of_rows** command returns the number of rows in the report panel, including the column heading row. Because the number of rows includes the column heading row, your loop should continue as long as the loop index is less than the number of rows, as illustrated in the following example.

Report panels are hierarchically arranged, and each level of hierarchy is denoted by the string "||" in the panel name. For example, the name of the Fitter Settings report panel is **Fitter||Fitter Settings** because it is in the Fitter folder. Panels at the highest hierarchy level do not use the "||" string. For example, the Flow Settings report panel is named **Flow Settings**.

Example 3–8 shows code that prints a list of all report panel names in your project:.

Example 3–8. Print All Report Panel Names

```
set panel_names [get_report_panel_names]
foreach panel_name $panel_names {
   post_message "$panel_name"
}
```

The following example prints the number of failing paths in each clock domain in your design. It uses a loop to access each row of the **Timing Analyzer Summary** report panel. Clock domains are listed in the column named **Type** with the format `Clock Setup:'<clock name>'`. Other summary information is listed in the **Type** column as well. If the **Type** column matches the pattern "`Clock Setup*`", the script prints the number of failing paths listed in the column named **Failed Paths**.

Example 3–9. Print Number of Failing Paths per Clock

```
load_package report
project_open my-project
load_report
set report_panel_name "Timing Analyzer||Timing Analyzer Summary"
set num_rows [get_number_of_rows -name $report_panel_name]

# Get the column indices for the Type and Failed Paths columns
set type_column [get_report_panel_column_index -name \
    $report_panel_name "Type"]
set failed_paths_column [get_report_panel_column_index -name \
    $report_panel_name "Failed Paths"]

# Go through each line in the report panel
for {set i 1} {$i < $num_rows} {incr i} {

    # Get the row of data, then the type of summary
    # information in the row, and the number of failed paths
    set report_row [get_report_panel_row -name \
    $report_panel_name -row $i]
    set row_type [lindex $report_row $type_column]
    set failed_paths [lindex $report_row $failed_paths_column]
    if { [string match "Clock Setup*" $row_type] } {
        puts "$row_type has $failed_paths failing paths"
    }
}
unload_report
```

Creating CSV Files for Excel

The Microsoft Excel software is sometimes used to view or manipulate timing analysis results. You can create a CSV file to import into Excel with data from any Quartus II report. This example shows a simple way to create a CSV file with data from a timing analysis panel in the report. You could modify the script to use command-line arguments to pass in the name of the project, report panel, and output file to use.

Example 3–10. Create CSV Files from Reports

```
load_package report
project_open my-project

load_report

# This is the name of the report panel to save as a CSV file
set panel_name "Timing Analyzer||Clock Setup: 'clk'"
set csv_file "output.csv"

set fh [open $csv_file w]
set num_rows [get_number_of_rows -name $panel_name]

# Go through all the rows in the report file, including the
# row with headings, and write out the comma-separated data
for { set i 0 } { $i < $num_rows } { incr i } {
    set row_data [get_report_panel_row -name $panel_name \
        -row $i]
    puts $fh [join $row_data ","]
}

close $fh
unload_report
```

Short Option Names

Beginning with version 6.0 of the Quartus II software, you can use short versions of command options, as long as they distinguish between the command's options. For example, the **project_open** command supports two options: `-current_revision` and `-revision`. You can use any of the following shortened versions of the `-revision` option: `-r`, `-re`, `-rev`, `-revi`, `-revis`, and `-revisio`. You can use an option as short as `-r` because no other option starts with the same letters as revision. However, the **report_timing** command includes the options `-recovery` and `-removal`. You cannot use `-r` or `-re` to shorten either of those options, because they do not uniquely distinguish between either option. You could use `-rec` or `-rem`.

Timing Analysis

The Quartus II software includes comprehensive Tcl APIs for both the Classic and TimeQuest analyzers. This section includes simple and advanced script examples for the Classic analyzer and introductory scripting information about the TimeQuest Tcl API.

Classic Timing Analysis

The following example script uses the **quartus_tan** executable to perform a timing analysis on the **fir_filter** tutorial design.

The **fir_filter** design is a two-clock design that requires a base clock and a relative clock relationship for timing analysis. This script first does an analysis of the two-clock relationship and checks for t_{SU} slack between `clk` and `clkx2`. The first pass of timing analysis discovers a negative slack for one of the clocks. The second part of the script adds a multicycle assignment from `clk` to `clkx2` and re-analyzes the design as a multi-clock, multicycle design.

The script does not recompile the design with the new timing assignments, and timing-driven compilation is not used in the synthesis and placement of this design. New timing assignments are added only for the timing analyzer to analyze the design with the **create_timing_netlist** and **report_timing** Tcl commands.

You must compile the project before running the script example shown in Example 3–11.

Example 3–11. Classic Timing Analysis

```
# This Tcl file is to be used with quartus_tan.exe
# This Tcl file will do the Quartus II tutorial fir_filter design
# timing analysis portion by making a global timing assignment and
# creating multi-clock assignments and run timing analysis
# for a multi-clock, multi-cycle design
# set the project_name to fir_filter
# set the revision_name to filtref
set project_name fir_filter
set revision_name filtref

# open the project
# project_name is the project name
project_open -revision $revision_name $project_name;

# Doing TAN tutorial steps this section re-runs the timing
# analysis module with multi-clock and multi-cycle settings
#------ Make timing assignments ------#

#Specifying a global FMAX requirement (tan tutorial)
set_global_assignment -name FMAX_REQUIREMENT 45.0MHz
set_global_assignment -name CUT_OFF_IO_PIN_FEEDBACK ON

# create a base reference clock "clocka" and specifies the
# following:
#   BASED_ON_CLOCK_SETTINGS = clocka;
#   INCLUDE_EXTERNAL_PIN_DELAYS_IN_FMAX_CALCULATIONS = OFF;
#   FMAX_REQUIREMENT = 50MHZ;
#   DUTY_CYCLE = 50;
# Assigns the reference clocka to the pin "clk"
create_base_clock -fmax 50MHZ -duty_cycle 50 clocka -target clk
```

```
# creates a relative clock "clockb" based on reference clock
# "clocka" with the following settings:
#   BASED_ON_CLOCK_SETTINGS = clocka;
#   MULTIPLY_BASE_CLOCK_PERIOD_BY = 1;
#   DIVIDE_BASE_CLOCK_PERIOD_BY = 2;clock period is half the base clk
#   DUTY_CYCLE = 50;
#   OFFSET_FROM_BASE_CLOCK = 500ps;The offset is .5 ns (or 500 ps)
#   INVERT_BASE_CLOCK = OFF;
# Assigns the reference clock to pin "clkx2"
create_relative_clock -base_clock clocka -duty_cycle 50\
-divide 2 -offset 500ps -target clkx2 clockb

# create new timing netlist based on new timing settings
create_timing_netlist

# does an analysis for clkx2
# Limits path listing to 1 path
# Does clock setup analysis for clkx2
report_timing -npaths 1 -clock_setup -file setup_multiclock.tao

# The output file will show a negative slack for clkx2 when only
# specifying a multi-clock design. The negative slack was created
# by the 500 ps offset from the base clock

# removes old timing netlist to allow for creation of a new timing
# netlist for analysis by report_timing
delete_timing_netlist

# adding a multi-cycle setting corrects the negative slack by adding a
# multicycle assignment to clkx2 to allow for more set-up time
set_multicycle_assignment 2 -from clk -to clkx2

# create a new timing netlist based on additional timing
# assignments create_timing_netlist

# outputs the result to a file for clkx2 only
report_timing -npaths 1 -clock_setup -clock_filter clkx2 \
 -file clkx2_setup_multicycle.tao
# The new output file will show a positive slack for the clkx2
project_close
```

Advanced Classic Timing Analysis

There may be times when the commands available for timing analysis reporting do not provide access to specific data you need. The **advanced_timing** package provides commands to access the data structures representing the timing netlist for your design. These commands provide low-level details about timing delays, node fan-in and fan-out, and timing data. Writing procedures to traverse the timing netlist and extract information gives you the most control to get exactly the data you need.

The timing netlist is represented with a graph, which is a collection of nodes and edges. Nodes represent elements in your design such as registers, combinational nodes, pins, and clocks. Edges connect the nodes and represent the connections between the logic in your design. Edges and nodes have unique positive integer IDs that identify them in the timing netlist. All the commands for getting information about the timing netlist use node and edge IDs instead of text-based names.

As an example of how to use the **advanced_timing** package, Example 3–12 shows one way to show the register-to-pin delays from all registers that drive the pins of an output bus. Specify the name of an output bus (for example, `address`), and the script prints out the names of all registers driving the pins of the bus and the delays from registers to pins.

Example 3–12. Report Register to Pin Delays

```
load_package advanced_timing
package require cmdline

# This procedure returns a list of IDs for pins with names
# that match the bus name passed in
proc find { bus_name } {

    set to_return [list]

    foreach_in_collection node_id [get_timing_nodes -type pin] {
        set node_name [get_timing_node_info -info name $node_id]
        if { [string match $bus_name* $node_name] } {
            lappend to_return $node_id
        }
    }
    return $to_return
}

# Required arguments for the script are the name of the project and
# revision, as well as the name of the bus to analyze
set options {\
    { "project.arg" "" "Project name" } \
    { "revision.arg" "" "Revision name" } \
    { "bus_name.arg" "" "Name of the bus to get timing data for" } \
}
array set opts [::cmdline::getoptions quartus(args) $options]

project_open $opts(project) -revision $opts(revision)

# The timing netlist must be created before accessing it.
create_timing_netlist

# This creates a data structure with additional timing data
create_p2p_delays

# Walk through each pin in the specified bus
foreach pin_id [find $opts(bus_name)] {
    set pin_name [get_timing_node_info -info name $pin_id]
```

```
    puts "$pin_name source registers and delays"
    # The get_delays_from_keepers command returns a list of all the
    # non-combinational nodes in the design that fan in to the
    # specified timing node, with the associated delays.
    foreach data [get_delays_from_keepers $pin_id] {
        set source_node [lindex $data 0]
        set max_delay [lindex $data 1]
        set source_node_name \
[get_timing_node_info -info name $source_node]
        puts " $source_node_name $max_delay"
    }
}
project_close
```

Type the command shown in Example 3–13 at a system command prompt to run this script.

Example 3–13.

```
quartus_tan -t script.tcl -project fir_filter
    -revision filtref -bus_name yn_out ↵
```

TimeQuest Timing Analysis

The TimeQuest timing analyzer includes support for SDC commands in the **::quartus::sdc** package.

Refer to the *TimeQuest Timing Analysis* chapter of the *Quartus II Handbook* for detailed information about how to perform timing analysis with the TimeQuest timing analyzer.

TimeQuest Scripting

In versions of the Quartus II software before 6.0, the **::quartus::project** Tcl package contained the following SDC-like commands for making timing assignments:

- **create_base_clock**
- **create_relative_clock**
- **get_clocks**
- **set_clock_latency**
- **set_clock_uncertainty**
- **set_input_delay**
- **set_multicycle_assignment**
- **set_output_delay**
- **set_timing_cut_assignment**

These commands are not SDC-compliant. Beginning with version 6.0, these commands are in a new package named **::quartus::timing_assignment**. To ensure backwards compatibility with existing Tcl scripts, the **::quartus::timing_assignment** package is loaded by default in the following executables:

- **quartus**
- **quartus_sh**
- **quartus_cdb**
- **quartus_sim**
- **quartus_stp**
- **quartus_tan**

The **::quartus::timing_assignment** package is not loaded by default in the **quartus_sta** executable. The **::quartus::sdc** Tcl package includes SDC-compliant versions of the commands listed above. The package is available only in the **quartus_sta** executable, and it is loaded by default.

Automating Script Execution

Beginning with version 4.0 of the Quartus II software, you can configure scripts to run automatically at various points during compilation. Use this capability to automatically run scripts that perform custom reporting, make specific assignments, and perform many other tasks.

The following three global assignments control when a script is run automatically:

- `PRE_FLOW_SCRIPT_FILE` —before a flow starts
- `POST_MODULE_SCRIPT_FILE` —after a module finishes
- `POST_FLOW_SCRIPT_FILE` —after a flow finishes

The `POST_FLOW_SCRIPT_FILE` and `POST_MODULE_SCRIPT_FILE` assignments are supported beginning in version 4.0, and the `PRE_FLOW_SCRIPT_FILE` assignment is supported beginning in version 4.1.

A module is a Quartus II executable that performs one step in a flow. For example, two modules are Analysis & Synthesis (**quartus_map**) and timing analysis (**quartus_tan**).

A flow is a series of modules that the Quartus II software runs with predefined options. For example, compiling a design is a flow that typically consists of the following steps (performed by the indicated module):

1. Analysis and synthesis (**quartus_map**)
2. Fitter (**quartus_fit**)

3. Assembler (**quartus_asm**)

4. Timing Analyzer (**quartus_tan**)

Other flows are described in the help for the **execute_flow** Tcl command. In addition, many commands in the Processing menu of the Quartus II GUI correspond to this design flow.

Making the Assignment

To make an assignment to automatically run a script, add an assignment with the following form to your project's Quartus II Settings File:

```
set_global_assignment -name <assignment name> \
    <executable>:<script name>
```

The assignment name is one of the following:

- `PRE_FLOW_SCRIPT_FILE`
- `POST_MODULE_SCRIPT_FILE`
- `POST_FLOW_SCRIPT_FILE`

The executable is the name of a Quartus II command-line executable that includes a Tcl interpreter.

- **quartus_cdb**
- **quartus_sh**
- **quartus_sim**
- **quartus_sta**
- **quartus_stp**
- **quartus_tan**

The script name is the name of your Tcl script.

Script Execution

The Quartus II software runs the scripts as shown Example 3–14.

Example 3–14.

```
<executable> -t <script name> <flow or module name> <project name> <revision name>
```

The first argument passed in the `argv` variable (or `quartus(args)` variable) is the name of the flow or module being executed, depending on the assignment you use. The second argument is the name of the project, and the third argument is the name of the revision.

When you use the POST_MODULE_SCRIPT_FILE assignment, the specified script is automatically run after every executable in a flow. You can use a string comparison with the module name (the first argument passed in to the script) to isolate script processing to certain modules.

Execution Example

Example 3–15 illustrates how automatic script execution works in a complete flow, assuming you have a project called **top** with a current revision called **rev_1**, and you have the following assignments in the Quartus II Settings File for your project.

Example 3–15.

```
set_global_assignment -name PRE_FLOW_SCRIPT_FILE quartus_sh:first.tcl
set_global_assignment -name POST_MODULE_SCRIPT_FILE quartus_sh:next.tcl
set_global_assignment -name POST_FLOW_SCRIPT_FILE quartus_sh:last.tcl
```

When you compile your project, the PRE_FLOW_SCRIPT_FILE assignment causes the following command to be run before compilation begins:

```
quartus_sh -t first.tcl compile top rev_1
```

Next, the Quartus II software starts compilation with analysis and synthesis, performed by the **quartus_map** executable. After the analysis and synthesis finishes, the POST_MODULE_SCRIPT_FILE assignment causes the following command to be run:

```
quartus_sh -t next.tcl quartus_map top rev_1
```

Then, the Quartus II software continues compilation with the Fitter, performed by the **quartus_fit** executable. After the Fitter finishes, the POST_MODULE_SCRIPT_FILE assignment runs the following command:

```
quartus_sh -t next.tcl quartus_fit top rev_1
```

Corresponding commands are run after the other stages of the compilation. Finally, after the compilation is over, the POST_FLOW_SCRIPT_FILE assignment runs the following command:

```
quartus_sh -t last.tcl compile top rev_1
```

Controlling Processing

The POST_MODULE_SCRIPT_FILE assignment causes a script to run after every module. Because the same script is run after every module, you may need to include some conditional statements that restrict processing in your script to certain modules.

For example, if you want a script to run only after timing analysis, you should include a conditional test like the one shown in Example 3–16. It checks the flow or module name passed as the first argument to the script and executes code when the module is quartus_tan.

Example 3–16. Restrict Processing to a Single Module

```
set module [lindex $quartus(args) 0]

if [string match "quartus_tan" $module] {

    # Include commands here that are run
    # after timing analysis
    # Use the post-message command to display
    # messages
    post_message "Running after timing analysis"
}
```

Displaying Messages

Because of the way the Quartus II software runs the scripts automatically, you must use the **post_message** command to display messages, instead of the **puts** command. This requirement applies only to scripts that are run by the three assignments listed in "Automating Script Execution" on page 3–30.

Refer to "Using the post_message Command" on page 3–35 for more information about this command.

Other Scripting Features

The Quartus II Tcl API includes other general-purpose commands and features described in this section.

Natural Bus Naming

Beginning with version 4.2, the Quartus II software supports natural bus naming. Natural bus naming means that square brackets used to specify bus indexes in hardware description languages do not have to be escaped to prevent Tcl from interpreting them as commands. For example, one

signal in a bus named address can be identified as `address[0]` instead of `address\[0\]`. You can take advantage of natural bus naming when making assignments, as in Example 3–17.

Example 3–17. Natural Bus Naming

```
set_location_assignment -to address[10] Pin_M20
```

The Quartus II software defaults to natural bus naming. You can turn off natural bus naming with the **disable_natural_bus_naming** command. For more information about natural bus naming, type `enable_natural_bus_naming -h` ↵ at a Quartus II Tcl prompt.

Using Collection Commands

Some Quartus II Tcl functions return very large sets of data that would be inefficient as Tcl lists. These data structures are referred to as collections and the Quartus II Tcl API uses a collection ID to access the collection. There are two Quartus II Tcl commands for working with collections, **foreach_in_collection** and **get_collection_size**. Use the **set** command to assign a collection ID to a variable.

For information about which Quartus II Tcl commands return collection IDs, see the Quartus II Help and search for the **foreach_in_collection** command.

The foreach_in_collection Command

The **foreach_in_collection** command is similar to the **foreach** Tcl command. Use it to iterate through all elements in a collection. Example 3–18 prints all instance assignments in an open project.

Example 3–18. Using Collection Commands

```
set all_instance_assignments [get_all_instance_assignments -name *]
foreach_in_collection asgn $all_instance_assignments {
    # Information about each assignment is
    # returned in a list. For information
    # about the list elements, refer to Help
    # for the get-all-instance-assignments command.
    set to [lindex $asgn 2]
    set name [lindex $asgn 3]
    set value [lindex $asgn 4]
    puts "Assignment to $to: $name = $value"
}
```

The get_collection_size Command

Use the **get_collection_size** command to get the number of elements in a collection. Example 3–19 prints the number of global assignments in an open project:

Example 3–19. get_collection_size Command

```
set all_global_assignments [get_all_global_assignments -name *]
set num_global_assignments [get_collection_size $all_global_assignments]
puts "There are $num_global_assignments global assignments in your project"
```

Using the post_message Command

To print messages that are formatted like Quartus II software messages, use the **post_message** command. Messages printed by the **post_message** command appear in the **System** tab of the Messages window in the Quartus II GUI, and are written to standard at when scripts are run. Arguments for the **post_message** command include an optional message type and a required message string.

The message type can be one of the following:

- info (default)
- extra_info
- warning
- critical_warning
- error

If you do not specify a type, Quartus II software defaults to `info`.

When you are using the Quartus II software in Windows, you can color code messages displayed at the system command prompt with the **post_message** command. Add the following line to your **quartus2.ini** file:

```
DISPLAY_COMMAND_LINE_MESSAGES_IN_COLOR = on
```

Example 3–20 shows how to use the **post_message** command.

Example 3–20. post_message command

```
post_message -type warning "Design has gated clocks"
```

Accessing Command-Line Arguments

Many Tcl scripts are designed to accept command-line arguments, such as the name of a project or revision. The global variable `quartus(args)` is a list of the arguments typed on the command-line following the name of the Tcl script. Example 3–21 shows code that prints all of the arguments in the `quartus(args)` variable.

Example 3–21. Simple Command-Line Argument Access

```
set i 0
foreach arg $quartus(args) {
   puts "The value at index $i is $arg"
   incr i
}
```

If you copy the script in the previous example to a file named **print_args.tcl**, it displays the following output when you type the command shown in Example 3–22 at a command prompt.

Example 3–22. Passing Command-Line Arguments to Scripts

```
quartus_sh -t print_args.tcl my_project 100MHz ↵
The value at index 0 is <my_project>
The value at index 1 is 100MHz
```

Beginning with version 4.1, the Quartus II software supports the Tcl variables `argv`, `argc`, and `argv0` for command-line argument access. Table 3–7 shows equivalent information for earlier versions of the software.

Table 3–7. Quartus II Support for Tcl Variables

Beginning with Version 4.1	Equivalent Support in Previous Software Versions
argc	`llength $quartus(args)`
argv	`quartus(args)`
argv0	`info nameofexecutable`

Using the cmdline Package

You can use the **cmdline** package included with the Quartus II software for more robust and self-documenting command-line argument passing. The **cmdline** package supports command-line arguments with the form *-<option> <value>*.

Example 3–23 uses the **cmdline** package:

Example 3–23. cmdline Package

```
package require cmdline
variable ::argv0 $::quartus(args)
set options {\
   { "project.arg" "" "Project name" } \
   { "frequency.arg" ""  "Frequency" } \
}
set usage "You need to specify options and values"

array set optshash [::cmdline::getoptions ::argv $options $usage]
puts "The project name is $optshash(project)"
puts "The frequency is $optshash(frequency)"
```

If you save those commands in a Tcl script called **print_cmd_args.tcl** you see the following output when you type the command shown in Example 3–24 at a command prompt:

Example 3–24. Passing Command-Line Arguments for Scripts

```
quartus_sh -t print_cmd_args.tcl -project my_project -frequency 100MHz ↵
The project name is <my_project>
The frequency is 100MHz
```

Virtually all Quartus II Tcl scripts must open a project. Example 3–25 opens a project, and you can optionally specify a revision name. The example checks whether the specified project exists. If it does, the example opens the current revision, or the revision you specify.

Example 3–25. Full-Featured Method to Open Projects

```
package require cmdline
variable ::argv0 $::quartus(args)
set options { \
{ "project.arg" "" "Project Name" } \
{ "revision.arg" "" "Revision Name" } \
}
array set optshash [::cmdline::getoptions ::argv0 $options]

# Ensure the project exists before trying to open it
if {[project_exists $optshash(project)]} {

    if {[string equal "" $optshash(revision)]} {

        # There is no revision name specified, so default
        # to the current revision
        project_open $optshash(project) -current_revision
    } else {

        # There is a revision name specified, so open the
        # project with that revision
        project_open $optshash(project) -revision \
            $optshash(revision)
    }
} else {
    puts "Project $optshash(project) does not exist"
    exit 1
}
# The rest of your script goes here
```

If you do not require this flexibility or error checking, you can use just the **project_open** command, as shown in Example 3–26.

Example 3–26. Simple Method to Open Projects

```
set proj_name [lindex $argv 0]
project_open $proj_name
```

For more information about the **cmdline** package, refer to the documentation for the package at <*Quartus II installation directory*> **/common/tcl/packages**.

Using the Quartus II Tcl Shell in Interactive Mode

This section presents an example of using the **quartus_sh** interactive shell to make some project assignments and compile the finite impulse response (FIR) filter tutorial project. This example assumes that you already have the FIR filter tutorial design files in a project directory.

To begin, run the interactive Tcl shell. The command and initial output are shown in Example 3–27.

Example 3–27. Interactive Tcl Shell

```
tcl> quartus_sh -s
tcl> Info: ************************************************************************
Info: Running Quartus II Shell
    Info: Version 6.0 Internal Build 170 03/29/2006 SJ Full Version
    Info: Copyright (C) 1991-2006 Altera Corporation. All rights reserved.
    Info: Your use of Altera Corporation's design tools, logic functions
    Info: and other software and tools, and its AMPP partner logic
    Info: functions, and any output files any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Altera Program License
    Info: Subscription Agreement, Altera MegaCore Function License
    Info: Agreement, or other applicable license agreement, including,
    Info: without limitation, that your use is for the sole purpose of
    Info: programming logic devices manufactured by Altera and sold by
    Info: Altera or its authorized distributors.  Please refer to the
    Info: applicable agreement for further details.
    Info: Processing started: Tue Apr 04 12:24:13 2006
Info: ************************************************************************
Info: The Quartus II Shell supports all TCL commands in addition
Info: to Quartus II Tcl commands. All unrecognized commands are
Info: assumed to be external and are run using Tcl's "exec"
Info: command.
Info: - Type "exit" to exit.
Info: - Type "help" to view a list of Quartus II Tcl packages.
Info: - Type "help <package name>" to view a list of Tcl commands
Info:   available for the specified Quartus II Tcl package.
Info: - Type "help -tcl" to get an overview on Quartus II Tcl usages.
Info: ************************************************************************

tcl>
```

Create a new project called **fir_filter**, with a revision called **filtref** by typing the following command at a Tcl prompt:

```
project_new -revision filtref fir_filter ↵
```

If the project file and project name are the same, the Quartus II software gives the revision the same name as the project.

Because the revision named **filtref** matches the top-level file, all design files are automatically picked up from the hierarchy tree.

Next, set a global assignment for the device with the following command:

```
set_global_assignment -name family Cyclone ↵
```

To learn more about assignment names that you can use with the `-name` option, refer to the Quartus II Help.

For assignment values that contain spaces, the value should be enclosed in quotation marks.

To quickly compile a design, use the `::quartus::flow` package, which properly exports the new project assignments and compiles the design using the proper sequence of the command-line executables. First, load the package:

```
load_package flow ↵
```

It returns the following:

```
1.0
```

For additional help on the `::quartus::flow` package, view the command-line help at the Tcl prompt by typing:

```
help -pkg  ::quartus::flow ↵
```

Example 3–28 shows an alternative command and the resulting output:

Example 3–28. Help Output

```
tcl> help -pkg flow
------------------------------------------------------------------
-------------------------
Tcl Package and Version:
-------------------------
::quartus::flow 1.0
------------
Description:
------------
        This package contains the set of Tcl functions
        for running flows or command-line executables.
-------------
Tcl Commands:
-------------
        execute_flow
        execute_module
------------------------------------------------------------------
```

This help display gives information about the flow package and the commands that are available with the package.To learn about the options available for the **execute_flow** Tcl command, type the following command at a Tcl prompt:

```
execute_flow -h ↵
```

To view additional information and example usage type the following command at a Tcl prompt:

```
execute_flow -long_help ↵
```

or

```
help -cmd execute_flow ↵
```

To perform a full compilation of the FIR filter design, use the `execute_flow` command with the `-compile` option, as shown in Example 3–29:

Example 3–29.

```
tcl> execute_flow -compile ↵
Info:*******************************************************
Info: Running Quartus II Analysis & Synthesis
Info: Version 6.0 SJ Full Version
Info: Processing started: Tues Apr 04 09:30:47 2006
Info: Command: quartus_map --import_settings_files=on --
export_settings_files=of fir_filter -c filtref
.
.
.
Info: Writing report file filtref.tan.rpt
tcl>
```

This script compiles the FIR filter tutorial project, exporting the project assignments and running **quartus_map**, **quartus_fit**, **quartus_asm,** and **quartus_tan**. This sequence of events is the same as selecting **Start Compilation** from the Processing menu in the Quartus II GUI.

When you are finished with a project, close it using the **project_close** command as shown in Example 3–30.

Example 3–30.

```
project_close ↵
```

Then, to exit the interactive Tcl shell, type `exit ↵` at a Tcl prompt.

Quartus II Legacy Tcl Support

Beginning with the Quartus II software version 3.0, command-line executables do not support the Tcl commands used in previous versions of the Quartus II software. These commands are supported in the GUI with the Quartus II Tcl console or by using the **quartus_cmd** executable at the system command prompt. If you source Tcl scripts developed for an earlier version of the Quartus II software using either of these methods, the project assignments are ported to the project database and settings file. You can then use the command-line executables to process the resulting project. This may be necessary if you create a Tcl file using EDA tools that do not generate Tcl scripts for the most recent version of the Quartus II software.

You should create all new projects and Tcl scripts with the latest version of the Quartus II Tcl API.

Tcl Scripting Basics

The core Tcl commands support variables, control structures, and procedures. Additionally, there are commands for accessing the file system and network sockets, and running other programs. You can create platform-independent graphical interfaces with the Tk widget set.

Tcl commands are executed immediately as they are typed in an interactive Tcl shell. You can also create scripts (including this chapter's examples) as files and run them with a Tcl interpreter. A Tcl script does not need any special headers.

To start an interactive Tcl interpreter, type `quartus_sh -s` ↵ at a command prompt. The commands you type are executed immediately at the interpreter prompt. If you save a series of Tcl commands in a file, you can run it with a Tcl interpreter. To run a script named **myscript.tcl**, type `quartus_sh -t myscript.tcl` ↵ at a command prompt.

Hello World Example

The following shows the basic "Hello world" example in Tcl:

```
puts "Hello world"
```

Use double quotation marks to group the words `hello` and `world` as one argument. Double quotation marks allow substitutions to occur in the group. Substitutions can be simple variable substitutions, or the result of running a nested command, described in "Substitutions" on page 3–43. Use curly braces { } for grouping when you want to prevent substitutions.

Variables

Use the **set** command to assign a value to a variable. You do not have to declare a variable before using it. Tcl variable names are case-sensitive. Example 3–31 assigns the value `1` to the variable named `a`.

Example 3–31. Assigning Variables

```
set a 1
```

To access the contents of a variable, use a dollar sign before the variable name. Example 3–32 prints `"Hello world"` in a different way.

Example 3–32. Accessing Variables

```
set a Hello
set b world
puts "$a $b"
```

Substitutions

Tcl performs three types of substitution:

- Variable value substitution
- Nested command substitution
- Backslash substitution

Variable Value Substitution

Variable value substitution, as shown in Example 3–32, refers to accessing the value stored in a variable by using a dollar sign ("$") before the variable name.

Nested Command Substitution

Nested command substitution refers to how the Tcl interpreter evaluates Tcl code in square brackets. The Tcl interpreter evaluates nested commands, starting with the innermost nested command, and commands nested at the same level from left to right. Each nested command result is substituted in the outer command. Example 3–33 sets `a` to the length of the string `foo`:

Example 3–33. Command Substitution

```
set a [string length foo]
```

Backlash Substitution

Backslash substitution allows you to quote reserved characters in Tcl, such as dollar signs ("$") and braces ("[ ]"). You can also specify other special ASCII characters like tabs and new lines with backslash substitutions. The backslash character is the Tcl line continuation character, used when a Tcl command wraps to more than one line. Example 3–34 shows how to use the backslash character for line continuation:

Example 3–34. Backslash Substitution

```
set this_is_a_long_variable_name [string length "Hello \
    world."]
```

Arithmetic

Use the **expr** command to perform arithmetic calculations. Using curly braces ("{ }") to group the arguments of this command makes arithmetic calculations more efficient and preserves numeric precision. Example 3–35 sets `b` to the sum of the value in the variable `a` and the square root of `2`:

Example 3–35. Arithmetic with the expr Command

```
set a 5
set b [expr { $a + sqrt(2) }]
```

Tcl also supports boolean operators such as `&&` (AND), `||` (OR), `!` (NOT), and comparison operators such as `<` (less than), `>` (greater than), and `==` (equal to).

Lists

A Tcl list is a series of values. Supported list operations include creating lists, appending lists, extracting list elements, computing the length of a list, sorting a list, and more. Example 3–36 sets `a` to a list with three numbers in it:

Example 3–36. Creating Simple Lists

```
set a { 1 2 3 }
```

You can use the **lindex** command to extract information at a specific index in a list. Indexes are zero-based. You can use the index `end` to specify the last element in the list, or the index `end-<n>` to count from the end of the list. Example 3–37 prints the second element (at index 1) in the list stored in `a`.

Example 3–37. Accessing List Elements

```
puts [lindex $a 1]
```

The **llength** command returns the length of a list. Example 3–38 prints the length of the list stored in `a`.

Example 3–38. List Length

```
puts [llength $a]
```

The **lappend** command appends elements to a list. If a list does not already exist, the list you specify is created. The list variable name is not specified with a dollar sign. Example 3–39 appends some elements to the list stored in `a`.

Example 3–39. Appending to a List

```
lappend a 4 5 6
```

Arrays

Arrays are similar to lists except that they use a string-based index. Tcl arrays are implemented as hash tables. You can create arrays by setting each element individually or by using the **array set** command. To set an element with an index of `Mon` to a value of `Monday` in an array called `days`, use the following command:

```
set days(Mon) Monday
```

The `array set` command requires a list of index/value pairs. This example sets the array called days:

```
array set days { Sun Sunday Mon Monday Tue Tuesday \
    Wed Wednesday Thu Thursday Fri Friday Sat Saturday }
```

Example 3–40 shows how to access the value for a particular index.

Example 3–40. Accessing Array Elements

```
set day_abbreviation Mon
puts $days($day_abbreviation)
```

Use the **array names** command to get a list of all the indexes in a particular array. The index values are not returned in any specified order. Example 3–41 shows one way to iterate over all the values in an array.

Example 3–41. Iterating Over Arrays

```
foreach day [array names days] {
   puts "The abbreviation $day corresponds to the day \
name $days($day)"
}
```

Arrays are a very flexible way of storing information in a Tcl script and are a good way to build complex data structures.

Control Structures

Tcl supports common control structures, including **if-then-else** conditions and **for**, **foreach**, and **while** loops. The position of the curly braces as shown in the following examples ensures the control structure commands are executed efficiently and correctly. Example 3–42 prints whether the value of variable a positive, negative, or zero.

Example 3–42. If-Then_Else Structure

```
if { $a > 0 } {
   puts "The value is positive"
} elseif { $a < 0 } {
   puts "The value is negative"
} else {
   puts "The value is zero"
}
```

Example 3–43 uses a **for** loop to print each element in a list.

Example 3–43. For Loop

```
set a { 1 2 3 }
for { set i 0 } { $i < [llength $a] } { incr i } {
   puts "The list element at index $i is [lindex $a $i]"
}
```

Example 3–44 uses a **foreach** loop to print each element in a list.

Example 3–44. foreach Loop

```
set a { 1 2 3 }
foreach element $a {
    puts "The list element is $element"
}
```

Example 3–45 uses a **while** loop to print each element in a list.

Example 3–45. while Loop

```
set a { 1 2 3 }
set i 0
while { $i < [llength $a] } {
    puts "The list element at index $i is [lindex $a $i]"
    incr i
}
```

You do not need to use the **expr** command in boolean expressions in control structure commands because they invoke the **expr** command automatically.

Procedures

Use the **proc** command to define a Tcl procedure (known as a subroutine or function in other scripting and programming languages). The scope of variables in a procedure is local to the procedure. If the procedure returns a value, use the **return** command to return the value from the procedure. Example 3–46 defines a procedure that multiplies two numbers and returns the result.

Example 3–46. Simple Procedure

```
proc multiply { x y } {
    set product [expr { $x * $y }]
    return $product
}
```

Example 3–47 shows how to use the **multiply** procedure in your code. You must define a procedure before your script calls it, as shown below.

Example 3–47. Using a Procedure

```
proc multiply { x y } {
    set product [expr { $x * $y }]
    return $product
}
set a 1
set b 2
puts [multiply $a $b]
```

You should define procedures near the beginning of a script. If you want to access global variables in a procedure, use the **global** command in each procedure that uses a global variable. Example 3–48 defines a procedure that prints an element in a global list of numbers, then calls the procedure.

Example 3–48. Accessing Global Variables

```
proc print_global_list_element { i } {
    global my_data
    puts "The list element at index $i is [lindex $my_data $i]"
}
set my_data { 1 2 3}
print_global_list_element 0
```

File I/O

Tcl includes commands to read from and write to files. You must open a file before you can read from or write to it, and close it when the read and write operations are done. To open a file, use the **open** command; to close a file, use the **close** command. When you open a file, specify its name and the mode in which to open it. If you do not specify a mode, Tcl defaults to read mode. To write to a file, specify `w` for write mode as shown in Example 3–49.

Example 3–49. Open a File for Writing

```
set output [open myfile.txt w]
```

Tcl supports other modes, including appending to existing files and reading from and writing to the same file.

The **open** command returns a file handle to use for read or write access. You can use the **puts** command to write to a file by specifying a filehandle, as shown in Example 3–50.

Example 3–50. Write to a File

```
set output [open myfile.txt w]
puts $output "This text is written to the file."
close $output
```

You can read a file one line at a time with the **gets** command. Example 3–51 uses the **gets** command that prints out each line of the file, with its line number.

Example 3–51. Read from a File

```
set input [open myfile.txt]
set line_num 1
while { [gets $input line] >= 0 } {
    # Process the line of text here
    puts "$line_num: $line"
    incr line_num
}
close $input
```

Syntax & Comments

Arguments to Tcl commands are separated by white space, and Tcl commands are terminated by a newline character or a semicolon. As shown in "Substitutions" on page 3–43, you must use backslashes when a Tcl command extends more than one line.

Tcl uses the hash or pound character (#) to begin comments. The # character must begin a command. If you prefer to include comments on the same line as a command, be sure to terminate the command with a semicolon before the # character. Example 3–52 is a valid line of code that includes a **set** command and a comment:

Example 3–52. Comments

```
set a 1;# Initializes a
```

Without the semicolon, it will be an invalid command because the **set** command will not terminate until the new line after the comment.

The Tcl interpreter counts curly braces inside comments, which can lead to errors that are difficult to track down. Example 3–53 causes an error because of unbalanced curly braces:

Example 3–53. Unbalanced Braces in Comments

```
# if { $x > 0 } {
if { $y > 0 } {
    # code here
}
```

References

For more information about using Tcl, refer to the following sources:

- *Practical Programming in Tcl and Tk*, Brent B. Welch
- *Tcl and the TK Toolkit*, John Ousterhout
- *Effective Tcl/TK Programming*, Michael McLennan and Mark Harrison
- Quartus II Tcl example scripts at **www.altera.com/support/examples/tcl/tcl.html**
- Tcl Developer Xchange at **tcl.activestate.com**

4. Quartus II Project Management

QII52012-6.0.0

Introduction

FPGA designs once required just one or two engineers, but today's larger and more sophisticated FPGA designs are often developed by several engineers and are constantly changing throughout the project. To ensure efficient design coordination, designers must track their project changes.

To help designers manage their FPGA designs, the Quartus® II software provides the following capabilities:

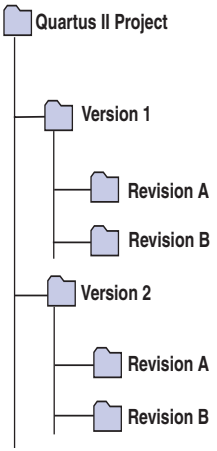
- Creating revisions
- Copying and archiving projects
- Making a version-compatible database
- Controlling message suppression

In the Quartus II software, a revision is one set of assignments and settings. A project typically has multiple revisions, with each revision having its own set of assignments and settings. Creating multiple revisions allows you to change assignments and settings while preserving the previous results.

A version is a Quartus II project that includes one set of design files and one or more revisions (assignments and settings for your project). Creating multiple versions with the Copy Project feature allows you to edit a copy of your design files while preserving the original functionality of your design.

The Quartus II Version-Compatible Database feature allows Quartus II databases to be compatible across different versions of the Quartus II software, which saves valuable design time by avoiding unnecessary compilations (Figure 4–1). This chapter also discusses how to migrate your projects from one computing platform to another as well as message suppression.

Figure 4–1. Quartus II Version-Compatible Database Structure



Creating a New Project

A Quartus II project contains all of the design files, the settings files and other files necessary for the successful compilation of your design. These files include two Quartus II settings files:

- Quartus II Project File (**.qpf**) containing the name of your project and all revisions of your project, described in "Using Revisions With Your Design" on page 4–3.
- Quartus II Settings File (**.qsf**) containing all assignments applied to your design including assignments to help fit your design and meet performance requirements. For more information on the Quartus II Settings File, refer to "Quartus II Settings File" on page 4–25.

To start a new Quartus II project, use the **New Project Wizard**. From the File menu, click the **New Project Wizard,** and add the following project information:

- Project name and directory
- Name of the top-level design entity
- Project files and user libraries
- Target device family and device
- EDA tool settings

For more information on user libraries, refer to "Specifying Libraries" on page 4–13 and "Specifying Libraries Using Scripts" on page 4–30.

Using Revisions With Your Design

The Revisions feature allows you to create a new set of assignments and settings for your design without losing your previous assignments and settings. This feature allows you to explore different assignments and settings for your design and then compare the results. You can use the Revisions feature in the following ways:

- Create a unique revision which is not based on a previous revision. Creating a unique revision lets you optimize a design for different fundamental reasons such as to optimize by area in one revision, then optimize for f_{MAX} in another revision. When you create a unique revision (a revision that is not based on an existing revision), all default settings are turned on.
- Create a revision based on an existing revision, but try new settings and assignments in the new revision. A new revision already includes all the assignments and settings applied in the previous revision. If you are not satisfied with the results in the new revision, you can revert to the original revision. You can compare revisions manually or with the Compare feature.

Creating & Deleting Revisions

All Quartus II assignments and settings are stored in the Quartus II Settings File. Each time you create a new revision of a project, the Quartus II software creates a new Quartus II Settings File and adds the name of the new revision to the list of revisions in the Quartus II Settings File.

The name of a new Quartus II Settings File matches the revision name.

You can manage revisions with the **Revisions** dialog box, which allows you to set the current revision, as well as create, delete, and compare revisions in a project.

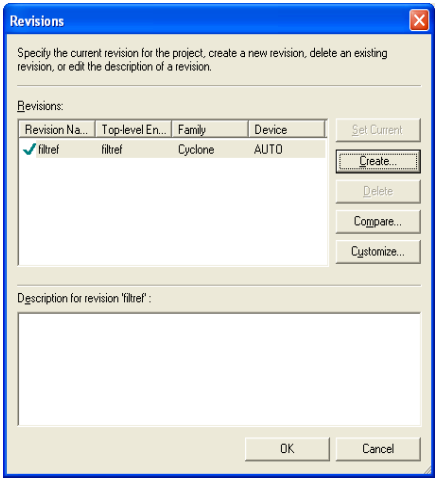
Creating a Revision

To create a revision, follow these steps:

1. If you have not already done so, create a new project or open an existing project. On the File menu, click **New Project Wizard** or **Open Project.**
2. On the Project menu, click **Revisions**.
3. To base the new revision on an existing revision for the current design, select the existing revision in the **Revisions** list.

4. Click **Create** (Figure 4–2).

Figure 4–2. Revisions Dialog Box



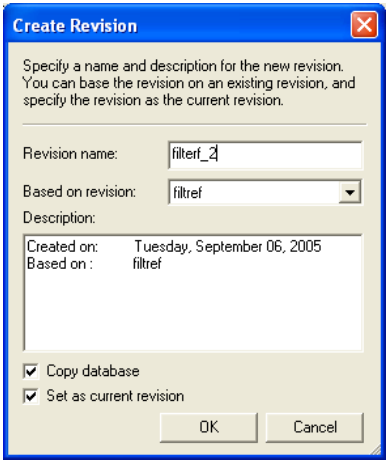
5. In the **Create Revision** dialog box (Figure 4–3), type the name of the new revision in the **Revisions name** box.

6. To base the new revision on an existing revision for the current design, if you did not select the correct revision in Step 3, select the revision in the **Based on revision** list (Figure 4–3).

   or

   To create a unique revision that is not based on an existing revision of the current design, select the "blank entry" in the **Based on revision** list.

Figure 4–3. Create Revisions Dialog Box



7. Optionally, edit the description of the revision in the **Description** box (Figure 4–3).

8. Turn off the **Copy database** option if you do not want the new revision to contain the database information from the existing revision. The **Copy database** option is on by default.

   Copying the database allows you to view the results from the previous compilation while you are making changes to the settings of the new revision.

9. If you do not want to use the new revision immediately, turn off **Set as current revision.** The **Set as current revision** option is on by default.

10. In the **Create Revision** dialog box (Figure 4–3), click **OK**.

Delete a Revision

To delete a revision, follow these steps:

1. If you have not already done so, open an existing project by clicking **Open Project** on the File menu and selecting a Quartus II Project File.

2. On the Project menu, click **Revisions**.

3. In the **Revisions** list, select the revision you want to delete and click **Delete**.

You cannot delete the current revision when it is active; you must first open another revision. For example, if revision A is currently active, you need to create (if the revision does not exist) and open revision B before you delete revision A.

Comparing Revisions

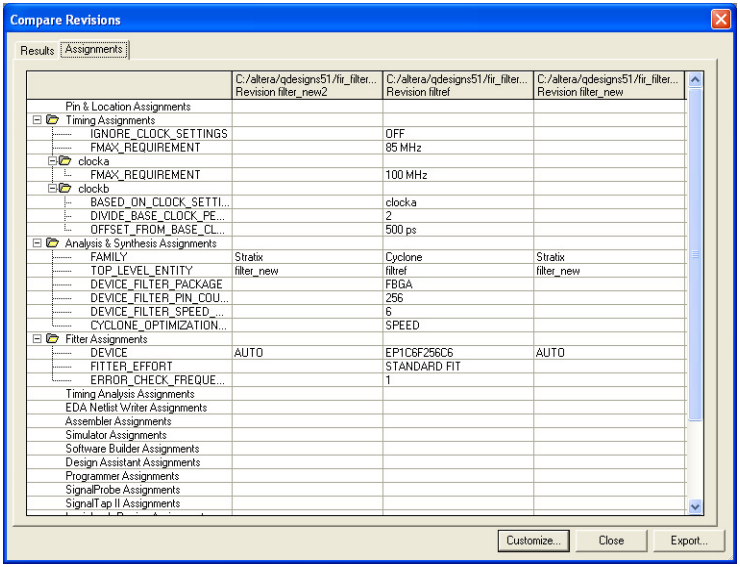
You can compare the results of multiple revisions side by side with the **Compare Revisions** dialog box.

1. On the Project menu, click **Revisions**.

2. In the **Revisions** dialog box, click **Compare** to compare all revisions in a single window.

The **Compare Revisions** dialog box (Figure 4–4) compares the results of each revision in three assignment categories: Analysis & Synthesis, Fitter, and Timing Analyzer.

Figure 4–4. Compare Revisions Dialog Box



In addition to viewing the results of each revision, you also can show the assignments for each revision. Click the **Assignments** tab in the **Compare Revisions** dialog box to view all assignments applied to each revision (Figure 4–4). To export both **Results** and **Assignments** for your revisions, click on **Export.** When the dialog box appears, enter the name of the Comma-Separated Value (.**csv**) file into which the software will export the data when you click **OK**. Gain better understanding of how different optimization options affect your design by viewing the results of each revision and their assignments.

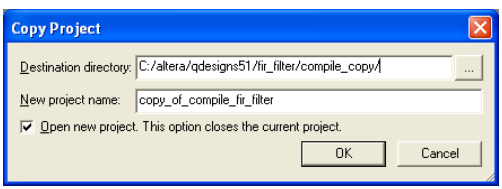
Creating Different Versions of Your Design

Managing different versions of design files in a large project can become difficult. To assist in this task, the Quartus II software provides utilities to copy and save different versions of your project. Creating a version of your project includes copying all your design files, your Quartus II settings file, and all your associated revisions (all assignments and settings).

To create a new version of your project with the Quartus II software, create a copy of your project and edit your design files. An example is if you have a design that is compatible with a 32-bit data bus and you require a new version of the design to interface with a 64-bit data bus. To solve this problem, create a new version of your project and edit the new version of the design files by performing the following steps:

1. On the Project menu, click **Copy Project.** The **Copy Project** dialog box appears (Figure 4–5).

Figure 4–5. Copy Project Dialog Box



2. Specify the path to your new project in the **Destination directory** box.
3. Type the new project name in the **New project name** box.
4. To open the new project immediately, turn on **Open new project**. This option closes the current project option.
5. Click **OK**.

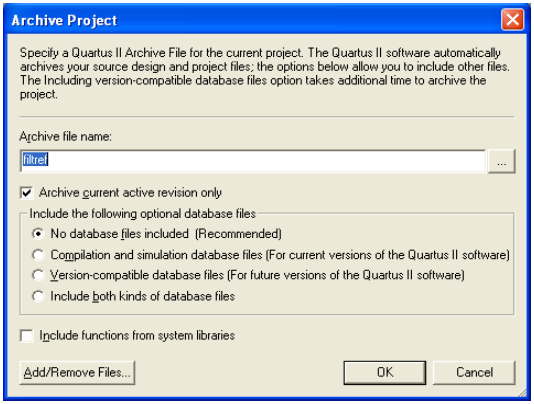
When creating a new version of your project with an Electronic Data Interchange Format (EDIF) or Verilog Quartus Mapping (.**vqm**) netlist from a third-party EDA synthesis tool, create a copy of your project and then replace the previous netlist file with the newly generated netlist file. On the Project menu, click **Copy Project** to create a copy of your design. On the Project menu, click the **Add/Remove Files** command to add and remove design files, if necessary.

Archiving Projects with the Quartus II Archive Project Feature

A single project can contain hundreds of files in many directories, which can make transferring a project between engineers difficult. You can use the Quartus II Archive Project feature to create a single compressed Quartus II Archive File (**.qar**) of your project containing all your design, project, and settings files. The Quartus II Archive File contains all the files, including the Quartus II Default Settings File (**.qdf**), required to perform a full compilation to restore the original results. The Quartus II Default Settings File contains all the project and assignment default settings from the current version of the Quartus II software. It is necessary to archive the Default Settings File to preserve your results when you restore the archive in a different version of the Quartus II software. For more information on the Quartus II Default Settings File, refer to "Quartus II Default Settings File" on page 4–26.

With the archive file generated by the Archive Project feature (Figure 4–6), you can easily share projects between engineers.

Figure 4–6. Archive Project Dialog Box



Archive a Project

To archive a project, perform these steps:

1. If you have not already done so, create a new project or open an existing project. On the File menu, click **New Project Wizard** or **Open Project**.

2. On the Processing menu, point to Start and click **Start Analysis & Elaboration**.

Altera® recommends that you perform analysis and elaboration before archiving a project to ensure that all design files are located and archived.

3. On the Project menu, click **Archive Project**.

4. In the **Archive file name** box, type the file name of the Quartus II Archive File you want to archive, or click **Browse** to select a Quartus II Archive File name.

5. Turn on **Archive current active revision only** to archive the currently active revision. If you do not turn on this option, all revisions within the project are included in the project archive.

6. Select one of the following items under **Include the following optional database files** in the **Archive Project** dialog box (Figure 4–6).

    a. Select **No database files included** to exclude both compilation and simulation database files and version-compatible database files from the archive.

    b. Select **Compilation and simulation database files** to include the compilation and simulation database files in the archive.

    c. Select **Version-compatible database files** to include the version-compatible database files in the archive.

    d. Select **Include both kinds of database files** to include both compilation and simulation database files and version-compatible database files in the archive.

7. Turn on **Include functions from system libraries** to include functions from system libraries in the archive.

8. Click **Add/Remove Files** to add or remove files from the archive.

9. Click **OK**.

Restore an Archived Project

To restore an archived project, perform the following steps:

1. On the Project menu, click **Restore Archived Project**.
2. In the **Archive file name** box, type the file name of the Quartus II Archive File you wish to restore, or click **Browse to** select a Quartus II Archive File.
3. In the **Destination folder** box, specify the directory path into which you will restore the contents of the Quartus II Archive File, or browse to a directory.
4. Click **Show log** to view the Quartus II Archive Log File (**.qarlog**) for the project you are restoring from the Quartus II Archive File.
5. Click **OK**.
6. If you did not include the compilation and simulation database files in the project archive (Figure 4–6), you must recompile the project.

Version-Compatible Databases

Prior to the Quartus II software version 4.1, compilation databases were locked to the current version of the Quartus II software. With the introduction of the Version-Compatible Database feature in the Quartus II software version 4.1, you can export a version-compatible database and import it into a later version. For example, using one set of design files, you can export a database generated from the Quartus II software version 4.1 and import it into the Quartus II software version 5.1 and later without recompiling your design. Using this feature eliminates unnecessary compilation time.

Migrate to a New Version

To migrate a design from one Quartus II software version to a newer version, perform the following steps:

1. On the File menu, open the older version of the Quartus II software project by clicking **Open Project**.
2. On the Project menu, click **Copy Project** to make a new copy of the project. The copied project will open in the older version.

3. On the Project menu, click **Export Database**. By default, the database is exported to the **export_db directory** of the copied project. If desired, a new directory can be created.

4. Open the copied project from the new version of the Quartus II software. The Quartus II software deletes the existing database but not the exported database.

5. On the Project menu, click **Import Database**. By default, the directory of the database you just exported is selected.

Save the Database in a Version-Compatible Format

To save the database in a version-compatible format during every compilation, perform the following steps:

1. On the Assignments menu, click **Settings.** The **Settings** dialog box displays.

2. In the **Category** list, select the **Compilation Process** page. The Compilation Process page displays.

3. Turn on the **Export version-compatible database** option.

4. Browse to the directory where you want to save the database.

5. Click **OK**.

Quartus II Project Platform Migration

When moving your project from one computing platform to another, you must think about the following cross-platform issues:

- Filenames and Hierarchy
- Specifying Libraries
- Quartus II Search Path Precedence Rules
- Quartus II-Generated Files for Third-Party EDA Tools
- Migrating Database Files

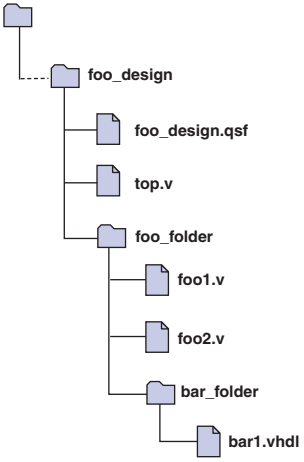
Filenames & Hierarchy

To ensure migration across platforms, you must consider a few basic differences between operating systems when naming source files, especially when interacting with these from the system-command prompt or a Tcl script:

- Some operating system file systems are case-sensitive. When writing scripts, ensure you specify paths exactly, even if the current operating system is not case-sensitive. For best results, use lowercase letters when naming files.
- Use a character set common to all the used platforms.
- You do not have to convert the forward-slash / and back-slash \ path separators in the Quartus Settings File because the Quartus II software changes all back-slash \ path separators to forward-slashes /.
- Observe the shortest file name length limit of the different operating systems you are using.

You can specify files and directories inside a Quartus II project as paths relative to the project directory. For instance, for a project titled **foo_design** with a directory structure shown in Figure 4–7, specify the source files as: **top.v, foo_folder/foo1.v**, **foo_folder/foo2.v**, and **foo_folder/bar_folder/bar1.vhdl**.

Figure 4–7. All-Inclusive Project Directory Structure



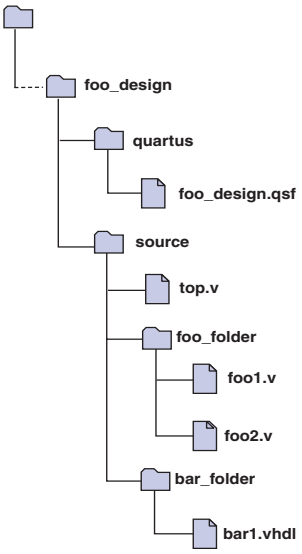
If the Quartus II Settings File is in a directory that is separate from the source files, you can specify paths using the following options:

- Relative paths
- Absolute paths
- Libraries

Relative Paths

If the source files are very near the Quartus II project directory, you can express relative paths using the . . notation. For example, given the directory structure shown in Figure 4–8, you can specify **top.v** as **../source/top.v** and **foo1.v** as **../source/foo_folder/foo1.v**.

Figure 4–8. Quartus II Project Directory Separate from Design Files



When you copy a directory structure to a different platform, ensure that any subdirectories are in the same hierarchical structure and relative path as in the original platform.

Specifying Libraries

You also can specify the directory (or directories) containing source files as a library that the Quartus II software searches when you compile your project. A Quartus II library is a directory containing design files used by your Quartus II project. You can specify the following two kinds of libraries in the Quartus II software:

- User libraries, which apply to a specific project
- Global libraries, which all projects use

Use the procedures in this section to specify user or global libraries.

All files in the directories specified as libraries are relative to the libraries. For example, if you want to include the file **/user_lib1/foo1.v** and the **user_lib1** directory is specified as a user library in the project, the **foo1.v** file can be specified in the Quartus II Settings File as **foo1.v**. The Quartus II software searches directories that are specified as libraries and finds the file.

Specifying User Libraries

To specify user libraries from the GUI: from the Assignments menu, click **Settings**, and select **User Libraries (Current Project)**. Type the name of the directory in the **Library name** box, or browse to it. User libraries are stored in the Quartus II Settings File of the current revision.

Specifying Global Libraries

Specify global libraries from the GUI: On the Tools menu, click **Options**, and select **Global User Libraries (All Project)**. Type the name of the directory in the **Library name** box, or browse to it. Global libraries are stored in the **quartus2.ini** file. The Quartus II software searches for the **quartus2.ini** file in the following order:

- USERPROFILE, for example, **C:\Documents and Settings**<*user name*>
- Directory specified by the **TMP** environmental variable
- Directory specified by **TEMP** environmental variable
- Root directory, for example, **C:**

For UNIX and Linux users, the file is created in the **altera.quartus** directory under the <*home*> directory, if the **altera.quartus** directory exists. If the **altera.quartus** directory does not exist, the file is created in the <*home*> directory.

Whenever you specify a directory name in the GUI or in Tcl, the name you use is maintained verbatim in the Quartus II Settings File rather than resolved to an absolute path.

If the directory is outside of the project directory, the path returned in the dialog box is an absolute path, and you can use the **Browse** button in either the **Settings** dialog box or the **Options** dialog box to select a directory. However, you can change this absolute path to a relative path by editing the absolute path displayed in the Library name field to create a relative path before you click **Add** to put the directory in the **Libraries** list.

When copying projects that specify user libraries, you must either copy your user library files along with the project directory or ensure that your user library files exist in the target platform.

Search Path Precedence Rules

If two files have the same file name, the file found is determined by the Quartus II software's search path precedence rules. The Quartus II software resolves relative paths by searching for the file in the following directories and order:

1. The project directory, which is the directory containing the Quartus II Settings File.
2. The project's database (**db)** directory.
3. User libraries are searched in the order specified by the **USER_LIBRARIES** setting of the Quartus II Settings File for the current revision.
4. Global user libraries are searched in the order specified by the **USER_LIBRARIES** setting on the **Global User Libraries** page in the **Options** dialog box.
5. The Quartus II software **libraries** directory.

For more information on libraries, refer to "Specifying Libraries Using Scripts" on page 4–30.

Quartus II-Generated Files for Third-Party EDA Tools

When you copy your project to another platform, regenerate any Quartus II software-generated files for use by other EDA tools, using the GUI or the **quartus_eda** executable.

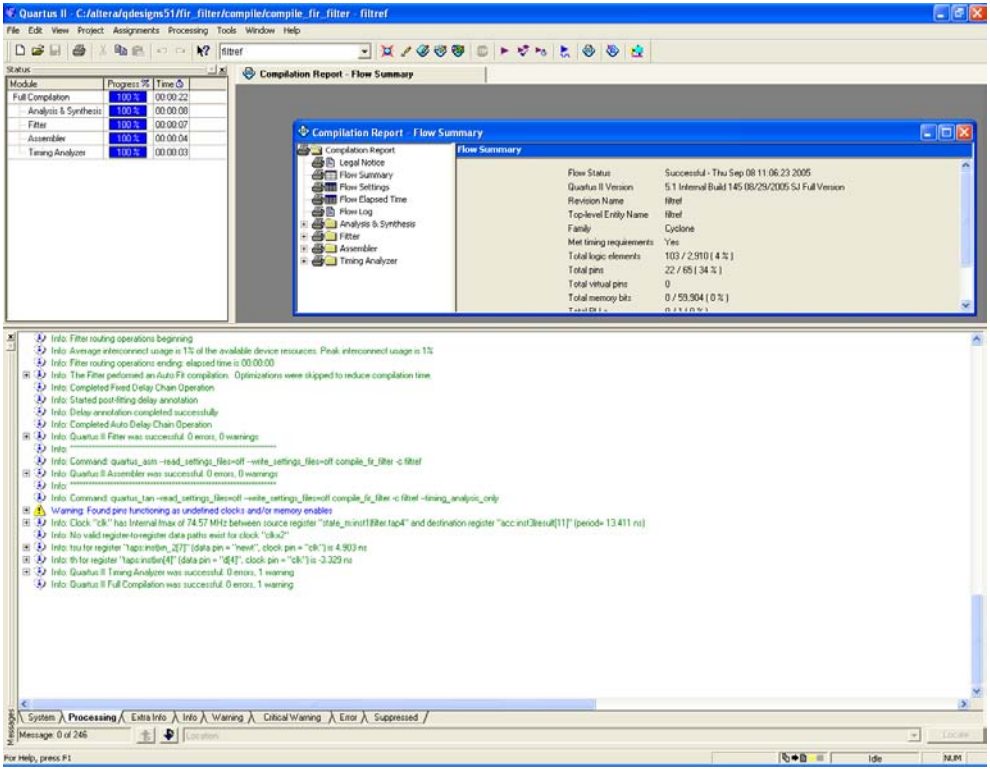
Migrating Database Files

There is nothing inherent in the file format and syntax of exported version-compatible database files that might cause problems for migrating the files to other platforms. However, the contents of the database can cause problems for platform migration. For example, use of absolute paths in version-compatible database files generated by the Quartus II software can cause problems for migration. Altera recommends that you change absolute paths to relative paths before migrating files whenever possible.

Working with Messages

The Quartus II software generates various types of messages, including Information, Warning, and Error messages. Some messages include information on software status during a compilation and alert you to possible problems with your design. Messages are displayed in the Messages window in the Quartus II GUI (Figure 4–9), and written to standard out and when you use command-line executables. In both cases, messages are written to Quartus II report files.

Figure 4–9. Viewing Quartus II Messages



You can right-click on a message in the Message window and get help on the message, locate the source of the message of your design, and manage messages.

Messages provide useful information if you take time to review them after each compilation. However, it can be tedious if there are thousands of them. Beginning with version 5.1 and later, the Quartus II software includes new features to help you manage messages.

Messages Window

By default, the Messages window displays eight message tabs (Table 4–1), which makes it easy to review all messages of a certain type.

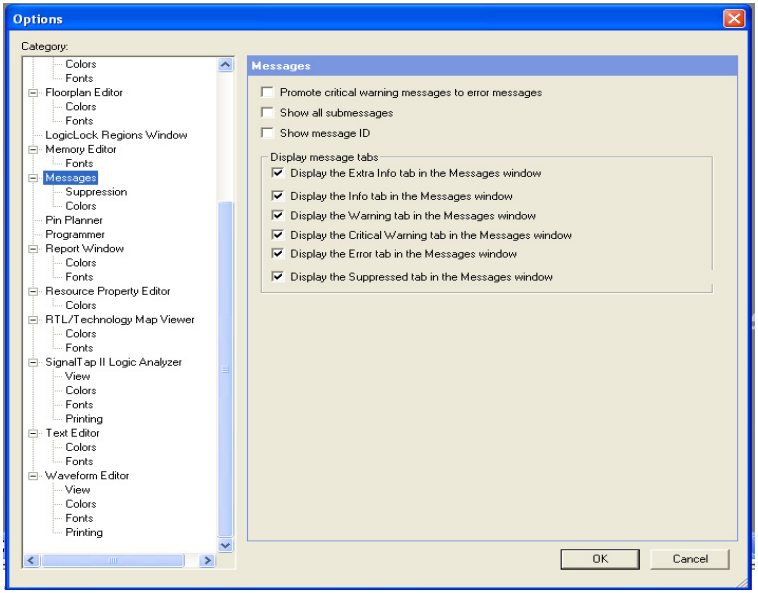
Table 4–1. Quartus II Message Tabs

Message Tab	Description
System	Displays messages that are unrelated to processing your design. For example, messages generated during programming are displayed in the **System** tab.
Processing	Displays messages that are generated when the Quartus II software processes your most recent compilation, simulation, or software build; timing analysis messages appear as part of the compilation messages.
Info	Displays general informational messages during a compilation, simulation, or software build. For example: legal and compilation-success messages.
Extra Info	Displays detailed informational messages about the operations for designers. For example: extra fitting information messages.
Warning	Displays strong warning messages generated during a compilation, simulation, or software build. For example: detection of signal promotion to global and high fan-out nets.
Critical Warning	Displays critical warning messages generated during a compilation, simulation, or software build. For example: detection of combinational feedback loops, gated clocks, or register duplication.
Error	Displays processing and compilation error messages generated during a compilation, simulation, or software build. Error messages can sometimes stop processing and cannot be disabled.
Suppressed	Displays suppressed messages during the last processing operation.

The **Info**, **Extra Info**, **Warning**, **Critical Warning**, and **Error** tabs display messages grouped by type. Warning messages are shown with all other types of messages in the Processing message window; all warning messages also appear in the **Warning message** tab.

You can control which tabs are displayed by right-clicking in the Messages window and choosing options from the right button pop-up menu, and with the options in the **Display Message** tabs section of the Messages page in the **Options** dialog box of the Tools menu (Figure 4–10).

Figure 4–10. Message Tab Options



The **Suppressed** tab shows messages suppressed during the last processing operation. You can also prevent the **Suppressed** tab from being displayed with an option in the **Display Message** tabs section of the Messages pane in the **Options** dialog box of the Tools menu.

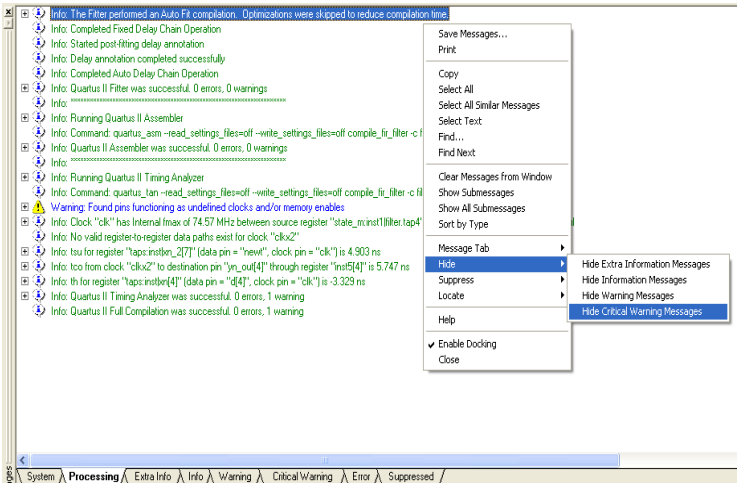
Hiding Messages

In the Messages window, you can hide all messages of a particular type. For example, to hide Info messages, follow these steps:

1. On the **Processing** tab, right-click in the **Processing** message window, and click the **Hide** option (Figure 4–11).

2. Select the Info message type.

Figure 4–11. Hiding Messages from the Processing Tab



All messages of the specified types are removed from the list of messages in the **Processing** tab, although they are still included in the separate tabs corresponding to the message type. For example, if you hide Info messages, no Info messages are shown in the Processing message window, but all the Info messages are shown in the Info messages window.

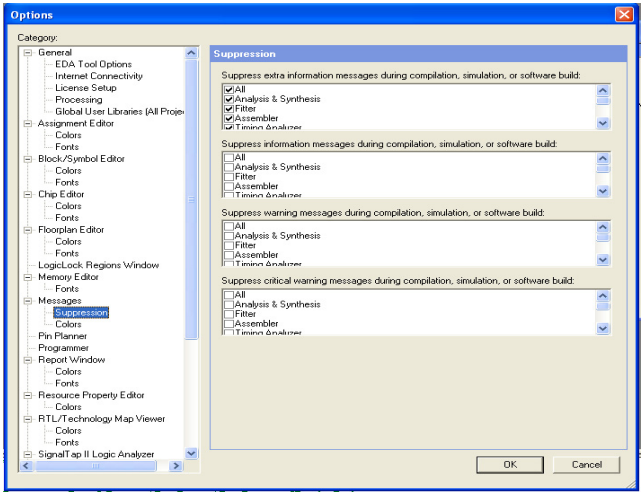
Message Suppression

Message suppression is a new feature in version 5.1 or later of the Quartus II software. You can use message suppression to reduce the number of messages to be reviewed after a compilation by preventing individual messages and entire categories of messages from being displayed. For example, if you review a particular message and determine that it is not caused by something in your design that should be changed or fixed, you can suppress the message so it is not displayed during subsequent compilations. This saves time because you see only new messages during subsequent compilations.

Every time you add a message to be suppressed, a suppression rule is created. Suppressing exact selected messages adds patterns that are exact strings to the suppression rules. Suppressing all similar messages adds patterns with wildcards to the suppression rules.

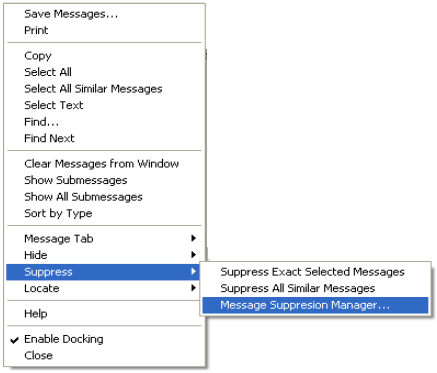
Furthermore, you can suppress all messages of a particular type in a particular stage of the compilation flow. On the Tools menu, click **Options,** and click **Suppression** from under the Messages section (Figure 4–12).

Figure 4–12. Controlling Suppression Messages



Suppressing individual messages is controlled in two locations in the Quartus II GUI. You can right-click on a message in the Messages window and choose commands in the Suppress sub-menu entry. To open the Message Suppression Manager, right-click in the Messages window. From the Suppress sub-menu item, click **Message Suppression Manager** (Figure 4–13).

Figure 4–13. Message Suppression Manager



Refer to "Message Suppression Manager" on page 4–22 for further information.

Message Suppression Methods

There are two methods you can use to create suppression rules: Suppress Exact Selected Messages and Suppress All Similar Messages. If you suppress a message with the exact selected messages option, only messages matching the exact text will be suppressed during subsequent compilations. The All Similar Messages option behaves like a wildcard pattern on variable fields in messages.

For an example of suppressing all similar messages, consider the following message:

```
Info: Found 1 design units, including 1 entities, in source file mult.v.
```

This type of message is common during synthesis and is displayed for each source file that is processed, with varying information about the number of design units, entities, and source file name.

Help for this message shows it is in the form Found <*number*> design units, including <*number*> entities, in source file <*name*>. Choosing to suppress all similar messages effectively replaces the variable parts of that message (<*number*>, <*number*>, and <*name*>) with wildcards, resulting in the following suppression rule:

```
Info: Found * design units, including * entities, in source file *.
```

As a result, all similar messages (ones that match the pattern) are suppressed.

Details & Limitations

The following limitations apply to which messages can be suppressed and how they can be suppressed:

- You cannot suppress error messages or messages with information about Altera legal agreements.
- Suppressing a message also suppresses all its submessages, if there are any.
- Suppressing a submessage causes matching submessages to be suppressed only if the parent messages are the same.
- You cannot create your own custom wildcards to suppress messages.
- You must use the Quartus II GUI to manage message suppression, including choosing messages to suppress. These messages are suppressed during compilation in the GUI and when using command-line executables.

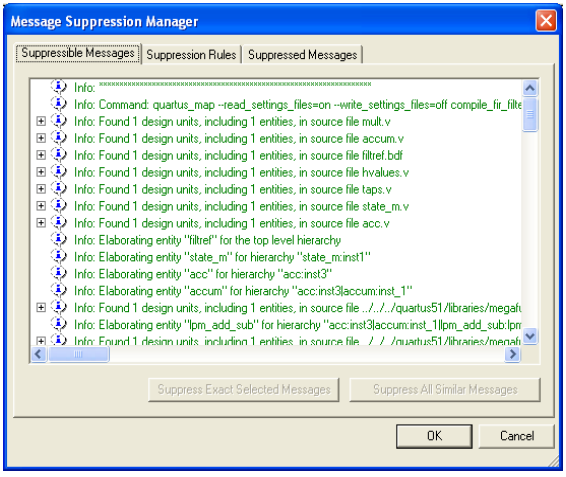
- Messages are suppressed on a per-revision basis, not for an entire project. Information about which messages to suppress is stored in a file called <*revision*>**.srf**. If you create a revision based on a revision for which messages are suppressed, the suppression rules file is copied to the new revision. You cannot make all revisions in one project use the same suppression rules file.
- You cannot remove messages or modify message suppression rules while a compilation is running.

Message Suppression Manager

You can use the Message Suppression Manager to view and suppress messages, view and delete suppression rules, and view suppressed messages.

Open the Message Suppression Manager by clicking the **Processing** tab. Right-click anywhere in the Messages window and click **Message Suppression Manager** from the Suppression sub-menu. The Message Suppression Manager has three tabs labeled Suppressible Messages, Suppression Rules, and Suppressed Messages (Figure 4–14).

Figure 4–14. Message Suppression Manager Window



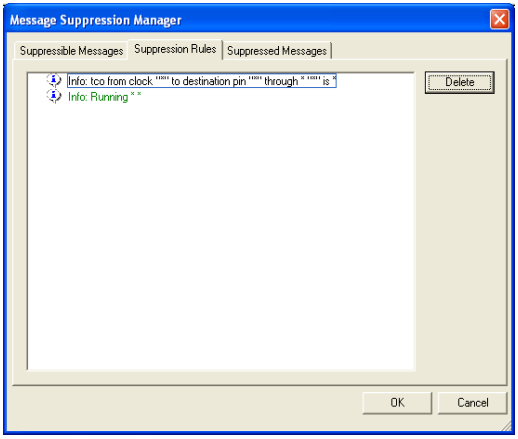
Suppressible Messages

Messages that are listed in the **Suppressible Messages** tab are messages that were not suppressed during the last compilation. These messages can be suppressed. The **Select All Similar Messages** option in the right click menu selects messages according to the example described in the "Message Suppression Methods" on page 4–21. You can select all similar messages to see which messages are suppressed if you choose to suppress all similar messages.

Suppression Rules

Items listed in the **Suppression Rules** tab are the patterns that the Quartus II software uses to determine whether to suppress a message. Messages matching any of the items listed in the **Suppression Rules** tab are suppressed during compilations (Figure 4–15).

Figure 4–15. Message Suppression Manager



An entry in the **Suppression Rules** tab that includes a message with submessages indicates the submessage is suppressed only when all its parent messages match.

You can stop suppressing messages by deleting the suppression rules that match them (causing them to be suppressed). Merely deleting suppression rules does not cause the formerly suppressed messages to be added to the messages generated during the previous compilation; you must recompile the design for the changed suppression rules to take effect.

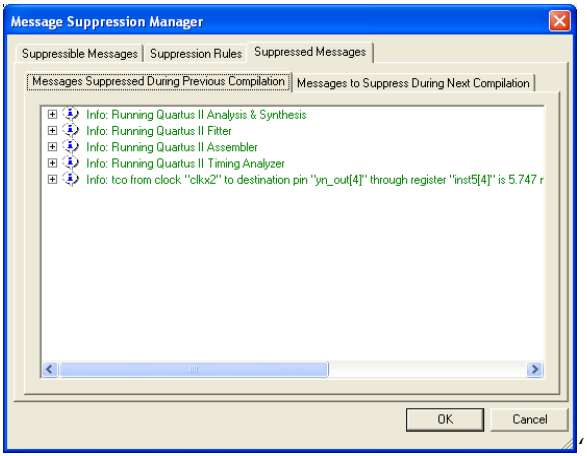
Suppressed Messages

Messages listed in the **Suppressed Messages** tab are divided in two sub-tabs:

- Messages Suppressed During Previous Compilation
- Messages to Suppress During Next Compilation

The messages listed in the Messages Suppressed During Previous Compilation sub-tab are all the suppressed messages from the previous compilation (Figure 4–16).

Figure 4–16. Messages Suppressed During Previous Compilation



These messages are also listed in the **Suppressed** tab in the Messages window. Messages listed in the Messages to Suppress During Next Compilation are messages that will be suppressed during the next compilation that match suppression rules created after the last compilation finished.

In addition to appearing in the **Suppressed** tab in the Messages window, suppressed messages are included in a Suppressed Messages entry in the Quartus II compilation report, viewable in the GUI. Suppressed messages are not included in the *<revision>*.*<module>*.**rpt** text files; they are written to a separate text report file called *<revision name>*.*<module>*.**smsg**.

Quartus II Settings File

All assignments made in the Quartus II software are stored as Tcl commands in the Quartus II Settings File. The Quartus II Settings File is a text based file containing Tcl commands and comments. The Quartus II Settings File is not a Tcl script and does not support the full Tcl scripting language.

As you make assignments in the Quartus II software, the assignments are either stored temporarily in memory or written out to the Quartus II Settings File. This is determined by the **Update assignments to disk during design processing only** option, which is located in the Tools menu under Options on the Processing page. If the option is turned on, then all assignments are stored in memory and are written to the Quartus II Settings File when a compilation has started or when you save or close the project. By saving assignments to memory, the performance of the software is improved because it avoids unnecessary reading and writing to the Quartus II Settings File on the disk. This performance improvement is seen more dramatically when the project files are stored on a remote data disk.

Beginning with the Quartus II software version 5.1, you can add lines of comments into the Quartus II Settings File, such as are shown in the following example:

```
# Assignments for input pin clk
# Clk is being driven by FPGA 1
set_location_assignment PIN_6 -to clk
set_instance_assignment -name IO_STANDARD "2.5 V" -to clk
```

Sourcing other Quartus II Settings Files is supported using the following Tcl command:

```
source <filename>.qsf
```

Format Preservation

Beginning with the Quartus II software version 5.1, the Quartus II software maintains the order of assignments within the Quartus II Settings File. When you make new assignments, they are appended to the end of the Quartus II Settings File. If you modify an assignment, the corresponding line in the Quartus II Settings File is modified and the order of assignments in the Quartus II Settings File is maintained except when you add and remove project source files, or when you add, remove, and exclude members from an assignment group. In these cases, all assignments are moved to the end of the Quartus II Settings File. For example, if you add a new design file into the project, the list of all your design files is removed from its current location in the file and moved to the end of the Quartus II Settings File.

The header that is located at the beginning of the Quartus II Settings File is written only if the Quartus II Settings File is newly created.

The Quartus II software preserves all spaces and tabs for all unmodified assignments and comments. When you make a new assignment or modify an existing assignment, the assignment is written using the default formatting.

Quartus II Default Settings File

The Quartus II Default Settings File contains all the project and assignment default settings from the current version of the Quartus II software. The Quartus II Default Settings File, located in the win directory of the Quartus II installation path, is used to ensure consistent results when defaults are changed between versions of the Quartus II software.

The Quartus II software reads assignments from various files and stores the assignments in memory. The Quartus II software reads settings files in the following order shown below, so that assignments in subsequent files take precedence over earlier ones:

1. **assignment_defaults.qdf** from <*Quartus II Installation directory*>**/win**
2. **assignment_defaults.qdf** from project directory
3. <*revision name*>**_assignment_defaults.qdf** from project directory
4. <*revision name*>**.qsf** from project directory

As each new file is read, if an existing assignment from a previous file matches (following rules of case sensitivity, multi-value fields as well as other rules), then the old value is removed and replaced by the new. For example, if the first file has a non multi-valued assignment A=1, and the second file has A=2, then the assignment A=1, stored in memory, is replaced by A=2.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp
```

The *Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Managing Revisions

You can use the following commands to create and manage revisions. For more information about managing revisions, including creating and deleting revisions, setting the current revision, and getting a list of revisions, refer to "Creating & Deleting Revisions" on page 4–3.

Creating Revisions

The following Tcl command creates a new revision called **speed_ch**, based on a revision called **chiptrip** and sets the new revision as the current revision. The **–based_on** and **–set_current** options are optional.

```
create_revision speed_ch -based_on chiptrip -set_current
```

Setting the Current Revision

Use the following Tcl command to specify the current revision:

```
set_current_revision <revision name>
```

Getting a List of Revisions

Use the following Tcl command to get a list of revisions in the opened project:

```
get_project_revisions
```

Deleting Revisions

Use the following Tcl command to delete a revision:

```
delete_revision <revision name>
```

Archiving Projects with a Tcl Command or at the Command Prompt

You can archive projects with a Tcl command or with a command run at the system command prompt. For more information about archiving projects, refer to "Archiving Projects with a Tcl Command or at the Command Prompt" on page 4–28.

The following Tcl command creates a project archive with the default settings and overwrites the specified archived file if it already exists:

```
project_archive archive.qar -overwrite
```

Type the following command at a command prompt to create a project archive called **top**:

```
quartus_sh --archive top ↵
```

Restoring Archived Projects

You can restore archived projects with a Tcl command or with a command run at a command prompt. For more information about restoring archived projects, refer to "Restore an Archived Project" on page 4–10.

The following Tcl command restores the project archive named **archive.qar** in the **restored** subdirectory and overwrites existing files:

```
project_restore archive.qar -destination restored -overwrite
```

Type the following command at a command prompt to restore a project archive:

```
quartus_sh --restore archive.qar ↵
```

Importing & Exporting Version-Compatible Databases

You can import and export version-compatible databases with either a Tcl command or a command run at a command prompt. For more information about importing and exporting version-compatible databases, refer to "Version-Compatible Databases" on page 4–10.

The `flow` and `database_manager` packages contain commands to manage version-compatible databases.

Use the following Tcl commands from the `database_manager` package to import or export version-compatible databases.

```
export_database <directory>
import_database <directory>
```

Use the following Tcl commands from the `flow` package to import or export version-compatible databases. If you use the flow package, you must specify the database directory variable name.

```
set_global_assignment \
-name VER_COMPATIBLE_DB_DIR <directory>
execute_flow –flow export_database
execute_flow –flow import_database
```

Add the following Tcl commands to automatically generate version-compatible databases after every compilation:

```
set_global_assignment \
-name AUTO_EXPORT_VER_COMPATIBLE_DB ON
set_global_assignment \
-name VER_COMPATIBLE_DB_DIR <directory>
```

The **quartus_cdb** and the **quartus_sh** executables provide commands to manage version-compatible databases:

```
quartus_cdb <project> -c <revision> \
--export_database=<directory> ↵
quartus_cdb <project> -c <revision> \
--import_database=<directory>↵

quartus_sh –flow export_database <project> -c \
<revision> ↵
quartus_sh –flow import_database <project> -c \
<revision> ↵
```

Specifying Libraries Using Scripts

In Tcl, use commands in the `::quartus::project` package to specify user libraries. To specify user libraries, use the **set_global_assignment** command. To specify global libraries use the **set_user_option** command. The following examples show typical usage of the **set_global_assignment** and **set_user_option** commands:

```
set_global_assignment -name USER_LIBRARIES \
"../other_dir/library1"
set_user_option -name USER_LIBRARIES \
"../an_other_dir/library2"
```

To report any user libraries specified for a project and any global libraries specified for the current installation of the Quartus II software, use the **get_global_assignment** and **get_user_option** Tcl commands. The following Tcl script outputs the user paths and global libraries for an open Quartus II project:

```
get_global_assignment -name USER_LIBRARIES
get_user_option -name USER_LIBRARIES
```

Conclusion

Designers often try different settings and versions of their designs throughout the development process. Quartus II project revisions facilitate the creation and management of different assignments and settings.

In addition, understanding how to smoothly migrate your projects from one computing platform to another, controlling messages, and reducing compilation time is important as well. The Quartus II software facilitates efficient management of your design to accommodate today's more sophisticated FPGA designs.

Section II. I/O & PCB Tools

This section provides an overview of the I/O planning process, Altera's FPGA pin terminology, as well as the various methods for importing, exporting, creating, and validating pin-related assignments using Quartus® II software, and describes the design flow that includes making and analyzing pin assignments using the **Start I/O Assignment Analysis** command in the Quartus II software, during and after the development of your HDL design.

This section includes the following chapters:

- Chapter 5, I/O Management
- Chapter 6, Mentor Graphics PCB Design Tools Support
- Chapter 7, Cadence PCB Design Tools Support

Revision History

The table below shows the revision history for Chapters 5 through 7.

Chapter(s)	Date / Version	Changes Made
5	May 2006, v6.0.0	Updated for the Quartus II software version 6.0.0. • Updated text and graphics to reflect the GUI changes. • Added pin filtering information. • Added pin assignments and Pad View information. • Added Package view information.
	October 2005, v5.1.0	• Updated for the Quartus II software version 5.1.0. • I/O Assignment Analysis material incorporated into chapter.
	May 2005, v5.0.0	Initial release.
6	May 2006, v6.0.0	Was chapter 7 in v5.1. Minor updates for the Quartus II software version 6.0.0.
	November 2005, v5.1.1	Corrected text in steps 3 and 4 on page 11.
	October 2005, v5.1.0	Initial release.
7	May 2006, v6.0.0	Was chapter 6 in v5.1. Minor updates for the Quartus II software version 6.0.0.
	November 2005, v5.1.1	Realigned figures 6-9 and 6-14.
	October 2005, v5.1.0	Initial release.

5. I/O Management

QII52013-6.0.0

Introduction

The process of managing I/Os for today's leading FPGA devices involves more than just fitting design pins into a package. The increasing complexity of today's I/O standards and pin placement guidelines are just some of the factors that influence pin-related assignments. The I/O capabilities of the FPGA device and board layout guidelines influence pin location and other types of assignments for each of your design pins. Therefore, it is necessary to begin I/O planning and printed circuit board (PCB) development even before starting the FPGA design.

This chapter provides an overview of the I/O planning process, FPGA pin terminology, the various methods for importing, exporting, creating, and validating pin-related assignments.

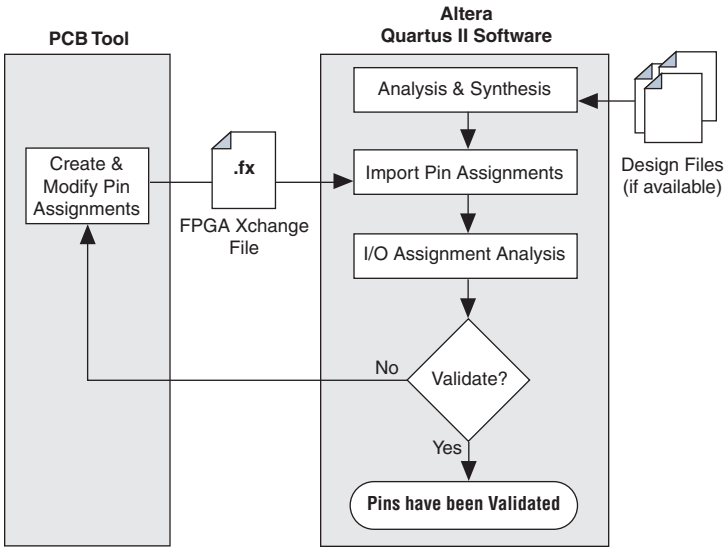
I/O Planning Overview

I/O planning includes creating pin-related assignments and validating them against pin placement guidelines. This process ensures a successful fit in your Altera® FPGA device. The Quartus® II software includes the Pin Planner and the I/O Assignment Analyzer to assist you in I/O planning.

The method you use to create your pin assignments depends on your requirements. If your PCB is partially designed, create your FPGA assignments in your PCB tool and import them into the Quartus II software for validation (Figure 5–1).

Currently, the Mentor IO Designer PCB tool is supported in the I/O planning flow.

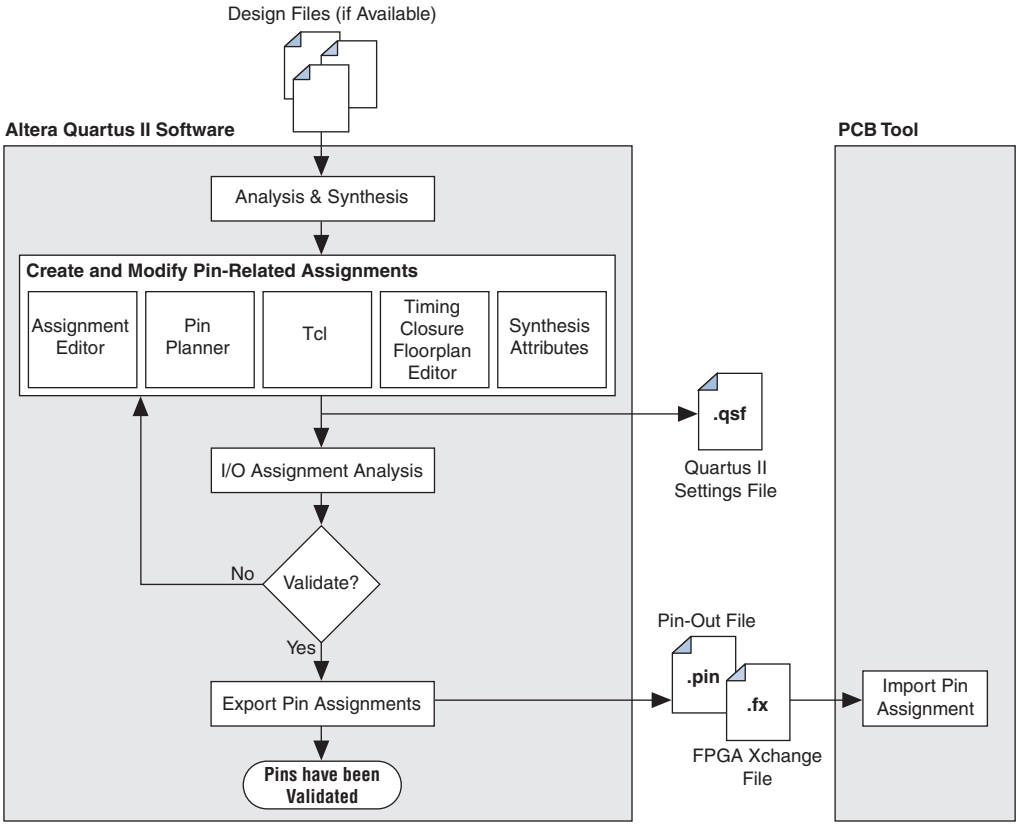
Figure 5–1. I/O Planning Flow Using an FPGA Xchange File from a PCB Tool



For more information on board layout, please refer to the *Cadence PCB Design Tools Support* and the *Mentor Graphics PCB Design Tools Support* chapters in volume 2 of the *Quartus II Handbook*.

If you have not designed the PCB, create and validate your I/O assignments in the Quartus II software, then export them to the PCB tool (Figure 5–2).

Figure 5–2. Quartus II Software I/O Planning Flow

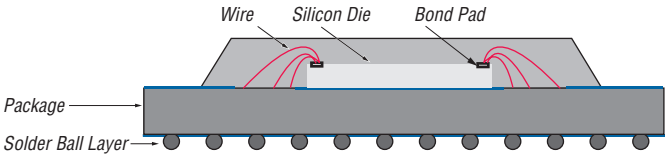


Understanding Altera FPGA Pin Terminology

Altera FPGA devices are available in a variety of packages to meet all of your complex design needs. In order to describe Altera FPGA pin terminology, a wirebond Ball Grid Array (BGA) package is used as an example. On the top surface of the silicon die there is a ring of bond pads that connect to the I/O pins of the silicon. In a wirebond BGA package, the silicon is placed inside the package and copper wires connect the bond pads to the solder balls of the package. Figure 5–3 shows a cross section of a wirebond BGA package.

For a list of all BGA packages available for each Altera FPGA device, refer to the *Altera Device Package Information Datasheet*.

Figure 5–3. Wire Bond BGA

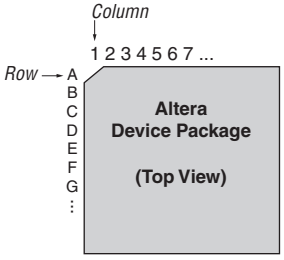


Package Pins

The pins of a BGA package are small solder balls arranged in a grid-like pattern on the bottom of the package. In the Quartus II software, the package pins are represented as pin numbers. The pin numbers are determined by their locations using a coordinate system with the letters and numbers identifying the row and column of the pins, respectively.

The upper-most row of pins is labeled "A" and continues alphabetically as you move downward (Figure 5–4). The left-most column of pins is labeled "1" and continues with increments of 1 as you move to the right. For example, pin number "A1" represents row "A" and column "1."

Figure 5–4. Row & Column Labeling



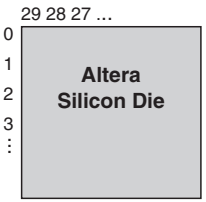
The letters I, O, Q, S, X, and Z are never used in pin numbers. If there are more rows than letters of the alphabet, then the alphabet is repeated, prefixed with the letter "A."

For more information about the pin numbers for your Altera device, refer to the device pin-outs available on the Altera website, **www.altera.com**.

Pads

Package pins are connected to pads located on the perimeter of the top metal layer of the silicon die (Figure 5–3). Each pad is identified by a pad ID, which is numbered starting at 0, incrementing by 1 in a counter clockwise direction (Figure 5–5).

Figure 5–5. Pad Number Ordering



To prevent any signal integrity issues, the Quartus II software uses pin placement rules to validate your pin placements and pin-related assignments. It is important to understand which pad locations your pins were assigned, since some pin placement rules describe pad placement restrictions. For example, in certain devices, there is a restriction on the number of I/O pins supported by a VREF pad to ensure signal integrity. There are also restrictions on the number of pads between single-ended input or output pins and a differential pin. The Quartus II software performs pin placement analysis, and if pins are not placed according to pin placement rules, the design compilation fails and the Quartus II software generates an error report.

For more information on pin placement guidelines, refer to the *Design Consideration* section of the *Selectable I/O Standards* chapter in volume 1 of the appropriate device handbook.

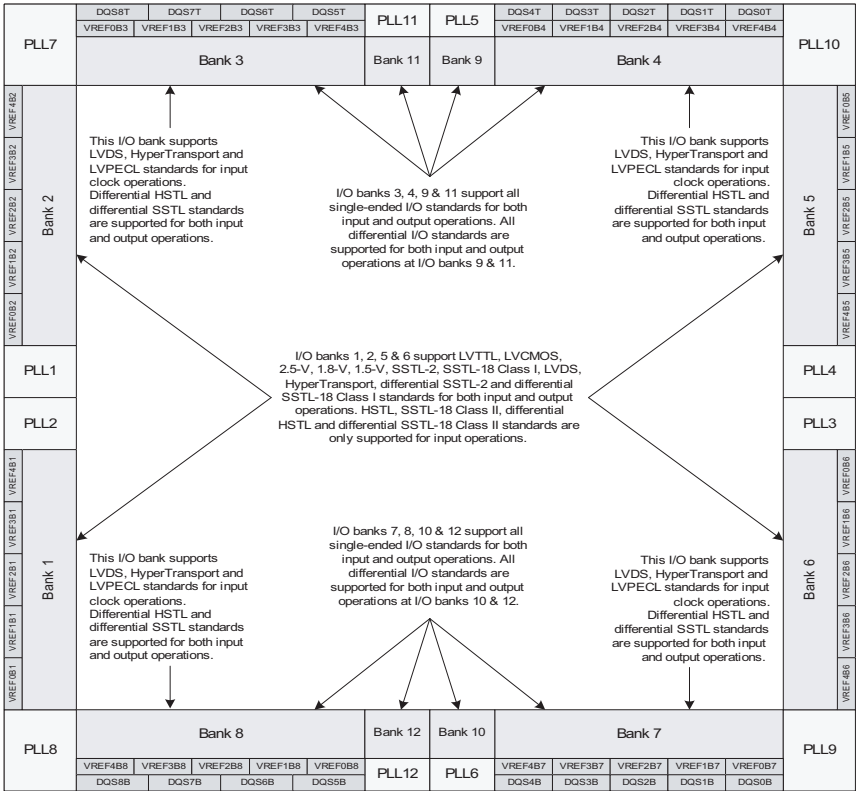
I/O Banks

I/O pins are organized into I/O banks designed to facilitate the various supported I/O standards. Each I/O bank is numbered and has its own voltage source pins, called VCCIO, to offer the highest I/O performance. Depending on the device and I/O standards for the pins within the I/O bank, the specified voltage of the VCCIO pin is between 1.5 V and 3.3 V. Each I/O bank can support multiple pins with different I/O standards that share the same VCCIO.

It is important to refer to the appropriate device handbook to determine the capabilities of each I/O bank. For example, the pins in the I/O banks on the left and right side of a Stratix® II device support high-speed I/O

standards such as LVDS, whereas the pins on the top and bottom I/O banks support all single-ended I/O standards, including DQS signaling (Figure 5–6). Pins belonging to the same I/O bank must use the same VCCIO signal.

Figure 5–6. Stratix II I/O Banks *Notes (1), (2), (3), (4)*



Notes to Figure 5–6:

(1) Figure 5–6 is a top view of the silicon die which corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(2) Depending on size of the device, different device members have different number of VREF groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high speed differential I/O standards. For more information on differential I/O standards, refer to the *High Speed Differential I/O Interfaces in Stratix II Devices* chapter in volume 2 of the *Stratix II Device Handbook*.

VREF Groups

A VREF group is a group of pins that includes one dedicated VREF pin as required by voltage-referenced I/O standards. A VREF group is made up of a small number of pins, compared to the I/O bank, in order to maintain the signal integrity of the VREF pin. One or more VREF groups exist in an I/O bank. Each pin in a VREF group shares the same V_{CCIO} and V_{REF} voltages.

For more information about I/O banks, VREF groups, and supported I/O standards, refer to the *Architecture and Selectable I/O Standards* chapters in volume 1 of the appropriate device handbook.

Importing & Exporting Pin Assignments

You can transfer pin-related assignments between the Quartus II software and other tools by importing and exporting these assignments in the following file formats: Comma Separated Value (**.csv**) file, Quartus II Settings File (**.qsf**), Tool command language (Tcl), FPGA Xchange (**.fx**) file, and Pin-Out (**.pin**) file which can only be exported.

Comma Separated Value File

You can transfer pin-related assignments as a Comma Separated Value file. This file consists of a row of column headings followed by rows of comma-separated data. The row of column headings are in the same order and format as the columns displayed in the Assignment Editor when the export was performed. Do not modify the row of column headings if you plan to import the Comma Separated Value file later.

To import a Comma Separated Value file into your project, on the Assignment menu, click **Import Assignments** and browse to the file.

To export your pin related assignments to a Comma Separated Value file, on the Assignment menu, click **Assignment Editor**, select the **Pin category** from the **Category** list, and on the File menu, click **Export**.

The Pin category displays detailed properties about each pin of the device, similar to the device pin-out files (available on the Altera website at **www.altera.com**) in addition to the pin name and pin number.

For more information on importing and exporting Comma Separated Value files and the Assignment Editor, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Quartus II Settings Files

You can transfer pin-related assignments as a Quartus II Settings File. The pin-related assignments are stored as Tcl commands in the Quartus II Settings File.

To import a Quartus II Settings File, on the Assignments menu, click **Import Assignments** and browse to the file. You can also import a Quartus II Settings File by sourcing the file in the Tcl console. To export a Quartus II Settings File, on the Assignments menu, click **Export Assignments**, type in a file name, and click **OK**.

For more information on Quartus II Settings Files, refer to the Quartus II *Project Management* chapter in volume 2 of the *Quartus II Handbook*.

Tcl Script

To import the pin-related assignments from a Tcl script, source the Tcl script in the Tcl console or run the Tcl script with the `quartus_sh` executable. For example:

```
quartus_sh -t my_pins.tcl ↵
```

To export pin-related assignments as a Tcl script, on the Assignments menu, click **Assignment Editor**, select the **Pin category** from the **Category** list and on the File menu, click **Export**. In the **Export** dialog box, type in a file name, select **Tcl Script File** (***.tcl**), and click **OK**. All pin-related assignments displayed in the spreadsheet of the Assignment Editor are saved as Tcl commands in the Tcl script.

For more information on Quartus II scripting support, including examples, refer to the *Tcl Scripting* and *Command-Line Scripting* chapters in volume 2 of the *Quartus II Handbook*.

FPGA Xchange File

An FPGA Xchange file contains device and pin-related information that allows you to transfer information between the Quartus II software and your PCB schematic or design tool. For example, you can use an FPGA Xchange file to transfer pin information from the Mentor Graphics I/O Designer software to the Quartus II software to validate the these pin assignment using the I/O Assignment Analyzer.

To import an FPGA Xchange file into the Quartus II software, perform the following steps:

1. On the Assignments menu, click **Import Assignments**.
2. In the **File name** box, click **Browse** and click FPGA Xchange Files **(*.fx)** from the **Files of type** list.
3. Browse to and select the F**PGA Xchange** file and click **Open**.
4. Click **OK**.

To generate an FPGA Xchange file in the Quartus II software, perform the following steps:

1. Complete an I/O Assignment Analysis or a fit.
2. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
3. In the **Category** list in the EDA Tool Settings, select **Board-Level**. In the **Tool name** list, select **Symbol Generation (FPGA Xchange)**.
4. Click **OK**.
5. On the Processing menu, point to Start and click **Run EDA Netlist Writer**. The FPGA Xchange file is located in the newly created **/board/fpgaxchange** directory.

Pin-Out File

A Pin-Out file is an ASCII text file containing pin location results and other pin information. To generate a pin file for your project, you must successfully complete an I/O Assignment Analysis or fit.

Use the pin file to understand which signals should be connected with which pins. You can also use the Pin-Out file to transfer the pin information of your project into third-party PCB tools for board development. Table 5–1 describes each header of the Pin-Out file, and Figure 5–7 is an example of a Pin-Out file.

Table 5–1. Pin-Out File Header Description (Part 1 of 2)

Column Name	Description
Pin Name/Usage	The name of a design pin, ground or power
Location	The pin number of the location on the device package

Table 5–1. Pin-Out File Header Description (Part 2 of 2)

Column Name	Description
Dir	The direction of the pin
I/O Standard	The name of the I/O standard that the pin is configured to
Voltage	The voltage level that is required to be connected to this pin
I/O Bank	The I/O bank number that the pin belongs to
User Assignment	Y or N indicating if the location assignment for the design pin was user assigned (Y) or assigned by the Fitter (N)

Figure 5–7. Example of a Pin-Out File

Pin Name/Usage	Location	Dir.	I/O Standard	Voltage	I/O Bank	User Assignment
VCCA_PLL1 clk	9 10	power input	 LVTTL	1.5V	 1	 N

For more information on the Pin Name/Usage, refer to the Device Pin-Out for the targeted device, available on the Altera website at **www.altera.com**.

For more information on using Cadence PCB tools with the Quartus II software, refer to the *Cadence PCB Design Tools Support* chapter in volume 2 of the *Quartus II Handbook*. For more information on using the Mentor Graphics PCB tools with the Quartus II software, refer to the *Mentor Graphics PCB Design Tools Support* chapter in volume 2 of the *Quartus II Handbook*.

Creating Pin-Related Assignments

A pin-related assignment is any assignment applied to a pin. An example of a pin-related assignment is a pin location assignment that assigns design pin to pin number/location on the targeted device. Other pin-related assignments include assigning an I/O standard or current drive strength to a pin.

You can make pin-related assignments at any time during the design cycle, even before any design files have been developed. The accuracy and completeness of the pin-related assignments determines the accuracy of the I/O assignment analysis. If you do not have design files, create reserved pins to temporarily represent your top-level design I/O pins until the I/O pins are defined in your design files. If you do not have design files in your project, create an empty Verilog HDL or VHDL file with all the ports of the design defined.

Reserved pins are pins that you reserve for future use but do not currently perform a function in your design. Reserved pins require a unique pin name and a pin location. Using reserved pins as place holders for a future design pins increases the accuracy of the I/O assignment analysis.

The Quartus II software offers many tools and features for creating reserved pins and other pin-related assignments (Table 5–2).

Table 5–2. Overview of Quartus II Tools & Features Used to Create Pin-Related Assignments

Feature	Overview
Pin Planner	• Make pin location assignments to one or more node names by dragging and dropping unassigned pins into the package view • Edit pin location assignments for one or more node names by dragging and dropping groups of pins within the package view • Visually analyze pin resources in the package view • Display I/O banks and VREF groups • View the function of package pins using the pin legend • Make correct pin location decisions by referring to the Pads view
Assignment Editor	• Create and edit all types of pin-related assignments • Create and edit multiple assignments simultaneously with the **Edit** bar • Efficiently create pin assignments by viewing the different font styles used to display assigned and unassigned node names, as well as occupied and available pin locations. • Provides user selectable information about each pin including the pad number the t_{CO} requirement, and the t_H requirement)
Tcl	• Create any pin-related assignments for multiple pins • Store and reapply all pin-related assignments with Tcl scripts • Make assignments from the command line
Timing closure Floorplan	• Create and change pin locations by dragging and dropping pins into the floorplan • Make correct pin location decisions by referring to the pad ID number and spacing • Display I/O banks, VREF groups, and differential pin pairing information
Synthesis Attributes	• Embed pin-related assignments using attributes in the design files to pass assignments to the Quartus II software

Pin Planner

Use the Pin Planner package view to make pin location assignments using a device package view instead of pin numbers. With the Pin Planner, you can identify I/O banks, VREF groups, and differential pin pairings to help you through the I/O planning process.

For more information on using the Pin Planner, refer to "Using the Pin Planner" on page 5–18.

Assignment Editor

The Assignment Editor provides a spreadsheet-like interface that allows you to create and change all types of assignments, including pin-related assignments.

Assigning Pin Locations Using the Assignment Editor

Use one of two methods for making pin assignments with the Assignment Editor. The first approach involves selecting from all assignable pin numbers of the device and assigning a pin name from your design to this location.

The second approach involves selecting from all pin names in your design and assigning a device pin number to the design pin name. In either method, select **Pin** from the **Category** bar to take advantage of the row background coloring (pin numbers within the same I/O bank have a common background color), auto fill node names, and pin numbers.

Setting Pin Locations From the Device Pin Number List

It is important to understand the properties of the pin number before you assign a location to each pin in your design. For example, you need to know which I/O bank or VREF group the pin number belongs to when following pin placement guidelines.

For more information on pin placement guidelines, refer to the appropriate device handbook.

Before creating pin-related assignments, start Analysis and Elaboration or Analysis and Synthesis on your design to create a database of your design pin names, perform the following steps:.

1. In the Quartus II software, on the Assignments menu, click **Assignment Editor** to open the Assignment Editor.

2. Select **Pin** in the **Category** bar.

   Creating pin assignments can be difficult when you need to check which I/O bank the pin number is in, or which VREF pad the pin uses. By selecting the **Pin** category, more pin-related information is visible in the spreadsheet to help you create pin location assignments.

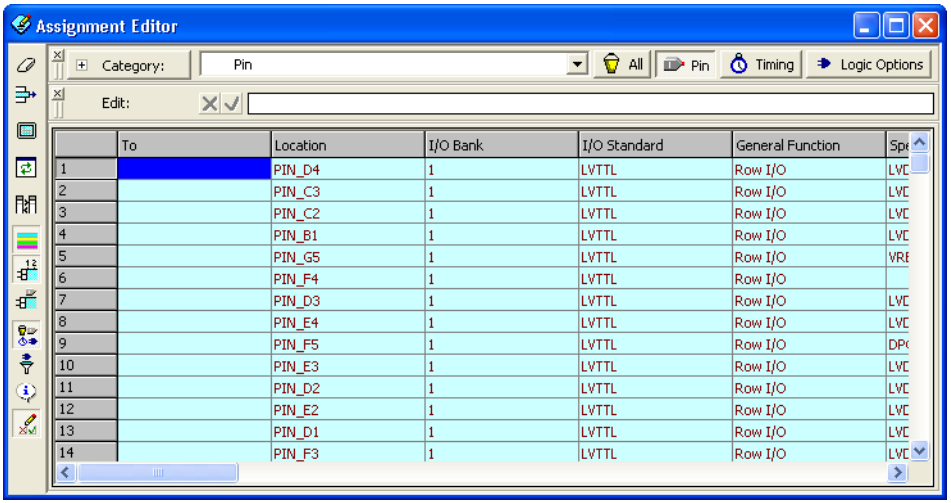
   

   The Assignment Editor does not show assignments to individual nodes made with wildcards or assignment groups.

3. On the View menu, click **Show All Assignable Pin Numbers**.

   A list of all assignable pin numbers for the targeted device displays in the **Location** column (Figure 5–8).

Figure 5–8. Assignment Editor with Show All Assignable Pin Numbers



4. Find a pin number in the spreadsheet and in the same row, double-click on the cell in the **To** column. Type the pin name or select a pin from the drop-down arrow. If analysis and elaboration has been performed, your design pins are listed in the drop-down arrow.

   As you type in a pin name, the Assignment Editor automatically completes the field by referencing the pin names stored in the database created from the initial analysis and elaboration. Pin names already assigned to a pin location are shown in italics.

Setting Pin Locations from the Design Signal Name List

It is important to understand the properties of the pin location before assigning the location to each pin in your design. For example, you need to know which I/O bank or VREF group the pin number belongs to when following pin placement guidelines.

For more information on pin placement guidelines, refer to the appropriate device handbook.

To set the pin locations from the **design pin name** list, perform the following steps:

1. On the Assignments menu of the Quartus II software, click **Assignment Editor** to start the Assignment Editor.

2. Select **Pin** from the **Category** bar.

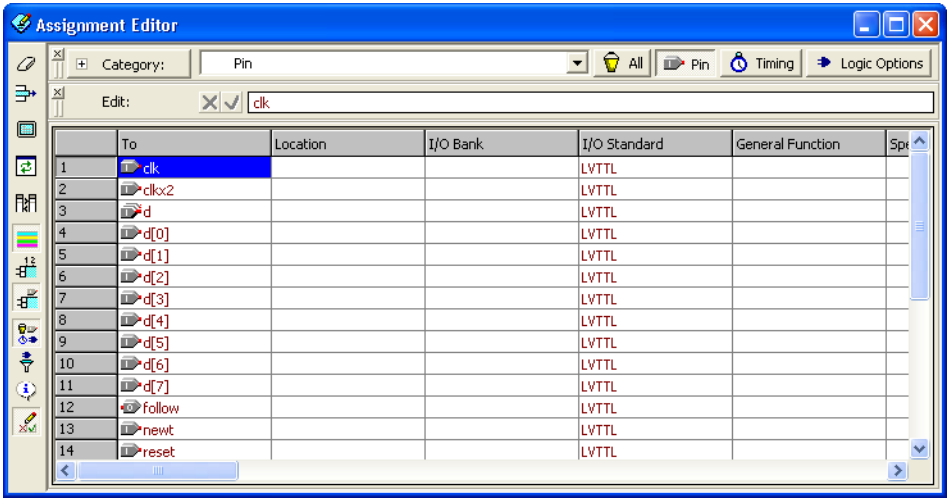
   It can be difficult to make pin assignments because you must check which I/O bank the pin number belongs to, or which VREF pad the pin uses. By selecting the **Pin** category, more pin-related information is visible in the spreadsheet to help you create pin location assignments.

   The Assignment Editor does not show assignments to nodes made with wildcards or timegroups.

3. On the View menu, click **Show All Known Pin Names**.

   A list of all pin names in your design is shown in the **To** column (Figure 5–9).

Figure 5–9. Assignment Editor with Show All Known Pin Names



To list a selection of pin names from your design into the spreadsheet of the Assignment Editor, type the pin names with or without wild cards into the **Node Filter** bar. This is effective when you want to assign common pin-related assignments to a selection of pins in your design.

For more information on using the **Node Filter** bar, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

4. Find a pin name in the spreadsheet, and double-click the **Location** cell in the same row. Select a pin number from the drop-down arrow containing all assignable pin numbers in the selected device. You can also type the pin number and let the Assignment Editor automatically complete the pin number.

Instead of typing `Pin_AA3`, you can type `AA3` and let the Assignment Editor auto complete the pin number to `Pin_AA3`.

Pin locations that already have a pin name assignment appear in italics.

For more information on using the Assignment Editor, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Tcl Scripts

Tcl scripting allows you to write scripts to create pin-related assignments. To run a Tcl script with your project, use the `quartus_sh` executable:

```
quartus_sh -t my_tcl_script.tcl ↵
```

You can also type individual Tcl commands into the Tcl console window. On the view menu, point to Utility Windows and click **Tcl Console**. In the Tcl Console window, type your Tcl commands. The following example shows a list of Tcl commands that creates pin related assignments to the input pin `address[10]`.

```
set_location_assignment Pin M20 -to address[10] "Address pin to Second FPGA"
set_instance_assignment -name IO_STANDARD "2.5 V" -to address[10]
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to address[10]
```

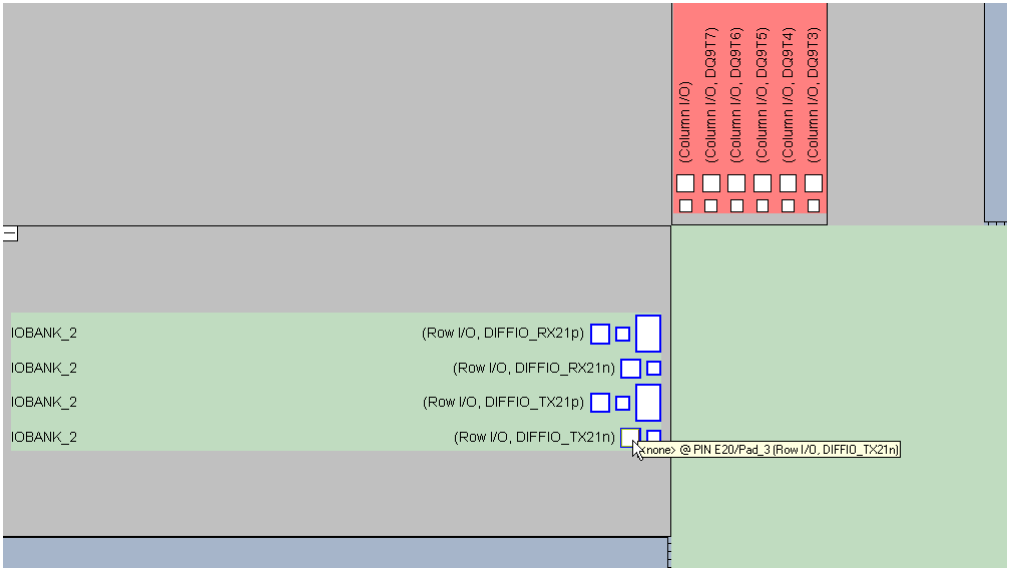
For more information on using Tcl scripts to create pin-related assignments, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Timing Closure Floorplan

The Timing Closure Floorplan shows the pins in the same order as the pads of the device. Understanding the relative distance between a pad and related logic can help you meet your timing requirements. You can also use the Timing Closure Floorplan to find the distances between user I/O pads and VCC, GND, and VREF pads to avoid signal integrity issues (Figure 5–10).

For more information about pin placement guidelines, refer to the *Selectable I/O Standards* chapter of the appropriate device handbook.

Figure 5–10. Timing Closure Floorplan of EP1C6F256I7



To create a pin location assignment with the Timing Closure Floorplan perform the following steps:

1. On the View menu, point to Utility windows, and **click Node Finder**. The **Node Finder** dialog box appears.
2. Select a design pin name in a design file, or highlight the text of the Timing Closure Floorplan.
3. Drag the selection into a pin location.

For more information on using the Timing Closure Floorplan, refer to the *Timing Closure Floorplan* chapter in volume 2 of the *Quartus II Handbook*.

Synthesis Attributes

Synthesis attributes allow you to embed assignments in your HDL code. The Quartus II software reads these synthesis attributes and translates them into assignments. The Quartus II integrated synthesis supports the `chip_pin`, `useioff`, and `altera_attribute` synthesis attributes.

For more information on integrated synthesis, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

For synthesis attribute support by third-party synthesis tools, contact your vendor.

chip_pin & useioff

You can use the `chip_pin` and `useioff` synthesis attributes to embed pin location and fast output/input register assignments, respectively. For all other assignments, including pin-related assignments, use the `altera_attribute` synthesis attribute as discussed in "altera_attribute" on page 5–18.

Synthesis attributes translated into assignments are stored in the database and take precedence over other assignments in the Quartus II Settings File. The following examples embeds a location and fast input assignment into both a Verilog HDL and VHDL design file using the `chip_pin` and `useioff` synthesis attributes.

Verilog HDL Example

```
input my_pin1 /* synthesis chip_pin = "C1" useioff = 1 */;
```

VHDL Example

```
entity my_entity is
        port(
                    my_pin1: in std_logic
        ;
end my_entity;

attribute useioff : boolean;
attribute useioff of my_pin1 : signal is true;
attribute chip_pin : string;
attribute chip_pin of my_pin1 : signal is "C1";
```

altera_attribute

To create other pin-related assignments, use the `altera_attribute` attribute. The `altera_attribute` is understood only by the Quartus II integrated synthesis and supports all types of instance assignments. The following examples use the `altera_attribute` to embed the fast input register and I/O standard assignments into both a Verilog HDL and a VHDL design file.

Verilog HDL Example

```
input my_pin1  /* synthesis altera_attribute = "-name FAST_INPUT_REGISTER ON;
-name IO_STANDARD \"2.5 V\" " */ ;
```

VHDL Example

```
entity my_entity is
        port)
                        my_pin1: in std_logic
        );
end my_entity;

attribute altera_attribute : string;
attribute altera_attribute of my_pin1: signal is "-name
FAST_INPUT_REGISTER ON; -name IO_STANDARD \"2.5 V\"" ;
```

For detailed information on using synthesis attributes and their usage syntax, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

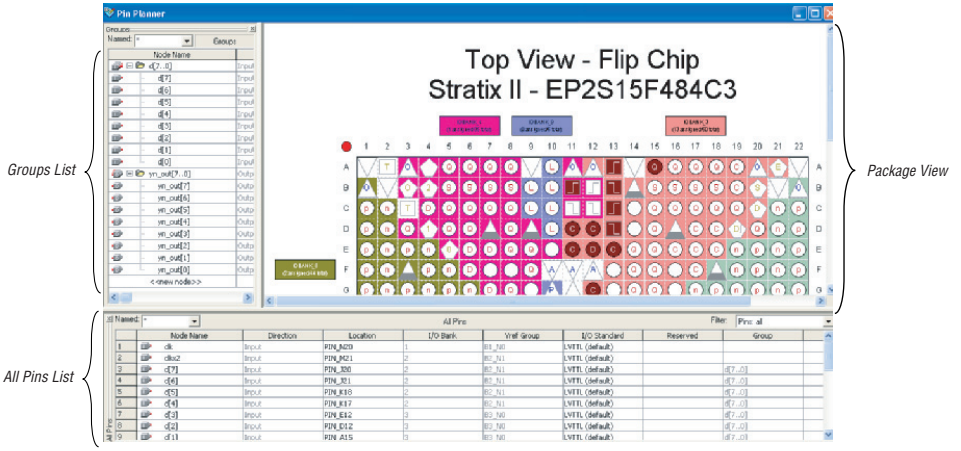
Using the Pin Planner

When planning your I/Os, it can be cumbersome to correlate pin numbers with their relative location on the package and their pin properties. The Pin Planner provides an intuitive graphical representation of the targeted device, also known as the package view, making it easy to plan your I/Os, create reserved pins, and make pin location assignments. When deciding on a pin location, you can use the Pin Planner to gather information about available resources, the functionality of each individual pin, I/O bank, and VREF group. You can assign locations to design pins by dragging and dropping each pin into the Package view.

Maintaining signal integrity (SI) requires that you follow pad distance and pin placement rules. Complementing the Pin Planner is the Pad View which displays the pads in order around the silicon die.

The Pin Planner includes the following sections: Package view, **All Pins** list, **Groups** list, and a Pad View window. Refer to Figures 5–11 through 5–15).

Figure 5–11. Pin Planner



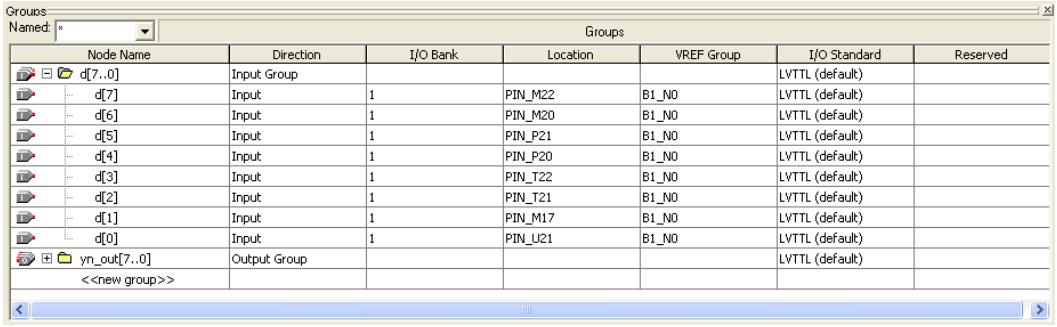
The Pin Planner feature supports cross-probing, allowing you to select a pin in one view, simultaneously highlighting the pin in all of the different views. For example, if you select a pin in the package view of the Pin Planner, the corresponding pad in the Pad View window is highlighted, and if the pin has an assigned node name, the node name in the **All Pins** list and the **Groups** list is highlighted.

Groups List

The **Groups** list displays all the buses from the top level ports of your design and all the assignment groups in your project (Figure 5–12). You can also filter the group names displayed by typing in a wild card filter into the **Named** list. The **Groups** list allows you to create your own custom groups of pins and make location assignments to groups by dragging them into the package view of the Pin Planner.

In the **Groups** list, all members of an assignment group are displayed regardless if the member is a pin or an internal node.

Figure 5–12. Groups List



To add a new group to the **Groups** list, perform the following steps:

1. In the **Node Name** column, double-click **<<***new group***>>**.
2. Type the group name.
3. Press **Enter**. The **Add Members** dialog box appears.
4. Type node names, wild cards, and assignment groups in the **Members** box, or browse to and select the node names from the **Node Finder** dialog box.
5. Click **OK**.

For more information on using Assignment Groups, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

You can also create a new group by selecting one or more node name within the **Groups** list or **All Pins** list and click **Add to Group** on the right-click menu.

As you plan your I/O placement, you may decide to add and remove members from a group.

To add a member to a group in the **Groups** list, perform the following steps:

1. On the Assignment menu, select **Assignment Groups**. The **Assignment Groups** dialog box appears.
2. Right-click a group name from the **Groups** list.

3. Select **Add Members** on the right-click window.

4. Type in the name of the member or click **browse** to select one or more nodes from the **Node Finder** dialog box.

To remove a member from a group in the **Groups** list, perform the following steps:

1. Expand the group where you want to remove a member.

2. Select one or more members that you want to remove.

3. Right-click the selected members, point to Edit and click **Delete**

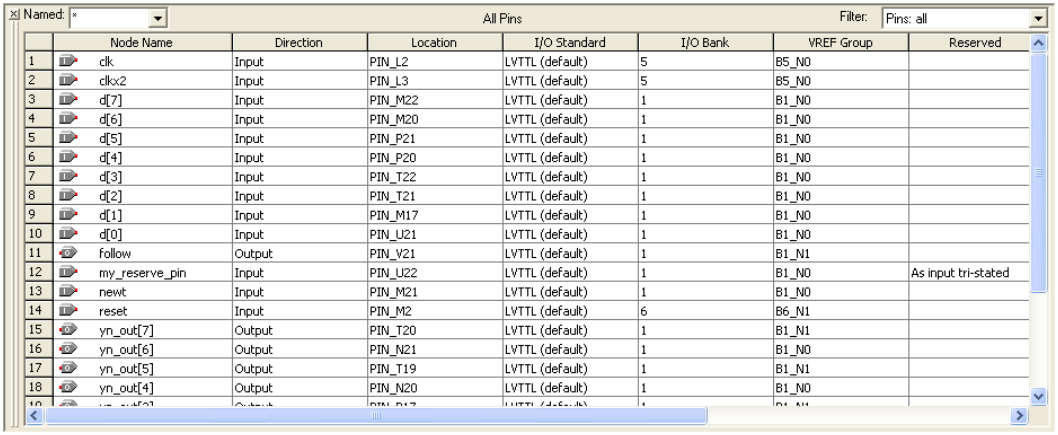
The **Groups** list provides many columns, some for information purposes and others to make assignments. The only editable cells in addition to the **Node Name** column are the Location, I/O Standard, and reserved cells. The other columns provide useful information during I/O planning, including the I/O Bank number, VREF group, and the direction. To show or hide a column, right-click the column and click **Customize Columns**. You can also reorder and sort the columns from this menu.

If an assignment group contains pins with different directions, the direction of the assignment group is a `bidir` group.

All Pins List

The **All Pins** list displays all the pins in your design including user-created pins (Figure 5–13). The **All Pins** list does not display buses; instead it displays each individual pin of the bus. You must complete an Analysis and Elaboration to display pins in your design in the **All Pins** list. Individual user-reserved pins and nodes with pin-related assignments are always shown in the **All Pins** list.

Figure 5–13. All Pins List



	Node Name	Direction	Location	I/O Standard	I/O Bank	VREF Group	Reserved
1	clk	Input	PIN_L2	LVTTL (default)	5	B5_N0	
2	clkx2	Input	PIN_L3	LVTTL (default)	5	B5_N0	
3	d[7]	Input	PIN_M22	LVTTL (default)	1	B1_N0	
4	d[6]	Input	PIN_M20	LVTTL (default)	1	B1_N0	
5	d[5]	Input	PIN_P21	LVTTL (default)	1	B1_N0	
6	d[4]	Input	PIN_P20	LVTTL (default)	1	B1_N0	
7	d[3]	Input	PIN_T22	LVTTL (default)	1	B1_N0	
8	d[2]	Input	PIN_T21	LVTTL (default)	1	B1_N0	
9	d[1]	Input	PIN_M17	LVTTL (default)	1	B1_N0	
10	d[0]	Input	PIN_U21	LVTTL (default)	1	B1_N0	
11	follow	Output	PIN_V21	LVTTL (default)	1	B1_N1	
12	my_reserve_pin	Input	PIN_U22	LVTTL (default)	1	B1_N0	As input tri-stated
13	newt	Input	PIN_M21	LVTTL (default)	1	B1_N0	
14	reset	Input	PIN_M2	LVTTL (default)	6	B6_N1	
15	yn_out[7]	Output	PIN_T20	LVTTL (default)	1	B1_N1	
16	yn_out[6]	Output	PIN_N21	LVTTL (default)	1	B1_N0	
17	yn_out[5]	Output	PIN_T19	LVTTL (default)	1	B1_N1	
18	yn_out[4]	Output	PIN_N20	LVTTL (default)	1	B1_N0	

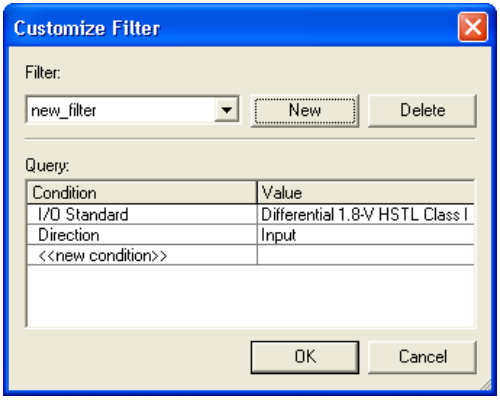
You can filter the list of pins in the **All Pins** list based on their node names by typing in a portion of the pin name in combination with wild card characters in the **Named** list. You can also filter the list of pins in the **All Pins** list based on the pins' attributes by selecting from the **Filter** list.

You can also create your own custom filter in the **Filter** list, where you can specify a set of conditions from the list below:

- Assigned or unassigned
- Current strength
- Direction
- Edge location
- I/O Bank location
- I/O Standard
- VREF Group

To create a new filter in the **All Pins** list, select <<*new filter*>> from the **Filter** list in the **All Pins** list. The **Customize Filter** dialog box appears (Figure 5–14).

Figure 5–14. Customized Filter Dialog Box



To create a custom filter for the **All Pins** list, perform the following steps:

1. In the **Customize Filter** dialog box, click **New**. The **New Filter** dialog box appears.
2. Enter the name of your custom filter in the **Filter name** text box.
3. You can base your new custom filter on existing filters by selecting from the **Based on Filter** list. If you do not want to base your custom filter on any other filter, select **Pins:** all from the Based on **Filter** list.
4. Click OK.
5. Add as many conditions as you like to the **Query** list. To add a condition, double-click <<*new condition*>> and from the **Condition** list. Select a value by double-clicking the cell next to your condition under the **Value** column.

To remove a condition from your filter, right-click the condition in the **Query** list and select **delete**.

After specifying your conditions, the pins meeting the specified conditions are the only pins shown in the **All Pins** list. If the set of conditions contains a condition with more than one value, then the pins displayed must meet at least one of the values for that multiple-value condition.

To edit an existing custom filter, select <<*new filter*>> from the **Filter** list in the **All Pins** list. In the **Customize Filter** dialog box, select the custom filter you want to edit from the **Filter** list and add and remove conditions to the **Query** list.

Pins generated from a compilation or from a bus group are not editable. All other user-created pins are editable.

The **All Pins** list provides many columns, some for information purposes and others to make assignments. To show or hide a column, right-click the column heading and select **Customize Columns**. In addition, you can reorder and sort the columns from this menu.

Pad View

To maintain high signal integrity in designs, use the Pad View to guide your pin placement decisions. Each device family is accompanied with pin placement rules including pad spacing between various pin types.

For more information on pin placement rules, refer to the appropriate device handbook.

You can edit or make pin assignments in the Pad View by dragging and dropping a design pin into an available pad location.

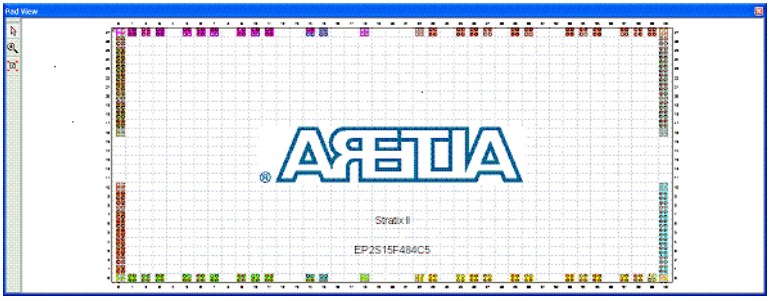
When you drag and drop a design pin into an available pad location, the corresponding pin number of the pad is assigned to the design pin. To assign a Pad number to the design pin, perform the following steps:

1. On the Tools menu, click **Options**. The **Options** dialog box appears.
2. Click **Pin Planner** and turn on **Create pad assignment** in the Pad View window.

The column and row numbering around the Pad View helps identify which pad row or pad column each pad is in. This is useful when the pin placement guidelines for your targeted device, refer to pad rows and columns.

Since the pad view is the view of the I/O ring of the silicon within the package, for flip chip packages, the Pad View appears flipped (The ALTERA logo appears flipped) as shown in Figure 5–15. To understand the correlation between the package pins and the pads on the silicon die, the Pad View window and Package View are closely integrated together. When a pad is selected, the corresponding pin in the package view is highlighted. This is also true when a pin is selected in the package view, the corresponding pad is highlighted in the Pad View window.

Figure 5–15. Pad View, of a Stratix II Flip Chip Device

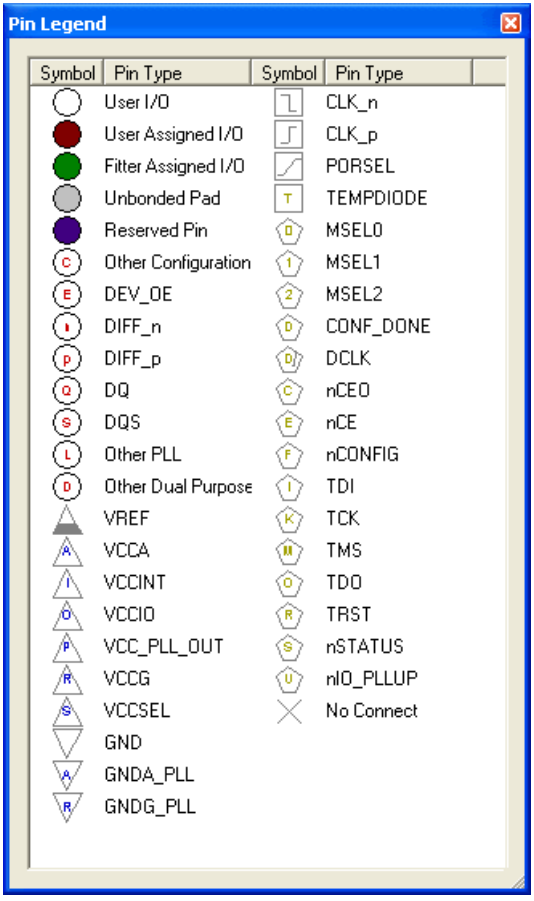


Package View

The package view in the Pin Planner uses pin symbols as a visual representation of the actual package (Figure 5–11). The package view eliminates the need to cross-reference each pin number with it's physical location on the package described in the device package datasheet. When making pin location assignments in the Package view, switch between the different views to help you decide on a pin location. The different views in the Package view include I/O banks, VREF groups, Edges, DQ/DQS pins, and differential pin pairs. For more information on the different views in the Package view refer to the "Using the Pin Planner" on page 5–18.

For more information on each of the pin symbol, refer to the Pin Legend window. To view the Pin Legend window, on the View menu, click **Pin Legend** (Figure 5–16).

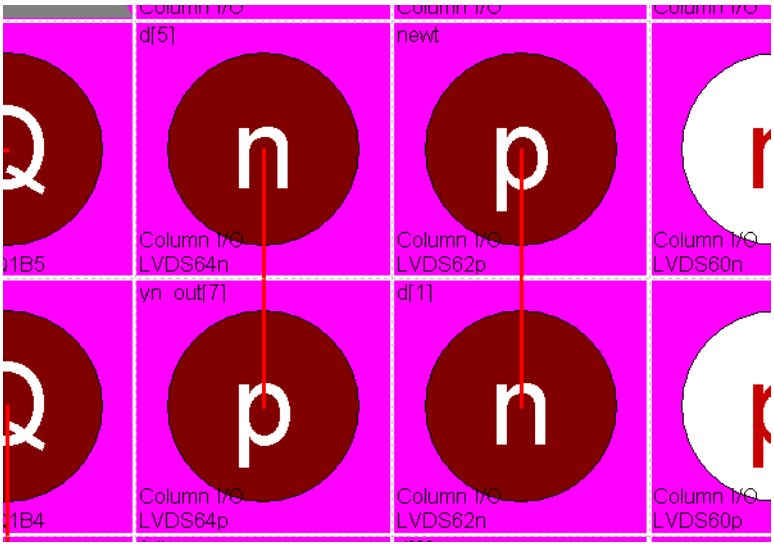
Figure 5–16. Pin Legend Window



Planning your I/Os along with your board is necessary in today's market. If your FPGA device is oriented differently than how it appears in the package and pad view of the pin planner, rotate the package view. To rotate the package view, on the View menu, click **Rotate Left 90°** and **Rotate Right 90°** until your FPGA is shown in the desired orientation in the Package view. The red dot in the package view indicates the location of the first pin. For example, the red circle identifies where Pin A1 is located for a BGA package and Pin 1 for a TQFP package.

You can also print the package view and show pin names and pin types (Figure 5–17). To show the pin name, if available, or pin type for each pin in the package view, on the View menu, click **Show Pin Names** and **Show Pin Types**.

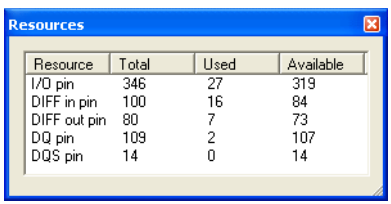
Figure 5–17. Package View with Show Pin Names & Show Pin Types



To view pin resource usage, on the View menu, click **Resources**. The **Resources** dialog box appears (Figure 5–18).

For more detailed information on resources, view the Resource section of the Compilation Report.

Figure 5–18. Resources Window



If a HardCopy® II companion device is selected, the Pin Planner shows the package view for the Stratix II device. In order to ensure correct pin migration between the Stratix II and HardCopy II devices, run the I/O Assignment Analysis command or the fitter.

If a migration device is selected, the Pin Planner shows only pins that are available for migration. Selecting a migration device allows you to either vertically migrate to a different density while using the same package, or migrate between packages with different densities and ball counts.

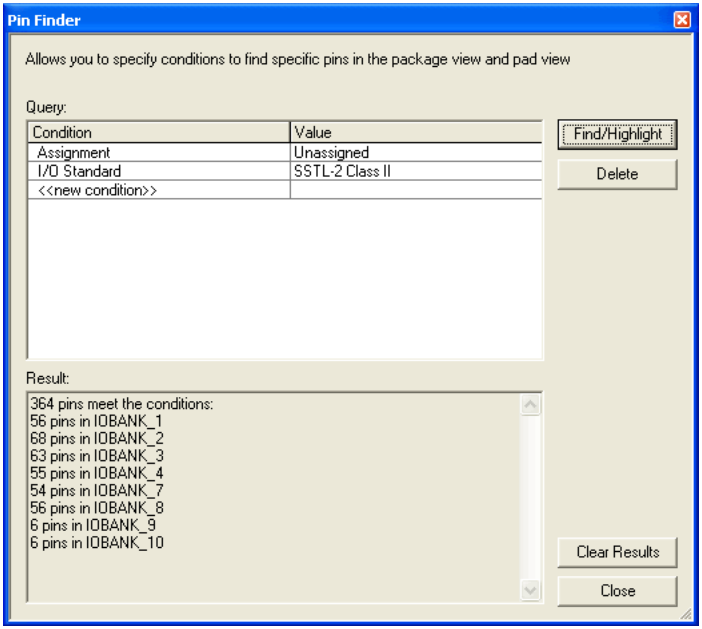
For more information about migration, refer to Alter application note, *AN90 SameFrame Pin-Out Design for FineLine BGA Packages*. For more information on designing for the HardCopy II devices, refer to the *Quartus II Support for HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook*.

Using the Pin Finder to Find Compatible Pin Locations

As FPGA pin-counts and I/O capabilities continue to increase, it is becoming more difficult to understand the capabilities of each I/O and to correctly assign your design I/Os. To help alleviate this problem, the Pin Planner highlights all pins that match the list of conditions that you entered. To enter your conditions, perform the following steps with the Pin Planner open:

1. On the View menu, click **Pin Finder.** The Pin Finder window is shown (Figure 5–19).

Figure 5–19. Pin Finder Window



2. In the Pin Finder window, create a list of conditions in the **Query** list.

   To add a condition to the **Query** list, double-click <<*new condition*>>, select a condition from the list, double-click the cell next to it, and then select the appropriate value. For example, to highlight all available pins that support the SSTL-2 Class II I/O standard, create an assignment condition and an I/O standard condition as shown in Figure 5–19.

   If you add the same condition type more than once, the Pin Finder searches for results that match any of the specified values. If you add more than one condition type, the Pin Finder searches for results that match all of the specified conditions.

3. In the Pin Finder window, click **Find/Highlight.** All of the pins that meet the specified conditions are highlighted in the Package view and in the Pad View window.

   Also in the **Results** list, a summary of the number of pins in each I/O Bank that meet the specified conditions are shown.

Creating Reserved Pin Assignments

Make reserved pin assignments to act as place holders for future design pins. To create a reserved pin in the Pin Planner **All Pins** list, perform the following steps:

1. Right-click on an available pin in the Package View.
2. On the right-click menu, point to reserve, and click on one of the available configurations.

When you reserve a pin from the Package view, the name of the reserved pin defaults to `user_reserve_`<*number*> and the pin symbol is filled with a dark purple color. The number increments by 1 for each additional reserve pin.

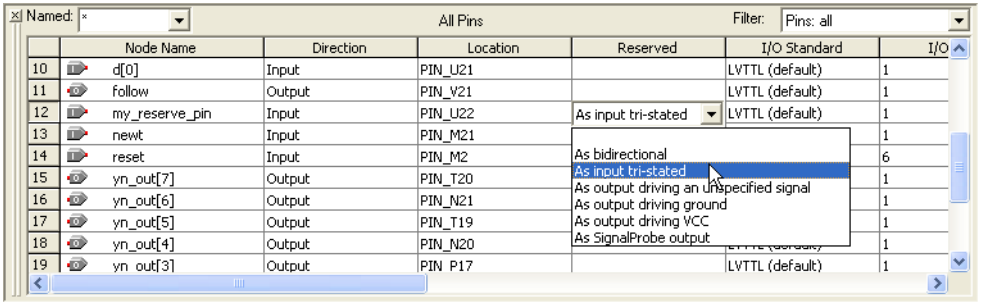
Alternately, you can also reserve a pin from the **All Pins** list

1. Type the pin name into an empty cell in the **Node Name** column. The pin name must not exist in your design.
2. Select a pin configuration from the **Reserved** list (Figure 5–20).

   The following configurations are available:

   - As bidirectional
   - As input tri-stated
   - As output driving unspecified signal
   - As output driving ground
   - As output driving VCC
   - As SignalProbe output

Figure 5–20. Reserving a Pin in the All Pins List



Release reserved pins by selecting the blank entry from the **Reserved** list.

The **Direction** column is a read-only column and changes direction depending on the reserved selection.

Creating Pin Location Assignments

You can create pin locations to one or more pins with the following methods:

- Assigning a location for unassigned pins
- Assigning a location for differential pins
- Assigning an unassigned pin to a pin location

Assigning Locations for Unassigned Pins
To assign locations for all of your design pins, perform the following steps:

1. On the Edit menu, select an assignment direction.

   You can assign several pins simultaneously by choosing an assignment direction (Table 5–3). When assigning an entire bus, assignments are made in order from the most significant bit to the least significant bit.

Table 5–3. Multiple Pins

Assignment	Pin Group
Assign Down	From the selected group of unassigned pins, assign each pin downwards starting from the selected pin.
Assign Up	From the selected group of unassigned pins, assign each pin upwards stating from the selected pin.
Assign Right	From the selected group of unassigned pins, assign each pin to the right of each other starting from the selected pin.
Assign Left	From the selected group of unassigned pins, assign each pin to the left of each other starting from the selected pin.
Assign One by One	Select a pin location for each of the pins selected from the **Unassigned Pins** list.

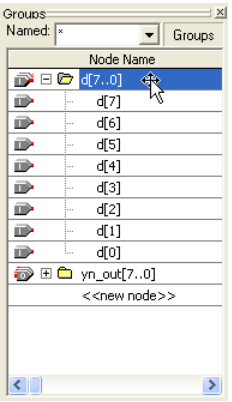
If there is an unassignable location in the path of the selected assignment direction pins are assigned, as far in the assignment direction as possible. Assign the rest of the pins in a separate location.

2. In the **Filter** list, select **Pins: unassigned**.

3. In the **All Pins** list, select one or more unassigned node names, or in the **Groups** list, select one or more buses.

   You can click on multiple node names using the control and shift keys. When you click on a pin or bus in the **All Pins** or **Groups** list, the node name is highlighted, and a crossing arrow displays above the cursor. Drag the selected cells into the package view (Figure 5–21).

Figure 5–21. Drag Node Name in the Groups List



4. Drag and drop the selected pins or buses from the **All Pins** or **Groups** list to a location in the package view.

   Before you drag and drop your pins, you can optionally use the Pin Finder to locate pin locations that support your selected pins. When creating a query in the Pin Finder, add an Assignment condition set to unassigned.

   If you don't use the Pin Finder, you can drop pins directly into any of the following locations in the Pin Planner package view: an available user I/O pin, I/O Bank, VREF Group, and Edge. On the View menu, you can display either I/O banks, VREF groups or edges by toggling between Show I/O Banks, Show VREF Groups, and Show Edges.

   Available user I/O pins are represented by empty circles in the package view. The letter inside the circle provides information about the user I/O pin. Negative and positive differential pins are indicated with the letters "n" and "p", respectively.

In the Pin Planner, I/O banks are displayed as rectangles labeled: IOBANK_<*number*> (Figure 5–26). In each I/O bank there are one or more VREF groups. VREF groups are displayed as rectangles labeled: VREF GROUP_B<*I/O Bank number*>_N<*index*> (Figure 5–28).

Edge locations are displayed as rectangles labeled: EDGE_<*direction*>. To make an edge assignment, drag and drop pins into one of the four edges, EDGE_TOP, EDGE_BOTTOM, EDGE_LEFT, or EDGE_RIGHT.

You can also drag and drop pins from the **Node Finder** dialog box and the Block Diagram/Schematic File into the package view.

Assigning a Location for Differential Pins

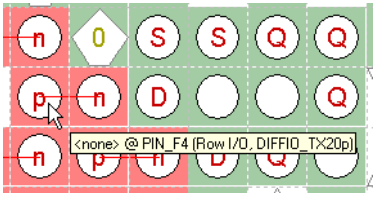
To identify and assign differential pins using the Pin Planner, perform the following steps:

1. On the View menu, click **Show Differential Pin Pair Connections**.

   When you select **Show Differential Pin Pair Connection**, a red line connects the positive and negative pins of the differential pin pairing. The positive and negative pins are labeled in the package view with the letters "p" and "n", respectively (Figure 5–22).

2. Use the tool tips to identify LVDS-compatible pin locations by holding the mouse pointer over a differential pin in the package view (Figure 5–22).

Figure 5–22. Tool Tip of the Positive Differential Pin



The tool tip shows the design pin name and pin number and its general and special functions.

Tool tip for differential receiver and transmitter channel pins that are also an available user I/O:

<*design pin name*> @ PIN_<*Package Pin Number*> (<*Row*|*Column*> I/O, DIFFIO_<*RX/TX*><*differential pin pair number*><*p*|*n*>)

Tool tip for dual-purpose LVDS I/O channel pins:

<*design pin name*> @ PIN_<*Package Pin Number*> (<*Row*|*Column*> I/O, LVDS<*differential pin pair number*><p|n>)

3. Click on the **differential pin** from the **All Pins** or **Groups** list.

4. Drag and drop the selected pin from the **All Pins** or **Groups** list to a differential positive pin location in the package view.

Optionally, before you drag and drop your pins, you can use the Pin Finder to locate pin locations that support your selected pins. When creating a query in the Pin Finder, add an Assignment condition set to unassigned and an I/O standard condition set to your differential I/O standard.

The unassigned differential pin that you drag to the package view represents the positive pin of the differential pair. The Fitter automatically recognizes the negative pin of the differential pair and creates it in the Pin-Out file.

If you assign a differential pin to a pin location, the negative pin becomes unassignable. The Quartus II software recognizes the negative pin as part of the differential pin pair assignment, however the assignment is not entered in the Quartus II Settings File (QSF).

If you have a single ended clock that feeds a PLL, assign the pin only to the positive clock pin in the targeted device. Single ended pins, that feed a PLL and are assigned to the negative clock pin in the targeted device cause the design to fail to fit.

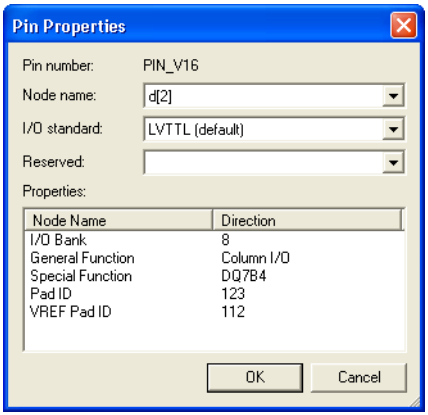
For more information on the general and special functions displayed by the tool tip, refer to the Device Pin-Outs available at **www.altera.com**.

Assigning an Unassigned Pin to a Pin Location
Use the following steps to select a pin location and assign a design pin to that location:

1. Select an available pin location in the package view.

2. On the View menu, click **Pin Properties. The Pin Properties** dialog box appears (Figure 5–23).

Figure 5–23. Pin Properties Dialog Box



You can use the **Pin Properties** dialog box to create pin location and I/O standard assignments. The **Pin Properties** dialog box also displays the properties of the pin location, including the pad ID (Table 5–4). The pad ID is important information when following pin spacing guidelines. Adjacent pin numbers do not always represent adjacent pads on the die. Use the Pads view to help correlate pad location and distance between your user I/O pins and VREF pins.

3. Select a pin from the **Node Name** list.

4. To assign or change the I/O standard, select an I/O standard from the **I/O standard** list.

5. Click **OK**.

For more information about pin placement, refer to the appropriate device handbook.

Table 5–4 provides a description of each field in the **Pin Properties** dialog box.

Table 5–4. Pin Properties

Pin Property	Description
Pin Number	Pin number used in package *(1)*
Node Name	Node name assigned to the pin location
I/O Standard	I/O standard assigned to the pin name and location
Reserved	If reserved, determines how to reserve this pin
I/O Bank	I/O bank number of the pin
General Function	General function of the pin (row/column I/O, dedicated clock pin VCC, GND)
Special Function	Special function of the pin (LVDS, PLL)
Pad ID	Pad number connected to pin
VREF Pad ID	The pad ID for the V_{REF} pin used for voltage referenced I/O standards

Note to Table 5–4:
(1) For more information on how pin numbers are derived, refer to the device pin-out on the Altera website, www.altera.com.

You can also open the **Pin Properties** dialog box using these alternative methods: Double-click on a pin in the package view of the Pin Planner, or right-click the pin in the package view of the Pin Planner, and click **Pin Properties**.

Error Checking Capability

The Pin Planner has basic pin placement checking capability, preventing pin placements that violate the fitting rules. The following checks are performed by the Pin Planner as you make pin-related assignments:

- An I/O Bank or VREF Group is an unassignable location if there are no available pins in the I/O bank or VREF group.
- The negative pin of the differential pair is unassignable if the positive pin of the differential pair has been assigned with a node name with a differential I/O standard.
- Dedicated input pins (for example, dedicated clock pins) are an unassignable location if you attempt to assign an output or bidirectional node name.
- Pin locations that do not support the I/O standard assigned to the selected node name become unassignable.
- All nodes in the same VREF group must have the same VREF voltage. Apply this only to HSTL- and SSTL-type I/O standards.

To perform a more comprehensive check on your pin placements, perform I/O assignment analysis.

For more information, refer to "Using I/O Assignment Analysis to Validate Pin Assignments" on page 5–47.

After creating a pin location, the **Location**, **I/O Bank**, and **VREF Group** fields are populated in both the **All Pins** list and the **Groups** list. In the package view, the occupied pins are filled with a dark brown color.

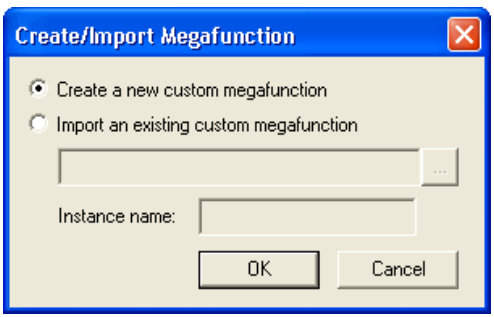
Creating & Importing Megafunctions & IP MegaCores in the Pin Planner

It may be difficult to plan your I/Os early in the design cycle because design files may not be available. However, the interfaces between your FPGA and other devices are typically determined and documented in the design specifications. By adding the bus or memory interface into the Pin Planner, you can efficiently plan your FPGA I/Os. You can add many types of interfaces, including Megafunctions like `ALTPLL` and `ALTDDIO` as well as IP MegaCores like PCI Compiler, QDR II, and Rapid IO. After adding the interfaces used in your design, the **Groups** list is automatically populated with all the external pins of your megafunctions and IP MegaCores.

The advantage of adding the interface information while planning your I/Os is that it eliminates the possibility of not assigning a required pin and eliminates manually creating each individual pin into the Pin Planner.

After creating or importing your Megafunction or IP MegaCore variation, the name of the Megafunction or IP MegaCore is shown in the **Groups** list with all the external I/O pin names listed as its members.

Figure 5–24. Create/Import Megafunction Dialog Box



Create a Megafunction or IP MegaCore Variation from the Pin Planner
To create a megafunction or IP MegaCore Variation from the Pin Planner, perform the following steps:

1. In the Pin Planner, right-click anywhere in the package view.
2. On the right-click menu, click **Create/Import Megafunction**. The **Create/Import Megafunction** dialog box appears. (Figure 5–24).
3. To create a new megafunction, select **Create a new megafunction** and click **OK**. The **MegaWizard® Plug-In Manager** dialog box appears.
4. Under the Installed Plug-Ins, a list of all of the supported Megafunctions and IP MegaCores are shown. Select the **Megafunction or IP MegaCore,** and complete the wizard.
5. After you complete the wizard, a new group, based on the file name you provided, is created and all the I/O names, direction and I/O standards are listed as members of the group in the **Groups** list. Make pin location assignments for the group or to each individual pin.

Import a Megafunction or IP MegaCore Variation from the Pin Planner
To import a Variation from the Pin Planner, perform the following steps:

1. In the Pin Planner, right-click anywhere in the package view
2. On the right-click menu, click **Create/Import Megafunction**. The **Create/Import Megafunction** dialog box appears (Figure 5–24).
3. If you are importing an existing megafunction, select **Import an existing customer megafunction,** and click **browse.** Select the **Pin Planner File** (**.ppf**) generated along with your Megafunction variation or your IP MegaCore files.
4. In the instance name, type in an instance name and Click **OK**.

   To avoid pin name conflicts when there are more than one instance of a Megafunction or IP MegaCore, the instance name is appended to the beginning of each pin name.
5. After you complete the wizard, a new group, based on your filename you provided, is created and all the I/Os that are used externally are listed as members of the group. Make pin location assignments for the group or to each individual pin.

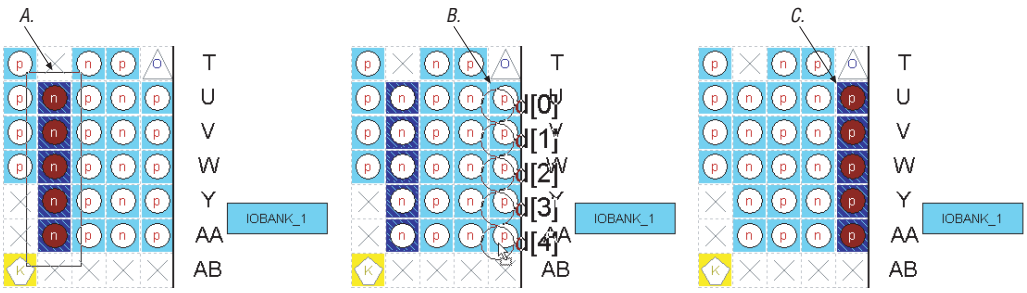
Changing Pin Locations

The Pin Planner allows you to change the location of multiple pins simultaneously. To change pin locations, select one or more pins in the package view or pad view, and drag the pins to a new location.

Understanding which user I/O pins are available and their physical locations on the device package makes it quick and easy to change pin locations. For example in the package view, you can move a column of pins closer to the edge of the device for easier PCB routing (Figure 5–25). In this example, you are moving multiple I/O pins to the area closest to the edge of the I/O bank

1. In the Package view select multiple pins by holding down the left mouse button and dragging over the pins you want to move (Figure 5–25, step A).
2. Drag the group of pins to the area of placement (Figure 5–25, step B).
3. Drop the pins into the area closest to the edge of the I/O bank (Figure 5–25, step C).

Figure 5–25. Changing the Locations for a Group of Pins

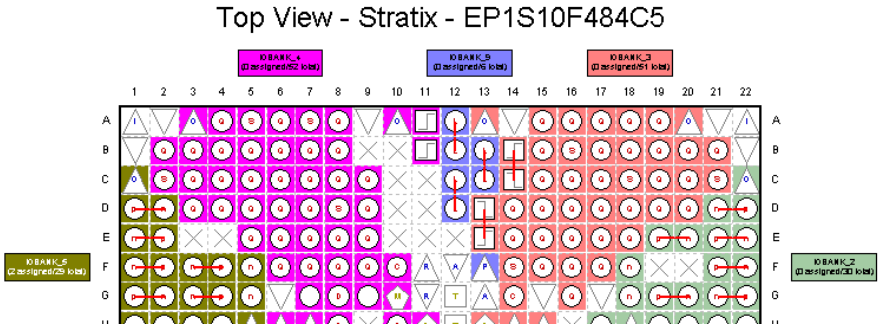


Show I/O Banks

When **Show I/O Banks** is turned on (on the **View** menu), the package view groups I/O pins that share the same `VCCIO` pin using different colors (Figure 5–26). When planning your I/O pins, it is important to guide your pin placement decisions by placing pins with compatible I/O standards into the same I/O bank. For example, you cannot place an `LVTTL` pin with an I/O standard of LVTTL in the same bank as another pin with an I/O standard of 1.5 V HSTL Class I.

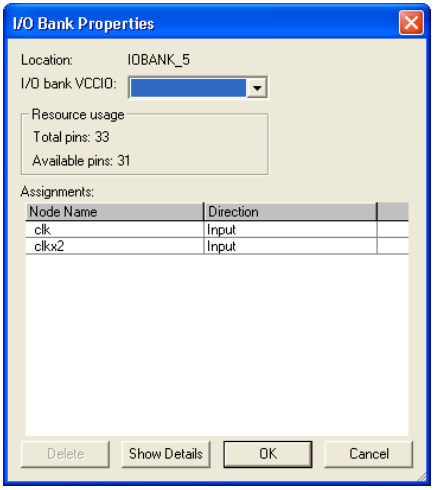
For more information on compatible I/O standards, refer to the appropriate device handbook.

Figure 5–26. Package View with Show I/O Banks Turned On



When **Show I/O Banks** is turned on, the package view allows you to view the properties of each I/O bank. Select an I/O Bank in the package view and on the View menu, click **I/O Bank Properties.** The **I/O Bank Properties** dialog box appears (Figure 5–27). The **I/O Bank Properties** dialog box lists all node names assigned to that I/O Bank. To view all node names that are assigned within the I/O Bank, click **Show Details** in the **I/O Bank Properties** dialog box. You can also assign the VCCIO for the I/O Bank by selecting a voltage from the **I/O bank VCCIO** list.

Figure 5–27. I/O Bank Properties Dialog Box



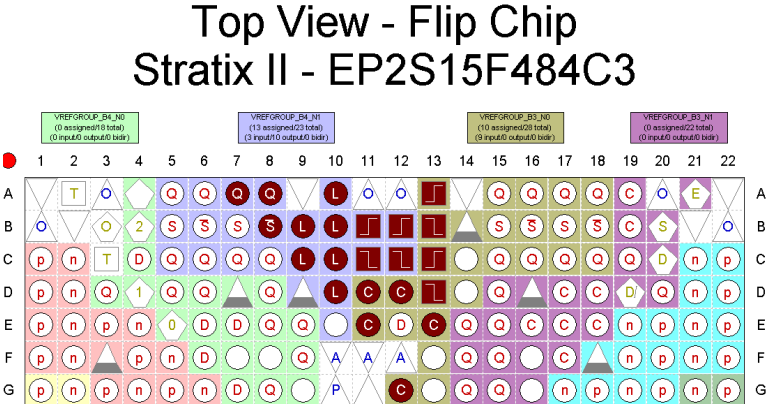
The Resource section describes the total number of pins in the I/O Bank including assignable and unassignable pins. and the total number of available assignable pins.

Show VREF Groups

On the View menu, when the **Show VREF Groups** is turned on, the package view uses different colors to indicate different groups of I/O pins sharing the same VCCIO and VREF pins (Figure 5–28). When planning your I/O pins, it is important to place pins with compatible voltage-referenced I/O standards in the same I/O bank. To guide your pin placement decision by placing compatible I/O standards requiring VREF pins into the same VREF group, on the View menu, click **Show VREF Group**. For example, pins with I/O standards SSTL-18 Class II and 1.8V-HSTL Class II are compatible and can be placed into the same VREF group. It is also important to be aware of the number and direction of pins within a VREF group for simultaneous switching noise (SSN) analysis.

For more information on compatible I/O standards, refer to the appropriate device handbook.

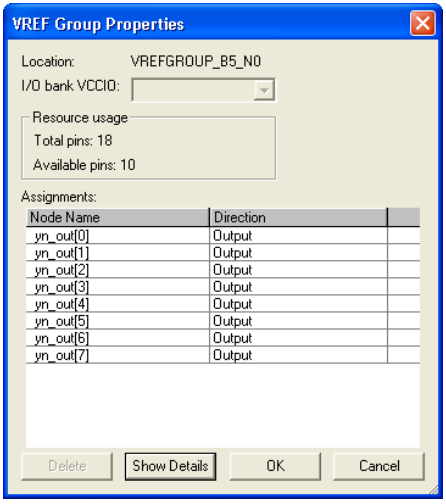
Figure 5–28. Package View Showing VREF Groups



When **Show VREF Groups** is turned on, the package view allows you to show the properties of each VREF group. Select a VREF group in the package view, and on the View menu, click **VREF Group Properties.** The **VREF Group Properties** dialog box appears (Figure 5–29). In the **VREF Group Properties** dialog box, all node names assigned to the VREF group are listed. Click **Show Details** to view node names that are assigned to pin numbers within the VREF group. Any design pins that are assigned to the VREF group and not to a pin number are listed in the **Assignments**

list. The Resource usage section describes the total number of pins in the VREF group and the total number of available assignable pins. It also keeps a running tally on the input, output, and bidirectional pins.

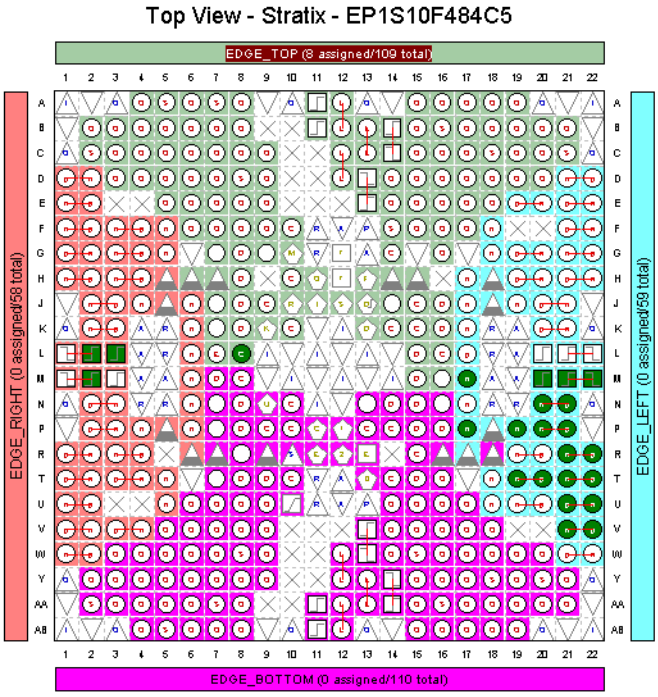
Figure 5–29. VREF Group Properties



Show Edges

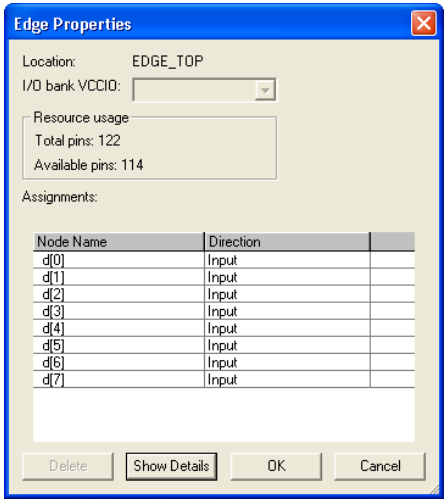
When you turn on **Show Edges**, on the View menu, the package view uses different colors to indicate the four edges of the package (Figure 5–30). When planning your I/O pins, if the exact location of a pin is not a priority, use an Edge assignment.

Figure 5–30. Package View with Show Edges



When Show Edges is turned on, the package view allows you to show the properties of each Edge. Select an Edge in the package view and on the View menu, click **Edge Properties. The Edge Properties dialog box appears**. In the **Edge Properties** dialog box, all node names assigned to the Edge are listed (Figure 5–31). To view all node names assigned to a pin number within an Edge, in the **Edge Properties** dialog box, click **Show Details**.

Figure 5–31. Edge Properties

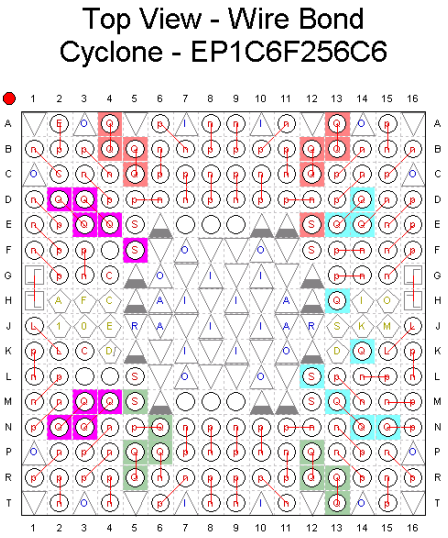


Show DQ/DQS Pins

When **Show DQ/DQS Pins** on the View menu is turned on, the package view uses different colors to highlight groups of DQ pins and DQS pins (Figure 5–32). Highlighting these DQ/DQS groups easily identifies which DQ pins are associated with the DQS strobe pin. You can select between the following DQ/DQS modes:

- In x4 Mode
- In x8/x9 Mode
- In x16/x18 Mode
- In x32/x36 Mode

Figure 5–32. DQ/DQS Pins (1)



Note to Figure 5–32:
(1) This DQ/DQS view shows an x8 mode.

For example, when implementing DDR II in a Stratix II device, there are dedicated pins designed specifically to be used as DQ and DQS pins.

For more information on using the `altdq` and `altdqs` megafunction, refer to the *altdq & altdqs Megafunction User Guide*.

Displaying & Accepting Fitter Placements

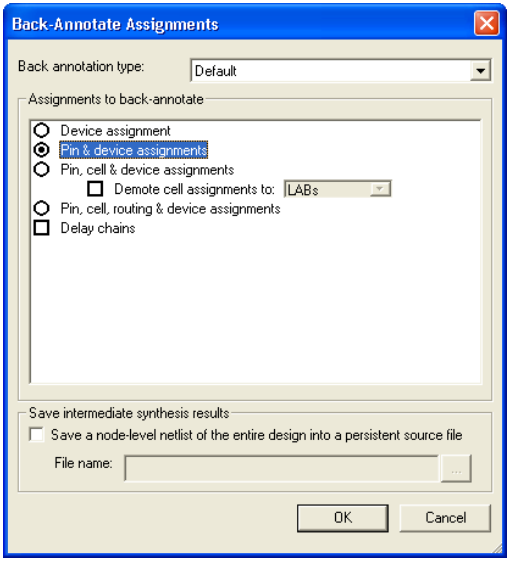
In addition to the **Show I/O Banks**, the **Show VREF Groups**, and the **Show Edge** views, you can also show pins placed by the Fitter by selecting **Show Fitter Placements** on the View menu.

The Fitter provides optimal placement to unassigned pins based on design constraints when you perform a compilation or an I/O Assignment Analysis. When you select **Show Fitter Placements** on the View menu, the Fitter-placed pins are shown as green filled pins in the package view of the Pin Planner. You can create a copy of the fitter placements in your project Quartus II Settings File using the

Back-Annotation command. To create assignments for all Fitter-placed pins into your project Quartus II Settings File, perform the following steps:

1. On the Processing menu in the Quartus II software, click **Start Compilation**, or on the Processing menu, point to Start and click **I/O Assignment Analysis**.
2. On the Assignments menu, click **Pin Planner**. The **Pin Planner** dialog box appears.
3. On the View menu, click **Show Fitter Placements**, and review the Fitter placements.
4. To create location assignments for these fitter placements, perform the following steps:
   a. On the assignments menu, click **Back-Annotate Assignments**. The **Back-Annotate Assignments** dialog box appears.
   b. Select **Pin & device assignments** (Figure 5–33).
   c. Click **OK**.

Figure 5–33. Back-Annotate Assignments Dialog Box



To create assignments for selection of the Fitter-placed pins, perform the following steps:

1. On the Processing menu in the Quartus II software, click **Start Compilation**, or on the Processing menu, point to Start**,** and click **I/O Assignment Analysis**.
2. On the Assignments menu, click **Pin Planner**.
3. On the View menu, click **Show Fitter Placements**, and review the Fitter placements.
4. In the Pin Planner, select one or more fitter-placed pins for which you want to create assignments.
5. Right-click one of the selected pins, and click **Back Annotate**.
6. On the File menu, click **Save Project**. The Assignments are written to the Quartus II Settings File.

For more information on how the Quartus II software writes and updates the Quartus II Settings File, refer to the *Quartus II Project Management* chapter in volume 2 of the *Quartus II Handbook*.

Using I/O Assignment Analysis to Validate Pin Assignments

This section describes a design flow that includes making and analyzing pin assignments with the Start I/O Assignment Analysis command in the Quartus II software, during and after the development of your HDL design.

The **Start I/O Assignment Analysis** command allows you to check your I/O assignments early in the design process. Use this command to check the legality of pin assignments before, during, or after compilation of your design. If design files are available, you can use this command to perform more thorough legality checks on your design's I/O pins and surrounding logic. These checks include proper reference voltage pin usage, valid pin location assignments, and acceptable mixed I/O standards.

The **Start I/O Assignment Analysis** command can be used for designs targeting Stratix series, Cyclone™ series, and MAX® II device families.

I/O Assignment Analysis Design Flows

The I/O assignment analysis design flows depend on whether your project contains design files. The following examples show two different times when I/O assignment analysis can be used:

- When the board layout must be complete before starting the FPGA design, use the flow shown in Figure 5–34 on page 5–49. This flow does not require design files and checks the legality of your pin assignments.
- With a complete design, use the flow shown in Figure 5–36 on page 5–51. This flow thoroughly checks the legality of your pin assignments against any design files provided. For more information on creating assignments, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Each flow involves creating pin assignments, running the analysis, and reviewing the report file.

You should run the analysis each time you add or modify a pin-related assignment. You can use the **Start I/O Assignment Analysis** command frequently since it completes in a short time.

The analysis checks pin assignments and surrounding logic for illegal assignments and violations of board layout rules. For example, the analysis checks whether your pin location supports the I/O standard assigned, current strength, supported V_{REF} voltages, and whether a PCI diode is permitted.

Along with the pin-related assignments, the **Start I/O Assignment Analysis** command also checks blocks that directly feed or are fed by resources such as a phase-locked loops (PLLs), low-voltage differential signals (LVDS), or gigabit transceiver blocks.

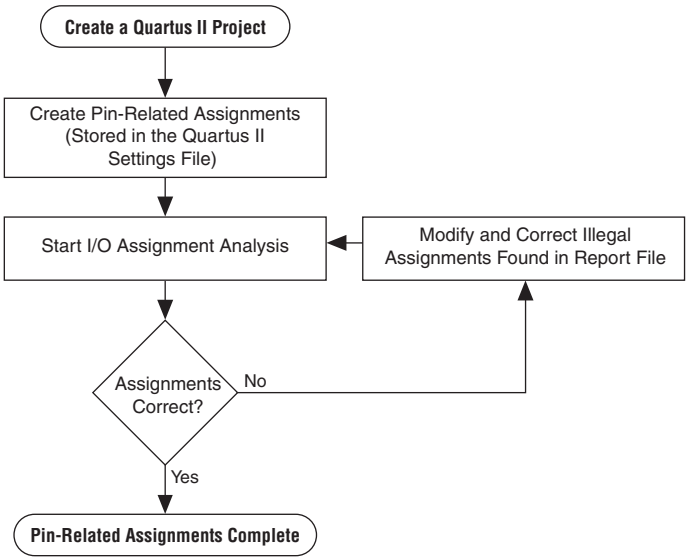
Design Flow without Design Files

During the early stages of development of an FPGA device, board layout engineers may request preliminary or final pin-outs. It is time consuming to manually check to see whether the pin-outs violate any design rules. Instead, you can use the **Start I/O Assignment Analysis** command to quickly perform basic checks on the legality of your pin assignments.

Without a complete design, the analysis performs limited checks and cannot guarantee that your assignments do not violate design rules.

The I/O Assignment Analysis command is able to perform limited checks on pin assignments made in a Quartus II project that has a device specified, but may not yet include any HDL design files. For example, you can create a Quartus II project with only a target device specified and create pin-related assignments based on circuit board layout considerations that are already determined. Even though the Quartus II project does not yet contain any design files, you can reserve input and output pins and make pin-related assignments for each pin using the Assignment Editor. After you assign an I/O standard to each reserved pin, run the I/O Assignment Analysis to ensure that there are no I/O standard conflicts in each I/O bank.

Figure 5–34. Assigning & Analyzing Pin-Outs without Design Files



To assign and analyze pin-outs using the **Start I/O Assignment Analysis** command without design files, perform the following steps:

1. In the Quartus II software, create a project.

2. Use the **Assignment Editor**, **Pin Planner**, or a Tcl script to create pin locations and related assignments. For the I/O assignment analysis to determine the type of pin, you must reserve your I/O pins. Refer to "Reserving Pins" on page 5–57.

If you make pin-related assignments in the Mentor Graphics I/O Designer software, you can import an FPGA Xchange file into the Quartus II software.

3. On the Processing menu, point to Start, and click **Start I/O Assignment Analysis** to start the analysis.

   For information on using a Tcl script or command prompt to start the analysis, refer to "Scripting Support" on page 5–60.

4. View the messages in the Compilation Report window, Fitter report file (*<project name>*.**fit.rpt**), or in the Messages window.

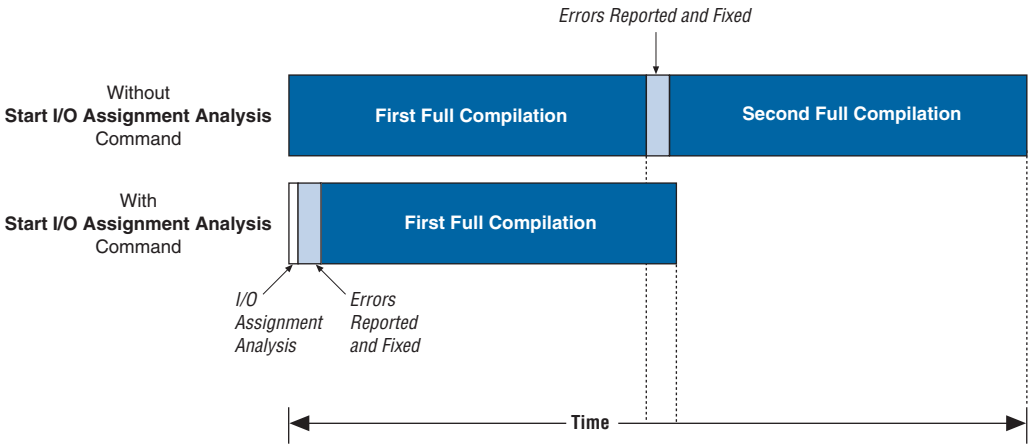
5. Correct any errors and violations reported by the I/O assignment analysis.

Repeat the above steps 1 through 5 until all of the errors are corrected.

Design Flow with Design Files

During a full compilation, the Quartus II software does not report illegal pin assignments until the fitter stage. To validate pin assignments sooner, you can run the **Start I/O Assignment Analysis** command after performing analysis and synthesis and before performing a full compilation. Typically, the analysis takes a short time. Figure 5–35 shows the benefits of using the **Start I/O Assignment Analysis** command.

Figure 5–35. Saving Compilation Time with the Start I/O Assignment Analysis Command

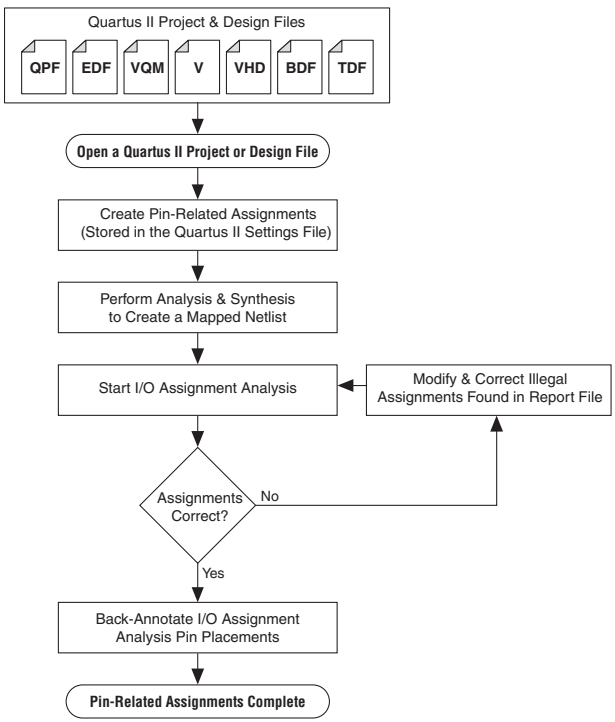


The rules that are checked by the I/O assignment analysis depend on the completeness of the design. With a complete design, the **Start I/O Assignment Analysis** command thoroughly checks the legality of all pin-related assignments. With a partial design, which can be just the top-level wrapper file, the **Start I/O Assignment Analysis** command checks the legality of those pin-related assignments for which it has enough information.

For example, you might assign a clock to a user I/O pin instead of assigning it to a dedicated clock pin, or you design the clock to drive a PLL that has not yet been instantiated in the design. Because the **Start I/O Assignment Analysis** command is unaware of the logic that the pin drives, it is not able to check that only a dedicated clock input pin can drive the clock port of a PLL.

Analyze as much of the design as possible, especially logic that connects to pins, to obtain better coverage. For example, if your design includes PLLs or LVDS blocks, you should include these MegaWizard Plug-In Manager-generated files in your project for analysis (Figure 5–36).

Figure 5–36. Assigning & Analyzing Pin-Outs with Design Files



To assign and analyze pin-outs using the **Start I/O Assignment Analysis** command with design files, perform the following steps:

1. In the Quartus II software, create a project including your design files.
2. Create pin-related assignments with the **Assignment Editor**.

   You can also create pin-related assignments by importing them from a Comma Separated Value file, executing Tcl commands, editing the Quartus II Settings File directly, or by dragging and dropping pins to point to Start and click **Start Analysis & Synthesis** to generate an internal mapped netlist.

   For information on using a Tcl script or the command prompt to start the analysis, refer to "Scripting Support" on page 5–60.
3. On the Processing menu, point to Start, and click **Start I/O Assignment Analysis** to start the analysis.
4. View the messages in the Compilation Report or in the Messages window.
5. Use the Assignment Editor to correct any errors and violations reported.
6. Use the **Start I/O Assignment Analysis** command until all errors are corrected.

I/O Rules Checked by the I/O Assignment Analysis

The effectiveness of the I/O Assignment Analysis is relative to the completeness of your pin-related assignments and design. To ensure your design functions correctly, include as many design files as possible and all pin-related assignments in your Quartus II project.

Tables 5–5 and 5–6 list a subset of the I/O rule checks performed when you execute an I/O Assignment Analysis with and without design files.

For more detailed information on each I/O rule, refer to the appropriate device handbook.

Table 5–5. General I/O-Related Rules (Part 1 of 2)

Rule	Description	Device *(1)* Families	HDL Required?
I/O bank capacity	Checks the number of pins assigned to an I/O bank against the number of pins allowed in the I/O bank.	All	No
I/O bank V_{CCIO} voltage compatibility	Checks that no more than one VCCIO is required from the pins assigned to the I/O bank.	All	No
I/O bank V_{REF} voltage compatibility	Checks that no more than one VREF is required from the pins assigned to the I/O bank.	All	No
I/O standard and location conflicts	Checks if the pin location supports the assigned I/O standard.	All	No
I/O standard and signal direction conflicts	Checks if the pin location supports the assigned I/O standard and direction. For example, certain I/O standards on a particular pin location can only support output pins.	All	No
Differential I/O standards cannot have open drain turned ON	Checks that open drain is turned off for all pins with a differential I/O standard.	All	No
I/O standard and drive strength conflicts	Checks if the drive strength assignments is within the specifications of the I/O standard.	All	No
Drive strength and location conflicts	Checks if the pin location supports the assigned drive strength.	All	No
BUSHOLD and location conflicts	Checks if the pin location supports BUSHOLD. For example, dedicated clock pins do not support BUSHOLD.	All	No
WEAK_PULLUP and location conflicts	Checks if the pin location supports WEAK_PULLUP (for example, dedicated clock pins do not support WEAK_PULLUP)	All	No
Electromigration check	Checks if combined drive strength of consecutive pads does not exceed a certain limit. For example, the total current drive for 10 consecutive pads on a Stratix II device cannot exceed 200 mA.	All	No
PCI_IO clamp diode, location, and I/O standard conflicts	Checks if the pin location along with the I/O standard assigned supports PCI_IO clamp diode.	All	No
SERDES and I/O pin location compatibility check	Checks that all pins connected to a SERDES in your design are assigned to dedicated SERDES pin locations.	All	Yes

Table 5–5. General I/O-Related Rules (Part 2 of 2)

Rule	Description	Device (1) Families	HDL Required?
PLL and I/O pin location compatibility check	Checks if pins connected to PLL are assigned to the dedicated PLL pin locations.	All	Yes

Note to Table 5–34:
(1) "All" includes the following device families: Stratix II, Stratix GX, Stratix, Cyclone II, Cyclone, MAX II, and HardCopy devices.

Table 5–6. SSN-Related Rules

Rule	Description	Device (1) Families	HDL Required?
I/O bank can not have single-ended I/O when DPA exists	Checks that no single-ended I/O pin exists in the same I/O bank as a DPA.	Stratix II, Stratix GX	No
A PLL I/O bank does not support both a single-ended I/O and a differential signal simultaneously	Checks that there are no single-ended I/O pins present in the PLL I/O Bank when a differential signal exists.	Stratix II	No
Single-ended output is required to be a certain distance away from a differential I/O pin	Checks if single-ended output pins are a certain distance away from a differential I/O pin.	All	No
Single-ended output has to be a certain distance away from a VREF pad	Checks if single-ended output pins are a certain distance away from a VREF pad.	Cyclone II, Cyclone	No
Single-ended input is required to be a certain distance away from a differential I/O pin	Checks if single-ended input pins are a certain distance away from a differential I/O pin.	Cyclone II, Cyclone	No
Too many outputs or bidirectional pins in a VREFGROUP when a VREF is used	Checks that there are no more than a certain number of outputs or bidirectional pins in a VREFGROUP when a VREF is used.	All	No
Too many outputs in a VREFGROUP	Checks if too many outputs are in a VREFGROUP .	All	No

Note to Table 5–6:
(1) "All" includes the following device families: Stratix II, Stratix GX, Stratix, Cyclone II, Cyclone, MAX II, and HardCopy devices.

Using Output Enable Group Logic Option Assignments with I/O Assignment Analysis

Each device has a certain number of VREF pins, and each VREF pin supports a certain number of I/O pins. Check the device pin-outs to locate the VREF pins and its associated I/O pins. The VREF pin, including its supported I/O pins, is called a VREF bank. The VREF pins are only used for VREF I/O standards, for example, SSTL and HSTL, input pins. VREF outputs do not require the VREF pin. When a voltage-referenced

input is present in a VREF bank, there can only be a certain number of outputs that can be present in that VREF bank. For the Stratix II flip chip package, only 20 outputs can be present in a VREF bank when a VREF I/O standard input is present in that bank.

For interfaces that use bidirectional VREF I/O pins, the VREF restriction must be met when the pins are driving in either direction. If a set of bidirectional signals are controlled by different output enables, the **I/O Assignment Analysis** command treats these as independent output enables. Use the output enable group logic option assignment to treat the set of bidirectional signals as a single output enable. This is important in the case of external memory interfaces.

For example, a DDR2 interface in a Stratix II device. A Stratix II device can have 30 pins in a VREF group. Each byte lane for a x8 DDR2 interfaces has 1 DQS pin and 8 DQ pins, totaling 9 pins per byte lane. DDR2 uses SSTL18 as its I/O standard, which is a VREF I/O standard. In typical interfaces, each byte lane has its own output enable. In this example, the DDR2 interface has 4 byte lanes. Using 30 I/O pins in a VREF group, there are 3 byte lanes, and an extra byte lane supporting the 3 remaining pins. If you do not use the output enable group logic option assignment, the I/O Assignment Analysis command analyzes each byte lane as an independent group driven by a unique output enable. With this arrangement, the worst case scenario is when the 3 pins are inputs, and the other 27 pins are outputs. In this case, the 27 output pins violate the 20 output pin limit.

In a DDR2 interface, all DQS and DQ pins are always driven in the same direction. Therefore, the I/O Assignment Analysis reports an error that is not applicable to your design. Assigning an output enable group logic option assignment to the DQS and DQ pins forces the I/O Assignment Analyzer to check these pins as a group driven by a common output enable. When using the output enable group logic option assignment, the DQS and DQ pins are checked as all input pins or all output pins. This does not violate the rules described in Tables 5–5 and 5–6.

The value for the output enable group logic option assignment should be an integer value. All sets of signals that are driving in the same direction should be given the same integer value. The output enable group logic option assignment can also be used with pins that are driven only at certain times. For example, the data mask signal in DDR2 interfaces are only outputs, but are driven only when the DDR2 is writing (bidirectional signals are outputs). Therefore, an output enable group logic option assignment should be assigned to the data mask with the same value of the DQ and DQS signals.

Output enable groups can also be used on VREF input pins. If the VREF input pins are not active during the time the outputs are driving, you can add the VREF input pins to the output enable group. This removes the VREF input pins from the VREF analysis. For example, the QVLD signal for RLDRAM II is only active during a read. During a write, the QVLD is not active and so it does not count as an active VREF input pin within the VREF group. The QVLD pins can be placed in the same output enable group as the RLDRAM II data pins.

Inputs for I/O Assignment Analysis

The **Start I/O Assignment Analysis** command reads the following inputs:

- Internal mapped netlist
- Quartus II Settings File

The internal mapped netlist is used when you have a partial or complete design. The Quartus II Settings File is always used to read all pin-related assignments for analysis.

Generating a Mapped Netlist

The **Start I/O Assignment Analysis** command uses a mapped netlist, if available, to identify the pin type and the surrounding logic. The mapped netlist is stored internally in the Quartus II software database.

To generate a mapped netlist, on the Processing menu, point to Start, and click **Start Analysis & Synthesis**.

To use the `quartus_map` executable to run analysis and synthesis, type the following command at a system command prompt:

```
quartus_map <project name> ↵
```

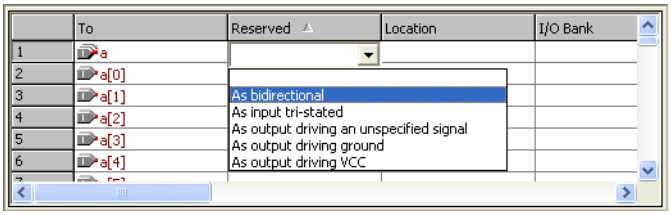
Creating Pin-Related Assignments

The **I/O Assignment Analysis** command reads a Quartus II Settings File containing all of your pin-related assignments. These pin-related assignments include pin settings such as I/O standards, drive strength, and location assignments. The following sections highlight some of the location assignments you can make.

Reserving Pins

If you do not have any design files, you can still reserve pin locations and create pin-related assignments. Reserving pins is necessary so that the **Start I/O Assignment Analysis** command has information about the pin and the pin type (input, output, or bidirectional) to correctly analyze the pins. To reserve a pin, on the Assignments menu, click **Assignment Editor**, In the **Category** bar, click **Pin** to open the Pin assignment category. Double click the cell in the **Reserved** column that corresponds to the pin which you want to reserve. Use the drop-down arrow to select from the reserve pin options (Figure 5–37).

Figure 5–37. Reserving an Input Pin with the Assignment Editor



For more information on using the Assignment Editor, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

You can also reserve pins using the Pin Planner. For more information on the Pin Planner, refer to "Pin Planner" on page 5–11.

Location Assignments

You can create the following types of location assignments for your design and its reserved pins:

- Pin number
- I/O bank
- VREF group
- Edge

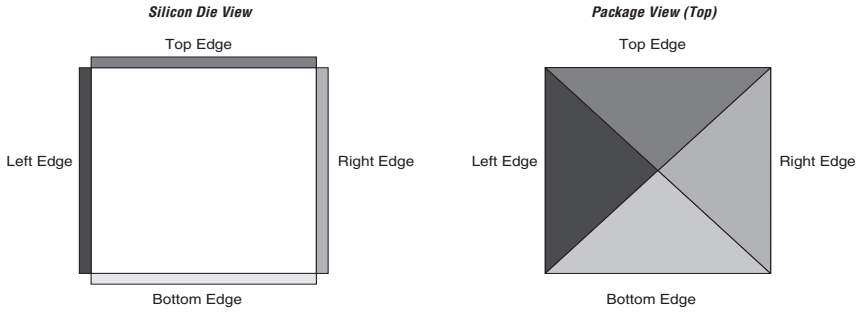
I/O bank, VREF group, and Edge location assignments are supported only for Stratix and Cyclone series device families.

You can assign a location to your pins using the Pin Planner or the Assignment Editor. To make a pin location assignment using the Assignment Editor, on the Assignments menu, click **Assignment Editor** and select the **Pin** category from the **Category** list. Type the pin name and select a location from the **Location** list.

It is common to place a group of pins (or bus) with compatible I/O standards in the same I/O bank or VREF group. For example, two buses with two compatible I/O standards, such as 2.5 V and SSTL-II, can be placed in the same I/O bank.

An easy way to place large buses that exceed the pins available in a particular I/O bank is to use edge location assignments. You can also use edge location assignments to improve the circuit board routing ability of large buses, since they are close together near an edge. Figure 5–38 shows the Altera device package edges.

Figure 5–38. Die View & Package View of the Four Edges on an Altera Device



Suggested & Partial Placement

The **Start I/O Assignment Analysis** command automatically assigns suggested pin locations to unassigned pins in your design so it can perform pin legality checks. For example, if you assign an edge location to a group of LVDS pins, the **I/O Assignment Analysis** command assigns pin locations for each LVDS pin in the specified edge location and then performs legality checks.

To accept these suggested pin locations, on the Assignments menu, click **Back-Annotate Assignments**, select **Pin & device** assignments, and click **OK**. Back-annotation saves your pin and device assignments in the Quartus II Settings File.

Understanding the I/O Assignment Analysis Report & Messages

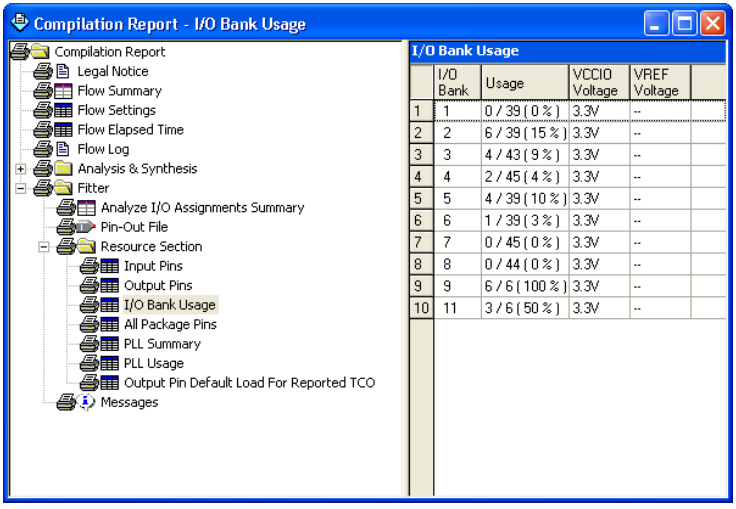
The **Start I/O Assignment Analysis** command generates a detailed analysis report (Figure 5–39) and a Pin-Out file. The detailed messages in the report help you quickly understand and resolve pin assignment errors. Each detailed message includes a related node name and a description of the problem.

To view the report file, on the Project menu, click **Compilation Report.** The **Fitter** section of the Compilation Report contains the following four sections:

- Analyze I/O Assignment Summary
- Resource Section
- Pin-Out File
- Fitter Messages

The Resource Section categorizes the pins as **Input Pins**, **Output Pins**, and **Bidir Pins**. View the utilization of each I/O bank in your device in the **I/O Bank Usage** section.

Figure 5–39. Summary of the I/O Bank Usage in the I/O Assignment Analysis Report



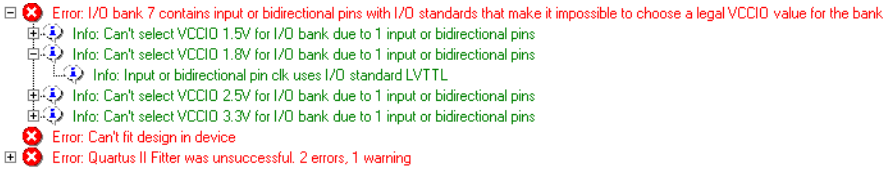
The **Fitter Messages** page stores all messages including errors, warnings, and information messages.

You can view the detailed messages in the **Fitter Messages** page in the compilation report and in the **Processing** tab in the **Messages** window. To open the **Messages** window, on the View menu, point to **Utility windows,** and click **Messages**.

Use the **Location** box to help resolve the error messages. Select from the **Location** list, and click **Locate**.

Figure 5–40 shows an example of error messages reported by I/O assignment analysis.

Figure 5–40. Error Message Report by I/O Assignment Analysis



Scripting Support

A Tcl script allows you to run procedures and make settings described in this chapter. You can also run some of these procedures at a command prompt.

For detailed information about specific scripting command options and Tcl API packages, type the following command at a system command prompt to run the Quartus II command-Line and Tcl API Help browser:

```
quartus_sh --qhelp ↵
```

at a system command prompt to run the Quartus II Command-Line and Tcl API Help browser.

For more information on Quartus II scripting support, including examples, refer to the *Tcl Scripting* and *Command-Line Scripting* chapters in volume 2 of the *Quartus II Handbook*.

Running the I/O Assignment Analysis

You can run the I/O Assignment Analysis with a Tcl command or with a command run at a command prompt. For more information about running the I/O Assignment Analysis, refer to "Understanding the I/O Assignment Analysis Report & Messages" on page 5–58.

Tcl Command
Enter the following in a Tcl console or script:

```
execute_flow -check_ios
```

Command Prompt
Type the following at a (non-Tcl) system command prompt:

```
quartus_fit <project-name> --check_ios ↵
```

Generating a Mapped Netlist

You can generate a mapped netlist with a Tcl command or with a command-line command. For more information about generating a mapped netlist, refer to "Generating a Mapped Netlist" on page 5–56.

Tcl Command
Enter the following in the Tcl console or in a script:

```
execute_module -tool map
```

The `execute_module` command is in the flow package.

Command Prompt
Type the following at a system command prompt:

```
quartus_map <project name>↵
```

Reserving Pins

Use the following Tcl command to reserve a pin. For more information about reserving pins, refer to "Reserving Pins" on page 5–57.

```
set_instance_assignment -name RESERVE_PIN <value> -to <signal name>
```

Valid values are: `"AS BIDIRECTIONAL"`, `"AS INPUT TRI-STATED"`,`"AS OUTPUT DRIVING AN UNSPECIFIED SIGNAL"`, `"AS OUTPUT DRIVING GROUND"` and `"AS SIGNALPROBE OUTPUT"`. Include the quotes when specifying the value.

Location Assignments

Use the following Tcl command to assign a signal to a pin or device location. For more information about location assignments, refer to "Location Assignments" on page 5–57.

```
set_location_assignment <location> -to <signal name>
```

Valid locations are pin location names, such as `Pin_A3`. The Stratix series and Cyclone device families also support edge and I/O bank locations. Edge locations are `EDGE_BOTTOM`, `EDGE_LEFT`, `EDGE_TOP`, and `EDGE_RIGHT`. I/O bank locations include `IOBANK_1` up to `IOBANK_n`, where *n* is the number of I/O banks in a particular device.

Generating IBIS Models

To help address signal integrity issues, Altera provides IBIS models to simulate Altera FPGA I/Os. IBIS model simulation provides many advantages, including the following:

- Protects proprietary information by not disclosing the internal circuitry and process of the devices.
- Provides accurate model generation since package parasitic and electrostatic discharge (ESD) structure is considered in generation of the models.
- Provides quick time-to-market since devices can be evaluated before silicon is available.
- Can be used for signal integrity simulation on boards.
- Provides faster simulation time compared to structural models such as Spice.
- IBIS is compatible with all industry simulation platforms.

You can generate IBIS models from the Quartus II software after a successful I/O assignment analysis or a fit by performing the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Settings** dialog box, under **Category**, select **Board-Level**.
3. In the **Tool name** list, select **Signal Integrity (IBIS)**.
4. Click **OK**.
5. On the Processing menu, click Start, and click **Start EDA Netlist Writer** or perform a full compilation.

A <*project name*>**.ibs** file is generated in the <*project directory*>/**board**/**ibis** directory.

For more information on IBIS model support, refer to www.altera.com.

Incorporating PCB Design Tools

This section provides an overview on transferring pin assignments to and from PCB tools. For more information, refer to the *Cadence PCB Design Tools Support* and the *Mentor Graphics PCB Design Tools Support* chapters in volume 2 of the *Quartus II Handbook*.

Signal and pin assignments are initially made by the FPGA or ASIC designer, and it is up to the board designer to correctly transfer these assignments to the symbols used in their system circuit schematics and board layout. As the board design progresses, pin reassignments may be requested or required to optimize the layout. These reassignments must in turn be relayed to the FPGA designer so that the new assignments can be validated with the I/O Assignment Analyzer and processed through an updated place-and-route of the FPGA.

The Quartus II software interacts with board layout tools by importing and exporting pin information files, including the Quartus II Settings File, Pin-Out file, and the FPGA Xchange file.

Conclusion

The Quartus II software provides many tools and features to help you through the I/O planning process. The I/O assignment analysis process offers the ability to validate pin assignments in all design stages, even before the development of the design. The ability to import and export assignments between the Quartus II software and other PCB tools also enables you to efficiently make iterative changes.

6. Mentor Graphics PCB Design Tools Support

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Introduction

With today's large, high-pin-count and high-speed FPGA devices, good and correct printed circuit board (PCB) design practices are more essential than ever for ensuring correct system operation. Typically, the PCB design takes place concurrently with the design and programming of the FPGA. Signal and pin assignments are initially made by the FPGA or ASIC designer, and the board designer must correctly transfer these assignments to the symbols used in their system circuit schematics and board layout. As the board design progresses, pin reassignments may be needed to optimize the PCB layout. These reassignments must in turn be relayed back to the FPGA designer so that the new assignments can be processed through an updated placement and routing of the FPGA design.

Mentor Graphics® provides tools to support this type of design flow. This chapter discusses how the Quartus® II software interacts with the Mentor Graphics I/O Designer software and the DxDesigner software to provide a completely cyclical FPGA-to-board integration design workflow. This chapter covers the following topics:

- General design flow between the Quartus II software, the Mentor Graphics I/O Designer software, and the DxDesigner software
- Setting up the Quartus II software to create the design flow files
- Creating an I/O Designer database project to incorporate the Quartus II software signal and pin assignment data
- Updating signal and pin assignment changes between the I/O Designer software and the Quartus II software
- Generating symbols in the I/O Designer software
- Creating symbols in the DxDesigner software from the Quartus II software output files without the use of the I/O Designer software

This chapter is intended primarily for board design and layout engineers who want to start the FPGA board integration while the FPGA is still in the design phase. Optionally, the board designer can plan the FPGA pinout and routing requirements in the Mentor Graphics tools and pass the information back to the Quartus II software for place-and-route. In addition, part librarians benefit from learning how to take output from the Quartus II software and use it to create new library parts and symbols.

The procedures in this chapter require the following software:

- The Quartus II software version 5.1 or higher
- DxDesigner software version 2004 or higher

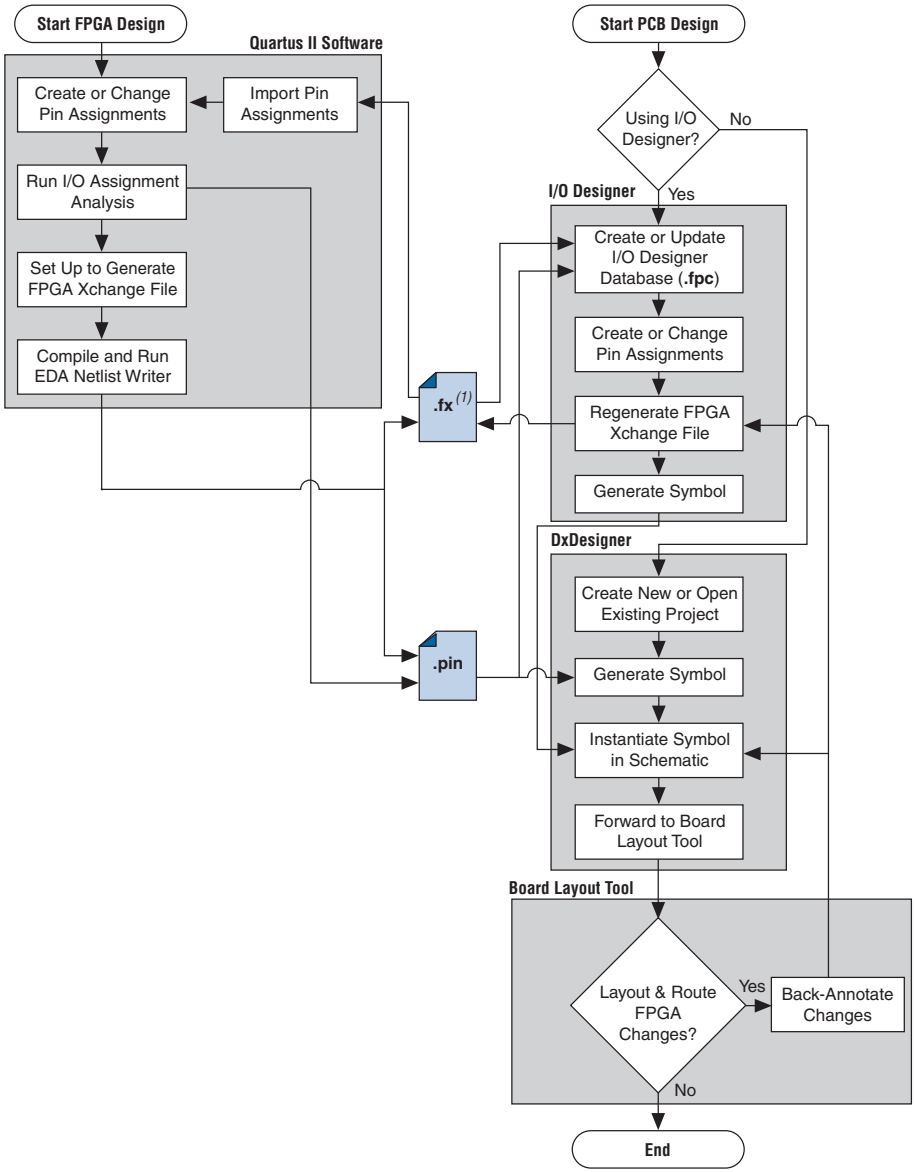
Mentor Graphics I/O Designer software is optional.

To obtain and license the Mentor Graphics tools and obtain product information, support, and training, go to the Mentor Graphics website at www.mentor.com.

FPGA-to-PCB Design Flow

In the examples in this section, you create a design flow integrating an Altera® FPGA design from the Quartus II software, and a circuit schematic in the DxDesigner software. Figure 6–1 shows the design flow with and without the I/O Designer software.

Figure 6–1. Design Flow with & without the I/O Designer Software



Note to Figure 6–1:

(1) The Quartus II software generates the FPGA Xchange file in the output directory you specify in the Board-Level Assignment Settings. However, the Quartus II software and the I/O Designer software can import pin assignments from an FPGA Xchange file located in any directory. Altera recommends that you work with a backup of the FPGA Xchange file to prevent overwriting existing assignments or importing invalid assignments.

The following tasks, which are described in this chapter, describe how to proceed through the design flow shown in Figure 6–1:

- Set up the board-level assignment settings to generate an FPGA Xchange file (**.fx**) for symbol generation in the Quartus II software
- Compile the design and generate the FPGA Xchange file and the Pin-Out file (**.pin**), which are located in the Quartus II project directory
- Create a board design using the DxDesigner software together with the I/O Designer software, which involves the following steps:
  - Create a new I/O Designer database based on the FPGA Xchange file and the Pin-Out file
  - Make adjustments to signal and pin assignments in the I/O Designer software
  - Regenerate the FPGA Xchange file in the I/O Designer software to reflect the I/O Designer software changes in the Quartus II software
  - Generate a single or fractured symbol for use in the DxDesigner software
  - Add the symbol to the **sym** directory of a DxDesigner project, or specify a new DxDesigner project with the new symbol
  - Instantiate the symbol in your DxDesigner schematic and export the design to the board layout tool
  - Back-annotate pin changes created in the board layout tool to the DxDesigner software and back to the I/O Designer software and the Quartus II software
- Create a board design using the DxDesigner software without the I/O Designer software, which involves the following steps:
  - Create a new DxBoardLink symbol using the Symbol Wizard and reference the Pin-Out file output from the Quartus II software in an existing DxDesigner project
  - Instantiate the symbol in your DxDesigner schematic and pass the design to a board layout tool

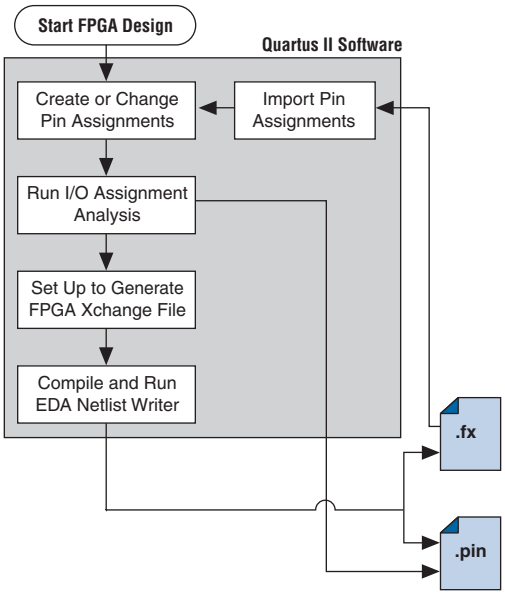
The I/O Designer software allows you to take advantage of the full FPGA symbol design, creation, editing, and back-annotation flow supported by Mentor Graphics tools.

Symbols can be updated with design changes at any point with or without the I/O Designer software. However, if symbols are changed in the DxDesigner software, the I/O Designer software does not see the changes. If you change symbols using the DxDesigner software, you must reimport the symbols into I/O Designer to avoid overwriting your symbol changes.

Setting Up the Quartus II Software

You can transfer pin and signal assignments from the Quartus II software to the Mentor Graphics tools by generating two output files, a Pin-Out file (**.pin**) and an FPGA Xchange file (**.fx**) (Figure 6–2).

Figure 6–2. Pin-Out Files & FPGA Xchange Files *Note (1)*



Note to Figure 6–2:

(1) Refer to Figure 6–1 for the full design flow, which includes the I/O Designer software, the DxDesigner software, and the board layout tool flowchart details.

The two output files, the Pin-Out file and the FPGA Xchange file, are described in Table 6–1.

Table 6–1. Pin Assignment Output File Format Comparison

File Format	Description
Pin-Out file (**.pin**) *(1)*	An output file generated by the Quartus II Fitter. The file cannot be imported into the Quartus II software to change pin assignments. The file contains a complete list of the device pins including any unused I/O pins, and provides the following basic information fields for each assigned pin on a device: • Pin signal name/usage • Pin number • Signal direction • I/O standard • Voltage • I/O Bank • User or fitter assigned
FPGA Xchange file (**.fx**) *(1)*,*(2)*	An input/output file generated by the Quartus II software and the I/O Designer software that can be imported and exported from both programs. Industry standard with room for future changes and additions. The FPGA Xchange file generated by the Quartus II software lists only assigned pins. The file provides the following advanced information fields for each pin on a device: • Pin number • I/O Bank • Signal name • Signal direction • I/O standard • Drive strength (mA) • Termination enabling • Slew rate • IOB Delay • Swap group • Differential pair type
	When generated by the I/O Designer software, all pins, including unused pins, are listed and the following fields are added: • Swap group • Differential pair type • Device pin name • Pin set • Pin set position • Pin set group • Super pin set group • Super pin set position

Notes to Table 6–1:

(1) For additional information about these file formats, refer to the Quartus II Help.

(2) For additional information about the information fields added by the Mentor Graphics software, refer to the Mentor Graphics website at www.mentor.com.

The I/O Designer software can also read from or update a Quartus II Settings File (**.qsf**). The Quartus II Settings File is used in the design flow in a similar manner to the FPGA Xchange file, but does not transfer pin swap group information between the I/O Designer software and the Quartus II software.

The **Quartus II Settings File** also contains additional important information about your project that is not used by the I/O Designer software. Because of this, Altera recommends that you use the FPGA Xchange file instead of the Quartus II Settings File for this design flow

For more information about the Quartus II Settings File, refer to the *Quartus II Settings File Reference Manual*.

Generating Pin-Out Files

The Quartus II Fitter generates the Pin-Out file whenever you perform a full compilation or I/O Assignment Analysis on your design. The file is generated and placed in your design directory and your file is named *<project name>***.pin**. The Mentor Graphics tools do not alter this file. The Quartus II software cannot import assignments from an existing Pin-Out file.

Generating FPGA Xchange Files

The FPGA Xchange file is not created automatically. To set up the Quartus II software to create the FPGA Xchange file, follow these steps:

1. Start the Quartus II software. On the Assignments menu, click **Settings**. The Settings dialog box appears.
2. Under EDA Tool Settings, click **Board-Level**. In the Board-Level Symbol Format list, choose **FPGA Xchange**.
3. Set the Output directory to the location where you want to save the file. The default output file path is *<project directory>***/symbols/fpgaxchange**. Click **OK**.
4. On the Processing menu, point to Start and click **Start EDA Netlist Writer**.

The output directory you selected is created when you generate the FPGA Xchange file.

CAUTION

Both the Quartus II software and the I/O Designer software can export and import an FPGA Xchange file. It is therefore possible to overwrite the FPGA Xchange file and import incorrect assignments into one or both programs. To prevent this occurrence from happening, make a backup copy of the file before importing, and import the copy instead of the file generated by the Quartus II software. In addition, assignments in the Quartus II software can be protected by following the steps in "Protecting Assignments in the Quartus II Software" on page 6–23.

Creating a Backup Quartus II Settings File

To create a backup Quartus II Settings File, perform the following steps:

1. On the Assignments menu, click **Import Assignments**. The Import Assignments dialog box appears.
2. In the Import Assignments dialog box, browse to your project and turn on **Copy existing assignments into** <*project name*>**.qsf.bak**.
3. Click **OK**.

Following these steps automatically creates a backup Quartus II Settings File of your current pin assignments.

For more information about pin and signal assignment transfer, and files the Quartus II software can import and export, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

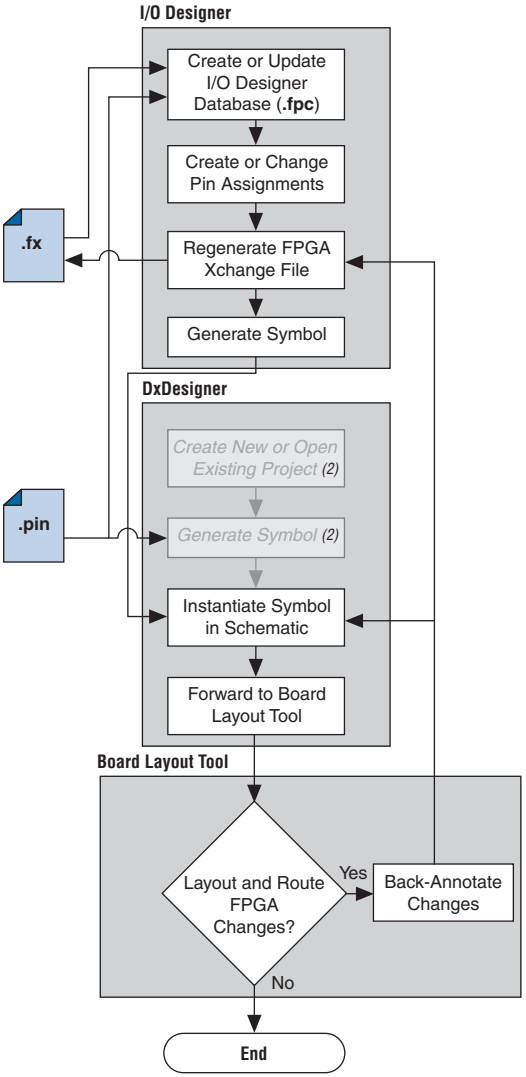
FPGA-to-Board Integration with the I/O Designer Software

The Mentor Graphics I/O Designer software allows you to integrate your FPGA and PCB designs. Pin and signal assignment changes can be made anywhere in the design flow, typically using either the Quartus II Pin Planner or the I/O Designer software. The I/O Designer software facilitates moving these changes, as well as synthesis, placement, and routing changes, between the Quartus II software, an external synthesis tool (if used), and a schematic capture tool such as the DxDesigner software.

This section describes how to use the I/O Designer software to transfer pin and signal assignment information to and from the Quartus II software with the FPGA Xchange file, and how to create symbols for the DxDesigner software.

Figure 6–3 shows the design flow using the I/O Designer software.

Figure 6–3. Design Flow Using the I/O Designer Software Note (1)



Notes to Figure 6–3:

(1) Refer to Figure 6–1 for the full design flow including the Quartus II software flowchart details.

(2) These are DxDesigner software-specific steps in the design flow and are not part of the I/O Designer flow.

For more information about the I/O Designer software, and to obtain usage, support, and product updates, use the Help menu in the I/O Designer software or refer to the Mentor Graphics website at www.mentor.com.

I/O Designer Database Wizard

All I/O Designer project information is stored in an I/O Designer Database (**.fpc**) file. You can create a new database that incorporates the FPGA Xchange file and Pin-Out file information generated by the Quartus II software by using the I/O Designer Database Wizard. You can also create a new, empty database and manually add the assignment information. If there is no signal or pin assignment information currently available, you can create an empty database that contains only a selection of the target device. This is useful if you know the signals in your design and the pins you want to assign. You can transfer this information at a later time to the Quartus II software for place-and-route.

It is possible to create an I/O Designer database with only one type of file or the other. However, if only a Pin-Out file is used, any I/O assignment changes made in the I/O Designer software cannot be imported back into the Quartus II software without first generating an FPGA Xchange file. If only an FPGA Xchange file is used to create the I/O Designer database, the database may not contain a complete picture of all of the I/O assignment information available. The FPGA Xchange file generated by the Quartus II software only lists pins with assigned signals. Since the Pin-Out file lists all device pins—whether signals are assigned to them or not—its use, along with the FPGA Xchange file, produces the most complete set of information for creating the I/O Designer Database.

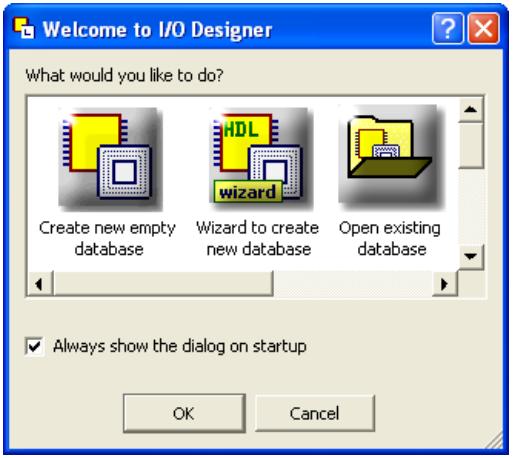
To create a new I/O Designer database using the Database Wizard, perform the following steps:

If you skip a step in this process, you can complete the skipped step later, filling in the appropriate information. To return to a skipped step, on the Properties menu, click **File**.

1. Start the I/O Designer software. The **Welcome to I/O Designer** dialog box appears (Figure 6–4). Select **Wizard to create new database** and click **OK**.

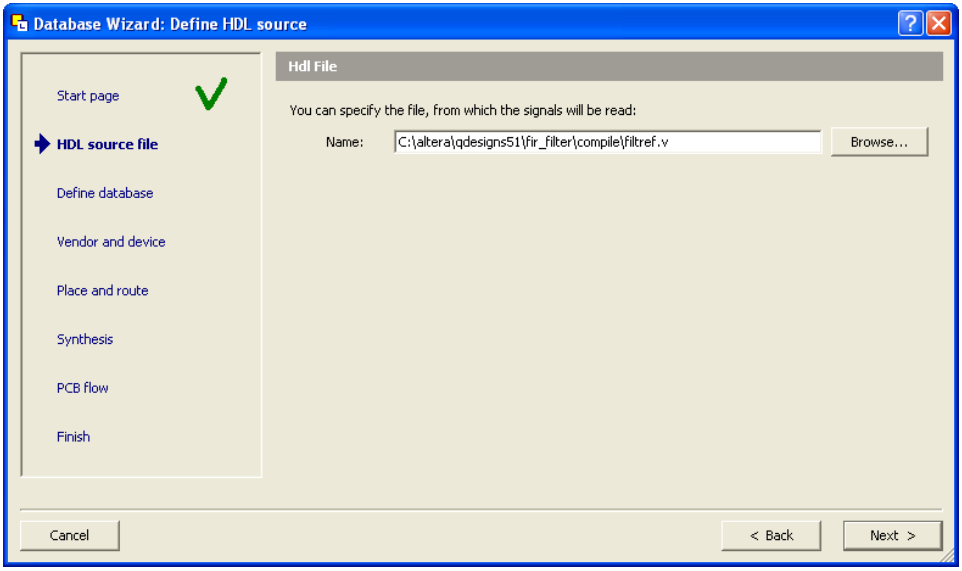
   If the **Welcome to I/O Designer** dialog box is not shown because it was disabled, you can access the Wizard through the menus. To access the Wizard on the File menu, click **Database Wizard**.

Figure 6–4. I/O Designer Welcome Dialog



2. Click **Next**. The **Define HDL source file** page opens (Figure 6–5).

Figure 6–5. Database Wizard HDL File Page



For more information about creating and using HDL files in the Quartus II software, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*, or refer to the I/O Designer Help.

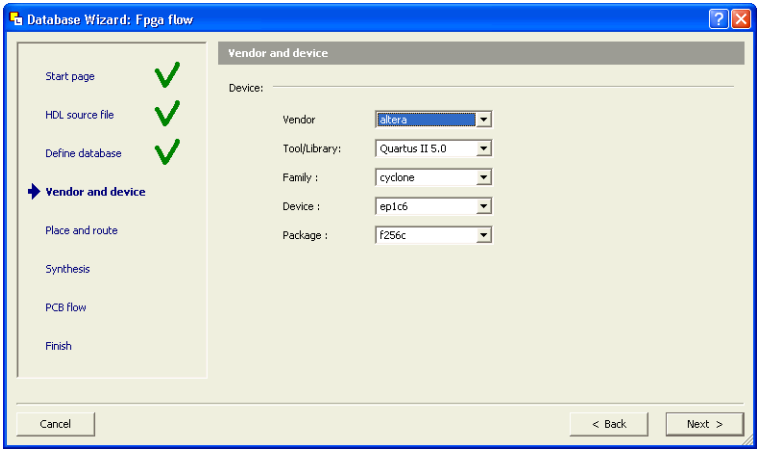
If no HDL files are available, or if your signal and pin assignments are already contained in the FPGA Xchange file, you do not have to complete step 3 and can proceed to step 4.

3. If you have created a Verilog HDL or VHDL file in your Quartus II software design, you can enter a top-level Verilog HDL or VHDL file. Adding a file allows you to create functional blocks or get signal names from your design. All physical pin assignments must be created in I/O Designer if no FPGA Xchange file or Pin-Out file is used. Click **Next**. The Database Name page is shown.

4. In the Database Name window, enter your database file name. Click **Next**. The Database Location window is shown.

5. Enter a path to the new database or an existing one in the **Location** field, or browse to a database location. Click **Next**. The **FPGA flow** page is shown (Figure 6–6).

Figure 6–6. Database Wizard Vendor & Device Page



6. In the Vendor menu, click **Altera**.

7. In the Tool/Library menu, click **Quartus II 5.0**, or a later version of the Quartus II software.

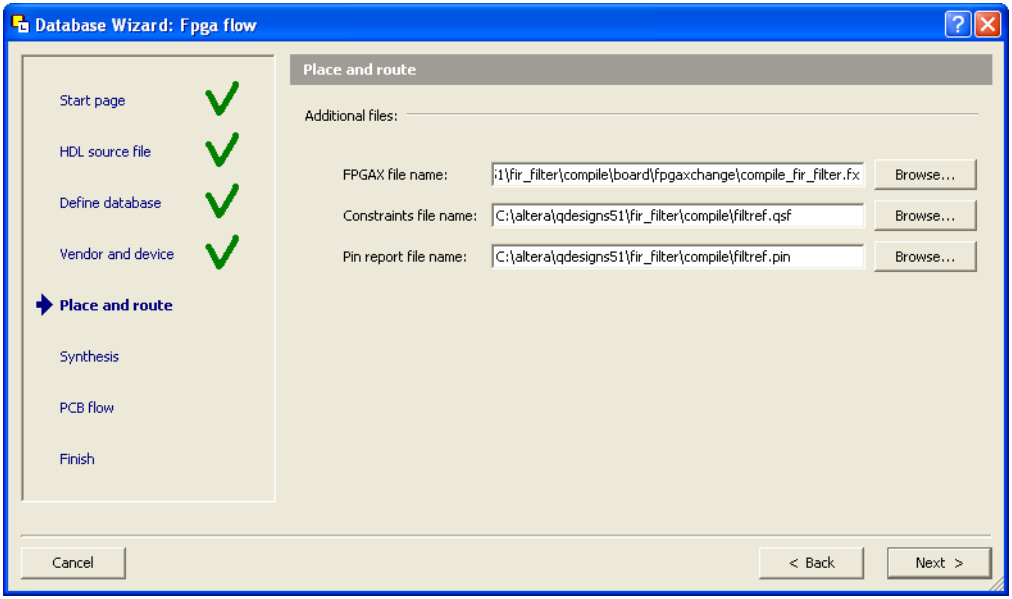
8. Select the appropriate device family, device, package, and speed (if applicable), from the corresponding menus. Click **Next**. The **Place and route** page is shown (Figure 6–7).

The Quartus II software version selections in the Tool/Library menu may not reflect the version of the Quartus II software currently installed on your system even if you are using the most current version of the I/O Designer software. The version number selection in this window is used in the I/O Designer software to identify the devices that were available or obsolete in that particular version of the Quartus II software. If you are unsure of the version to select, use the most recent version listed in the menu. If the device you are targeting does not appear in the device menu after making this selection, the device may be new and not yet added to the I/O Designer software. A list of unsupported devices for recent versions of the I/O Designer software can be found in Table 6–2. For I/O Designer software updates, contact Mentor Graphics or refer to their website at www.mentor.com.

Table 6–2. I/O Designer Unsupported Devices

Version of I/O Designer	Unsupported Devices
2005 (current release)	Stratix II GX
2004.2	Hardcopy II Stratix II GX

Figure 6–7. Database Wizard Place and Route Page



9. In the **FPGAX file name** field, type or browse to the backup copy of the FPGA Xchange file generated by the Quartus II software.

10. In the **Pin report file name** field, type or browse to the Pin-Out file generated by the Quartus II software. Click **Next**.

    In addition, you can select a Quartus II Settings File for update. The I/O Designer software can update the pin assignment information in the Quartus II Settings File without affecting any other information contained in the file.

    You can select a Pin-Out file without selecting an FPGA Xchange file for import. The I/O Designer software does not generate a Pin-Out file. To transfer assignment information to the Quartus II software, select an additional file and file type. Altera recommends selecting an FPGA Xchange file in addition to a Pin-Out file for transferring all of the assignment information contained within both types of files.

In some versions of the I/O Designer software, the standard file picker may incorrectly look for a Pin-Out file instead of an FPGA Xchange file. In this case, select **All Files (*.*)** from the **Save as type** list and select the file from the list.

11. The **Synthesis** page displays. On the **Synthesis** page, you can specify an external synthesis tool and a synthesis constraints file for use with the tool. If you do not use an external synthesis tool, click **Next**.

For more information about third-party synthesis tools, refer to volume 3 of the *Quartus II Handbook*.

12. The **PCB Flow** page is shown (Figure 6–8). On the **PCB Flow** page, you can select an existing schematic project or create a new project as a destination for symbol information.

    - To select an existing project, select **Choose existing project** and click **Browse** after the Project Path field. The **Select project** dialog box appears. Select the project.
    - To create a new project, in the **Select project** dialog box, select **Create new empty project**. Enter the project file name in the **Name** field and browse to the location where you want to save the file (Figure 6–9). Click **OK**.

Figure 6–8. PCB Flow Page

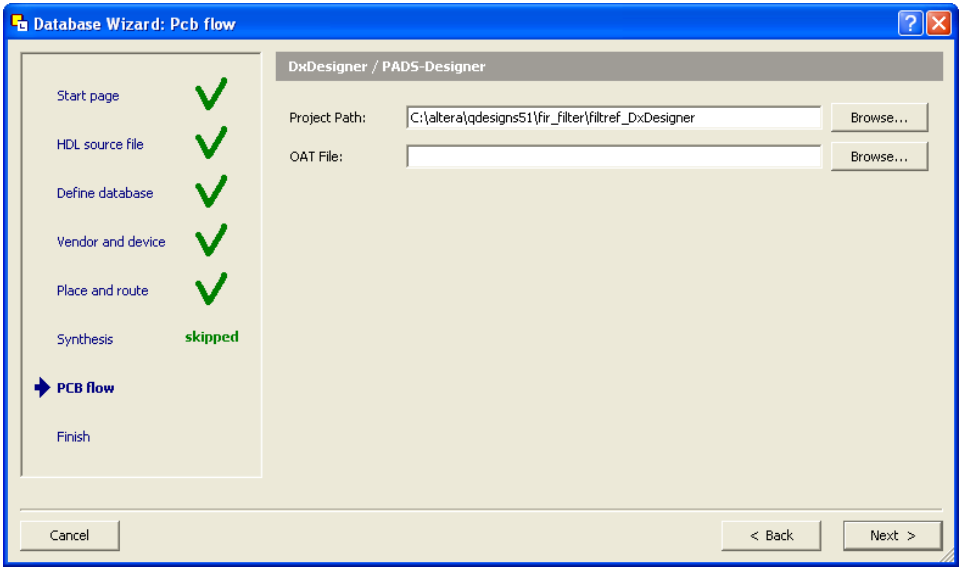
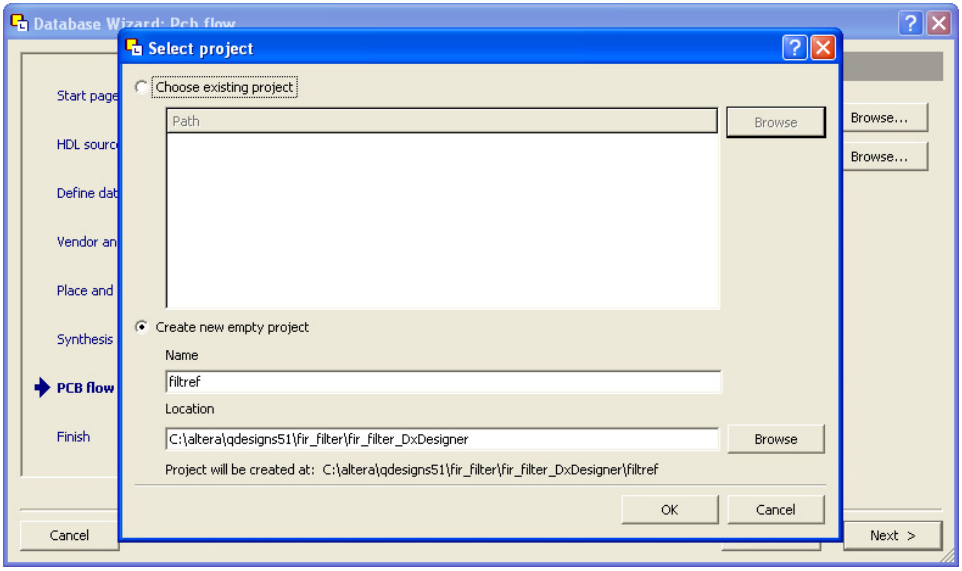


Figure 6–9. Select Project Dialog Box

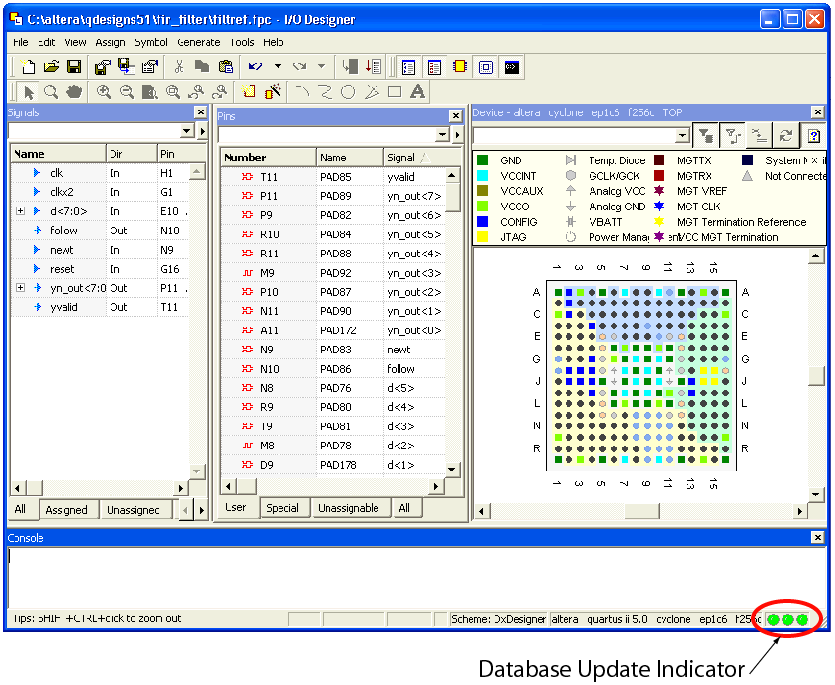


If you have not specified a design tool for sending symbol information to in I/O Designer, click **Advanced** in the **PCB Flow** page and select your design tool. If the DxDesigner software is selected, you have the option of specifying a Hierarchical Occurrence Attributes (**.oat**) file to import into the I/O Designer software (Figure 6–8). Click **Next**, then click **Finish** to create the database.

In I/O Designer version 2005 or later, the Update Wizard (refer to Figure 6–13 on page 6–21) is shown when you finish creating the database using the database wizard. Use the Update Wizard to confirm creation of the I/O Designer database using the selected FPGA Xchange and Pin-Out files.

Use the I/O Designer software and your newly created database to make pin assignment changes, create pin swap groups, or adjust signal and pin properties in the I/O Designer GUI (Figure 6–10).

Figure 6–10. I/O Designer Main Window

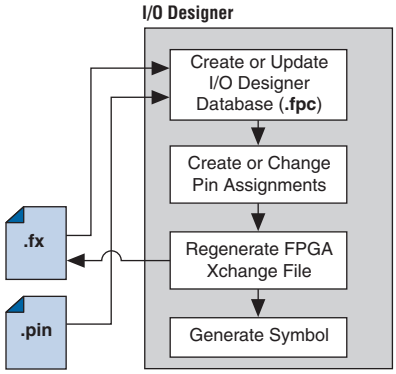


For more information about using the I/O Designer software and the DxDesigner software, refer to the Mentor Graphics website at www.mentor.com or refer to the I/O Designer software or the DxDesigner Help.

Updating Pin Assignments from the Quartus II Software

As the design process continues, the FPGA designer may need to make changes to the logic design in the Quartus II software that place signals on different pins after the design is recompiled, or manually by using the Quartus II Pin Planner. These types of changes must be carried forward to the circuit schematic and board layout tools to ensure that signals are connected to the correct pins on the FPGA. Updating the FPGA Xchange file and the Pin-Out file in the Quartus II software facilitates this flow (Figure 6–11).

Figure 6–11. Updating the I/O Designer Pin Assignments in the Design Flow *Note (1)*



Note to Figure 6–11:

(1) Refer to Figure 6–1 for the full design flow, which includes the Quartus II software, the DxDesigner software, and the board layout tool flowchart details.

To update the FPGA Xchange file and the Pin-Out file in the Quartus II software after making changes to the design, run a full compilation, or on the Start menu, point to Processing and click **Start EDA Netlist Writer**. The FPGA Xchange file in your selected output directory and the Pin-Out file in your project directory are updated. You must rerun the I/O Assignment Analyzer whenever you make I/O changes in the Quartus II software. To rerun the I/O Assignment Analyzer, on the Processing menu, click **Start Compilation**, or to run a full compilation, on the Processing menu, point to Start and click **Start I/O Assignment Analysis**.

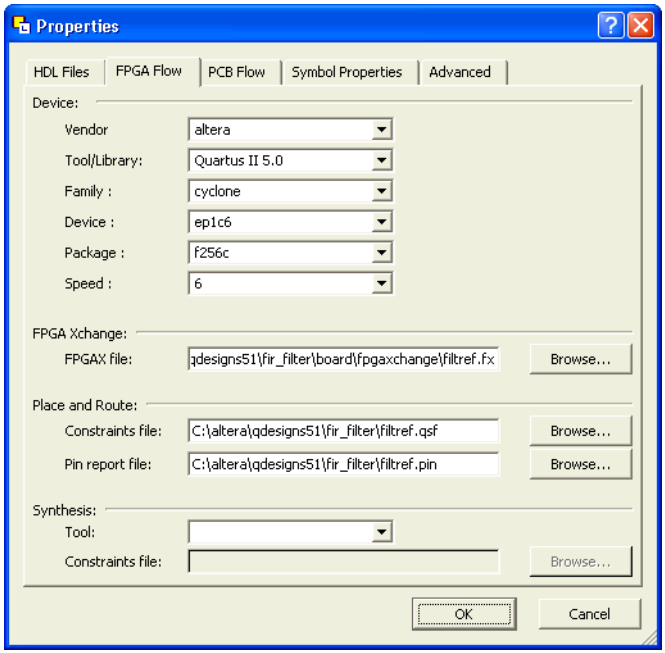
Refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook* for more information about setting up the FPGA Xchange file and running the I/O Assignment Analyzer.

If your I/O Designer database points to the FPGA Xchange file generated by the Quartus II software instead of a backup copy of the file, updating the file in the Quartus II software overwrites any changes made to the file by the I/O Designer software. If there are I/O Designer assignments in the FPGA Xchange file that you want to preserve, create a backup copy of the file before updating it in the Quartus II software, and verify that your I/O Designer database points to the backup copy. To point to the backup copy, perform the steps in the following section.

Whenever the FPGA Xchange file or the Pin-Out file is updated in the Quartus II software, the changes can be imported into the I/O Designer database. You must set up the locations for the files in the I/O Designer software.

1. To set up the file locations if they are not already set, on the File menu, click **Properties**. The Project Properties dialog box appears (Figure 6–12).

Figure 6–12. Project Properties Dialog Box



2. Under **FPGA Xchange**, click **Browse** to select the FPGA Xchange file name and file location.

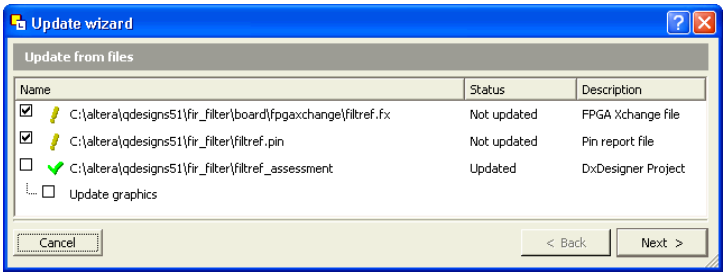
3. To specify a Pin report file, under **Place and Route**, click **Browse** to select the Pin-Out file name and file location.

Once you have set up these file locations, the I/O Designer software monitors these files for changes. If the FPGA Xchange file or Pin-Out file changes during the design flow, three indicators flash red in the lower right-hand corner of the I/O Designer main window (see Figure 6–10 on page 6–17). You can continue working or click on the indicators to open the I/O Designer Update Wizard. If you have made changes to your design in the Quartus II software that result in an updated FPGA Xchange file or Pin-Out file and the update indicators do not flash or you have previously canceled an indicated update, manually open the Update Wizard. To open the Wizard, on the File menu, click **Update**.

In versions of the I/O Designer software before version 2005, instead of using flashing indicators, the I/O Designer software displays a dialog box asking if you want to open the Update Wizard.

The I/O Designer Update Wizard lists the updated files associated with the database (Figure 6–13).

Figure 6–13. Update Wizard Dialog Box



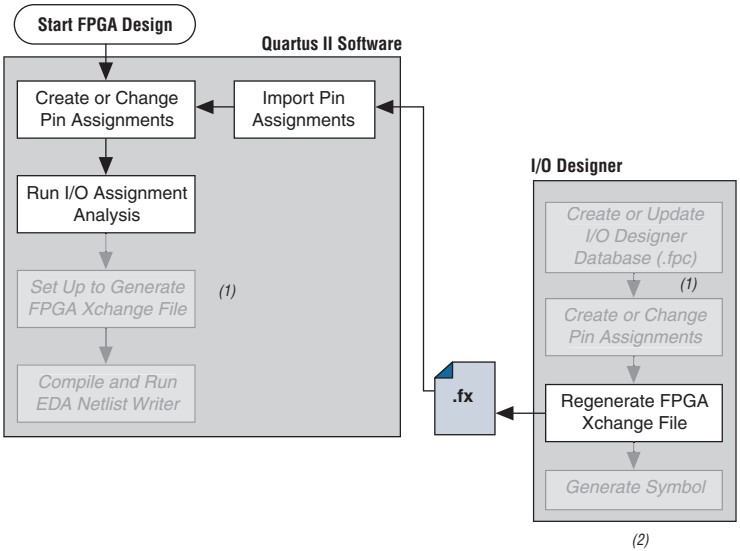
The paths to the updated files have yellow exclamation points and the **Status** column shows **Not updated**, indicating that the database has not yet been updated with the newer information contained in the files. A checkmark to the left of any updated file indicates that the file will update the database. Turn on any files you want to use to update the I/O Designer database, and click **Next**. If you are not satisfied with the database update, on the Edit menu, click **Undo**.

You can update the I/O Designer database using both the FPGA Xchange file and the Pin-Out file at the same time. Turning on both the FPGA Xchange file and the Pin-Out file for update causes the Update Wizard to provide options for using assignments from one file or the other exclusively or merging the assignments contained in both files into the I/O Designer database. Versions of the I/O Designer software older than version 2005 simply merge assignments contained in multiple files.

Sending Pin Assignment Changes to the Quartus II Software

In the same way that the FPGA designer can make adjustments that affect the PCB design, the board designer can make changes to optimize signal routing and layout that must be applied to the FPGA. The FPGA designer can take these required changes back into the Quartus II software to refit the logic to match the adjustments to the pinout. The I/O Designer software can accommodate this reverse flow as shown in Figure 6–14.

Figure 6–14. Updating the Quartus II Pin Assignments in the Reverse Design Flow



Notes to Figure 6–14:

(1) These are software-specific steps in the design flow and are not necessary for the reverse flow steps of the design.

(2) Refer to Figure 6–1 for the full design flow, which includes the complete I/O Designer software, the DxDesigner software, and the board layout tool flowchart details.

Pin assignment changes are made directly in the I/O Designer software, or the software automatically updates changes made in a board layout tool that are back-annotated to a schematic entry program such as the DxDesigner software. You must update the FPGA Xchange file to reflect these updates in the Quartus II software. To perform this update in the I/O Designer software, on the Generate menu, click **FPGA Xchange File**.

CAUTION

If your I/O Designer database points to the FPGA Xchange file generated by the Quartus II software instead of a backup copy, updating the file from the I/O Designer software overwrites any changes that may have been made to the file by the Quartus II software. If there are assignments from the Quartus II software in the file that you want to preserve, make a backup copy of the file before updating it in the I/O Designer software, and verify that your I/O Designer database points to the backup copy. To point to the backup copy, perform the steps in "Updating Pin Assignments from the Quartus II Software" on page 6–18.

After the FPGA Xchange file is updated, you must import it into the Quartus II software. To import the file, perform the following steps:

1. Start the Quartus II software and open your project.
2. On the Assignments menu, click **Import Assignments**.
3. In the File name box, click **Browse** and from the **Files of type** list, select **FPGA Xchange Files (*.fx)**.
3. Select the FPGA Xchange file and click **Open**.
4. Click **OK**.

Both the Quartus II software and the I/O Designer software can export and import an FPGA Xchange file. It is therefore possible to overwrite the FPGA Xchange file and import incorrect assignments into one or both programs. To prevent this occurrence from happening, make a backup copy of the file before importing, and import the copy instead of the file generated by the Quartus II software. In addition, assignments in the Quartus II software can be protected by following the steps in "Protecting Assignments in the Quartus II Software" on page 6–23.

Protecting Assignments in the Quartus II Software

To protect assignments in the Quartus II software, use the following steps:

1. Start the Quartus II software.
2. On the Assignments menu, click **Import Assignments**. The Import Assignments dialog box appears.
3. Turn on **Copy existing assignments into** <*project name*>**.qsf.bak before importing** before importing the FPGA Xchange file. This action automatically creates a backup Quartus II constraints file that contain all of your current pin assignments.

Generating Symbols for the DxDesigner Software

Along with circuit simulation, circuit board schematic creation is one of the first tasks required in the design of a new PCB. Schematics are required to understand how the PCB will work, and to generate a netlist

that is passed to a board layout tool for board design and routing. The I/O Designer software provides the ability to create schematic symbols based on the FPGA design exported from the Quartus II software.

Most FPGA devices contain hundreds of pins, requiring large schematic symbols that may not fit on a single schematic page. Symbol designs in the I/O Designer software can be split or fractured into a number of functional blocks, allowing multiple part fractures on the same schematic page or across multiple pages. In the DxDesigner software, these part fractures are joined together with the use of the `HETERO` attribute.

The I/O Designer software can generate symbols for use in a number of Mentor Graphics schematic entry tools, and can import changes back-annotated by board layout tools to update the database and feed updates back to the Quartus II software using the FPGA Xchange file. This section discusses symbol creation specifically for the DxDesigner software.

Schematic symbols are created in the I/O Designer software in the following ways:

- Manually
- Using the I/O Symbol Wizard
- Importing previously created symbols from the DxDesigner software

The I/O Designer Symbol Wizard can be used as a design base that allows you to quickly create a symbol for manual editing at a later time. If you have already created symbols in a DxDesigner project and want to apply a different FPGA design to them, you can manually import these symbols from the DxDesigner project. To import the symbols, open the I/O Designer software, and on the File menu, click **Import Symbol**.

For more information about importing symbols from the DxDesigner software into an I/O Designer database, refer to the I/O Designer Help.

Symbols created in the I/O Designer software are either functional, physical (PCB), or a combination of functional and physical. A functional symbol is based on signals imported into the database, usually from Verilog HDL or VHDL files. No physical device pins must be associated with the signals to generate a functional symbol. This section focuses on board-level PCB symbols with signals directly mapped to physical device pins through assignments in either the Quartus II Pin Planner or in the I/O Designer database.

For information about manually creating symbols, importing symbols, and editing symbols in the I/O Designer software, as well as the different types of symbols the software can generate, refer to the I/O Designer Help.

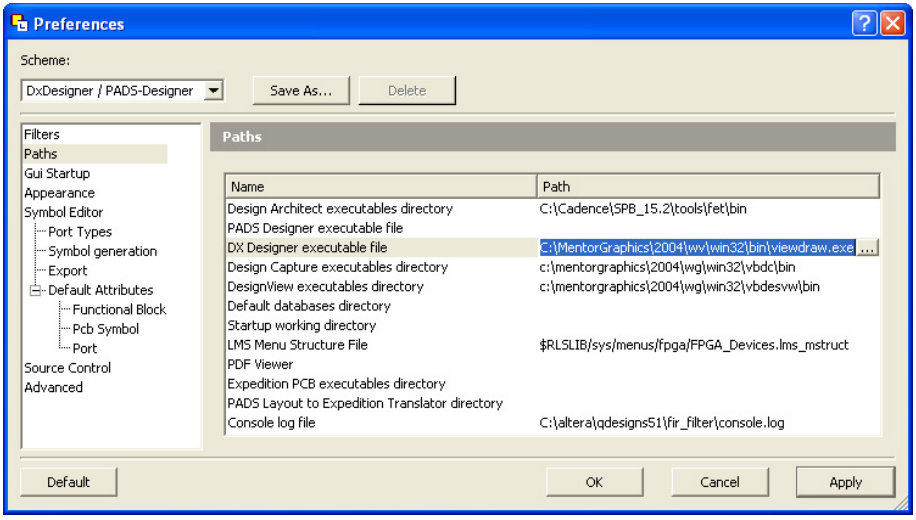
Setting Up the I/O Designer Software to Work with the DxDesigner Software

If you created your I/O Designer database using the Database Wizard, you may already be set up to export symbols to a DxDesigner project. To verify this, or to manually set up the I/O Designer software to work with the DxDesigner software, you must set the path to the DxDesigner executable, set the export type to DxDesigner, and set the path to a DxDesigner project directory.

To set these options, perform the following steps:

1. Start the I/O Designer software.
2. On the Tools menu, click **Preferences**. The Preferences dialog box appears.
3. Click **Paths**, double-click on the DxDesigner executable file path field, and click **Browse** to select the location of the DxDesigner application (Figure 6–15). Click **Apply**.

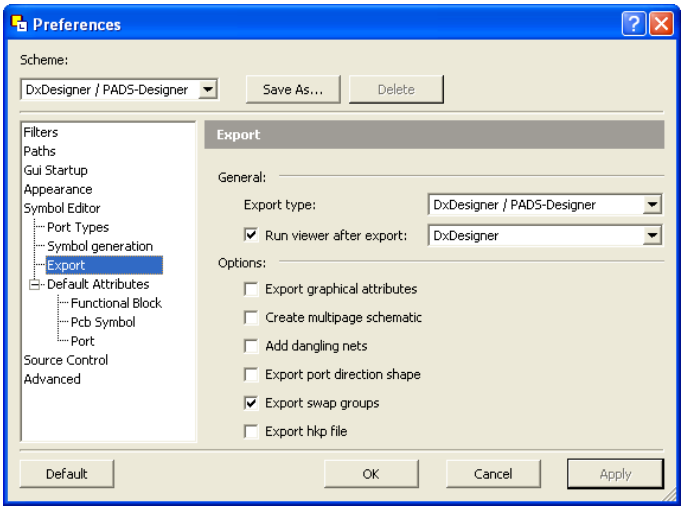
Figure 6–15. Path Preferences Dialog Box



4. Click **Symbol Editor** and click **Export**. In the Export type menu, under General, select **DxDesigner/PADS-Designer** (Figure 6–16).

5. Click **Apply** and click **OK**.

Figure 6–16. Symbol Editor Export Preferences



6. On the File menu, click **Properties**. The project Properties dialog box appears.

7. Click the **PCB Flow** tab and click **Path to a DxDesigner project directory**.

8. Click **OK**.

If you did not create a new DxDesigner project in the Database Wizard and you do not already have a DxDesigner project, you must create a new database using the DxDesigner software, and point the I/O Designer software to this new project.

For information about creating and working with DxDesigner projects, refer to the DxDesigner Help.

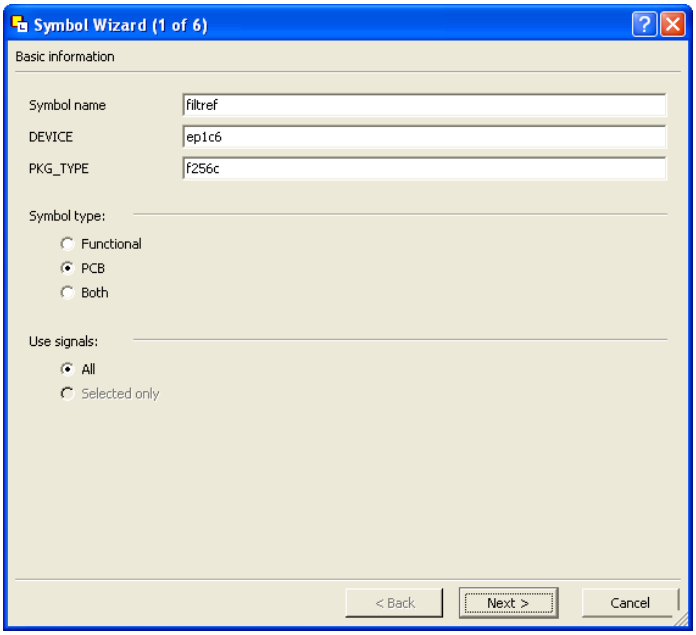
Create Symbols with the Symbol Wizard

FPGA symbols based on Altera devices can be created, fractured, and edited using the I/O Designer Symbol Wizard. To create a symbol based on a selected Altera FPGA device:

1. Start the I/O Designer software.

2. Click **Symbol Wizard** in the toolbar, or on the Symbol menu, click **Symbol Wizard**. The **Symbol Wizard (1 of 6) page** is shown (Figure 6–17).

Figure 6–17. Symbol Wizard



3. On the first Symbol Wizard page, in the **Symbol name** field, enter the symbol name. The **DEVICE** and **PKG_TYPE** fields are populated with the device and package information automatically. Under Symbol type, click **PCB**. Under Use signals, click **All**.

4. Click **Next**. The **Symbol Wizard (2 of 6)** page is shown.

If the **DEVICE** and **PKG_TYPE** fields are blank or incorrect, cancel the Symbol Wizard and select the correct device information. On the File menu, click **Properties**. In the Properties window, click the **FPGA Flow** tab and enter the correct device information.

5. On page 2 of the Symbol Wizard, select fracturing options for your symbol. If you are using the Symbol Wizard to edit a previously created fractured symbol, you must turn on **Reuse existing fractures** so that your current fractures are not altered. Select other options on this page as appropriate for your symbol.

6. Click **Next**. The **Symbol Wizard (3 of 6)** page is shown.

7. Additional fracturing options are available on page 3 of the Symbol Wizard. After selecting the desired options, click **Next**. The **Symbol Wizard (4 of 6)** page is shown.

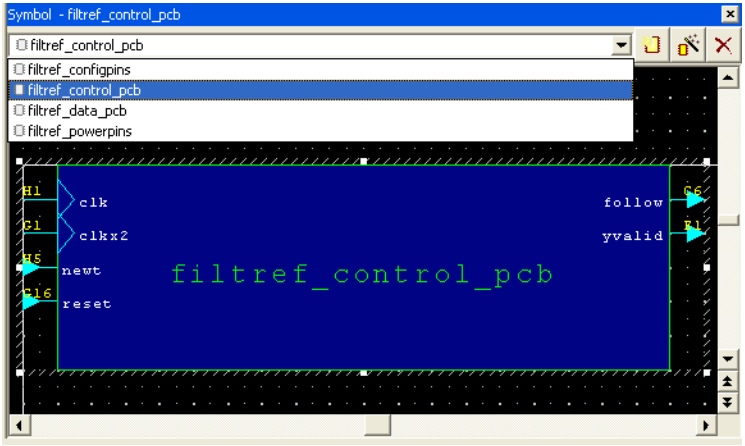
8. On page 4 of the Symbol Wizard, select the options for how the symbols will look. Select the desired options and click **Next**. The **Symbol Wizard (5 of 6)** page is shown.

9. On page 5 of the Symbol Wizard, define what information will be labeled for the entire symbol and for individual pins. Select the desired options and click **Next**. The **Symbol Wizard (6 of 6)** page is shown.

10. On the final page of the Symbol Wizard, add additional signals and pins that have not already been placed in the symbol. Click **Finish** when you complete your selections.

Your symbol is complete. You can view your symbol and any fractures you created using the Symbol Editor (Figure 6–18). You can edit parts of the symbol, delete fractures, or rerun the Symbol Wizard.

Figure 6–18. The I/O Designer Symbol Editor



If assignments in the I/O Designer database are updated, the symbols created in the I/O Designer software automatically reflect these changes. Assignment changes can be made within the I/O Designer software, with an updated FPGA Xchange file from the Quartus II software, or from a back-annotated change in your board layout tool.

Export Symbols to the DxDesigner Software

After you have completed your symbols, export the symbols to your DxDesigner project. To generate all the fractures of a symbol, on the Generate menu, click **All Symbols**. To generate a symbol for the currently displayed symbol in Symbol Editor, click **Current Symbol Only**. Each symbol in the database is saved as a separate file in the **/sym** directory in your DxDesigner project. The symbols can be instantiated in your DxDesigner schematics.

For more information about working with DxDesigner projects, refer to the DxDesigner Help.

Scripting Support

The I/O Designer software features a command line Tcl interpreter. All commands issued through the GUI in the I/O Designer software are translated into Tcl commands that are run by the tool. You can view the generated Tcl commands and run scripts, or enter individual commands in the I/O Designer Console window.

The following section includes commands that perform some of the operations described in this chapter.

If you want to change the FPGA Xchange file from which the I/O Designer software updates assignments, type the following command at an I/O Designer Tcl prompt:

```
set_fpga_xchange_file <file name>
```

After the FPGA Xchange file is specified, use the following command to update the I/O Designer database with assignment updates made in the Quartus II software:

```
update_from_fpga_xchange_file
```

Use the following command to update the FPGA Xchange file with changes made to the assignments in the I/O Designer software for transfer back into the Quartus II software:

```
generate_fpga_xchange_file
```

If you want to import assignment data from a Pin-Out file created by the Quartus II software, use the following command:

```
set_pin_report_file -quartus_pin <file name>
```

Run the I/O Designer Symbol Wizard with the following command:

```
symbolwizard
```

Set the DxDesigner project directory path where symbols are saved with the following command:

```
set_dx_designer_project -path <path>
```

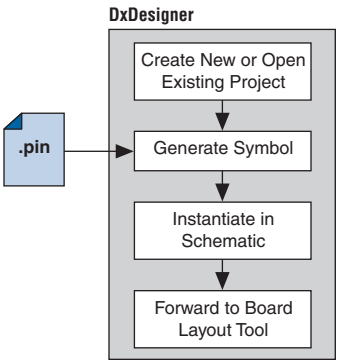
For more information about Tcl scripting and Tcl scripting with the Quartus II software, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. For more information about the Tcl scripting capabilities of the I/O Designer software as well as a list of all the commands available, refer to the I/O Designer Help.

FPGA-to-Board Integration with the DxDesigner Software

The Mentor Graphics DxDesigner software is a design entry tool for schematic capture. You can use it to create flat circuit schematics for all types of PCB design. You can also use the DxDesigner software to create hierarchical schematics that facilitate design reuse and a team-based design. You can use the DxDesigner software in the design flow alone or in conjunction with the I/O Designer software. However, if you use the DxDesigner software without the I/O Designer software, the design flow is one-way, using only the Pin-Out file generated by the Quartus II software.

Signal and pin assignment changes can be made only in the Quartus II software and are reflected in updated symbols in a DxDesigner schematic. You cannot back-annotate changes made in a board layout tool or in a DxDesigner symbol to the Quartus II software. Figure 6–19 shows the design flow when the I/O Designer software is not used.

Figure 6–19. Design Flow Without the I/O Designer Software *Note (1)*



Note to Figure 6–19:

(1) Refer to Figure 6–1 for the full design flow, which includes the Quartus II software, the I/O Designer software, and the board layout tool flowchart details.

For more information about the DxDesigner software, including usage, support, training, and product updates, refer to the Mentor Graphics web page at www.mentor.com, or choose Schematic Design Help Topics in the DxDesigner Help.

DxDesigner Project Settings

New projects in the DxDesigner software are already set up to create FPGA symbols by default. However, for complete support and compatibility with the I/O Designer software, if it is used with the DxDesigner software, you should enable the DxBoardLink Flow options.

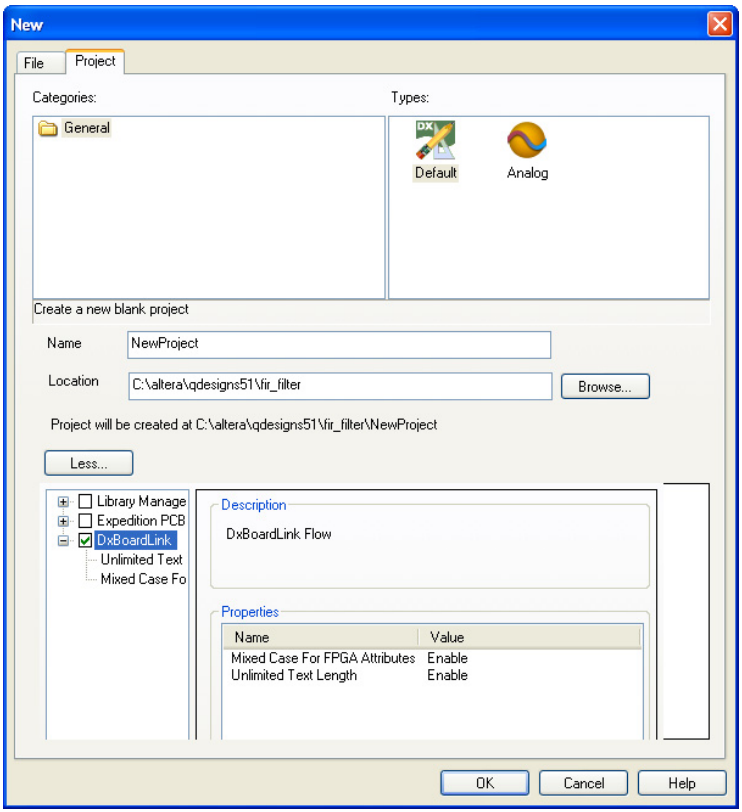
You can enable the DxBoardLink flow design configuration while creating a new DxDesigner project or after a project is created.

To enable the DxBoardLink flow design configuration when creating a new DxDesigner project, perform the following steps:

1. Start the DxDesigner software.

2. On the File menu, click **New** and click the **Project** tab. The New Project dialog box appears.

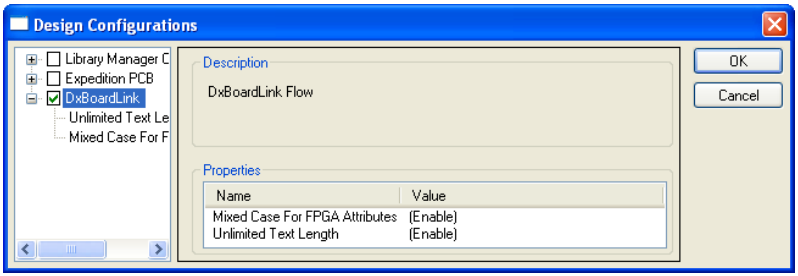
Figure 6–20. New Project Dialog Box



3. Click **More**. Turn on **DxBoardLink**. (Figure 6–20)

To enable the DxBoardLink Flow design configuration in an existing project, click **Design Configurations** in the Design Configuration toolbar and turn on **DxBoardLink** (Figure 6–21).

Figure 6–21. DxBoardLink Design Configuration



DxDesigner Symbol Wizard

In addition to circuit simulation, circuit board schematic creation is one of the first tasks required in the design of a new PCB. Schematics are required to understand how the PCB will work, and to generate a netlist that is passed on to a board layout tool for board stackup design and routing.

You can create schematic symbols using the DxDesigner software based on FPGA designs exported from the Quartus II software through the Pin-Out file for instantiation in DxDesigner schematic design files. Most FPGA devices are physically large with hundreds of pins, requiring large schematic symbols that may not fit on a single schematic page. You can split or fracture symbols created in the DxDesigner software into a number of functional blocks, allowing multiple part fractures on the same schematic page or across multiple pages. In the DxDesigner software, these part fractures are joined together with the use of the `HETERO` attribute.

You can create schematic symbols in the DxDesigner software manually or with the Symbol Wizard. The DxDesigner Symbol Wizard is similar to the I/O Designer Symbol Wizard, but with fewer fracturing options.

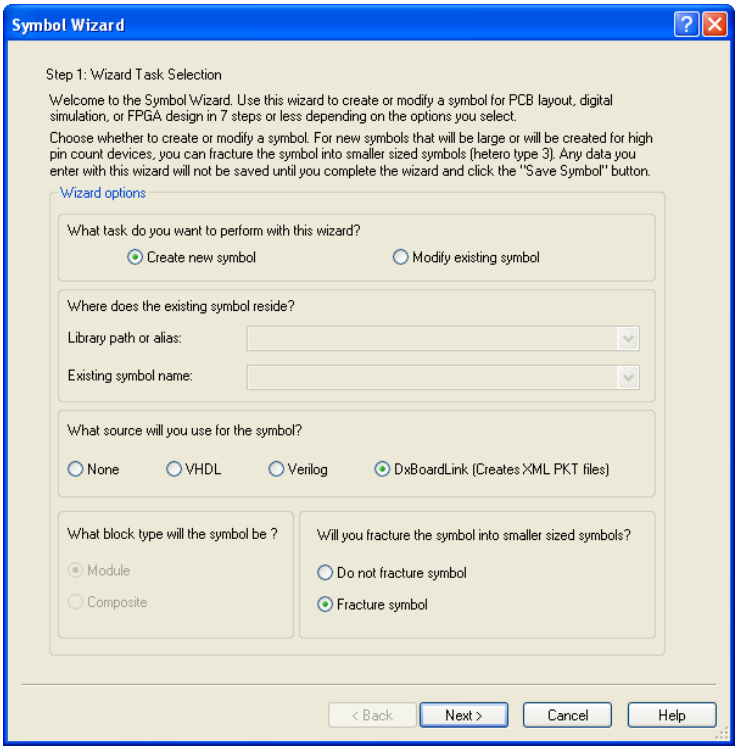
FPGA symbols based on Altera devices can be created, fractured, and edited using the DxDesigner Symbol Wizard. To start the Symbol Wizard, perform the following steps:

1. Start the DxDesigner software.

2. Click **Symbol Wizard** in the toolbar, or on the File menu, click **New**. The New window is shown. Click the **File** tab and create a new file of type **Symbol Wizard**.

3. Enter the new symbol name in the name field and click **OK**. The **Symbol Wizard** page is shown (Figure 6–22).

Figure 6–22. Wizard Task Selection



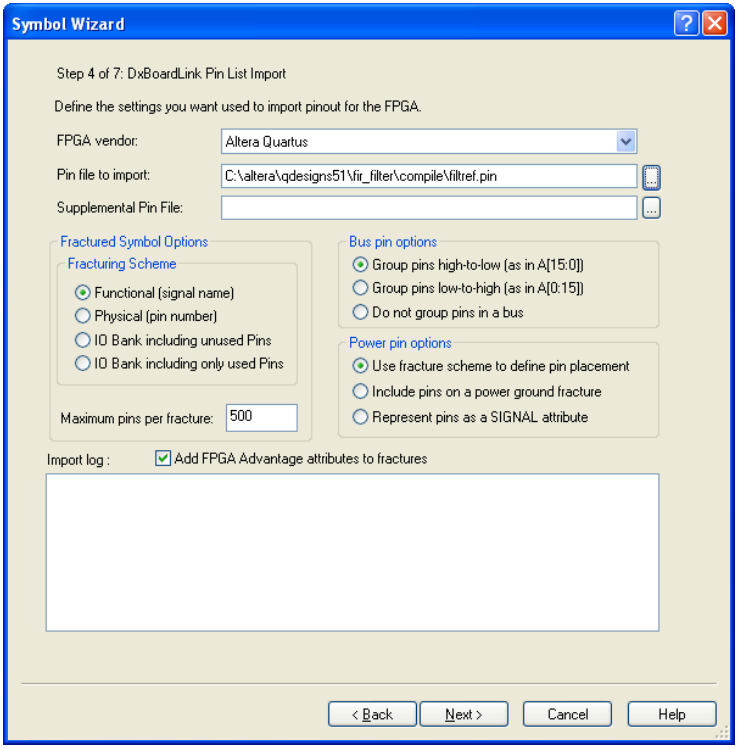
4. On the **Wizard Task Selection** page, choose to create a new symbol or modify an existing symbol. If you are modifying an existing symbol, specify the library path or alias, and select the existing symbol. If you are creating a new symbol, select DxBoardLink for the symbol source. The DxDesigner block type defaults to Module

because the FPGA design does not have an underlying DxDesigner schematic. Define whether or not to fracture the symbol. After making your selections, click **Next**. The **New Symbol and Library Name** page is shown.

5. On the **New Symbol and Library Name** page, enter a name for the symbol, an overall part name for all of the symbol fractures, and a library name for the new library created for this symbol. By default, the part and library names are the same as the symbol name. Click **Next**. The **Symbol Parameters** page is shown.

6. On the **Symbol Parameters** page, decide how the generated symbol will look and how it will match up with the grid you have set in your DxDesigner project schematic. After making your selections, click **Next**. The **DxBoardLink Pin List Import** page is shown (Figure 6–23).

Figure 6–23. DxBoardLink Pin List Import



7. On the **DxBoardLink Pin List Import** page, in the **FPGA vendor** list, select **Altera Quartus**. In the Pin-Out file to import field, browse to and select the Pin-Out file from your Quartus II design project directory. Additionally, select choices from the Fracturing Scheme options, Bus pin options, and Power pin options. After you make your selections, click **Next**. The **Symbol Attributes** page is shown.

8. On the **Symbol Attributes** page, select to create or modify symbol attributes for use in the DxDesigner software. After you make your selections, click **Next**. The **Pin Settings** page is shown.

9. On the **Pin Settings** page, make any final adjustments to pin and label location and information. Each tabbed spreadsheet represents a fracture of your symbol. After you make your selections, click **Save Symbol**.

After you save the symbol, you can examine and place any fracture of the symbol in your schematic. When you are finished with the Symbol Wizard, all the fractures you created are saved as separate files in the library you specified or created in the **/sym** directory in your DxDesigner project. You can add the symbols to your schematics or you can edit the symbols manually or with the Symbol Wizard.

Symbols created in the DxDesigner software can be edited and updated with newer versions of the Pin-Out file generated by the Quartus II software. However, symbol fracturing is fixed, and the symbol cannot be fractured again. To create new fractures for your design, create a new symbol in the Symbol Wizard, and follow the steps in "DxDesigner Symbol Wizard" on page 6–33.

For more information about creating, editing, and instantiating component symbols in DxDesigner, choose Schematic Design Help Topics from the Help menu in the DxDesigner software.

Conclusion

Transferring a complex, high-pin-count FPGA design to a PCB for prototyping or manufacturing is a daunting process that can lead to errors in the PCB netlist or design, especially when multiple engineers are working on different parts of the project. The design workflow available when the Quartus II software is used in conjunction with the Mentor Graphics toolset assists the FPGA designer and the board designer in preventing errors and focusing their attention on the design.

7. Cadence PCB Design Tools Support

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Introduction

With today's large, high-pin-count and high-speed FPGA devices, good printed circuit board (PCB) design practices are more essential than ever to ensure the correct operation of your system. Typically, the PCB design takes place concurrently with the design and programming of the FPGA. Signal and pin assignments are initially made by the FPGA or ASIC designer, and it is up to the board designer to correctly transfer these assignments to the symbols used in their system circuit schematics and board layout. As the board design progresses, pin reassignments may be requested or required to optimize the layout. These reassignments must in turn be relayed to the FPGA designer so that the new assignments can be processed through the FPGA using updated place-and-route.

Cadence provides tools to support this type of design flow. This chapter addresses how the Quartus II software interacts with the Cadence Allegro Design Entry HDL software and the Allegro Design Entry CIS (Component Information System) software (also known as OrCAD Capture CIS) to provide a complete FPGA-to-board integration design workflow. This chapter provides information about the following topics:

- Cadence tool description, history, and comparison
- The general design flow between the Quartus II software and the Cadence Allegro Design Entry HDL software and the Cadence Allegro Design Entry CIS software
- Generating schematic symbols from your FPGA design for use in the Cadence Allegro Design Entry HDL software
- Updating Design Entry HDL symbols when signal and pin assignment changes are made in the Quartus II software
- Creating schematic symbols in the Cadence Allegro Design Entry CIS software from your FPGA design
- Updating symbols in the Cadence Allegro Design Entry CIS software when signal and pin assignment changes are made in the Quartus II software
- Using Altera®-provided device libraries in the Cadence Allegro Design Entry CIS software

This chapter is intended primarily for board design and layout engineers who want to begin the FPGA board integration process while the FPGA is still in the design phase. In addition, part librarians benefit from learning how to take output from the Quartus II software and use it to create new library parts and symbols.

The instructions in this chapter require the following software:

- The Quartus II software version 5.1 or later
- The Cadence Allegro Design Entry HDL or the Cadence Allegro Design Entry CIS software version 15.2 or later
- If you are using the OrCAD Capture software, you must have version 10.3 or later (CIS is optional)

Because the Cadence Allegro Design Entry CIS software is based on OrCAD Capture, these programs are very similar. For this reason, this chapter refers to the Allegro Design Entry CIS software in directions; however, these directions also apply to OrCAD Capture unless otherwise noted.

To obtain and license the Cadence tools described in this chapter, and for product information, support, and training, refer to the Cadence website, www.cadence.com. For information about OrCAD Capture and the CIS option, refer to the OrCAD website, www.orcad.com. For Cadence and OrCAD support and training, refer to the EMA Design Automation website, www.ema-eda.com.

Product Comparison

The design tools described in this chapter have similar functionality, but there are differences in their use as well as where to access product information. Table 7–1 lists the products described in this chapter and provides information about changes, product information, and support.

Table 7–1. Cadence & OrCAD Product Comparison

	Cadence Allegro Design Entry HDL	Cadence Allegro Design Entry CIS	OrCAD Capture CIS
Former Name	Concept HDL Expert	Capture CIS Studio	N/A
History	More commonly known by its former name, Cadence renamed all board design tools in 2004 under the Allegro name.	Based directly on OrCAD Capture CIS, this tool is still developed by OrCAD but sold and marketed by Cadence. EMA provides support and training.	The basis for Design Entry CIS is still developed by OrCAD for continued use by existing OrCAD customers. EMA now provides support and training for all OrCAD products.
Vendor Design Flow	Cadence Allegro 600 series, formerly known as Expert Series, for high-end, high-speed design.	Cadence Allegro 200 series, formerly known as Studio Series, for small- to medium-level design.	N/A
Information & Support	www.cadence.com www.ema-eda.com	www.cadence.com www.ema-eda.com www.orcad.com	www.ema-eda.com www.orcad.com

FPGA-to-PCB Design Flow

In the examples in this section, you create a design flow integrating an Altera FPGA design from the Quartus II software through a circuit schematic in the Allegro Design Entry HDL software (Figure 7–1) or the Allegro Design Entry CIS software (Figure 7–2).

Figure 7–1. Design Flow with the Allegro Design Entry HDL Software

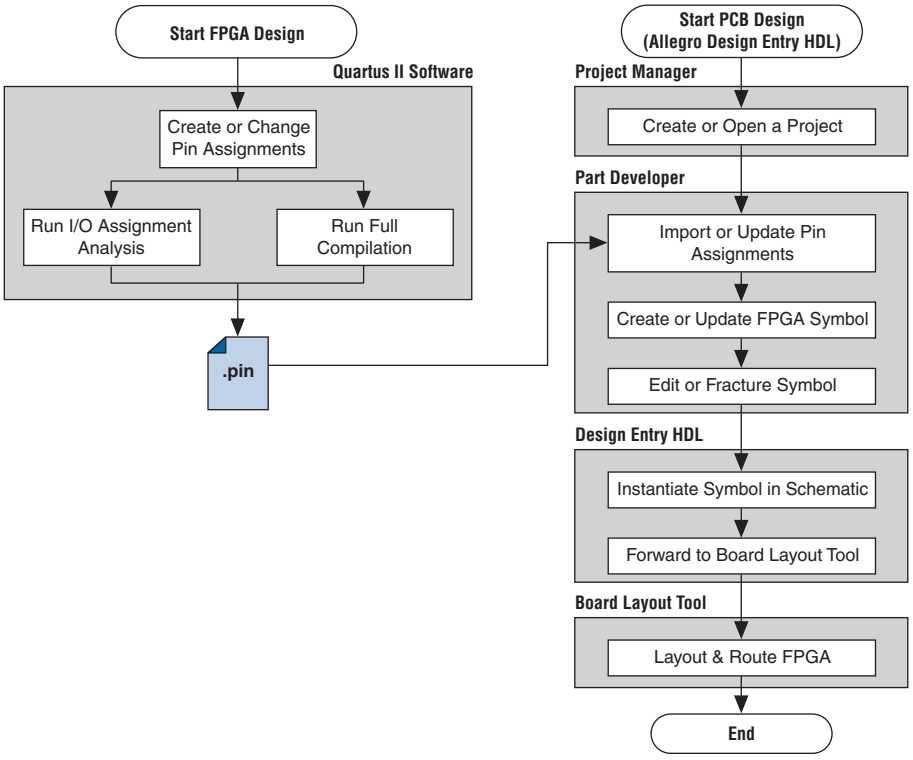
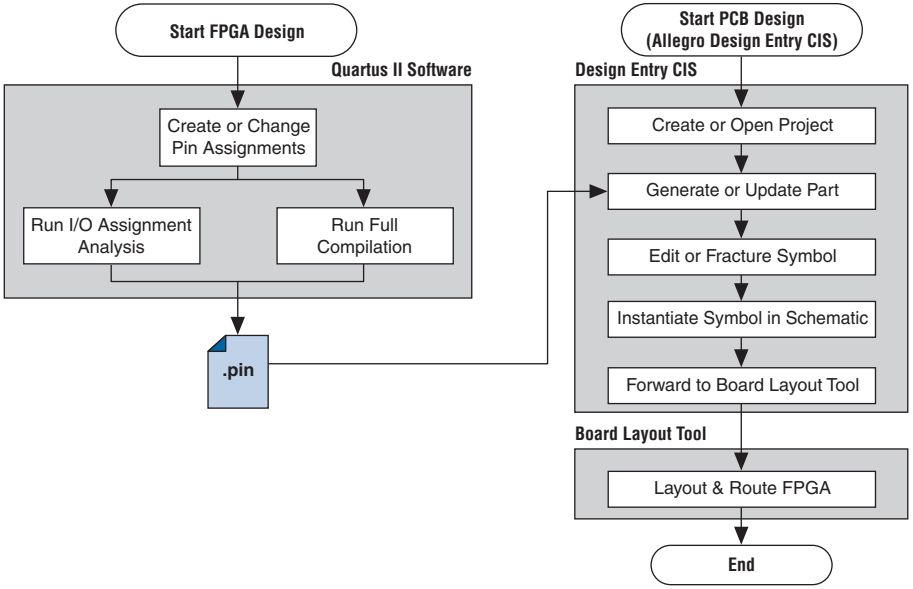


Figure 7–2. Design Flow with the Allegro Design Entry CIS Software



The basic steps in a complete design flow to integrate an Altera FPGA design starting in the Quartus II software through to a circuit schematic in Design Entry HDL or Design Entry CIS are as follows:

- Start the Quartus II software.
- In the Quartus II software, compile your design to generate a Pin-Out (**.pin**) file to transfer assignments to the Cadence tool.
- If you are using the Cadence Allegro Design Entry HDL software for your schematic design:
  - Open an existing project or create a new project in the Allegro Project Manager.
  - Construct a new symbol or update an existing symbol using the Allegro PCB Librarian Part Developer.
  - With the Part Developer, edit your symbol or fracture it into smaller parts, if desired.
  - Instantiate the symbol in your Design Entry HDL software schematic and transfer the design to your board layout tool.

- If you are using the Cadence Allegro Design Entry CIS software for your schematic design, perform the following steps:
  - Generate a new part within an existing or new Allegro Design Entry CIS project, referencing the Pin-Out file output from the Quartus II software. You can update an existing symbol with a new Pin-Out file.
  - Split the symbol into smaller parts as desired.
  - Instantiate the symbol in your Design Entry CIS schematic and transfer the design to your board layout tool.

Figures 7–1 and 7–2 show the possible design flows, depending on your tool choice. The Cadence PCB Librarian Expert license is required to use the PCB Librarian Part Developer to create FPGA symbols. You can update symbols with changes made to the FPGA design at any point using any of these tools.

Setting Up the Quartus II Software

You can transfer pin and signal assignments from the Quartus II software to the Cadence design tools by generating the Quartus II project Pin-Out file. The Pin-Out file is an output file generated by the Quartus II Fitter that contains pin assignment information. Use the Quartus II Pin Planner or Assignment Editor to set and change the assignments contained in the Pin-Out file. This file cannot be used to import pin assignment changes into the Quartus II software. Use it only to transfer assignments for use with the Cadence design tools.

The Pin-Out file lists all used and unused pins on your selected Altera device. It also provides the following basic information fields for each assigned pin on a device:

- Pin signal name and usage
- Pin number
- Signal direction
- I/O standard
- Voltage
- I/O bank
- User or Fitter-assigned

For information about using the Quartus II Pin Planner to create or change pin assignment details, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Generating Pin-Out Files

The Quartus II software automatically generates the Pin-Out file when your FPGA design is fully compiled or when you start I/O Assignment Analysis. To start I/O Assignment Analysis, on the Processing menu, point to Start and click **Start I/O Assignment Analysis**. The file is output by the Quartus II Fitter. The file is generated and placed in your Quartus II design directory with the name <*project name*>**.pin**. The Cadence design tools do not generate or change this file.

For more information about pin and signal assignment transfer and the files that the Quartus II software can import and export, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

FPGA-to-Board Integration with the Cadence Allegro Design Entry HDL Software

The Cadence Allegro Design Entry HDL software is Cadence's high-end schematic capture tool (part of the Cadence 600 series design flow). Use this software to create flat circuit schematics for all types of PCB design. The Cadence Allegro Design Entry HDL software can also create hierarchical schematics to facilitate design reuse and team-based design. With the Cadence Allegro Design Entry HDL software, the design flow from FPGA-to-board is one-way, using only the Pin-Out file generated by the Quartus II software. Signal and pin assignment changes can only be made in the Quartus II software and are reflected in updated symbols in a Design Entry HDL project.

Routing or pin assignment changes made in a board layout tool or a Design Entry HDL symbol cannot be back-annotated to the Quartus II software.

Figure 7–1 shows the design flow with the Cadence Allegro Design Entry HDL software.

For more information about the Cadence Allegro Design Entry HDL software and the Part Developer, including licensing, support, usage, training, and product updates, refer to the Help in the software or refer to the Cadence web page at www.cadence.com.

Symbol Creation

In addition to circuit simulation, circuit board schematic creation is one of the first tasks required in the design of a new PCB. Schematics are required to understand how the PCB works, and to generate a netlist that is passed on to a board layout tool for board design and routing. The Allegro PCB Librarian Part Developer provides the ability to create schematic symbols based on FPGA designs exported from the Quartus II software.

Create symbols for Design Entry HDL with the Allegro PCB Librarian Part Developer available in the Allegro Project Manager. The Part Developer is the recommended method for importing FPGA designs into the Cadence Allegro Design Entry HDL software.

You must have a PCB Librarian Expert license from Cadence to run the Part Developer. The Part Developer provides a graphical interface with many options for creating, editing, fracturing, and updating symbols. If you do not use the Part Developer, you must create and edit symbols manually in the Symbol Schematic View in the Cadence Allegro Design Entry HDL software.

If you do not have a PCB Librarian Expert license, you can still automatically create FPGA symbols using the programmable IC (PIC) design flow found in the Allegro Project Manager. For more information about using the PIC design flow, refer to the Help in the Cadence design tools, or go to the Cadence website at www.cadence.com.

Before you create a symbol from an FPGA design, you must open or create a Design Entry HDL design project. You can do this with the Allegro Project Manager, the main interface to all of the Cadence tools.

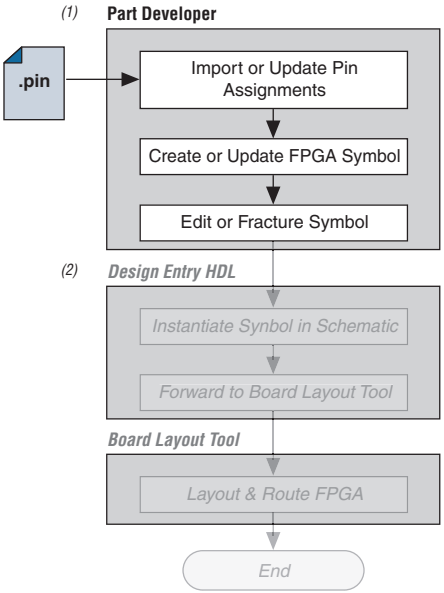
To open an existing design in the Allegro Project Manager, on the File menu, click **Open** and select the main design file for your project (found in your Allegro Design Entry HDL project directory and called <*project directory*>**.cpm**).

To create a new project, on the File menu, point to New and click **New Design**. The New Project Wizard appears. Use the wizard to name your new project, set the file location, and define associated part libraries.

Allegro PCB Librarian Part Developer

Create, fracture, and edit schematic symbols for your FPGA designs in Altera devices using the Part Developer. Most FPGA devices are physically large with hundreds of pins, requiring large schematic symbols that may not fit on a single schematic page. Symbols designed in the Part Developer can be split or fractured into a number of functional blocks called slots, allowing multiple smaller part fractures to exist on the same schematic page or across multiple pages. Figure 7–3 highlights how the Part Developer fits into the design flow.

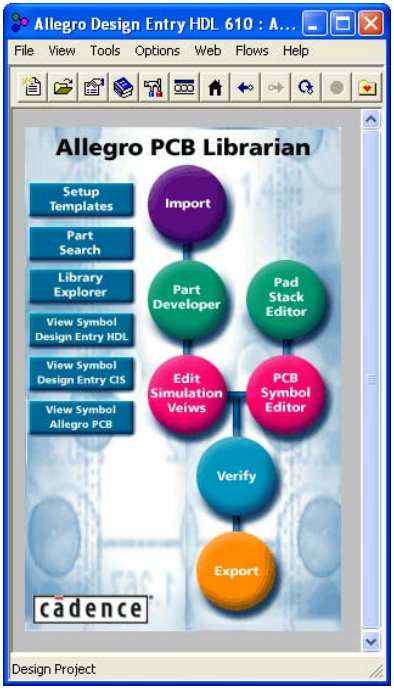
Figure 7–3. Part Developer in the Design Flow



Notes to Figure 7–3:
(1) Refer to Figure 7–1 for the full design flow flowchart details.
(2) Grayed out steps are not part of the FPGA Symbol creation or update process.

Run the Part Developer from the Project Manager (Figure 7–4). To start the Part Developer in the Project Manager, on the Flows menu, click **Library Management**. Click **Part Developer** to start the tool.

Figure 7–4. Invoking the Part Developer from the Project Manager

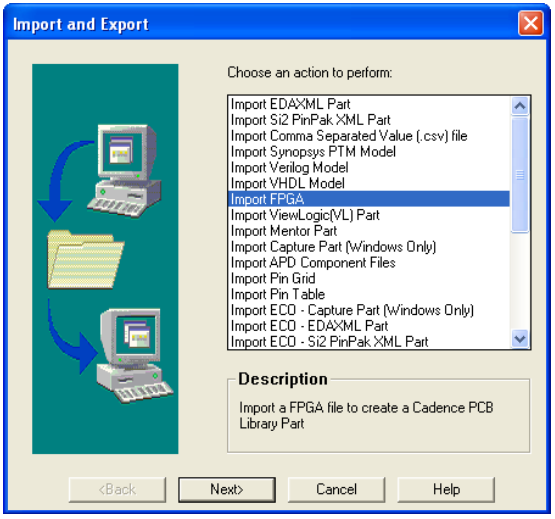


Import and Export Wizard

Once you are in the Part Developer, you can use the Import and Export Wizard to import your pin assignments from the Quartus II software. To access the Wizard, perform the following steps:

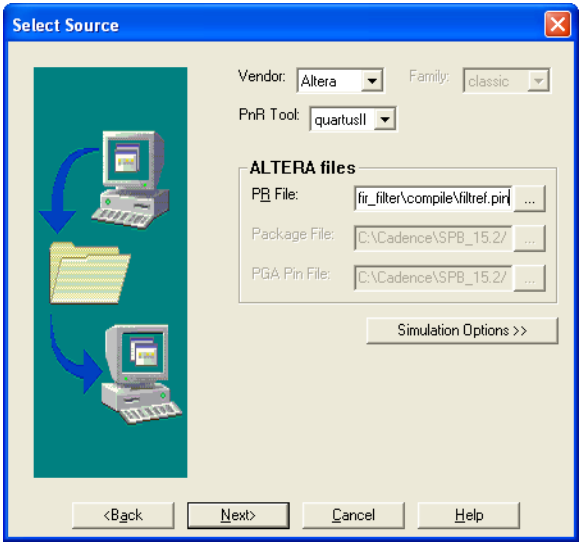
1. On the File menu, click **Import and Export**. The Import and Export Wizard appears (Figure 7–5).

Figure 7–5. Import and Export Wizard



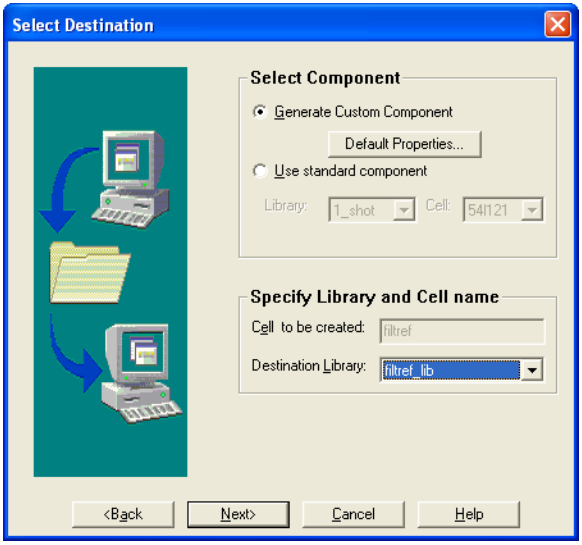
2. Select **Import FPGA**. Click **Next**. The **Select Source** page appears (Figure 7–6).

Figure 7–6. Select Source Page



3. In the **Vendor** list, select **Altera**. In the **PnR Tool** list, select **quartusII**. To specify the Pin-Out file in the **PR File** field, select the Pin-Out file in your Quartus II project directory. Click **Simulation Options** if you want to select simulation input files. Click **Next**. The **Select Destination** page is shown (Figure 7–7).

Figure 7–7. Select Destination Page

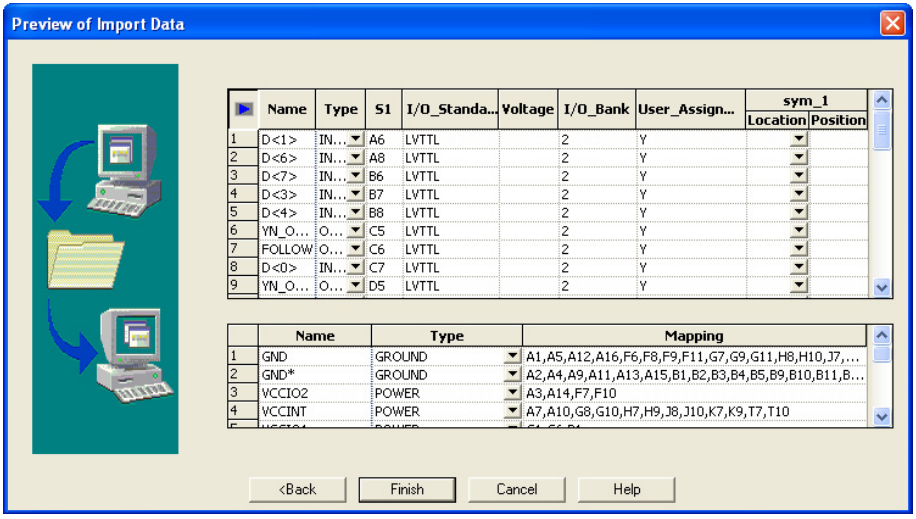


4. To create a new component in a library, click **Generate Custom Component**. To base your symbol on an existing component, click **Use standard component**.

You may want to do this if you previously created generic symbols for an FPGA device. You can place your pin and signal assignments from the Quartus II software on this symbol and reuse the symbol as a base any time you have a new FPGA design.

In the **Library** list, select an existing library. You can now select from the cells contained in the selected library. Each cell represents all of the symbol versions and part fractures for that particular part. In the **Cell** list, select the existing cell to use as a base for your part. In the **Destination Library** list, select a destination library for the component. Click **Next**. A preview of your import data is shown (Figure 7–8).

Figure 7–8. Preview of Import Data Window



5. Review the assignments you are importing into the Part Developer based on the data in the Pin-Out file. The location of each pin is not included in the information in this window, but inputs are placed on the left side of the created symbol, outputs on the right, power pins on the top, and ground pins on the bottom. Make any desired changes. When you have completed your changes, click **Finish** to create the symbol. The Part Developer main screen is shown.

If the Part Developer is not set up to point to your PCB Librarian Expert license file, an error message displays in red at the bottom of the message text window of the **Part Developer** when you select the Import and Export command. To point to your PCB Librarian Expert license, on the **File** menu, click **Change Product** and select the correct product license.

For more information about licensing and obtaining licensing support, contact Cadence or refer to their website at www.cadence.com.

Edit & Fracture Symbol

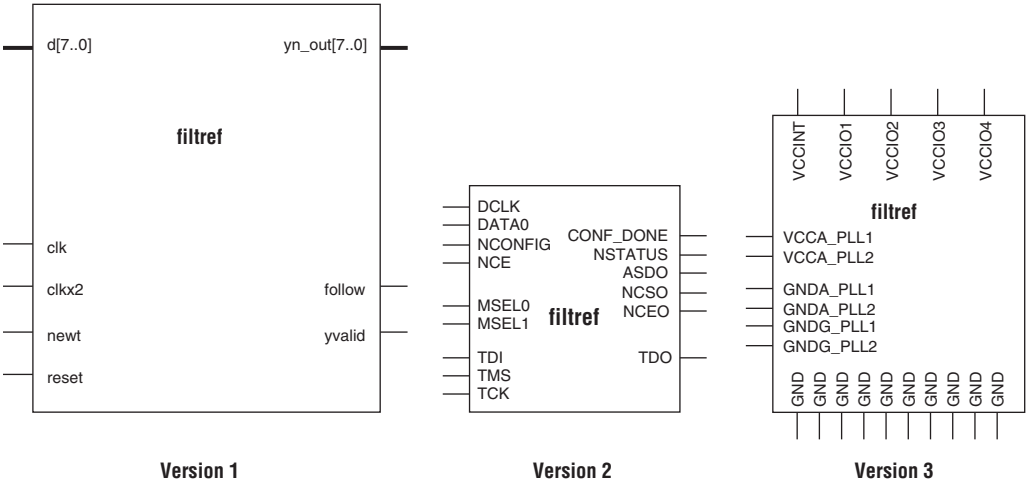
After you save your new symbol in the Part Developer software, you can edit the symbol graphics, fracture the symbol into multiple slots, and add or change package or symbol properties. These actions are available from the **Part Developer** main window.

The Part Developer Symbol Editor contains many graphical tools to edit the graphics of a particular symbol. Select the symbol in the cell hierarchy to edit the symbol graphics. The **Symbol Pins** tab is shown. Edit the preview graphic of the symbol in the **Symbol Pins** tab.

Fracturing a Part Developer package into separate symbol slots is especially useful for FPGA designs. A single symbol for most FPGA packages may be too large for a single schematic page. Splitting the part into separate slots allows you to organize parts of the symbol by function, creating cleaner circuit schematics. For example, you could create one slot for an I/O symbol, a second slot for a JTAG symbol, and a third slot for a power/ground symbol.

Figure 7–9 shows a part fractured into separate slots.

Figure 7–9. Splitting a Symbol into Multiple Slots *Notes (1), (2)*



Notes to Figure 7–9:

(1) Figure 7–9 represents a Cyclone device with JTAG or passive serial (PS) mode configuration option settings. Symbols created for other devices or other configuration modes may have different sets of configuration pins, but can be fractured in a similar manner.

(2) Symbol fractures are referred to in different ways in each of the tools described in this chapter. Refer to Table 7–2 for the specific tool naming conventions.

(3) The power/ground slot shows only a representation of power and ground pins. In actuality, the device contains a high number of power and ground pins.

While the Part Developer software refers to symbol fractures as slots, the other tools described in this chapter use different names to refer to symbol fractures. Table 7–2 lists the symbol fracture naming conventions for each of the tools addressed in this chapter.

Table 7–2. Symbol Fracture Naming

	Allegro PCB Librarian Part Developer Software	Allegro Design Entry HDL Software	Allegro Design Entry CIS Software
During symbol generation	Slots	N/A	Sections
During symbol schematic instantiation	N/A	Versions	Parts

To fracture a part into separate slots, or modify the slot locations of pins on parts that are already fractured in the Part Developer, perform the following steps:

1. Start the Cadence Allegro Design Project Manager.
2. On the Flows menu, click **Library Management**. The Library Management design flow is shown. Click **Part Developer**. The Part Developer launches.
3. Click on the name of the package you want to change in the cell hierarchy. The **Package Pin** tab appears.
4. Click **Functions/Slots**. If you are not creating new slots but want to change the slot location of some pins, proceed to step 5. If you are creating new slots, click **Add**. A dialog box appears, allowing you to add extra symbol slots. Set the number of extra slots you want to add to the existing symbol, not the total number of desired slots for the part. Click **OK**.
5. Click **Distribute Pins**. Set the slot where each pin should reside. Use the checkboxes in each column to move pins from one slot to another. You can use the standard cut, copy, and paste keyboard commands on selected groups of checkboxes to move multiple pins from one slot to another. Click **OK**.
6. After distributing the pins, click the **Package Pin** tab and click **Generate Symbol(s)**. the **Generate Symbols** dialog box appears.
7. Select whether to create a new symbol or modify an existing symbol in each slot. Click **OK**.

The newly generated or modified slot symbols display as separate symbols in the cell hierarchy. Each of these symbols can be edited individually.

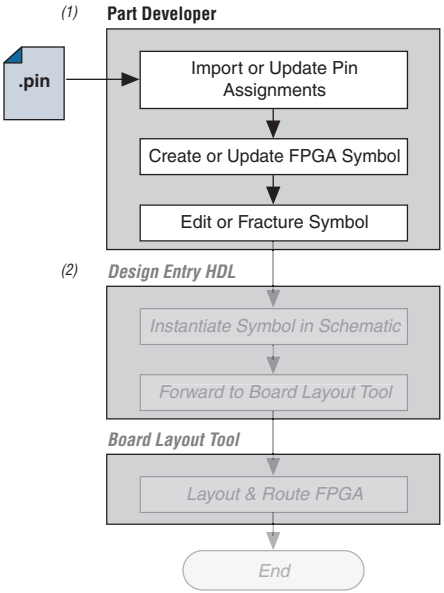
The Part Developer lets you remap pin assignments in the Package Pin tab of the main **Part Developer** window. If signals are remapped to different pins in the Part Developer, the changes are reflected only in regenerated symbols for use in your schematics. You cannot transfer pin assignment changes to the Quartus II software from the Part Developer, which creates a potential mismatch of the schematic symbols and assignments in the FPGA design. If pin assignment changes are necessary, make the changes in the Quartus II Pin Planner instead of the Part Developer, and update the symbol as described in the following sections.

For more information about creating, editing, and organizing component symbols with the Allegro PCB Librarian Part Developer, refer to the Part Developer Help.

Update FPGA Symbol

As the design process continues, you may need to make changes to the logic design in the Quartus II software, placing signals on different pins after the design is recompiled, or use the Quartus II Pin Planner to make changes manually. The board designer may request such changes to improve the board routing and layout. These types of changes must be carried forward to the circuit schematic and board layout tools to ensure signals are connected to the correct pins on the FPGA. Updating the Pin-Out file in the Quartus II software facilitates this flow. Figure 7–10 shows this part of the design flow.

Figure 7–10. Updating the FPGA Symbol in the Design Flow



Notes to Figure 7–10:
(1) Refer to Figure 7–1 for the full design flow flowchart details.
(2) Grayed out steps are not part of the FPGA Symbol update process.

Once the Pin-Out file has been updated, perform the following steps to update the symbol using the Allegro PCB Librarian Part Developer:

1. On the File menu, click **Import and Export**. The Import and Export Wizard appears.

2. In the list of actions to perform, select **Import ECO - FPGA.** Click **Next**. The **Select Source Page** is shown.

3. Select the updated source of the FPGA assignment information. In the **Vendor** list, select **Altera**. In the **PnR Tool** list, select **quartusII**. In the **PR File** field, click browse to specify the updated Pin-Out file in your Quartus II project directory. Click **Next**. The **Select Destination** window is shown.

4. Select the source component and a destination cell for the updated symbol. To create a new component based on the updated pin assignment data, select **Generate Custom Component**. This replaces the cell listed under the Specify Library and Cell name header with a new, non-fractured cell. Any symbol edits or fractures

are lost. You can preserve these edits by selecting **Use standard component and select the existing library and cell**. Select the destination library for the component and click **Next**. The Preview of Import Data page is shown.

5. Make any additional changes to your symbol. Click **Next**. A list of ECO messages displays summarizing what changes will be made to the cell. To accept the changes and update the cell, click **Finish**.

6. The main **Part Developer** window is shown. You can edit, fracture, and generate the updated symbols as usual from this window.

If the Part Developer is not set up to point to your PCB Librarian Expert license file, an error message displays in red at the bottom of the message text window of the **Part Developer** when you select the **Import and Export** command. To point to your PCB Librarian Expert license, on the File menu, click **Change Product**, and select the correct product license. For more information about licensing and obtaining licensing support, contact Cadence or refer to their website at www.cadence.com.

Instantiating the Symbol in the Cadence Allegro Design Entry HDL Software

Once the new symbol is saved in the Part Developer, instantiate the symbol in your Design Entry HDL schematic.

1. In the Allegro Project Manager, switch to the board design flow.

2. On the Flows menu, click **Board Design**.

3. Click **Design Entry** to start the Design Entry HDL software.

4. To add the newly created symbol to your schematic, right-click in the main schematic window and choose **Add Component**, or on the Component menu, click **Add**. The **Add Component** dialog box appears.

5. Select the new symbol library location, and select the name of the cell you created from the list of cells.

The symbol is now "attached" to your cursor for placement in the schematic. If you fractured the symbol into slots, right-click the symbol and choose **Version** to select one of the slots for placement in the schematic.

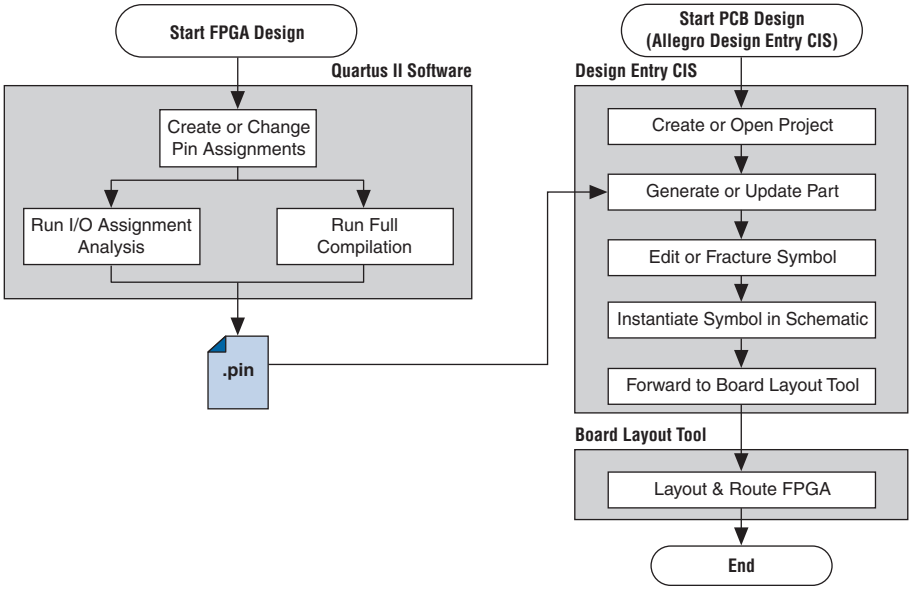
For more information about the Cadence Allegro Design Entry HDL software, including licensing, support, usage, training, and product updates, refer to the Help in the software or go to the Cadence website at www.cadence.com.

FPGA-to-Board Integration with Allegro Design Entry CIS

The Cadence Allegro Design Entry CIS software is Cadence's mid-level schematic capture tool (part of the Cadence 200 series design flow based on OrCAD Capture CIS). Use this software to create flat circuit schematics for all types of PCB design. You can also create hierarchical schematics to facilitate design reuse and team-based design using this software. With the Cadence Allegro Design Entry CIS software, the design flow from FPGA-to-board is unidirectional using only the Pin-Out file generated by the Quartus II software. Signal and pin assignment changes can only be made in the Quartus II software and are reflected in updated symbols in a Design Entry CIS schematic project.

Routing or pin assignment changes made in a board layout tool or a Design Entry CIS symbol cannot be back-annotated to the Quartus II software. Figure 7–11 shows the design flow with the Cadence Allegro Design Entry CIS software.

Figure 7–11. Design Flow with the Cadence Allegro Design Entry CIS Software



For more information about the Cadence Allegro Design Entry CIS software, including licensing, support, usage, training, and product updates, refer to the Help in the software, go to the Cadence website at www.cadence.com, or go to the EMA Design Automation website at www.ema-eda.com.

Allegro Design Entry CIS Project Creation

The Cadence Allegro Design Entry CIS software has built-in support for creating schematic symbols using pin assignment information imported from the Quartus II software.

If you have not already created a new project in the Cadence Allegro Design Entry CIS software, perform the following steps to create a new project:

1. On the File menu, point to **New** and click **Project**. The New Project Wizard starts.

   When you create a new project, you can select the PC Board Wizard, the Programmable Logic Wizard, or a blank schematic.

2. Select the **PC Board Wizard** to create a project where you can select which part libraries to use, or select a blank schematic.

   The Programmable Logic Wizard is used only to build an FPGA logic design in the Cadence Allegro Design Entry CIS software, which is unnecessary when using the Quartus II software.

   No other special configuration for your project is required. Your new project is created in the specified location and initially consists of two files: the OrCAD Capture Project (**.opj**) file and the Schematic Design (**.dsn**) file.

Generate Part

After you create a new project or open an existing project in the Allegro Design Entry CIS software, you can generate a new schematic symbol based on your Quartus II FPGA design. You can also update an existing symbol if your Pin-Out file has been updated in the Quartus II software. The Cadence Allegro Design Entry CIS software stores component symbols in OrCAD Library (**.olb**) files. When a symbol is placed in a library attached to a project, it is immediately available for instantiation in the project schematic.

You can add symbols to an existing library or you can create a new library specifically for the symbols generated from your FPGA designs. To create a new library, perform the following steps:

1. On the File menu, point to New and click **Library** in the Cadence Allegro Design Entry CIS software to create a default library named library1.olb. This library appears in the Library folder in the **Project Manager** window of the Cadence Allegro Design Entry CIS software.

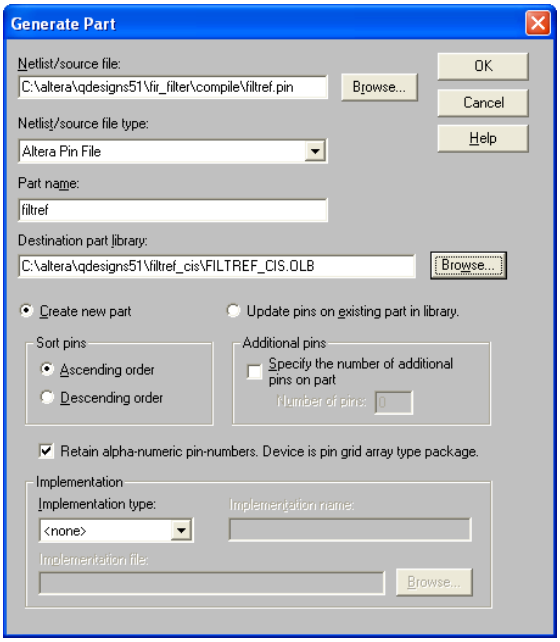
2. Right-click the new library and choose **Save As** to specify a desired name and location for the library. The library file is not created until you save the new library.

You can now create a new symbol to represent your FPGA design in your schematic. To generate a schematic symbol, perform the following steps:

1. Start the Cadence Allegro Design Entry CIS software.

2. On the Tools menu, click **Generate Part**. The **Generate Part** dialog box appears (Figure 7–12).

Figure 7–12. Generate Part Dialog Box



3. In the **Netlist/source file type** field, click **Browse** to specify the Pin-Out file from your Quartus II design.

4. In the **Netlist/source file type** list, select **Altera Pin File**.

5. Enter the new part name.

6. Specify the Destination part library for the symbol. If you do not select an existing library for the part, a new library is created with a default name that matches the name of your Design Entry CIS project.

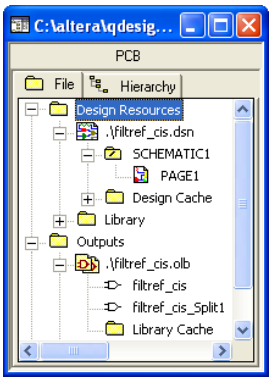
7. Select **Create new part** if you are creating a brand new symbol for this design. Select **Update pins on existing part in library** if you updated your Pin-Out file in the Quartus II software and want to transfer any assignment changes to an existing symbol.

8. Select any other desired options and set Implementation type to **<none>**. The symbol is for a primitive library part based only on the Pin-Out file and does not need a special implementation. Click **OK**.

9. Review the Undo warning and click **Yes** to complete the symbol generation.

The symbol is generated and placed in the selected library or in a new library found in the Outputs folder of the design in the **Project Manager** window. Double-click the name of the new symbol to see its graphical representation and edit it manually using the tools available in the Cadence Allegro Design Entry CIS software.

Figure 7–13. Project Manager Window



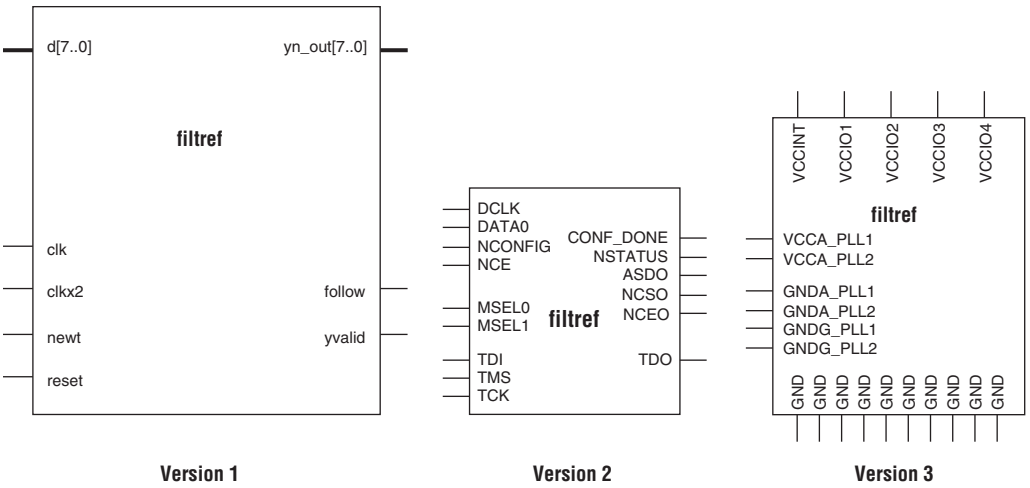
For more information about creating and editing symbols in the Allegro Design Entry CIS software, refer to the Help in the software.

Split Part

Once a new symbol is saved in a project's library, you can fracture the symbol into multiple parts called sections. Fracturing a part into separate sections is especially useful for FPGA designs. A single symbol for most FPGA packages may be too large for a single schematic page. Splitting the part into separate sections allows you to organize parts of the symbol by function, creating cleaner circuit schematics. For example, you could create one slot for an I/O symbol, a second slot for a JTAG symbol, and a third slot for a power/ground symbol.

Figure 7–14 shows a part fractured into separate sections.

Figure 7–14. Splitting a Symbol into Multiple Sections *Notes (1), (2)*



Notes to Figure 7–14:

(1) Figure 7–14 represents a Cyclone device with JTAG or passive serial (PS) mode configuration option settings. Symbols created for other devices or other configuration modes may have different sets of configuration pins, but can be fractured in a similar manner.

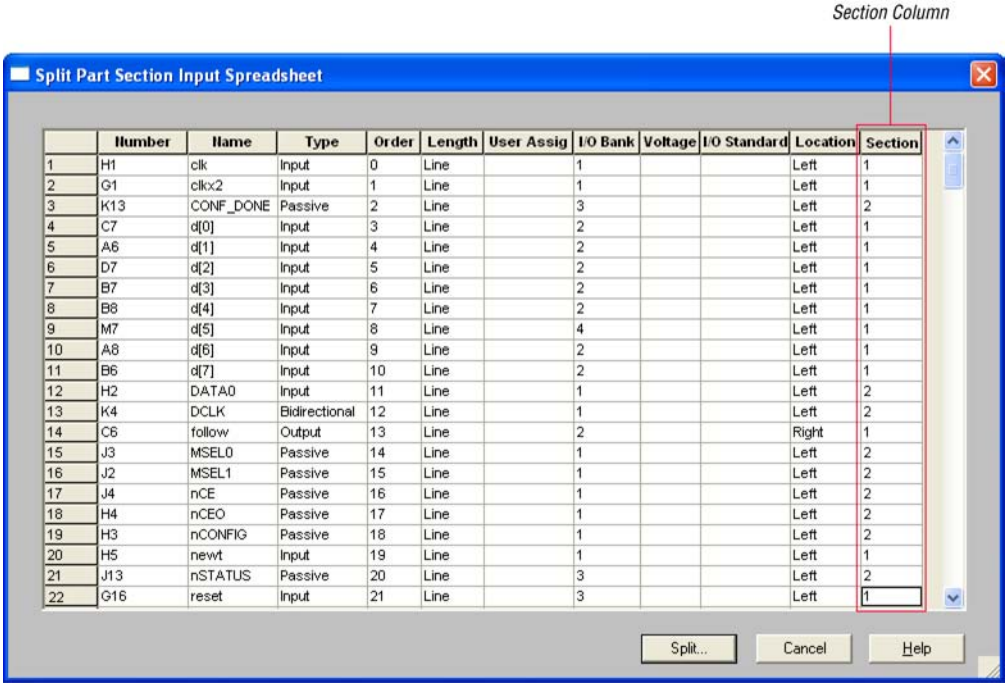
(2) Symbol fractures are referred to in different ways in each of the tools described in this chapter. Refer to Table 7–2 for the specific tool naming conventions.

(3) The power/ground section shows only a representation of power and ground pins. In actuality, the device contains a high number of power and ground pins.

While symbol generation in the Design Entry CIS software refers to symbol fractures as sections, the other tools described in this chapter use different names to refer to symbol fractures. Refer to Table 7–2 on page 7–14 for the symbol fracture naming conventions for each of the tools addressed in this chapter.

To split a part into sections, select the part in its library in the **Project Manager** window of Design Entry CIS. On the Tools menu, click **Split Part** or right-click the part and choose **Split Part**. The **Split Part Section Input Spreadsheet** is shown (Figure 7–15).

Figure 7–15. Split Part Section Input Spreadsheet



	Number	Name	Type	Order	Length	User Assig	I/O Bank	Voltage	I/O Standard	Location	Section
1	H1	clk	Input	0	Line		1			Left	1
2	G1	clkx2	Input	1	Line		1			Left	1
3	K13	CONF_DONE	Passive	2	Line		3			Left	2
4	C7	d[0]	Input	3	Line		2			Left	1
5	A6	d[1]	Input	4	Line		2			Left	1
6	D7	d[2]	Input	5	Line		2			Left	1
7	B7	d[3]	Input	6	Line		2			Left	1
8	B8	d[4]	Input	7	Line		2			Left	1
9	M7	d[5]	Input	8	Line		4			Left	1
10	A8	d[6]	Input	9	Line		2			Left	1
11	B6	d[7]	Input	10	Line		2			Left	1
12	H2	DATA0	Input	11	Line		1			Left	2
13	K4	DCLK	Bidirectional	12	Line		1			Left	2
14	C6	follow	Output	13	Line		2			Right	1
15	J3	MSEL0	Passive	14	Line		1			Left	2
16	J2	MSEL1	Passive	15	Line		1			Left	2
17	J4	nCE	Passive	16	Line		1			Left	2
18	H4	nCEO	Passive	17	Line		1			Left	2
19	H3	nCONFIG	Passive	18	Line		1			Left	2
20	H5	newt	Input	19	Line		1			Left	1
21	J13	nSTATUS	Passive	20	Line		3			Left	2
22	G16	reset	Input	21	Line		3			Left	1

Each row in the spreadsheet represents a pin in the symbol. The spreadsheet column labeled Section indicates the section of the symbol to which each pin is assigned. By default, all pins in a new symbol are located in section 1. Change the values in this column to assign pins to different, new sections of the symbol. You can also specify the side of a section on which the pin will reside by changing the values in the Location column. When you are finished, click **Split**. A new symbol appears in the same library as the original with the name *<original part name>*_**Split1.**

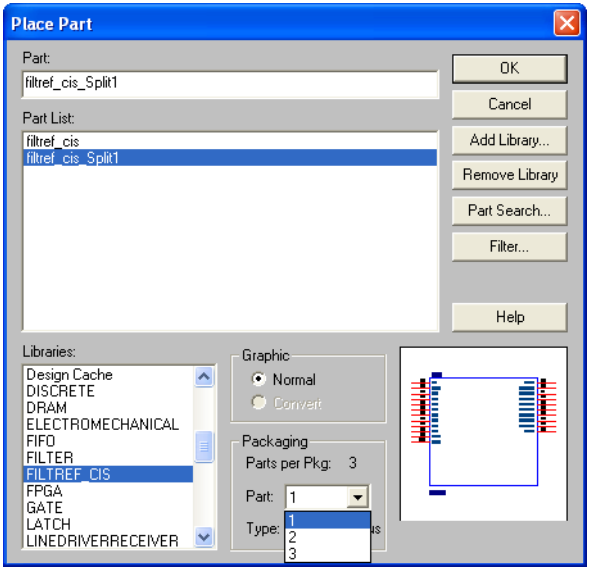
View and edit each section individually. To view the new sections of the part, double-click the part. The **Part Symbol Editor** window is shown. The first section of the part is displayed for editing. On the View menu, click **Package** to view thumbnails of all the part sections. Double-click a thumbnail to edit that section of the symbol.

For more information about splitting parts into sections and editing symbol sections in the Cadence Allegro Design Entry CIS software, refer to the Help in the software.

Instantiate Symbol in Design Entry CIS Schematic

After a new symbol is saved in a library in your Design Entry CIS project, you can instantiate it on a page in your schematic. Open a schematic page in the **Project Manager** window of the Cadence Allegro Design Entry CIS software. On the schematic page, to add the newly created symbol to your schematic, on the Place menu, click **Part**. The **Place Part** dialog box appears (Figure 7–16).

Figure 7–16. Place Part Dialog Box



Select the new symbol library location and the newly created part name. If you select a part that is split into sections, you can select the section to place from the Part pop-up menu. Click **OK**. The symbol is now attached to your cursor for placement in the schematic. Click on the schematic page to place the symbol.

For more information about using the Cadence Allegro Design Entry CIS software, refer to the Help in the software.

Altera Libraries for Design Entry CIS

Altera provides downloadable OrCAD Library Files for many of its device packages. You can add these libraries to your Design Entry CIS project and update the symbols with the pin assignments contained in the Pin-Out file generated by the Quartus II software. This allows you to use the downloaded library symbols as a base for creating custom schematic symbols with your pin assignments that you can edit or fracture as desired. This can increase productivity by reducing the amount of time it takes to create and edit a new symbol.

To use the Altera-provided libraries with your Design Entry CIS project, perform the following steps:

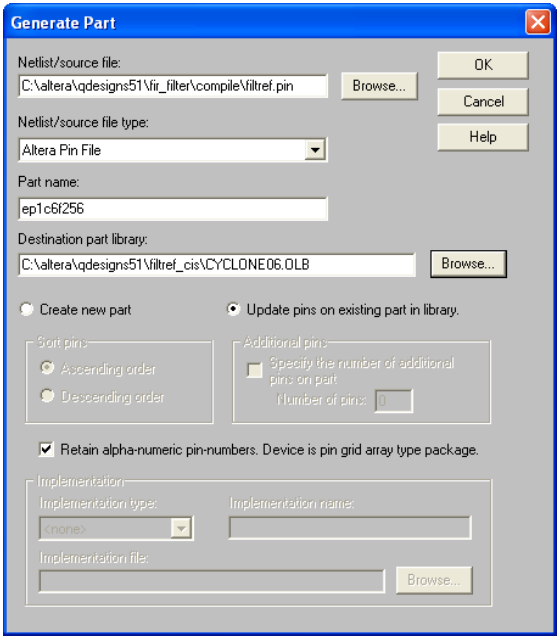
1. Download the library of your target device from the Download Center page found through the Support page on the Altera website at www.altera.com.

2. Make a copy of the appropriate OrCAD Library file so that the original symbols are not altered. Place the copy in a convenient location such as your Design Entry CIS project directory.

3. In the **Project Manager** window of the Cadence Allegro Design Entry CIS software, click once on the Library folder to select it. On the Edit menu, click **Project** or right-click the Library folder and choose **Add File** to select the copy of the downloaded OrCAD Library file and add it to your project. The new library is added to the list of part libraries for your project.

4. On the Tools menu, click **Generate Part.** The **Generate Part** dialog box appears (Figure 7–17).

Figure 7–17. Generate Part Dialog Box



5. In the **Netlist/source file type** field, click **Browse** to specify the Pin-Out file in your Quartus II design.

6. From the **Netlist/source file type** list, select **Altera Pin File**.

7. For the part name, enter the name of the target device the same as it appears in the downloaded library file. For example, if you are using a device from the CYCLONE06.OLB library, set the part name to match one of the devices in this library such as ep1c6f256. You can rename the symbol later in the **Project Manager** window after the part is updated.

8. Set the Destination part library to the copy of the downloaded library you added to the project.

9. Select **Update pins on existing part in library**. Click **OK,** then click **Yes**.

The symbol is updated with your pin assignments. Double-click the symbol in the **Project Manager** window to view and edit the symbol. On the View menu, click **Package** if you want to view and edit other sections

of the symbol. If the symbol in the downloaded library is already fractured into sections, as some of the larger packages are, you can edit each section but you cannot further fracture the part. Generate a new part without using the downloaded part library if you require additional sections.

For more information about creating, editing, and fracturing symbols in the Cadence Allegro Design Entry CIS software, refer to the Help in the software.

Conclusion

Transferring a complex, high-pin-count FPGA design to a PCB for prototyping or manufacturing is a daunting process that can lead to errors in the PCB netlist or design, especially when different engineers are working on different parts of the project. The design workflow available when the Quartus II software is used with tools from Cadence assists the FPGA designer and the board designer in preventing such errors and focusing all attention on the design.

Section III. Area, Timing & Power Optimization

Techniques for achieving the highest design performance are important when designing for programmable logic devices (PLDs), especially higher density FPGAs. The Altera® Quartus® II software offers many advanced design analysis tools that allow for detailed timing analysis of your design, including a fully integrated Timing Closure Floorplan Editor. With these tools and options, critical paths can be easily determined and located in the targeted device floorplan. This section explains how to use these tools and options to enhance your FPGA design analysis flow.

This section includes the following chapters:

Revision History

The table below shows the revision history for Chapters 8 through 14.

Chapter(s)	Date / Version	Changes Made
8	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Added Optimization advisors. • Added initial compilation information. • Added design analysis information. • Added f_{MAX} timing optimization techniques.
	December 2005 v5.1.1	Minor typographic corrections.
	October 2005 v5.1.0	Chapter 8 was formerly Chapter 7 in version 5.0.
	May 2005 v5.0.0	Chapter 7 was formerly Chapter 6 in version 4.2.
	Dec. 2004 v2.1	Updated for Quartus II software version 4.2: • Re-organized chapter. • Added Early Timing Estimation segment. • Removed Incremental Fitting segment. • Updated Optimization Advisors. • Updated Resource Utilization Optimization Techniques (LUT-Based Devices) segment. • Added the DSP Block Balancing logic option to Retarget or Balance DSP Blocks segment. • Updated Duplicate Logic for Fan-Out Control segment. • Updates to tables, figures.
	June 2004 v2.0	• Updates to tables, figures. • New functionality in the Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
9	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Updated device support. • Added multi-VCD/SAF support information. • Updated achieved power reductions values.
	October 2005 v5.1.0	Chapter 9 was formerly Chapter 7 in Volume 1: Stratix II Low Power Design Techniques.
10	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Updated device support.
	October 2005 v5.1.0	Chapter 10 was formerly Chapter 8 in version 5.0.
	May 2005 v5.0.0	Chapter 8 was formerly Chapter 7 in version 4.2.
	Dec. 2004 v2.1	Updated for Quartus II software version 4.2: • Removed By Delay and Show Routing Delays options from the Viewing Critical Paths segment. • Updates to figures.
	June 2004 v2.0	• Updates to tables, figures. • New functionality in the Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.

Chapter(s)	Date / Version	Changes Made
11	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Chapter 11 was formerly Chapter 9 in version 5.0.
	May 2005 v5.0.0	Chapter 9 was formerly Chapter 8 in version 4.2.
	Dec. 2004 v2.1	Updated for Quartus II software version 4.2: • General formatting and editing updates. • Additional description about fixed and primitive node names for synthesis netlist optimization and physical synthesis options. • Updates to figures. • Clarified APEX support. • Added information about node name changes for atoms during physical synthesis. • Deleted Physical Synthesis Report section.
	June 2004 v2.0	• Updates to tables and figures. • New functionality in the Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
12	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Updated with the new TimeQuest Timing Analyzer feature.
	October 2005 v5.1.0	Chapter 12 was formerly Chapter 10 in version 5.0.
	May 2005 v5.0.0	Chapter 10 was formerly Chapter 9 in version 4.2.
	Dec. 2004 v2.1	• Updates to tables and figures. • New functionality in the Quartus II software version 4.2.
	June 2004 v2.0	• Updates to tables and figures. • New functionality in the Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
13	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Chapter 13 was formerly Chapter 11 in version 5.0.
	May 2005 v5.0.0	Chapter 11 was formerly Chapter 10 in version 4.2.
	Dec. 2004 v2.2	• Updates to tables and figures. • New functionality in the Quartus II software version 4.2.
	August 2004 v2.1	• New functionality in the Quartus II software version 4.1 Sp1.
	June 2004 v2.0	• Updates to tables and figures. • New functionality in the Quartus II software version 4.1.
	Feb. 2004 v1.0	Initial release.
14	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Chapter 14 was formerly Chapter 12 in version 5.0.
	May 2005 v5.0.0	Chapter 12 was formerly Chapter 11 in version 4.2.
	Dec. 2004 v1.1	• Chapter 11 was formerly Chapter 12. • Updates to tables and figures. • New functionality in the Quartus II software version 4.2
	Feb. 2004 v1.0	Initial release.

8. Area & Timing Optimization

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Introduction

Techniques for achieving the highest quality of results are important when designing for programmable logic devices (PLDs). The tools that facilitate these techniques must provide the highest level of flexibility without compromising ease-of-use. The optimization features available in the Quartus® II software allow you to meet design requirements by facilitating optimization at multiple points in the design process.

This chapter explains techniques to reduce resource usage, improve timing performance, and reduce compilation times when designing for Altera® devices. It also explains how and when to use some of the features described in other chapters of the *Quartus II Handbook*.

For more information about power optimization, refer to the *Power Optimization* chapter in volume 2 of the *Quartus II Handbook*.

The effects of these techniques vary from design to design. Applying each technique does not always improve design results. Settings and options in the Quartus II software have default values that generally provide the best trade-off between compilation time, resource utilization, and timing performance. You can adjust these settings to determine whether other settings provide better results for your design. When using advanced optimization settings and tools, it is important to benchmark their effect on your quality of results and to use them only if they improve results for your design.

Use the optimization flow described in this chapter to explore various compiler settings and determine the techniques that provide the best results.

Optimization Process Stages

The first stage in the optimization process is to perform an initial compilation to view the quality of results for your design. "Initial Compilation" on page 8–5 provides guidelines on some of the settings and assignments that are recommended for your initial compilation. "Design Analysis" on page 8–12 explains how to analyze the compilation results.

After you have analyzed the compilation results, perform the optimization stages in the recommended order, as described in this chapter.

For LUT-based devices (FPGAs and MAX® II CPLDs), perform optimizations in the following order:

1. If your design does not fit, refer to "Resource Utilization Optimization Techniques (LUT-Based Devices)" on page 8–20 before trying to optimize I/O timing or f_{MAX} timing.
2. If the I/O timing performance requirements are not met, refer to "I/O Timing Optimization Techniques (LUT-Based Devices)" on page 8–33 before trying to optimize f_{MAX} timing.
3. If f_{MAX} performance requirements are not met, refer to "f_{MAX} Timing Optimization Techniques (LUT-Based Devices)" on page 8–40 on page 7–32.

For macrocell-based devices (MAX 7000 and MAX 3000 CPLDs), perform optimizations in the following order:

1. If your design does not fit, refer to "Resource Utilization Optimization Techniques (Macrocell-Based CPLDs)" on page 8–57 before trying to optimize I/O timing or f_{MAX} timing.
2. If the timing performance requirements are not met, refer to "Timing Optimization Techniques (Macrocell-Based CPLDs)" on page 8–65.

For techniques to reduce compilation time, which are device-independent, refer to "Compilation-Time Optimization Techniques" on page 8–72.

You can use all these techniques in the GUI or with Tcl commands. For more information about scripting techniques, refer to "Scripting Support" on page 8–77.

Design Space Explorer

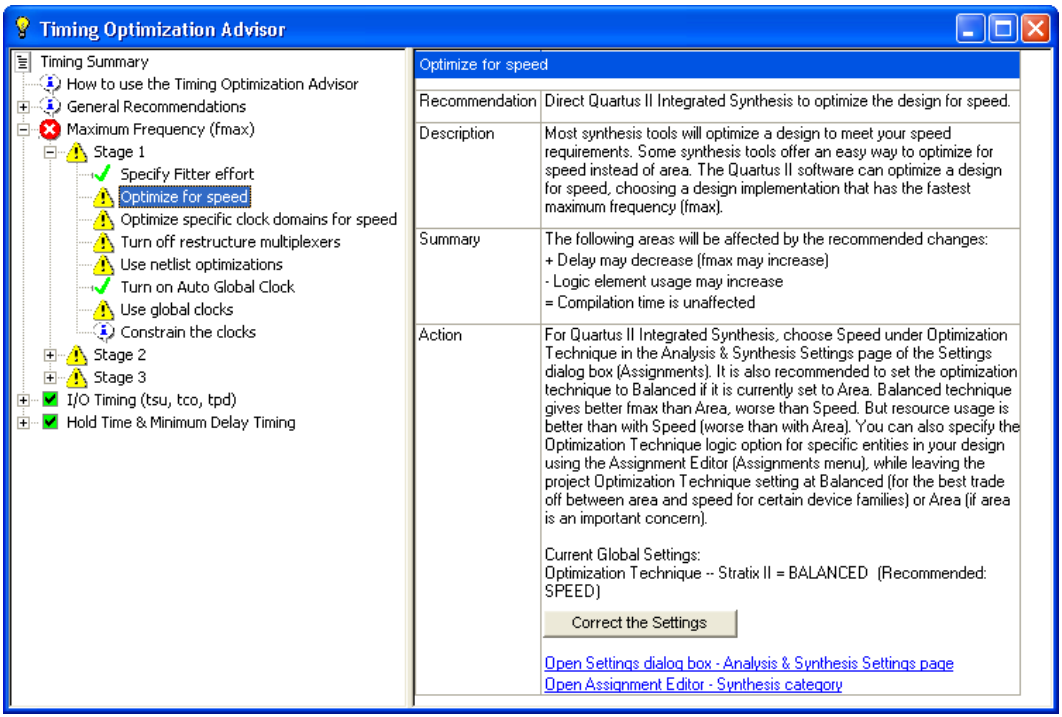
The Design Space Explorer (DSE) automates the process of running multiple compilations with different settings. You can use DSE to try the techniques described in this chapter. The DSE utility automates the process of finding the best set of options for your design. DSE explores the design space by applying various optimization techniques and analyzing the results.

For more information, refer to the *Design Space Explorer* chapter in volume 2 of the *Quartus II Handbook*.

Optimization Advisors

The optimization advisors provide guidance in making settings that optimize your design. On the Tools menu, click **Advisors**, and click **Resource Optimization Advisor** or **Timing Optimization Advisor**. The advisors describe many of the suggestions listed in this chapter. The Power Optimization Advisor is also available, to provide guidance for reducing power consumption. If you open the advisors after compilation, the Resource and Timing Optimization Advisors display icons indicating which resources or timing constraints were not met. The example in Figure 8–1 shows the Timing Optimization Advisor after compiling a design that fails to meet its frequency requirements. An error icon is shown next to the **Maximum Frequency (f_{MAX})** entry in the advisor.

Figure 8–1. Timing Optimization Advisor



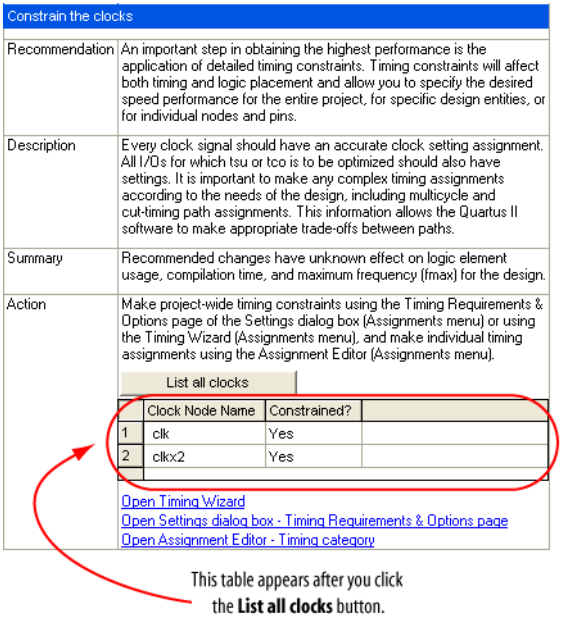
When you expand one of the categories in the Advisor, such as **Logic Element Usage** or **Maximum Frequency (f_{MAX})**, the recommendations are divided into stages. The stages show the order in which you should

apply the recommended settings. The first stage contains the options that are easiest to change, make the least drastic changes to your design optimization, and have the least effect on compilation time. Icons indicate whether each recommended setting has been made in the current project. In Figure 8–1, the check mark icons in the list of recommendations for **Stage 1** indicates recommendations that are already implemented. The warning icons indicate recommendations that are not followed for this compilation. The information icon indicates general suggestions. For these entries, the advisor does not report whether these recommendations were followed, but instead explains how you can achieve better performance. Refer to the "How to use" page in the Advisor for a legend that provides more information for each icon.

There is a link from each recommendation to the appropriate location in the Quartus II user interface where you can change the settings. For example, the **Synthesis Netlist Optimizations** page of the **Settings** dialog box or the **Global Signals** category in the Assignment Editor. This approach provides the most control over which settings are made, and helps you learn about the settings in the software. In some cases, you can also use the **Correct the Settings** button, shown in the advisor in Figure 8–1, to automatically make the suggested change to global settings.

For some entries in the advisor, a button appears that allows you to further analyze your design and gives you more information. For example, Figure 8–2 shows the guidelines for the **Constrain the clocks** entry, after the user has clicked **List all clocks**. The advisor provides a table with the clocks in the design, and indicates whether they have been assigned a timing constraint.

Figure 8–2. Timing Optimization Advisor



Initial Compilation

This section describes the basic assignments and settings to make for your initial compilation. Ensure that you check all the following suggested compilation assignments before compiling the design in the Quartus II software. Significantly different compilation results can occur depending on assignments made.

This chapter refers to timing settings and analysis in the Quartus II Classic Timing Analyzer. For equivalent settings and analysis in the TimeQuest Timing Analyzer, refer to the *TimeQuest Timing Analyzer* and the *Switching to the TimeQuest Timing Analyzer* chapters in volume 3 of the *Quartus II Handbook*.

Device Setting

Assigning a specific device determines the timing model that the Quartus II software uses during compilation. Choose the correct speed grade to obtain accurate results and the best optimization. The device size and the package determine the device pin-out and how many resources are available in the device.

To choose the target device, on the Assignments menu, click **Device**.

Smart Compilation Setting

Smart compilation can reduce compilation time by skipping compiler stages that are not needed to recompile the design. This is especially useful when you perform multiple compilation iterations during the optimization phase of the design process. However, smart compilation uses more disk space. To turn on smart compilation, on the Assignments menu, click **Settings**. In the Category list, select **Compilation Process Settings** and turn on **Use Smart compilation**.

This feature skips entire compiler stages (such as Analysis & Synthesis) when they are not needed. This feature is different from incremental compilation, which you can use to compile parts of your design while preserving results for unchanged parts. For information about using the incremental compilation feature to reduce your compilation time, refer to "Incremental Compilation" on page 8–72.

Timing Requirement Settings

An important step in the optimal quality of results, especially for high-performance FPGA designs, is to make comprehensive timing requirement settings. It is important to apply these settings for the following reasons:

- The Quartus II PowerFit™ Fitter attempts to meet or exceed specified timing requirements depending on the selected options as described in "Fitter Effort Setting" on page 8–9.
- The Quartus II software performs physical synthesis optimizations based on timing requirements (refer to "Synthesis Netlist Optimizations & Physical Synthesis Optimizations" on page 8–41 for more information).
- Correct timing assignment allow the software to work hardest to optimize the performance of the timing-critical parts of the design, and make trade-offs for performance or save area utilization in non-critical parts of the design.

  Do not over-constrain the software by applying timing requirements that are higher than your design requirements; use your real design requirements to get the best results.

- The Timing Analyzer (Classic or TimeQuest) checks your design against the timing assignments. The Compilation Report (or timing analysis reporting commands) shows whether timing requirements are met, and provide detailed timing information about paths that violate timing requirements.

To make clock assignments, on the Assignments menu, click **Settings**. In the Category list, select **Timing Analysis Settings**. Use the **Delay requirements**, **Minimum delay requirements**, and **Clock Settings** boxes to make global settings, or to apply settings to individual clocks, click **Individual Clocks** (recommended for multiple-clock designs). Create the clock setting, and apply it to the appropriate clock node in the design. The Timing Wizard can also step you through the process of making individual clock constraints. To run the Timing Wizard, on the Assignments menu, click **Timing Wizard**.

Ensure that every clock signal has an accurate clock setting assignment. If clocks come from a common oscillator, they may be considered related. Ensure that all related or derived clocks are set up correctly in the assignments. All I/O pins that require I/O timing optimization must have settings. You should also specify minimum timing constraints as applicable. If there is more than one clock or there are different I/O requirements for different pins, make multiple clock settings and individual I/O assignments instead of using the global settings.

Make any complex timing assignments required in the design, including any cut-timing and multicycle path assignments. Common situations for these types of assignments include reset or static control signals, cases where it is not important how long it takes a signal to reach a destination, and paths that can operate in more than one clock cycle. These assignments allow the Quartus II software to make appropriate trade-offs between timing paths, and can enable the Compiler to improve timing performance in other parts of the design. Specify these settings in the Assignment Editor.

For more information about timing assignments and timing analysis, refer to the *Classic Timing Analyzer* and the *TimeQuest Timing Analyzer* chapters in volume 3 of the *Quartus II Handbook*.

Timing Constraint Check

To ensure that all constraints or assignments have been applied to design nodes when using the Classic Timing Analyzer, you can use the Timing Constraint Check feature to report all unconstrained paths in your design. On the Assignments menu, click **Timing Analysis settings**, and click **More Settings**. In the **More Settings** dialog box, turn on **Report Unconstrained Paths**.

Optimize Hold Timing

The **Optimize hold timing** option directs the Quartus II software to optimize minimum delay timing constraints. This option is available only for the Stratix® and Stratix II devices, Cyclone™ series of devices, and

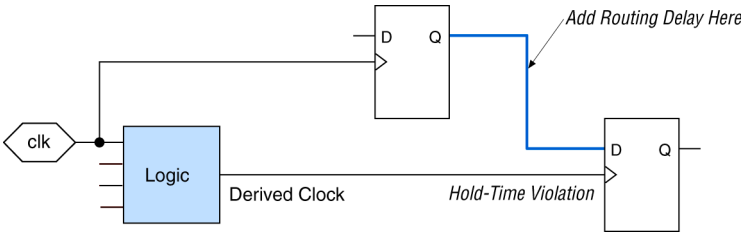
MAX II devices. When you turn on this option, the Quartus II software adds delay to connections to guarantee that the minimum delay requirements are satisfied.

When using the Classic Timing Analyzer, if you choose **I/O Paths and Minimum TPD Paths** (the default choice if you turn on **Optimize hold timing**), the Fitter works to meet the following criteria:

- Hold times (t_H) from device input pins to registers
- Minimum delays from I/O pins or registers to I/O pins or registers (t_{PD})
- Minimum clock-to-out time (t_{CO}) from registers to output pins

If you select **All paths** (or if you're using the TimeQuest Timing Analyzer), the Fitter also works to meet hold requirements from registers to registers, as in Figure 8–3, where a derived clock generated with logic causes a hold time problem on another register. However, if your design has internal hold time violations between registers, Altera recommends that you correct the problems by making changes to your design, such as using a clock enable signal instead of a derived or gated clock.

Figure 8–3. Optimize Hold Timing Option Fixing an Internal Hold Time Violation



For design practices that can help eliminate internal hold time violations, refer to the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Optimize Fast Corner Timing

By default, the Fitter optimizes constraints using the worst-case timing model, which uses the worst-case or slowest timing delay numbers. On the Assignments menu, click **Settings**. In the Category list, select **Fitter Settings**. The Fitter also analyzes the fast delay corner, which uses the best-case or fastest timing numbers. Using the two different timing

models can be important to account for process, voltage, and temperature variations for each device. Turning this option on increases compilation time by approximately 10%.

Asynchronous Control Signal Recovery/Removal Analysis

Determine whether you require the software to analyze the results of recovery and removal checks for paths that end at an asynchronous clear, preset, or load signal of a register. Recovery time is the minimum length of time an asynchronous control signal, for example, clear and preset, must be stable before the active clock edge. Removal time is the minimum length of time an asynchronous control signal must be stable after the active clock edge.

This analysis is turned off by default. Turning on the option adds additional constraints during placement and routing which can increase compilation time and reduce performance. If this analysis is required, on the Assignments menu, click **Settings**. In the Category list, select **Timing Requirements & Options**, then click **More Settings**. Turn on **Enable Recovery/Removal analysis**.

Fitter Effort Setting

On the Assignments menu, click **Settings**. In the Category list, select **Fitter Settings**. The default setting depends on the device family specified.

Use the **Standard Fit** option to exceed specified timing requirements and achieve the best possible timing results for your design. However, this setting usually increases compilation time.

The **Fast Fit** option reduces the amount of optimization effort for each algorithm employed during fitting. This reduces the compilation time by about 50%, resulting in a fit that has, on average, 10% lower f_{MAX} than that achieved using the **Standard Fit** setting. For a small minority of hard-to-fit circuits, the reduced optimization that results from using the **Fast Fit** option can cause the first fitting attempt to fail due to routing problems, resulting in multiple fitting attempts and increased compilation time.

The **Auto Fit** option (available only for Stratix and Cyclone series of devices, and MAX II devices) decreases compilation time by directing the Fitter to reduce Fitter effort after meeting the design's timing requirements and internal routability requirements. The internal routability requirements reduce the possibility of routing congestion and help ensure quick, successful routing. If you want the Fitter to try to

exceed the timing requirements by a certain margin before reducing Fitter effort, specify a minimum slack before reducing Fitter effort in the **Desired worst case slack** box.

The **Auto Fit** option also causes the Quartus II Fitter to optimize for shorter compilation times instead of maximum performance when there are no timing assignments. For designs with no timing assignments, the resulting f_{MAX} is, on average, 10% lower than using the **Standard Fit** option. If your design has aggressive timing requirements or is hard to route, the placement does not stop early, and the compilation time is the same as using the **Standard Fit** option. For designs with no timing requirements, or easily achieved timing requirements, you can achieve an average compilation time reduction of 40% by using the **Auto Fit** option.

Selecting this option does not guarantee that the Fitter meets the design's timing requirements, and specifying a minimum slack does not guarantee that the Fitter achieves the slack requirement.

I/O Assignments

The I/O standards and drive strengths specified for a design affect I/O timing. Specify I/O assignments so that the Quartus II software uses accurate I/O timing delays in timing analysis and Fitter optimizations.

The Quartus II software can choose pin locations automatically for best quality of results. If your pin locations are not fixed due to printed circuit board (PCB) layout requirements, leave pin locations unconstrained to achieve the best results. If your pin locations are already fixed, make pin assignments to constrain the compilation appropriately. "Resource Utilization Optimization Techniques (Macrocell-Based CPLDs)" on page 8–57 includes recommendations for making pin assignments that can have a larger affect on your quality of results in smaller macrocell-based architectures.

Use the **Assignment Editor** and **Pin Planner** to assign I/O standards and pin locations.

For more information about I/O standards and pin constraints, refer to the appropriate handbook. For information about planning and checking I/O assignments, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*. For information about using the Assignment Editor, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Early Timing Estimation

The Quartus II software provides an Early Timing Estimation feature that estimates your design's timing results before the software performs full placement and routing. On the Processing menu, point to Start, and click **Start Early Timing Estimate** to generate initial compilation results after you have run analysis and synthesis. When you want a quick estimate of a design's performance before proceeding with further design or synthesis tasks, this command can save significant compilation time. Using this feature provides a timing estimate up to 45× faster than running a full compilation, and the fit is not fully optimized or routed. Therefore, the timing report is only an estimate. On average, the estimated delays are within 11% of those achieved by a full compilation compared to the final timing results.

You can specify what type of delay estimates to use with this feature. On the Assignments menu, click **Settings**. In the Category list, select **Compilation Process Settings**, and select **Early Timing Estimate**. On the Early Timing Estimate page, the following options are available:

- The **Realistic** option, which is the default, generates delay estimates that will likely be close to the results of a full compilation.
- The **Optimistic** option uses delay estimates that are lower than those likely to be achieved by a full compilation, which results in an optimistic performance estimate.
- The **Pessimistic** option uses delay estimates that are higher than those likely to be achieved by a full compilation, which results in a pessimistic performance estimate.

All three options offer the same reduction in compilation time.

You can use the Timing Closure Floorplan to view the placement estimate created by this feature to identify critical paths in the design. Then, if necessary, you can add or modify floorplan constraints such as LogicLock™ regions, or make other changes to the design. You can then rerun the Early Timing Estimator to quickly assess the impact of any floorplan assignments or logic changes, enabling you to try different design variations and find the best solution.

Design Assistant

You can run the Design Assistant to analyze the post-fitting results of your design during a full compilation. The Design Assistant checks rules related to areas such as gated clocks, reset signals, asynchronous design practices, and signal race conditions. This is especially useful during the early stages of your design, so that you can work on any areas of concern in your design before proceeding with design optimization.

On the Assignments menu, click **Settings**. In the Category list, select **Design Assistant** and turn on **Run Design Assistant during compilation**.

You can also specify which rules you want the Design Assistant to apply when analyzing and generating messages for a design.

Design Analysis

The initial compilation establishes whether the design achieves a successful fit and meets the specified performance. The Compilation Report reports the design results. This section describes how to analyze your design results. After design analysis, proceed to optimization as described in "Optimization Process Stages" on page 8–1.

Error & Warning Messages

After your initial compilation, it is important to evaluate all error and warning messages to see if any design or setting changes are required. If needed, make these changes and recompile the design before proceeding with design optimization.

To suppress messages that you have evaluated and that can be ignored, right-click on the message in the Messages window and click **Suppress**.

For more information about message suppression, refer to the *Message Suppression* section in the *Quartus II Project Management* chapter in volume 2 of the *Quartus II Handbook*.

Ignored Timing Assignments

You can use the Ignored Timings Assignments page in the Compilation Report to view any assignments that were ignored by the Classic Timing Analyzer during the previous compilation. The Classic Timing Analyzer ignores assignments that are invalid, conflict with other assignments, or that become obsolete through the use of other assignments. If any assignments have been ignored, analyze why they have been ignored. If needed, correct the assignments and recompile the design before proceeding with design optimization.

Resource Utilization

Determining device utilization is important regardless of whether a successful fit is achieved. If your compilation results in a no-fit error, then resource utilization information is important so you can analyze the fitting problems in your design. If your fitting is successful, review the

resource utilization information to determine whether the future addition of extra logic or other design changes will introduce fitting difficulties.

To determine resource usage, refer to the **Flow Summary** section of the Compilation Report. This section reports how many pins are used, as well as other device resources such as memory bits, digital signal processing (DSP) block 9-bit elements, and phase-locked loops (PLLs). The **Flow Summary** indicates whether the design exceeds the available device resources. More detailed information is available by viewing the reports under **Resource Section** in the **Fitter** section of the **Compilation Report**.

For the Stratix II family of devices, a device with low utilization does not have the lowest adaptive logic module (ALM) utilization possible. For these devices, the Fitter uses adaptive look-up tables (ALUTs) in different ALMs even when the logic can be placed within one ALM so that it can achieve the best timing and routability results. In achieving these results, logic can be spread throughout the device. As the device fills up, the Fitter automatically searches for logic functions with common inputs to place in one ALM. The number of partnered ALUTs and packed registers also increases.

If resource usage is reported as less than 100% and a successful fit cannot be achieved, either there are not enough routing resources or some assignments are illegal. In either case, a message appears in the **Processing** tab of the Messages window describing the problem.

If the Fitter finishes very quickly, then a resource may be over-utilized or there may be an illegal assignment. If the Quartus II software runs for a long time, then a legal placement or route probably cannot be found. Look for errors and warnings that indicate these types of problems.

You can use the Timing Closure Floorplan to find areas of the device that have routing congestion.

For details about using the Timing Closure Floorplan, refer to the *Timing Closure Floorplan* chapter in volume 2 of the *Quartus II Handbook*.

I/O Timing (Including t_{PD})

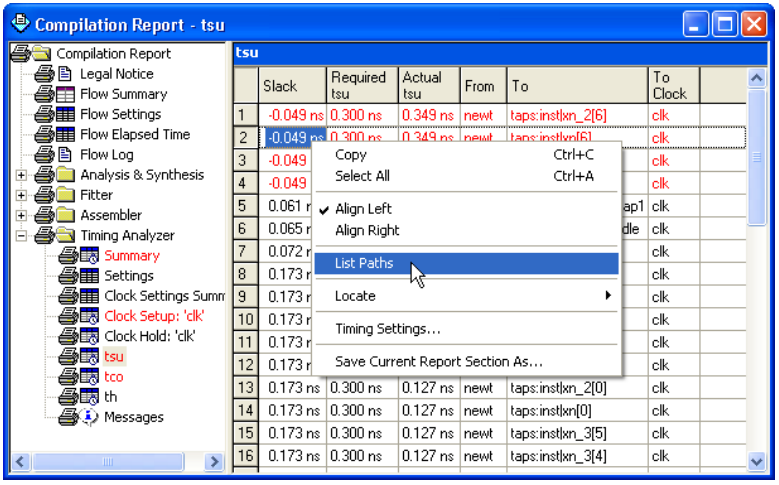
This chapter refers to timing settings and analysis in the Quartus II Classic Timing Analyzer.

For equivalent settings and analysis in the TimeQuest Timing Analyzer, refer to the *TimeQuest Timing Analyzer* and *Switching to the TimeQuest Timing Analyzer* chapters in volume 3 of the *Quartus II Handbook*.

From the Compilation Report, use the **Timing Analyzer** to determine whether or not I/O timing has been met. The t_{SU}, t_H, and t_{CO} reports list the I/O paths, together with the required timing number if you have made a timing requirement, the actual timing number for the timing as reported by the Quartus II software, and the slack, or difference between your requirement and the actual number. If you have any point-to-point propagation delay (t_{PD}) assignments, the t_{PD} report lists the corresponding paths.

The I/O paths that do not meet the required timing performance are reported as having negative slack and are displayed in red (Figure 8–4). In cases when you do not make an explicit I/O timing assignment to an I/O pin, the Quartus II synthesis software still reports the **Actual** number, which is the timing number that must be met for that timing parameter when the device runs in your system.

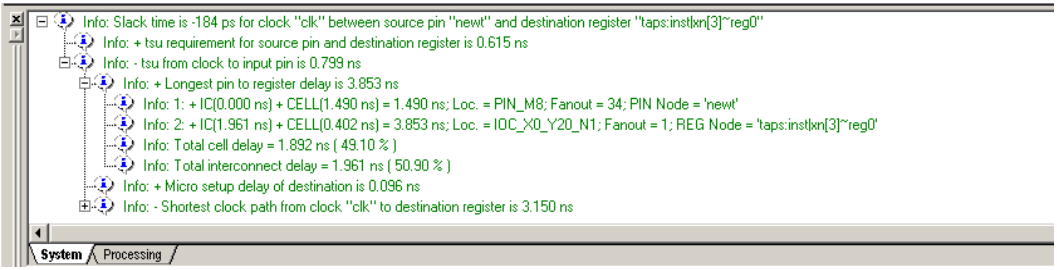
Figure 8–4. I/O Timing Analyzer Report



To analyze the reasons why your timing requirements are not met, right-click an entry in the report and click **List Paths** (Figure 8–4). A message listing the paths appears in the **System** tab of the Messages window. To expand a selection, click the "+" icon at the beginning of the line (Figure 8–5). This is a good method to determine where the greatest delay is located along the path.

The List Paths report lists the slack time and how that slack time was calculated. By expanding the various entries, you can see the incremental delay through each node in the path as well as the total delay. The incremental delay is the sum of the interconnect delay (IC) and the cell delay (CELL) through the logic.

Figure 8–5. I/O Slack Report



To analyze I/O timing, right-click on an I/O entry in the report, point to Locate, and click **Locate in Timing Closure Floorplan** to highlight the I/O path on the floorplan. Negative slack indicates paths that failed to meet their timing requirements. There are also options that allow you to see all the intermediate nodes (combinational logic cells) on a path and the delay for each level of logic. You also can look at the fan-in and fan-out of a selected node.

For more information about how timing numbers are calculated, refer to the *Classic Timing Analyzer* or *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

f_{MAX} Timing

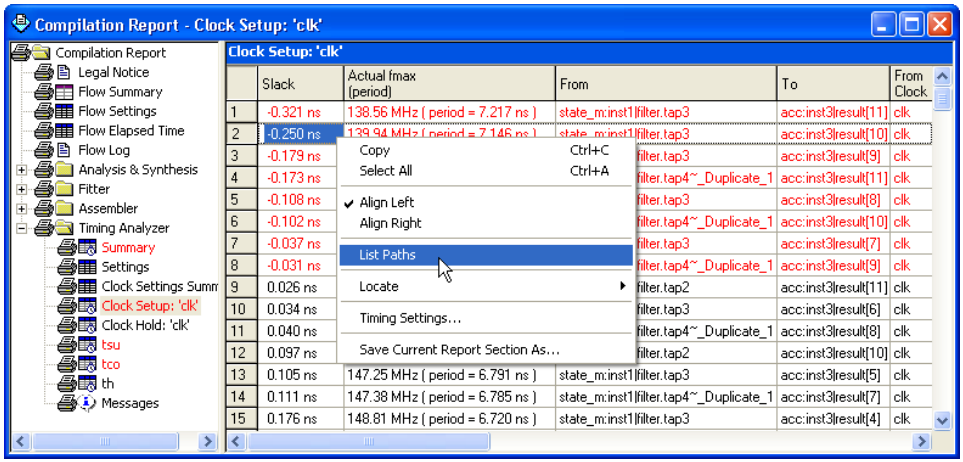
This chapter refers to timing settings and analysis in the Quartus II Classic Timing Analyzer.

For equivalent settings and analysis in the TimeQuest Timing Analyzer, refer to the *TimeQuest Timing Analyzer* or the *Switching to the TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

In the Compilation Report window, use the **Timing Analyzer** section to determine whether f_{MAX} timing requirements are met. The **Clock Setup** folder gives you figures for the actual register-to-register f_{MAX} for each clock as reported by the Quartus II software, and the slack, or difference

between the timing requirement you specified and the actual compilation results. The paths that do not meet timing requirements are shown with a negative slack and appear in red (Figure 8–6).

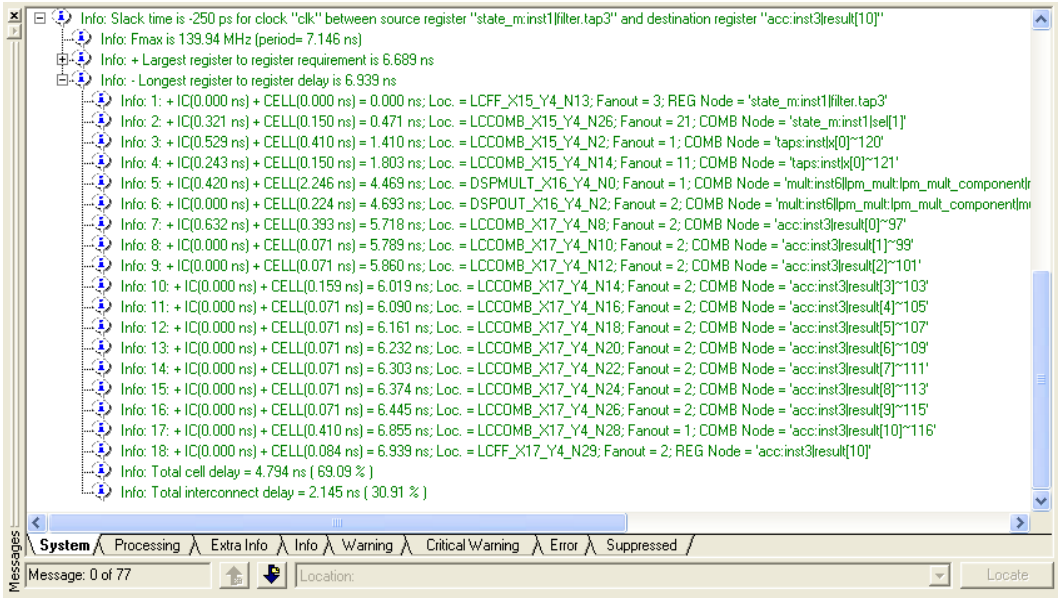
Figure 8–6. f_{MAX} Timing Analysis Report



To analyze why your timing requirements were not met, right-click on an entry in the report and click **List Paths** (Figure 8–6). A message listing the paths appears in the **System** tab of the Messages window. To expand a selection, as shown in Figure 8–7, click the "**+**" icon at the beginning of the line. This is a good way to determine where the greatest delay is located along the path.

The List Paths report shows the slack time and how that slack time was calculated. By expanding the various entries, you can see the incremental delay through each node in the path as well as the total delay. The incremental delay is the sum of the interconnect delay (IC) and the cell delay (CELL) through the logic.

Figure 8–7. f_{MAX} Slack Report



To visually analyze f_{MAX} paths, right-click on a path, point to Locate, and click **Locate in Timing Closure Floorplan**. The Timing Closure Floorplan is shown and the path is highlighted. Use the **Critical Path Settings** to select which failing paths to show. To turn critical paths on or off, use the **Show Critical Paths** command.

For more information about how timing analysis results are calculated, refer to the *Classic Timing Analyzer* or the *TimeQuest Timing Analyzer* chapters in volume 3 of the *Quartus II Handbook*.

You also can see the logic in a particular path by cross-probing to the RTL Viewer or Technology Map Viewer. These viewers allow you to see a gate-level or technology-mapped representation of your design netlist. To locate a timing path in one of the viewers, right-click on a path in the report, point to Locate, and click **Locate in RTL Viewer** or **Locate in Technology Map Viewer**. When you locate a timing path in the Technology Map Viewer, the annotated schematic displays the same delay information that is shown when you use the List Paths command.

For more information about the netlist viewers, refer to the *Analyzing Designs with Quartus II Netlist Viewers* chapter in volume 1 of the *Quartus II Handbook*.

Tips for Analyzing Failing Paths

When you are analyzing clock path failures, focus on improving the paths that show the worst slack. The Fitter works hardest on paths with the most slack. If you fix these paths, the Fitter may be able to improve the other failing timing paths in the design.

Check for particular nodes that appear in many failing paths. Look for paths that have common source registers, destination registers, or common intermediate combinational nodes. In some cases, the registers may not be identical, but are part of the same bus. It can be helpful to click on the **From** or **To** column headers to sort the paths by the source or destination registers. Clicking first on **From**, then on **To**, uses the **To** register as the primary sort and **From** as the secondary sort. If you see common nodes, these nodes indicate areas of your design that could possibly be improved through source code changes or Quartus II optimization settings. Constraining the placement for just one of the paths could worsen the timing performance for other paths by moving the common node further away in the device.

Tips for Analyzing Failing Clock Paths that Cross Clock Domains

When analyzing clock path failures, check whether these paths cross between two clock domains. This is the case if the **From Clock** and **To Clock** in the timing analysis report are different. There could also be paths that involve a different clock in the middle of the path, even if the source and destination register clock are the same. To analyze these paths in more detail, right-click on the entry in the report and click **List Paths**.

Expand the **List Paths** entry in the **Messages** window and analyze the largest register to register requirement. Evaluate the setup relationship between the source and destination (launch edge and latch edge) to determine if that is reducing the available setup time. For example, the path may go from a rising edge to a falling edge, which reduces the setup relationship by one half clock cycle.

Check if the PLL phase shift is reducing the setup requirement. You may be able to adjust this using PLL parameters and settings.

Check if the PLL compensation delay is reducing the setup relationship. You can direct the software to analyze this delay as clock skew by enabling Clock Latency. On the **Assignments** menu, click **Settings** and choose **Timing Requirements & Options**. Click **More Settings** and turn on **Enable Clock Latency**. This option should typically be enabled if your design results in timing violations for paths that pass between PLL clock domains.

Evaluate the clock skew between the source clock and the destination clock to determine if that is reducing the available setup time. You can check the shortest and longest clock path reports to see what is causing any clock skew. Avoid using combinational logic in clock paths because it contributes to clock skew. Differences in the logic or in its routing between the source and destination can cause clock skew problems and result in warnings during compilation.

Global Routing Resources

Check the global signal utilization in your design to ensure that appropriate signals have been placed on global routing resources. In the Compilation Report, open the Fitter report and click the **Resource Section**. Analyze the **Global & Other Fast Signals** and **Non-Global High Fan-out Signals** reports to see if any changes are required.

You may be able to reduce clock skew for high fan-out signals by placing them on global routing resources. Conversely, you can reduce the insertion delay of low fan-out signals by removing them from global routing resources. Doing so can improve clock enable timing and control signal recovery/removal timing, but increases clock skew. You also can use the **Global Signal** setting in the **Assignment Editor** to control global routing resources. If the signal fan-out is low and it feeds locations in one area of the device, you can use any regional or fast regional clocks available.

Compilation Time

In long compilations, most of the time is spent in the Analysis & Synthesis and Fitter modules. Analysis & Synthesis includes synthesis netlist optimizations, if you have turned on those options. The Fitter includes two steps, placement and routing, and also includes physical synthesis if you turned on those options. The **Flow Elapsed Time** section of the Compilation Report shows how much time is spent running the Analysis & Synthesis and Fitter modules. The **Fitter Messages** report in the **Fitter** section of the Compilation Report shows specifically how much time was spent in placement and how much time was spent in routing.

The applicable messages say `Info: Fitter placement operations ending: elapsed time = <n> seconds` and `Info: Fitter routing operations ending: elapsed time = <n> seconds`.

Placement is the process of finding optimum locations for the logic in your design. Routing is the process of connecting the nets between the logic in your design. There are many possible placements for the logic in

a design, and finding better placements typically takes more compilation time. Good logic placement allows you to more easily meet your timing requirements and makes the design easy to route.

Resource Utilization Optimization Techniques (LUT-Based Devices)

After design analysis, the next stage of design optimization is to improve resource utilization. Complete this stage before proceeding to I/O timing optimization or f_{MAX} timing optimization. Ensure that you have already set the basic constraints described in "Initial Compilation" on page 8–5 before proceeding with the resource utilization optimizations discussed in this section. If a design does not fit into a specified device, use the techniques in this section to achieve a successful fit. After you optimize resource utilization and your design fits in the desired target device, optimize I/O timing as described in the ""I/O Timing Optimization Techniques (LUT-Based Devices)" on page 8–33.

Resolving Resource Utilization Issues Summary

Resource utilization issues can be divided into the following three categories:

- Issues relating to I/O pin utilization or placement, including dedicated I/O blocks such as PLLs or LVDS transceivers ("I/O Pin Utilization or Placement" on page 8–20).
- Issues relating to logic utilization or placement, including logic cells containing registers and look-up-tables as well as dedicated logic such as memory blocks and DSP blocks ("Logic Utilization or Placement" on page 8–21).
- Issues relating to routing ("Routing" on page 8–31).

I/O Pin Utilization or Placement

Use the suggestions in the following sections to help you resolve I/O resource problems.

Use I/O Assignment Analysis

On the Processing menu, point to **Start** and click **Start I/O Assignment Analysis** to help with pin placement. The **Start I/O Assignment Analysis** command allows you to check your I/O assignments early in the design process. You can use this command to check the legality of pin assignments before, during, or after compilation of your design. If design files are available, you can use this command to perform more thorough legality checks on your design's I/O pins and surrounding logic. These checks include proper reference voltage pin usage, valid pin location assignments, and acceptable mixed I/O standards.

Common issues with I/O placement relate to the fact that differential standards have specific pin pairings, and certain I/O standards may be supported only on certain I/O banks.

If your compilation or I/O assignment analysis results in specific errors relating to I/O pins, follow the recommendations in the error message. Right-click on the message in the Messages window and click **Help** to open the Quartus II Help topic for this message.

Modify Pin Assignments or Choose a Larger Package

If a design that has pin assignments fails to fit, compile the design without the pin assignments to determine whether a fit is possible for the design in the specified device and package. You can use this approach if a Quartus II error message indicates fitting problems due to pin assignments.

If the design fits when all pin assignments are ignored or when several pin assignments are ignored or moved, you may have to modify the pin assignments for the design or choose a larger package.

If the design fails to fit because of lack of available I/Os, a successful fit can often be obtained by using a larger device package (which could be the same device density) that has more available user I/O pins.

For more information about I/O assignment analysis, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

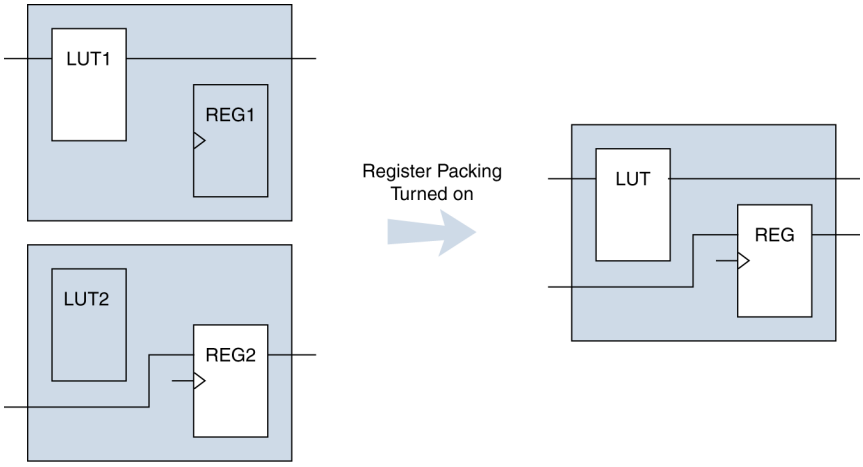
Logic Utilization or Placement

Use the suggestions in the following subsections to help you resolve logic resource problems, including logic cells containing registers and look-up-tables as well as dedicated logic such as memory blocks and DSP blocks.

Use Register Packing

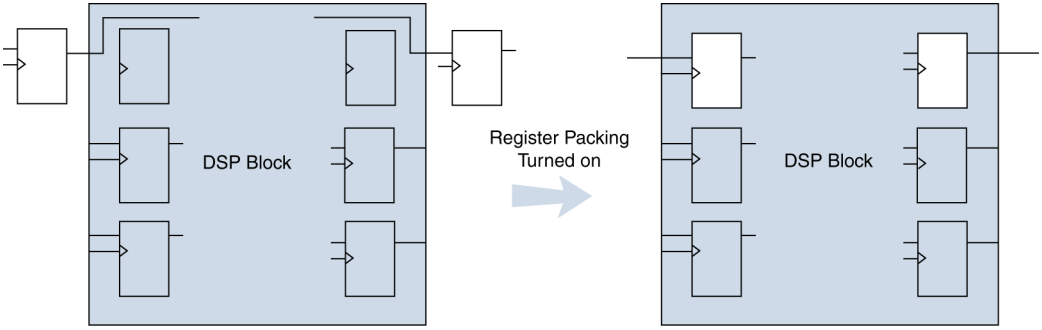
The **Auto Packed Registers** option implements the functions of two cells into one logic cell by combining the register of one cell in which only the register is used with the lookup table (LUT) of another cell in which only the LUT is used. Figure 8–8 shows register packing and the gain of one logic cell in the design.

Figure 8–8. Register Packing



Registers can also be packed into DSP blocks (Figure 8–9).

Figure 8–9. Register Packing in DSP Blocks



The following list shows the most common cases in which register packing helps to optimize a design:

- A LUT can be implemented in the same cell as an unrelated register with a single data input
- A LUT can be implemented in the same cell as the register that is fed by the LUT
- A LUT can be implemented in the same cell as the register that feeds the LUT
- A register can be packed into a RAM block
- A register can be packed into a DSP block
- A register can be packed into an I/O Element (IOE)

The following options are available for register packing (for certain device families):

- **Off**—Does not pack registers.
- **Normal**—Default setting packs registers when this is not expected to hurt timing results.
- **Minimize Area**—Aggressively packs registers to reduce area.
- **Minimize Area with Chains**—Aggressively packs registers to reduce area. This option packs registers with carry chains. It also converts registers into register cascade chains and packs them with other logic to reduce area. This option is available only for Stratix and Cyclone series devices, and MAX II devices.
- **Auto**—Attempts to achieve the best performance while maintaining a fit for the design in the specified device. The Fitter combines all combinational (LUT) and sequential (register) functions that benefit circuit speed. In addition, more aggressive combinations of unrelated combinational and sequential functions are performed to the extent required to reduce the area of the design to achieve a fit in the specified device. This option is available only for Stratix and Cyclone series devices, and MAX II devices.

Turning on register packing decreases the number of logic elements (LEs) or adaptive logic modules (ALMs) in the design, but could also decrease performance in some cases. On the Assignments menu, click **Settings**. In the Category list, select **Fitter Settings**, and then click **More Settings.** Turn on **Auto Packed Registers** to turn on register packing.

The area reduction and performance results can vary greatly depending on the design. Typical results for register packing are shown in the following tables. Table 8–1 shows typical results for Stratix II devices. Table 8–2 shows typical results for Cyclone II devices, and Table 8–3 shows typical results for Stratix, Stratix GX, and Cyclone devices.

The **Auto** setting performs more aggressive register packing as needed, so the typical results vary depending on the device resource utilization.

Table 8–1. Typical Register Packing Results for Stratix II Devices

Register Packing Setting	Relative f_{MAX}	Relative LE Count
Off	0.95	1.29
Normal	1.00	1.00
Minimize Area	0.98	0.97
Minimize Area with Chains	0.98	0.97
Auto (default)	1.0 until device is very full, then gradually to 0.98 as required	1.0 until device is very full, then gradually to 0.97 as required

Table 8–2 shows typical results for Cyclone II devices.

Table 8–2. Typical Register Packing Results for Cyclone II Devices

Register Packing Setting	Relative f_{MAX}	Relative LE Count
Off	0.97	1.40
Normal	1.00	1.00
Minimize Area	0.96	0.93
Minimize Area with Chains	0.94	0.91
Auto (default)	1.0 until device is very full, then gradually to 0.94 as required	1.0 until device is very full, then gradually to 0.91 as required

Table 8–3 shows results for Stratix, Stratix GX, and Cyclone devices.

Table 8–3. Typical Register Packing Results for Stratix, Stratix GX & Cyclone Devices

Register Packing Setting	Relative f_{MAX}	Relative LE Count
Off	1.00	1.12
Normal	1.00	1.00
Minimize Area	0.97	0.93
Minimize Area with Chains	0.94	0.90
Auto (default)	1.0 until device is very full, then gradually to 0.94 as required	1.0 until device is very full, then gradually to 0.90 as required

Remove Fitter Constraints

A design with conflicting constraints or constraints that are difficult to meet may not fit the targeted device. This can occur when the location or LogicLock assignments are too strict and there are not enough routing resources.

In this case, use the **Routing Congestion** view in the Timing Closure Floorplan to locate routing problems in the floorplan, then remove any location or LogicLock region assignments in that area. If your design still does not fit, the design is over-constrained. To correct the problem, remove all location and LogicLock assignments and run successive compilations, incrementally constraining the design before each compilation. You can delete specific location assignments in the Assignment Editor or Timing Closure Floorplan. Remove LogicLock assignments in the Timing Closure Floorplan or the **LogicLock Regions Window**, or, on the Assignments menu, click **Remove Assignments.** Turn on the assignment categories you want to remove from the design in the **Available assignment categories** list.

For more information about the **Routing Congestion** view in the Timing Closure Floorplan, refer to the Quartus II Help.

Perform WYSIWYG Resynthesis with Balanced or Area Setting

If you use another EDA synthesis tool and want to determine if the Quartus II software can remap the circuit to use fewer LEs or ALMs, follow these steps:

1. On the Assignments menu, click **Settings**. In the Category list, select **Analysis & Synthesis Settings**, and turn on **Perform WYSIWYG primitive resynthesis (using optimization techniques specified in Analysis & Synthesis settings)** on the **Synthesis Netlist Optimizations** page. Or, on the Assignments menu, click **Assignment Editor**, and apply the **Perform WYSIWYG Primitive Resynthesis** logic option to a specific module in your design.

2. On the Assignments menu, click **Settings**. In the Category list, select **Analysis & Synthesis Settings**, and choose **Balanced** or **Area** under Optimization Technique. Or, on the Assignments Menu, click **Assignment Editor**. Set the Optimization Technique to **Balanced** or **Area** for a specific module in your design.

3. Recompile the design.

The **Balanced** setting typically produces utilization results that are very similar to the Area setting, with better performance results. The Area setting may give better results in some unusual cases. Performing WYSIWYG resynthesis for area in this way typically reduces f_{MAX}.

Optimize Synthesis for Area, not Speed

If your design fails to fit because it uses too much logic, resynthesize the design to improve the area utilization. First, ensure that you have set your device and timing constraints correctly in your synthesis tool. Particularly when the area utilization of the design is a concern, ensure that you do not over-constrain the timing requirements for the design. Synthesis tools generally try to meet the specified requirements, which can result in higher device resource usage if the constraints are too aggressive.

If resource utilization is an important concern, some synthesis tools offer an easy way to optimize for area instead of speed. If you are using Quartus II integrated synthesis, choose **Balanced** or **Area** for the **Optimization Technique**. You can also specify this logic option for specific modules in your design with the Assignment Editor in cases where you want to reduce area using the **Area** setting (potentially at the expense of f_{MAX} performance) while leaving the default **Optimization Technique** setting at **Balanced** (for the best trade-off between area and speed for certain device families) or **Speed**. You can also use the **Speed Optimization Technique for Clock Domains** logic option to specify that all combinational logic in or between the specified clock domain(s) is optimized for speed.

In some synthesis tools, not specifying an f_{MAX} requirement may result in less resource utilization.

In the Quartus II software, the **Balanced** setting typically produces utilization results that are very similar to those produced by the **Area** setting, with better performance results. The **Area** setting may give better results in some unusual cases.

For information about setting timing requirements and synthesis options in Quartus II integrated synthesis and other synthesis tools, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*, or your synthesis software's documentation.

Other attributes or options can also help improve the quality of synthesis results, including the recommendations in the following sections.

Change State Machine Encoding

State machines can be encoded using various techniques. Using binary or gray code encoding typically results in fewer state registers than one-hot encoding, which requires one register for every state bit. If your design contains state machines, changing the state machine encoding to one that uses the minimal number of registers may reduce resource utilization. The effect of state machine encoding varies depending on the way your design is structured.

If your design does not manually encode the state bits, you can specify the state machine encoding in your synthesis tool. When using Quartus II Integrated Synthesis, go to the Assignments menu and click **Settings**. In the Category list, select A**nalysis & Synthesis Settings** and turn on **Minimal Bits for State Machine Processing**. You also can specify this logic option for specific modules or state machines in your design with the Assignment Editor.

Flatten the Hierarchy During Synthesis

Synthesis tools typically provide the option of preserving hierarchical boundaries, which may be useful for verification or other purposes. However, optimizing across hierarchical boundaries allows the synthesis tool to perform the most logic minimization, which can reduce area. Therefore, to achieve the best results, flatten your design hierarchy whenever possible. If you are using Quartus II integrated synthesis, ensure that the **Preserve Hierarchical Boundary** logic option is turned off, that is, make sure that you have not turned on the option in the Assignment Editor or with Tcl assignments. If you are using Quartus II incremental compilation, you cannot flatten your design across design partitions. Incremental compilation always preserves the hierarchical boundaries between design partitions.

For more information about using incremental compilation and recommendations for design partitioning, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*. If you are using an incremental synthesis flow that requires separate hierarchy blocks, you can find additional recommendations for design partitioning in the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Follow Altera's recommendations for design partitioning such as registering partition boundaries to reduce the effect of cross-boundary optimizations.

Restructure Multiplexers

Multiplexers form a large portion of the logic utilization in many FPGA designs. By optimizing your multiplexed logic, you can achieve a more efficient implementation in your Altera device.

The Quartus II software provides the **Restructure Multiplexers** logic option, which can extract and optimize buses of multiplexers during synthesis. This option is available on the **Analysis & Synthesis Settings** page of the **Settings** dialog box and is useful if your design contains buses of fragmented multiplexers. This option restructures multiplexers more efficiently for area, allowing the design to implement multiplexers with a reduced number of LEs or ALMs. Using the Restructure Multiplexers logic option can reduce your design's f_{MAX}. This option is turned on automatically when you set the **Quartus II Analysis & Synthesis Optimization Technique** option to **Area** or **Balanced**. To change the default setting, on the Assignments menu, click **Settings**. In the Category list, select **Analysis & Synthesis Settings**, and click the appropriate option from the **Restructure Multiplexers** list to set the option globally.

For design guidelines to achieve optimal resource utilization for multiplexer designs, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*. For more information about the Restructure Multiplexers option in the Quartus II software, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

Retarget Memory Blocks

If the design fails to fit because it runs out of device memory resources, it might be due to a lack of a certain type of memory. For example, a design that requires two M-RAM blocks might be targeted to a Stratix EP1S10 device, which has only one M-RAM block. By building one of the memories with a different size memory block, such as an M4K memory block, you might obtain a fit.

If the memory was created with the MegaWizard® Plug-In Manager, open the MegaWizard Plug-In Manager and edit the RAM block type so it targets a new memory block size.

ROM and RAM memory blocks can also be inferred from your HDL code, and your synthesis software can place large shift registers into memory blocks by inferring the `altshift_taps` megafunction. This inference can be turned off in your synthesis tool to cause the memory to be placed in logic instead of in memory blocks. To disable inference when using Quartus II Integrated Synthesis, on the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis**, and turn off

the **Auto RAM Replacement**, **Auto ROM Replacement**, or **Auto Shift Register Replacement** logic option as appropriate for your project. Or, disable the option for a specific entity in the Assignment Editor.

Depending on your synthesis tool, you can also set the RAM block type for inferred memory blocks. In Quartus II integrated synthesis, set the **ramstyle** attribute to the desired memory type for the inferred RAM blocks: `M512`, `M4K`, or `M-RAM`, or set the option to **logic** to implement the memory block in standard logic instead of a memory block.

For more information about memory inference control in other synthesis tools, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*, or your synthesis software's documentation. For more information about coding styles and HDL examples that ensure memory inference, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

Retarget or Balance DSP Blocks

A design may not fit because it requires too many DSP blocks. All DSP block functions can be implemented with logic cells, so you can retarget some of the DSP blocks to logic to obtain a fit.

If the DSP function was created with the MegaWizard Plug-In Manager, open the MegaWizard Plug-In Manager and edit the function so it targets logic cells instead of DSP blocks. The Quartus II software uses the `DEDICATED_MULTIPLIER_CIRCUITRY` megafunction parameter to control the implementation.

DSP blocks also can be inferred from your HDL code for multipliers, multiply-adders, and multiply-accumulators. This inference can be turned off in your synthesis tool. When you are using Quartus II integrated synthesis, you can disable inference by turning off the Auto DSP Block Replacement logic option for your whole project. On the Assignments menu, click **Settings**. In the Category list, select **Analysis & Synthesis Settings**, and turn off **Auto DSP Block Replacement**. Alternatively, you can disable the option for a specific block with the Assignment Editor.

For more information about disabling DSP block inference in other synthesis tools, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*, or your synthesis software's documentation.

The Quartus II software also offers the **DSP Block Balancing** logic option, which implements DSP block elements in logic cells or in different DSP block modes. The default **Auto** setting allows DSP block balancing

to convert the DSP block slices automatically as appropriate to minimize the area and maximize the speed of the design. You can use other settings for a specific node or entity, or on a project-wide basis, to control how the Quartus II software converts DSP functions into logic cells and DSP blocks. Using any value other than **Auto** or **Off** overrides the `DEDICATED_MULTIPLIER_CIRCUITRY` parameter used in megafunction variations.

For more details about the Quartus II logic options described in this section, refer to the Quartus II Help.

Optimize Source Code

If your design does not fit because of logic utilization, and the methods described in the preceding sections do not sufficiently improve the resource utilization of the design, modify the design at the source to achieve the desired results. You can often improve logic significantly by making design-specific changes to your source code. This is typically the most effective technique for improving the quality of your results.

If your design does not fit into available LEs or ALMs, but you have unused memory or DSP blocks, check to see if you have code blocks in your design that describe memory or DSP functions that are not being inferred and placed in dedicated logic. You may be able to modify your source code to allow these functions to be placed into dedicated memory or DSP resources in the target device.

Ensure that your state machines are recognized as state machine logic and optimized appropriately in your synthesis tool. State machines that are recognized are generally optimized better than if the synthesis tool treats them as generic logic. In the Quartus II software, you can check for the **State Machine** report under **Analysis & Synthesis** in the Compilation Report. This report provides details, including the state encoding for each state machine that was recognized during compilation. If your state machine is not being recognized, you may need to change your source code to enable it to be recognized.

For coding style guidelines including examples of HDL code for inferring memory and DSP functions, refer to the *Inferring and Instantiating Altera Megafunctions* section of the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*. For guidelines and sample HDL code for state machines, refer to the *State Machines* section in the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

Use a Larger Device

If a successful fit cannot be achieved because of a shortage of LEs or ALMs, memory, or DSP blocks, you may need to use a larger device.

Routing

Use the suggestions in the following subsections to help you resolve routing resource problems.

Set Fitter Aggressive Routability Optimizations to Always

If routing resources are resulting in no-fit errors, use this option to reduce routing wire utilization. On the Assignments menu, click **Settings**. In the Category list, select **Fitter Settings**. Click **More Settings**. In the More Fitter Settings dialog box, set **Fitter Aggressive Routability Optimizations** to **Always** and click **OK**. On average, in Stratix II devices, the option saves approximately 3% wire utilization but can hurt performance by approximately 1%.

These optimizations are used automatically when the Fitter performs more than one fitting attempt, but turning the option on increases the optimization effort on the first fitting attempt.

Increase Placement Effort Multiplier

Increasing the placement effort can improve the routability of the design, allowing the software to route a design that otherwise requires too many routing resources. On the Assignments menu, click **Settings**. In the Category list, select **Fitter Settings**. Click **More Settings**. In the More Fitter Settings dialog box, increase the value of the **Placement Effort Multiplier** to increase placement effort. The default value is `1.0`. Legal values must be greater than `0` and can be non-integer values. Higher numbers increase compilation time but may improve placement quality. For example, a value of `4` increases fitting time by approximately 2 to 4 times but may increase the quality of results.

Increased effort is used automatically when the Fitter performs more than one fitting attempt, but turning the option on increases the optimization effort on the first fitting attempt.

Remove Fitter Constraints

A design with conflicting constraints or constraints that are difficult to meet may not fit the targeted device. This can occur when location or LogicLock assignments are too strict and there are not enough routing resources.

In this case, use the **Routing Congestion** view in the Timing Closure Floorplan to locate routing problems in the floorplan, then remove any location or LogicLock region assignments from that area. If your design still does not fit, the design is over-constrained. To correct the problem, remove all location and LogicLock assignments and run successive compilations, incrementally constraining the design before each compilation. You can delete specific location assignments in the Assignment Editor or Timing Closure Floorplan. On the Assignments menu, click **LogicLock Regions Window** to remove LogicLock assignments. Or, on the Assignments menu, click **Remove Assignments** and turn on the assignment categories you want to remove from the design in the **Available assignment categories** list.

For more information about the **Routing Congestion** view in the Timing Closure Floorplan, refer to the Quartus II Help. The Routing Congestion view is available on the View menu if you enable **Field View**.

Optimize Synthesis for Area, Not Speed

In some cases, resynthesizing the design to improve the area utilization can also improve the routability of the design. First, ensure that you have set your device and timing constraints correctly in your synthesis tool. Ensure that you do not over-constrain the timing requirements for the design, particularly when the area utilization of the design is a concern. Synthesis tools generally try to meet the specified requirements, which can result in higher device resource usage if the constraints are too aggressive.

If resource utilization is important to improving the routing results in your design, some synthesis tools offer an easy way to optimize for area instead of speed. If you are using Quartus II integrated synthesis, on the Assignments menu, click **Settings**. In the Category list, select **Analysis & Synthesis Settings**, and choose **Balanced** or **Area** under **Optimization Technique**.

You can also specify this logic option for specific modules in your design with the Assignment Editor in cases where you want to reduce area using the **Area** setting (potentially at the expense of f_{MAX} performance). You can apply the setting to specific modules while leaving the default Optimization Technique setting at **Balanced** (for the best trade-off between area and speed for certain device families) or **Speed**. You can also use the **Speed Optimization Technique for Clock Domains** logic option to specify that all combinational logic in or between the specified clock domain(s) is optimized for speed.

In the Quartus II software, the **Balanced** setting typically produces utilization results that are very similar to those obtained with the **Area** setting, with better performance results. The Area setting may give better results in some unusual cases.

In some synthesis tools, not specifying an f_{MAX} requirement may result in less resource utilization which may improve routability.

For information about setting timing requirements and synthesis options in Quartus II integrated synthesis and other synthesis tools, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*, or your synthesis software's documentation.

Optimize Source Code

If your design does not fit because of routing problems, and the methods described in the preceding sections do not sufficiently improve the routability of the design, modify the design at the source to achieve the desired results. You can often improve results significantly by making design-specific changes to your source code, such as duplicating logic or changing the connections between blocks that require significant routing resources.

Use a Larger Device

If a successful fit cannot be achieved because of a shortage of routing resources, you may need to use a larger device.

I/O Timing Optimization Techniques (LUT-Based Devices)

The next stage of design optimization focuses on I/O timing. Ensure that you have made the appropriate assignments as described in "Initial Compilation" on page 8–5, and that the resource utilization is satisfactory, before proceeding with I/O timing optimization. Because changes to the I/O paths affect the internal f_{MAX}, complete this stage before proceeding to the f_{MAX} timing optimization stage as described in the "f_{MAX} Timing Optimization Techniques (LUT-Based Devices)" on page 8–40.

The options presented in this section address how to improve I/O timing, including the setup delay (t_{SU}), hold time (t_H), and clock-to-output (t_{CO}) parameters.

Improving Setup & Clock-to-Output Times Summary

Table 8–4 shows the recommended order in which to use techniques to reduce t_{SU} and t_{CO} times. Check marks indicate which timing parameters are affected by each technique. Reducing t_{SU} times increases hold (t_H) times.

Table 8–4. Improving Setup & Clock-to-Output Times *Note (1)*

Technique	Affects t_{SU}	Affects t_{CO}
Ensure that the appropriate constraints are set for the failing I/Os (page 8–10)	✓	✓
Use timing-driven compilation for I/O (page 8–34)	✓	✓
Use fast input register (page 8–35)	✓	—
Use fast output register and fast output enable register (page 8–35)	—	✓
Set Decrease Input Delays to Input Register = ON or decrease the value of Input Delay from Pin to Input Register (page 8–36)	✓	—
Set Decrease Input Delays to Internal Cells = ON or decrease the value of Input Delay from Pin to Internal Cells (page 8–36)	✓	—
Set Increase Delay to Output Pin = OFF or decrease the value of Delay from Output Register to Output Pin (page 8–36)	—	✓
Increase the value of Input Delay from Dual-Purpose Clock Pin to Fan-Out Destinations (page 8–38)	✓	—
Use PLLs to shift clock edges (page 8–38)	✓	✓
Use the Fast Regional Clock option (page 8–39)	—	✓
For MAX II devices, set **Guarantee I/O paths** to zero, **Hold Time at Fast Timing Corner** to OFF, or When t_{SU} and t_{PD} constraints permit (page 8–39)	✓	—

Note to Table 8–4:
(1) These options may not apply to all device families.

Timing-Driven Compilation

To perform I/O timing optimization using the **Optimize IOC Register Placement For Timing**, perform the following steps.

1. On the Assignments menu, click **Settings**.
2. In the Category list, select **Fitter Settings** and click **More Settings**.
3. In the More Fitter Settings dialog box, under **Existing options settings**, select **Optimize IOC Register Placement for Timing**.

This option moves registers into I/O elements if required to meet t_{SU} or t_{CO} assignments, duplicating the register if necessary (as in the case where a register fans out to multiple output locations). This option is enabled by default and is a global setting. The option does not apply to MAX II devices because they do not contain I/O registers.

For APEX™ 20KE and APEX 20KC devices, if the I/O register is not available, the Fitter tries to move the register into the logic array block (LAB) adjacent to the I/O element.

The **Optimize IOC Register Placement for Timing** option affects only pins that have a t_{SU} or t_{CO} requirement. Using the I/O register is only possible if the register directly feeds a pin or is fed directly by a pin. This setting does not affect registers with the following characteristics:

- Have combinational logic between the register and the pin
- Are part of a carry or cascade chain
- Have an overriding location assignment
- Use the synchronous load or asynchronous clear ports of APEX 20K and APEX II devices
- Are input registers that use the synchronous load port and the value is not 1 (in device families where the port is available, other than APEX 20K, APEX II, and FLEX® 6000 devices)
- Use the asynchronous load port and the value is not 1 (in device families where the port is available)

Registers with the characteristics listed are optimized using the regular Quartus II Fitter optimizations.

Fast Input, Output & Output Enable Registers

You can place individual registers in I/O cells manually by making fast I/O assignments with the Assignment Editor. For an input register, use the **Fast Input Register** option; for an output register, use the **Fast Output Register** option; and for an output enable register, use the **Fast Output Enable Register** option. In MAX II devices, which have no I/O registers, these assignments lock the register into the LAB adjacent to the I/O pin if there is a pin location assignment for that I/O pin.

If the fast I/O setting is on, the register is always placed in the I/O element. If the fast I/O setting is off, the register is never placed in the I/O element. This is true even if the **Optimize IOC Register Placement for Timing** option is turned on. If there is no fast I/O assignment, the Quartus II software determines whether to place registers in I/O elements if the **Optimize IOC Register Placement for Timing** option is turned on.

The three fast I/O options (**Fast Input Register**, **Fast Output Register**, and **Fast Output Enable Register**) also can be used to override the location of a register that is in a LogicLock region, and force it into an I/O cell. If this assignment is applied to a register that feeds multiple pins, the register is duplicated and placed in all relevant I/O elements. In MAX II devices, the register is duplicated and placed in each distinct LAB location that is next to an I/O pin with a pin location assignment.

Programmable Delays

Various programmable delay options can be used to minimize the t_{SU} and t_{CO} times. For Stratix series devices, Cyclone series devices, and MAX II devices, the Quartus II software automatically adjusts the applicable programmable delays to help meet timing requirements. For APEX series devices, the default values are set to avoid any hold time problems. Programmable delays are advanced options that you should use only after you compile a project, check the I/O timing, and determine that the timing is unsatisfactory. For detailed information about the effect of these options, refer to the device family handbook or data sheet.

After you have made a programmable delay assignment and compiled the design, you can view the value of every delay chain for every I/O pin in the **Delay Chain Summary** section of the Quartus II Compilation Report.

You can assign programmable delay options to supported nodes with the Assignment Editor. You also can view and modify the delay chain setting for the target device with the Quartus II Chip Editor and Resource Property Editor. When you use the Resource Property Editor to make changes after performing a full compilation, recompiling the entire design is not necessary; you can save changes directly to the netlist. Because these changes are made directly to the netlist, the changes are not made again automatically when you recompile the design. The change management features allow you to reapply the changes on subsequent compilations.

For more information about using the Quartus II Chip Editor and Resource Property Editor, refer to the *Design Analysis & Engineering Change Management with Chip Editor* chapter in volume 3 of the *Quartus II Handbook*.

Table 8–5 summarizes the programmable delays available for Altera devices.

Table 8–5. Programmable Delays for Altera Devices (Part 1 of 2)

Programmable Delay	Description	I/O Timing Impact	Device Families
Decrease input delay to input register	Decreases propagation delay from an input pin to the data input of the input register in the I/O cell associated with the pin. Applied to input/bidirectional pin or register it feeds.	Decreases t_{SU} Increases t_H	Stratix, Stratix GX, Cyclone, APEX II, APEX 20KE, APEX 20KC, Mercury™, MAX 7000B
Input delay from pin to input register	Sets propagation delay from an input pin to the data input of the input register implemented in the I/O cell associated with the pin. Applied to input/bidirectional pin.	Changes t_{SU} Changes t_H	Stratix II, Stratix II GX, Cyclone II
Decrease input delay to internal cells	Decreases the propagation delay from an input or bidirectional pin to logic cells and embedded cells in the device. Applied to input/bidirectional pin or register it feeds.	Decreases t_{SU} Increases t_H	Stratix, Stratix GX, Cyclone, APEX II, APEX 20KE, APEX 20KC, Mercury, FLEX 10K®, FLEX 6000, ACEX® 1K
Input delay from pin to internal cells	Sets the propagation delay from an input or bidirectional pin to logic and embedded cells in the device. Applied to a input or bidirectional pin.	Changes t_{SU} Changes t_H	Stratix II, Stratix II GX, Cyclone II, MAX II
Decrease input delay to output register	Decreases the propagation delay from the interior of the device to an output register in an I/O cell. Applied to input/bidirectional pin or register it feeds.	Decreases t_{PD}	Stratix, Stratix GX, APEX II, APEX 20KE, APEX 20KC
Increase delay to output enable pin	Increases the propagation delay through the tri-state output to the pin. The signal can either come from internal logic or the output enable register in an I/O cell. Applied to output/bidirectional pin or register feeding it.	Increases t_{CO}	Stratix, Stratix GX, APEX II, Mercury
Delay to output enable pin	Sets the propagation delay to an output enable pin from internal logic or the output enable register implemented in an I/O cell.	Changes t_{CO}	Stratix II, Stratix II GX

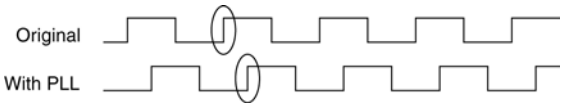
Table 8–5. Programmable Delays for Altera Devices (Part 2 of 2)

Programmable Delay	Description	I/O Timing Impact	Device Families
Increase delay to output pin	Increases the propagation delay to the output or bidirectional pin from internal logic or the output register in an I/O cell. Applied to output/bidirectional pin or register feeding it.	Increases t_{CO}	Stratix, Stratix GX, Cyclone, APEX II, APEX 20KE, APEX 20KC, Mercury
Delay from output register to output pin	Sets the propagation delay to the output or bidirectional pin from the output register implemented in an I/O cell. This option is off by default.	Changes t_{CO}	Stratix II, Cyclone II, Stratix II GX,
Increase input clock enable delay	Increases the propagation delay from the interior of the device to the clock enable input of an I/O input register.	N/A	Stratix, Stratix GX, APEX II, APEX 20KE, APEX 20KC
Input Delay from Dual Purpose Clock Pin to Fan-Out Destinations	Sets the propagation delay from a dual-purpose clock pin to its fan-out destinations that are routed on the global clock network. Applied to an input or bidirectional dual-purpose clock pin.	N/A	Cyclone II
Increase output clock enable delay	Increases the propagation delay from the interior of the device to the clock enable input of the I/O output register and output enable register.	N/A	Stratix, Stratix GX, APEX II, APEX 20KE, APEX 20KC
Increase output enable clock enable delay	Increases the propagation delay from the interior of the device to the clock enable input of an output enable register.	N/A	Stratix, Stratix GX
Increase t_{ZX} delay to output pin	Used for zero bus-turnaround (ZBT) by increasing the propagation delay of the falling edge of the output enable signal.	Increases t_{CO}	Stratix, Stratix GX, APEX II, Mercury

Use PLLs to Shift Clock Edges

Using a PLL typically improves I/O timing automatically. If the timing requirements are still not met, most devices allow the PLL output to be phase shifted in order to change the I/O timing. Shifting the clock backwards gives a better t_{CO} at the expense of t_{SU}, while shifting it forward gives a better t_{SU} at the expense of t_{CO} and t_H. Refer to Figure 8–10. This technique can be used only in devices that offer PLLs with the phase shift option.

Figure 8–10. Shift Clock Edges Forward to Improve t_{SU} at the Expense of t_{CO}



You can achieve the same type of effect in certain devices using the programmable delay called **Input Delay from Dual Purpose Clock Pin to Fan-Out Destinations**, described in Table 8–5.

Use Fast Regional Clocks in Stratix Devices & Regional Clocks in Stratix II Devices

Stratix EP1S25, EP1S20, and EP1S10 devices, and Stratix GX EP1SGX25 and EP1SGX10 devices, contain two fast regional clock networks, `FCLK[1..0]`, in each quadrant, fed by input pins that can connect to other fast regional clock networks.

In Stratix EP1S30, Stratix GX EP1SGX40, and larger devices in both families, there are two fast regional clock networks in each half-quadrant. Dedicated FCLK input pins feed these clock nets directly. Stratix fast regional clocks have less delay to I/O elements than regional or global clocks, and are used for high fan-out control signals.

Stratix II and Stratix II GX devices provide 32 regional clock networks. There are eight regional clock networks, `RCLK[7..0]` in each quadrant of the device that are driven by the dedicated input pins `CLK[15..0]`, by PLL outputs, or by internal logic. These regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. Placing clocks on these low-skew and low-delay clock nets provides better t_{CO} performance.

Change How Hold Times are Optimized for MAX II Devices

For MAX II devices, you can use the **Guarantee I/O paths have zero hold time at Fast Timing Corner** option to control how hold time is optimized by the Quartus II software. On the Assignments menu, click **Settings**. In the Category list, select **Fitter Settings**. Click **More Settings.** In the More Fitter Settings dialog box, set the option globally. Or, on the Assignments menu, click **Assignment Editor** to set this option for specific I/Os.

The option controls whether the Fitter uses timing-driven compilation to optimize a design to achieve a zero hold time for I/Os that feed globally clocked registers at the fast (best-case) timing corner, even in the absence of any user timing assignments. When this option is set to **On** (default),

the Fitter guarantees zero hold time (t_H) for I/Os feeding globally clocked registers at the fast timing corner, at the expense of possibly violating t_{SU} or t_{PD} timing constraints. When this option is set to **When tsu and tpd constraints permit**, the Fitter achieves zero hold time for I/Os feeding globally clocked registers at the fast timing corner only when t_{SU} or t_{PD} timing constraints are not violated. When this option is set to **Off**, designs are optimized to meet user timing assignments only.

By setting this option to **Off** or **When tsu and tpd constraints permit**, you improve t_{SU} at the expense of t_H.

f_{MAX} Timing Optimization Techniques (LUT-Based Devices)

The next stage of design optimization is to improve f_{MAX} timing. There are a number of options available if the performance requirements are not achieved after compilation.

Before optimizing your design, you should understand the structure of your design as well as the type of logic affected by each optimization. An optimization can decrease performance if the optimization does not benefit your logic structure.

Improving f_{MAX} Summary

The choice of options and settings to improve f_{MAX} depends on the failing paths in the design. To achieve the best results relative to your performance requirements, apply the following techniques, and compile the design after each:

1. Ensure that your timing assignments are complete. For details, refer to "Timing Requirement Settings" on page 8–6.
2. Ensure that you have reviewed any warning messages from your initial compilation, and checked for ignored timing assignments. Refer to "Design Analysis" on page 8–12 for details and fix any of these problems before proceeding with optimization.
3. Apply netlist synthesis optimization options and physical synthesis (page 8–41).
4. Modify the Fitter seed (page 8–48). You can omit this step if a large number of critical paths are failing, or if paths are failing by large amounts.

5. Apply the following synthesis options to optimize for speed:
   - Optimize synthesis for speed instead of area (page 8–45).
   - Flatten the hierarchy (page 8–45).
   - Set the synthesis effort to high (page 8–46).
   - Change state machine encoding (page 8–46).
   - Duplicate logic for fan-out control (page 8–47).
   - Prevent shift register inference.
   - Use other synthesis options available in your synthesis tool (page 8–48).
6. Make LogicLock assignments (page 8–50) to control placement.
7. Make design source code modifications to fix areas of the design that are still failing timing requirements by significant amounts (page 8–49).
8. Make location assignments, or perform manual placement by back-annotating the design (page 8–52).

You can use the DSE to automate the process of running several different compilations with different settings. For more information, refer to the *Design Space Explorer* chapter in volume 2 of the *Quartus II Handbook*.

If these techniques do not achieve performance requirements, additional design source code modifications may be required (page 8–49).

Synthesis Netlist Optimizations & Physical Synthesis Optimizations

The Quartus II software offers advanced netlist optimization options, including physical synthesis. Various netlist optimizations can help improve the performance of many designs regardless of the synthesis tool used. Netlist optimizations can be applied both during synthesis and during fitting.

The synthesis netlist optimizations occur during the synthesis stage of the Quartus II compilation. Operating either on the output from another EDA synthesis tool or as an intermediate step in Quartus II integrated synthesis, these optimizations make changes to the synthesis netlist to improve either area or speed, depending on your selected optimization technique.

The following synthesis netlist optimizations are available:

- WYSIWYG primitive resynthesis (for netlists from third-party EDA synthesis tools)
- Gate-level register retiming

On the Assignments menu, click **Settings**. In the **Category** list, expand **Analysis & Synthesis Settings** and select **Synthesis Netlist Optimizations** to view and modify the synthesis netlist optimization options.

If you use another EDA synthesis tool and want to determine if the Quartus II software can remap the circuit to improve performance, you can use the **Perform WYSIWYG Primitive Resynthesis** option. This option directs the Quartus II software to unmap the LEs in an atom netlist to logic gates, and then map the gates back to Altera-specific primitives. Using Altera-specific primitives enables the Fitter to remap the circuits using architecture-specific techniques.

To turn on the **Perform WYSIWYG Primitive Resynthesis** option, on the Assignments menu, click **Settings**. In the **Category** list, expand **Analysis & Synthesis Settings** and select **Synthesis Netlist Optimizations**. Turn on **Perform WYSIWYG primitive resynthesis (using optimization techniques specified in Analysis & Synthesis settings)**.

The Quartus II technology mapper optimizes the design for **Speed**, **Area**, or **Balanced**, according to the setting of the **Optimization Technique** option. To change this setting, on the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**, and choose **Speed** or **Balanced** under **Optimization Technique**.

The **Perform gate-level register retiming** option enables movement of registers across combinational logic to balance timing, allowing the Quartus II software to trade off the delay between timing-critical paths and non-critical paths. You can use this option with Quartus II Integrated synthesis, or if you are using a third-party EDA synthesis tool, you can use this option if you have turned on **Perform WYSIWYG primitive resynthesis (using optimization techniques specified in Analysis & Synthesis settings)**.

The physical synthesis optimizations occur during the Fitter stage of Quartus II compilation. Physical synthesis optimizations make placement-specific changes to the netlist that improve speed performance results for a specific Altera device.

The following physical synthesis optimizations are available:

- Physical synthesis for combinational logic
- Automatic asynchronous signal pipelining
- Physical synthesis for registers
  - Register duplication
  - Register retiming

On the Assignments menu, click **Settings**. In the **Category** list, select **Fitter Settings**, and specify the physical synthesis optimization options on the **Physical Synthesis Optimizations** page. You can also specify the **Physical synthesis effort**, which sets the level of physical synthesis optimization that you want the Quartus II software to perform.

The **Perform physical synthesis for combinational logic** option allows the Quartus II Fitter to resynthesize the combinational logic in a design to reduce delay along the critical path and improve design performance.

The **Perform automatic asynchronous signal pipelining** allows the Quartus II Fitter to insert pipeline stages for asynchronous clear and asynchronous load signals automatically during fitting to increase circuit performance. You can use this option if asynchronous control signal recovery and removal times do not meet your requirements. The option improves performance for designs in which asynchronous signals in very fast clock domains cannot be distributed across the chip quickly enough (because of long global network delays).

The **Perform automatic asynchronous signal pipelining** option adds registers to nets driving the asynchronous clear or asynchronous load ports of registers. This adds register delays (and latency) to the reset, adding the same number of register delays for each destination using the reset. Therefore the option should be used only when adding latency to reset signals does not violate any design requirements. This option also prevents the promotion of signals to use global routing resources.

The **Perform register duplication** fitter option allows the Quartus II Fitter to duplicate registers based on fitter placement information to improve design performance. The Fitter can also duplicate combinational logic when this option is enabled.

The **Perform register retiming** fitter option allows the Quartus II Fitter to move registers across combinational logic to balance timing. This option turns on algorithms similar to the Perform gate-level register retiming option. This option applies to registers and combinational logic that have already been placed into logic cells, and it compliments the synthesis gate-level option.

For more information and detailed descriptions of these netlist optimization options, refer to the *Netlist Optimizations & Physical Synthesis* chapter in volume 2 of the *Quartus II Handbook*.

Because performance results are design dependant, try these options in different combinations until you achieve the best results. Performance results are design dependent. Generally, turning on all the options gives the best results but significantly increases compilation time. Typical benchmark results with netlists from leading third-party synthesis tools and compiled with Quartus II software are shown in Table 8–6. These results were obtained for Stratix devices, using various designs and numbers of LEs. These results use the default Balanced setting for the Optimization Technique for WYSIWYG resynthesis. Changing the setting to Speed or Area can affect your results.

Table 8–6. Average Performance of Synthesis Netlist & Physical Synthesis Optimizations for Stratix Designs *Notes (1), (2)*

Optimization Method	f_{MAX} Gain (%)	Win Ratio (%) *(3)*	Winner's f_{MAX} Gain (%) *(4)*	Logic Area Change (%) *(5)*	Compile Time Change (×)
WYSIWYG primitive resynthesis	3	60	6	–8	1.0
Physical synthesis for combinational logic and registers					
Using physical synthesis Fast effort level	10	86	12	4	1.4
Using physical synthesis Normal effort level	15	86	16	4	2.2
Using physical synthesis Extra effort level	17	86	18	4	3.7
WYSIWYG primitive resynthesis as well as physical synthesis for combinational logic and registers					
Using physical synthesis Fast effort level	13	87	14	–5	1.4
Using physical synthesis Normal effort level	18	87	19	–5	2.2
Using physical synthesis Extra effort level	20	87	21	–5	3.7
All options on (WYSIWYG primitive resynthesis, gate level register retiming, and physical synthesis for combinational logic and registers)					
Using physical synthesis Extra effort level	20	82	21	–6	3.7

Notes to Table 8–6:

(1) The average f_{MAX} gain for Stratix II is 10% with a win ratio of 85%

(2) The average f_{MAX} gain for Cyclone II is 10% with a win ratio of 80%.

(3) Win ratio is the percentage of designs that showed better performance with the option on than without the option on.

(4) Winner's f_{MAX} gain refers to the average improvement for the designs that showed better performance with these settings (designs considered a win).

(5) Negative values mean reduced area. Positive values mean increased area.

Optimize Synthesis for Speed, not Area

The manner in which the design is synthesized has a large impact on design performance. Design performance varies depending on the way the design is coded, which synthesis tool is used, and which options are specified when synthesizing. Change your synthesis options if a large number of paths are failing, or specific paths are failing by a large amount and have many levels of logic.

Set your device and timing constraints in your synthesis tool. Synthesis tools are timing-driven and optimize to meet specified timing requirements. If you do not specify target frequency, some synthesis tools optimize for area.

Some synthesis tools offer an easy way to instruct the tool to focus on speed instead of area.

For Quartus II integrated synthesis, on the Assignments menu, click **Settings**. In the Category list, select **Analysis & Synthesis Settings**, and specify **Speed** as the **Optimization Technique** option. You can also specify this logic option for specific modules in your design with the Assignment Editor while leaving the default **Optimization Technique** setting at **Balanced** (for the best trade-off between area and speed for certain device families) or **Area** (if area is an important concern). You can also use the **Speed Optimization Technique for Clock Domains** option to specify that all combinational logic in or between the specified clock domain(s) is optimized for speed.

To achieve best performance with push-button compilation, follow the recommendations in the following sections for other synthesis settings. You can use DSE to experiment with different Quartus II synthesis options to optimize your design for the best performance.

For information about setting timing requirements and synthesis options in Quartus II integrated synthesis and third-party synthesis tools, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*, or refer to your synthesis software documentation.

Flatten the Hierarchy During Synthesis

Synthesis tools typically let you preserve hierarchical boundaries, which can be useful for verification or other purposes. However, the best optimization results generally occur when the synthesis tool optimizes across hierarchical boundaries because doing so often allows the synthesis tool to perform the most logic minimization, which can improve performance. Whenever possible, flatten your design hierarchy to achieve the best results. If you are using Quartus II integrated

synthesis, ensure that the **Preserve Hierarchical Boundary** option is turned off. If you are using Quartus II incremental compilation, you cannot flatten your design across design partitions. Incremental compilation always preserves the hierarchical boundaries between design partitions. Follow Altera's recommendations for design partitioning such as registering partition boundaries to reduce the effect of cross-boundary optimizations.

For more information about using incremental compilation and recommendations for design partitioning, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the Quartus II handbook. If you are using an incremental synthesis flow that requires separate hierarchy blocks, you can find additional recommendations for design partitioning in the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Handbook*.

Set the Synthesis Effort to High

Some synthesis tools offer varying synthesis effort levels to trade off compilation time with synthesis results. Set the synthesis effort to high to achieve best results when applicable.

Change State Machine Encoding

State machines can be encoded using various techniques. One-hot encoding, which uses one register for every state bit, usually provides the best performance. If your design contains state machines, changing the state machine encoding to one-hot can improve performance at the cost of area.

If your design does not manually encode the state bits, you can select the state machine encoding chosen in your synthesis tool. In Quartus II integrated synthesis, on the Assignments menu, click **Settings**. In the Category list, select **Analysis & Synthesis Settings**, and choose **One-Hot** for **State Machine Processing**. You also can specify this logic option for specific modules or state machines in your design with the Assignment Editor.

In some cases (especially in Stratix II devices), encoding styles other than the default offer better performance. Experiment with different encoding styles to see what effect the style has on your resource utilization and timing performance.

Duplicate Logic for Fan-Out Control

Duplicating logic or registers can help improve timing in cases where moving a register in a failing timing path to reduce routing delay creates other failing paths, or where there are timing problems due to the fan-out of the registers.

Many synthesis tools support options or attributes that specify the maximum fan-out of a register. When using Quartus II integrated synthesis, you can set the **Maximum Fan-Out** logic option in the Assignment Editor to control the number of destinations for a node so that the fan-out count does not exceed a specified value. You can also use the `maxfan` attribute in your HDL code. The software duplicates the node as needed to achieve the specified maximum fan-out.

You can manually duplicate registers in the Quartus II software regardless of the synthesis tool used. To duplicate a register, apply the **Manual Logic Duplication** option to the register with the Assignment Editor.

The manual logic duplication option also accepts wildcards. This is an easy and powerful duplication technique that you can use without editing your source code. You can use this technique, for example, to make a duplicate of a large fan-out node for all of its destinations in a certain design hierarchy, such as `hierarchy_A`. To apply such an assignment in the Assignment Editor, make an entry such as the one shown in Table 8–7:

Table 8–7. Duplicating Logic in the Assignment Editor

From	To	Assignment Name	Value
`My_high_fanout_node`	`*hierarchy_A*`	Manual Logic Duplication	`high_fanout_to_A`

For more information about the manual logic duplication option, refer to the Quartus II Help.

Prevent Shift Register Inference

In some cases, turning off the inference of shift registers increases performance. Doing so forces the software to use logic cells to implement the shift register instead of implementing the registers in memory blocks using the `altshift_taps` megafunction. If you implement shift registers in logic cells instead of memory, logic utilization is increased.

Use Other Synthesis Options Available in Your Synthesis Tool

With your synthesis tool, experiment with the following options if they are available:

- Turn on register balancing or retiming
- Turn on register pipelining
- Turn off resource sharing

These options may increase performance. They typically increase the resource utilization of your design.

Fitter Seed

The Fitter seed affects the initial placement configuration of the design. Changing the seed value changes the Fitter results because the fitting results change whenever there is a change in the initial conditions. Because each seed value results in a somewhat different fit, you can experiment with several different seeds to attempt to obtain better fitting results and timing performance. For example, the f_{MAX} variation between different seeds is typically about 3% for Stratix devices.

When there are changes in your design, there is some random variation in performance between compilations. This variation is inherent in placement and routing algorithms—there are too many possibilities to try them all and get the absolute best result, so the initial conditions change the compilation result.

Note that any design change that directly or indirectly affects the Fitter has the same type of random effect as changing the seed value. This includes any change in source files, Analysis & Synthesis settings, Fitter settings, or Timing Analyzer settings. The same effect can appear if you use a different computer processor type or different operating system because different systems can change the way floating point numbers are calculated in the Fitter.

If your design is finalized, you can compile your design with different seeds to obtain one optimal result. If any design or setting changes occur, they can make a previously optimal seed value no longer optimal.

If a design optimization slightly changes the f_{MAX} timing or number of failing paths, you can't always be certain that your change caused the improvement or degradation or whether it could be due to random effects in the Fitter. If your design is still changing, running a seed sweep (compiling your design with multiple seeds) determines whether the average result has improved after an optimization change and whether a setting that increases compilation time has benefits worth the increased

time (such as turning the physical synthesis effort to extra). The sweep also shows the amount of random variation you should expect for your design.

On the Assignments menu, select **Fitter Settings** to control the initial placement with the Seed. You can use the Design Space Explorer (DSE) to perform a seed sweep easily.

For more information about compiling with different seeds using the DSE script, refer to the *Design Space Explorer* chapter in volume 2 of the *Quartus II Handbook*.

Optimize Source Code

If the methods described in the preceding sections do not sufficiently improve timing of the design, modify your design files to achieve the desired results. Try restructuring the design to use pipelining or more efficient coding techniques. In many cases, optimizing the design's source code can have a very significant effect on your design performance. In fact, optimizing your source code is typically the most effective technique for improving your quality of results, and is often a better choice than using LogicLock or location assignments.

If the critical path in your design involves memory or DSP functions, check whether you have code blocks in your design that describe memory or functions that are not being inferred and placed in dedicated logic. You may be able to modify your source code to cause these functions to be placed into high-performance dedicated memory or resources in the target device.

Ensure that your state machines are recognized as state machine logic and optimized appropriately in your synthesis tool. State machines that are recognized are generally optimized better than if the synthesis tool treats them as generic logic. In the Quartus II software, you can check for the State Machine report under **Analysis & Synthesis** in the Compilation Report. This report provides details, including the state encoding for each state machine that was recognized during compilation. If your state machine is not being recognized, you may need to change your source code to enable it to be recognized.

For coding style guidelines including examples of HDL code for inferring memory, and functions and guidelines and sample HDL code for state machines, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

LogicLock Assignments

You can make LogicLock assignments for optimization based on nodes, design hierarchy, or critical paths. This method can be used if a large number of paths are failing, and recoding the design does not seem to be necessary. LogicLock assignments can help if routing delays form a large portion of your critical path delay, and placing logic closer together in the device improves the routing delay. This technique is most beneficial for devices with hierarchical routing structures such as the APEX 20K device family.

Improving fitting results, especially for larger devices such as Stratix and Stratix II, can be difficult. The LogicLock feature is intended to be used for performance preservation, therefore LogicLock assignments do not always improve the performance of the design. In many cases you cannot improve upon results from the Fitter by making location assignments.

If there are existing LogicLock assignments in your design, remove the assignments if your design methodology permits it. Recompile the design to see if the assignments are making the performance worse.

When making LogicLock assignments, it is important to consider how much flexibility to give the Fitter. LogicLock assignments provide more flexibility than hard location assignments. Assignments that are more flexible require higher Fitter effort, but reduce the chance of design over-constraint. The following types of LogicLock assignments are available, listed in order of decreasing flexibility:

- Soft LogicLock regions
- Auto size, floating location regions
- Fixed size, floating location regions
- Fixed size, locked location regions

To determine what to put into a LogicLock region, refer to the timing analysis results and the Timing Closure Floorplan. The register-to-register f_{MAX} paths in the Timing Analyzer section of the Compilation Report help you recognize patterns.

The following sections describe cases in which LogicLock regions help to optimize a design.

For more information about the LogicLock design methodology, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

Hierarchy Assignments

For a design with the hierarchy shown in Figure 8–11, which has failing paths in the timing analysis results similar to those shown in Table 8–8, `mod_A` is probably a problem module. In this case, a good strategy to fix the failing paths is to place the `mod_A` hierarchy block in a LogicLock region so that all the nodes are closer together in the floorplan.

Figure 8–11. Design Hierarchy

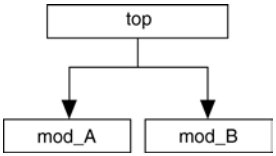


Table 8–8 shows the failing paths connecting two regions together within `mod_A` listed in the timing analysis report.

Table 8–8. Failing Paths in a Module Listed in Timing Analysis

From	To
|mod_A|reg1	|mod_A|reg9
|mod_A|reg3	|mod_A|reg5
|mod_A|reg4	|mod_A|reg6
|mod_A|reg7	|mod_A|reg10
|mod_A|reg0	|mod_A|reg2

Path Assignments

If you see a pattern such as the one shown in Figure 8–12 and Table 8–9, it often indicates paths with a common problem. In this case, a path-based assignment can be made from all **d_reg** registers to all **memaddr** registers. You can make a path-based assignment to place all source registers, destination registers, and the nodes between them in a LogicLock region with the wildcard characters "*" and "?".

You also can explicitly place the nodes of a critical path in a LogicLock region. However, using this method instead of path assignments can result in alternate paths between the source and destination registers becoming critical paths.

Figure 8–12. Failing Paths in Timing Analysis

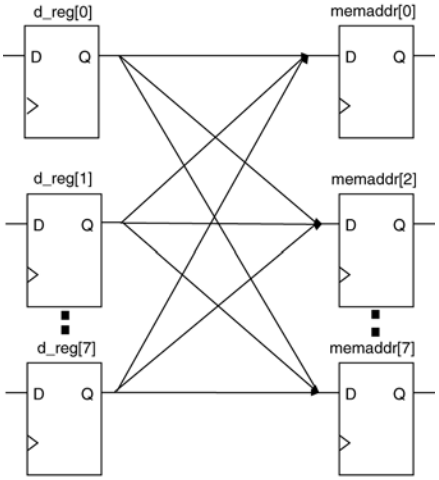


Table 8–9 shows the failing paths listed in the timing analysis report.

Table 8–9. Failing Paths in Timing Analysis

From	To
|d_reg[1]	|memaddr[5]
|d_reg[1]	|memaddr[6]
|d_reg[1]	|memaddr[7]
|d_reg[2]	|memaddr[0]
|d_reg[2]	|memaddr[1]

For more information about the LogicLock design methodology, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

Location Assignments & Back-Annotation

If a small number of paths are failing to meet their timing requirements, you can use hard location assignments to optimize placement. Location assignments are less flexible for the Quartus II Fitter than LogicLock assignments. In some cases, when you are very familiar with your design, you can enter location constraints in a way that produces better results.

Improving fitting results, especially for larger devices such as Stratix and Stratix II, can be difficult. Location assignments do not always improve the performance of the design. In many cases you cannot improve upon the results from the Fitter by making location assignments.

The following are commonly used location assignments, listed in order of decreasing flexibility:

- Custom regions
- Back-annotated LAB location assignments
- Back-annotated LE or ALM location assignments

Custom Regions

A custom region is a rectangular region containing user-assigned nodes, which are then constrained in the region's boundaries. If any portion of a block in the device floorplan, such as an M-RAM block, overlaps a custom region, it is considered to be entirely in that region.

Custom regions are hard location assignments that cannot be overridden and are very similar to fixed-size, locked-location LogicLock regions. Custom regions are commonly used when logic must be constrained to a specific portion of the device.

Back-Annotation & Manual Placement

Assigning the location of nodes in a design to the locations to which they were assigned during the last compilation is called back-annotation. When nodes are locked to their assigned locations in a back-annotated design, you can manually move specific nodes without affecting other back-annotated nodes. The process of manually moving and reassigning specific nodes is called manual placement.

Back-annotation is very restrictive to the compiler, so you should back-annotate only when the design has been finalized and no further changes are expected. Assignments can become invalid if the design is changed. Combinational nodes often change names when a design is resynthesized, even if they are unrelated to the logic that was changed.

Moving nodes manually can be very difficult for large devices. In many cases you cannot improve upon the Fitter's results.

Illegal or unroutable location constraints can cause "no fit" errors.

Before making location assignments, determine whether to back-annotate to lock down the assigned locations of all nodes in the design. When you are using a hierarchical design flow, you can lock down node locations in one LogicLock region only, while other node locations are left floating in a fixed LogicLock region. By implementing a hierarchical approach, you can use the LogicLock design methodology to reduce the dependence of logic blocks on other logic blocks in the device.

Consistent node names are required to perform back-annotation. If you use Quartus II integrated synthesis or any Quartus II optimizations such as the WYSIWYG primitive resynthesis netlist optimization or any physical synthesis optimizations, before you back-annotate, you must create an atom netlist to lock down the placement of any nodes, which creates consistent node names.

Physical synthesis optimizations are placement-specific as well as design-specific. Unless you back-annotate the design before recompilation, the physical synthesis results can differ. This happens because the atom netlist creates different placement results. By back-annotating the design, the design source and the atom netlist use the same placement when the design is recompiled. When you are using an atom netlist and you want to maintain the same placement results as a previous compilation, use LogicLock regions and back-annotate the placement of all nodes in the design. Not back-annotating the design can result in the design source and the atom netlist having different placement results and therefore different synthesis results.

For more information about using a block-based design approach and creating atom netlists for your design, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

When you back-annotate a design, you can choose whether to assign the nodes either to LABs (this is preferred because of increased flexibility) or LEs/ALMs. You also can choose to back-annotate routing to further restrict the Fitter and force a specific routing within the device.

Using back-annotated routing with physical synthesis optimizations can result in a routing failure.

For more information about back-annotating routing, refer to the Quartus II Help.

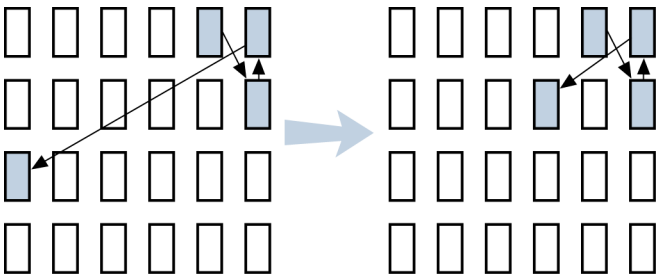
When performing manual placement at a detailed level, Altera suggests that you move LABs, not logic cells (LEs or ALMs). The Quartus II software places nodes that share the same control signals in appropriate

LABs. Successful placement and routing is more difficult when you move individual logic cells because if LEs with different control signals are put into the same LAB, the LAB may not have any unused control signals available and the design may not fit.

In general, when you are performing manual placement and routing, fix all I/O paths firsts because there are often fewer options available to meet I/O timing. After I/O timing has been met, focus on manually placing f_{MAX} paths. This strategy is consistent with the methodology outlined in this chapter.

The best way to meet performance is to move nodes closer together. For a critical path such as the one shown in Figure 8–13, moving the destination node closer to the other nodes reduces the delay and helps meet your timing requirements.

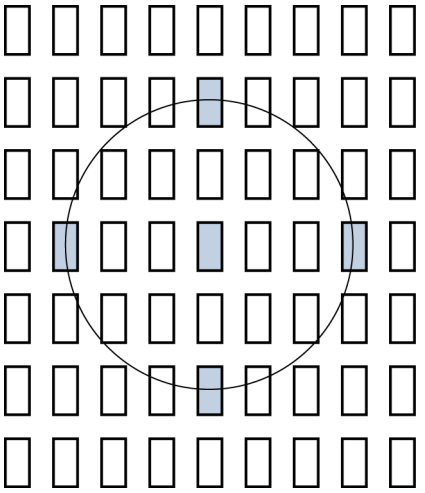
Figure 8–13. Reducing Delay of Critical Path



Optimizing Placement for Stratix II, Stratix, Stratix GX & Cyclone II Devices

In Stratix II, Stratix, Stratix GX, and Cyclone II device families, the row interconnect delay is slightly faster than the column interconnect delay. Therefore, when placing nodes, optimal placement is typically an ellipse around the source or destination node. In Figure 8–14, if the source is located in the center, any of the shaded LABs should give approximately the same delay.

Figure 8–14. Possible Optimal Placement Ellipse



In addition, you should avoid crossing any M-RAM memory blocks for node-to-node routing, because routing paths across M-RAM blocks requires using R24 or C16 routing lines.

To determine the actual delays to and from a resource, use the **Show Physical Timing Estimate** feature in the Timing Closure Floorplan.

For more information about using the Timing Closure Floorplan, refer to the *Timing Closure Floorplan* chapter in volume 2 of the *Quartus II Handbook*.

Optimizing Placement for Cyclone Devices

In Cyclone devices, the row and column interconnect delays are similar; therefore, when placing nodes, optimal placement is typically a circle around the source or destination node.

Try to avoid long routes across the device. Long routes require more than one routing line to cross the Cyclone device.

Optimizing Placement for Mercury, APEX II & APEX 20KE/C Devices

For the Mercury, APEX II, and APEX 20KE/C device families, the delay for paths reduce by placing the source and destination nodes in the same geographical resource location. The following list shows the device resources in order from fastest to slowest:

- LAB
- MegaLAB™ structure
- MegaLAB column
- Row

For example, if the nodes cannot be placed in the same MegaLAB structure to reduce the delay, then place them in the same MegaLAB column. For the actual delays to and from resources, use the **Show Physical Timing Estimate** feature in the Timing Closure Floorplan.

Resource Utilization Optimization Techniques (Macrocell-Based CPLDs)

The following recommendations help you take advantage of the macrocell-based architecture in the MAX 7000 and MAX 3000 device families to yield maximum speed, reliability, and device resource utilization while minimizing fitting difficulties.

After design analysis, the first stage of design optimization is to improve resource utilization. Complete this stage before proceeding to timing optimization. First, ensure that you have set the basic constraints described in "Initial Compilation" on page 8–5. If your design is not fitting into a specified device, use the techniques in this section to achieve a successful fit.

Use Dedicated Inputs for Global Control Signals

MAX 7000 and MAX 3000 devices have four dedicated inputs that can be used for global register control. Because the global register control signals can bypass the logic cell array and directly feed registers, product terms can be preserved for primary logic. Also, because each signal has a dedicated path into the LAB, global signals also can bypass logic and data path interconnect resources.

Because the dedicated input pins are designed for high fan-out control signals and provide low skew, you should always assign global signals (such as clock, clear, and output enable) to the dedicated input pins.

You can use logic-generated control signals for global control signals instead of dedicated inputs. However, the following list shows the disadvantages to using logic-generated control signals:

- More resources are required (logic cells, interconnect).
- More data skew is introduced.
- If the logic-generated control signals have high fan-out, the design may be more difficult to fit.

By default, the Quartus II software uses dedicated inputs for global control signals automatically. You can assign control signals to dedicated input pins in one of the following ways:

- In the Assignment Editor, choose one of the two following methods:
  - Assign pins to dedicated pin locations.
  - Assign a **Global Signal** setting to the pins.
- On the Assignments menu, click **Settings**. In the **Category** list, select **Register Control Signals** in the **Auto Global Options** section of the **Analysis & Synthesis Settings** page.
- Insert a `GLOBAL` primitive after the pins.
- If you have already assigned pins for the design in the MAX+PLUS® II software, on the Assignments menu, click **Import Assignments**.

Reserve Device Resources

Because pin and logic option assignments might be necessary for board layout and performance requirements, and because full utilization of the device resources can increase the difficulty of fitting the design, Altera recommends that you leave 10% of the device's logic cells and 5% of the I/O pins unused to accommodate future design modifications. Following the Altera-recommended device resource reservation guidelines for macrocell-based CPLDs increases the chance that the Quartus II software can fit the design during recompilation after changes or assignments have been made.

Pin Assignment Guidelines & Procedures

Sometimes user-specified pin assignments are necessary for board layout. This section discusses pin assignment guidelines and procedures.

To minimize fitting issues with pin assignments, follow these guidelines:

- Assign speed-critical control signals to dedicated inputs.
- Assign output enables to appropriate locations.
- Estimate fan-in to assign output pins to appropriate LAB.
- Assign output pins that require parallel expanders to macrocells numbered 4 to 16.

Altera recommends that you allow the Quartus II software to choose pin assignments automatically when possible.

Control Signal Pin Assignments

Assign speed-critical control signals to dedicated input pins. Every MAX 7000 and MAX 3000 device has four dedicated input pins (GCLK1, OE2/GCLK2, OE1, GCLRn). You can assign clocks to global clock dedicated inputs (GCLK1, OE2/GCLK2), clear to the global clear dedicated input (GCLRn), and speed-critical output enable to global OE dedicated inputs (OE1, OE2/GCLK2).

Output Enable Pin Assignments

Occasionally, because the total number of required output enable pins is more than the dedicated input pins, output enable signals must be assigned to I/O pins. Therefore, to minimize possible fitting errors, refer to the pin tables on the Literature page of Altera's website when assigning the output enable pins for MAX 7000 and MAX 3000 devices.

Estimate Fan-In when Assigning Output Pins

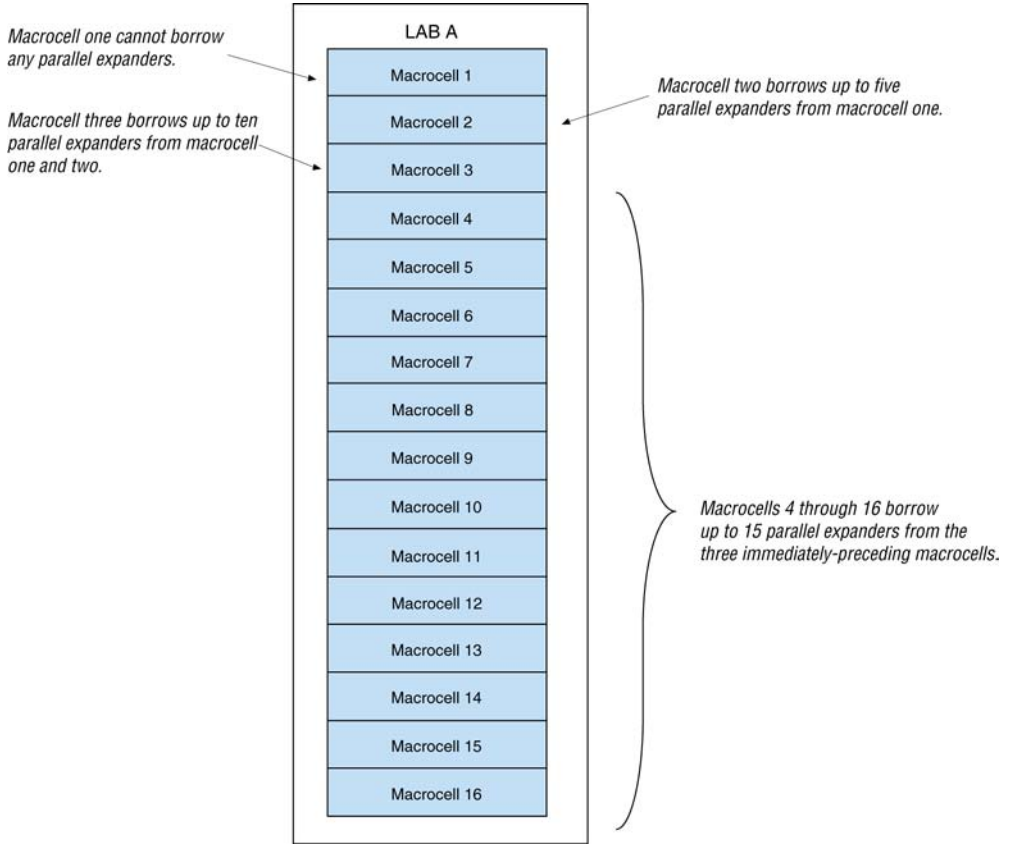
Macrocells with high fan-in can cause more placement problems for the Quartus II Fitter than those with low fan-in. The maximum fan-in per LAB should not exceed 36 in MAX 7000 and MAX 3000 devices. Therefore, estimate the fan-in of logic (such as an *x*-input AND gate) that feeds each output pin. If the total fan-in of logic that feeds each output pin in the same LAB exceeds 36, compilation may fail. To save resources and prevent compilation errors, avoid assigning pins that have high fan-in.

Outputs Using Parallel Expander Pin Assignments

Figure 8–15 illustrates how parallel expanders are used within a LAB. MAX 7000 and MAX 3000 devices contain chains that can lend or borrow parallel expanders. The Quartus II Fitter places macrocells in a location that allows them to lend and borrow parallel expanders appropriately.

As shown in Figure 8–15, only macrocells 2 through 16 can borrow parallel expanders. Therefore, assign output pins that may need parallel expanders to pins adjacent to macrocells 4 through 16. Altera recommends using macrocells 4 through 16 because they can borrow the largest number of parallel expanders.

Figure 8–15. LAB Macrocells & Parallel Expander Associations



Resolving Resource Utilization Problems

There are two common Quartus II compilation fitting issues that cause errors: excessive macrocell usage and lack of routing resources. Macrocell usage errors occur when the total number of macrocells in the design exceeds the available macrocells in the device. Routing errors occur when the available routing resources are insufficient to implement the design. Check the Message Window for the no-fit compilation results.

Messages in the Message window are also copied in the Report Files. Right-click on a message and select **Help** for more information.

Resolving Macrocell Usage Issues

Occasionally, a design requires more macrocell resources than are available in the selected device, which results in the design not fitting. The following list provides tips for resolving macrocell usage issues as well as tips to minimize the number of macrocells used.

- On the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**, and turn off **Auto Parallel Expanders**. If the design's clock frequency (f_{MAX}) is not an important design requirement, turn off parallel expanders for all or part of the project. The design usually requires more macrocells if parallel expanders are turned on.
- Change Optimization Technique from **Speed** to **Area**. Selecting **Area** instructs the compiler to give preference to area utilization rather than speed (f_{MAX}). On the Assignments menu, click **Settings**. In the **Category** list, change the **Optimization Technique** option in the **Analysis & Synthesis Settings** page.
- Use D-type flipflops instead of latches. Altera recommends that you always use D-type flipflops instead of latches in your design because D-type flipflops can reduce the macrocell fan-in, and thus reduce macrocell usage. The Quartus II software uses extra logic to implement latches in MAX 7000 and MAX 3000 designs because MAX 7000 and MAX 3000 macrocells contain D-type flipflops instead of latches.
- Use asynchronous clear and preset instead of synchronous clear and preset. To reduce the product term usage, use asynchronous clear and preset in your design whenever possible. Using other control signals such as synchronous clear produces macrocells and pins with higher fan-out.

After following the suggestions in this section, if your project still does not fit the targeted device, consider using a larger device. When upgrading to a different density, the vertical-package-migration feature of the MAX 7000 and MAX 3000 device families allows pin assignments to be maintained.

Resolving Routing Issues

Routing is another resource that can cause design fitting issues. For example, if the total fan-in into a LAB exceeds the maximum allowed, a no-fit error can occur during compilation. If your design does not fit the targeted device because of routing issues, consider the following suggestions.

- Use dedicated inputs/global signals for high fan-out signals. The dedicated inputs in MAX 7000 and MAX 3000 devices are designed for speed-critical and high fan-out signals. Always assign high fan-out signals to dedicated inputs/global signals.
- Change the **Optimization Technique** option from **Speed** to **Area**. This option may resolve routing resource and macrocell usage issues. Refer to the same suggestion in "Resolving Macrocell Usage Issues" on page 8–61.
- Reduce the fan-in per cell. If you are not limited by the number of macrocells used in the design, you can use the **Fan-in per cell (%)** option to reduce the fan-in per cell. The allowable values are 20–100%; the default value is 100%. Reducing the fan-in can reduce localized routing congestion but increase the macrocell count. You can set this logic option in the Assignment Editor or under More Settings in the **Analysis & Synthesis Settings** page of the **Settings** dialog box.
- On the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**, and turn off **Auto Parallel Expanders**. By turning off the parallel expanders, the Quartus II software has more fitting flexibility for each macrocell, allowing macrocells to be relocated. For example, each macrocell (previously grouped together in the same LAB) can be moved to a different LAB to reduce routing constraints.

- Insert logic cells. Inserting logic cells reduces fan-in and shared expanders used per macrocell, increasing routability. By default, the Quartus II software automatically inserts logic cells when necessary. Otherwise, **Auto Logic Cell** can be disabled as follows. On the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**. Under More Settings, turn off **Auto Logic Cell Insertion**. Refer to "Using LCELL Buffers to Reduce Required Resources" on page 8–63 for more information.
- Change pin assignments. If you are willing to discard your pin assignments, you can let the Quartus II Fitter ignore some or all the assignments.

If you prefer reassigning pins to increase routing efficiency, refer to "Pin Assignment Guidelines & Procedures" on page 8–58.

Using LCELL Buffers to Reduce Required Resources

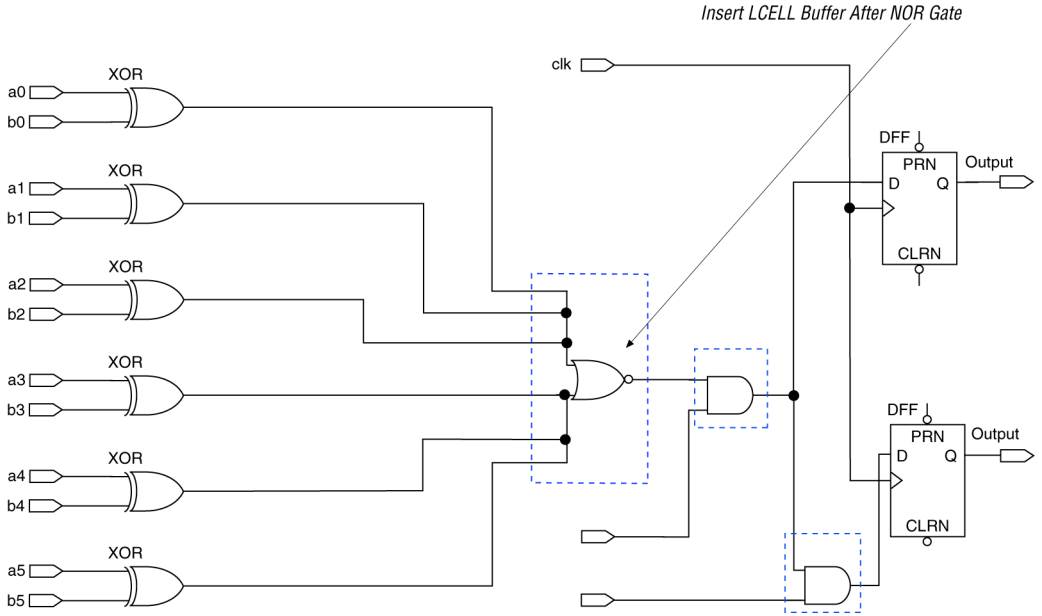
Complex logic, such as multilevel XOR gates, are often implemented with more than one macrocell. When this occurs, the Quartus II software automatically allocates shareable expanders—or additional macrocells (called synthesized logic cells)—to supplement the logic resources that are available in a single macrocell. You also can break down complex logic by inserting logic cells in the project to reduce the average fan-in and the total number of shareable expanders needed. Manually inserting logic cells can provide greater control over speed-critical paths.

Instead of using the Quartus II software's **Auto Logic Cell Insertion** option, you can manually insert logic cells. However, Altera recommends that you use the **Auto Logic Cell Insertion** option unless you know which part of the design is causing the congestion.

A good location to manually insert LCELL buffers is where a single complex logic expression feeds multiple destinations in your design. You can insert an LCELL buffer just after the complex expression; the Quartus II Fitter extracts this complex expression and places it in a separate logic cell. Rather than duplicate all the logic for each destination, the Quartus II software feeds the single output from the logic cell to all destinations.

To reduce fan-in and prevent no-fit compilations caused by routing resource issues, insert an LCELL buffer after a NOR gate, refer to Figure 8–16. The Figure 8–16 design was compiled for a MAX 7000AE device. Without the LCELL buffer, the design requires two macrocells, eight shareable expanders, and the average fan-in is 14.5 macrocells. However, with the LCELL buffer, the design requires three macrocells, eight shareable expanders, and the average fan-in is just 6.33 macrocells.

Figure 8–16. Reducing the Average Fan-In by Inserting LCELL Buffers



Timing Optimization Techniques (Macrocell-Based CPLDs)

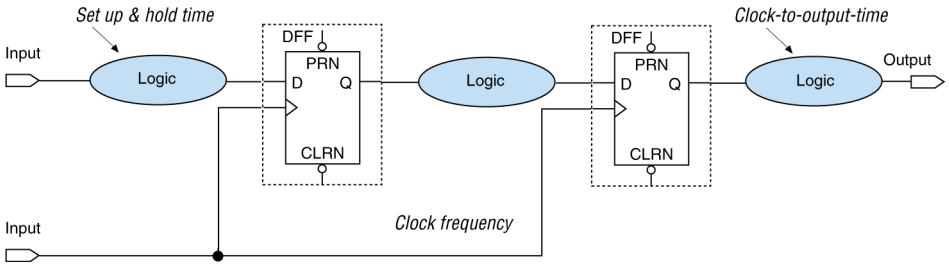
After resource optimization, design optimization focuses on timing. Ensure that you have made the appropriate assignments as described in "Initial Compilation" on page 8–5, and that the resource utilization is satisfactory before proceeding with timing optimization.

Maintaining system performance at or above certain timing requirements is an important goal of circuit designs. The following five timing parameters are primarily responsible for a design's performance:

- Setup time (t_{SU}), the propagation time for input data signals
- Hold time (t_H), the propagation time for input data signals
- Clock-to-output time (t_{CO}), the propagation time for output signals.
- Pin-to-pin delays (t_{PD}), the time required for a signal from an input pin to propagate through combinational logic and appear at an external output pin
- Maximum clock frequency (f_{MAX}), the internal register-to-register performance.

This section provides guidelines to improve the timing if the timing requirements are not met. Figure 8–17 shows the parts of the design that determine the t_{SU}, t_H, t_{CO}, t_{PD}, and f_{MAX} timing parameters.

Figure 8–17. Main Timing Parameters that Determine the System's Performance



Timing results for t_{SU}, t_H, t_{CO}, t_{PD}, and f_{MAX} are found in the Compilation Report, as discussed in "Design Analysis" on page 8–12.

When you are analyzing a design to improve performance, be sure to consider the two major contributors to long delay paths:

- Excessive levels of logic
- Excessive loading (high fan-out)

For MAX 7000 and MAX 3000 devices, when a signal drives more than one LAB, the programmable interconnect array (PIA) delay increases by 0.1 ns per additional LAB fan-out. Therefore, to minimize the added delay, concentrate the destination macrocells into fewer LABs, minimizing the number of LABs that are driven. The main cause of long delays in circuit design is excessive levels of logic.

Improving Setup Time

Sometimes the t_{SU} timing reported by the Quartus II Fitter does not meet your timing requirements. To improve the t_{SU} timing, refer to the following guidelines:

- Turn on the **Fast Input Register** option using the Assignment Editor. The **Fast Input Register** option allows input pins to directly drive macrocell registers via the fast-input path, thus minimizing the pin-to-register delay. This option is useful when a pin drives a D-type flipflop that does not have combinational logic between the pin and the register.
- Reduce the amount of logic between the input and the register. Excessive logic between the input pin and register causes more delays. To improve setup time, Altera recommends that you reduce the amount of logic between the input pin and the register whenever possible.
- Reduce fan-out. The delay from input pins to macrocell registers increases when the fan-out of the pins increases. To improve the setup time, minimize the fan-out.

Improving Clock-to-Output Time

To improve a design's clock-to-output time, minimize the register-to-output-pin delay. To improve the t_{CO} timing, refer to the following guidelines.

- Use the global clock. In addition to minimizing the delay from a register to an output pin, minimizing the delay from the clock pin to the register also can improve t_{CO} timing. Always use the global clock for low-skew and speed-critical signals.
- Reduce the amount of logic between the register and output pin. Excessive logic between the register and the output pin causes more delay. Always minimize the amount of logic between the register and output pin for faster clock-to-output time.

Table 8–10 shows the timing results for an EPM7064AETC100-4 device when a combination of the **Fast Input Register** option, global clock, and minimal logic is used. When the **Fast Input Register** option is turned on, the t_{SU} timing is improved (t_{SU} decreases from 1.6 ns to 1.3 ns and from 2.8 ns to 2.5 ns). The t_{CO} timing is improved when the global clock is used for low-skew and speed-critical signals (t_{CO} decreases from 4.3 ns to 3.1 ns). However, if there is additional logic used between the input pin and the register or the register and the output pin, the t_{SU} and t_{CO} delays increase.

Table 8–10. EPM7064AETC100-4 Device Timing Results

Number of Registers	t_{SU} (ns)	t_H (ns)	t_{CO} (ns)	Global Clock Used	Fast Input Register Option	D Input Location	Q Output Location	Additional Logic Between:	
								D Input Location & Register	Register & Q Output Location
1	1.3	1.2	4.3	No	On	LAB A	LAB A	No	No
1	1.6	0.3	4.3	No	Off	LAB A	LAB A	No	No
1	2.5	0	3.1	Yes	On	LAB A	LAB A	No	No
1	2.8	0	3.1	Yes	Off	LAB A	LAB A	No	No
1	3.6	0	3.1	Yes	Off	LAB A	LAB A	Yes	No
1	2.8	0	7.0	Yes	Off	LAB D	LAB A	No	Yes
16 with the same D and clock inputs	2.8	0	All 6.2	Yes	Off	LAB D	LAB A, B	No	No
32 with the same D and clock inputs	2.8	0	All 6.4	Yes	Off	LAB C	LAB A, B, C	No	No

Improving Propagation Delay (t_{PD})

Achieving fast propagation delay (t_{PD}) timing is required in many system designs. However, if there are long delay paths through complex logic, achieving fast propagation delays can be difficult. To improve your design's t_{PD}, Altera recommends that you follow the guidelines discussed in this section.

- On the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**, and turn on **Auto Parallel Expanders**. Turning on the parallel expanders for individual nodes or sub-designs can increase the performance of complex logic functions. However, if the project's pin or logic cell assignments use parallel expanders placed physically together with macrocells (which can reduce routability), parallel expanders can cause the Quartus II Fitter to have difficulties finding and optimizing a fit. Additionally, the number of macrocells required to implement the design increases and results in a no-fit error during compilation if the device resources are limited. For more information about turning the **Auto Parallel Expanders** option on, refer to "Resolving Macrocell Usage Issues" on page 8–61.
- Set the Optimization Technique to **Speed**. By default, the Quartus II software sets the **Optimization Technique** option to **Speed** for MAX 7000 and MAX 3000 devices. Reset the **Optimization Technique** option to **Speed** only if you previously set it to **Area**. On the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**, and turn on **Speed** under **Optimization Technique**.

Improving Maximum Frequency (f_{MAX})

Maintaining the system clock at or above a certain frequency is a major goal in circuit design. For example, if you have a fully synchronous system that must run at 100 MHz, the longest delay path from the output of any register to the inputs of the registers it feeds must be less than 10 ns. Maintaining the system clock speed can be difficult if there are long delay paths through complex logic. Altera recommends that you follow the following guidelines to improve your design's clock speed (f_{MAX}).

- On the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings** and turn on **Auto Parallel Expanders**. Turning on the parallel expanders for individual nodes or subdesigns can increase the performance of complex logic functions. However, if the project's pin or logic cell assignments use parallel expanders placed physically together with macrocells (which can reduce routability), parallel expanders can cause the Quartus II Compiler to have difficulties finding and optimizing a fit. Additionally, the amount of macrocells required to implement the design also increases and can result in a no-fit error during compilation if the device's resources are limited. For more information about turning the **Auto Parallel Expanders** option on, refer to "Resolving Macrocell Usage Issues" on page 8–61.
- Use global signals or dedicated inputs. Altera MAX 7000 and MAX 3000 devices have dedicated inputs that provide low skew and high speed for high fan-out signals. Minimize the number of control signals in the design and use the dedicated inputs to implement them.
- Set the **Optimization Technique** to **Speed**. By default, the Quartus II software sets the **Optimization Technique** option to **Speed** for MAX 7000 and MAX 3000 devices. Reset the **Optimization Technique** option to **Speed** only if you have previously set it to **Area**. You can reset the **Optimization Technique** option. In the **Category** list, choose **Analysis & Synthesis Settings**, and turn on **Speed** under Optimization Technique.
- Pipeline the design. Pipelining, which increases clock frequency (f_{MAX}), refers to dividing large blocks of combinational logic by inserting registers. For more information about pipelining, refer to "Optimizing Source Code—Pipelining for Complex Register Logic" on page 8–69.

Optimizing Source Code—Pipelining for Complex Register Logic

If the methods described in the preceding sections do not sufficiently improve your results, modify the design at the source to achieve the desired results. Using a pipelining technique can consume device resources, but it also lowers the propagation delay between registers, allowing you to maintain high system clock speed.

The benefits of pipelining can be demonstrated with a 4-to-16 pipelined decoder that decodes 4-bit numbers. The decoder is based on five 2-to-4 pipelined decoders with outputs that are registered using D-type flipflops. Figure 8–18 shows one of the 2-to-4 pipelined decoders. The function 2TO4DEC is the 2-to-4 decoder that feeds all four decoded outputs (out1, out2, out3, and out4) to the D-type flipflops in 4REG.

Figure 8–18. A 2- to 4-Pipelined Decoder

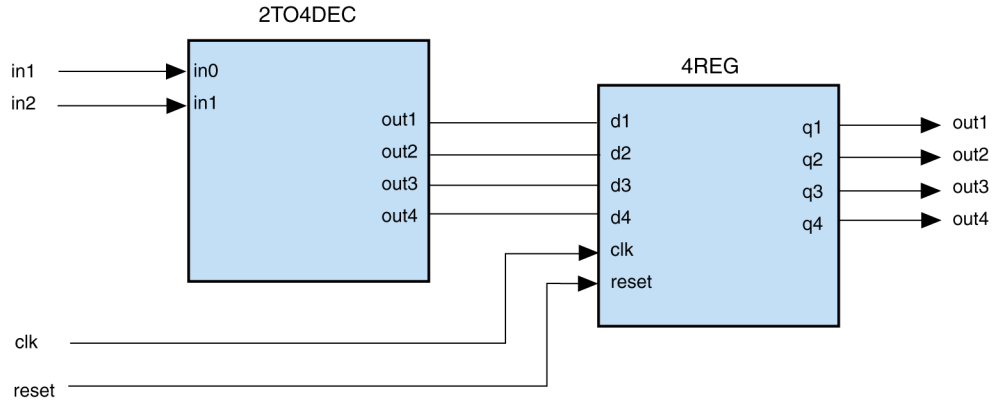
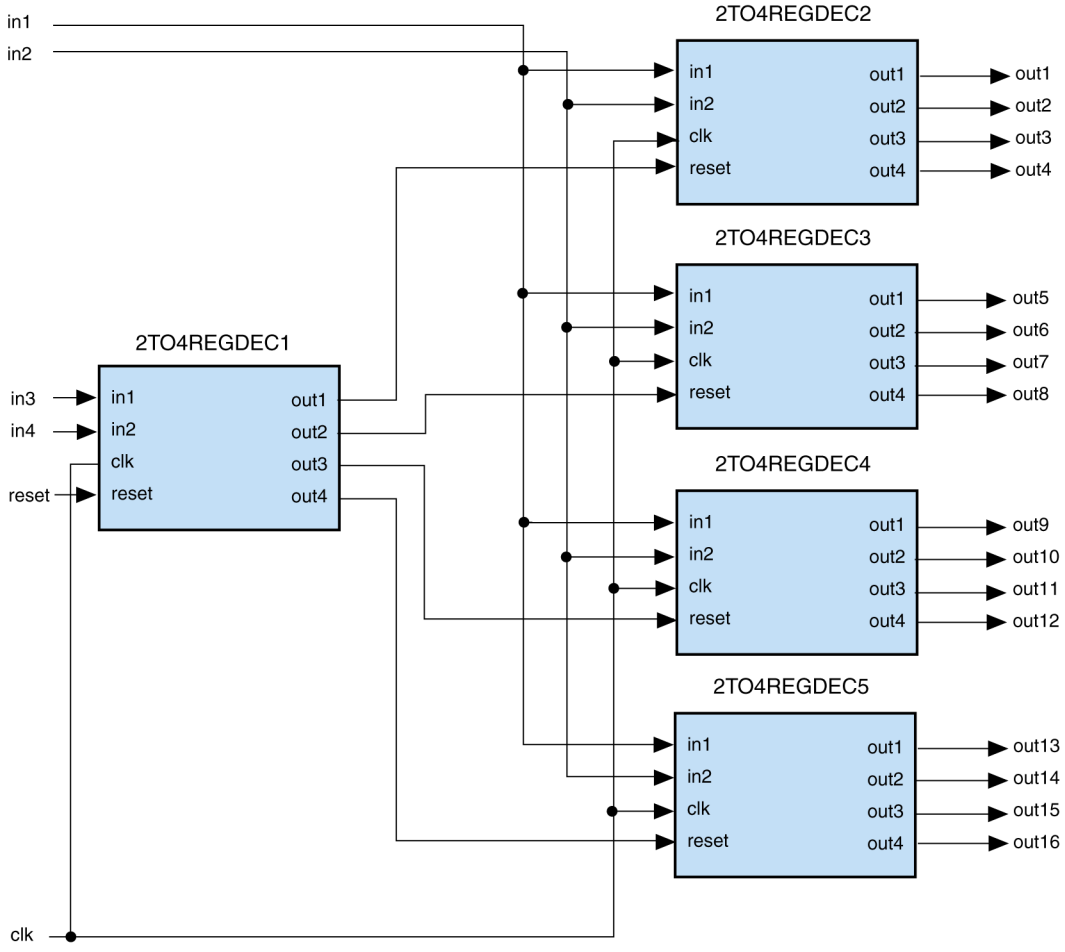


Figure 8–19 shows five 2-to-4 decoders (2TO4REGDEC) that are combined to form a 4-to-16 pipelined decoder. The first decoder (2TO4REGDEC1) decodes the two most significant bits (MSB) (in3 and in4) of the 4-to-16 decoder. The decoded output from the 2TO4REGDEC1 decoder enables only one of the rest of the 2-to-4 decoders (2TO4REGDEC2, 2TO4REGDEC3, 2TO4REGDEC4, or 2TO4REGDEC5). The inputs in1 and in2 are decoded by the enabled 2-to-4 decoder. Because the time to generate the decoded output increases with the size of the decoder, pipelining the design reduces the time consumed to generate the decoded output, thus improving the maximum frequency. In Figure 8–19, the MSBs (in3 and in4) are decoded in the first clock cycle, while the other bits (in1 and in2) are decoded in the following clock cycle.

Figure 8–19. Five 2-to-4 Pipelined Decoders Combined to Form a 4-to-16 Pipelined Decoder



Compilation-Time Optimization Techniques

If optimizing the compilation time of your design is important, use the techniques in this section. Be aware that reducing compilation time using some of these techniques can reduce the overall quality of results.

Incremental Compilation

You can speed up design iteration time by an average of 60% when making changes to the design and reach design timing closure more efficiently with the incremental compilation feature. Using incremental compilation allows you to organize your design into logical and physical partitions for design synthesis and fitting. Design iterations can be made dramatically faster by recompiling only a particular design partition and merging results with previous compilation results of other partitions. You can also use optimization techniques such as physical synthesis for specific design partitions while leaving other modules untouched to preserve performance.

When making changes to the design, use the incremental synthesis feature (part of incremental compilation) to save synthesis time. Incremental synthesis allows you to set design partitions to ensure that only those sections of a design that have been updated are resynthesized when the design is compiled, which reduces synthesis time and run-time memory usage.

If you are using a third-party synthesis tool, you can create separate atom netlist files for parts of your design that you already have synthesized and optimized so that you update only the parts of the design that change.

Regardless of your synthesis tool, you can use full incremental compilation along with LogicLock regions to preserve your placement and routing results for unchanged partitions while working on other partitions. This ability provides the most reduction in compilation time and run-time memory usage because neither synthesis nor fitting must be performed for unchanged partitions in the design.

For information about the full incremental compilation flow in the Quartus II software, refer to the *Quartus II Incremental Compilation* chapter in volume 1 of the *Quartus II Handbook*. For information about using the Quartus II incremental synthesis feature alone, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*. For information about creating multiple netlist files in third-party tools for use with incremental compilation, refer to the appropriate chapter in the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

Reduce Synthesis Time & Synthesis Netlist Optimization Time

You can reduce synthesis time by reducing your use of netlist optimizations and by using incremental synthesis. For more ideas on reducing synthesis time in third-party EDA synthesis tools, refer to your tool's documentation.

Synthesis Netlist Optimizations

You can use Quartus II integrated synthesis to synthesize and optimize HDL designs, and you can use synthesis netlist optimizations to optimize netlists that were synthesized by third-party EDA software. Using these netlist optimizations can cause the Analysis & Synthesis module to take much longer to run. Look at the Analysis & Synthesis messages to find out how much time these optimizations take. The compilation time spent in Analysis & Synthesis is typically small compared to the compilation time spent in the Fitter.

If your design meets your performance requirements without synthesis netlist optimizations, turn off the optimizations to save time. If you need to turn on synthesis netlist optimizations to meet performance, you can optimize parts of your design hierarchy separately to reduce the overall time spent in analysis and synthesis.

Check Early Timing Estimation Before Fitting

The Quartus II software allows you to get an estimate of your timing results after synthesis, before the design is fully processed by the Fitter. In cases where you want a quick estimate of your design results before proceeding with further design or synthesis tasks, this feature can save you significant compilation time. For more information, refer to "Early Timing Estimation" on page 8–11.

In the Processing menu, point to **Start,** and click **Start Early Timing Estimate** after you perform analysis and synthesis in the Quartus II software.

Reduce Placement Time

The time needed to place a design depends on two factors: the number of ways the logic in the design can be placed in the device and the settings that control how hard the placer works to find a good placement. You can reduce the placement time in two ways:

- Change the settings for the placement algorithm.
- Use incremental compilation to preserve the placement for parts of the design.

Sometimes there is a trade-off between placement time and routing time. Routing time can increase if the placer does not run long enough to find a good placement. When you reduce placement time, make sure that it does not increase routing time and negate the overall time reduction.

Fitter Effort Setting

On the Assignments menu, click **Settings**. In the **Category** list, select **Fitter Settings**, and use the **Fitter effort** setting to shorten runtime by changing the effort level to **Auto Fit** or **Fast Fit.**

Placement Effort Multiplier Settings

You can control the amount of time the Fitter spends in placement by reducing one aspect of placement effort with the **Placement Effort Multiplier** option. On the Assignments menu, click **Settings**. Select Fitter Settings, and click **More Settings**. Under **Existing Option Settings**, select **Placement Effort Multiplier**. The default is `1.0`. Legal values must be greater than 0 and can be non-integer values. Numbers between 0 and 1 can reduce fitting time, but also can reduce placement quality and design performance. Numbers higher than 1 increase placement time and placement quality, but may reduce routing time for designs with routing congestion. For example, a value of 4 increases placement time by approximately 2 to 4 times, but may increase quality.

Physical Synthesis Effort Settings

You can use the physical synthesis options to optimize your post-synthesis netlist and improve your timing performance. These options, which affect placement, can significantly increase compilation time. Refer to Table 8–6 on page 8–44 for detailed results.

If your design meets your performance requirements without physical synthesis options, turn them off to save time. You also can use the **Physical synthesis effort** setting on the **Physical Synthesis Optimizations** page under **Fitter Settings** in the **Category** list to reduce the amount of extra compilation time that these optimizations use. The **Fast** setting directs the Quartus II software to use a lower level of physical synthesis optimization that, compared to the normal level, can cause a smaller increase in compilation time. However, the lower level of optimization can result in a smaller increase in design performance.

Limit to One Fitting Attempt

This option causes the software to quit after one fitting attempt option, instead of looping through placement and routing with increased effort. Preventing multiple fitter loops controls compilation time. The option increases the fitting effort on this one fitting attempt so it increases the compilation time as compared to a compilation that requires only one fitting attempt.

If your design is not routable, using the **Limit to one fitting attempt option** results in a fitting error due to routing. The option might also be useful in this case, because finishing fitting more quickly allows you to analyze the results more quickly and optimize your design appropriately to improve routability.

From the Assignments menu, select **Settings**. On the Fitter Settings page, turn on **Limit to one fitting attempt**.

Preserving Placement, Incremental Compilation, & LogicLock Regions

Preserving information about previous placements can make future placements take less time. The incremental compilation provides an easy-to-use methodology for preserving placement results. For more information, refer to "Incremental Compilation" on page 8–72 and the references listed in the section.

Reduce Routing Time

The time needed to route a design depends on three factors: the device architecture, the placement of the design in the device, and the connectivity between different parts of the design. Typically the routing time is not a significant amount of the compilation time. If your design takes a long time to route, perform one or more of the following actions:

- Check for routing congestion
- Let the placer run longer to find a more routable placement
- Use incremental compilation to preserve routing information for parts of your design

Identify Routing Congestion in the Timing Closure Floorplan

To identify areas of congested routing in your design, open the Timing Closure Floorplan. On the Assignments menu, click **Timing Closure Floorplan,** and turn on **Show Routing Congestion**. This feature is available only when you choose the **Field View** on the View menu. Routing resource usage above 90% indicates routing congestion. You can change the connections in your design to reduce routing congestion. If the area with routing congestion is in a LogicLock region or between LogicLock regions, change or remove the LogicLock regions and recompile the design. If the routing time remains the same, then the time is a characteristic of the design and the placement. If the routing time decreases, consider changing the size, location, or contents of LogicLock regions to reduce congestion and decrease routing time.

Router Effort Multiplier Setting

To control how quickly the router finds a fit, you can change the value of the **Router Effort Multiplier** option by performing the following steps:

1. On the Assignments menu, click **Settings**.
2. In the Category list, select **Fitter Settings**, and click **More Settings**.
3. Select the **Router Effort Multiplier** option from the drop-down menu.

The default value is `1.0`. Legal values must be greater than `0`. Numbers closer to `0` (for example, `0.1`) can reduce router run-time, but usually reduce router quality slightly, which also may reduce design performance.

Preserve Routing Incremental Compilation & LogicLock Regions

Preserving information about the previous routing results for part of the design can make future routing efforts take less time. The use of LogicLock regions with incremental compilation provides an easy-to-use methodology that preserves placement and routing results. For more information, refer to "Incremental Compilation" on page 8–72 and the references listed in the section.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The *Quartus II Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

You can specify many of the options described in this section either in an instance, or at a global level, or both.

Use the following Tcl command to make a global assignment:

```
set_global_assignment -name <QSF variable name> <value>
```

Use the following Tcl command to make an instance assignment:

```
set_instance_assignment -name <QSF variable name> <value> \
-to <instance name>
```

Initial Compilation Settings

The Quartus Settings File variable name is used in the Tcl assignment to make the setting along with the appropriate value. The Type column indicates whether the setting is supported as a global setting, an instance setting, or both.

This chapter refers to timing settings and analysis in the Quartus II Classic Timing Analyzer. For equivalent settings and analysis in the TimeQuest Timing Analyzer, refer to the *TimeQuest Timing Analyzer* or the *Switching to the TimeQuest Timing Analyzer* chapters in volume 3 of the *Quartus II Handbook*.

Table 8–11 lists the Quartus Settings File variable name and applicable values for the settings discussed in "Initial Compilation" on page 8–5.

Table 8–11. Initial Compilation Settings

Setting Name	Quartus Settings File Variable Name	Values	Type
Device Setting	DEVICE	<*device part number*>	Global
Use Smart Compilation	SPEED_DISK_USAGE_TRADEOFF	SMART, NORMAL	Global
Optimize IOC Register Placement For Timing	OPTIMIZE_IOC_REGISTER_PLACEMENT_FOR_TIMING	ON, OFF	Global
Optimize Hold Timing	OPTIMIZE_HOLD_TIMING	OFF, "IO PATHS AND MINIMUM TPD PATHS", "ALL PATHS"	Global
Fitter Effort	FITTER_EFFORT	"STANDARD FIT", "FAST FIT", "AUTO FIT"	Global

Resource Utilization Optimization Techniques (LUT-Based Devices)

Table 8–12 lists the Quartus Settings File variable name and applicable values for the settings discussed in "Resource Utilization Optimization Techniques (LUT-Based Devices)" on page 8–20. The QSF variable name is used in the Tcl assignment to make the setting along with the appropriate value. The Type column indicates whether the setting is supported as a global setting, an instance setting, or both.

Table 8–12. Resource Utilization Optimization Settings (Part 1 of 2)

Setting Name	QSF Variable Name	Values	Type
Auto Packed Registers *(1)*	AUTO_PACKED_REGISTERS_<*device family name*>	OFF, NORMAL, "MINIMIZE AREA", "MINIMIZE AREA WITH CHAINS", AUTO	Global, Instance
Perform WYSIWYG Primitive Resynthesis	ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP	ON, OFF	Global, Instance
Optimization Technique	<*device family name*>_OPTIMIZATION_TECHNIQUE	AREA, SPEED, BALANCED	Global, Instance
Speed Optimization Technique for Clock Domains	SYNTH_CRITICAL_CLOCK	ON, OFF	Instance

Table 8–12. Resource Utilization Optimization Settings (Part 2 of 2)

Setting Name	QSF Variable Name	Values	Type
State Machine Encoding	STATE_MACHINE_PROCESSING	AUTO, "ONE-HOT", "MINIMAL BITS", "USER-ENCODE"	Global, Instance
Preserve Hierarchy	PRESERVE_HIERARCHICAL_BOUNDARY	OFF, RELAXED, FIRM,	Instance
Auto RAM Replacement	AUTO_RAM_RECOGNITION	ON, OFF	Global, Instance
Auto ROM Replacement	AUTO_ROM_RECOGNITION	ON,OFF	Global, Instance
Auto Shift Register Replacement	AUTO_SHIFT_REGISTER_RECOGNITION	ON, OFF	Global, Instance
Auto Block Replacement	AUTO_DSP_RECOGNITION	ON, OFF	Global, Instance

Notes to Table 8–12:
(1) Allowable values for this setting depend on the device family that is selected.

I/O Timing Optimization Techniques (LUT-Based Devices)

Table 8–13 lists the QSF variable name and applicable values for the settings discussed in "I/O Timing Optimization Techniques (LUT-Based Devices)" on page 8–33. The QSF variable name is used in the Tcl assignment to make the setting along with the appropriate value. The **Type** column indicates whether the setting is supported as a global setting, an instance setting, or both.

Table 8–13. I/O Timing Optimization Settings

Setting Name	Quartus Settings File Variable Name	Values	Type
Optimize IOC Register Placement For Timing	OPTIMIZE_IOC_REGISTER_PLACEMENT_FOR_TIMING	ON, OFF	Global
Fast Input Register	FAST_INPUT_REGISTER	ON, OFF	Instance
Fast Output Register	FAST_OUTPUT_REGISTER	ON, OFF	Instance
Fast Output Enable Register	FAST_OUTPUT_ENABLE_REGISTER	ON, OFF	Instance

f_{MAX} Timing Optimization Techniques (LUT-Based Devices)

Table 8–14 lists the QSF variable name and applicable values for the settings discussed in "f_{MAX} Timing Optimization Techniques (LUT-Based Devices)" on page 8–40. The QSF variable name is used in the Tcl assignment to make the setting along with the appropriate value. The **Type** column indicates whether the setting is supported as a global setting, an instance setting, or both.

Table 8–14. F_{MAX} Timing Optimization Settings

Setting Name	Quartus Settings File Variable Name	Values	Type
Perform WYSIWYG Primitive Resynthesis	ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP	ON, OFF	Global, Instance
Perform Gate Level Register Retiming	ADV_NETLIST_OPT_SYNTH_GATE_RETIME	ON, OFF	Global
Allow Register Retiming to trade off T_{SU}/T_{CO} with f_{MAX}	ADV_NETLIST_OPT_RETIME_CORE_AND_IO	ON, OFF	Global
Perform Physical Synthesis for Combinational Logic	PHYSICAL_SYNTHESIS_COMBO_LOGIC	ON, OFF	Global
Perform Register Duplication	PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION	ON, OFF	Global
Perform Register Retiming	PHYSICAL_SYNTHESIS_REGISTER_RETIMING	ON, OFF	Global
Physical Synthesis Effort	PHYSICAL_SYNTHESIS_EFFORT	NORMAL, EXTRA, FAST	Global
Seed	SEED	*<integer>*	Global
Maximum Fan-Out	MAX_FANOUT	*<integer>*	Instance
Manual Logic Duplication	DUPLICATE_ATOM	*<node name>*	Instance

Duplicate Logic for Fan-Out Control

The manual logic duplication option accepts wildcards. This is an easy and powerful duplication technique that you can use without editing your source code. You can use this technique, for example, to make a duplicate of a large fan-out node for all of its destinations in a certain design hierarchy, such as `hierarchy_A`. To make such an assignment with Tcl, use a command similar to Example 8–1.

Example 8–1. Duplication Technique

```
set_instance_assignment -name DUPLICATE_ATOM \
  high_fanout_to_A -from high_fanout_node \
  -to *hierarchy_A*
```

Conclusion

Today's complex designs have complex requirements. Methodologies for fitting your design and for achieving timing closure are fundamental to optimal performance in today's designs. Using the Quartus II design optimization methodology closes timing quickly on complex designs, reduces iterations by providing more intelligent and better linkage between analysis and assignment tools, and balances multiple design constraints including multiple clocks, routing resources, and area constraints.

The Quartus II software provides many features to achieve optimal results. Follow the techniques presented in this chapter to efficiently optimize a design for area or timing performance, or to reduce compilation time.

9. Power Optimization

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Introduction

The Quartus® II software introduces power-driven compilation to fully optimize device power consumption. Power-driven compilation focuses on reducing your design's total power consumption using power-driven synthesis and power-driven place-and-route. This chapter describes the power-driven compilation feature and flow in detail, as well as low power design techniques that can further reduce power consumption in your design. The techniques primarily target Stratix® II, Stratix II GX, Cyclone™ II, and HardCopy® II devices. These devices are based on a 1.2-V core voltage and 90 nm process technology. These devices are the first 90 nm FPGAs that utilize a low-k dielectric material that dramatically reduces dynamic power and improves performance. Stratix II devices include new, more efficient, logic structures called adaptive logic modules (ALMs) that obtain maximum performance while minimizing power consumption. Cyclone II devices offer the optimal blend of high performance and low power in a low-cost FPGA.

Altera® provides the Quartus II PowerPlay Power Analyzer to aid you during the design process by delivering fast and accurate estimations of power consumption. You can minimize power consumption, while taking advantage of the industry's leading FPGA performance, by using the tools and techniques described in this chapter.

For more information on the PowerPlay Power Analyzer, refer to the *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

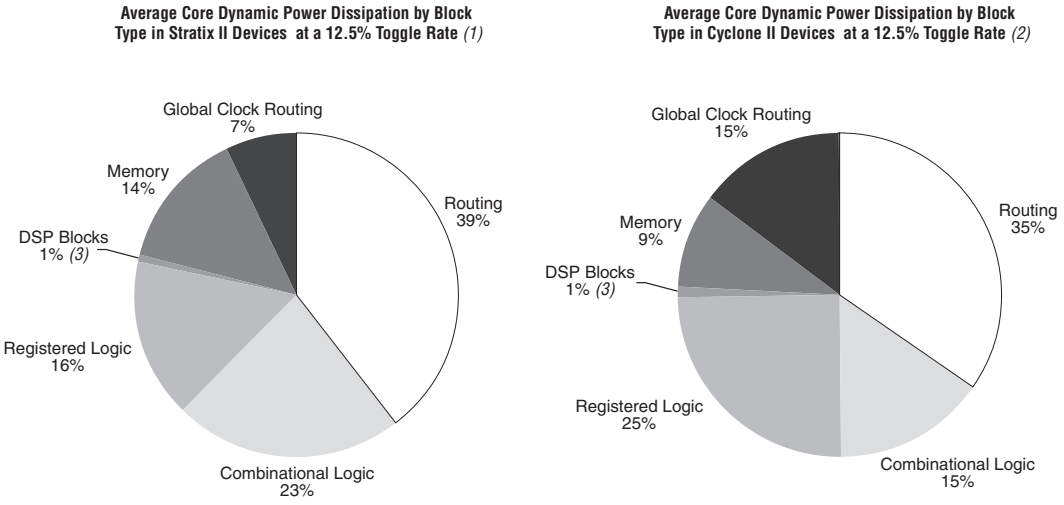
Total FPGA power consumption is comprised of I/O power, core static power, and core dynamic power. This chapter focuses on design optimization options and techniques that help reduce core dynamic power and I/O power.

Power Dissipation

This section describes the sources of power dissipation in Stratix II and Cyclone II devices. You can refine techniques that reduce power consumption in your design by understanding the sources of power dissipation.

Figure 9–1 shows the power dissipation of Stratix II and Cyclone II devices in different designs. All designs were analyzed at a fixed clock rate of 200 MHz and exhibited varied logic resource utilization across available resources.

Figure 9–1. Average Core Dynamic Power Dissipation



Notes to Figure 9–1:
(1) 112 different designs were used to obtain these results.
(2) 93 different designs were used to obtain these results.
(3) In designs using DSP blocks, DSPs consumed 5% of core dynamic power.

As shown in Figure 9–1, a significant amount of the total power is dissipated in routing for both Stratix II and Cyclone II devices, with the remaining power dissipated in logic, clock, and RAM blocks.

In Stratix II and Cyclone II devices, a series of column and row interconnect wires of varying lengths provide signal interconnections between logic array blocks (LABs), memory block structures, and digital signal processing (DSP) blocks or multiplier blocks. These interconnects dissipate the largest component of device power.

FPGA combinational logic is another source of power consumption. The basic building block of logic in Stratix II devices is the ALM, and in Cyclone II devices, it is the logic element (LE).

For more information on ALMs and LEs in Stratix II and Cyclone II devices, refer to the *Stratix II Device Handbook* and the *Cyclone II Device Handbook*, respectively.

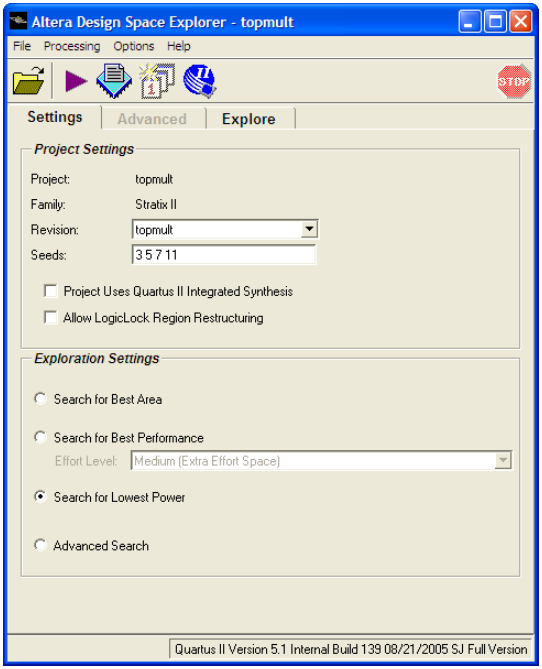
Memory and clock resources are other major consumers of power in FPGAs. Stratix II devices feature the TriMatrix™ memory architecture. TriMatrix memory includes 512-bit M512 blocks, 4-Kbit M4K blocks, and 512-Kbit M-RAM blocks, which are each configurable to support many features. Cyclone II devices have 4-Kbit M4K memory blocks.

Design Space Explorer

The Design Space Explorer (DSE) is a simple, easy-to-use, design optimization utility that is included in the Quartus II software. The DSE explores and reports optimal Quartus II software options for your design, targeting either power optimization, design performance, or area utilization improvements. You can use the DSE to implement the techniques described in this chapter.

Figure 9–2 shows the DSE user interface. The **Settings** tab is divided into **Project Settings** and **Exploration Settings**.

Figure 9–2. Design Space Explorer User Interface



The **Search for Lowest Power** option under **Exploration Settings** uses a predefined exploration space that targets overall design power improvements. This setting focuses on applying different options that specifically reduce total design thermal power. You can also set the **Optimization Goal** option for your design using the **Advanced** tab in the DSE window. You can select your design optimization goal, such as optimize for power, from the list of available settings in the **Optimization Goal** list. The DSE then uses the selection from the **Optimization Goal** list, along with the **Search for Lowest Power** selection, to determine the best compilation results.

By default, the Quartus II PowerPlay Power Analyzer is run for every exploration performed by the DSE when the **Search for Lowest Power** option is selected. This helps you debug your design and determine trade-offs between power requirements and performance optimization.

For more information on the DSE, refer to the *Design Space Explorer* chapter in volume 2 of the *Quartus II Handbook*.

Power-Driven Compilation

The standard Quartus II compilation flow consists of Analysis and Synthesis, Fitter, Assembler, and Timing Analysis. Power-driven compilation takes place at the analysis and synthesis and fitter levels. Power-driven compilation settings are divided in the **PowerPlay power optimization** list on the **Analysis & Synthesis Settings** page, and **PowerPlay power optimization** on the **Fitter Setting** page. The following section describes these power optimization options at the analysis and synthesis and fitter levels.

Power-Driven Synthesis

Synthesis netlist optimization occurs during the synthesis stage of the compilation flow. The optimization technique makes changes to the synthesis netlist to optimize your design according to the selection of area, speed, or power optimization. This section describes power optimization techniques at the synthesis level.

The **Analysis & Synthesis Settings** page allows you to specify logic synthesis options. The **PowerPlay power optimization** option is available for Stratix II, Stratix, Stratix GX, Cyclone II, Cyclone, and MAX® II devices (Figure 9–3).

To perform power optimization at the synthesis level in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Analysis & Synthesis**. The **Analysis & Synthesis** page is shown.
3. In the **PowerPlay power optimization** list, select your preferred setting. This option determines how aggressively Analysis and Synthesis optimizes the design for power.

Figure 9–3. Analysis & Synthesis Settings Page

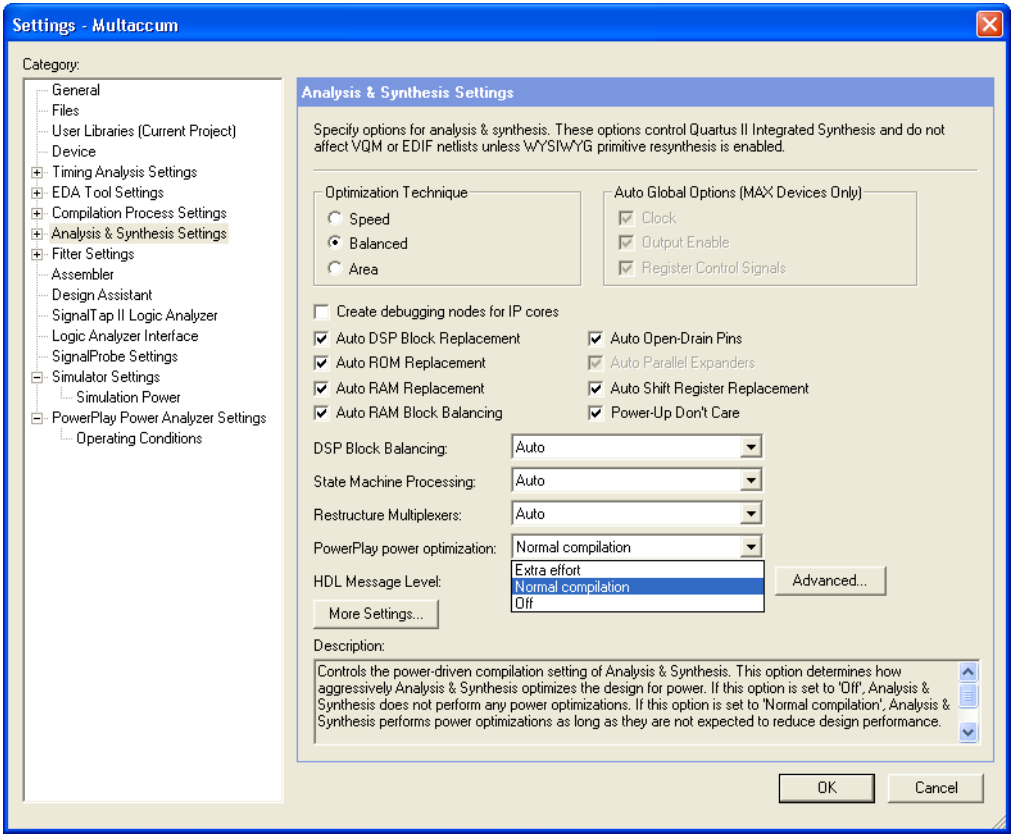


Table 9–1 shows the settings in the **PowerPlay power optimization** list. You can apply these settings on a project or entity level.

Table 9–1. Optimize Power during synthesis options

Settings	Description
Off	No power optimizations are performed
Normal compilation (Default)	Enables power optimizations as long as they are not expected to reduce design performance
Extra effort	Enables you to perform additional power optimizations which can reduce design performance

The **Normal compilation** setting is turned on by default. This setting performs memory optimization and power-aware logic mapping during synthesis.

Memory blocks can represent a large fraction of total design dynamic power as described in "Reducing Memory Power Consumption" on page 9–22. Minimizing the number of memory blocks accessed during each clock cycle can significantly reduce memory power. Memory optimization involves effective movement of user-defined read/write enable signals to associated read-and-write clock enable signals for all memory types (Figure 9–4).

Figure 9–4. Memory Transformation

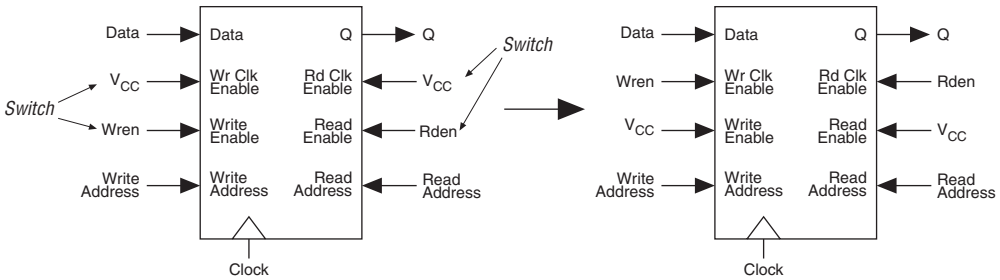


Figure 9–4 shows a default implementation of a simple dual-port memory block in which write-clock enable and read-clock enable signals are connected to V_{CC}, making both read-and-write memory ports active during each clock cycle. Memory transformation effectively moves the read-enable and write-enable signals to the respective read-clock enable and write-clock enable signals. By using this technique, memory ports are shut down when they are not accessed. This significantly reduces your design's memory power consumption. For more information on clock enable signals, refer to "Reducing Memory Power Consumption" on page 9–22.

The other type of power optimization that takes place with the **Normal compilation** setting is power-aware logic mapping. The power-aware logic mapping reduces power by rearranging the logic during synthesis to eliminate nets with high toggle rates.

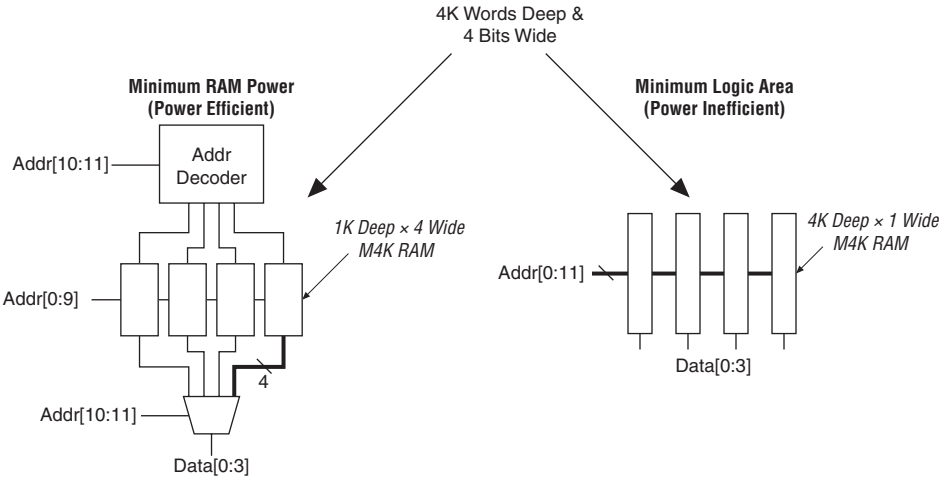
The **Extra effort** setting performs the functions of the **Normal compilation** setting and other memory optimizations to further reduce memory power by shutting down memory blocks that are not accessed. This level of memory optimization may require extra logic which can reduce design performance.

The **Extra effort** setting also performs power-aware memory balancing. Power-aware memory balancing automatically chooses the best memory configuration for your memory implementation, and provides optimal power saving by determining the number of memory blocks, decoder, and multiplexer circuits needed. If you have not previously specified target-embedded memory blocks for your design's memory functions, the power-aware balancer automatically selects it during memory implementation.

Figure 9–5 shows an example of a 4K × 4 (4K deep and 4 bit wide) memory implementation in two different configurations using M4K memory blocks. The minimum logic area implementation uses M4K blocks configured as 4K × 1. This implementation is the default in the Quartus II software, because it has the minimum logic area (0 logic cells) and the highest speed. However, all four M4K blocks are active on each memory access in this implementation, which increases RAM power. The minimum RAM power implementation is created by selecting **Extra effort** in the **PowerPlay power optimization** list. This implementation automatically uses four M4K blocks configured as 1K × 4 for optimal power saving. An address decoder is implemented by the `altsyncram` megafunction to select which of the four M4K blocks should be activated on a given cycle, based on the state of the top two user address bits. The `altsyncram` megafunction automatically implements a multiplexer to feed the downstream logic by choosing the appropriate M4K output. This implementation reduces RAM power, because only one M4K block is active on any cycle, but it requires extra logic cells, costing logic area and potentially impacting design performance.

There is a trade-off between power saved by accessing fewer memories and power consumed by the extra decoder and multiplexor logic. The Quartus II software automatically balances the power savings against the costs to choose the lowest power configuration for each logical RAM.

Figure 9–5. 4K × 4 Memory Implementation Using Multiple M4K Blocks



Memory optimization options can also be controlled by the `Low_Power_Mode` parameter in the **Default Parameters** page of the **Settings** dialog box. The settings for this parameter are **None**, **Auto**, and **ALL**. **None** corresponds to the **Off** setting in the **PowerPlay power optimization** list. **Auto** corresponds to the **Normal compilation** setting and **ALL** corresponds to the **Extra effort** setting respectively. You can apply PowerPlay power optimization either on a compiler basis or on individual entities. The `Low_Power_Mode` parameter always takes precedence over the Optimize Power for Synthesis option for power optimization on memory.

You can also set the `MAXIMUM_DEPTH` parameter manually to configure the memory for low power optimization. This technique is the same as the power-aware memory balancer, but it is manual rather than automatic like the **Extra effort** setting in the **PowerPlay power optimization** list. You can set the `MAXIMUM_DEPTH` parameter for memory modules manually in the megafunction instantiation or in the MegaWizard® Plug-In Manager for power optimization as described in "Reducing Memory Power Consumption" on page 9–22. The `MAXIMUM_DEPTH` parameter always takes precedence over the Optimize Power for Synthesis options for power optimization on memory optimization.

Power-Driven Synthesis Experiment for Stratix II Devices

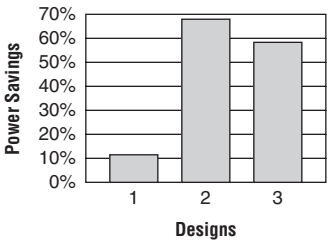
In this experiment for Stratix II devices, three designs are compiled with the Quartus II software using **Normal compilation** and **Extra effort** settings in the **PowerPlay power optimization** list. The default setting for Fitter is **Normal compilation**.

Table 9–2. Resources Used in the Power-Driven Synthesis Experiment for Stratix II Devices

Design Name	Settings	ALUT	Register	Memory Bits
Design 1	Normal compilation	8,941	9,150	293,856
	Extra effort	8,954	9,151	293,856
Design 2	Normal compilation	28,169	12,148	1,009,920
	Extra effort	28,817	12,297	1,009,920
Design 3	Normal compilation	5,376	2,809	153,864
	Extra effort	5,559	2,813	153,864

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–6 shows that the power-driven synthesis reduces memory power consumption by as much as 68% in Stratix II devices.

Figure 9–6. Memory Blocks Power Saving Using the Power-Driven Synthesis for Stratix II Devices



Power-Driven Fitter

The **Fitter Settings** page enables you to specify options for fitting (Figure 9–7). The **PowerPlay power optimization** option is available for Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II devices.

To perform power optimization at the fitter level, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Fitter Settings**. The **Fitter Settings** page is shown.
3. In the **PowerPlay power optimization** list, select your preferred setting. This option determines how aggressively the Fitter optimizes the design for power.

Figure 9–7. Fitter Settings Window

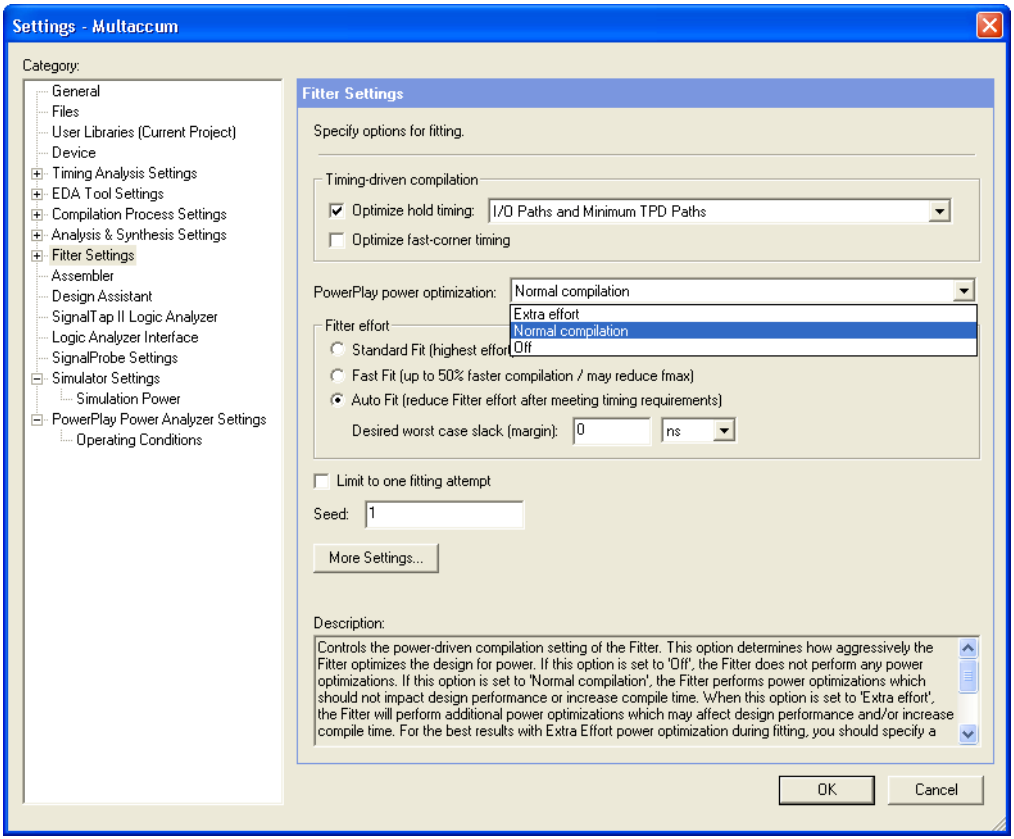


Table 9–3 lists the settings in the **PowerPlay power optimization** list. These settings can only be applied on a project-wide basis. The **Extra effort** setting for the Fitter requires extensive effort to optimize the design for power and can increase the compilation time.

Table 9–3. Power-Driven Fitter Option

Settings	Description
Off	No power optimizations are performed
Normal compilation (Default)	Enables power optimizations as long as they are not expected to reduce design performance
Extra effort	Enables you to perform additional power optimizations that can reduce design performance

The **Normal compilation** setting is selected by default and performs DSP optimization by creating power-efficient DSP block configurations for your DSP functions. This level of power optimization will not have any affect on the fitting or timing results or the compile time.

The **Extra effort** setting performs the functions of the **Normal compilation** setting and other place-and-route optimizations during fitting to fully optimize the design for power. The Fitter applies an extra effort to minimize power even after timing requirements have been met by effectively moving the logic closer during placement to localize high-toggling nets, and using routes with low capacitance. However, this effort can increase the compilation time.

The **Extra effort** setting uses a Signal Activity File (**.saf**) or Verilog Value Change Dump File (**.vcd**) that guides the Fitter to fully optimize the design for power based on the signal activity of the design. The best power optimization during fitting results from using the most accurate signal activity information. Signal activities from full post-fit netlist (timing) simulation provide the highest accuracy because all node activities reflect the actual design behavior, provided that supplied input vectors are representative of typical design operation. If you do not have a Signal Activity File (from simulation or other source), then the Quartus II software uses assignments, clock assignments, and vectorless estimation values (PowerPlay Power Analyzer Tool settings) estimate the signal activities. This information is used to optimize your design for power during fitting.

Only the **Extra effort** setting in the **PowerPlay power optimization** list for the Fitter option uses the signal activities (from Value Change Dump File or SAF) during fitting. The settings made in the **PowerPlay Power Analyzer Settings** page in the **Settings** dialog box are used to calculate the signal activity of your design.

For more information on Signal Activity Files and Verilog Value Change Dump Files, and how to create them, refer to the *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Power-Driven Fitter Experiment for Stratix II Devices

In this experiment for Stratix II devices, three designs are compiled with the Quartus II software using the **Normal compilation** and **Extra effort** settings in the Fitter for the PowerPlay power optimization list. The default setting for Analysis and Synthesis is **Normal compilation**.

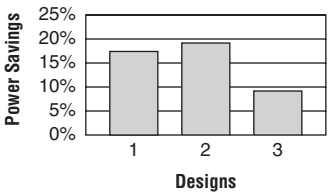
Table 9–4 shows resources used in the power-driven fitter experiment.

Table 9–4. Designs Used in the Power-Driven Fitter Experiment for Stratix II Devices

Design Name	ALUTs (Normal Compilation)	ALUTs (Extra Effort)
Design 1	21,435	21,363
Design 2	19,035	18,970
Design 3	5,335	5,328

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–8 shows that the power-driven fitter technique reduces power consumption by as much as 19% in Stratix II devices.

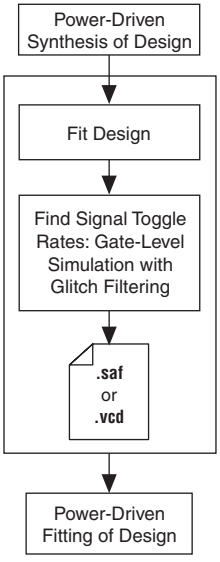
Figure 9–8. Power Savings Using the Power-Driven Fitter for Stratix II Devices



Recommended Flow for Power-Driven Compilation

Figure 9–9 shows the recommended design flow to fully optimize your design for power during compilation. This flow utilizes the power-driven synthesis and power-driven fitter options. On average, you can reduce core dynamic power by 16% with the extra effort synthesis and extra effort fitting settings, as compared to off settings in both synthesis and fitter options for power-driven compilation.

Figure 9–9. Recommended Flow for Power-Driven Compilation



Area-Driven Synthesis

The use of area optimization rather than timing or delay optimization during synthesis saves power because fewer logic blocks are used. Using less logic usually means less switching activity.

Area-Driven Synthesis Experiment for Stratix II Devices

In this experiment for Stratix II devices, five designs are compiled with the Quartus II software in two ways. First, the designs are compiled optimizing for area. The same designs are then compiled optimizing for speed. The power optimization settings for synthesis and fitting are set to **Off**.

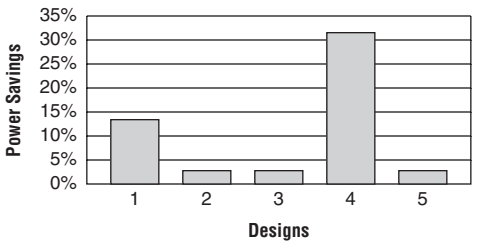
Table 9–5 shows ALUT usage in the area-driven synthesis experiment.

Table 9–5. Designs Used in the Area-Driven Synthesis Experiment for Stratix II Devices

Design Name	ALUTs (Area Mapping)	ALUTs (Speed Mapping)
Design 1	5,682	8,553
Design 2	16,986	17,783
Design 3	36,554	36,312
Design 4	4,717	5,820
Design 5	15,947	15,978

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–10 shows that the area-driven technique reduces power consumption by as much as 31% in Stratix II devices.

Figure 9–10. Power Savings Using Area-Driven Synthesis for Stratix II Devices



Area-Driven Synthesis Experiment for Cyclone II Devices

In this experiment for Cyclone II devices, five designs are compiled with the Quartus II software in two ways. First, the designs are compiled optimizing for area. The same designs are then compiled optimizing for speed.

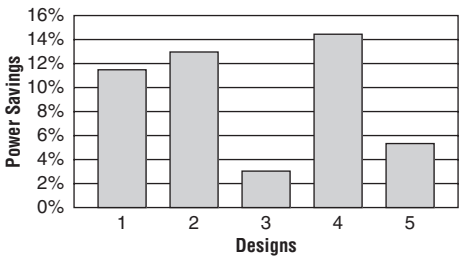
Table 9–6 shows LE usage in the area-driven synthesis experiment.

Table 9–6. Designs Used in the Area-Driven Synthesis Experiment for Cyclone II Device

Design Name	LEs (Area Mapping)	LEs (Speed Mapping)
Design 1	13,020	16,429
Design 2	13,317	13,636
Design 3	5,384	5,690
Design 4	33,640	40,008
Design 5	21,409	22,988

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–11 shows that the area-driven technique reduces power consumption by as much as 15% in Cyclone II devices.

Figure 9–11. Power Savings Using Area-Driven Synthesis for Cyclone II Devices

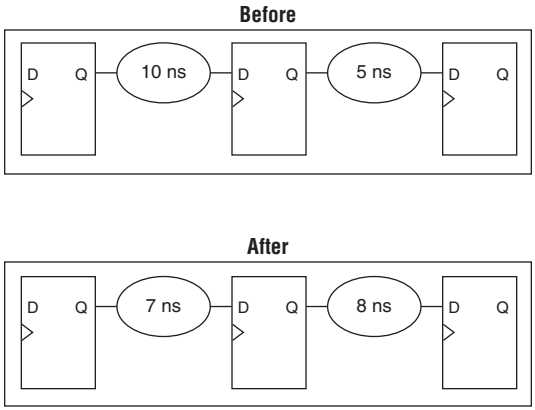


Gate-Level Register Retiming

You can also use gate-level register retiming to reduce circuit switching activity. Retiming shuffles registers across combinational blocks without changing design functionality. The **Perform gate-level register retiming** option in the Quartus II software enables the movement of registers across combinational logic to balance timing, allowing the software to trade off the delay between timing critical and non-critical timing paths.

Retiming uses fewer registers than pipelining. Figure 9–12 shows an example of gate-level register retiming, where the 10 ns critical delay is reduced by moving the register relative to the combinational logic, resulting in the reduction of data depth and switching activity.

Figure 9–12. Gate-Level Register Retiming



Gate-level register retiming makes changes at the gate level. If you are using an atom netlist from a third-party synthesis tool, you must also select the **Perform WYSIWYG primitive resynthesis** option to undo the atom primitives to gates mapping (so that register retiming can be performed), and then to remap gates to Altera primitives. When using the Quartus II integrated synthesis, retiming occurs during synthesis before the design is mapped to Altera primitives.

For more information on register retiming, refer to the *Netlist Optimizations & Physical Synthesis* chapter in volume 2 of the *Quartus II Handbook*.

Gate-Level Register Retiming Experiment for Stratix II Devices

In this experiment for Stratix II devices, three designs are compiled with the Quartus II software in two ways. First, a netlist from a third-party synthesis tool is compiled. Then, the same netlist is compiled after selecting the **Perform WYSIWYG primitive resynthesis** and **Perform gate-level register retiming** options.

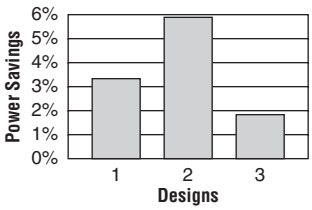
Table 9–7 shows resource usage results.

Table 9–7. Resources Used in the Gate-Level Register Retiming Experiment for Stratix II Devices

Design Name	WYSIWYG & Register Retiming	ALUTs	Registers	DSP Blocks	Memory
Design 1	No	2,051	691	0	16
	Yes	1,882	731	0	16
Design 2	No	123,909	40,070	0	0
	Yes	95,593	39,816	0	0
Design 3	No	6,354	6,019	64	3,584
	Yes	7,496	5,970	64	3,584

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–13 shows that the combination of WYSIWYG remapping and gate-level register retiming reduces power consumption by nearly 6% in Stratix II devices.

Figure 9–13. Power Savings Using Retiming for Stratix II Devices



Gate-Level Register Retiming Experiment for Cyclone II Devices

In this experiment for Cyclone II devices, three designs are compiled with the Quartus II software in two ways. First, a netlist from a third-party synthesis tool is compiled. Then, the same netlist is compiled by selecting the **Perform WYSIWYG primitive resynthesis** and **Perform gate-level register retiming** options.

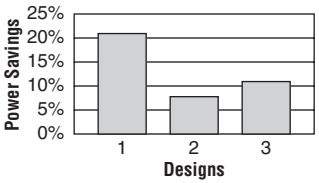
Table 9–8 shows resource usage results.

Table 9–8. Resources Used in the Gate-Level Register Retiming Experiment for Cyclone II Devices

Design Name	WYSIWYG & Register Retiming	LEs	Registers	Multiplier Blocks	Memory
Design 1	No	385	137	0	0
	Yes	278	143	0	0
Design 2	No	14,758	1,683	0	0
	Yes	13,079	1,683	0	0
Design 3	No	31,727	29,097	96	3,120
	Yes	27,038	24,272	96	3,120

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–14 shows that the combination of WYSIWYG remapping and gate-level register retiming reduces power consumption by as much as 21% in Cyclone II devices.

Figure 9–14. Power Savings Using Retiming for Cyclone II Devices



Design Guidelines

Several low-power design techniques can reduce power consumption when applied during FPGA design implementation. This section provides detailed design techniques for Stratix II and Cyclone II devices that affect overall design power. The results of these techniques may be different from design to design.

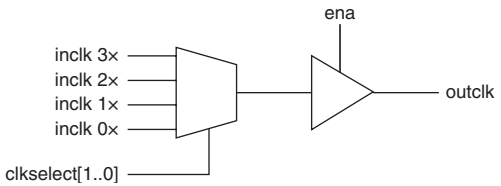
Clock Power Management

Clocks represent a significant portion of dynamic power consumption due to their high switching activity and long paths. Figure 9–1 shows a 7% average contribution to power consumption for global clock routing in Stratix II devices and 15% in Cyclone II devices. Actual clock-related power consumption is higher than this because the power consumed by local clock distribution within logic, memory, and DSP or multiplier blocks is included in the power consumption for the respective blocks.

Clock routing power is automatically optimized by the Quartus II software, which only enables those portions of the clock network that are required to feed downstream registers. Power can be further reduced by gating clocks when they are not needed. It is possible to build clock gating logic, but this approach is not recommended because it is difficult to generate a glitch-free clock in FPGAs using ALMs or LEs.

Stratix II and Cyclone II devices use clock control blocks that include an enable signal. A clock control block is a clock buffer that lets you dynamically enable or disable the clock network and dynamically switch between multiple sources to drive the clock network. You can use the Quartus II MegaWizard Plug-In Manager to create this clock control block with the `altclkctrl` megafunction. Stratix II and Cyclone II devices provide clock control blocks for global clock networks. In addition, Stratix II devices have clock control blocks for regional clock networks. The dynamic clock enable feature lets internal logic control the clock network. When a clock network is powered down, all the logic fed by that clock network does not toggle, thereby reducing the overall power consumption of the device. Figure 9–15 shows a 4-input clock control block diagram.

Figure 9–15. Clock Control Block Diagram

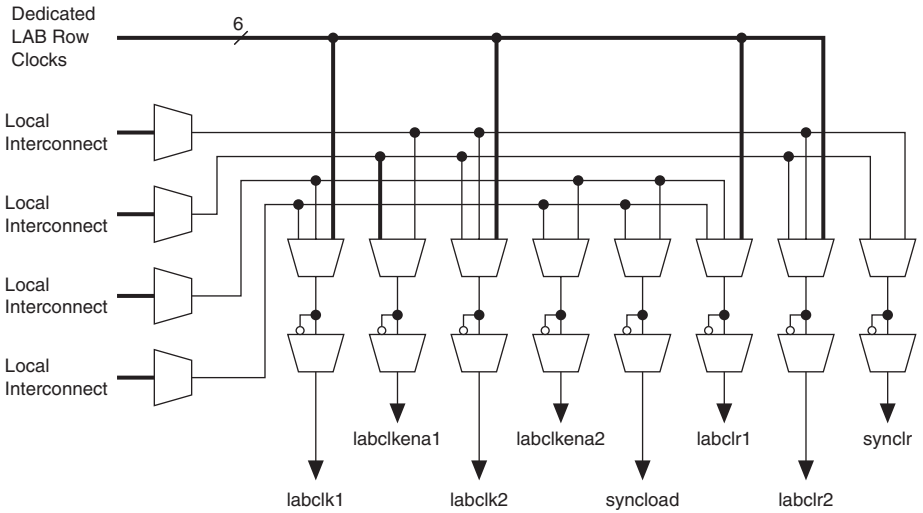


The enable signal is applied to the clock signal before being distributed to global routing. Therefore, the enable signal can either have a significant timing slack (at least as large as the global routing delay) or it can reduce the f_{MAX} of the clock signal.

For more information about using clock control blocks, refer to the *altclkctrl Megafunction User Guide*.

Another contributor to clock power consumption is the LAB clock that distributes a clock to the registers within a LAB. LAB clock power can be the dominant contributor to overall clock power. For example, in Cyclone II devices, each LAB can use two clocks and two clock enable signals as shown in Figure 9–16. Each LAB's clock signal and clock enable signal are linked. For example, an LE in a particular LAB using the `labclk1` signal also uses the `labclkena1` signal.

Figure 9–16. LAB-Wide Control Signals



To reduce LAB-wide clock power consumption without disabling the entire clock tree, use the LAB-wide clock enable to gate the LAB-wide clock. The Quartus II software automatically promotes register-level clock enable signals to the LAB-level. All registers within an LAB that share a common clock and clock enable are controlled by a shared gated clock. To take advantage of these clock enables, use a clock enable construct in the relevant HDL code for the registered logic.

LAB-Wide Clock Enable Example

This VHDL code makes use of a LAB-wide clock enable. This clock-gating logic is automatically turned into an LAB-level clock enable signal.

```
IF clk'event AND clock = '1' THEN
    IF logic_is_enabled = '1' THEN
        reg <= value;
    ELSE
        reg <= reg;
    END IF;
END IF;
```

For more information on LAB-wide control signals, refer to the *Stratix II Architecture* or *Cyclone II Architecture* chapters in the respective device handbook.

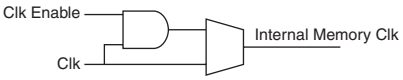
Reducing Memory Power Consumption

The memory blocks in FPGA devices can represent a large fraction of typical core dynamic power. Memory represents 14% of the core dynamic power in a typical Stratix II device design and 9% in a Cyclone II device design. Memory blocks are unlike most other blocks in the device because most of their power is tied to the clock rate, and is insensitive to the toggle rate on the data and address lines.

When a memory block is clocked, there is a sequence of timed events that occur within the block to execute a read or write. The circuitry controlled by the clock consumes the same amount of power regardless of whether or not the address or data has changed from one cycle to the next. Thus, the toggle rate of input data and the address bus have no impact on memory power consumption.

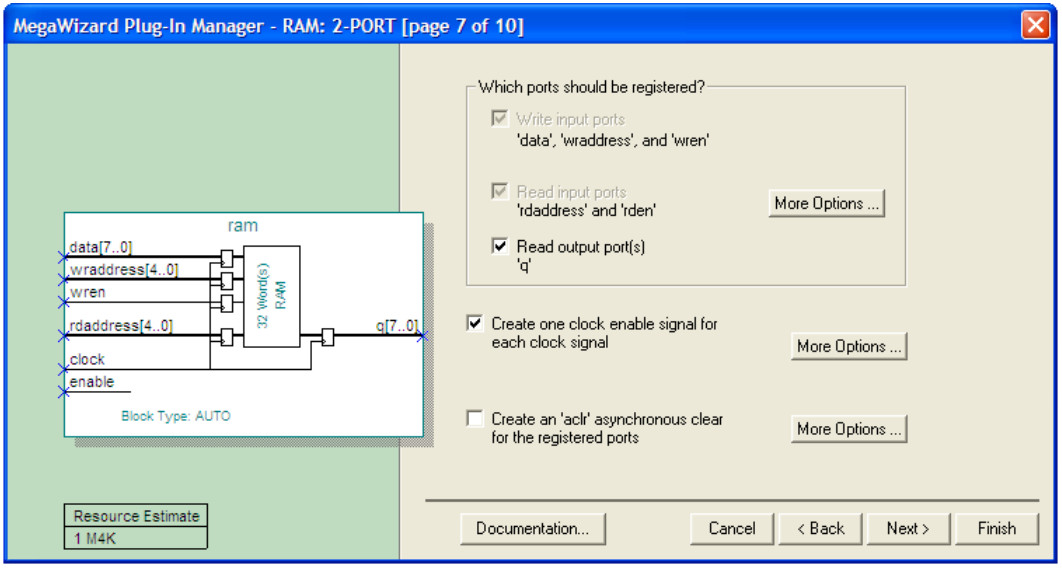
The key to reducing memory power consumption is to reduce the number of memory clocking events. You can achieve this through clock network-wide gating described in "Clock Power Management" on page 9–20, or on a per-memory basis through use of the clock enable signals on the memory ports. Figure 9–17 shows the logical view of the internal clock of the memory block. Use the appropriate enable signals on the memory to make use of the clock enable signal instead of gating the clock.

Figure 9–17. Memory Clock Enable Signal



Use of the clock enable signal enables the memory only when necessary and shuts it down for the rest of the time, reducing the overall memory power consumption. You can use the Quartus II MegaWizard Plug-In Manager to create these enable signals by selecting the **Clock enable signal** option for the appropriate port when generating the memory block function (Figure 9–18).

Figure 9–18. MegaWizard Plug-In Manager RAM 2-Port Clock Enable Signal Selectable Option

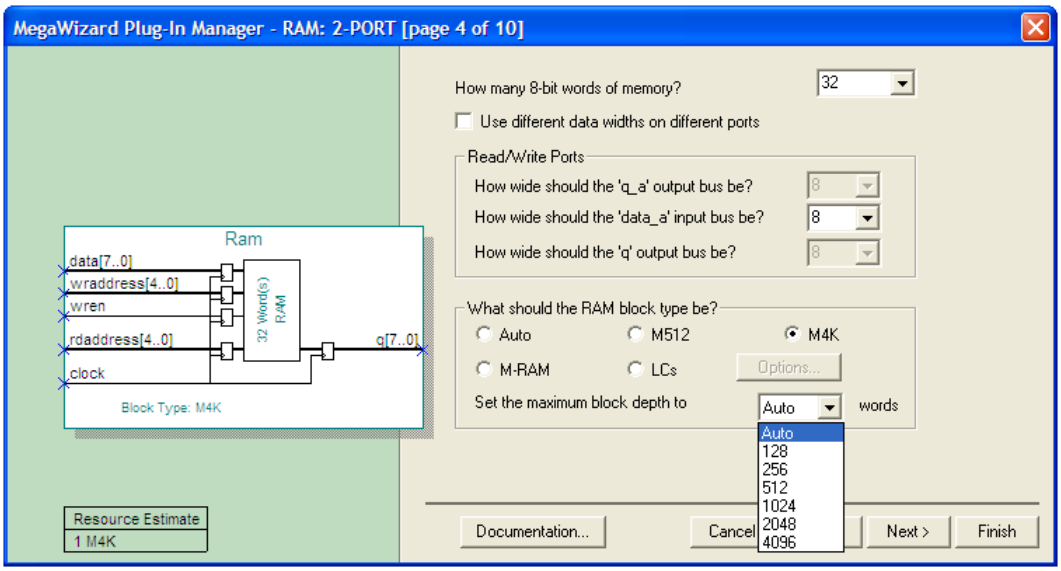


For example, consider a design that contains a 32-bit-wide M4K memory block in ROM mode that is running at 200 MHz. Assuming that the output of this block is only needed approximately every four cycles, this memory block will consume 8.45 mW of dynamic power according to the demands of the downstream logic. By adding a small amount of control logic to generate a read clock enable signal for the memory block only on the relevant cycles, the power can be cut 75% to 2.15 mW.

You can also use the MAXIMUM_DEPTH parameter in your memory megafunction to save power in Stratix II and Cyclone II devices; however, this approach may increase the number of LEs required to implement the memory and affect design performance.

The MAXIMUM_DEPTH parameter for memory modules can be set manually in the megafunction instantiation or in the MegaWizard Plug-In Manager (Figure 9–19). The Quartus II software can automatically choose the best design memory configuration for optimal power as described in "Power-Driven Compilation" on page 9–5.

Figure 9–19. MegaWizard Plug-In Manager RAM 2-Port Maximum Depth Selectable Option



Memory Power Reduction Example

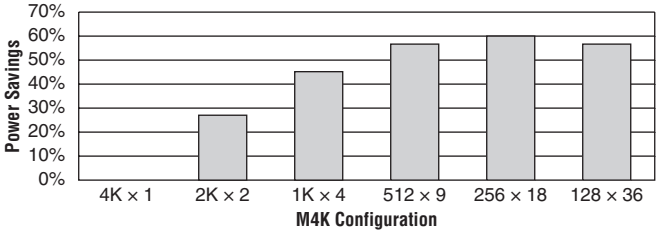
Table 9–9 shows power usage measurements for a 4K × 36 simple dual-port memory implemented using multiple M4K blocks in a Stratix II EP2S15 device. For each implementation, the M4K blocks are configured with a different memory depth.

Table 9–9. 4K × 36 Simple Dual-Port Memory Implemented Using Multiple M4K Blocks

M4K Configuration	Number of M4K Blocks	ALUTs
4K × 1 (Default setting)	36	0
2K × 2	36	40
1K × 4	36	62
512 × 9	32	143
256 × 18	32	302
128 × 36	32	633

Figure 9–20 shows the amount of power saved using the `MAXIMUM_DEPTH` parameter. For all implementations, a user-provided read enable signal is present to indicate when read data is needed. Using this power saving technique can reduce power consumption by as much as 60%.

Figure 9–20. Power Savings Using MAXIMUM_DEPTH Parameter



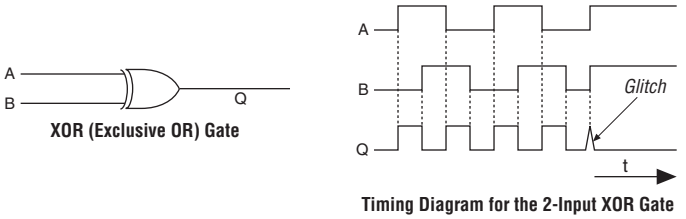
As the memory depth becomes shallower, memory dynamic power decreases because unaddressed M4K blocks can be shut off using a decoded combination of address bits and the read enable signal. For a 128-deep memory block, power used by the extra LEs starts to outweigh the power gain achieved by using a shallower memory block depth. The power consumption of the memory blocks and associated LEs depends on the memory configuration.

Pipelining & Retiming

Designs with many glitches consume more power because of faster switching activity. Glitches cause unnecessary and unpredictable temporary logic switches at the output of combinational logic. A glitch usually occurs when there is a mismatch in input signal timing leading to unequal propagation delay.

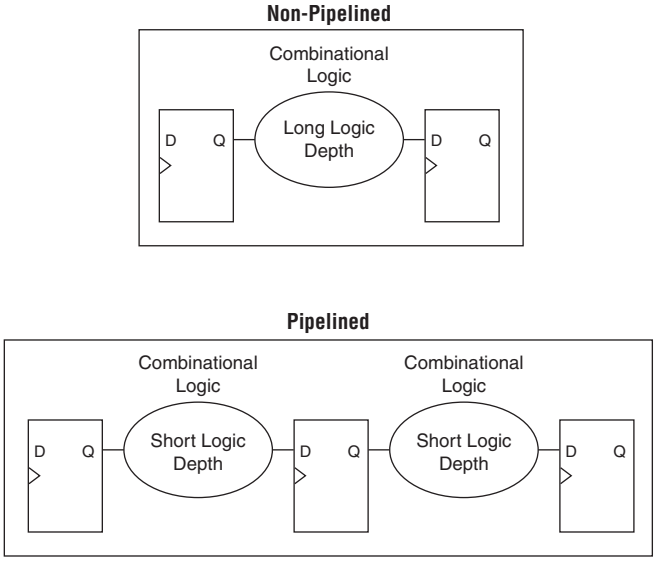
For example, consider an input change on one input of a 2-input XOR gate from 1 to 0, followed a few moments later by an input change from 0 to 1 on the other input. For a brief moment of time, both inputs become 1 (high) during the state transition, resulting in 0 (low) at the output of the XOR gate. Subsequently, when the second input transition takes place, the XOR gate output becomes 1 (high). During signal transition, a glitch is produced before the output becomes stable, as shown in Figure 9–21. This glitch can propagate to subsequent logic and create unnecessary switching activity, increasing power consumption. Circuits with many XOR functions, such as arithmetic circuits or cyclic redundancy check (CRC) circuits, tend to have many glitches if there are several levels of combinational logic between registers.

Figure 9–21. XOR Gate Showing Glitch at the Output



Pipelining can reduce design glitches by inserting flipflops into long combinational paths. Flipflops do not allow glitches to propagate through combinational paths. Therefore, a pipelined circuit tends to have less glitching. Pipelining has the additional benefit of generally allowing higher clock speed operations, although it does increase the latency of a circuit (in terms of the number of clock cycles to a first result). Figure 9–22 shows an example where pipelining is applied to break-up a long combinational path.

Figure 9–22. Pipelining Example



Pipelining is very effective for glitch-prone arithmetic systems because it reduces switching activity, resulting in reduced power dissipation in combinational logic. Additionally, pipelining allows higher-speed operation by reducing logic-level numbers between registers. The disadvantage of this technique is that if there are not many glitches in your design, pipelining may increase power consumption by adding unnecessary registers. Pipelining can also increase resource utilization.

Pipelining Experiment for Stratix II Devices

In this experiment, three designs are implemented in Stratix II devices with and without pipelining. These three designs use arithmetic heavily (based on XOR functions) that may result in significant glitching.

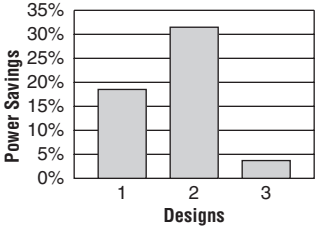
Table 9–10 shows the resource utilization for the designs used in the experiment.

Table 9–10. Resources Used in the Pipelining Experiment for Stratix II Devices

Design Name	Pipelined	ALUTs	Registers
Multiplier (Design 1)	No	9,726	448
	Yes	9,772	1,109
Accumulator multipliers (Design 2)	No	13,719	1,120
	Yes	14,007	2,260
Fir filter (Design 3)	Yes (level 1)	1,048	949
	Yes (level 2)	932	929

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–23 shows that pipelining reduces dynamic power consumption by as much as 31% in Stratix II devices.

Figure 9–23. Power Savings Using Pipelining for Stratix II Devices



Pipelining Experiment for Cyclone II Devices

In this experiment, four designs are implemented in Cyclone II devices with and without pipelining. These three designs heavily use arithmetic (based on XOR functions) that may result in significant glitching.

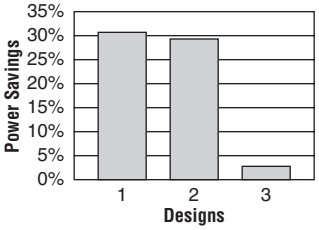
Table 9–11 shows resource utilization for the designs used in the experiment.

Table 9–11. Resources Used in the Pipelining Experiment for Cyclone II Devices

Design Name	Pipelined	LEs	Registers
Accumulator Multipliers (Design 1)	No	6,870	320
	Yes	13,071	3,719
Adder (Design 2)	No	7,392	1,076
	Yes	7,343	752
Divider (Design 3)	No	6,659	320
	Yes	6,735	520

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–24 shows that pipelining reduces dynamic power by as much as 31% in Cyclone II devices.

Figure 9–24. Power Savings Using Pipelining for Cyclone II Devices



Architectural Optimization

You can use design-level architectural optimization by taking advantage of specific device architecture features. These features include dedicated memory and DSP or multiplier blocks available in FPGA devices to perform memory or arithmetic-related functions. You can use these blocks in place of LUTs to reduce power consumption. For example, you can build large shift registers from RAM-based FIFO buffers instead of building the shift registers from the LE registers.

The Stratix II device family allows you to efficiently target small, medium, and large memories with the TriMatrix memory architecture. Each TriMatrix memory block is optimized for a specific function. The M512 memory blocks are useful for implementing small FIFO buffers,

DSP, and clock domain transfer applications. M512 memory blocks are more power-efficient than the distributed memory structures in some competing FPGAs. The M4K memory blocks are used to implement buffers for a wide variety of applications, including processor code storage, large look-up table implementation, and large memory applications. The M-RAM blocks are useful in applications where a large volume of data must be stored on-chip. Effective utilization of these memory blocks can have a significant impact on power reduction in your design.

The Cyclone II device family has configurable M4K memory blocks that provide various memory functions such as RAM, FIFO buffers, and ROM.

For more information on using DSP and memory blocks efficiently, refer to the *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Architectural Optimization Experiment for Stratix II Devices

In this experiment, three designs are implemented in Stratix II devices in three ways to illustrate the power-reducing capabilities of dedicated blocks. The first two designs use logic elements and DSP blocks. The third design uses M4K and M-RAM blocks. In the third design, you can see that using MRAM blocks is more power efficient than using M4K blocks for large memory applications. The power optimization options for synthesis and fitting are turned off in this experiment.

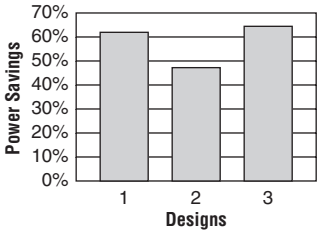
Table 9–12 shows relative resource usage results.

Table 9–12. Designs Used in the Architectural Optimization Experiment for Stratix II Devices

Design Name	Implementation	ALUT	Register	DSP Blocks	Memory
Design 1	Regular implementation	9,726	448	0	0
	Dedicated resource implementation	1,124	448	121	0
Design 2	Regular implementation	13,719	1,120	0	0
	Dedicated resource implementation	2,880	896	212	0
Design 3	M4K	286	228	0	1,835,008 (M4K)
	M-RAM	224	224	0	1,835,008 (M-RAM)

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–25 shows that the architectural optimization technique has power savings of over 60% in Stratix II devices.

Figure 9–25. Power Savings Using Dedicated Blocks for Stratix II Devices



Architectural Optimization Experiment for Cyclone II

In this experiment, three designs are implemented in Cyclone II devices in three ways to illustrate the power-reducing capabilities of dedicated blocks. The first two designs use LEs and multiplier blocks. The third design uses LEs and M4K blocks.

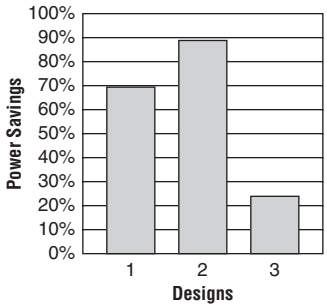
Table 9–13 shows relative resource usage results.

Table 9–13. Designs Used in the Architectural Optimization Experiment for Cyclone II Devices

Design Name	Implementation	LEs	Register	Multiplier Blocks	Memory
Design 1	Regular implementation	6,870	320	0	0
	Dedicated resource implementation	1,130	320	49	0
Design 2	Regular implementation	7,343	752	0	0
	Dedicated resource implementation	1,401	608	44	0
Design 3	Regular implementation	1,550	1,265	0	0
	M4K	72	72	0	1,152

The PowerPlay Power Analyzer estimates the power using a gate-level simulation output file. Figure 9–26 shows that the architectural optimization technique has power savings of as much as 88% in Cyclone II devices.

Figure 9–26. Power Savings Using Dedicated Blocks for Cyclone II Devices



I/O Power Guidelines

Non-terminated I/O standards such as LVTTL and LVCMOS have a rail-to-rail output swing. The voltage difference between logic-high and logic-low signals at the output pin is equal to the V_{CCIO} supply voltage. If the capacitive loading at the output pin is known, the dynamic power consumed in the I/O buffer can be calculated as:

$$P = 0.5 \times F \times C \times V^2$$

In this equation, *F* is the output transition frequency and *C* is the total load capacitance being switched. *V* is equal to V_{CCIO} supply voltage. Because of the quadratic dependence on V_{CCIO}, lower voltage standards consume significantly less dynamic power. In addition, lower pin capacitance is an important factor in considering I/O power consumption. Hardware and simulation data show that Stratix II device I/O pins have half the pin capacitance of the nearest competing FPGA. Cyclone II devices exhibit 20% less I/O power consumption than competitive, low-cost, 90 nm FPGAs.

Transistor-to-transistor logic (TTL) I/O buffers consume very little static power. As a result, the total power consumed by a LVTTL or LVCMOS output is highly dependent on load and switching frequency.

When using resistively terminated I/O standards like SSTL and HSTL, the output load voltage swings by a small amount around some bias point. The same dynamic power equation is used, where *V* is the actual

load voltage swing. Because this is much smaller than V_{CCIO}, dynamic power is lower than for nonterminated I/O under similar conditions. These resistively terminated I/O standards dissipate significant static (frequency-independent) power, because the I/O buffer is constantly driving current into the resistive termination network. However, the lower dynamic power of these I/O standards means they often have lower total power than LVCMOS or LVTTL for high-frequency applications. Use the lowest drive strength I/O setting that meets your speed and waveform requirements to minimize I/O power when using resistively terminated standards.

You can save a small amount of static power by connecting unused I/O banks to the lowest possible V_{CCIO} voltage of 1.2 V.

Table 9–14 shows the total supply and thermal power consumed by outputs using different I/O standards for Stratix II devices. The numbers are for an I/O pin transmitting random data clocked at 200 MHz with a 10 pF capacitive load.

Table 9–14. I/O Power for Different I/O Standards for Stratix II Devices

Standard	Total Supply Current Drawn from V_{CCIO} Supply (mA)	Total On-Chip Thermal Power Dissipation (mW)
3.3-V LVTTL	2.42	9.87
2.5-V LVCMOS	1.9	6.69
1.8-V LVCMOS	1.34	4.18
1.5-V LVCMOS	1.18	3.58
3.3-V PCI	2.47	10.23
SSTL-2 class I	6.07	4.42
SSTL-2 class II	10.72	5.1
SSTL-18 class I	5.33	3.28
SSTL-18 class II	8.56	4.06
HSTL-15 class I	6.06	3.49
HSTL-15 class II	11.08	4.87
HSTL-18 class I	6.87	4.09
HSTL-18 class II	12.33	5.82

For this specific configuration, non-terminated standards generally use less power, but this is not always the case. If the frequency or the capacitive load is increased, the power consumed by non-terminated outputs increases faster than the power of terminated outputs.

For more information on I/O Standards, refer to the *Selectable I/O Standards in Stratix II Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Selectable I/O Standards in Cyclone II Devices* chapter in the *Cyclone II Device Handbook*.

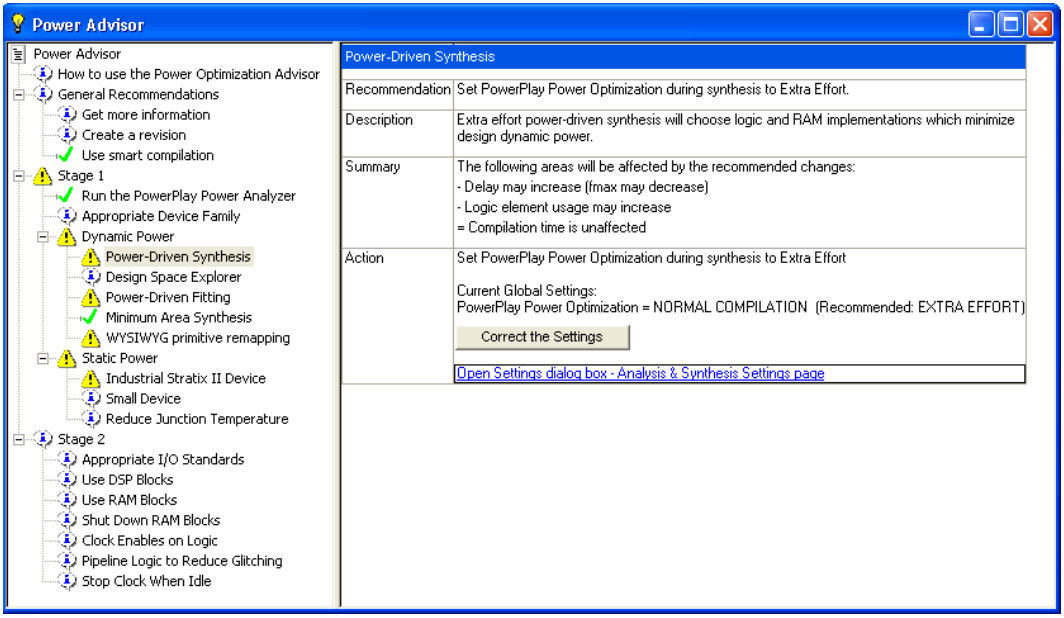
Power Optimization Advisor

The Quartus II software, beginning with version 5.1, includes the Power Optimization Advisor which provides specific power optimization advice and recommendations based on the current design project settings and assignments. The advisor covers many of the suggestions listed in this chapter. The following example shows how to reduce your design power with the Power Optimization Advisor.

Power Optimization Advisor Example

After compiling your design, run the PowerPlay Power Analyzer to determine your design power and to see where power is dissipated in your design. Based on this information, you can run the power optimization advisor to implement recommendations that can reduce design power. Figure 9–27 shows the Power Optimization Advisor after compiling a design that is not fully optimized for power.

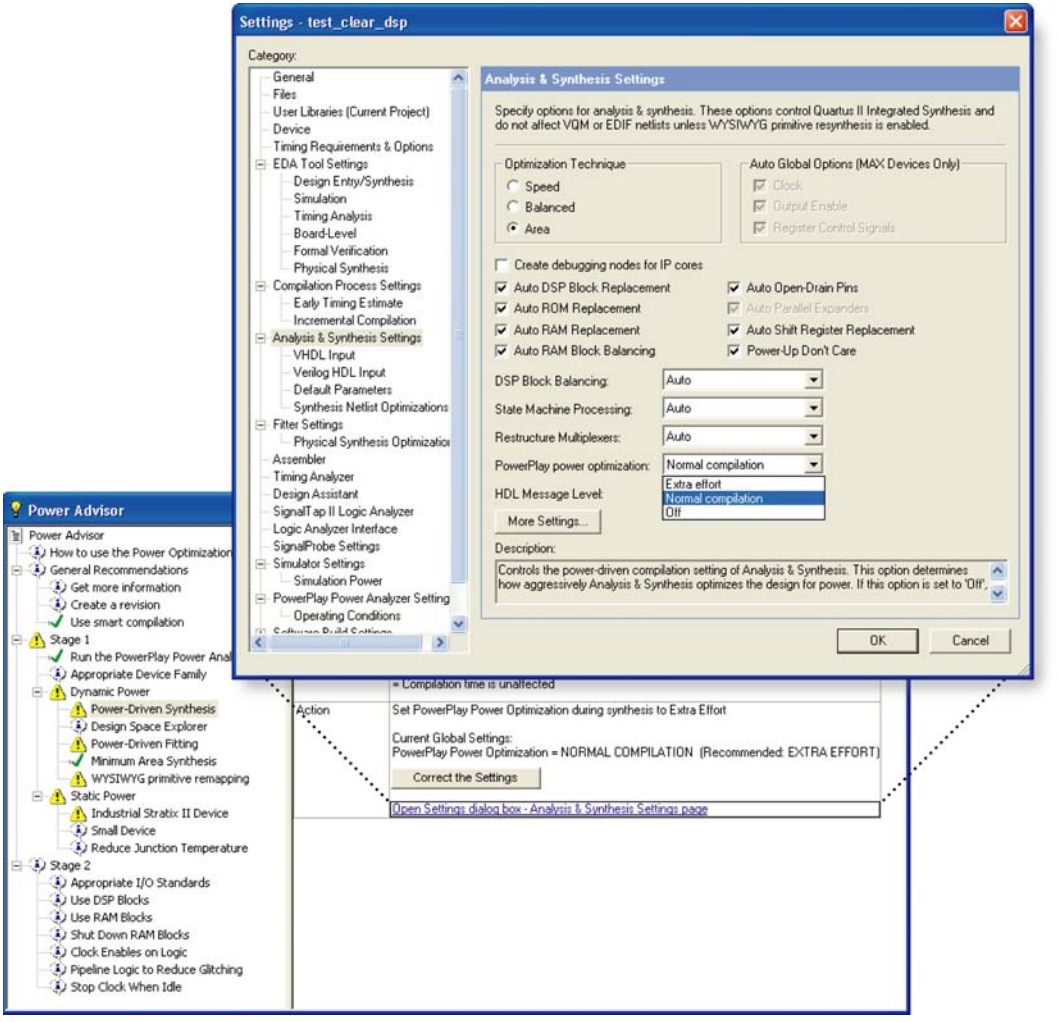
Figure 9–27. Power Optimization Advisor



The Power Optimization Advisor shows the recommendations that can reduce power in your design. The recommendations are split into stages to show the order in which you should apply the recommended settings. The first stage shows the options that are easy to implement, as it has to do mostly with CAD settings, and are highly effective in reducing design power. An icon indicates whether each recommended setting is made in the current project. In Figure 9–27, the check mark icon for Stage 1 shows the recommendations that are already implemented. The warning icons indicate recommendations that are not followed for this compilation. The information icon shows the general suggestions. Each recommendation includes the description, summary of the affect of the recommendation, and the action required to make the appropriate setting.

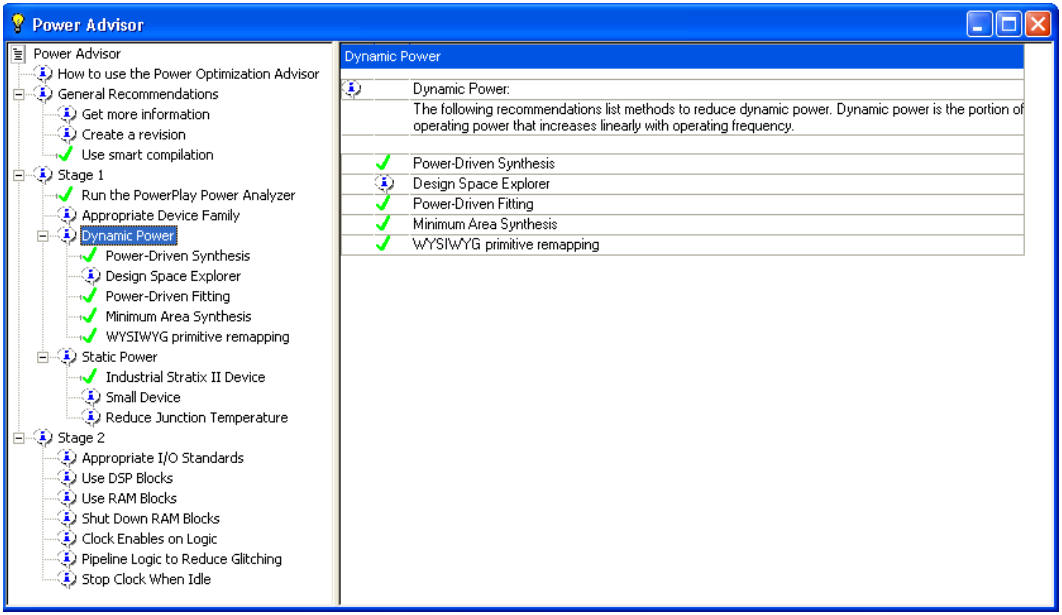
There is a link from each recommendation to the appropriate location in the Quartus II user interface where you can change the setting, such as the **Power-Driven Synthesis** setting. You can change the **Power-Driven Synthesis** setting by clicking **Open Settings dialog box - Analysis & Synthesis Settings page** (Figure 9–28). The **Setting** dialog box is shown with the **Analysis & Synthesis Settings** page selected, where you can change the **PowerPlay power optimization** settings.

Figure 9–28. Analysis & Synthesis Settings Page



After making the recommended changes, recompile your design. The Power Optimization Advisor indicates with green check marks that the recommendations were implemented successfully (Figure 9–29). You can use the PowerPlay Power Analyzer to verify your design power results.

Figure 9–29. Implementation of Power Optimization Advisor Recommendations



The recommendations listed in Stage 2 generally involve design changes, rather then CAD settings changes as in Stage 1. You can use these recommendations to further reduce your design power consumption. It is recommended to implement Stage 1 recommendations first, then the Stage 2 recommendations.

Conclusion

The combination of a smaller process technology (specifically a 90 nm geometry), the use of low-k dielectric material, and reduced supply voltage, significantly reduces dynamic power consumption in Stratix II and Cyclone II FPGAs. However, this reduction in dynamic power may be offset as design complexity and clock frequencies increase in 90 nm technology devices. Use the design recommendations presented in this chapter to optimize resources utilization and minimize power consumption.

10. Timing Closure Floorplan

QII52006-6.0.0

Introduction

With FPGA designs surpassing the million-gate mark, designers need advanced tools to better analyze timing closure issues to achieve their system performance goals. The Altera® Quartus® II software offers many advanced design analysis tools that allow detailed timing analysis of your designs, including a fully integrated Timing Closure Floorplan Editor. With these tools and options, you can easily determine and locate the critical paths in the floorplan of the targeted device. This chapter explains how to use these tools and options to enhance your FPGA design analysis.

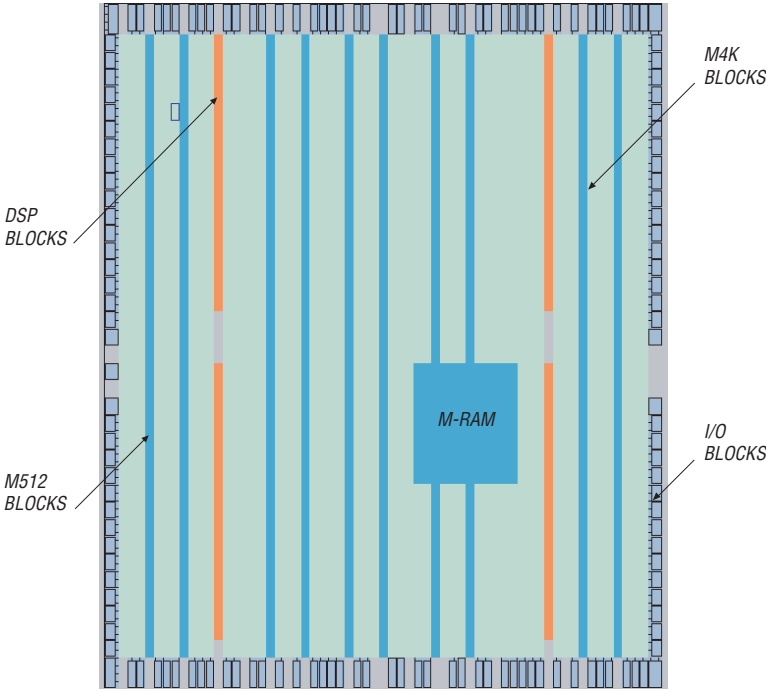
Design Analysis Using the Timing Closure Floorplan

The Timing Closure Floorplan Editor assists you in visually analyzing your designs before and after performing a full design compilation in the Quartus II software. This floorplan editor, used in conjunction with traditional Quartus II timing analysis features, provides a powerful method for performing design analysis.

Timing Closure Floorplan Views

The Timing Closure Floorplan Editor incorporates several views of your design. The Field View is a color-coded, high-level view of resources. Figure 10–1 shows the Field View of a Stratix® II device.

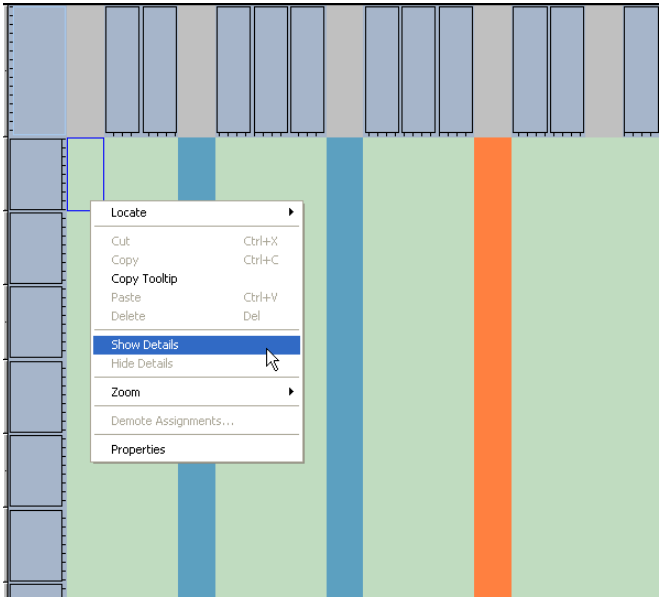
Figure 10–1. Field View of a Stratix II Device



In the Field View, you can view the details of a resource by selecting the **resource,** right-click and select **Show Details**. To hide the details, select all the resources, right-click, and select **Hide Details** (Figure 10–2).

You can also view your design in the Timing Closure Floorplan Editor with the traditional Interior Cells, Package Top, and Package Bottom views. Use the View menu to change to the various floorplan views.

Figure 10–2. Show Details & Hide Details of a Logic Array Block in Field View



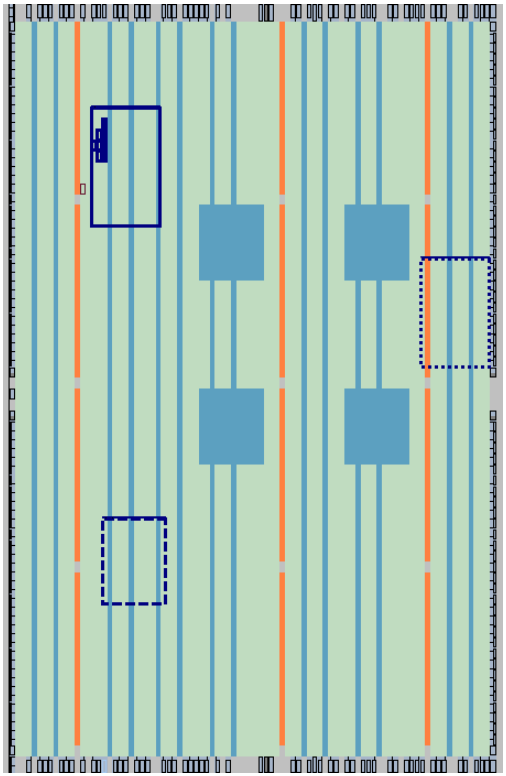
Viewing Assignments

The Timing Closure Floorplan Editor differentiates between user assignments (Figure 10–3) and fitter placements (Figure 10–4). User assignments are assignments that a user makes including LogicLock™ regions. Fitter placements are the locations where the Quartus II software placed unconstrained (or unassigned) nodes in the last compilation. You can view both user and fitter placements at the same time.

If the device is changed after a compilation, the user assignment and fitter placement options cannot be used together. When this situation occurs, the fitter placement displays the last compilation result and the user assignment displays the floorplan of the newly selected device.

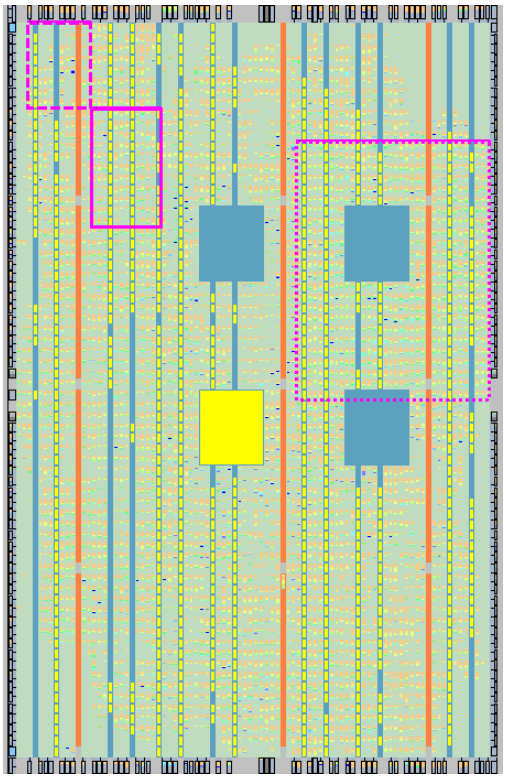
To see user assignments, click the **User Assignments** icon in the Floorplan Editor toolbar, or on the View menu, point to **Assignments** and click **Show User Assignments (**Figure 10–3).

Figure 10–3. User Assignments



To see fitter placements, click the **Fitter Placements** icon in the Floorplan Editor toolbar, or on the View menu, point to **Assignments** and click **Show Fitter Placements** (Figure 10–4).

Figure 10–4. Fitter Placements

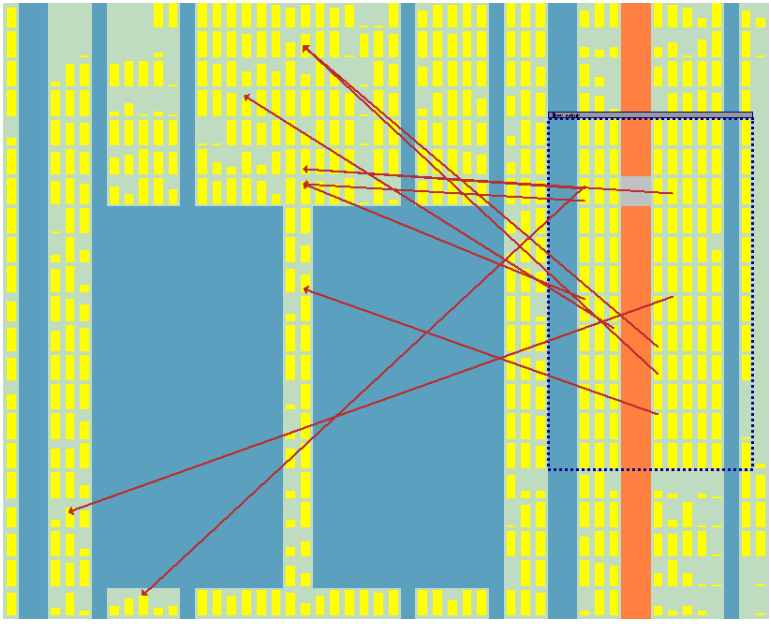


Viewing Critical Paths

The View Critical Paths feature displays routing paths in the Timing Closure floorplan, as shown in Figure 10–5. The criticality of a path is determined by its slack and is also shown in the timing analysis report.

To view critical paths in the floorplan, click the **Show Critical Paths** icon, or on the View menu, point to **Routing** and click **Show Critical Paths**. To set the criteria for the critical path you want to view, select the **Critical Paths Settings** icon, or on the View menu, point to **Routing** and click **Critical Paths Settings** (Figure 10–6).

Figure 10–5. Critical Paths

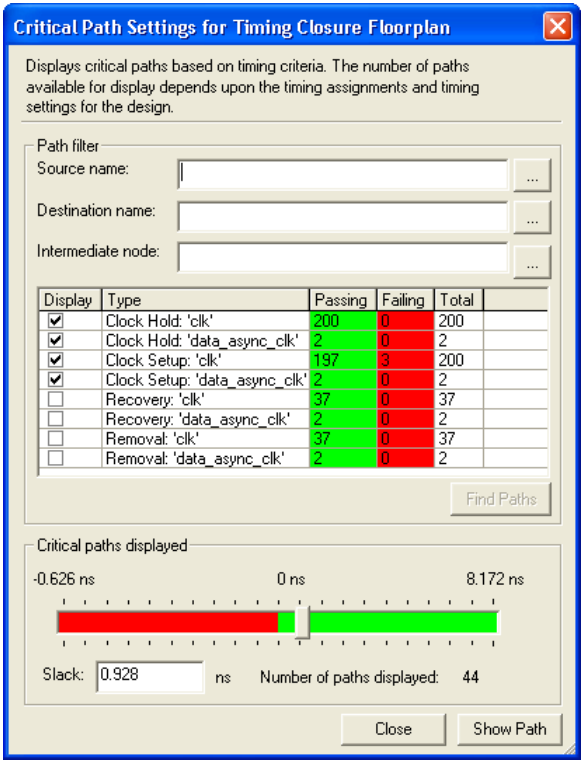


When viewing critical paths, you can specify the clock in the design to be viewed.You determine the paths to be displayed by specifying the slack threshold in the slack field. For example, you can view all paths with a slack of 4.5 ns or worse.

Timing settings must be made and a timing analysis performed for paths to be displayed in the floorplan.

The critical path feature is extremely useful in determining the criticality of nodes based on placement. There are a number of options to view the details of the critical path.

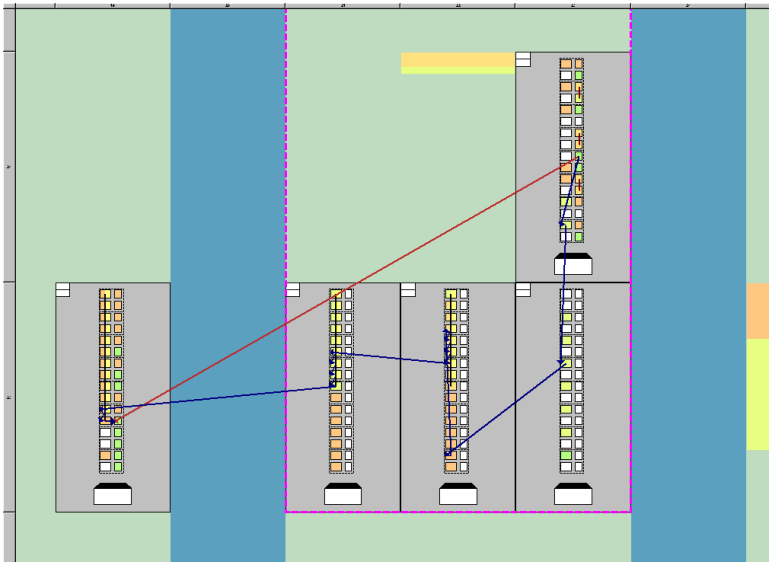
Figure 10–6. Critical Paths Settings Window



The default view shows the path with the source and destination registers displayed. You can also view all the combinational nodes along the worst-case path between the source and destination nodes. To view the full path, select the path by clicking on the delay label, right click, and select **Show Path Edges**. Figure 10–7 shows a critical path through combinational nodes. To hide the combinational nodes, select the path, right click, and select **Hide Path Edges**.

You must view the routing delays to select a path.

Figure 10–7. Worst-Case Combinational Paths of Critical Paths

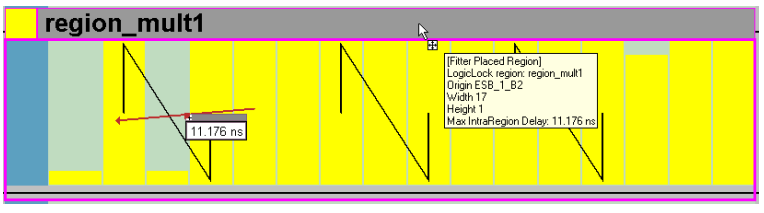


To assign the path to a LogicLock region using the Paths dialog box, select the path, right-click, and select **Properties**.

For more information on creating path-based assignments with LogicLock regions, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

You can determine the maximum routing delay between two nodes within a LogicLock region. To use this feature, click the **Show Intra-region Delay** icon or on the View menu click **Routing** > **Show Intra-region Delay**. Place your cursor over a fitter-placed LogicLock region to see the maximum delay. Figure 10–8 shows the maximum routing delay of a LogicLock region.

Figure 10–8. Maximum Intra-Region Delay

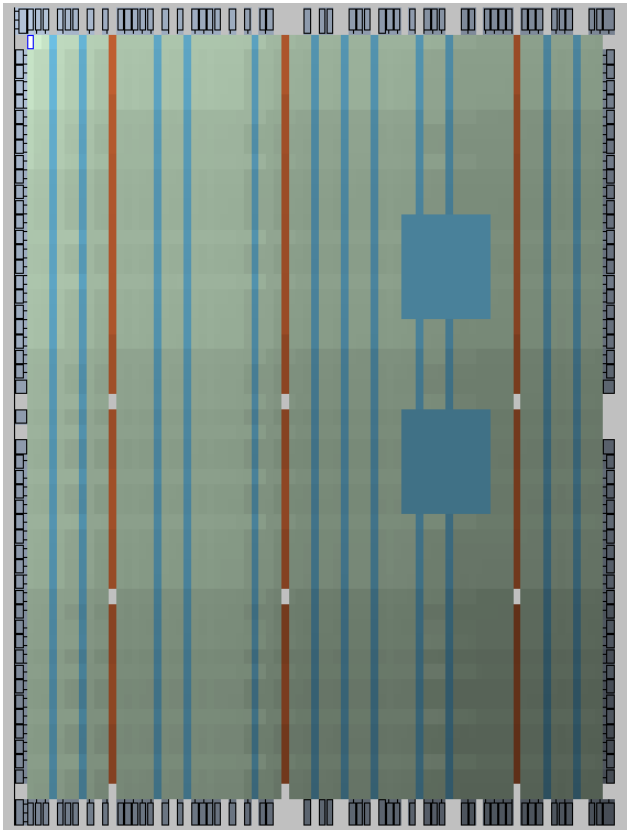


For more information on making path assignments with the Paths dialog box, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

Physical Timing Estimates

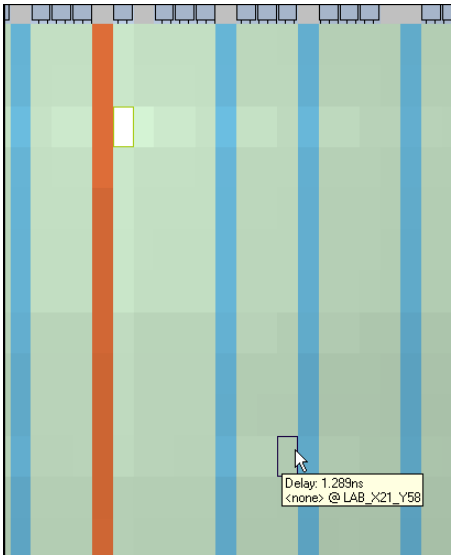
In the Timing Closure Floorplan Editor, you can select a resource and see the approximate delay to any other resource on the device. Once you select a resource, the delay is represented by the color of potential destination resources. The darker the color of the resource, the longer the delay (Figure 10–9).

Figure 10–9. Physical Timing Estimates View



You can also obtain an approximation of the delay between two points by selecting a source and holding your cursor over a potential destination resource (Figure 10–10).

Figure 10–10. Delay for Physical Timing Estimate



The delays represent an estimate based on probable best-case routing. It is possible the delay is greater than what is shown, depending on the availability of routing resources. In general, there is a strong correlation between the probable and actual delay.

To view the physical timing estimates, click the **Show Physical Timing Estimate** icon, or on the View menu, point to **Routing** and click **Show Physical Timing Estimates**.

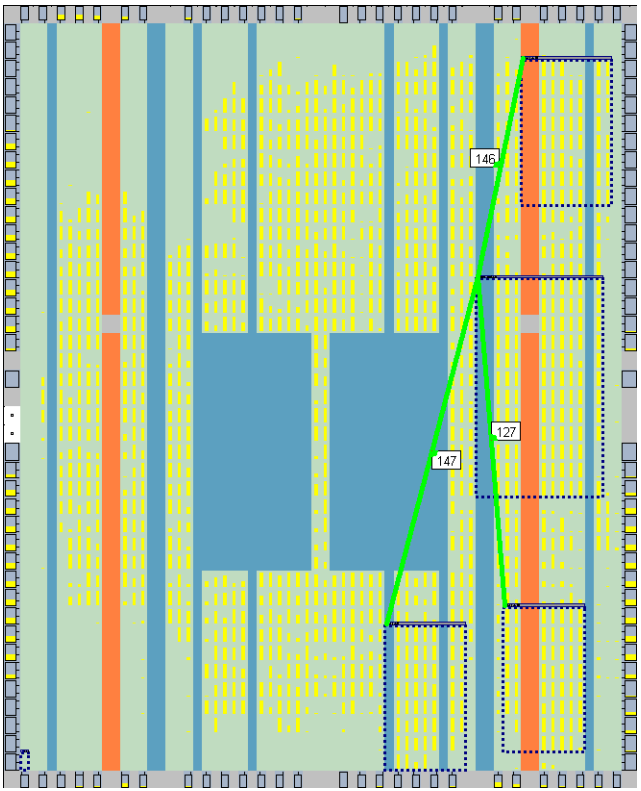
You can use the physical timing estimate information when manually placing logic in a device. This allows you to place critical nodes and modules closer together, and non-critical or unrelated nodes and modules further apart, reducing the routing congestion between critical and non-critical entities and modules. This allows the Quartus II Fitter to select the timing requirements.

LogicLock Region Connectivity

To see how logic in LogicLock regions interfaces, view the connectivity between LogicLock regions. This capability is extremely valuable when entities are assigned to LogicLock regions. It is also possible to see the fan-in and fan-out of selected LogicLock regions.

To view the connections in the timing closure floorplan, click the **Show LogicLock Regions Connectivity** icon in the toolbar, or in the View menu, point to **Routing** and click **Show LogicLock Regions Connectivity**. Figure 10–11 shows standard LogicLock region connections.

Figure 10–11. LogicLock Region Connections with Connection Count

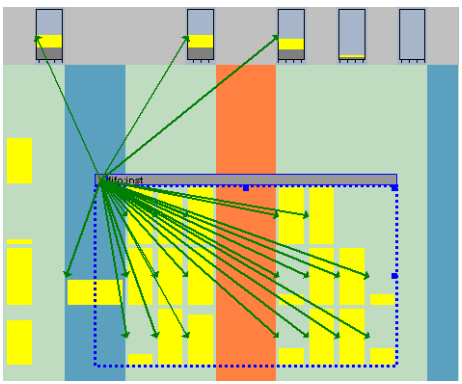


The connection line thickness indicates how many connections exist between regions. To view the number of connections between regions, click the **Show Connection Count** icon, or on the View menu, point to **Routing** and click **Show Connection Count**.

LogicLock region connectivity is applicable only when the user assignments are enabled in the Timing Closure Floorplan. When you use floating LogicLock regions, the origin of the user-assigned region is not necessarily the same as the fitter-placed region. You can change the origin of your floating LogicLock regions to that of the last compilation origin in the LogicLock Regions window or by selecting **Back-Annotate Origin and Lock** under Location in the LogicLock Regions Properties dialog box.

To see the fan-in or fan-out of a LogicLock region, select the user-assigned LogicLock region while the fan-in or the fan-out option is turned on. To set the fan-in option, click the **Show Node Fan-In** icon, or on the View menu, point to **Routing** and click **Show Node Fan-In**. To set the Fan-Out option, select the **Show Node Fan-Out** icon, or on the View menu, point to **Routing** and click **Show Node Fan-Out**. Only the nodes that have user assignments are seen when viewing fan-in or fan-out of LogicLock regions. Figure 10–12 shows the fan-out of a selected LogicLock region.

Figure 10–12. Fan-In or Fan-Out



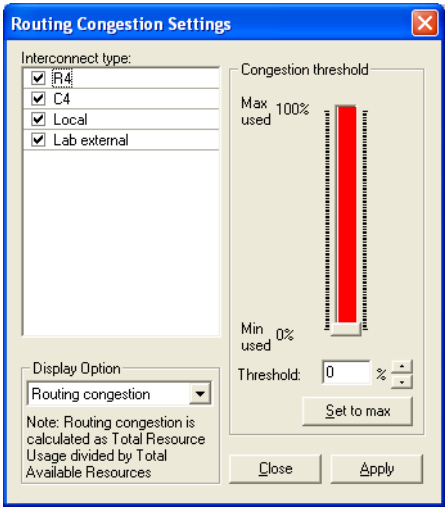
Viewing Routing Congestion

The View Routing Congestion feature allows you to determine the percentage of routing resources used after a compilation. This feature identifies where there is a lack of routing resources.

The congestion is visually represented by the color and shading of logic resources. The darker shading represents a greater routing resource utilization. Logic resources that are red have routing resource utilization greater than the specified threshold.

To view routing congestion in the floorplan, click the **Show Routing Congestion** icon, or on the View menu, point to Routing and click **Show Routing Congestion**. To set the criteria for the critical path you wish to view, click the **View Routing Congestion Settings** icon, or on the View menu, point to Routing and click **Routing Congestion Settings** (Figure 10–13).

Figure 10–13. Routing Congestion Settings Window



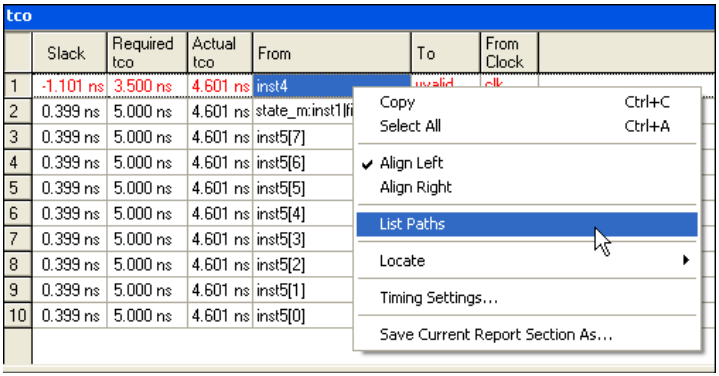
You can choose the routing resource you want to examine and set the congestion threshold. Routing congestion is calculated based on the total resource usage divided by the total available resources.

If you are using the routing congestion viewer to determine where there is a lack of routing resources, examine each routing resource individually to see which ones use close to 100% of available resources.

I/O Timing Analysis Report File

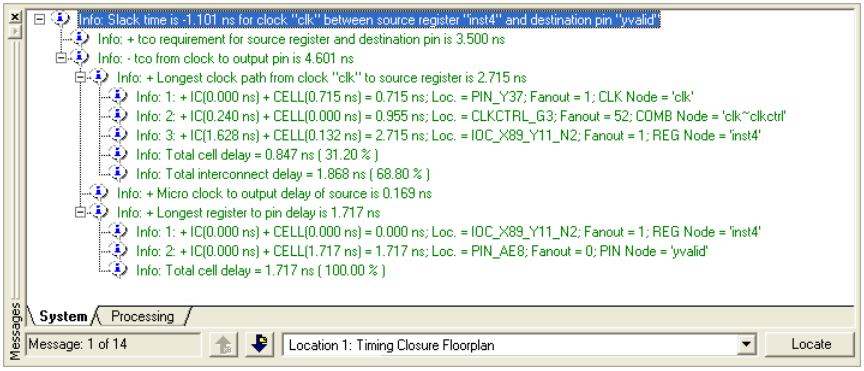
Use the Timing Analyzer folder in the Compilation Report on the Processing menu to determine whether I/O timing has been met. The t_{SU}, t_H, and t_{CO} reports list the I/O paths and the slack associated with each. The I/O paths that did not meet the required timing are reported with a negative slack and are displayed in red (Figure 10–14).

Figure 10–14. I/O Requirements



To determine why timing requirements are not met, right-click a particular I/O entry and choose **List Paths**. A message appears in the **System** tab of the Message window. You can expand a selection by clicking the "+" icon at the beginning of the line (Figure 10–15). This is a good method to help you determine where the greatest delay is located on the path.

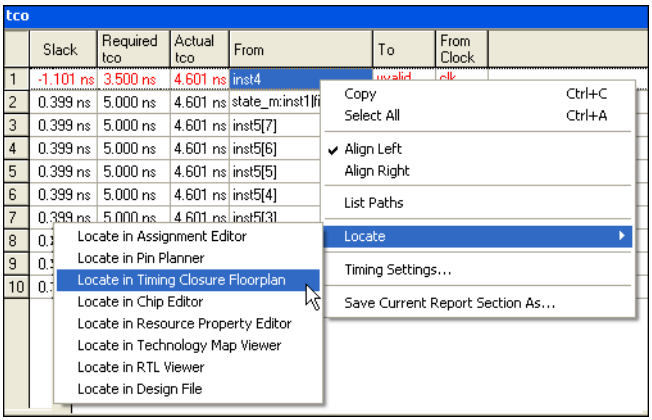
Figure 10–15. I/O Slack Report



To visually analyze I/O timing, right-click on an I/O entry in the report and select **Locate in Timing Closure Floorplan** (Figures 10–16). The Timing Closure Floorplan Editor is displayed, highlighting the I/O path.

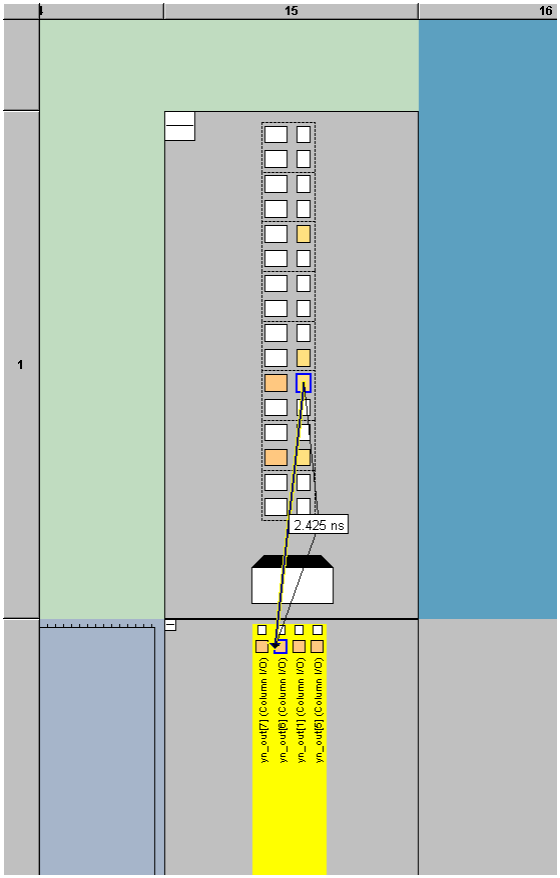
You can set the level of detail in the floorplan in the View menu.

Figure 10–16. Locate Failing Path in Timing Closure Floorplan Editor



In Figure 10–17, the arrows indicate the critical path (for example, a register) from the beginning point to the end point (such as a pin). The times shown are the slack figures for each path. Negative slack indicates paths that failed to meet their timing requirements.

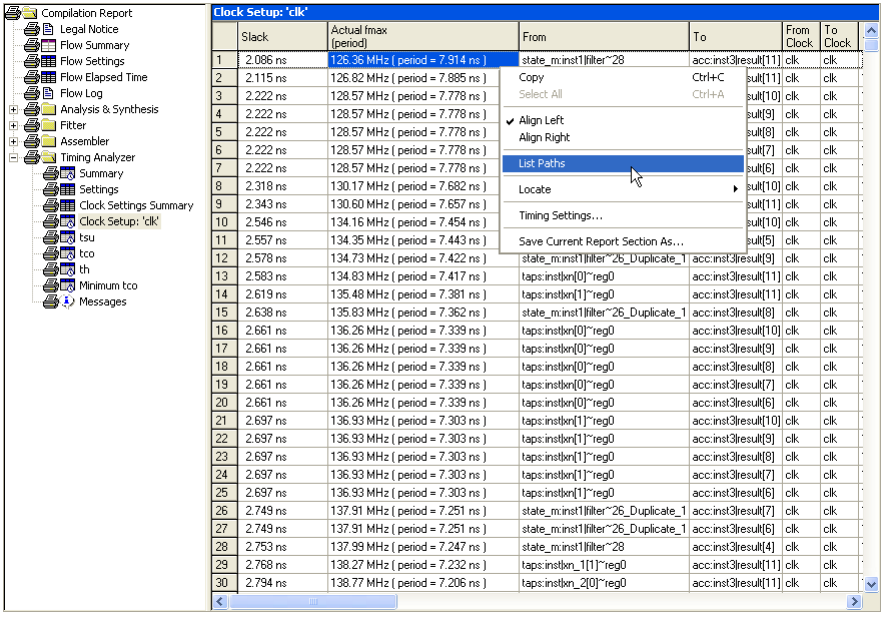
Figure 10–17. Critical I/O Paths in the Timing Closure Floorplan



f_{MAX} Timing Analysis Report File

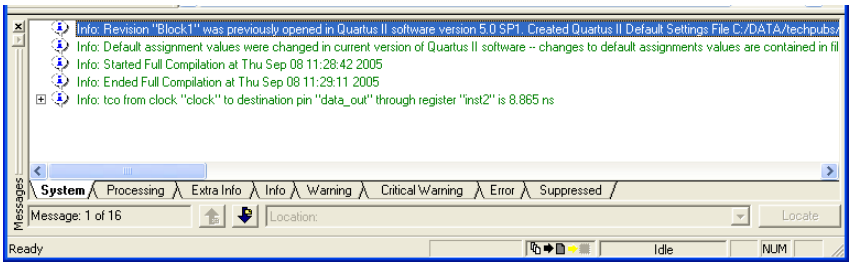
To determine whether your system performance or f_{MAX} timing requirements are met, the Quartus II software generates a timing analysis report that provides detailed timing information on every clock in your design. To access this report, on the Processing menu click the **Compilation Report** and open the **Timing Analyzer** folder. The Clock Setup folder of the Compilation Report provides figures for slack and register-to-register f_{MAX}. The paths that are not meeting timing requirements are shown in red (Figure 10–18).

Figure 10–18. f_{MAX} Requirements



To analyze why timing was not met, right-click on a particular path reported in the System tab of the Message window (Figure 10–19) and right-click the mouse and on the pop-up menu click **List Paths** to determine the location of the greatest delay along the path. Expand a selection by clicking the "+" icon at the beginning of the line.

Figure 10–19. f_{MAX} Slack Report



To visually analyze the f_{MAX} paths, right-click on a path in the report and click **Locate in Timing Closure Floorplan** to display the Timing Closure Floorplan Editor, which highlights the path (Figure 10–20). Figure 10–21 shows the Timing Closure Floorplan Editor displaying a failing path.

Double-clicking the section **Info: - Longest register to register delay is** <*slack value*> **ns** in the list path text locates the path in the Timing Closure Floorplan.

Figure 10–20. Locate Failing Path in Timing Closure Floorplan

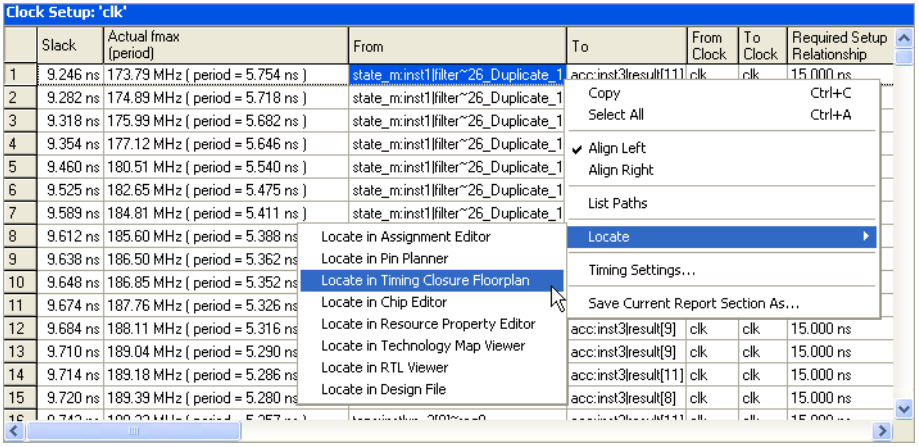
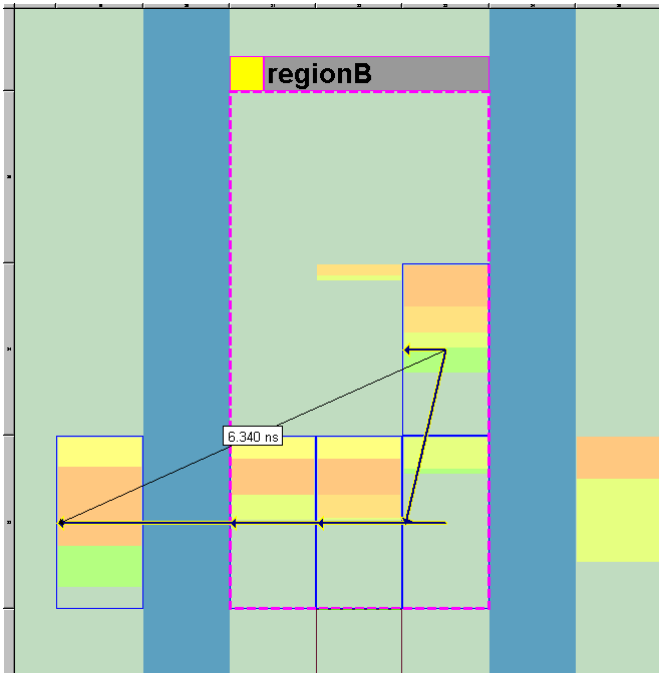
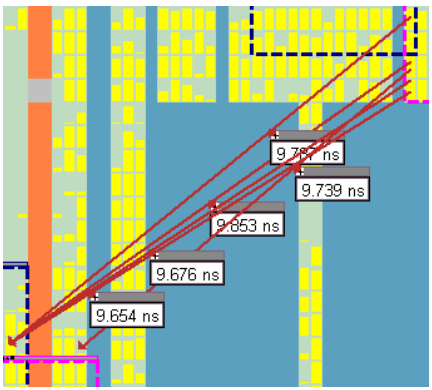


Figure 10–21. Path in Timing Closure Floorplan



You can view all failing paths in the Timing Closure Floorplan Editor using the Show Critical Paths feature. Figure 10–22 shows critical f_{MAX} paths in the Timing Closure Floorplan Editor.

Figure 10–22. Critical Paths in the Timing Closure Floorplan Editor



The *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook* shows you how to optimize your design in the Quartus II software. With the options and tools available in the Timing Closure Floorplan and the techniques described in that chapter, the Quartus II software can assist you in achieving timing closure in a more time-efficient manner.

Conclusion

Design analysis for timing closure is a fundamental requirement for optimal performance in highly complex designs. The Quartus II Timing Closure Floorplan Editor assists in closing timing quickly on complex designs, reduces iterations by providing more intelligent and better linkage between analysis and assignment tools, and balances multiple design constraints including multiple clocks, routing resources, and area constraints.

11. Netlist Optimizations & Physical Synthesis

QII52007-6.0.0

Introduction

The Quartus® II software offers advanced netlist optimization options, including physical synthesis, to optimize your design beyond the optimization performed in the course of the standard Quartus II compilation flow. The effect of these options depends on the structure of your design, but netlist optimizations can help improve the performance of your design regardless of the synthesis tool used. Device support for these optimizations varies; see the appropriate section for details.

Netlist optimization options work with your design's atom netlist, which describes a design in terms of Altera®-specific primitives. An atom netlist file can take the form of an Electronic Design Interchange Format file (**.edf**) or a Verilog Quartus Mapping file (**.vqm**) generated by a third-party synthesis tool, or a netlist used internally by the Quartus II software. Netlist optimizations are applied at different stages of the Quartus II compilation flow, either during synthesis or during fitting.

The synthesis netlist optimizations occur during the synthesis stage of the Quartus II compilation flow. The synthesis netlist optimizations make changes to the synthesis netlist output from a third-party synthesis tool or make changes as an intermediate step in Quartus II integrated synthesis (one of the optimizations applies only to third-party synthesis netlists). These netlist changes are beneficial in terms of area or speed, depending on your selected optimization technique.

Physical synthesis optimizations take place during the fitter stage of the Quartus II compilation flow. These optimizations make placement-specific changes to the netlist that improve performance results for a specific Altera device.

This chapter explains how the netlist optimizations in the Quartus II software can modify your design's netlist and help improve your quality of results. The following sections "Synthesis Netlist Optimizations" on page 11–3 and "Physical Synthesis Optimizations" on page 11–11 explain how the available optimizations work. This chapter also provides information about preserving your compilation results through back-annotation and writing out a new netlist, and provides guidelines for applying the various options.

When synthesis netlist optimization or physical synthesis options are turned on, the node names for primitives in the design can change. The fact that nodes may be renamed must be considered if you are using a LogicLock™ or verification flow that may require fixed node names, such as the SignalTap® II logic analyzer or formal verification. If your design flow requires fixed node names, you may need to turn off the synthesis netlist optimization and physical synthesis options.

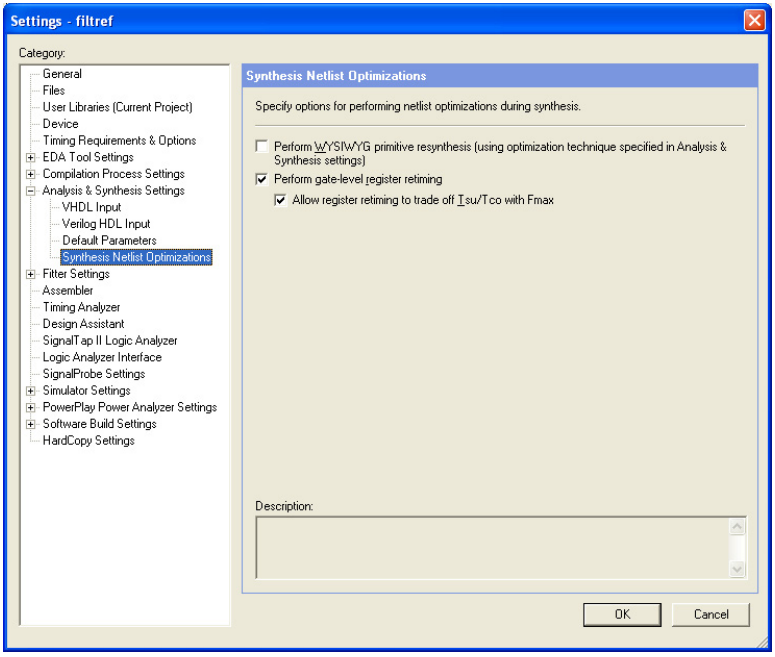
Primitive node names are specified during synthesis. When netlist optimizations are applied, node names may change as primitives are created and removed. Hardware description language (HDL) attributes applied to preserve logic in third-party synthesis tools cannot be honored because those attributes are not written into the atom netlist read by the Quartus II software. If you are synthesizing in the Quartus II software, you can use the Preserve Register (`preserve`) and Keep Combinational Logic (`keep`) attributes to maintain certain nodes in the design.

For more information about using these attributes during synthesis in the Quartus II software, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook.*

Synthesis Netlist Optimizations

To view and modify the synthesis netlist optimization options, on the Assignments menu, click **Settings**. In the **Category list**, select **Analysis & Synthesis Settings**, select **Synthesis Netlist Optimizations**, and specify the options for performing netlist optimization during synthesis, as shown in Figure 11–1.

Figure 11–1. Synthesis Netlist Optimizations Page



The sections "WYSIWYG Primitive Resynthesis" and "Gate-Level Register Retiming" on page 11–5 describe these synthesis netlist optimizations, and how they can help improve the quality of results for your design.

WYSIWYG Primitive Resynthesis

You can use the **Perform WYSIWYG primitive resynthesis (using optimization technique specified in Analysis & Synthesis settings)** synthesis option when you have an atom netlist file that specifies a design as Altera-specific primitives. Atom netlist files can take the form of either an Electronic Design Interchange Format file or a Verilog Quartus Mapping file generated by a third-party synthesis tool. To select this option, on the Assignments menu, click **Settings**. In the **Category list**, select **Analysis & Synthesis Settings**, select **Synthesis Netlist**

Optimizations, and turn on **Perform WYSIWYG primitive resynthesis (using optimization technique specified in Analysis & Synthesis settings)**. If you want to perform WYSIWYG resynthesis on only a portion of your design, you can use the Assignment Editor to assign the **Perform WYSIWYG primitive resynthesis** logic option to a lower-level entity in your design. This option can be used with the HardCopy® series, Stratix® series, Cyclone™ series, MAX® II, or APEX™ series device families.

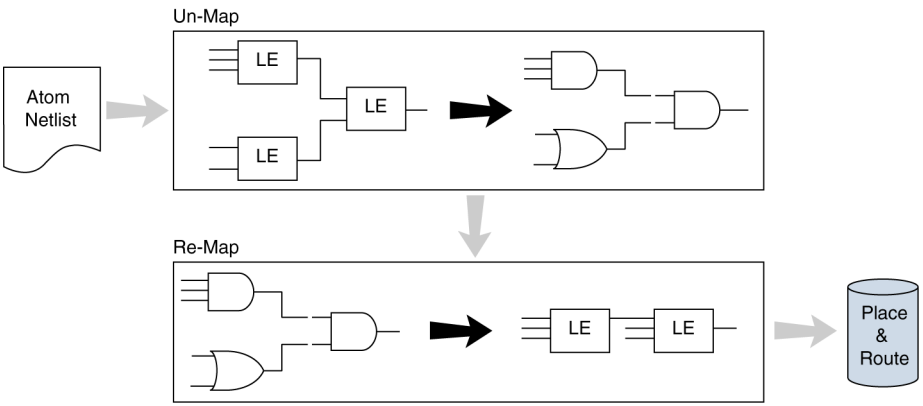
The Perform WYSIWYG primitive resynthesis option directs the Quartus II software to un-map the logic elements (LEs) in an atom netlist to logic gates, and then re-map the gates back to Altera-specific primitives. This feature allows the Quartus II software to use different techniques specific to the device architecture during the re-mapping process. This feature re-maps the design using the Optimization Technique specified for your project.

To turn on this option, on the Assignments menu, click **Settings**. In the **Category list**, select **Analysis & Synthesis Settings**. In the **Analysis & Synthesis Settings** page, under **Optimization Technique**, select **Speed**, **Area**, or **Balanced** to specify how the Quartus II technology mapper optimizes the design. The Balanced setting is the default for many Altera device families; this setting optimizes the timing critical parts of the design for speed and the rest for area.

Refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook* for details on the Optimization Technique option.

Figure 11–2 shows the Quartus II software flow for this feature.

Figure 11–2. WYSIWYG Primitive Resynthesis



The **Perform WYSIWYG primitive resynthesis** option is not applicable if you are using Quartus II integrated synthesis. With the Quartus II synthesis, you do not have to un-map Altera primitives; they are already mapped during the synthesis step using the techniques that are used with the WYSIWYG primitive resynthesis option.

The **Perform WYSIWYG primitive resynthesis** option un-maps and re-maps only logic cell, also referred to as LCELL or LE primitives, and regular I/O primitives (which may contain registers). Double data rate (DDR) I/O primitives, memory primitives, digital signal processing (DSP) primitives, and logic cells in carry/cascade chains are not touched. Logic specified in an encrypted Verilog Quartus Mapping file or an Electronic Design Interchange Format file, such as third-party intellectual property (IP), is not touched.

Turning on this option can cause drastic changes to the node names in the Verilog Quartus Mapping file or Electronic Design Interchange Format file from your third-party synthesis tool, because the primitives in the atom netlist are being broken apart and then remapped within the Quartus II software. Registers can be minimized away and duplicates removed, but registers that are not removed have the same name after remapping.

Any nodes or entities that have the **Netlist Optimizations** logic option set to **Never Allow** are not affected during WYSIWYG primitive resynthesis. To apply this logic option, on the Assignments menu, click **Assignment Editor**. This option disables WYSIWYG resynthesis for parts of your design.

Gate-Level Register Retiming

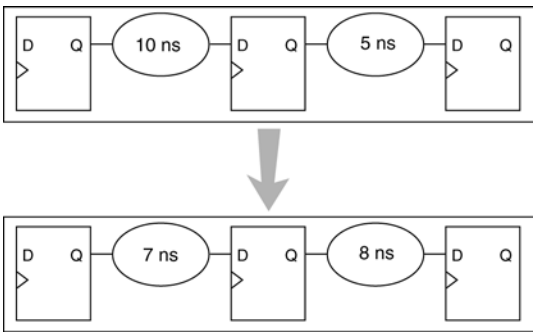
The **Perform gate-level register retiming** option enables movement of registers across combinational logic to balance timing, allowing the Quartus II software to trade off the delay between timing-critical paths and non-critical paths. See Figure 11–3 on page 11–6 for an example. This option can be used with the HardCopy® series, Stratix series, Cyclone series, MAX II, and APEX series device families. To set this option, on the Assignments menu, click **Settings**. In the **Category list**, select **Analysis & Synthesis Settings**, select **Synthesis Netlist Optimizations**. In the **Synthesis Netlist Optimizations** page, turn on **Perform gate-level register retiming**.

The functionality of your design is not changed when the **Perform gate-level register retiming** option is turned on. However, if any registers in your design have the **Power-Up Don't Care** logic option assigned, the values of registers during power-up may change due to this register and logic movement. The **Power-Up Don't Care** logic option is turned on globally by default. To change the default setting for this option, on the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**. In the **Analysis & Synthesis Settings** page, click **More Settings**.

You can set the **Power-Up Don't Care** logic option for individual registers or entities using the Assignment Editor. You can also specify a power-up value for individual registers or entities with the **Power-Up Level** logic option. Registers that are explicitly assigned power-up values are not combined with registers that have been explicitly assigned other values.

Figure 11–3 shows an example of gate-level register retiming where the 10 ns critical delay is reduced by moving the register relative to the combinational logic.

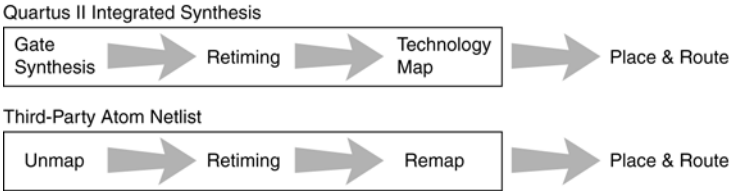
Figure 11–3. Gate-Level Register Retiming Diagram



Register retiming makes changes at the gate level. If you are using an atom netlist from a third-party synthesis tool, you must also use the **Perform WYSIWYG primitive resynthesis** option to un-map atom primitives to gates (so that register retiming can be performed) and then to re-map gates to Altera primitives. If your design uses Quartus II integrated synthesis, retiming occurs during synthesis before the design is mapped to Altera primitives. Megafunctions instantiated in a design are always synthesized using the Quartus II software.

The design flows for the case of integrated Quartus II synthesis and a third-party atom netlist are shown in Figure 11–4.

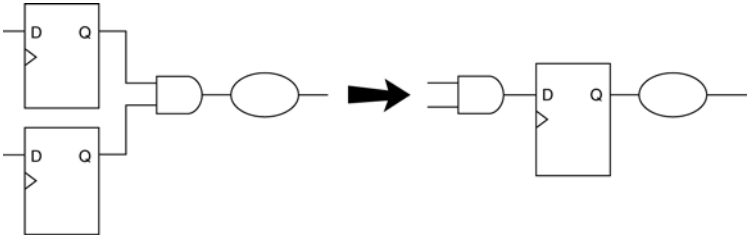
Figure 11–4. Gate-Level Synthesis



The gate-level register retiming option only moves registers across combinational gates. Registers are not moved across LCELL primitives instantiated by the user, memory blocks, DSP blocks, or carry/cascade chains that you have instantiated. Carry/cascade chains are always left intact when performing register retiming.

One benefit of register retiming is the ability to move registers from the inputs of a combinational logic block to the output, potentially combining the registers. In this case, some registers are removed, and one is created at the output, as shown in Figure 11–5.

Figure 11–5. Combining Registers with Register Retiming



The register retiming option can only move and combine registers in this type of situation if the following conditions are met:

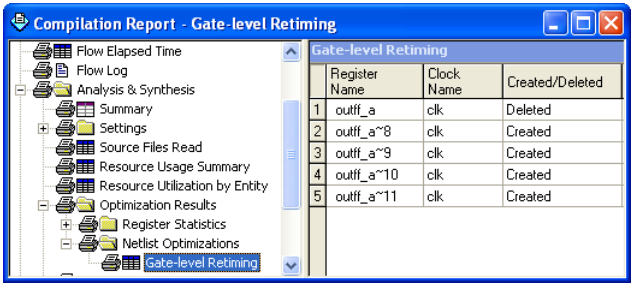
- All registers have the same clock signal
- All registers have the same clock enable signal
- All registers have asynchronous control signals that are active under the same conditions
- Only one register has an asynchronous load other than VCC or GND

Retiming can always create multiple registers at the input of a combinational block from a register at the output of a combinational block. In this case, the new registers have the same clock and clock enable. The asynchronous control signals and power-up level are derived from previous registers to provide equivalent functionality.

The **Gate-level Retiming** report provides a list of registers that were created and removed during register retiming. To access this report, on the Processing menu, click **Compilation Report**. In the **Analysis & Synthesis** list, select **Optimization Results**, select **Netlist Optimizations**, and click **Gate-level Retiming** (Figure 11–6).

The node names for these registers change during the retiming process.

Figure 11–6. Gate-Level Retiming Report



You can set the **Netlist Optimizations** logic option to **Never Allow** to prevent register movement during register retiming. This option can be applied either to individual registers or entities in the design using the Assignment Editor.

The following registers are not moved during gate-level register retiming:

- Registers that have any timing constraint other than global f_{MAX}, t_{SU}, or t_{CO}. For example, any node affected by a Multicycle or Cut Timing assignment is not moved.
- Registers that feed asynchronous control signals on another register.
- Registers feeding the clock of another register.
- Registers feeding a register in another clock domain.
- Registers that are fed by a register in another clock domain.
- Registers connected to serializer/deserializer (SERDES).
- Registers that have the **Netlist Optimizations** logic option set to **Never Allow**.

- Registers feeding output pins (without logic between the register and the pin).
- Registers fed by an input pin (without logic between register and input pin).
- Both registers in a direct connection from input pin-to-register-to-register if both registers have the same clock and the first register does not fan out to anywhere else. These registers are considered synchronization registers.
- Both registers in a direct connection from register-to-register if both registers have the same clock, the first register does not fan out to anywhere else, and the first register is fed by another register in a different clock domain (directly or through combinational logic). These registers are considered synchronization registers.

You can change the retiming behavior for a sequence of synchronization or meta-stability registers by changing the value of the **Retiming Meta-Stability Register Sequence Length** logic option. The value of this option indicates the number of synchronization registers that will not be moved during gate-level register retiming. The default value is 2. To set the value to any number greater than 0, on the Assignments menu, click Settings. In the Settings dialog box, select **Analysis & Synthesis Settings** and click **More Settings**. A value of 1 means that any registers connected to the first register in a register-to-register connection can be moved during retiming. A value of $n > 1$ means that any registers in a sequence of length 1, 2,… n are not moved during gate-level register retiming as long as all of the following are true:

- The first register is fed either directly by a pin or by a register in another clock domain (directly or through combinational logic)
- All registers in the sequence have the same clock
- All but the last register feed the next register in the sequence directly and do not fan out to anywhere else

If you want to consider registers with any of these conditions for register retiming, you can override these rules by setting the **Netlist Optimizations** logic option to **Always Allow** for a given set of registers.

Allow Register Retiming to Trade-Off t_{SU}/t_{CO} with f_{MAX}

To determine whether the Quartus II compiler should attempt to increase f_{MAX} at the expense of t_{SU} or t_{CO} times, on the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**, and select **Synthesis Netlist Optimizations**. In the **Synthesis Netlist Optimizations** page, turn on **Allow register retiming to trade off Tsu/Tco with Fmax**. This option affects the optimizations performed due to the gate-level register retiming option.

When both the **Perform gate-level register retiming** and the **Allow register retiming to trade off Tsu/Tco with Fmax** options are turned on, retiming can affect registers that feed and are fed by I/O pins. If the latter option is not turned on, the retiming option does not touch any registers that connect to I/O pins through one or more levels of combinational logic.

Preserving Synthesis Netlist Optimization Results

The Quartus II software generates the same results on every compilation for the same source code and settings on a given system. Therefore, it is typically not necessary to take any steps to preserve your results from compilation to compilation. When changes are made to the source code or to the settings, you usually get the best results by allowing the software to compile without using any previous compilation results or location assignments. In some cases, if you avoid running **Analysis & Synthesis**, or **quartus_map**, and run the Fitter or another desired Quartus II executable instead, you can skip the synthesis stage of the compile.

You can use the incremental compilation feature to preserve synthesis results for a particular partition of your design by choosing a netlist type of post-synthesis.

You should use the incremental compilation flow to preserve compilation results instead of the LogicLock back-annotation flow described here.

For information about the incremental compilation design methodology, refer to the *Quartus II Incremental Compilation* chapter in volume 1 of the *Quartus II Handbook*.

If you wish, you may preserve the nodes resulting from netlist optimizations. Preserving the nodes may be required if you use the LogicLock flow to back-annotate placement and/or import one design into another. (Note that this is not needed if you use the incremental compilation design flow along with the LogicLock feature).

If you are using any Quartus II synthesis netlist optimization options, you can save your optimized results. To do so, on the Assignments menu, click **Settings**. In the **Category** list, select **Compilation Process Settings**. In the **Compilation Process Settings** page, turn on **Save a node-level netlist of the entire design into a persistent source file**. This option saves your final results as an atom-based netlist in Verilog Quartus Mapping file format. By default, the Quartus II software places the Verilog Quartus Mapping file in the **atom_netlists** directory under the current project directory. If you want to create a different Verilog Quartus Mapping file

using different Quartus II settings, on the Assignments menu, click **Settings**. In the **Category** list, select **Compilation Process Settings**. In the **Compilation Process Settings** page, change the **File name** setting.

If you are using the synthesis netlist optimizations (and not any physical synthesis optimizations), generating a Verilog Quartus Mapping file is optional. To lock down the location of all logic and device resources in the design with or without a Quartus II-generated Verilog Quartus Mapping file, on the Assignments menu, click **Back-Annotate Assignments** and specify the desired options. You should use back-annotated location assignments unless the design has been finalized. Making any changes to the design invalidates your back-annotated location assignments. If you need to make changes later on, use the new source HDL code as your input files, and remove the back-annotated assignments corresponding to the old code or netlist.

If you create a Verilog Quartus Mapping file and wish to recompile the design, use the new Verilog Quartus Mapping file as the input source file and turn off the synthesis netlist optimizations for the new compilation.

Physical Synthesis Optimizations

Traditionally, the Quartus II design flow has involved separate steps of synthesis and fitting. The synthesis step optimizes the logical structure of a circuit for area, speed, or both. The fitter then places and routes the logic cells to ensure critical portions of logic are close together and use the fastest possible routing resources. While this push-button flow produces excellent results, the synthesis stage is unable to anticipate the routing delays seen in the fitter. Since routing delays are a significant part of the typical critical path delay, performing synthesis operations with physical delay knowledge allows the tool to target its timing-driven optimizations at these parts of the design. This tight integration of the fitting and synthesis processes is known as physical synthesis.

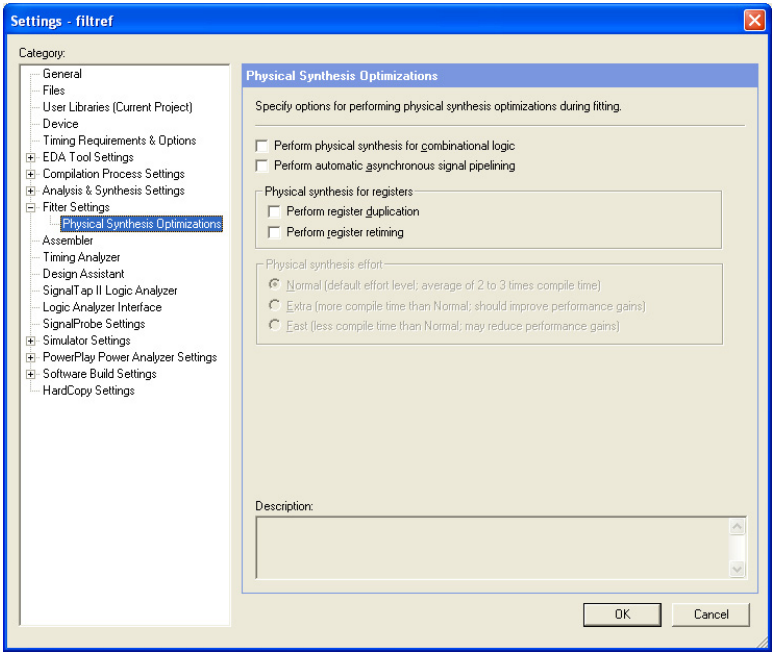
The following sections describe the physical synthesis optimizations available in the Quartus II software, and how they can help improve your performance results. Physical synthesis optimization options can be used with the Stratix and Cyclone series device families, as well as with HardCopy II devices.

If you are migrating your design to a HardCopy II device, you can target physical synthesis optimizations to the FPGA architecture in the FPGA-first flow or to the HardCopy II architecture in the HardCopy-first flow. The optimizations are mapped to the other device architecture during the migration process. Note that you cannot target optimizations to optimize for both device architectures individually because doing so would result in a different post-fitting netlist for each device.

For more information about using physical synthesis with HardCopy devices, refer to the *Quartus II Support of HardCopy Series Devices* chapter in volume 1 of the *Quartus II Handbook*.

To view and modify the physical synthesis optimization options, on the Assignments menu, click **Settings**. In the **Category** list, select **Fitter Settings** and select **Physical Synthesis Optimizations** as shown in Figure 11–7.

Figure 11–7. Physical Synthesis Optimization Settings



The physical synthesis optimizations are split into two groups: those that affect only combinational logic and not registers, and those that can affect registers. The options are split to allow you to keep your registers intact for formal verification or other reasons.

The following physical synthesis optimizations are available:

- Physical synthesis for combinational logic
- Automatic asynchronous signal pipelining
- Physical synthesis for registers:
  - Register duplication
  - Register retiming

You can control the effect of physical synthesis with the **Physical synthesis effort** option. The default selection is **Normal**. The **Extra** effort setting uses extra compilation time to try to achieve extra circuit performance, while the **Fast** effort setting uses less compilation time than **Normal** but may not achieve the same gains.

All Physical Synthesis optimizations write results to the **Netlist Optimizations** report. To access this report, on the Processing menu, click **Compilation Report**. In the **Category** list, select **Fitter** and select **Compilation Report**. This report provides a list of atom netlist files that were modified, created, and deleted during physical synthesis.

The node names for these atoms change during the physical synthesis process.

Nodes or entities that have the **Netlist Optimizations** logic option set to **Never Allow** are not affected by the physical synthesis algorithms. To access this logic option, on the Assignments menu, click **Assignment Editor**. Use this option to disable physical synthesis optimizations for parts of your design.

Automatic Asynchronous Signal Pipelining

The **Perform automatic asynchronous signal pipelining** option on the **Physical Synthesis Optimizations** page in the **Fitter Settings** section of the **Settings** dialog box allows the Quartus II fitter to perform automatic insertion of pipeline stages for asynchronous clear and asynchronous load signals during fitting when these signals negatively affect performance. You can use this option if asynchronous control signal recovery and removal times are not achieving their requirements.

This option improves performance for designs in which asynchronous signals in very fast clock domains cannot be distributed across the chip fast enough due to long global network delays. This optimization performs automatic pipelining of these signals, while attempting to minimize the total number of registers inserted.

The **Perform automatic asynchronous signal pipelining** option adds registers to nets driving the asynchronous clear or asynchronous load ports of registers. This adds register delays (adds latency) to the reset, adding the same number of register delays for each destination using the reset, changing the behavior of the signal in the design. Therefore this option should only be used when adding latency to reset signals does not violate any design requirements. This option also prevents the promotion of signals to global routing resources.

The Quartus II software performs automatic asynchronous signal pipelining only if **Recovery/Removal Analysis** is enabled. Pipelining is allowed only on asynchronous signals that have the following properties:

- The asynchronous signal is synchronized to a clock (a synchronization register drives the signal)
- The asynchronous signal fans-out only to asynchronous control ports of registers

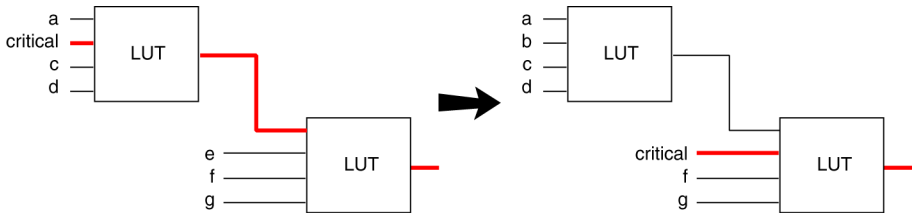
To access the **Recovery/Removal Analysis** option, on the Assignments menu, click **Settings**. In the **Category list**, select **Timing Requirements & Options**. On the Timing Requirements & Options page, click **More Settings**.

The Quartus II software does not perform automatic asynchronous signal pipelining on asynchronous signals that have the **Netlist Optimization logic** option set to **Never Allow**.

Physical Synthesis for Combinational Logic

To resynthesize the design and reduce delay along the critical path using the Quartus II fitter, on the Assignments menu, click **Settings**. In the **Category** list, select **Fitter Settings** and select **Physical Synthesis Optimizations**. In the **Physical Synthesis Optimizations** page, click **Perform physical synthesis for combinational logic**. The software can accomplish this type of optimization by swapping the look-up table (LUT) ports within LEs so that the critical path has fewer layers through which to travel. See Figure 11–8 for an example. This option also allows the duplication of LUTs to enable further optimizations on the critical path.

Figure 11–8. Physical Synthesis for Combinational Logic



In the first case, the critical input feeds through the first LUT to the second LUT. The Quartus II software swaps the critical input to the first LUT with an input feeding the second LUT. This reduces the number of LUTs contained in the critical path. The synthesis information for each LUT is altered to maintain design functionality.

The **Physical synthesis for combinational logic** option affects only combinational logic in the form of LUTs. The registers contained in the affected logic cells are not modified. Inputs into memory blocks, DSP blocks, and I/O elements (IOEs) are not swapped.

The Quartus II software does not perform combinational optimization on logic cells that have the following properties:

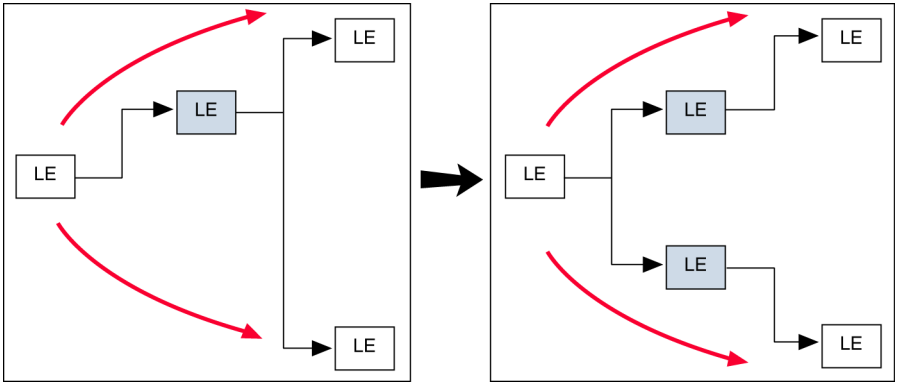
- Are part of a chain
- Drive global signals
- Are constrained to a single logic array block (LAB) location
- Have the **Netlist Optimizations** option set to **Never Allow**

If you want to consider logic cells with any of these conditions for physical synthesis, you can override these rules by setting the **Netlist Optimizations** logic option to **Always Allow** on a given set of nodes.

Physical Synthesis for Registers—Register Duplication

The **Perform register duplication** fitter option on the **Physical synthesis Optimizations** page in the **Fitter Settings** section of the **Settings** dialog box allows the Quartus II fitter to duplicate registers based on fitter placement information. Combinational logic can also be duplicated when this option is enabled. A logic cell that fans out to multiple locations can be duplicated to reduce the delay of one path without degrading the delay of another. The new logic cell may be placed closer to critical logic without affecting the other fan-out paths of the original logic cell. Figure 11–9 shows an example of register duplication.

Figure 11–9. Register Duplication



The Quartus II software does not perform register duplication on logic cells that have the following properties:

- Are part of a chain
- Contain registers that drive asynchronous control signals on another register
- Contain registers that drive the clock of another register
- Contain registers that drive global signals
- Contain registers that are constrained to a single LAB location
- Contain registers that are driven by input pins without a t_{SU} constraint
- Contain registers that are driven by a register in another clock domain
- Are considered virtual I/O pins
- Have the **Netlist Optimizations** option set to **Never Allow**

For more information about virtual I/O pins, see the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook.*

If you want to consider logic cells that meet any of these conditions for physical synthesis, you can override these rules by setting the **Netlist Optimizations** logic option to **Always Allow** on a given set of nodes.

Physical Synthesis for Registers—Register Retiming

The **Perform register retiming** fitter option in the **Physical Synthesis Optimizations** page in the **Fitter Settings** section of the **Settings** dialog box allows the Quartus II fitter to move registers across combinational logic to balance timing. This option enables algorithms similar to the **Perform gate-level register retiming** option (see "Gate-Level Register Retiming" on page 11–5). This option applies to the atom level (registers and combinational logic have already been placed into logic cells), and it compliments the synthesis gate-level option.

The Quartus II software does not perform register retiming on logic cells that have the following properties:

- Are part of a cascade chain
- Contain registers that drive asynchronous control signals on another register
- Contain registers that drive the clock of another register
- Contain registers that drive a register in another clock domain
- Contain registers that are driven by a register in another clock domain
- Contain registers that are constrained to a single LAB location
- Contain registers that are connected to SERDES
- Are considered virtual I/O pins
- Registers that have the **Netlist Optimizations** logic option set to **Never Allow**

For more information about virtual I/O pins, refer to the *LogicLock Design Methodology* chapter in volume 2 of the *Quartus II Handbook*.

If you want to consider logic cells that meet any of these conditions for physical synthesis, you can override these rules by setting the **Netlist Optimizations** logic option to **Always Allow** on a given set of registers.

Preserving Your Physical Synthesis Results

Given the same source code and settings on a given system, the Quartus II software generates the same results for every compilation. Therefore, it is typically not necessary to take any steps to preserve your results from compilation to compilation. When changes are made to the source code or to the settings, you usually get the best results by allowing the software to compile without using any previous compilation results or location assignments. However, if you do wish to preserve the compilation results, make sure to follow the guidelines outlined in this section.

You can use the incremental compilation feature to preserve fitting results for a particular partition of your design by choosing a netlist type of post-fit.

You should use the incremental compilation flow to preserve compilation results instead of the LogicLock back-annotation flow described here.

For information about the incremental compilation design methodology, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

If you wish, you can preserve the nodes resulting from physical synthesis. Preserving the nodes may be required if you use the LogicLock flow to back-annotate placement and/or import one design into another. (Note that this is not needed if you use the incremental compilation design flow along with the LogicLock feature).

If you are using any Quartus II physical synthesis optimization options, you can save the nodes in your optimized result using the **Save a node-level netlist into a persistent source file (Verilog Quartus Mapping File)** option on the **Compilation Process Settings** page in the **Settings** dialog box. This option saves your final results as an atom-based netlist in Verilog Quartus Mapping file format. By default, the Quartus II software places the Verilog Quartus Mapping file in the **atom_netlists** directory under the current project directory. If you want to create a different Verilog Quartus Mapping file using different Quartus II settings, you may do so by changing the **File name** setting on the **Compilation Process Settings** page in the **Settings** dialog box.

If you are using the physical synthesis optimizations and you wish to lock down the location of all LEs and other device resources in the design using the **Back-Annotate Assignments** command, a Verilog Quartus Mapping file netlist is required to preserve the changes that were made to your original netlist. Since the physical synthesis optimizations depend on the placement of the nodes in the design, back-annotating the placement changes the results from physical synthesis. Changing the results means that node names are different, and your back-annotated locations are no longer valid. To access this option, on the Assignments menu, click **Back-Annotate Assignments**.

You should not use a Quartus II-generated Verilog Quartus Mapping file or back-annotated location assignments with physical synthesis optimizations unless the design has been finalized. Making any changes to the design invalidates your physical synthesis results and back-annotated location assignments. If you need to make changes later, use the new source HDL code as your input files, and remove the back-annotated assignments corresponding to the Quartus II-generated Verilog Quartus Mapping file.

To back-annotate logic locations for a design that was compiled with physical synthesis optimizations, first create a Verilog Quartus Mapping file. When recompiling the design with the hard logic location assignments, use the new Verilog Quartus Mapping file as the input source file and turn off the physical synthesis optimizations for the new compilation.

If you are importing a Verilog Quartus Mapping file and back-annotated locations into another project that has any **Netlist Optimizations** turned on, it is important to apply the **Netlist Optimizations** = **Never Allow** constraint, to make sure node names don't change, otherwise the back-annotated location or LogicLock assignments are invalid.

You should use the incremental compilation flow to preserve compilation results instead of using logic back-annotation.

Applying Netlist Optimization Options

Netlist optimizations options can have various effects on different designs. Designs that are well coded or have already been restructured to balance critical path delays may not see a noticeable difference in performance.

To obtain optimal results when using netlist optimization options, you may need to vary the options applied to find the best results. By default, all options are off. Turning on additional options leads to the largest effect on the node names in the design. Take this into consideration if you are using a LogicLock or verification flow such as the SignalTap II logic analyzer or formal verification that requires fixed or known node names. On average, applying all of the **physical synthesis** options at the **Extra** effort level produces the best results for those options, but adds significantly to the compilation time. You can also use the **Physical synthesis effort** option to decrease the compilation time.

The synthesis netlist optimizations typically do not add much compilation time, relative to the overall design compilation time.

When you are using a third-party atom netlist (Verilog Quartus Mapping file or Electronic Design Interchange Format file), the **WYSIWYG Primitive Resynthesis** option must be turned on in order to use the **Gate-level Register Retiming** option.

The Design Space Explorer (DSE) tool command language (Tcl)/Tk script is provided with the Quartus II software to automate the application of various sets of netlist optimization options.

For more information about using the DSE script to run multiple compilations, refer to the *Design Space Explorer* chapter in volume 2 of the *Quartus II Handbook*. For information about typical performance results using combinations of netlist optimization options and other optimization techniques, refer to the *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The *Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

You can specify many of the options described in this section either on an instance, or at a global level, or both.

Use the following Tcl command to make a global assignment:

```
set_global_assignment -name <QSF variable name> <value>
```

Use the following Tcl command to make an instance assignment:

```
set_instance_assignment -name <QSF variable name> <value> -to <instance name>
```

Synthesis Netlist Optimizations

Table 11–1 lists the Quartus II Settings File (**.qsf**) variable name and applicable values for the settings discussed in "Synthesis Netlist Optimizations" on page 11–3. The Quartus II Settings File variable name

is used in the Tcl assignment to make the setting along with the appropriate value. The Type column indicates whether the setting is supported as a global setting, an instance setting, or both.

Table 11–1. Synthesis Netlist Optimizations & Associated Settings

Setting Name	Quartus II Settings File Variable Name	Values	Type
Perform WYSIWYG Primitive Resynthesis	ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP	ON, OFF	Global, Instance
Optimization Technique	<*Device Family Name*>_OPTIMIZATION_TECHNIQUE	AREA, SPEED, BALANCED	Global, Instance
Perform Gate-Level Register Retiming	ADV_NETLIST_OPT_SYNTH_GATE_RETIME	ON, OFF	Global
Power-Up Don't Care	ALLOW_POWER_UP_DONT_CARE	ON, OFF	Global
Allow Register Retiming to trade off Tsu/Tco with Fmax	ADV_NETLIST_OPT_RETIME_CORE_AND_IO	ON, OFF	Global
Save a node-level netlist into a persistent source file	LOGICLOCK_INCREMENTAL_COMPILE_ASSIGNMENT	ON, OFF	Global
	LOGICLOCK_INCREMENTAL_COMPILE_FILE	<*filename*>	
Allow Netlist Optimizations	ADV_NETLIST_OPT_ALLOWED	"ALWAYS ALLOW", DEFAULT, "NEVER ALLOW"	Instance

Physical Synthesis Optimizations

Table 11–2 lists the Quartus II Settings File variable name and applicable values for the settings discussed in "Physical Synthesis Optimizations" on page 11–11. The Quartus II Settings File variable name is used in the Tcl assignment to make the setting, along with the appropriate value. The Type column indicates whether the setting is supported as a global setting, an instance setting, or both.

Table 11–2. Physical Synthesis Optimizations & Associated Settings (Part 1 of 2)

Setting Name	Quartus II Settings File Variable Name	Values	Type
Physical Synthesis for Combinational Logic	PHYSICAL_SYNTHESIS_COMBO_LOGIC	ON, OFF	Global
Automatic Asynchronous Signal Pipelining	PHYSICAL_SYNTHESIS_ASYNCHRONOUS_SIGNAL_PIPELINING	ON, OFF	Global

Table 11–2. Physical Synthesis Optimizations & Associated Settings (Part 2 of 2)

Setting Name	Quartus II Settings File Variable Name	Values	Type
Perform Register Duplication	PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION	ON, OFF	Global
Perform Register Retiming	PHYSICAL_SYNTHESIS_REGISTER_RETIMING	ON, OFF	Global
Power-Up Don't Care	ALLOW_POWER_UP_DONT_CARE	ON, OFF	Global, Instance
Power-Up Level	POWER_UP_LEVEL	HIGH, LOW	Instance
Allow Netlist Optimizations	ADV_NETLIST_OPT_ALLOWED	"ALWAYS ALLOW", DEFAULT, "NEVER ALLOW"	Instance
Save a node-level netlist into a persistent source file	LOGICLOCK_INCREMENTAL_COMPILE_ASSIGNMENT	ON, OFF	Global
	LOGICLOCK_INCREMENTAL_COMPILE_FILE	<*filename*>	

Incremental Compilation

For information about scripting and command line usage for incremental compilation as mentioned in "Preserving Synthesis Netlist Optimization Results" on page 11–10 or "Preserving Your Physical Synthesis Results" on page 11–17, refer to the *Quartus II Incremental Compilation* chapter in volume 1 of the *Quartus II Handbook*.

Back-Annotating Assignments

You can use the `logiclock_back_annotate` Tcl command to back-annotate resources in your design. This command can back-annotate resources in LogicLock regions, and resources in designs without LogicLock regions.

For more information about back-annotating assignments, see "Preserving Synthesis Netlist Optimization Results" on page 11–10 or "Preserving Your Physical Synthesis Results" on page 11–17.

The following Tcl command back-annotates all registers in your design.

```
logiclock_back_annotate -resource_filter "REGISTER"
```

The `logiclock_back_annotate` command is in the `backannotate` package.

Conclusion

Synthesis netlist optimizations and physical synthesis optimizations work in different ways to restructure and optimize your design netlist. Taking advantage of these Quartus II netlist optimizations can help improve your quality of results.

12. Design Space Explorer

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Introduction

The Quartus® II software includes many advanced optimization algorithms to help you achieve timing closure and reduce dynamic power. The various settings and parameters control the behavior of the algorithms. These options provide complete control over the Quartus II software optimization and power techniques.

Each FPGA design is unique. There is no standard set of options that always results in the best performance or power utilization. Each design requires a unique set of options to achieve optimal performance. This chapter describes the Design Space Explorer (DSE), a utility written in Tcl/Tk that automates finding the best set of options for your design. DSE explores the design space of your design by applying various optimization techniques and analyzing the results.

DSE Concepts

This section explains the concepts and terminology used by DSE.

Exploration Space & Exploration Point

Before DSE explores a design, DSE creates an exploration space, which consists of Synthesis and Fitter settings available in the Quartus II software. Each group of settings in an exploration space is referred to as a *point*. An exploration space contains one or more points. DSE traverses the points in the exploration space to determine optimal settings for your design.

Seed & Seed Sweeping

The Quartus II Fitter uses a seed to specify the starting value that randomly determines the initial placement for the current design. The seed value can be any non-negative integer value. Changing the starting value may or may not produce better fitting. However, varying the value of the seed or seed sweeping allows the Quartus II software to determine an optimal value for the current design.

DSE extends Fitter seed sweeping in exploration spaces by providing a method for sweeping through general compilation and Fitter parameters to find the best options for your design. You can run DSE in various exploration space modes, ranging from an exhaustive try-all-options-and-values mode to a mode that focuses on one parameter.

DSE Exploration

DSE compares all exploration point results with the results of a base compilation, generated from the initial settings that you specify in the original Quartus II project files. As DSE traverses all points in the exploration space, all settings, not explicitly modified by DSE, default to the base compilation setting. For example, if an exploration point turns on register retiming but does not modify the register packing setting, the register packing setting defaults to the value you specified in the base compilation.

DSE performs the base compilation with the settings you specified in the original Quartus II project. These settings are restored after DSE traverses all points in the exploration space.

General Description

You can use DSE in either the graphical user interface (GUI) or from a command line. To run DSE with the GUI, either click **Design Space Explorer** on the Tools menu in the Quartus II software, or at the command prompt, type:

```
quartus_sh --dse ↵
```

To run DSE from a command line, type the following command at the command prompt:

```
quartus_sh --dse -nogui [<options>] ↵
```

You can run DSE with the following options:

```
-archive
      -concurrent-compiles [0..6]
      -custom-file <filename>
      -decision-column <"column name">
      -exploration-space <"space">
      -ignore-failed-base
      -ignore-signalprobe
      -ignore-signaltap
      -llr-restructuring
      -lower-priority
      -lsf-queue <queue name>
      -nogui
      -optimization-goal <"goal">
      -project <project name>
      -revision <revision name>
      -run-power
      -search-method <"method">
      -seeds <seed list>
      -skip-base
      -slaves <"slave list">
      -stop-after-time <dd:hh:mm>
      -stop-after-zero-failing-paths
      -use-lsf
```

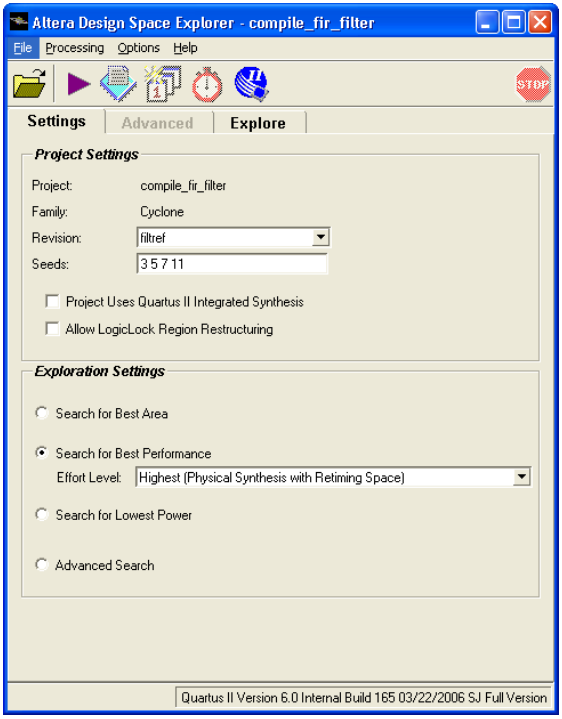
The DSE script is in the default Quartus II software installation in <*Quartus II installation directory*>**/common/tcl/apps/dse/dse.tcl** on the PC, Solaris, HP-UX, and Linux platforms. You can launch DSE using one of the following methods:

- On the Tools menu, click **Launch Design Space Explorer**.
- On Windows, select **Start** > **Programs** > **Altera** > **Design Space Explorer** or **Quartus II** <*version number*>.

For more information on DSE, launch the DSE GUI. On the Help menu, click **Contents** or press the **F1** key.

Figure 12–1 shows the DSE user interface. The **Settings** tab is divided into two sections: **Project Settings** and **Exploration Settings**.

Figure 12–1. DSE User Interface



Timing Analyzer Support

DSE supports both the Classic Timing Analyzer and the TimeQuest Timing Analyzer. You must set the timing analyzer prior to opening the project in DSE. Once the timing analyzer is set, DSE performs the design exploration with the selected timing analyzer that guides the fitter.

TimeQuest is launched directly from DSE if you set the default timing analyzer to TimeQuest.

DSE Flow

You can run DSE at any point in the design process. However, Altera recommends that you run DSE late in your design cycle when you are focusing on optimizing performance and power. The results gained from different combinations of optimization options may not persist over large changes in a design. Running DSE in signature mode (refer to "Signature Mode" on page 12–13) at the midpoint of your design cycle shows you the affect of various parameters such as the register packing logic option on your design.

DSE runs the Quartus II software for every compilation specified in the **Exploration Settings** options. DSE selectively determines the best settings for your design based on the **Optimization Goal** selected for the exploration. The Quartus II software always attempts to achieve all your timing requirements regardless of the Optimization Goal set in DSE. The Optimization Goal changes the metrics that DSE evaluates to determine if one compilation is better than another. Design Space Explorer does not change the behavior of the Quartus II software.

DSE reports the compilation that has the smallest slack. Specifying all timing requirements before you use DSE to explore your design is very important to ensure that DSE finds the optimal set of parameters for your design based on design criteria you set in your initial design.

You can change the initial placement configuration used by the Quartus II Fitter by varying the **Fitter Seed** value. You can enter seed values in the **Seeds** field of the DSE user interface.

You can set the seed value on the Assignments menu, click **Fitter Settings** in the **Settings** dialog box.

Compilation time increases as DSE exploration spaces become more comprehensive. Increased compilation time results from running several compilations and comparing the generated results with the original base compilation results.

For typical designs, varying only the seed value results in a 5% f_{MAX} increase. For example, when compiling with three different seeds, one-third of the time f_{MAX} does not improve over the initial compilation, one-third of the time f_{MAX} gets 5% better, and one-third of the time f_{MAX} gets 10% better.

DSE Support for Altera Device Families

DSE setting support varies across device families. To see the range of settings DES supports, click the **Advanced Search** radio button on the **Settings** tab, then select the **Advanced** tab to access the settings listed in the following categories:

- Exploration Space
- Optimization Goal
- Search Method

The following device families support all **Advanced** setting types:

- Stratix® II
- Stratix
- Stratix GX
- Cyclone™ II
- Cyclone
- MAX® II

The following device families support only the **Advanced Exploration Space** and **Optimization Goal** settings shown in Table 12–1:

- APEX™ 20K
- APEX 20KC
- APEX 20KE
- APEX II
- FLEX® 10K
- FLEX 10KA
- FLEX 10KE

Click the **Advanced Search** radio button on the **Settings** tab before you select the **Advanced** tab to access the settings in Table 12–1.

Table 12–1. Advanced Exploration Space Support for APEX 20K, APEX II & FLEX 10K Devices

Seed sweep	Area optimization space
Signature fitting effort level	Extra effort space
Extra effort for Quartus II Integrated Synthesis Projects	Custom space

DSE Project Settings

This section provides the following information about DSE project settings:

- Setting up the DSE work environment
- Specifying the revision
- Setting the initial seed
- Quartus II integrated synthesis
- Restructuring LogicLock regions

Setting Up the DSE Work Environment

From the DSE user interface, you can open a Quartus II project for a design exploration with either of the following actions:

- On the File menu, click **Open Project** and browse to your project.
- Use the **Open** icon to open a project.

Specifying the Revision

You can specify the revision to be explored with the **Revision** field in the DSE user interface. The **Revision** field is populated after the Quartus II project has been opened.

If no revisions were created in the Quartus II project, the default revision, which is the top-level entity, is used. For more information, refer to *Quartus II Project Management* chapter in volume 2 of the *Quartus II Handbook*.

Setting the Initial Seed

To specify the seed that DSE uses for an exploration, specify a non-negative integer value in the **Seed** box under **Project Settings** on the **Settings** tab. The seed value determines your design's initial placement in a Quartus II compilation.

To specify a range of seeds, type the low end of the range followed by a hyphen, followed by the high end of the range. For example, 2-5-DSE uses every seed in the range.

Restructuring LogicLock Regions

The **Allow LogicLock Region Restructuring** option allows DSE to modify LogicLock region properties in your design, if any exist. DSE applies the **Soft** property to LogicLock regions to improve timing. In addition, DSE can remove LogicLock regions that negatively affect the performance of the design.

Use the **Exploration Settings** list to select the type of exploration to perform: **Search for Best Area**, **Search for Best Performance**, **Search for Lowest Power**, or **Advanced Search**.

The "Exploration Space" on page 12–10 describes the type of explorations you can perform.

Search for Best Performance, Search for Best Area Options, or Search for Lowest Power Option

The **Search for Best Performance** option uses a predefined exploration space that targets performance improvements for your design. Depending on the device your design targets, you can select up to four predefined exploration spaces: **Low** (**Seed Sweep**), **Medium** (**Extra Effort Space**), **High (Physical Synthesis Space)**, and **Highest** (**Physical Synthesis with Retiming Space**). As you move from **Low** to **Highest**, the number of options explored by DSE increases, causing compilation time to increase.

The **Search for Lowest Power** option uses a predefined exploration space that targets overall power improvements for your design. When **Search for Lowest Power** is selected, DSE automatically runs the PowerPlay Power Analyzer for each point in the space. You must ensure that the PowerPlay Power Analyzer is configured correctly to ensure accurate results. DSE issues a warning if the confidence level for any power estimate is low.

The **Search for Best Area** option uses a predefined exploration space that targets device utilization improvements for your design.

Advanced Search Option

The **Advanced Search** option provides full control over the exploration space, the optimization goal for your design, and the search method used in a design exploration. Refer to "Performing an Advanced Search in Design Space Explorer" on page 12–9 for detailed information on how to set up and perform an **Advanced Search** in DSE.

You can use **Advanced Search** to define exploration spaces that are equivalent to the **Search for Best Area**, **Search for Lowest Power**, and **Search for Best Performance** options.

Quartus II Integrated Synthesis

The **Project Uses Quartus II Integrated Synthesis** option works only for designs that have been synthesized with Quartus II integrated synthesis. With this option turned on, DSE explores options that affect the synthesis stage of compilation.

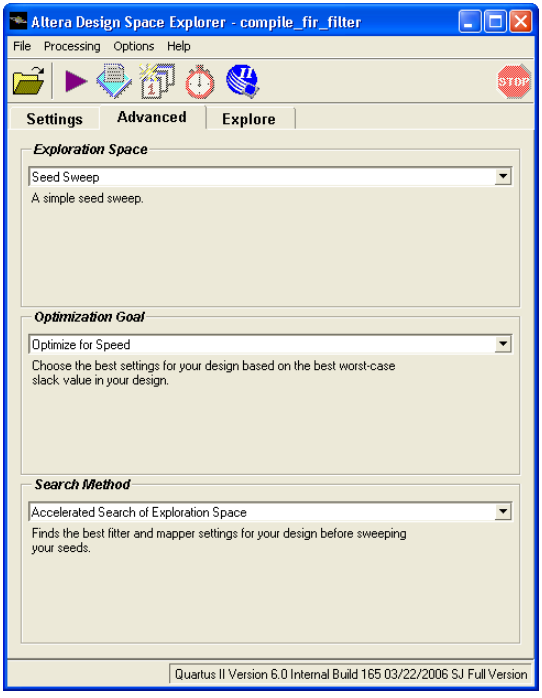
For more information on integrated synthesis options, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

Performing an Advanced Search in Design Space Explorer

You must make three exploration settings in the **Advanced Search** dialog box before exploring a design. These three settings, **Exploration Space**, **Optimization Goal**, and **Search Method**, are described in the following sections. Figure 12–2 shows the **Advanced Search** dialog box.

You can access the **Advanced** tab only after you open a Quartus II project in DSE and select **Advanced Search** on the **Settings** tab.

Figure 12–2. DSE Advanced Search Dialog Box



Exploration Space

The **Exploration Space** list controls the types of explorations that DSE performs on your design. DSE traverses the points in the exploration space, applying the settings to the design and comparing compilation results to determine the best settings for your design. DSE offers the following exploration space types:

- Seed Sweep
- Extra Effort Spaces
- Physical Synthesis Spaces
- Retiming Spaces
- Area Optimization Space
- Custom Space
- Signature mode—Power Optimization Spaces

Not all **Advanced** exploration space types are available for every device family. Refer to "DSE Support for Altera Device Families" on page 12–6 for **Advanced** exploration space support for various device families.

Compilation time increases proportionally to the breadth of the explorations. The exploration space compilation time increases with the number and type of exploration spaces DSE explores, especially with exploration space types that have more optimization options and parameters.

On the Options menu, click **Advanced**, and turn on **Save Exploration Space to File** to save an XML file representing the exploration space. DSE writes the exploration space to a file named **<***project name***>.dse** in the project directory. You can modify this file to create a custom exploration space.

For more information on using custom exploration spaces in DSE, refer to "Creating Custom Spaces for DSE" on page 12–21.

Seed Sweep

Enter the seed values in the **Seeds** field in the DSE user interface. There are no "magic" seeds. The variation between seeds is truly random, any non-negative integer value is as likely to produce good results. DSE defaults to seeds 3, 5, 7, and 11. The **Seed Sweep** exploration space does not change your netlist.

The **Seeds** field accepts individual seed values, for example, 2, 3, 4, and 5, or seed ranges, for example, 2-5.

Compilation time increases 1× for every seed value you specify. For example, if you enter five seeds, the compilation time increases to 5× the initial compilation time.

Extra Effort Spaces

The **Extra Effort Space** exploration space adds the **Register Packing** option to the exploration space done by the **Seed Sweep**. The **Extra Effort Space** exploration space also increases the Quartus II Fitter effort during placement and routing. However, the **Extra Effort Space** exploration space does not change your netlist.

Physical Synthesis Spaces

The **Physical Synthesis Space** exploration space adds physical synthesis options such as register retiming and physical synthesis for combinational logic to the options included in the **Extra Effort Space** exploration space. These netlist optimizations move registers in your design. Look-up tables (LUTs) are modified by these options. However, the design behavior is not affected by these options.

For more information about physical synthesis, refer to the *Netlist Optimizations & Physical Synthesis* chapter in volume 2 of the *Quartus II Handbook*.

The **Physical Synthesis for Quartus II Integrated Synthesis Projects** exploration space includes all the options in the **Physical Synthesis** exploration space and explores various Quartus II integrated synthesis optimization options. The **Physical Synthesis for Quartus II Integrated Synthesis Projects** exploration space works only for designs that have been synthesized using Quartus II integrated synthesis software.

Retiming Space

The **Physical Synthesis with Retiming Space** exploration space includes all the options in the **Physical Synthesis Space** exploration space and explores register retiming. Register retiming can move registers in your design.

The **Physical Synthesis Retiming Space for Quartus II Integrated Synthesis Projects** exploration space includes all the options in **Physical Synthesis with Retiming Space** exploration space, and also explores various Quartus II integrated synthesis optimization options. The **Physical Synthesis with Retiming Space for Quartus II Integrated Synthesis Projects** exploration space works only for designs that have been synthesized using the Quartus II integrated synthesis.

Area Optimization Space

The **Area Optimization Space** exploration space explores options that affect logic cell utilization for your design. These options include register packing and **Optimization Technique** set to **Area**.

Custom Space

Use the **Custom Space** exploration space to selectively explore the effects of various optimization options on your design. This exploration space gives you complete control over which options are explored and in what mode. In the **Custom Space** mode you can explore all optimization options available in DSE.

For a summary of the settings adjusted by each exploration space, refer to Table 12–2.

Table 12–2. Summaries of Exploration Spaces *Note (1)*

Search Type	Exploration Spaces					
	Seed Sweep	Extra Effort	Physical Synthesis	Retiming	Area Optimization	Custom
Analysis & Synthesis Settings						
Optimization technique			✓	✓	✓	✓
Perform WYSIWYG resynthesis			✓	✓	✓	✓
Perform gate-level register retiming				✓		✓
Fitter Settings						
Fitter seed	✓	✓	✓	✓	✓	✓
Register packing		✓	✓	✓	✓	✓
Increase PowerFit fitter effort		✓	✓	✓		✓
Perform physical synthesis for combinational logic			✓	✓		✓
Perform register retiming				✓		✓

Note to Table 12–2:
(1) For exploration spaces that includes Quartus II Integrated Synthesis Projects, DSE increases the synthesis effort.

For more information about using custom exploration spaces with DSE, refer to "Creating Custom Spaces for DSE" on page 12–21.

Signature Mode

In **Signature** mode, DSE analyzes the f_{MAX}, slack, compilation time, and area trade-offs of a single parameter. Running the single parameter over multiple seeds, DSE reports the average of the resulting values. With this information you gain a better understanding of how that parameter affects your design. There are four signature mode settings in DSE:

- Signature: Fitting Effort Level
- Signature: Netlist Optimizations
- Signature: Fast Fit
- Signature: Register Packing

Each setting explores a specific optimization option for your design. For example, in **Signature: Register Packing** mode, DSE explores the **Auto Packed Registers** logic option with its four settings (**OFF, Normal**, **Minimized Area**, and **Minimize Area with Chains**), and reports the effects of each on your design.

Optimization Goal

Design metrics are extremely important in exploring your design, whether the metric is performance, logic utilization, or a combination of both. These metrics allow you to determine which compilation is best, based on the design requirements. By specifying options in the **Optimization Goal** settings, you specify your optimization design goals. DSE then uses the **Optimization Goal** settings to determine the best compilation results. Table 12–3 summarizes the six available optimization settings.

Table 12–3. Optimization Goal Settings

Setting	Description
Optimize for Speed	The exploration point containing the smallest worst-case slack value is selected as the best run.
Optimize for Area	The exploration point containing the lowest logic cell count is selected as the best run
Optimize for Power	The exploration point containing the lowest thermal power dissipation, and, if possible, a positive worst-case slack value, is selected as the best run.
Optimize for Negative Slack and Failing Path	The exploration point containing the best average negative worst-case slack and lowest number of failing paths is selected as the best run.
Optimize for Average Period	The exploration point containing the highest average period in a multiclock design is selected as the best run.
Optimize for Quality Fit	The exploration point containing the highest quality of fit is selected as the best run.

Quality of Fit (QoF)

Quality of Fit (QoF) is a better evaluation of fit than traditional worst-case slack metrics, because QoF considers all timing domains. QoF is not susceptible to the common mistake of accepting a fit because it has marginally better worst-case slack than other marginal timing domains with much worse slack. For example, the traditional worst-case slack metric favors a fit that achieves -2 ns slack for clock A and -5 ns slack for clock B, over a fit that achieves 1 ns slack for clock A and -5.5 ns slack for clock B. By applying a piece-wise linear function to each domain slack value, QoF ensures that large improvements in domains with ample slack do not unnecessarily skew the overall quality assessment of the fit.

To achieve a representative QoF value, ensure that slack values from domains that are easily meeting timing requirements do not offset the slack values from domains that are marginally meeting timing requirements. To correlate these values correctly, DSE applies a piece-wise linear function to the individual slack values before they are added together. This function reduces the improvement per unit of additional slack in a domain, as the domain slack improves. For example, the improvement of 100 ps in a domain that begins with 0 ns of slack is weighted more significantly than a 100 ps improvement in a domain that begins with 10 ns of slack.

To calculate the QoF for a design, use the sum of worst- case slack values for all timing domains reported by timing analysis. Timing domains include: Clock Setup, Clock Hold, t_{SU}, t_{CO}, t_{PD}, t_H, min t_{CO}, min t_{PD}, and other timing parameters. For example, if clock A has a Clock Setup slack of -500 ps, and clock B has a Clock Setup slack of 200 ps, the QoF for these two domains is -700 ps. The higher the QoF value reported, the better the QoF.

The QoF can be calculated for every design by entering the following Tcl command in the Tcl console:

```
source [file join $::quartus(binpath) tcl_scripts dse
calculate_quality_of_fit.tcl]
```

All variables in the above statement are predefined; type the statement as shown without any variable substitution.

Search Method

The **Search Method** setting allows you to control the breadth of the search that DSE performs. DSE provides two search methods: **Exhaustive search of exploration space** and **Accelerated search of exploration space**. These search methods are described in Table 12–4.

Table 12–4. Search Methods

Search Method	Description
Exhaustive search of exploration space	Applies all settings available in the exploration space to all seeds specified. This search method yields optimal settings for your design, but this search requires the most time.
Accelerated search of exploration space	Finds the best exploration space for your design by first determining the best settings and then sweeping the settings across all seeds specified.

DSE Flow Options

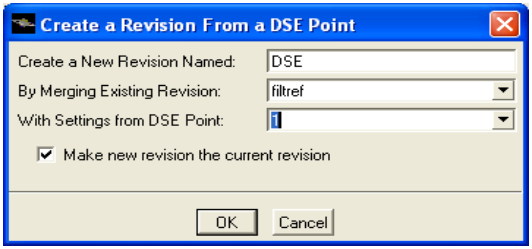
You can control the configuration of DSE with the following options:

- Create a Revision from a DSE Point
- Stop If Zero Failing Paths are Achieved
- Continue Exploration Even If Base Compilation Fails
- Run Quartus II PowerPlay Power Analyzer During Exploration
- Archive All Compilations
- Stop Flow After Time
- Save Exploration Space to File
- Ignore SignalTap & SignalProbe Settings
- Skip Base Analysis & Compilation If Possible
- Lower Priority of Compilation Threads
- DSE Configuration File

Create a Revision from a DSE Point

After you have performed a design exploration with DSE, a Quartus II revision can be made from any exploration point. This option facilitates the creation of multiple revisions based on the same space point for further optimization within the Quartus II software. Figure 12–3 shows the **Create a Revision From a DSE Point** dialog box.

Figure 12–3. Create a Revision from a DSE Point



The criteria DSE uses to determine the best space point in an exploration is known as the **Decision** column. As DSE explores a design space, the best exploration point changes according to the following inequality:

<Current Decision Column Value> > <Previous Decision Column Value>

By default, DSE uses worst-case slack as the **Decision** column for an exploration. The worst-case slack **Decision** column is the greatest slack value in an exploration, which can be I/O timing or clock slack values. You can change the **Decision** column on the Options menu. On the Options menu, click **Advanced**, and select **Change Decision Column**. Table 12–5 lists the available **Decision** columns. The **Decision** column can be any column within the Quartus II Timing Analyzer Report.

Table 12–5. DSE Change Decision Columns

Decision Column Name	Description
Worst-case slack (default)	Determines best exploration point on worst-case slack in the exploration space.
Clock Setup: '*<clock name>*': Slack	Determines best exploration point on the *<clock name>* specified.
Clock Setup: '*': Slack	Determines best exploration point on all clocks.
Worst-case minimum t_{CO} Slack	Determines best exploration point on worst case minimum t_{CO} slack.
Worst-case t_H Slack	Determines best exploration point on worst-case t_H slack.
Worst-case t_{SU} Slack	Determines best exploration point on worst case t_{SU} slack.
<any column name>	Determines best exploration point on any column available in the Quartus II timing analysis report file.

Stop If Zero Failing Paths are Achieved

Instructs DSE to stop exploring the space after it encounters any point, including the base point, that has zero failing paths. DSE uses the failing path count reported in the **All Failing Paths report** column to make this decision.

Continue Exploration Even If Base Compilation Fails

With the **Continue Exploration Even If Base Compilation Fails** option turned on, DSE continues the exploration even when a design compilation error occurs. For example, if timing settings are not applied to your design, a DSE error occurs. To cause DSE to continue with the exploration instead of halting when an error occurs, turn on this option.

Run Quartus II PowerPlay Power Analyzer During Exploration

Turn on **Run Quartus II PowerPlay Power Analyzer During Exploration** to invoke the Quartus II PowerPlay Analyzer for every exploration performed by DSE. Using this option can help you debug your design and determine trade-offs between power requirements and performance optimization.

Archive All Compilations

Turn on **Archive All Compilations** to create a Quartus II Archive File (.**qar**) for each compilation. These archive files are saved to the **dse** directory in the design's working directory.

Stop Flow After Time

Turn on **Stop Flow After Time** to stop further exploration after a specified number of days, hours, and/or minutes.

Exploration time might exceed the specified value because DSE does not stop in the middle of a compilation.

Save Exploration Space to File

Turn on **Save Exploration Space to File** to write out a <*project name*>**.dse** file containing all options explored by DSE. You can use or modify this file to perform a custom exploration.

Ignore SignalTap & SignalProbe Settings

DSE uses advanced physical synthesis options that are not compatible with the SignalTap® II or SignalProbe™ features. As a result, DSE issues an error message when a project is opened for exploration that has either SignalTap II or SignalProbe turned on. The error message is similar to the following:

```
Error Opening Project--------------------------
Project is using SignalProbe. Please turn off
SignalProbe before using this project with Design Space
Explorer or Ignore SignalProbe Setting in your Design
on the Options menu.
```

When the **Ignore SignalTap and SignalProbe Settings** option is turned on, DSE bypasses this check.

If you have already verified the design, you might save compilation time and improve resource utilization by turning this option on.

Skip Base Analysis & Compilation If Possible

Skip Base Analysis & Compilation If Possible allows the DSE to skip the Analysis & Elaboration stage or the compilation of the base point if base point compilation results are available from a previous Quartus II compilation.

Lower Priority of Compilation Threads

The **Lower Priority of Compilation Threads** option allows DSE to run the Quartus II executables with the `lower_priority` option. The `lower_priority` option lowers the priority of the Quartus II executable.

DSE Configuration File

Many options exist that allow you to customize the behavior of each DSE exploration. For example, you can specify seed values or a list of slave computers to be used for a distributed exploration run. Each time you close the DSE GUI it saves these values in a configuration file, **dse.conf**. The net time you launch the DSE GUI, it reads the values from **dse.conf** and restores the previous exploration settings.

Where the **dse.conf** file is stored varies based on the operating system that launches DSE. Table 12–6 specifies the locations where **dse.conf** files are stored based on operating system usage.

Table 12–6. DSE Configuration File Location

OS	File Location (default)	Comment
Windows	%APPDATA%/Altera/dse.conf	If the variable %APPDATA% is not defined, the configuration file is saved to **/.altera.quartus/dse.conf**
Unix	**~/.altera.quartus/dse.conf**	

Settings specified in the DSE command-line mode are not saved to a **dse.conf** configuration file.

DSE Advanced Information

This section covers advanced features that are available in DSE. These features increase the processing efficiency of design space exploration and provide further customization of the design space.

Computer Load Sharing in DSE Using Distributed Exploration

When you select **Distribute Compiles to Other Machines**, the DSE uses cluster computing technology to decrease exploration time. DSE uses multiple client computers to compile points in the specified exploration space. When you select the **Distributed DSE** option, DSE functions in one of the following operation modes:

- **Use LSF Resources**: DSE uses the Platform LSF grid computing technology to distribute exploration space points to a computing network.
- **Distribute Compiles to Other Machines** uses a Quartus II master process: DSE acts as a master and distributes exploration space points to client computers.

Distributed DSE Using LSF Resources

The easiest way to use distributed DSE technology is to submit the compilations to a preconfigured LSF cluster at your local site. For more information on LSF software, refer to **www.platform.com**, or contact your system administrator. Turn on **Use LSF resources** to enable this feature.You can specify an LSF queue when you select the **Configure Clients** option.

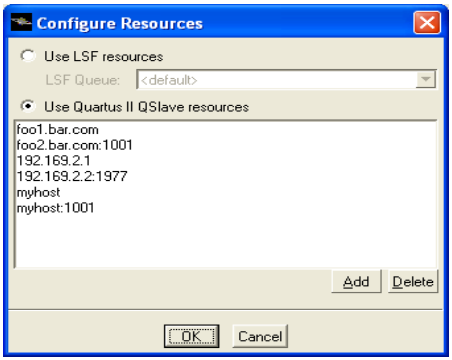
Distributed DSE Using a Quartus II Master Process

Before DSE can use computers in the local area network to compile points in the exploration space, you must create Quartus II software slave instances on the computers that will be used as clients. Type the following command at a command prompt on a client computer:

```
quartus_sh --qslave ↵
```

Repeating this on several computers creates a cluster of Quartus II software slaves for DSE to use. After you have created a set of Quartus II software slaves on the network, add the names of each slave computer in the **Configure Clients** dialog box. Figure 12–4 shows an example of client entries for a distributed search.

Figure 12–4. Client Entry in DSE



At the start of an exploration, DSE assumes the role of a Quartus II software master process and submits points to the slaves on the list to compile. If the list is empty, DSE issues an error and the search stops.

For more information on running and configuring Quartus slaves, at the command prompt type:

```
quartus_sh --help=qslave ↵
```

You must use the same version of the Quartus II software to run the slave processes as you use to run DSE. To determine which Quartus II software version that you are using to run DSE, select Help and click **About DSE.** Unexpected results can occur if you mix different Quartus II software versions when using the Distributed DSE search feature.

Concurrent Local Compilations

To reduce compilation time, DSE can compile exploration points concurrently. The **Concurrent Local Compilations** option allows you to specify the number of local compilations that DSE performs. For the **Concurrent Local Compilations** option, you can specify up to six concurrent compilations by choosing an integer value ranging from 1 through 6. You can use this option in conjunction with distributed processing. However, your system must have both the appropriate resources and licenses to perform concurrent compilations, and distributed processing. Multiprocessor or multicore systems are recommended for concurrent local compilations.

Concurrent Local Compilations require a separate Quartus II software license for each concurrent compilation. For example, if you compile four concurrent compilations, you need four licenses. Be sure before you choose a **Concurrent Local Compilations** value and start compilation that sufficient licenses are available.

Creating Custom Spaces for DSE

You can use custom spaces to explore combinations of options that are not in the predefined **Exploration Space** list. An exploration space is defined in an XML file. The following sections describe the tags you use to create a **Custom Space** that DSE can process.

A custom space is defined by the following three pairs of tags:

- `<DESIGNSPACE>` and `</DESIGNSPACE>`
- `<POINT>` and `</POINT>`
- `<PARAM>` and `</PARAM>`

DESIGNSPACE Tag

The `<DESIGNSPACE>` tag defines the start of the exploration space of a custom space. The end tag `</DESIGNSPACE>` defines the end of the exploration space. Both of these tags are required for all custom spaces.

POINT Tag

The `POINT` tag pair must occur within the `DESIGNSPACE` tag pair. The `<POINT` *<name>*=*<stage>* *enabled=”<value>”*`>` tag defines the start of the exploration point in a custom exploration space. The end tag `</POINT>` defines the end of the exploration point. The `POINT` also allows you to specify the *<stage>* value and whether a particular point is active for a particular DSE exploration.

The "<*stage*>" value in the POINT tag can be one of the following:

- **map**—indicates an Analysis & Synthesis setting change for that point
- **fit**—indicates a Fitter setting change for that point
- **seed**—indicates a Fitter seed change
- **llr**—indicates a LogicLock property change

The <*value*> value in the POINT tag can either be "**1**," indicating that for a specific stage the exploration point is active, or "**0**" for an inactive point.

An example of a POINT tag follows:

```
<POINT space="map" enabled="1">
...
</POINT>
```

The preceding point indicates a point that has Analysis & Synthesis setting changes and is active during Analysis & Synthesis.

PARAM Tag

The PARAM tag pair must occur within the POINT tag pair. The <PARAM name="<*parameter*>"> tag defines the start of a parameter to be modified for a particular exploration point. The end tag </PARAM> defines the end of the parameter. The **Analysis & Synthesis** settings and the "<*parameter*>" values are shown in Table 12–7.

Table 12–7. Analysis & Synthesis Settings *Note (1)*

Analysis & Synthesis Settings	Description	Value
STRATIX_OPTIMIZATION_TECHNIQUE	Type of optimization technique to use during the Analysis & Synthesis stage of a Quartus II software compilation for a Stratix device.	SPEED, AREA, BALANCED
CYCLONE_OPTIMIZATION_TECHNIQUE	Type of optimization technique to use during the Analysis & Synthesis stage of a Quartus II software compilation for a Cyclone device.	SPEED, AREA, BALANCED
ADV_NETLIST_OPT_SYNTH_GATE_RETIME	Gate-level register retiming.	OFF, ON
ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP	WYSIWYG primitive resynthesis.	OFF, ON
DSE_SYNTH_EXTRA_EFFORT_MODE	Controls the Quartus II software synthesis effort.	MODE_1, MODE_2, MODE_3

Note to Table 12–7:
(1) Not all Analysis & Synthesis settings are available for all device families.

Table 12–8 shows the Fitter settings. An example of a PARAM tag is shown below:

```
<PARAM name="ADV_NETLIST_OPT_SYNTH_GATE_RETIME"> ON </PARAM>
```

The point in the example above indicates that the Analysis and Synthesis setting gate-level retiming is turned on for the exploration space point.

Table 12–8. Fitter Settings *Note (1)*

Fitter Settings	Description	Value
AUTO_PACKED_REGISTERS_STRATIX	Register packing for Stratix devices	NORMAL, MINIMIZE_AREA, MINIMIZE_AREA_WITH_CHAINS
AUTO_PACKED_REG_CYCLONE	Register packing for Cyclone devices	OFF, MINIMIZE_AREA, MINIMIZE_AREA_WITH_CHAINS
INNER_NUM	PowerFit fitter effort level	{integer value}
PHYSICAL_SYNTHESIS_COMBO_LOGIC	Physical synthesis for combinational logic	OFF, ON
PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION	Physical synthesis for register duplication	OFF, ON
PHYSICAL_SYNTHESIS_REGISTER_RETIMING	Physical synthesis for register retiming	OFF, ON

Note to Table 12–8:
(1) Not all Fitter settings are available for all device families.

Simple Custom Space

The custom exploration space example below shows a simple custom exploration space performing a seed sweep with settings for the Analysis & Synthesis and the Fitter compilation stages.

```
<DESIGNSPACE>
 <POINT space="map" enabled="1">
  <PARAM name="CYCLONE_OPTIMIZATION_TECHNIQUE">SPEED</PARAM>
  <PARAM name="ADV_NETLIST_OPT_SYNTH_GATE_RETIME">ON</PARAM>
  <PARAM name="ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP">ON</PARAM>
  <PARAM name="STRATIX_OPTIMIZATION_TECHNIQUE">SPEED</PARAM>
 </POINT>
 <POINT space="fit" enabled="1">
  <PARAM name="PHYSICAL_SYNTHESIS_REGISTER_RETIMING">ON</PARAM>
  <PARAM name="PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION">
   ON</PARAM>
  <PARAM name="AUTO_PACKED_REG_CYCLONE">OFF</PARAM>
  <PARAM name="AUTO_PACKED_REGISTERS_STRATIX">OFF</PARAM>
  <PARAM name="SEED">3</PARAM>
  <PARAM name="PHYSICAL_SYNTHESIS_COMBO_LOGIC">ON</PARAM>
 </POINT>
</DESIGNSPACE>
```

The example defines a custom exploration space that has two points: one map exploration point which changes synthesis settings, and one fit exploration point which change the Quartus II Fitter settings. The map point sets the optimization technique to speed, turns on gate-level retiming, and turns on the WYSIWYG resynthesis. For the fit point, register retiming, register duplication, and physical synthesis for combinational logic are turned on; register packing is turned off; and a seed value of three is used.

Custom Space XML Schema

The following example contains an XML schema describing the XML format for custom exploration space files. You can use an advanced XML editor or XML verification tool to validate any custom exploration files against this schema.

```
<?xml version="1.0" encoding="UTF-8"?>
<xs:schema xmlns:xs="http://www.w3.org/2001/XMLSchema" elementFormDefault="qualified"
                    attributeFormDefault="unqualified">
    <xs:element name="DESIGNSPACE">
        <xs:annotation>
            <xs:documentation>The root element of a design space
                              description</xs:documentation>
        </xs:annotation>
        <xs:complexType>
            <xs:sequence minOccurs="0" maxOccurs="unbounded">
                <xs:element ref="POINT"/>
            </xs:sequence>
            <xs:attribute name="project" type="xs:string" use="optional"/>
```

13. LogicLock Design Methodology

QII52009-6.0.0

Introduction

Available exclusively in the Altera® Quartus® II software, the LogicLock™ feature enables you to design, optimize, and lock down your design one module at a time. With the LogicLock feature, you can independently create and implement each logic module into a hierarchical or team-based design. With this method, you can preserve the performance of each module during system integration. The LogicLock feature also facilitates the incremental compilation flow for block-based design available in the Quartus II software.

For more information on hierarchical and team-based design, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

The Quartus II software beginning with version 4.2 supports the LogicLock block-based design flow for all of the following device families:

- Stratix® II, Stratix, Stratix GX
- Cyclone™ series
- MAX® II, APEX®, APEX II
- Excalibur™
- Mercury™ (Mercury devices support only locked and fixed regions)

This chapter assumes that you are familiar with the basic functionality of the Quartus II software.

Improving Design Performance

The LogicLock flow helps you optimize and preserve performance. You can use the LogicLock flow to place modules, entities, or any group of logic into regions in a device's floorplan. LogicLock assignments can be hierarchical, which allows you to have more control over the placement and performance of each module as well as groups of modules.

In addition to hierarchical blocks, you can apply LogicLock constraints to individual nodes; for example, you can make a wildcard path-based LogicLock assignment on a critical path. This technique is useful if the critical path spans multiple design blocks.

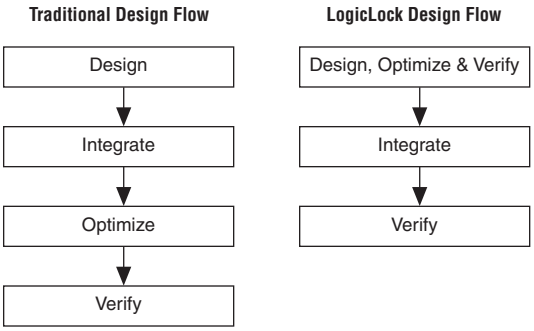
Although LogicLock constraints can improve performance, they can also degrade performance if they are not applied correctly.

The Quartus II LogicLock Methodology

The LogicLock design methodology lets you place the logic in each netlist file into a fixed or floating region in an Altera device. You can then maintain the placement and, if necessary, the routing of your blocks in the Altera device, thus retaining performance. Also, the LogicLock design methodology allows you to create design floorplans to obtain good results with the full incremental compilation flow in the Quartus II software.

Figures 13–1 compares the traditional design flow with the LogicLock design flow.

Figure 13–1. Traditional Design Flow Compared with Quartus II LogicLock Design Flow



For more information on block-based design with the LogicLock feature, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

Preserving Timing Results Using the LogicLock Flow

To preserve the timing results for a design module in the Quartus II software, you need to preserve the placement and routing information for all the logic in the design module. You can use one of two methods to preserve the placement and the routing results for a design module:

- You can use the LogicLock design methodology to back-annotate logic locations within a LogicLock region, which makes assignments to each node in the design.
- You can use the incremental compilation flow to preserve the fitting results for a design partition, and use the LogicLock design methodology to create a design floorplan that achieves good results.

For more information on block-based design with the LogicLock feature, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

When preserving logic placement in an Altera device, using LogicLock back-annotation, an atom netlist preserves the node names in subblocks of your design. An atom netlist contains design information that fully describes the submodule logic in terms of the device architecture. In the atom netlist, the nodes are fixed as Altera primitives and the node names do not change if the atom netlist does not change. If a node name changes, any placement information associated with that node, such as LogicLock assignments made when back-annotating a region, is invalid and ignored by the compiler.

If all the netlists are contained in one Quartus II project, use the LogicLock flow to back-annotate the logic in each region. If a design region changes, only the netlist associated with the changed region is affected. When you place and route the design using the Quartus II software, the software needs to re-fit only the LogicLock region associated with the changed netlist file.

Turn on the **Prevent further netlist optimization** option when back-annotating a region with the **Synthesis Netlist Optimizations** and/or **Physical Synthesis Optimization** options turned on. This sets the **Netlist Optimizations** option to **Never Allow** for all nodes in the region, avoiding the possibility of a node name change in the top-level design when the region is recompiled.

You may need to remove previously back-annotated assignments for a modified block because the node names may be different in the newly synthesized version. When you recompile with one new netlist file, the placement and assignments for the unchanged netlist files assigned to other LogicLock regions are not affected. Therefore, you can make changes to code in an independent block and not interfere with another designer's changes, even when all the blocks are integrated into the same top-level design.

With the LogicLock design methodology, you can develop and test submodules without affecting other areas of a design.

Designing with the LogicLock Feature

To design with the LogicLock feature, create a LogicLock region in a supported device and then assign logic to the region. The LogicLock region can contain any contiguous, rectangular block of device resources. After you optimize the logic placed within the boundaries of a region to achieve the required performance, you must back-annotate the region's contents to lock the logic placement and routing. Locking the placement and routing preserves the performance when you integrate the region with the rest of the design.

This section explains the basics of designing with the LogicLock regions, including:

- Creating LogicLock Regions
- Timing Closure Floorplan View
- LogicLock Region Properties
- Hierarchical (Parent and/or Child) LogicLock Regions
- Assigning LogicLock Region Content
- Excluded Resources
- Tcl Scripts
- Importing and Exporting LogicLock Regions
- Additional Quartus II LogicLock Design Features

Creating LogicLock Regions

There are four ways to create a LogicLock region:

- On the Assignments menu, click **LogicLock Regions Window**.
- Using the Create New Region button in the Timing Closure Floorplan.
- On the View menu, click **Project Navigator**. Use the **Hierarchy** tab.
- Tcl scripts.

LogicLock Regions Window

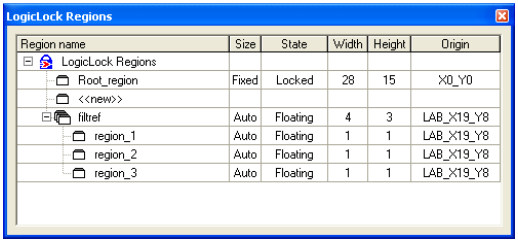
The LogicLock window is comprised of the LogicLock Regions window (Figure 13–2) and LogicLock Region Properties dialog box. Use the LogicLock Regions window to create LogicLock regions and assign nodes and entities to them. The dialog box provides a summary of all LogicLock regions in your design. In the LogicLock Regions window, you can modify a LogicLock region's size, state, width, height, and origin as well as whether the region is soft or reserved. When the region is back-annotated, the placement of the nodes within the region are relative to the region's origin, and the region's node placement during subsequent compilations is maintained.

The origin location varies based on device family. For Stratix II, Stratix, Stratix GX, Cyclone series, and MAX II devices, the LogicLock region's origin is located at the bottom-left corner of the region. For all other supported devices, the origin is located at the top-left corner of the region.

The LogicLock Regions window displays any LogicLock regions that contain illegal assignments in red. If you make illegal assignments, you can use the Repair Branch command to reset the assignments for the currently selected region and its descendents to legal default values.

For more information on the Repair Branch command, refer to "Repair Branch" on page 13–22.

Figure 13–2. LogicLock Regions Window



You can customize the LogicLock Regions window by dragging and dropping the various columns. The columns can also be hidden.

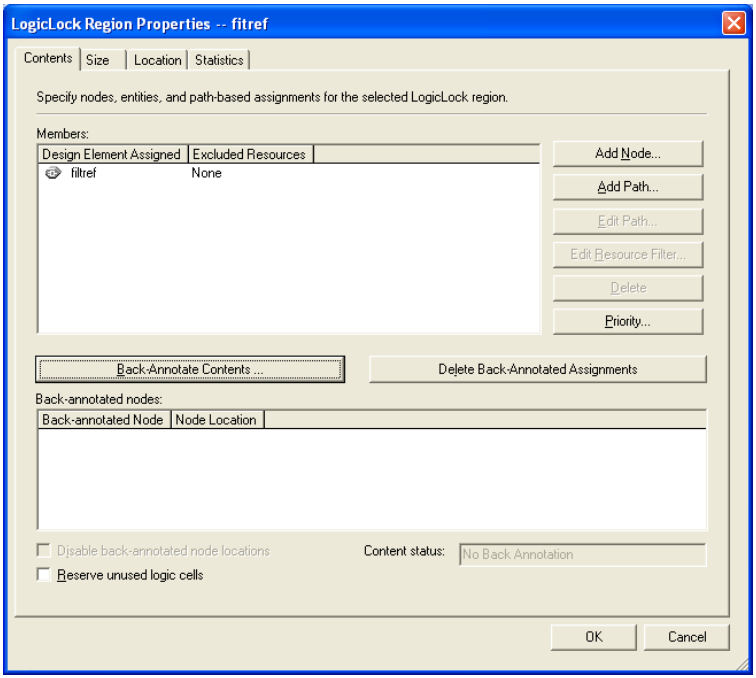
The **Soft** and **Reserved** columns are not shown by default.

For designs targeting Stratix II, Stratix, Stratix GX, Cyclone series, and MAX II devices, the Quartus II software automatically creates a LogicLock region that encompasses the entire device. This default region is labelled `Root_region`, and it is effectively locked and fixed.

Use the **LogicLock Region Properties** dialog box to obtain detailed information about your LogicLock region, such as which entities and nodes are assigned to your region and what resources are required (see Figure 13–3). The **LogicLock Region Properties** dialog box shows the properties of the current selected regions.

To open the **LogicLock Region Properties** dialog box, double-click any region in the LogicLock Regions window, or right-click the region and click **Properties**.

Figure 13–3. LogicLock Region Properties Dialog Box



To back-annotate the contents of your LogicLock regions, perform these steps:

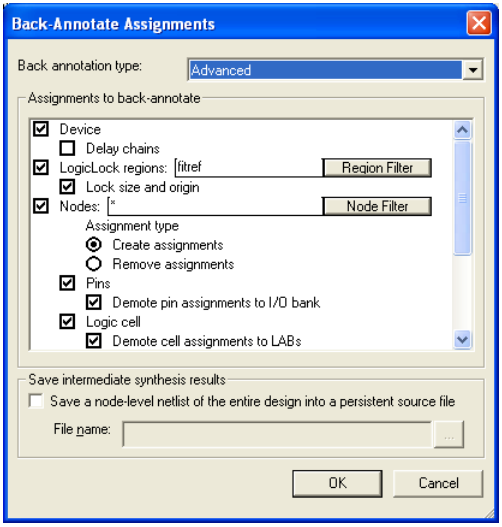
1. In the **LogicLock Region Properties** dialog box, click **Back-Annotate Contents**. The **Back-Annotate Assignments** dialog is shown.

2. In the **Back-Annotate Assignments** dialog box, in the **Back annotation type** list, select **Advanced** (Figure 13–4) and click **OK**.

3. In the **LogicLock Region Properties** dialog box, click **OK**.

If using the incremental compilation flow, logic back-annotation is not required. Preserve placement results using the Post-Fit Netlist Type instead of making placement assignments with back-annotation as described in this section.

Figure 13–4. Back-Annotate Assignments Dialog Box (Advanced Type)



You also can back-annotate routing within LogicLock regions to preserve performance of the regions. For more information on back-annotating routing, refer to "Back-Annotating Routing Information" on page 13–34.

When you back-annotate a region's contents, all of the design element nodes appear under **Back-annotated nodes** with an assignment to a device resource under **Node Location**, for example, logic array block (LAB), M512, M4K, M-RAM, and digital signal processing (DSP) block. Each node's location is the placement of the node after the last compilation. If the origin of the region changes, the node's location changes to maintain the same relative placement. This relative placement preserves the performance of the module. If cell assignments are demoted, then the nodes are assigned to LABs rather than directly to logic cells.

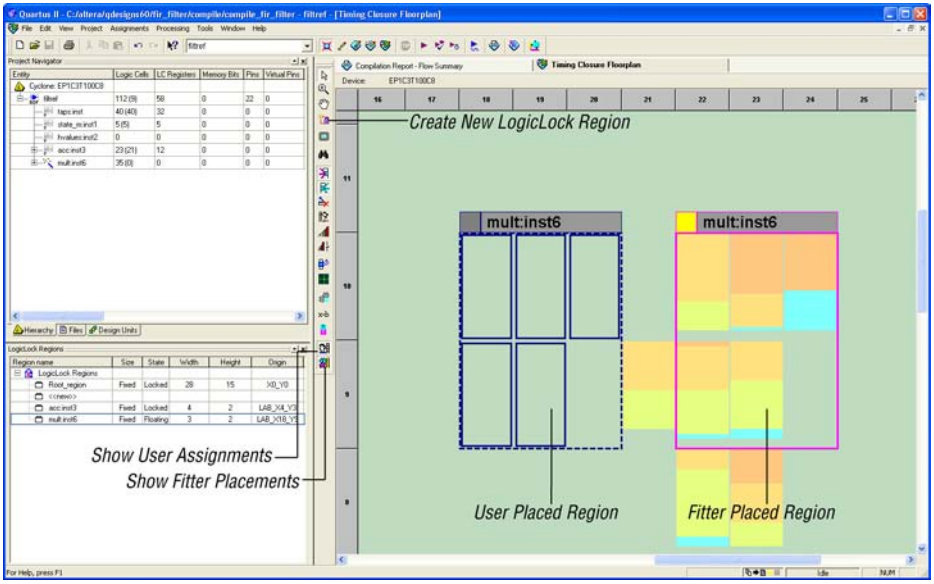
Timing Closure Floorplan Editor

The Timing Closure Floorplan Editor has toolbar buttons that are used to manipulate LogicLock regions as shown in Figure 13–5. You can use the **Create New LogicLock Region** button to draw LogicLock regions in the device floorplan.

The Timing Closure Floorplan Editor displays LogicLock regions when you select **Show User Assignments** or **Show Fitter Placements**. The type of region determines its appearance in the floorplan.

The Timing Closure Floorplan Editor differentiates between user assignments and fitter placements. When the **Show User Assignments** option is enabled in the Timing Closure Floorplan, you can see current assignments made to a LogicLock region. When the Fitter Placement option is enabled, you can see the properties of the LogicLock region after the last compilation. User-assigned LogicLock regions appear in the Floorplan Editor with a dark blue border (Figure 13–5). Fitter-placed regions appear in the Floorplan Editor with a magenta border.

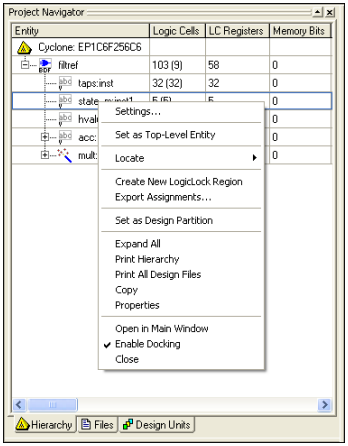
Figure 13–5. Floorplan Editor Toolbar Buttons



Design Hierarchy

After you perform either a full compilation or analysis and elaboration on the design, the Quartus II software displays the hierarchy of the design. On the View menu, click **Project Navigator**. With the hierarchy of the design fully expanded, as shown in Figure 13–6, To create a LogicLock region, with the design fully expanded, right-click on any design entity in the design and click **Create New LogicLock Region**.

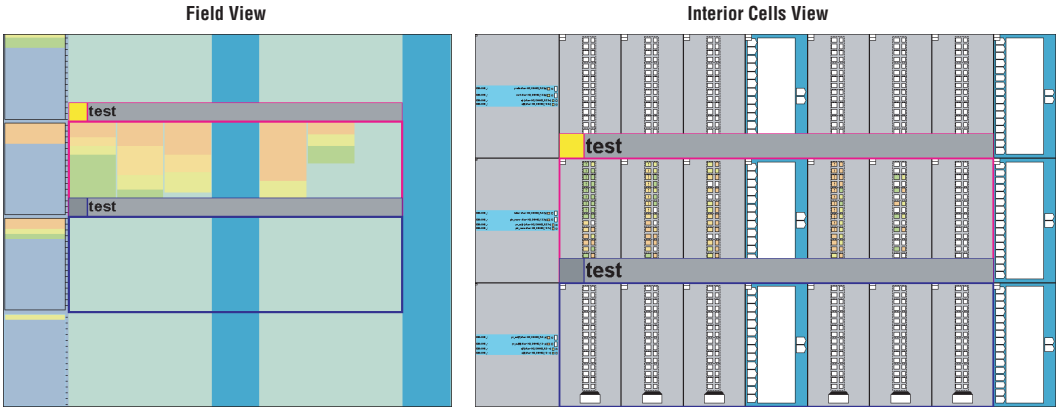
Figure 13–6. Using the Project Navigator to Create LogicLock Regions



Timing Closure Floorplan View

The **Timing Closure Floorplan** view provides you with current and last compilation assignments on one screen. You can display device resources in either of two views: the Field View and the Interior Cells View, as shown in Figure 13–7. The Field View provides an uncluttered view of the device floorplan in which all device resources such as embedded system blocks (ESBs) and MegaLAB™ blocks are outlined. The Interior Cells View provides a detailed view of device resources, including individual logic elements within a MegaLAB and device pins.

Figure 13–7. Timing Closure Floorplan Editor



LogicLock Region Properties

A LogicLock region is defined by its size (height and width) and location (where the region is located on the device). You can specify the size and/or location of a region, or the Quartus II software can generate them automatically. The Quartus II software bases the size and location of the region on the region's contents and the module's timing requirements. Table 13–1 describes the options for creating LogicLock regions.

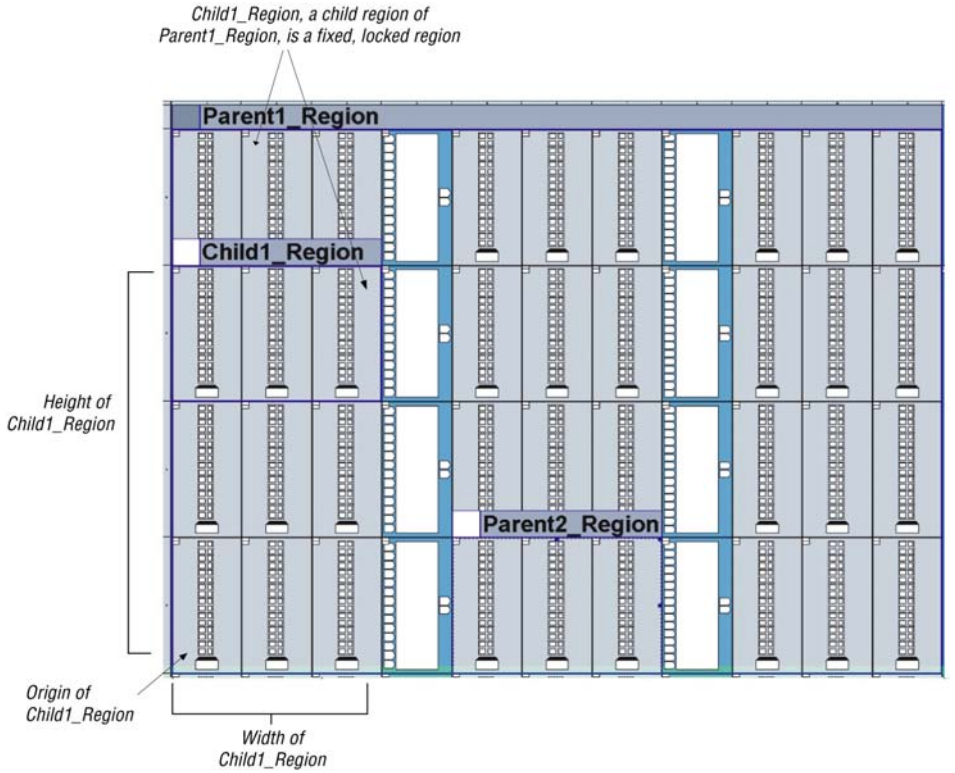
Table 13–1. Types of LogicLock Regions

Properties	Values	Behavior
State	Floating (default), Locked	Floating regions allow the Quartus II software to determine the region's location on the device. Locked regions represent user-defined locations for a region and are shown with a solid boundary in the floorplan. A locked region must have a fixed size.
Size	Auto (default), Fixed	Auto-sized regions allow the Quartus II software to determine the appropriate size of a region given its contents. Fixed regions have a user-defined shape and size.
Reserved	Off (default), On	The reserved property allows you to define whether the Fitter can use the resources within a region for entities that are not assigned to the region. If the reserved property is turned on, only items assigned to the region can be placed within its boundaries.
Soft	Off (default), On	Soft (on) regions give more deference to timing constraints, and allow some entities to leave a region if it improves the performance of the overall design. Hard (off) regions do not allow contents to be placed outside of the boundaries of the region.
Origin	Any Floorplan Location	The origin is the origin of the LogicLock region's placement on the floorplan. For Stratix, Stratix II, Stratix GX, Cyclone series, and MAX II devices, the origin is located in the lower left corner. The origin is located in the upper left corner for other device families.

The Quartus II software cannot automatically define a region's size if the location is locked. Therefore, if you want to specify the exact location of the region, you must also specify the size. Mercury devices support only locked and fixed regions.

The floorplan excerpt in Figure 13–8 shows the LogicLock region properties for a design implemented in a Stratix device.

Figure 13–8. LogicLock Region Properties

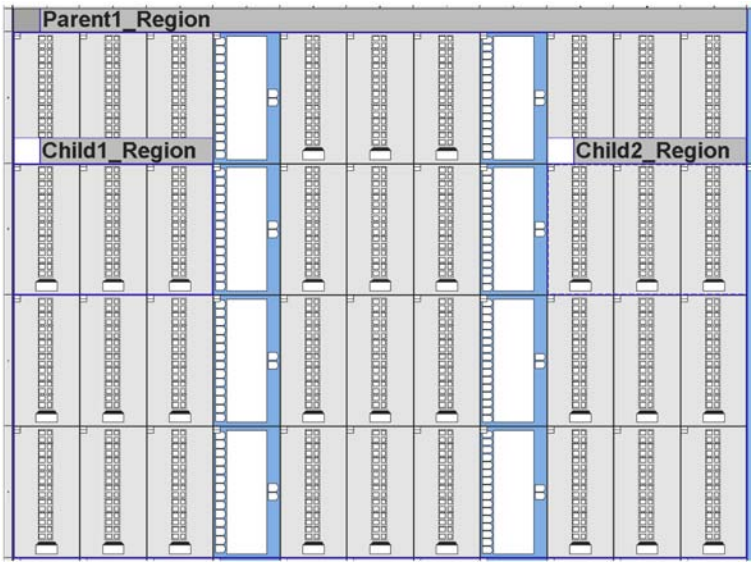


Hierarchical (Parent and/or Child) LogicLock Regions

With the LogicLock design flow, you can define a hierarchy for a group of regions by declaring parent and/or child regions. The Quartus II software places a child region completely within the boundaries of its parent region, allowing you to further constrain module locations. Additionally, parent and child regions allow you to further improve a module's performance by constraining the nodes in the module's critical

path. Figure 13–9 shows an example child region within a parent region, including labels for a locked location and floating location in a Stratix II device.

Figure 13–9. Child Region Within a Parent Region



The LogicLock region hierarchy does not have to be the same as the design hierarchy.

A child region's location can float within its parent or remain locked relative to its parent's origin. A locked parent region's location is locked relative to the device. If the child's location is locked and the parent's location is changed, the child's origin changes but maintains the same placement relative to the origin of its parent. Either you or the Quartus II software can determine a child region's size; however, the child region must fit entirely within the parent region.

Assigning LogicLock Region Content

Once you have defined a LogicLock region, you must assign resources to it using the Timing Closure Floorplan, the **LogicLock Regions** dialog box, the Assignment Editor, or Tcl scripts with the Quartus II Tcl Console or the `quartus_sh` executable.

Using Drag & Drop to Place Logic

You can drag selected logic displayed in the **Hierarchy** tab of the **Project Navigator**, Node Finder, or a schematic design file and drop it into the Timing Closure Floorplan or the **LogicLock Regions** dialog box. Figure 13–10 shows logic that has been dragged from the **Hierarchy** tab of the **Project Navigator** and dropped into a LogicLock region in the **Timing Closure Floorplan**.

Figure 13–10. Drag & Drop Logic in the Timing Closure Floorplan

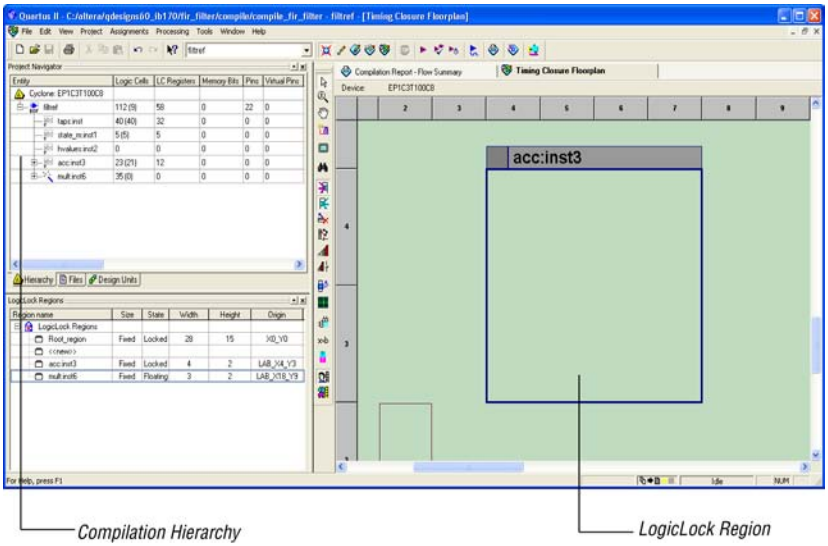
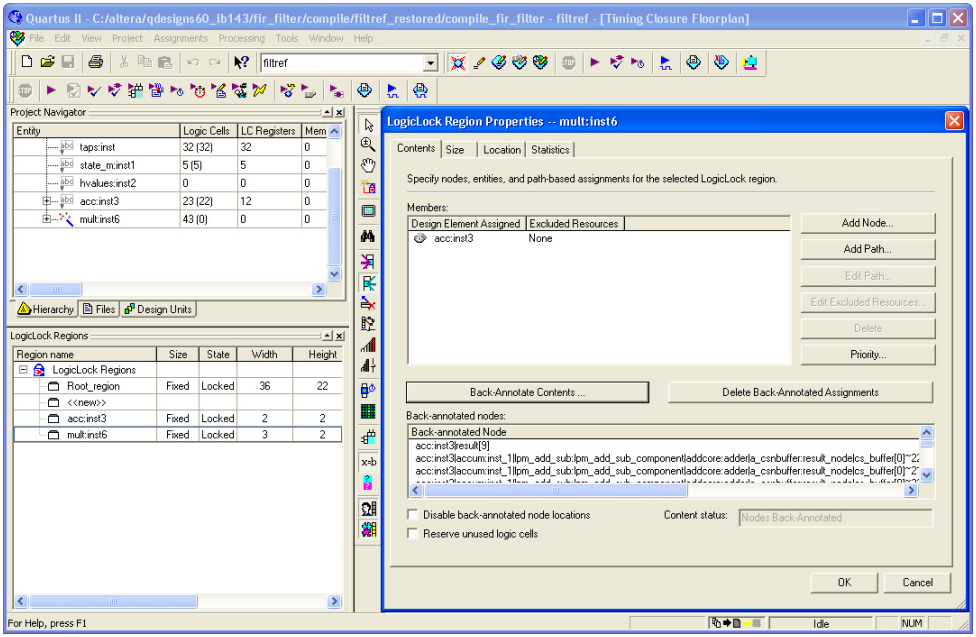


Figure 13–11 shows logic that has been dragged from the **Hierarchy** tab of the **Project Navigator** and dropped into the **LogicLock Regions Properties** dialog box. Logic can also be dropped into the **Design Element Assigned** column of the **Contents** tab of the **LogicLock Region Properties** box.

Figure 13–11. Drag & Drop Logic into the LogicLock Regions Dialog Box

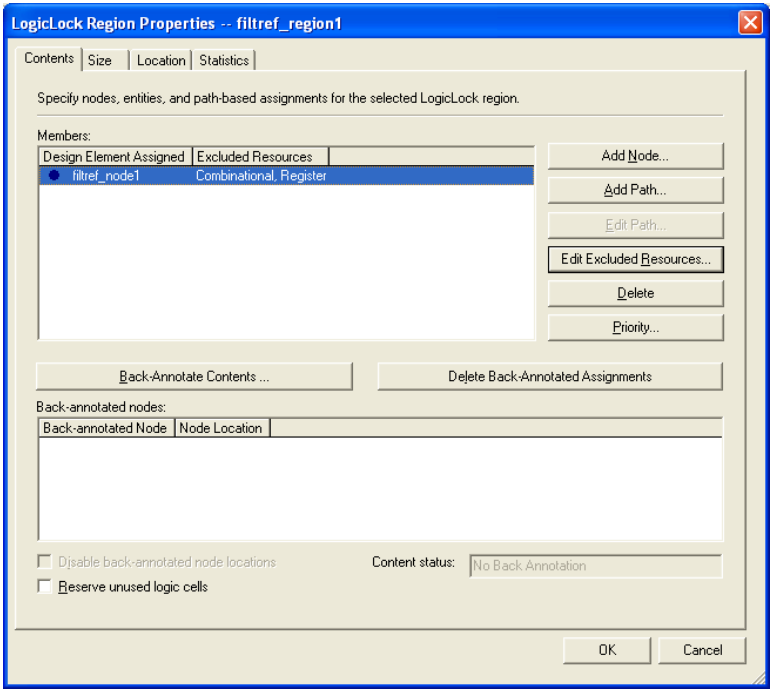


You must manually assign pins to a LogicLock region. The Quartus II software does not include pins automatically when you assign an entity to a region. The software only obeys pin assignments to locked regions that border the periphery of the device. For Stratix, Stratix II, Cyclone II, Cyclone, and MAX II devices, the locked regions must include the I/O pins as resources.

Excluded Resources

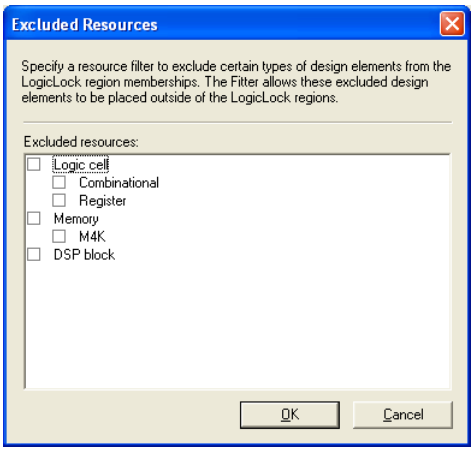
The Excluded Resources feature allows you to easily exclude specific device resources such as DSP blocks or M4K memory blocks from a LogicLock region. For example, you can specify resources that belong to a specific entity that are assigned to a LogicLock region, and specify that these resources be included with the exception of the DSP blocks. Use the Excluded Resources feature on a per-LogicLock region member basis. Figure 13–12 shows the **LogicLock Region Properties** dialog box with the Excluded Resources highlighted.

Figure 13–12. LogicLock Region Properties Dialog Box



To exclude certain device resources from an entity, in the **LogicLock Region Properties** dialog box, highlight the entity in the **Design Element Assigned** column, and click **Edit Excluded Resources**. The **Excluded Resources** dialog box is shown (Figure 13–13). In the **Excluded Resources** dialog box, you can select the device resources you want to exclude from the entity. Once you have selected the resources to exclude, the **Excluded Resources** column is updated in the **LogicLock Region Properties** dialog box to reflect the excluded resources.

Figure 13–13. Excluded Resources



The Excluded Resources feature prevents certain resource types from being included in a region, but it does not prevent the resources from being placed inside the region unless the region's "Reserved" property is set to **On**. To inform the Fitter that certain resources are not required inside a LogicLock region, define a resource filter.

Tcl Scripts

You can create LogicLock regions and assign nodes to them with Tcl commands that you can run from the Tcl Console or at the command prompt. The Tcl command `set_logiclock` is used to create or change the attributes of LogicLock regions.

For more information on creating and using LogicLock regions and contents, refer to the *Command Line* and *Tcl API* topics in the Quartus II online Help or "Scripting Support" on page 13–38.

Importing and Exporting LogicLock Regions

This section describes the steps required to import and export the LogicLock regions. For information on importing and exporting the assignments for lower-level design partitions using the incremental compilation flow, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

For the Quartus II software to achieve optimal placement, you should make timing assignments for all clock signals in the design, including t_{SU}, t_{CO}, and t_{PD}.

To facilitate the LogicLock design flow, the **Timing Closure Floorplan** highlights resources that have back-annotated LogicLock regions.

Export the Module

This section describes how to export a module's constraints to a format that can be imported by a top-level design. To be exported, a module requires design information as an atom netlist (VQM or EDF), placement information stored in a Quartus II Settings File, and routing information stored in a Routing Constraints File (**.rcf**).

Atom Netlist Design Information

The atom netlist contains design information that fully describes the module's logic in terms of an Altera device architecture. If the design was synthesized using a third-party tool and then brought into the Quartus II software, an atom netlist already exists and the node names are fixed. You do not need to generate another atom netlist. However, if you use any Synthesis Netlist Optimizations or Physical Synthesis Optimizations, you must generate a Verilog Quartus Mapping Netlist File (**.vqm**) using the Quartus II software, because the original atom netlist may have changed as a result of these optimizations.

Turn on the **Prevent further netlist optimization** option when back-annotating a region with the **Synthesis Netlist Optimizations** and/or **Physical Synthesis Optimization** options turned on. This sets the **Netlist Optimizations** to **Never Allow** for all nodes in the region, avoiding the possibility of a node name change when the region is imported into the top-level design.

If you synthesized the design as a VHDL Design File (**.vhd**), Verilog Design File (**.v**), Text Design File (**.tdf**), or a Block Design File (**.bdf**) in the Quartus II software, you must also create an atom netlist to fix the node names. During compilation, the Quartus II software creates a Verilog Quartus Mapping Netlist File in the **atom_netlists** subdirectory in the project directory.

If the atom netlist is from a third-party synthesis tools and the design has a black-box library of parameterized modules (LPM) functions or Altera megafunctions, you must generate a Quartus II Verilog Quartus Mapping Netlist File for the black-box modules.

For instructions on creating an atom netlist in the Quartus II software, refer to *Saving Synthesis Results for an Entity to a Verilog Quartus Mapping File* in Quartus II Help.

When you export LogicLock regions, all your design assignments are exported. Filtering is done only when the design is imported. However, you can export a subentity of the compilation hierarchy and all of its relevant regions. To do this, right-click the entity in the **Hierarchy** tab of the **Project Navigator** and click **Export Assignments.**

Placement Information
The Quartus II Settings File contains the module's LogicLock constraint information, including clock settings, pin assignments, and relative placement information for back-annotated regions. To maintain performance, you must back-annotate the module.

Routing Information
The Routing Constraints File (**.rcf**) contains the module's LogicLock routing information. To maintain performance, you must back-annotate the module.

Exporting the Routing Constraint File and Atom Netlist
To specify the Routing Constraint File and Atom Netlist to export, perform the following steps:

1. Run a full compilation.
2. On the Assignments menu, click **LogicLock Regions Window**.
3. Right-click the region name, and click **Properties**.
4. In the **LogicLock Region Properties** dialog box, click **Back-Annotate Contents**.
5. Enable or disable any of the advanced options such as **Prevent further netlist optimization**.
6. Turn on **Routing**, and click **OK**.
7. In the **LogicLock Region Properties** dialog box, click **OK**.
8. On the Assignments menu, click **Export Assignments**.
9. In the **Export Assignments** dialog box, turn on **Export back-annotated routing** and **Save a node-level netlist of the entire design into a persistent source file**, click **OK**.

For instructions on exporting a LogicLock region assignment in the Quartus II software, refer to *Exporting LogicLock Region Assignments & Other Entity Assignments* in Quartus II Help.

Import the Module

To specify which Quartus II Settings File for a specific instance or entity, use the **LogicLock Import File Name** option in the Assignment Editor. This option lets you specify different LogicLock region constraints for each instance of an entity and import them into the top-level design. You also can specify an RCF file with the **LogicLock Routing Constraints File Name** option in the Assignment Editor.

When importing LogicLock regions into the top-level design, you must specify the Quartus II Settings File and Routing Constraints File for the modules in the project. If the design instantiates a module multiple times, the Quartus II software applies the LogicLock regions multiple times.

Before importing LogicLock regions, you must perform analysis and elaboration, or compile the top-level design, thus ensuring that the Quartus II software is aware of all instances of the lower-level modules.

The following sections describe how to specify a Quartus II Settings File for a module and how to import the LogicLock assignments into the top-level design.

Importing the Routing Constraints File and the Atom Netlist File
To specify the Quartus II Settings File and atom netlist to import, perform the following steps:

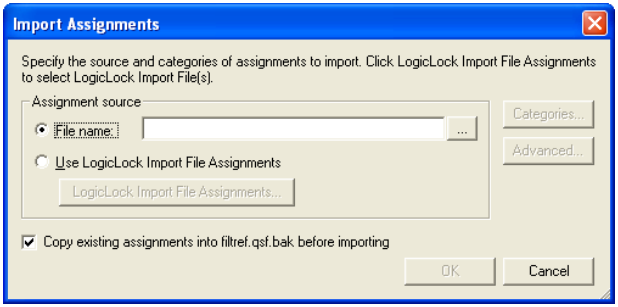
1. On the Assignments menu, click **Import Assignments**. In the **Import Assignments** dialog box, click **Advanced**.

2. In the **Advanced Import Settings** dialog box, turn on **Back-annotated routing**.

Now, when you import a LogicLock region, the routing constraint file is also be imported.

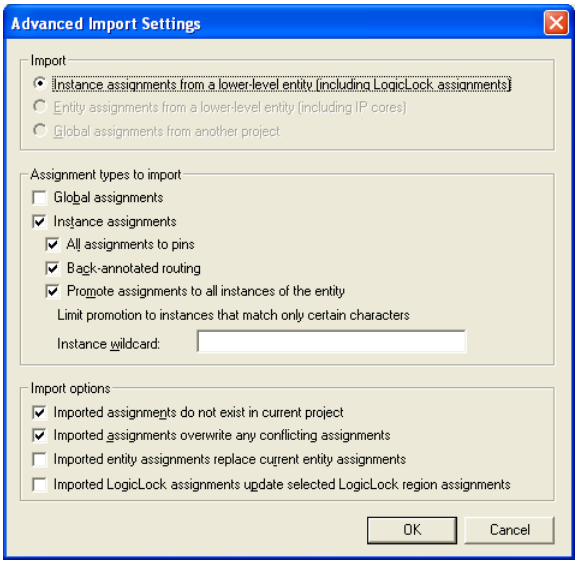
Import the Assignments
On the Assignments menu, click **Import Assignments** to import the assignments. The Import Assignments dialog box is shown (Figure 13–14).

Figure 13–14. Import Assignments Dialog Box



Use the options available in the **Advanced Import Settings** dialog box to control how you import your LogicLock regions (Figure 13–15).

Figure 13–15. Advanced Import Settings Dialog Box



To prevent spurious no-fit errors, parent, or top-level regions with multiple instances (that do not contain back-annotated routing information), are imported with their states set to floating. Otherwise, the region's state remains as specified in the Quartus II Settings File. This allows the Quartus II software to move LogicLock regions to areas on the

device with free resources. A child region is locked or floating relative to its parent region's origin as specified in the module's original LogicLock constraints.

If you want to lock a LogicLock region to a location, you can manually lock down the region in the **LogicLock Regions** dialog box or the Timing Closure Floorplan.

Each imported LogicLock region has a name that corresponds to the original LogicLock region name combined with the instance name in the form of <*instance name*>|<*original LogicLock region name*>. For example, if a LogicLock region for a module is named `LLR_0` and the instance name for the module is `Filter:inst1`, then the LogicLock region name in the top-level design is `Filter:inst1|LLR_0`.

Compile & Verify the Top-Level Design

After importing all modules, you can compile and verify the top-level design. The compilation report shows whether system timing requirements have been met.

Additional Quartus II LogicLock Design Features

To complement the **LogicLock Regions** dialog box and Device Floorplan view, the Quartus II software has additional features to help you design with the LogicLock feature.

Tooltips

When you move the mouse pointer over a LogicLock region name on the **Hierarchy** tab of the **Project Navigator** or **LogicLock Regions** dialog box, or over the top bar of the LogicLock region in the Timing Closure Floorplan, the Quartus II software displays a tooltip with information about the properties of the LogicLock region.

Placing the mouse pointer over fitter-placed LogicLock regions displays the maximum routing delay within the LogicLock region. To enable this feature, on the View menu, point to Routing and click **Show Intra-region Delay**.

Repair Branch

When you retarget your design to either a larger or smaller device, there is a chance that your LogicLock regions no longer contain valid values for location or size in the new device, resulting in an illegal LogicLock region. In the **LogicLock Regions** dialog box, the Quartus II software identifies and displays in red the names of illegal LogicLock regions.

To correct the illegal LogicLock region, use the **Repair Branch** command. Right click the desired LogicLock region's name and choose **Repair Branch**.

If more then one illegal LogicLock region exists, you can repair all regions. To do so, right-click the first line in the LogicLock window that contains the text "LogicLock Regions" and click **Repair Branch**.

Reserve LogicLock Region

The Quartus II software honors all entity and node assignments to LogicLock regions. Occasionally, entities and nodes do not occupy an entire region, which leaves some of the region's resources unoccupied. To increase the region's resource utilization and performance, the Quartus II software's default behavior fills the unoccupied resources with other nodes and entities that have not been assigned to any other region. You can prevent this behavior by turning on **Reserve unused logic cells** on the **Contents** tab of the **LogicLock Region Properties** dialog box. When this option is turned on, your LogicLock region only contains the entities and nodes that you have specifically assigned to your LogicLock region.

In a team-based design environment, this option is extremely helpful in device floorplanning. When this option is turned on, each team can be assigned a portion of the device floorplan where placement and optimization of each submodule occurs. Device resources can be distributed to every module without affecting the performance of other modules.

Prevent Assignment to LogicLock Regions Option

Turning on the **Prevent Assignment to LogicLock Regions** option excludes the specified entity or node from being a member of any LogicLock region. However, it does not prevent the entity or node from entering into LogicLock regions. The fitter places the entity or node anywhere on the device as if no regions exist. For example, if an entire module is assigned to a LogicLock region, when this option is turned on, you can exclude a specific subentity or node from the region.

You can make the **Prevent Assignment to LogicLock Regions** assignment to an entity or node in the Assignment Editor under **Assignment Name**.

LogicLock Regions Connectivity

The Timing Closure Floorplan Editor allows you to see connections between various LogicLock regions that exist within a design. The connection between the regions is drawn as a single line between the LogicLock regions. The thickness of this line is proportional to the number of connections between the regions.

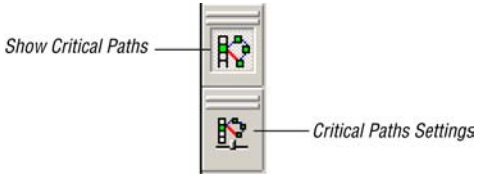
Rubber Banding

On the View menu, click Routing, and select **Rubber Banding** to show existing connections between LogicLock regions and nodes during movement of LogicLock regions within the Floorplan Editor.

Show Critical Paths

You can display the critical paths in the design by turning on the **Show Critical Paths** option. Use this option with the **Critical Paths Settings** option to display paths based on the Timing Analysis report, as shown in Figure 13–16.

Figure 13–16. Show Critical Paths & Critical Paths Settings



Show Connection Count

You can determine the number of connections between LogicLock regions by turning on the **Show Connection Count** option.

Analysis & Synthesis Resource Utilization by Entity

The Compilation Report contains an **Analysis & Synthesis Resource Utilization by Entity** section, which reports accurate resource usage statistics, including entity-level information. This feature is useful when manually creating LogicLock regions.

Path-Based Assignments

You can assign paths to LogicLock regions based on source and destination nodes, allowing you to easily group critical design nodes into a LogicLock region. The path source and destination nodes can be any of the following:

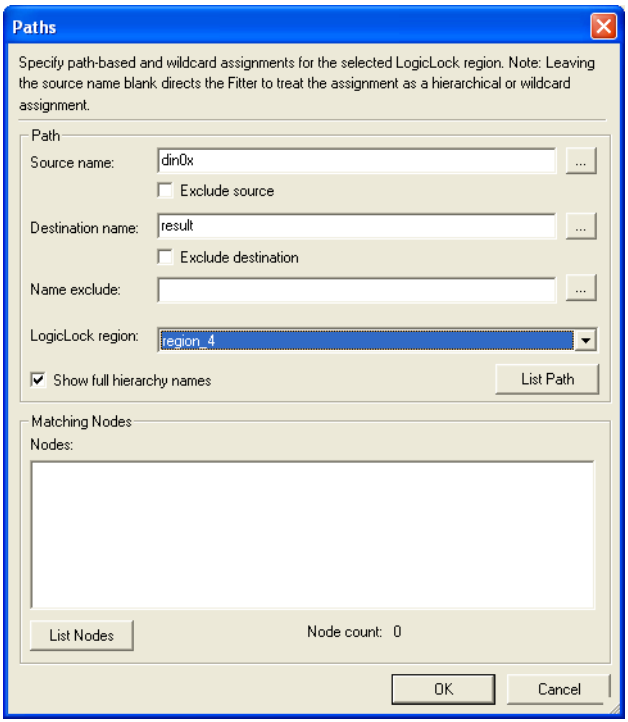
- Valid register-to-register path, meaning that the source and destination nodes must be registers
- Valid pin-to-register path, meaning the source node is a pin and the destination node is a register
- Valid register to pin path, meaning that the source node is a register and the destination node is a pin
- Valid pin-to-pin path, meaning that both the source and destination nodes are pins

Figure 13–17 shows the **Paths** dialog box.

To access the **Paths** dialog box, on the **Contents** tab of the **Logic Lock Regions** dialog box, click **Add Path** or **Edit Path**.

Both "*" and "?" wildcard characters are allowed for the source and destination nodes. When creating path-based assignments, you can exclude specific nodes using the **Name exclude** field in the **Paths** dialog box.

Figure 13–17. Paths Dialog Box



You can also use the Quartus II Timing Analysis Report to create path-based assignments by following these steps:

1. Expand the **Timing Analyzer** section in the **Compilation Report**.
2. Select any of the clocks in the section that is labeled "Clock Setup:<*clock name*>."
3. Locate a path that you want to assign to a LogicLock region. Drag this path from the Report window and drop it in the <<new>> section of the LogicLock Region window.

This operation creates a path-based assignment from the source register to the destination register as shown in the **Timing Analysis Report**.

Quartus II Revisions Feature

When you create, modify, or import LogicLock regions into a top-level design, you may need to experiment with different configurations to achieve your desired results. The Quartus II software provides the Revisions feature that allows for a convenient way to organize the same project with different settings until an optimum configuration is found.

On the Project menu, click **Revisions**. In the **Revisions** dialog box, create and set revisions. Revision can be based on the current design or any previously created revisions. A description can also be entered for each revision created. This is a convenient way to organize the placement constraints created for your LogicLock regions.

LogicLock Assignment Precedence

Conflicts might arise during the assignment of entities and nodes to LogicLock regions. For example, an entire top-level entity might be assigned to one region and a node within this top-level entity assigned to another region. To resolve conflicting assignments, the Quartus II software maintains an order of precedence for LogicLock assignments. The Quartus II software's order of precedence is as follows from highest to lowest:

1. Exact node-level assignments
2. Path-based and wildcard assignments
3. Hierarchical assignments

However, conflicts might also occur within path-based and wildcard assignments. Path-based and wildcard assignment conflicts arise when one path-based or wildcard assignment contradicts another path-based or wildcard assignment. For example, a path-based assignment is made containing a node labeled `X` and assigned to LogicLock region `PATH_REGION`. A second assignment is made using wildcard assignment `X*` with node `X` being placed into region `WILDCARD_REGION`. As a result of these two assignments, node `X` is assigned to two regions: `PATH_REGION` and `WILDCARD_REGION`.

To resolve this type of conflict, the Quartus II software keeps the order in which the assignments were made and treats the last assignment created with the highest priority.

Open the **Priority** dialog box by selecting **Priority** on the **Contents** tab of the **LogicLock properties** dialog box. You can change the priority of path-based and wildcard assignments by using the Up or Down buttons in the **Priority** dialog box. To prioritize assignments between regions, you must select multiple LogicLock regions. Once the regions have been selected, you can open the **Priority** dialog box from the LogicLock Properties window.

LogicLock Regions Versus Soft LogicLock Regions

Normally all nodes assigned to a particular LogicLock region always reside within the boundaries of that region. Soft LogicLock regions can enhance design performance by removing the fixed rectangular boundaries of LogicLock regions. When you assign a LogicLock region as being "Soft," the Quartus II software attempts to place as many nodes assigned to the region as close together as possible, and has the added flexibility of moving nodes outside of the soft region to meet your design performance requirement. This allows the Quartus II Fitter greater flexibility in placing nodes in the device to meet your performance requirements.

When you assign nodes to a soft LogicLock region, they can be placed anywhere in the device, but if the soft region is the child of a region, the nodes are not assigned outside the boundaries of the first non-soft parent region. If a non-soft parent does not exist (in a design targeting a Stratix II, Stratix GX, Stratix, Cyclone II, Cyclone, or MAX II device), the region floats within the `Root_region`, that is, the boundaries of the device. You can turn on the **Soft Region** option on the **Location** tab of the **LogicLock Region Properties** dialog box.

Soft regions can have an arbitrary hierarchy that allows any combination of parent and child to be a soft region. The **Reserved** option is not compatible with soft regions.

Soft LogicLock regions cannot be back-annotated because the Quartus II software may have placed nodes outside of the LogicLock region resulting in undefinable location assignments relative to the region's origin and size.

Soft LogicLock regions are available for all device families that support floating LogicLock regions.

Virtual Pins

When you compile a design in the Quartus II software, all I/O ports are directly mapped to pins on the targeted device. The I/O port mapping may create problems for a modular and hierarchical design as lower level modules may have I/O ports that exceed device pins available on the targeted device. Or, the I/O ports may not directly feed a device pin, but instead drive other internal nodes. The Quartus II accommodates this situation by supporting virtual pins.

The Virtual Pin assignment communicates to the Quartus II software which I/O ports of the design module are internal nodes in the top-level design. These assignments prevent the number of I/O ports in the lower level module from exceeding the total number of available device pins. Every I/O port that is designated as a virtual pin is mapped to either an LCELL or ALM, depending on the target device. Figure 13–19 shows the virtual input and output pins in the Timing Closure Floorplan Editor.

Bidirectional, registered I/O pins, and I/O pins with output enable signals cannot be virtual pins.

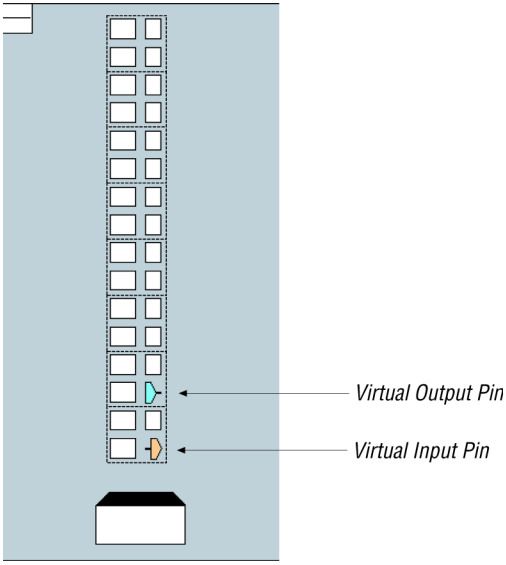
In the top-level design, these virtual pins are connected to an internal node of another module. Making assignments to virtual pins allows you to place them in the same location or region on the device as the corresponding internal nodes would exist in the top-level module. This feature has the added benefit of providing accurate timing information during lower-level module optimization.

To accommodate designs with multiple clock domains, you can specify individual clock signals by turning on the **Virtual Pin Clock** option for each virtual pin.

Use the following guidelines for creating virtual pins in the Quartus II software:

- Clock pins should not be declared as virtual pins.
- Nodes/signals that drive physical device pins in the top-level design should not be declared as virtual pins.

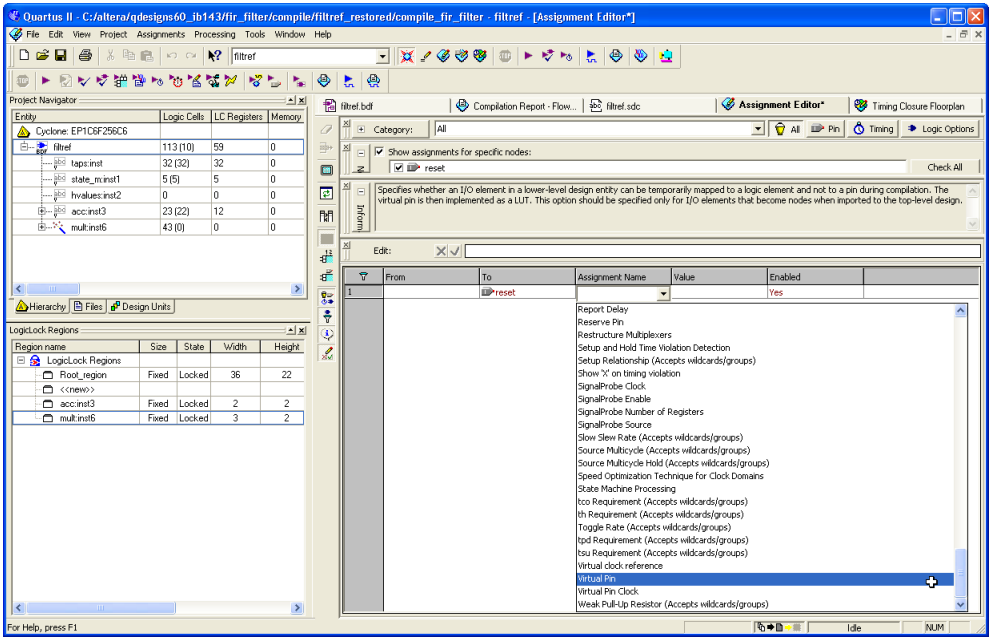
Figure 13–18. Virtual I/O Pins in the Quartus II Floorplan Editor



Bidirectional, registered I/O pins, and I/O pins with output enable signals cannot be virtual pins. All virtual pins must map to device I/O pins in the top-level design.

Figure 13–19 shows assigning virtual pins using the Assignment Editor.

Figure 13–19. Using the Assignment Editor to Assign Virtual Pins



In the Node Finder, setting **Filter Type to Pins: Virtual** allows you to display all assigned virtual pins in the design. From the Assignment Editor, to access the Node Finder, double-click the **To** field; when the arrow appears on the right side of the field, click the arrow and select **Node Finder**.

LogicLock Restrictions

This section discusses restrictions to consider when you use the LogicLock design flow, including:

- Constraint priority
- Placing LogicLock regions
- Placing memory, pins, and other device features into LogicLock regions

Constraint Priority

During the design process, placing restrictions on nodes or entities in the design often is necessary. These restrictions often conflict with the node or entity assignments for a LogicLock region. To avoid conflicts, consider

the order of precedence given to constraints by the Quartus II software during fitting. The following assignments have priority over LogicLock region assignments:

- Assignments to device resources and location assignments
- Fast input register and fast output register assignments
- Local clock assignments for Stratix devices
- Custom region assignments
- I/O standard assignments

The Quartus II software removes nodes and entities from LogicLock regions if any of these constraints are applied to them.

Placing LogicLock Regions

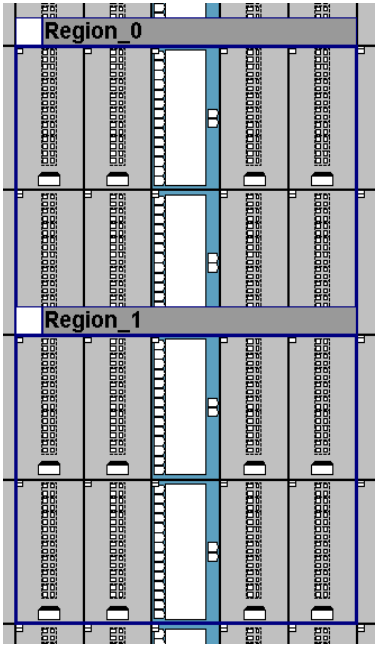
A fixed region must contain all of the resources required for the module. Although the Quartus II software automatically can place and size LogicLock regions to meet resource and timing requirements, you can manually place and size regions to meet your design needs. To do so, follow these guidelines:

- LogicLock regions with pin assignments must be placed on the periphery of the device, adjacent to the pins. (For Stratix II, Stratix, Stratix GX, Cyclone series, and MAX II devices, you must also include the I/O block.)
- Floating LogicLock regions cannot overlap.
- Avoid creating fixed and locked regions that overlap.
- After back-annotating a region, the software can place the region only in areas on the device with exactly the same resources.

These guideline are particularly important if you want to import multiple instances of a module into a top-level design, because you must ensure that the device has two or more locations with exactly the same device resources. If the device does not have another area with exactly the same resources, the Quartus II software generates a fitting error during compilation of the top-level design.

Figure 13–20 shows a floorplan with two instantiations of the same module. Both modules have the same LogicLock constraints and require exactly the same resources. The Quartus II software places the two LogicLock regions in different areas of the device that have the same resources.

Figure 13–20. Floorplan of Two Instances of a LogicLock Region



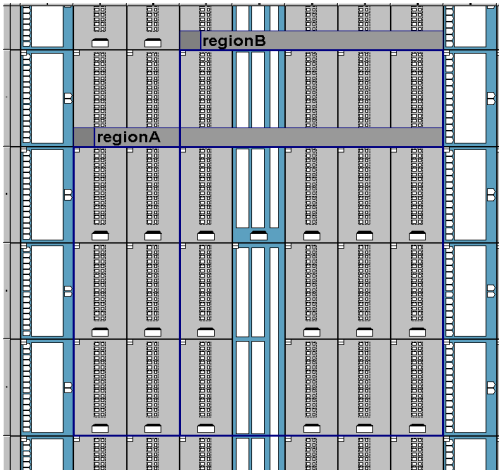
Placing Memory, Pins & Other Device Features into LogicLock Regions

A LogicLock region includes all device resources within its boundaries. You can assign pins to LogicLock regions; however, this placement puts location constraints on the region. When the Quartus II software places a floating auto-sized region, it places the region in an area that meets the requirements of the LogicLock region's contents.

Pin assignments to LogicLock regions are effective only in fixed and locked regions. Pins assigned to floating regions do not influence the region's placement.

Only one LogicLock region can claim a device resource. If the boundary includes part of a device resource, such as a DSP block, the Quartus II software allocates the entire resource to the LogicLock region. Figure 13–21 shows two overlapping regions in the same Stratix DSP block. The Quartus II software can assign this resource to only one of the LogicLock regions. The region's resource requirements determine which region gets the assignment. If both regions require a DSP block, the Quartus II software issues a fitting error.

Figure 13–21. Overlapping LogicLock Regions



Back-Annotating Routing Information

LogicLock regions not only allow you to preserve the placement of logic from one compilation to the next, but also allow you to retain the routing inside the LogicLock regions. With both placement and routing locked, you have an extremely portable design module that can be used many times in a top-level design without requiring further optimization.

Back-annotate routing only if necessary because this can prevent the Quartus II Fitter from finding an optimal fit for your design.

Back-annotate the routing from the Assignments menu, by choosing **Routing** from the **Back-Annotate Assignments** dialog box. Refer to Figure 13–4.

If you are not using an atom netlist, you must turn on the **Save a node-level netlist of the entire design into a persistent source file** option (on the Assignments menu, click **Back-Annotate Assignments**) if back-annotation of routing is selected. Writing out a Verilog Quartus Mapping Netlist File causes the Quartus II software to enforce persistent naming of nodes when saving the routing information. The Verilog Quartus Mapping Netlist File is then used as the design's source.

Back-annotated routing information is valid only for regions with fixed sizes and locked locations. The Quartus II software ignores the routing information for LogicLock regions you specify as floating and automatically sized.

The **Disable Back-Annotated Node locations** option in the **LogicLock Region Properties** dialog box is not available if the region contains both back-annotated routing and back-annotated nodes.

Exporting Back-Annotated Routing in LogicLock Regions

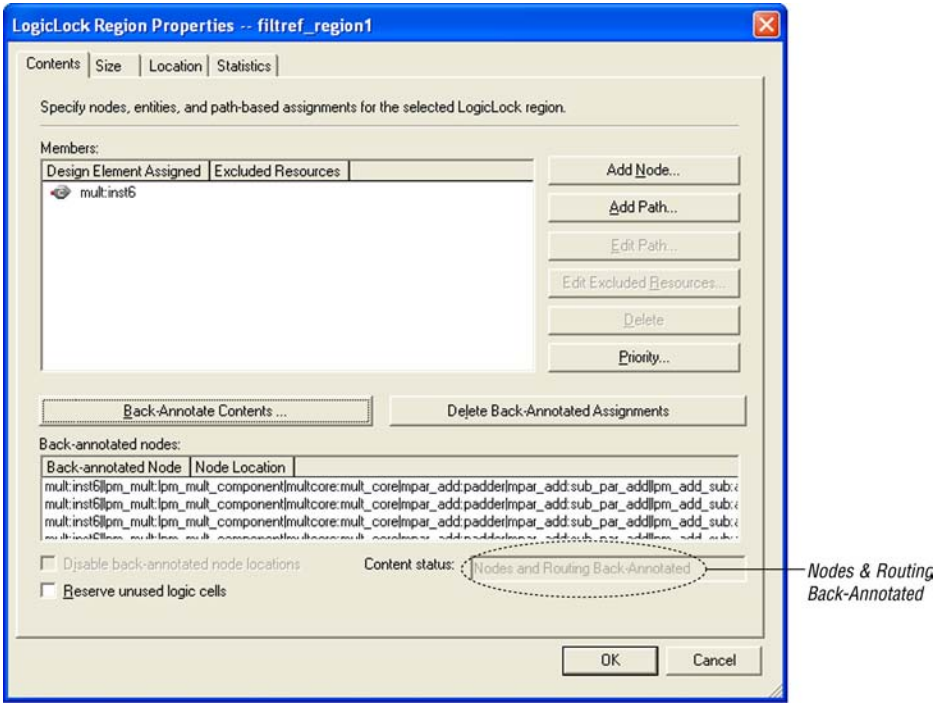
To export the LogicLock region routing information, on the Assignments menu, click **Export Assignments,** and in the **Export Assignments** dialog box, turn on **Export Back-annotated routing**. This generates a Quartus II Settings File and a Routing Constraints File in the specified directory. The Quartus II Settings File contains all LogicLock region properties as specified in the current design. The Routing Constraints File contains all the necessary routing information for the exported LogicLock regions.

This Routing Constraints File works only with the atom netlist for the entity being exported.

Only regions that have back-annotated routing information have their routing information exported when you export the LogicLock regions. All other regions are exported as regular LogicLock regions.

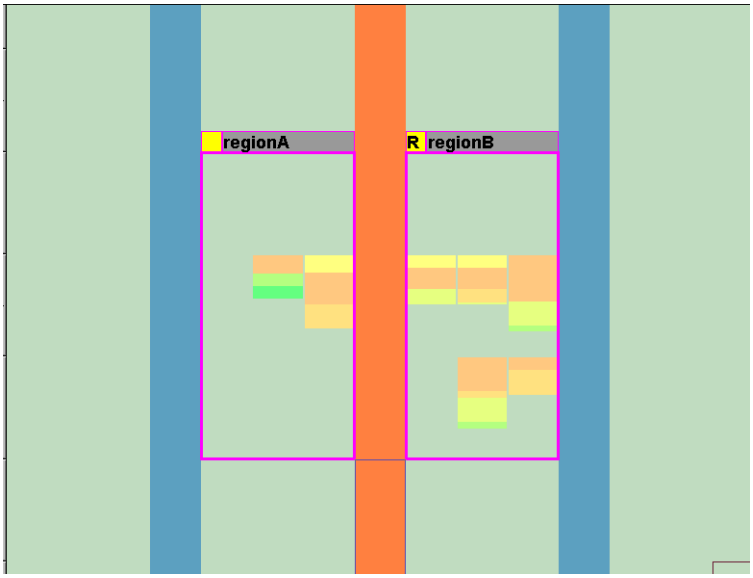
To determine if a LogicLock region contains back-annotated routing, refer to the **Content Status** box shown on the **Contents** tab of the **LogicLock Region Properties** dialog box. If routing has been back-annotated, the status is "Nodes and Routing Back-Annotated" (Figure 13–22).

Figure 13–22. LogicLock Status



The Quartus II software also reports whether routing information has been back-annotated in the Timing Closure Floorplan. LogicLock regions with back-annotated routing have an "R" in the top-left hand corner of the region (Figure 13–23).

Figure 13–23. Back-Annotation of Routing



Importing Back-Annotated Routing in LogicLock Regions

To import LogicLock region routing information, you must specify the instance that will have its routing information imported. This is done with the assignment LogicLock Routing Constraints File in the Assignment Editor.

A Routing Constraints File must be explicitly specified using the LogicLock **Back-annotated Routing Import File Name** assignment prior to importing any LogicLock region.

The Quartus II software imports LogicLock regions with back-annotated routing as regions locked to a location and of fixed size.

You can import back-annotated routing if only one instance of the imported region exists in the top level of the design. If more than one instance of the imported region exists in the top level of the design, the routing constraint is ignored and the LogicLock region is imported without back-annotation of routing. This is because routing resources from one part of the device may not be exactly the same in another area of the device.

When importing the Routing Constraints File for a lower level entity, you must use the same atom netlist, that is, the Verilog Quartus Mapping Netlist File that was used to generate the Routing Constraints File. This ensures that the node names annotated in the Routing Constraints File match those in the atom netlist.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The *Scripting Reference Manual* has the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Initializing & Uninitializing a LogicLock Region

You must initialize the LogicLock data structures before creating or modifying any LogicLock regions and before executing any of the Tcl commands listed below.

Use the following Tcl command to initialize the LogicLock data structures:

```
initialize_logiclock
```

Use the following command to uninitialize the LogicLock data structures before closing your project:

```
uninitialize_logiclock
```

Creating or Modifying LogicLock Regions

Use the following Tcl command to create or modify a LogicLock region:

```
set_logiclock -auto_size true -floating true -region \
<my_region-name>
```

In the above example, the region's size is set to auto and the state set to floating.

If you specify a region name that does not exist in the design, the command creates the region with the specified properties. If you specify the name of an existing region, the command changes all properties you specify, and leaves unspecified properties unchanged.

For more information about creating LogicLock regions, refer to "Creating LogicLock Regions" on page 13–4.

Obtaining LogicLock Region Properties

Use the following Tcl command to obtain LogicLock region properties. This example returns the height of the region named `my_region`.

```
get_logiclock -region my_region -height
```

Assigning LogicLock Region Content

Use the following Tcl commands to assign or change nodes and entities in a LogicLock region. This example assigns all nodes with names matching `fifo*` to the region named `my_region`.

```
set_logiclock_contents -region my_region -to fifo*
```

You can also make path-based assignments with the following Tcl command:

```
set_logiclock_contents -region my_region -from \
fifo -to ram*
```

For more information about assigning LogicLock Region Content, refer to "Assigning LogicLock Region Content" on page 13–13.

Prevent Further Netlist Optimization

Use this Tcl code to prevent further netlist optimization for nodes in a back-annotated LogicLock region. In your code, specify the name of your LogicLock region.

```
foreach node [get_logiclock_contents -region \
<region name> -node_locations] {

    set node_name [lindex $node 0]
```

```
    set_instance_assignment -name
ADV_NETLIST_OPT_ALLOWED "NEVER ALLOW" -to $node_name
```

The `get_logiclock_contents` command is in the `logiclock` package.

Save a Node-level Netlist for the Entire Design into a Persistent Source File (.vqm)

Make the following assignments to cause the Quartus II Fitter to save a node-level netlist for the entire design into a Verilog Quartus Mapping Netlist File:

```
set_global_assignment \
-name LOGICLOCK_INCREMENTAL_COMPILE_ASSIGNMENT ON
set_global_assignment \
-name LOGICLOCK_INCREMENTAL_COMPILE_FILE <file name>
```

Any path specified in the file name must be relative to the project directory. For example, specifying **atom_netlists/top.vqm** places **top.vqm** in the **atom_netlists** subdirectory of your project directory.

A Verilog Quartus Mapping Netlist File is saved in the directory specified at the completion of a full compilation.

For more information about saving a node-level netlist, refer to "Atom Netlist Design Information" on page 13–18.

Exporting LogicLock Regions

Use the following Tcl command to export LogicLock region assignments. This example exports all LogicLock regions in your design to a file called **export.qsf**.

```
logiclock_export -file export.qsf
```

For more information about exporting LogicLock regions refer to "Export the Module" on page 13–18.

Importing LogicLock Regions

Use the following Tcl commands to import LogicLock region assignments. This example ignores any pin assignments in the imported region.

```
set_instance_assignment -name LL_IMPORT_FILE \
my_region.qsf -to my_destination

logiclock_import -no_pins
```

Running the import command imports the assignment types for each entity in the design hierarchy. The assignments are imported from the file specified in the `LL_IMPORT_FILE` setting.

For more information about importing LogicLock regions, refer to "Import the Module" on page 13–20.

Setting LogicLock Assignment Priority

Use the following Tcl code to set the priority for a LogicLock region's members. This example reverses the priorities of the LogicLock region in your design.

```
set reverse [list]
foreach member [get_logiclock_member_priority] {
    set reverse [insert $reverse 0 $member]
{
set_logiclock_member_priority $reverse
```

For more information about setting the LogicLock assignment priority, refer to "Constraint Priority" on page 13–31.

Assigning Virtual Pins

Use the following Tcl command to turn on the virtual pin setting for a pin called `my_pin`:

```
set_instance_assignment -name VIRTUAL_PIN ON \
-to my_pin
```

For more information about assigning virtual pins, refer to "Virtual Pins" on page 13–29.

Back-Annotating LogicLock Regions

The Quartus II software provides the back-annotate Tcl package that allows you to back-annotate the contents of a LogicLock region. Use the following command line option to back-annotate a LogicLock region:

```
logiclock_back_annotate [-h | -help] [-long_help]
[-region <region name>] [-from <source name>]
[-to <destination name>] [-exclude_from] [-exclude_to] [-path_exclude <path_exclude name>]
[-no_delay_chain] [-no_contents] [-lock] [-routing]
[-resource_filter <resource_filter value>] [-no_dont_touch]

[-remove_assignments] [-no_demote_lab] [-no_demote_mac] [-no_demote_pin] [-no_demote_ram]
```

For example, the following command back-annotates all nodes and routing in the region, `one_region`.

```
package require ::quartus::backannotate
logiclock_back_annotate -routing -lock -no_demote_lab -region one_region
```

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Conclusion

The LogicLock block-based design flow shortens design cycles because it allows design and the implementation of design modules to occur independently, and also preserves performance of each design module during system integration. You can export modules, making design reuse easier.

You can include a module in one or more projects while maintaining performance, and reducing development costs and time-to-market. LogicLock region assignments give you complete control over logic and memory placement so that you can use LogicLock region assignments to improve the performance of non-hierarchical designs.

14. Synplicity Amplify Physical Synthesis Support

QII52011-6.0.0

Introduction

Synplicity has developed the Amplify Physical Optimizer physical synthesis software to help designers meet performance and time-to-market goals. You can use this software to create location assignments and optimize critical paths outside the Quartus® II software design environment. The Amplify Physical Optimizer design software, which runs on the Synplify Pro synthesis engine, creates a Tcl script with hard location assignments and LogicLock™ regions to control logic placement in the Quartus II software. Depending on the design, the Amplify Physical Optimizer software can improve Altera® device performance over Synplify Pro-compiled designs by reducing the number of logic levels and the interconnect delays in critical paths. Moreover, the Amplify Physical Optimizer software allows designers to compile multiple implementations in parallel to reduce optimization time.

For more information on the Synplify Pro software, refer to *Synplicity Synplify & SynplifyPro Support* chapter in volume 1 of the *Quartus II Handbook*.

This chapter explains the physical synthesis concepts, including an overview of the Amplify Physical Optimizer software and Quartus II flow.

Software Requirements

The examples in this document were generated using the following software versions:

- Quartus II, version 5.1
- Amplify Physical Optimizer, version 3.7

Amplify Physical Synthesis Concepts

The Amplify Physical Optimizer physical synthesis tool uses information about the interconnect architectures of Altera devices to reduce interconnect and logic delays in the critical paths. Timing-driven synthesis tools cannot accurately predict how place-and-route tools function; therefore, determining the real critical path with the synthesis tool is a difficult task.

Synthesis tools create technology-level netlist files that work with floorplans using place-and-route tools. Synthesis tools also define netlist names that are used in place-and-route, which means hard location assignments may not apply in the next revision of the resynthesized netlist as nodes names might have been renamed or removed.

Physical synthesis allows you to create floorplans at the register transfer level (RTL) of a design, giving you the ability to perform logic tunneling and replication. Physical synthesis also gives you the flexibility to make changes at the RTL level, allowing these changes to reflect in previously planned paths.

Physical synthesis uses knowledge of the FPGA device architecture to place paths into customized regions. This process will minimize interconnect delays as interconnect and placement information influences the synthesis process of the design.

When the Amplify Physical Optimizer software synthesizes a design, it creates a .**vqm** atom-netlist and Tcl script files, which are read by the Quartus II software. You can create a Quartus II project with the VQM netlist as the top-level module and source the Tcl script generated by the Amplify Physical Optimizer software. The Tcl script sets the design's device, timing constraints (Timing Driven Compilation [TDC] value, multicycle paths, and false paths), and any other constraints specified by the Amplify Physical Optimizer software. After you source the Tcl script, you can compile the design in the Quartus II software.

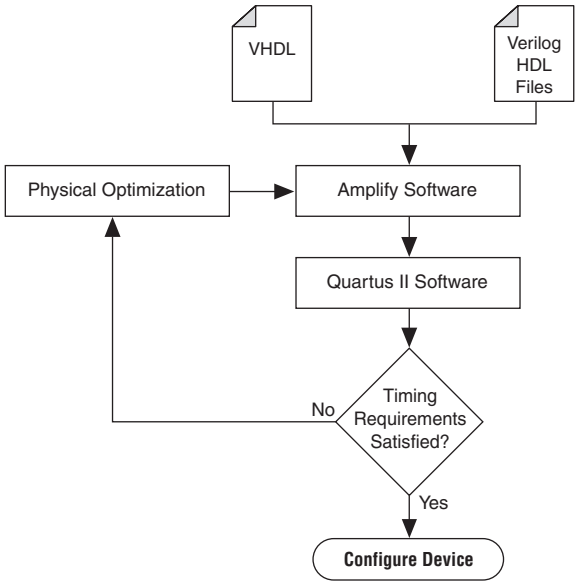
Refer to "Forward Annotating Amplify Physical Optimizer Constraints into the Quartus II Software" on page 14–12 for more information on setting up a Quartus II project with Amplify Physical Optimizer Tcl script files.

After the Quartus II software compiles the design, the software performs a timing analysis on the design. The timing analysis reports all timing-related information for the design. If the design does not meet the timing requirements, you can use the timing analysis numbers as a reference when running the next iteration of physical synthesis through the Amplify Physical Optimizer software. This same timing analysis information is also reported in a file called <*revision name*>**.tan.rpt** in the design directory.

Amplify-to-Quartus II Flow

If timing requirements are not met with the Amplify Physical Optimizer flow, you should first place and route the design in the Quartus II software without physical constraints. After compilation, you can determine which critical paths should be optimized in the Amplify Physical Optimizer tool in the next iteration. Figure 14–1 shows the Amplify Physical Optimizer design flow.

Figure 14–1. Software Design Flow



Initial Pass: No Physical Constraints

The initial iteration involves synthesizing the design in the Amplify Physical Optimizer software without physical constraints.

Before beginning the physical synthesis flow, run an initial pass in the Amplify Physical Optimizer without physical constraints. At the completion of every Quartus II compilation, the Quartus II Timing Analyzer performs a comprehensive static timing analysis on your design and reports your design's performance and any timing violations. If the design does not meet performance requirements after the first pass, additional passes can be made in the Amplify software.

Create New Implementations

To set the Amplify Physical Optimizer software options, perform the following steps:

1. Compile the design with the **Resource Sharing** and **FSM Compiler** options selected and the **Frequency** setting specified in MHz. For optimal synthesis, the Amplify software includes the retiming, pipelining, and FSM Explorer options. For designs with multiple clocks, set the frequency of individual clocks with Synthesis Constraints Optimization Environment (SCOPE).

2. Select **New Implementation**. The **Options for Implementation** dialog box appears.

3. Specify the part, package, and speed grade of the targeted device in the **Device** tab.

4. Turn on the **Map Logic to Atoms** option in the **Device Mapping Options** dialog box.

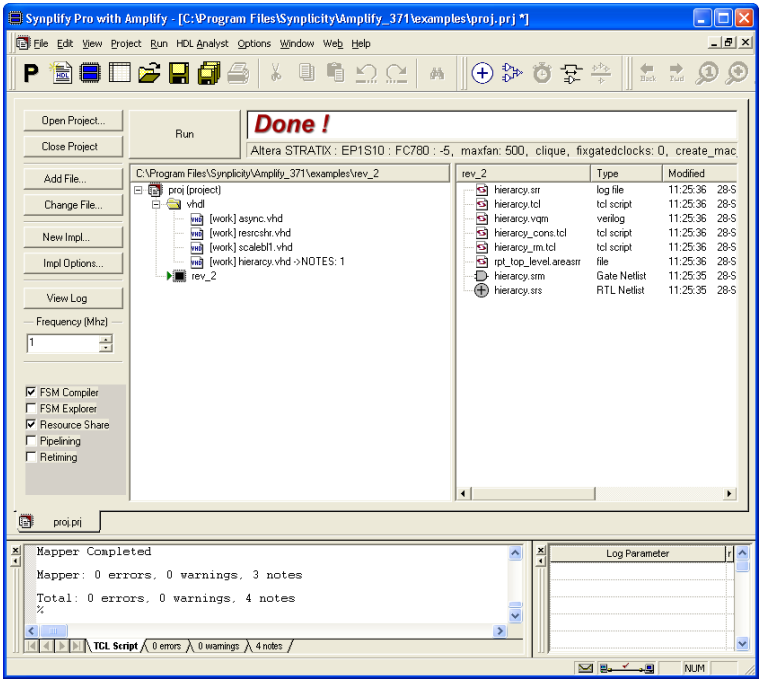
5. Turn off the **Disable I/O Insertion** and **Perform Cliquing** options.

6. Specify the name and directory in the **Implementation Results** tab. The result format should be VQM, and you should select **Optional Output Files** as the **Write Vendor Constraint File** option so that the software can generate the Tcl script containing the project constraints.

7. Specify the number of critical paths and the number of start and end points to report in the **Timing Report** tab. Figure 14–2 shows the main Amplify Physical Optimizer project window.

These steps create a directory where the results of this pass are recorded. Ensure that the Amplify Physical Optimizer software implementation options are set as described in the initial pass.

Figure 14–2. Amplify Physical Optimizer Project Window



Iterative Passes: Optimizing the Critical Paths

In the iterative passes, you optimize the design by placing logic in the device floorplan within the Amplify software. Amplify's floorplan is a high-level view of the device architecture. The floorplan view is dependent upon the target device family. When the Amplify Physical Optimizer re-optimizes the current critical path, additional critical paths may be created. Continue to add new constraints to the existing floorplan until it meets the performance requirements. The design may need several iterations to meet these performance requirements. Since optimizing critical paths involves trying different implementations, the creation of various Amplify project implementations will help in organizing the placement of logic in the floorplan.

Using the Amplify Physical Optimizer Floorplans

When designs do not meet performance requirements with the initial pass through the Amplify Physical Optimizer software, you can create location assignments to reduce interconnect and logic delays to improve your design's performance.

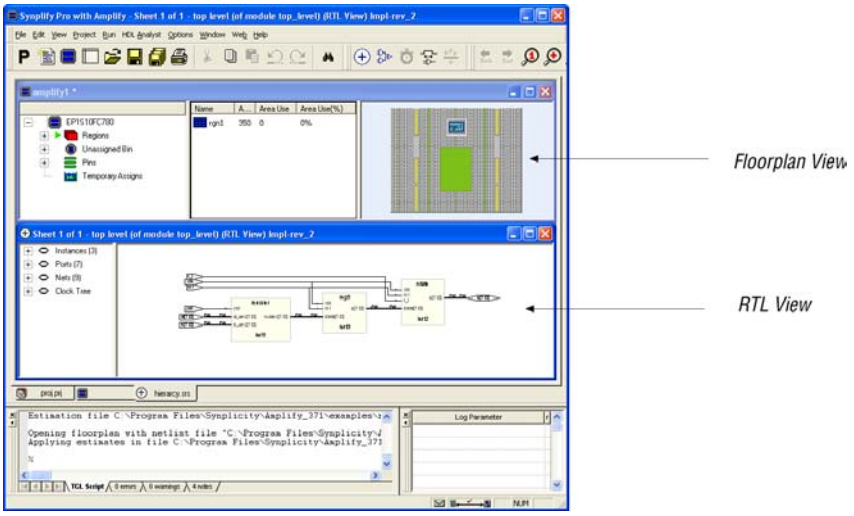
You must determine which paths to constrain based on the critical paths from the previous implementation. When Quartus II projects are launched with the Amplify Tcl script, the Quartus II software generates a **<***revision name***>.tan. rpt** file that lists the critical paths for the design. You can then create custom structure regions for critical paths. After critical paths are implemented in a floorplan with the Amplify Physical Optimizer software, you must resynthesize the design. The software will then attempt to optimize the critical paths and reduce the number of logic levels. After the Amplify Physical Optimizer software resynthesizes the design, the Quartus II software must compile the new implementation. If the design does not meet timing requirements, perform another physical synthesis iteration.

Use the following steps to create a floorplan in the Amplify Physical Optimizer software:

1. Click the **New Physical Constraint File** icon at the top of the Amplify Physical Optimizer window.

2. Click **Yes** on the **Estimation Needed** dialog box; the floorplan window is shown (Figure 14–3).

Figure 14–3. Stratix 1S20 Floorplan in the Amplify Physical Optimizer Software



The floorplan view is located at the top of the screen and the RTL view is at the bottom of the screen.

You can specify modules or individual paths in the Amplify Physical Optimizer software. Using modules can quickly resolve timing problems.

Use the following steps in the software to create a floorplan module:

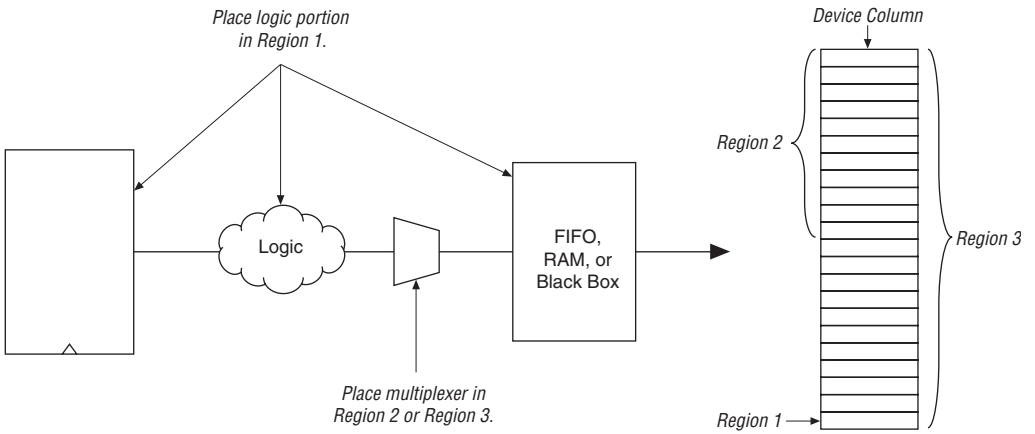
1. Create a region in the Amplify Physical Optimizer device floorplan window and select the module in the RTL view of the design.
2. Drag the module to the new region. The software will then report the utilization of the region.
3. Resynthesize the design in the software to reoptimize the critical path after the modules have location constraints.
4. Write out the placement constraints into the VQM netlist and the Tcl script.

Repeat the above procedure to create as many regions as required.

Multiplexers

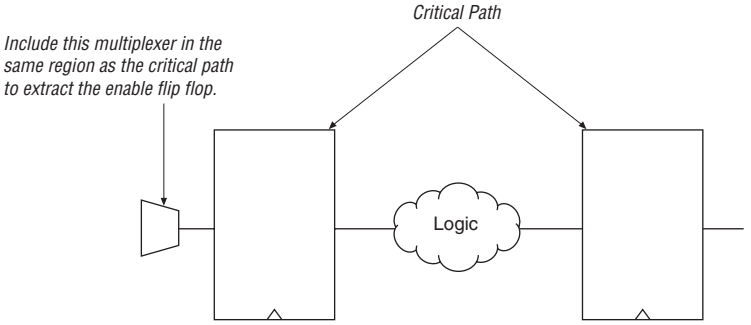
To create a floorplan for critical paths with one or more multiplexers, create multiple regions and assign the multiplexer to one region and the logic to another. Figure 14–4 shows placing critical paths with multiplexers.

Figure 14–4. Placing Critical Paths with Multiplexers



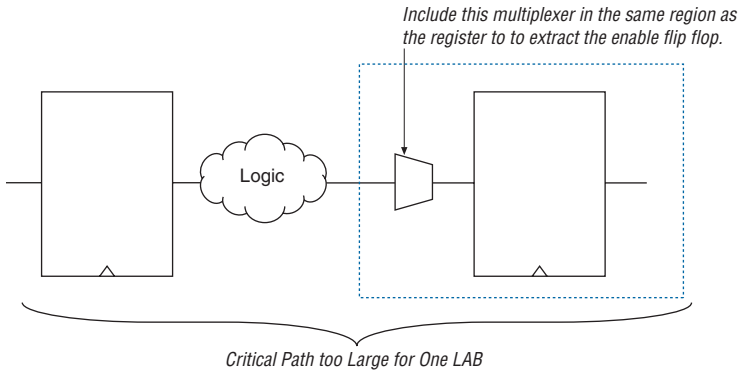
If the critical path contains a multiplexer feeding a register, create a region and place the multiplexer along with the entire critical path in the region (Figure 14–5).

Figure 14–5. Critical Paths with Multiplexers Feeding Registers



If the critical path is too large for the region, divide the critical path and ensure that the multiplexer and register are in the same region. Figure 14–6 shows large critical paths with multiplexers feeding registers.

Figure 14–6. Large Critical Paths with Multiplexers Feeding Registers



Independent Paths

Designs may have two or more independent critical paths. To create an independent path in the Amplify Physical Optimizer software, follow the steps below:

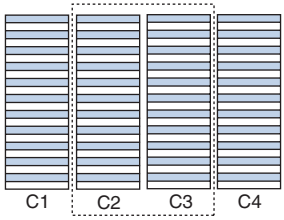
1. Create a region and assign the first critical path to that region.
2. Create another region, leaving one MegaLAB structure between the first and second regions.
3. Assign the second critical path to the second region.

Feedback Paths

If critical paths have the same start and end points, follow the steps below in the Amplify Physical Optimizer software (Figure 14–7):

1. Select the register and instance not directly connected to the register.
2. Right-click and select **Filter Schematic** twice.
3. Highlight the line leading out of the register and either press **P** or right-click the line. Select **Expand Paths**. Assign this logic to a region.

Figure 14–7. Critical Paths with the Same Starting or Ending Points

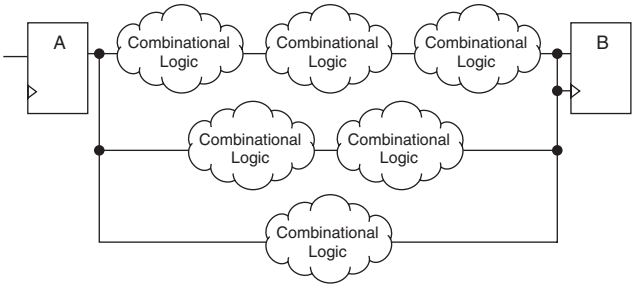


Starting & Ending Points

Figure 14–8 shows a critical path that has multiple starting and ending points. Use **Find** to display all the starting and ending points in the RTL view in Amplify. Expand the paths between those points. If there is unrelated logic between the multiple starting points and ending points,

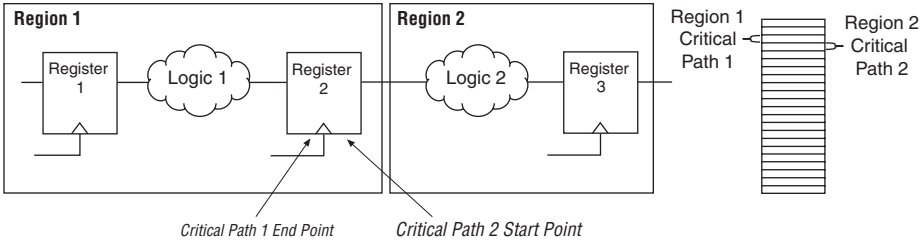
assign the starting points and ending points to the same region. Similarly, if there is unrelated logic between starting points and multiple ending points, assign the starting points and ending points to the same region.

Figure 14–8. Critical Paths with Multiple Starting or Ending Points



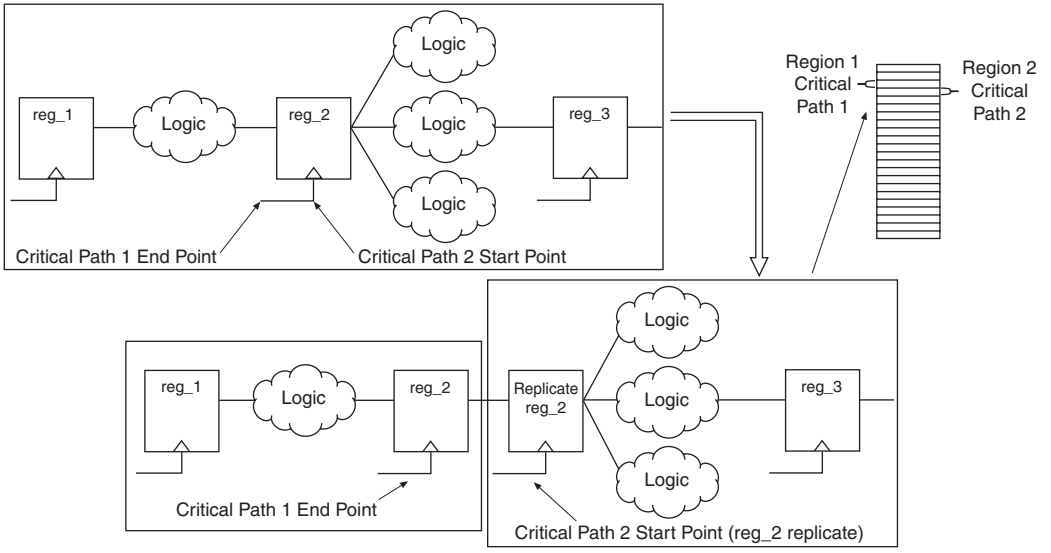
If the two critical paths share a register at the starting or ending point, assign one critical path to one region, and assign the other critical path to an adjacent region. Figure 14–9 shows two critical paths that share a register.

Figure 14–9. Two Critical Paths Sharing a Register



If the fanout is on the shared region, replicate the register and assign both registers to two regions (Figure 14–10). This is done by dragging the same register to the required regions. Entities and nodes are also replicated by performing the same procedure.

Figure 14–10. Fanout on a Shared Region



Utilization

Designs with device utilizations of 90% or higher may have difficulties during fitting in the Quartus II software. If the device has several finite state machines, you should implement the state machines with sequential encoding, as opposed to one-hot encoding.

To check area utilization, check the Amplify Physical Optimizer **log** file and **.srr** file for region utilization, after the mapping stage is complete. On the Run menu, click **Estimate Area** to update the utilization estimates.

Detailed Floorplans

If the critical path does not meet timing requirements after physical optimization, you can create new regions to achieve timing closure. It is recommended that regions do not overlap. Regions should either be entirely contained in another region or remain entirely outside of it. Select the logic requiring optimization from the existing region. Deselect the logic and assign it to the new region. Run the Amplify Physical Optimizer software on the design with the modified physical constraints. Then place and route the design.

Forward Annotating Amplify Physical Optimizer Constraints into the Quartus II Software

The Amplify Physical Optimizer software simplifies the forward annotating of both timing and location constraints into the Quartus II software through the generation of three Tcl scripts. At the completion of a physical synthesis run, in the Amplify Physical Optimizer software, the following Tcl scripts are generated:

- <*project name*>**_cons.tcl**
- <*project name*>**.tcl**
- <*project name*>**_rm.tcl**

Table 14–1 provides a description of each script's purpose.

Table 14–1. Amplify Physical Optimizer Tcl Script Description

Tcl File	Description
<*project name*>**_cons**	This Tcl script will create and compile a Quartus II project. The <*project name*>**.tcl** will automatically be sourced when this script is sourced.
<*project name*>	This script contains forward annotation of constraint information including clock frequency, duty cycle, location, etc.
<*project name*>**_rm**	This script removes any previous constraints from the project. The removed constrainst is saved in <*project name*>**_prev.tcl**

To forward annotate Amplify Physical Optimizer's constraints into the Quartus II software you must use **quartus_cmd**. The **quartus_cmd** command must be used as Amplify Physical Optimizer's Tcl scripts are not compatible with **quartus_sh**. The following command will execute the <*project name*>**_cons**, which will create a Quartus II project with all Amplify Physical Optimizer constraints forward annotated, and will perform a compilation.

```
<command prompt>quartus_cmd f-my_project_cons.tcl ↵
```

You must execute the <*project name*>**_cons.tcl** first.

After compilation, you may customize the project either in the Quartus II GUI or sourcing a custom Tcl script.

Refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook* for more information on creating and understanding Tcl scripts in the Quartus II software.

Altera Megafunctions Using the MegaWizard Plug-In Manager with the Amplify Software

When you use the Quartus II MegaWizard® Plug-In Manager to set up and parameterize a megafunction, it creates either a VHDL or Verilog HDL wrapper file. This file instantiates the megafunction (a black box methodology) or, for some megafunctions, generates a fully synthesizeable netlist for improved results with EDA synthesis tools such as Synplify (a clear box methodology).

Clear Box Methodology

The MegaWizard Plug-In Manager-generated fully synthesizeable netlist is referred to as a clear box methodology because the Amplify Physical Optimizer software can "see" into the megafunction file. The clear box feature enables the synthesis tool to report more accurate timing estimates and take better advantage of timing driven optimization.

To turn on the clear box, go to the Tools menu, and select the **MegaWizard Plug-In Manager.** Turn on the **Generate Clearbox body (for EDA tools only)** option. This option is only for certain megafunctions. If this option does not appear, then clear box models are not supported for the selected megafunction. Turning on this option causes the MegaWizard Plug-In Manager to generate a synthesizable clear box netlist instead of the megafunction wrapper file described in "Black Box Methodology" on page 14–14.

Using MegaWizard Plug-In Manager-generated Verilog HDL Files for Clear Box Megafunction Instantiation

If you check the <*output file*>**_inst.v** option on the last page of the wizard, the MegaWizard Plug-In Manager generates a Verilog HDL instantiation template file for use in your Synplify design. This file can help you instantiate the megafunction clear box netlist file, <*output file*>**.v**, in your top-level design. Include the megafunction clear box netlist file in your Amplify Physical Optimizer project and the information gets passed to the Quartus II software in the Amplify Physical Optimizer-generated VQM output file.

Using MegaWizard Plug-In Manager-generated VHDL Files for Clear Box Megafunction Instantiation

If you check the <*output file*>.**cmp** and <*output file*>**_inst.vhd** options on the last page of the wizard, the MegaWizard Plug-In Manager generates a VHDL component declaration file and a VHDL instantiation template file for use in your design. These files help to instantiate the megafunction clear box netlist file, <*output file*>.**vhd**, in your top-level design. Include

the megafunction clear box netlist file in your Amplify Physical Optimizer project and the information gets passed to the Quartus II software in the Amplify Physical Optimizer-generated VQM output file.

Black Box Methodology

The MegaWizard Plug-In Manager-generated wrapper file is referred to as a black-box methodology because the megafunction is treated as a "black box" in the Amplify Physical Optimizer software. The black box wrapper file is generated by default in the **MegaWizard Plug-In Manager** and is available for all megafunctions.

The black-box methodology does not allow the synthesis tool any visibility into the function module thus not taking full advantage of the synthesis tool's timing driven optimization. For better timing optimization, especially if the black box does not have registered inputs and outputs, add timing models to black boxes.

For more information on instantiating MegaWizard Plug-In Manager modules or black boxes, refer to the *Synplicity Synplify & SynplifyPro Support* chapter in volume 1 of the *Quartus II Handbook*.

Conclusion

Physical synthesis uses improved delay estimation to optimize critical paths. The Amplify Physical Optimizer software uses the hierarchical structure of logic and interconnect in Altera devices so that designers can direct a critical path to be placed into several well-defined blocks. The Amplify Physical Optimizer-to-Quartus II software flow is one of the steps to solving the problem of achieving timing closure through physical synthesis.

Quartus II Version 6.0 Handbook

Volume 3: Verification

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QII5V3_6.0

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Chapter Revision Dates

The chapters in this book, the Quartus II Handbook, Volume 3, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Quartus II Simulator
Revised: *May 2006*
Part number: *QII53017-6.0.0*

Chapter 2. Mentor Graphics ModelSim Support
Revised: *May 2006*
Part number: *QII53001-6.0.0*

Chapter 3. Synopsys VCS Support
Revised: *May 2006*
Part number: *QII53002-6.0.0*

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Revised: *May 2006*
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Revised: *May 2006*
Part number: *QII53014-6.0.0*

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Revised: *July 2006*
Part number: *QII53018-6.0.1*

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Revised: *July 2006*
Part number: *QII53019-6.0.1*

Chapter 8. Classic Timing Analyzer
Revised: *May 2006*
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Part number: *QII53005-6.0.0*

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Revised: *May 2006*
Part number: *QII53013-6.0.0*

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Revised: *May 2006*
Part number: *QII53008-6.0.0*

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Revised: *May 2006*
Part number: *QII53009-6.0.0*

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Revised: *May 2006*
Part number: *QII53016-6.0.0*

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Revised: *May 2006*
Part number: *QII53010-6.0.0*

Chapter 15. In-System Updating of Memory & Constants
Revised: *May 2006*
Part number: *QII53012-6.0.0*

Chapter 16. Cadence Encounter Conformal Support
Revised: *May 2006*
Part number: *QII53011-6.0.0*

Chapter 17. Synopsys Formality Support
Revised: *May 2006*
Part number: *QII53015-6.0.0*

About this Handbook

This handbook provides comprehensive information about the Altera® Quartus® II design software, version 6.0.

How to Contact Altera

For the most up-to-date information about Altera products, go to the Altera world-wide web site at www.altera.com. For technical support on this product, go to www.altera.com/mysupport. For additional information about Altera products, consult the sources shown below.

Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	altera.com/mysupport/
	(800) 800-EPLD (3753) (7:00 a.m. to 5:00 p.m. Pacific Time)	(408) 544-7000 *(1)* (7:00 a.m. to 5:00 p.m. Pacific Time)
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com *(1)*	literature@altera.com *(1)*
Non-technical customer service	(800) 767-3753	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)
FTP site	ftp.altera.com	ftp.altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Third-Party Software Product Information

Third-party software products described in this handbook are not Altera products, are licensed by Altera from third parties, and are subject to change without notice. Updates to these third-party software products may not be concurrent with Quartus II software releases. Altera has assumed responsibility for the selection of such third-party software products and its use in the Quartus II 6.0 software release. To the extent that the software products described in this handbook are derived from third-party software, no third party warrants the software, assumes any liability regarding use of the software, or undertakes to furnish you any support or information relating to the software. EXCEPT AS EXPRESSLY SET FORTH IN THE APPLICABLE ALTERA PROGRAM LICENSE SUBSCRIPTION AGREEMENT UNDER WHICH THIS SOFTWARE WAS PROVDED TO YOU, ALTERA AND THIRD-PARTY LICENSORS DISCLAIM ALL WARRANTIES WITH RESPECT TO THE USE OF SUCH THIRD-PARTY SOFTWARE CODE OR DOCUMENTATION IN THE SOFTWARE, INCLUDING, WITHOUT LIMITATION, ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND NONINFRINGEMENT. For more information, including the latest available version of specific third-party software products, refer to the documentation for the software in question.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section I. Simulation

As the design complexity of FPGAs continues to rise, verification engineers are finding it increasingly difficult to simulate their system-on-a-programmable-chip (SOPC) designs in a timely manner. The verification process is now the bottleneck in the FPGA design flow. You can perform functional and timing simulation of your design by using the Quartus® II Simulator. The Quartus II software also provides a wide range of features for performing simulation of designs in EDA simulation tools.

This section includes the following chapters:

Revision History

The following table shows the revision history for Chapters 1 to 5.

Chapter(s)	Date / Version	Changes Made
1	May 2006 v6.0.0	Initial release.
2	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Added a section on setting ModelSim as the Simulation Tool • Updated EDA Tools Settings in the GUI. • Updated the Synopsys Design Constraints File information. • Updated the device information. • Added Quartus II-Generated Testbench information • Updated megafunction information.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	• Updates to tables, figures. • Updated information. • New functionality for Quartus II software 5.0.
	Dec. 2004 v3.0	• Reorganized chapter, updated information. • Updates to tables, figures. • New functionality for Quartus II software 4.2.
	June 2004 v2.0	• Updates to tables, figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.
3	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Added a section on setting VCS as the Simulation Tool • Updated EDA Tools Settings in the GUI. • Updated the Synopsys Design Constraints File information. • Added transceiver information to simulating designs. • Added Quartus II-Generated Testbench information • Updated megafunction information.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	• Updated information. • Updated tables. • Added Using NativeLink® with VCS section. • New functionality for Quartus II software 5.0.
	Dec. 2004 v2.1	• Updates to tables, figures. • New functionality for Quartus II software 4.2.
	June 2004 v2.0	• Updates to tables and figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.

Chapter(s)	Date / Version	Changes Made
4	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: ● Added a section on setting VCS as the Simulation Tool ● Updated EDA Tools Settings in the GUI. ● Updated the Synopsys Design Constraints File information. ● Added pulse_e and pulse_r information to simulation sections. ● Added Quartus II-Generated Testbench information ● Updated megafunction information.
	December 2005 v5.1.1	● Removed reference to convert_hex2ver.obj.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	● Updated information. ● Added Using NativeLink with NC-Sim section. ● New functionality for Quartus II software 5.0.
	Dec. 2004 v3.0	Reorganized chapter and updated information.
	Aug. 2004 v2.1	● New functionality for Quartus II software 4.1 SP1.
	June 2004 v2.0	● Updates to tables and figures. ● New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.
5	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	Chapter 4 was formerly in Section I, Vol 3 in 4.2.
	Dec. 2004 v1.0	Initial release.

1. Quartus II Simulator

QII53017-6.0.0

Introduction

With today's FPGAs becoming faster and more complex, designers face challenges in validating their designs. Simulation verifies the correctness of the design, reducing board testing and debugging time.

Altera® offers the Simulator as part of the Quartus® II software to assist designers with design verification. The Quartus II Simulator has a comprehensive set of features that are covered within the following topics:

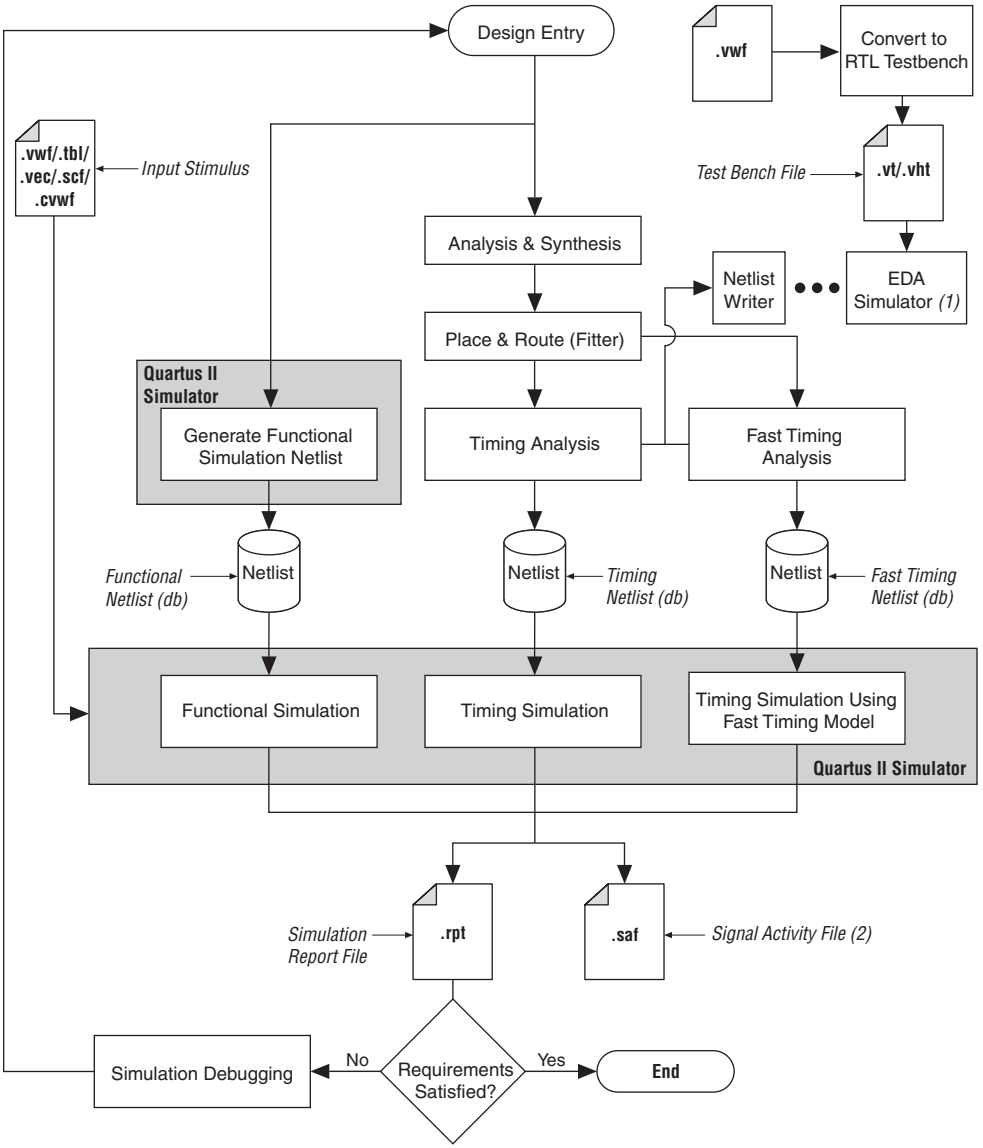
- Simulation flow
- Waveform Editor
- Simulator settings
- Simulation report
- Debugging with the Quartus II Simulator
- Scripting support

This chapter describes how to perform different types of simulations with the Quartus II Simulator.

Simulation Flow

You can perform both functional and timing simulations with the Quartus II Simulator. Functional simulations verify the behavior of your design and timing simulations verify the correctness of your design with timing delays. Figure 1–1 shows the Quartus II Simulator flow.

Figure 1–1. Simulation Flow



Notes to Figure 1–1:

(1) For more information on EDA Simulators, refer to the *Simulation* section in volume 3 of the *Quartus II Handbook*.

(2) You can use Signal Activity Files (**.saf**) in the PowerPlay Power Analyzer to check power resources.

To functionally simulate a design, you must first generate a functional simulation netlist. A functional netlist file is a flattened netlist extracted from the design files that does not contain timing information because the Fitter has not been run.

For timing simulations, you must first perform place and route and static timing analysis to generate a timing simulation netlist. A timing simulation netlist includes timing delays of each device atom block and the routing delays.

For third-party EDA simulators, generate an EDA netlist with the EDA Netlist Writer and simulate the netlist together with your testbench.

For more information on third-party simulators, refer to the respective EDA Simulation chapter in the *Simulation* section in volume 3 of the *Quartus II Handbook*.

After performing place and route, you can run any of the three types of simulation modes: Functional, Timing, or Timing using Fast Timing Model. The three modes are used for different simulation needs. For example, in functional simulation, only the logical behavior is important.

Functional Simulation

To run a functional simulation, perform the following steps:

1. On the Processing menu, click **Generate Functional Simulation Netlist**. This flattens the functional simulation netlist extracted from the design files. The netlist does not contain timing information.
2. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
3. In the **Category** list, select **Simulator Settings**. The **Simulator Settings** page is shown.
4. In the **Simulation mode** list, select **Functional**.
5. In the **Simulation input** box, specify the vector source. You must specify the vector file in order to run the simulation.
6. Click **OK**.
7. On the Processing menu, click **Start Simulation**.

Timing Simulation

To run a timing simulation, perform the following steps:

1. On the Processing menu, click **Start Compilation**. This flattens the design and generates an internal netlist with timing delay information annotated.

   Or you can follow these steps:

   a. On the Processing menu, point to Start and click **Start Analysis & Synthesis**.

   b. On the Processing menu, point to Start and click **Start Fitter**.

   c. On the Processing menu, point to Start and click **Start Timing Analyzer**.

2. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.

3. In the **Category** list, select **Simulator Settings**. The **Simulator Settings** page is shown.

4. In the **Simulation Mode** list, select **Timing**.

5. In the **Simulation input** list, specify the vector source. You need to specify the vector file in order to run the simulation.

6. Click **OK**.

7. On the Processing menu, click **Start Simulation**.

Timing Simulation Using Fast Timing Model Simulation

To run a timing simulation using a fast timing model, perform the following steps:

1. On the Processing menu, click **Start Compilation**. This flattens the design and generates an internal netlist with fast timing delay information annotated.

Or you can follow these steps:

a. On the Processing menu, point to Start and click **Start Analysis & Synthesis**.

b. On the Processing menu, point to Start and click **Start Fitter**.

You must perform fast timing analysis before you can perform a timing simulation using the fast timing models.

2. On the Processing menu, point to Start and click **Start Timing Analysis (Fast Timing Model)**.
3. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
4. In the **Category** list, select **Simulator Settings**. The **Simulator Settings** page is shown.
5. In the **Simulation mode** list, select **Timing using Fast Timing Model**.
6. In the **Simulation input** box, specify the vector source. You need to specify the vector file in order to run the simulation.
7. Click **OK**.
8. On the Processing menu, click on **Start Simulation**.

Waveform Editor

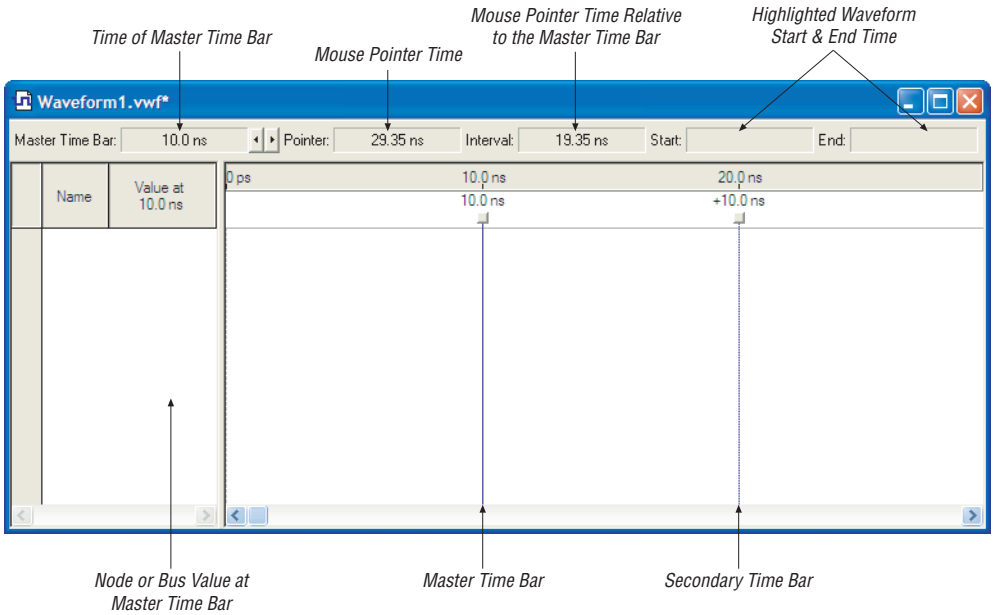
The most common input stimulus for the Quartus II Simulator are Vector Waveform Files (**.vwf**). You can use the Waveform Editor to generate a Vector Waveform File.

Creating Vector Waveform Files

To create a Vector Waveform File, perform the following steps:

1. On the File menu, click **New**. The **New** dialog box appears.
2. Click the **Other Files** tab, and select **Vector Waveform File**.
3. Click **OK**. A blank Waveform Editor window appears (Figure 1–2).

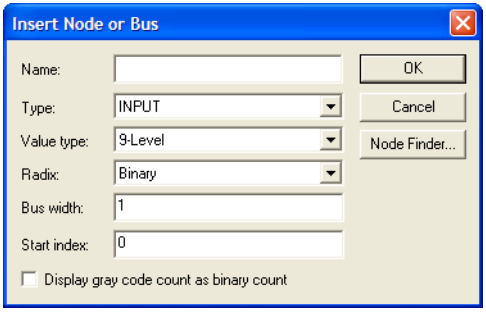
Figure 1–2. Waveform Editor Window



4. Add nodes and buses. To add a node or bus, on the Edit menu, click **Insert Node or Bus**. The **Insert Node or Bus** dialog box appears (Figure 1–3). All nodes and buses, as well as the internal signals, are listed under **Name** in the Waveform Editor window.

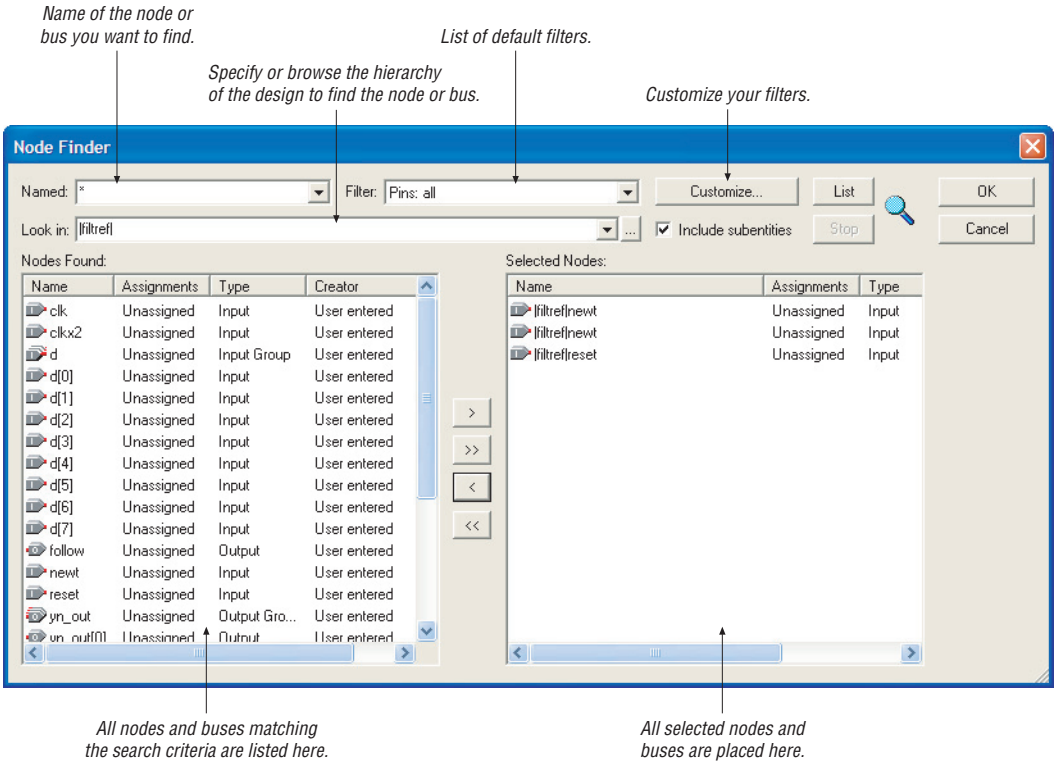
You can also open the **Insert Node or Bus** dialog box by double-clicking under **Name** in the Waveform Editor.

Figure 1–3. Insert Node or Bus Dialog Box



5. You can customize the type of node or bus you want to add. If you have a large design with many nodes or buses, you may want to use the Node Finder for node or bus selection. To use the Node Finder, click **Node Finder**. The **Node Finder** dialog box appears (Figure 1–4).

Figure 1–4. Node Finder Dialog Box



You can use the Node Finder to find your nodes for simulation among all the nodes and buses in your design. Use the Node Finder to filter and add nodes to your waveform. The Node Finder is equipped with multiple default filter options. By using the correct filter in the Node Finder, you can find the internal node's name and add it to your Vector Waveform File for simulation.

Table 1–1 describes twelve of the Node Finder default filters.

Table 1–1. Filter Options

Filter	Description
Pins: input	Finds all input pin names in your design file(s).
Pins: output	Finds all output pin names in your design file(s).
Pins: bidirectional	Finds all bidirectional pin names in your design file(s).
Pins: virtual	Finds all virtual pin names.
Pins: all	Finds all pin names in your design file(s).
Registers: pre-synthesis	Finds all user-entered register names contained in the design after design elaboration, but before physical synthesis does any synthesis optimizations.
Registers: post-fitting	Finds all user-entered register names in your design file(s) that survived physical synthesis and fitting.
Design Entry (all names)	Finds all user-entered names in your design file(s).
Post-Compilation	Finds all user-entered and compiler-generated names that do not have location assignments and survived fitting.
SignalTap II: pre-synthesis	Finds all internal device nodes in the pre-synthesis netlist that can be analyzed by the SignalTap® II Logic Analyzer.
SignalTap II: post-fitting	Finds all internal device nodes in the post-fitting netlist that can be analyzed by the SignalTap II Logic Analyzer.
SignalProbe	Finds all SignalProbe™ device nodes in the post-fitting netlist.

To customize your own filters in the Node Finder, perform the following steps:

a. Click **Customize**. The **Customize Filter** dialog box appears.

b. To configure settings, click **New**. The **New Custom Filter** dialog box appears.

c. In the **Filter name** box, type the name of the custom filter.

d. In the **Copy settings from filter** list, select the filter setting.

e. Click **OK**.

f. You can now customize your filters in the **Customize Filter** dialog box.

6. In the **Look in** box, you can view and edit the current search hierarchy path. You can type the search hierarchy path or you can browse for the hierarchy path by clicking the browse button.

You can move up the search hierarchy by selecting hierarchical names in the **Select Hierarchy Level** dialog box. This ensures that in a large design with many signals, you can specify which hierarchy you would like to get the node from to reduce the amount of signals displayed.

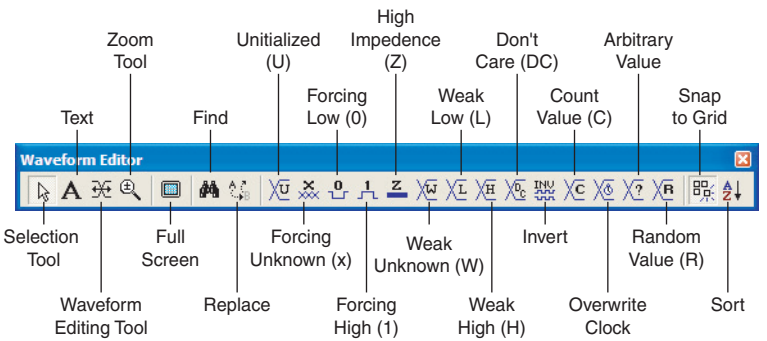
7. After you have configured the filter and specified the correct hierarchy in the **Node Finder** dialog box, click **List** to display all relevant nodes or buses.

   Select any node(s) or bus(es) from the **Nodes Found** list and click **>** to include it in the waveform, or you can click **>>** to include all nodes and buses displayed in the **Nodes Found** list.

8. Click **OK**.

9. Create a waveform for a signal. The Quartus II Waveform Editor toolbar includes some of the most common waveform settings, making waveform vector drawings easier and user friendly. Figure 1–5 shows the options available on the Waveform Editor toolbar.

Figure 1–5. Waveform Editor Toolbar

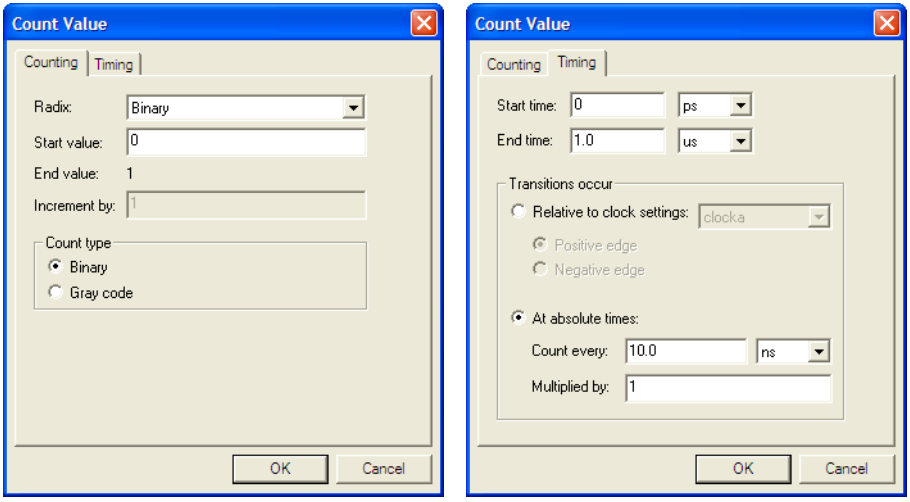


10. After you edit your waveform, save the waveform. On the File menu, click **Save As**. The **Save As** dialog box appears. Type your file name and specify the file type, and click **Save**.

Count Value

Count Value applies a count value to a bus to increment the value of the bus by a specified time interval. Instead of manually editing the values for each node, the Count Value feature on the Waveform Editor toolbar automatically creates the counting values for buses. This feature enables you to specify a starting value for a bus, what time interval to increment, and when to stop counting. You can also configure transition occurrences, while setting the count type and increment number. When you click on the **Count Value** button in the Waveform Editor toolbar, the **Count Value** dialog box appears (Figure 1–6). You can also open the **Count Value** dialog box by right-clicking the selected node, pointing to Value, and clicking **Count Value**.

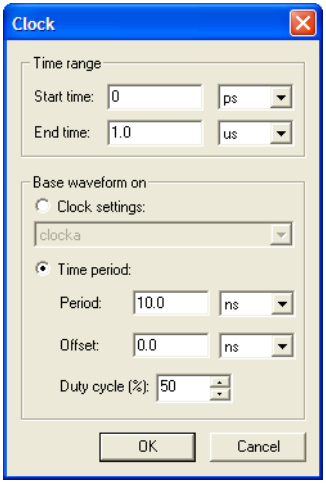
Figure 1–6. Count Value Dialog Box



Clock

You can use the Clock feature in the Waveform Editor toolbar to automatically generate the clock wave, rather than drawing each clock triggering pulse. To generate a clock signal with the **Clock** dialog box, click the **Overwrite Clock** button on the Waveform Editor toolbar. Furthermore, you can determine the start and end time of a clock signal, whether to manually configure the period (the offset and the duty cycle), or whether to generate the clock based on a specified clock. Figure 1–7 shows the **Clock** dialog box.

Figure 1–7. Clock Dialog Box

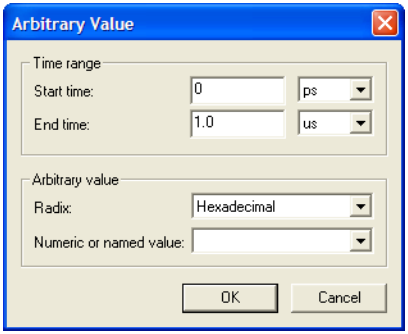


Arbitrary Value

Arbitrary Value allows you to overwrite a node value over the selected waveform, waveform interval, or across one or more nodes or groups. To overwrite a node value, perform the following steps:

1. Select a node or a bus and click the **Arbitrary Value** button on the Waveform Editor toolbar (Figure 1–5). The **Arbitrary Value** dialog box appears (Figure 1–8).
2. Under **Time range**, specify the start and end time you want to overwrite for the node value.
3. In the **Radix** list, select the radix type.
4. Specify the new value you want overwritten in the **Numeric or named value** box.
5. Click **OK**.

Figure 1–8. Arbitrary Value Dialog Box



Generating a Testbench

You can export your Vector Waveform File as a VHDL Test Bench File (**.vht**) or Verilog Test Bench File (**.vt**). This is useful when you want to use a vector waveform in different EDA tools. To export a waveform vector, have your vector waveform open and perform the following steps:

1. On the File menu, click **Export**. The **Export** dialog box appears.
2. In the **Save as type** list, select **VHDL Test Bench File (*.vht)** or **Verilog Test Bench File (*.vt)**.
3. You can optionally turn on **Add self-checking code to file**. This option adds additional logic to check the results of the output and compares it to the original Vector Waveform File.

You must open your project in the Quartus II software before you can export a Vector Waveform File.

For more information on using the generated test bench in other EDA tools, refer to the respective EDA simulator chapter in the *Simulation* section in volume 3 of the *Quartus II Handbook*.

Grid Size

When you select portions of your waveform, the selection area snaps to time intervals specified in the **Grid Size** dialog box. You can customize the grid size in the Waveform Editor. You can change the grid size based on the clock settings or by setting the time period. To customize the grid size, on the Edit menu, click **Grid Size**.

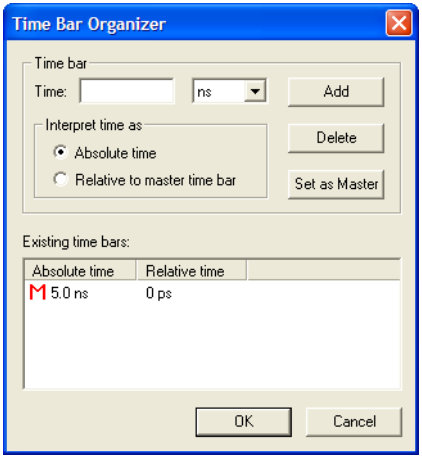
Time Bars

Add time bars in the Waveform Editor to compare edges between different signals. You can also use time bars to jump forward and backward to the next edge transition in the selected signal, and read the logic level of signals by sliding the Time Bar in your waveform. The logic level is displayed in the **Value at** column of the Waveform Editor.

The **Time Bar Organizer** dialog box enables you to create, delete, and edit a time bar, and to create a master time bar. Only one master time bar is allowed per waveform file. To use the Time Bar Organizer, on the Edit menu, click **Time Bar Organizer**.

Under **Existing time bars**, in the **Absolute time** column, the red **M** indicates the master time bar (Figure 1–9).

Figure 1–9. Time Bar Organizer Dialog Box



Grow or Shrink a Signal Waveform

You can grow or shrink a waveform interval in the Waveform Editor, which enables you to analyze the effects on a compressed or expanded waveform. For example, you can check the behavior of your design at high speeds for a short interval by using the shrink option to compress the waveform. You can also use this feature to delay the transition of a signal by growing the waveform.

You have to specify the original start and end time, and the new time for the waveform you want to shrink or grow. If you want to grow or shrink all the nodes or buses, deselect all nodes and buses and set the shrink or grow feature.

To grow or shrink a waveform or waveform interval, on the Edit menu, click **Grow or Shrink**. The **Grow or Shrink** dialog box appears.

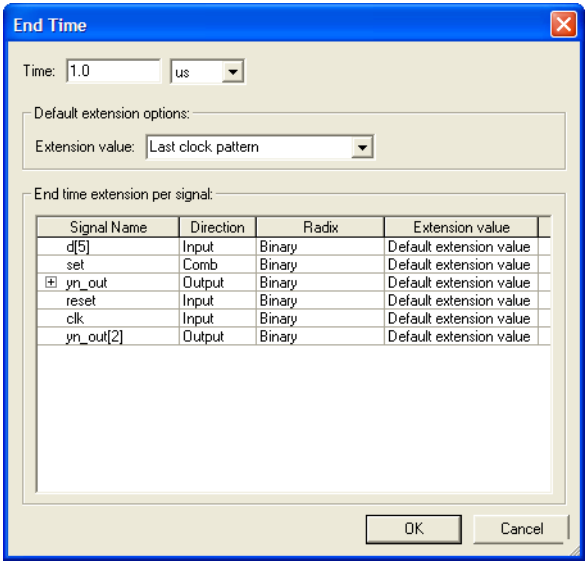
The end time specified in the **Grow or Shrink** dialog box cannot be larger then the End Time specified in the **Simulator Settings** page of the **Settings** dialog box (Figure 1–11). Otherwise, the Quartus II software displays a message indicating the invalid time value.

End Time

The End Time setting enables you to change the end time of the Vector Waveform File. The end time represent the maximum length of time in the Vector Waveform File. You can specify the end time and your preferred time unit, and have different extension values for different nodes or buses. With the waveform open, specify the end time by performing the following steps:

1. On the Edit menu, click **End Time**. The **End Time** dialog box appears (Figure 1–10).

Figure 1–10. End Time Dialog Box



2. In the **Time** box, specify the end time and select the time unit in the **Time** list.

3. Under **Default extension options**, select the **Extension value**.

4. Under **End time extension per signal**, you can select specific extension values for each signal by clicking in the **Extension value** column.

The options in the **End time** dialog box are different settings than those under **Simulation period** in the **Settings** dialog box. Simulation period is the period that the Quartus II software simulates the stimuli. End time is the maximum length of time in the Vector Waveform File. For information on the simulation period, refer to Table 1–2 on page 1–17.

Simulator Settings

You can enhance your output, reduce debugging time, and provide better coverage before running a simulation. This section covers the different simulation modes supported by the Quartus II Simulator. Additionally, the Quartus II Simulator offers common setup features like glitch filtering, setup and hold violation detection, and simulation coverage.

To setup simulation settings, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.

2. In the **Category** list, select **Simulator Settings**. The **Simulator Settings** page is shown (Figure 1–11).

Figure 1–11. Simulator Settings Page

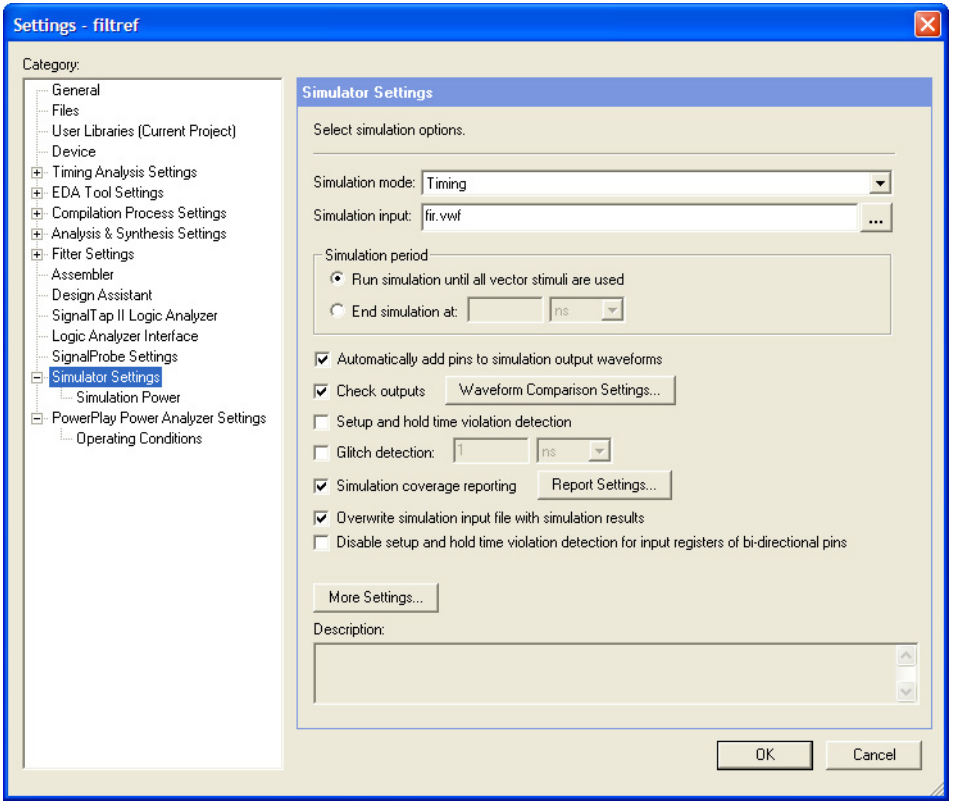


Table 1–2 shows the options in the **Simulator Settings** page.

Table 1–2. Quartus II Simulator Settings (Part 1 of 3)

Settings & Options	Description
Simulation mode *(1)*	**Functional** This simulation mode uses a pre-synthesis compiler database to simulate the logical performance of a project without the timing information. This mode enables you to check the simulation coverage of a design. All nodes and buses are preserved in this simulation because functional simulation is performed before synthesis, partitioning, or fitting. A Vector Waveform File is required to perform this simulation mode. **Timing** This simulation mode takes the compiled netlist that includes timing information. With this simulation mode, you can check setup, hold violation, glitches, and simulation coverage. You can remove nodes or buses using the Quartus II Compiler when logic is optimized. This simulation mode uses the worst case timing model. **Timing using Fast Timing Model** This simulation mode is similar to timing simulation but this mode uses the best-case timing model.
Simulation input	You must include the vector file in the **Simulation input** box. You can type the name of the file or use the browse button. In the **Files of type** list, you can select **Vector Waveform File (*.vwf)**, **Compressed Vector Waveform File (*.cvwf)**, **Vector Text File (*.vec)**, or **All File (*.*)**.
Simulation period	The simulation period determines the length of time that the simulator runs the stimuli with the maximum period being equal to the end time of a Vector Waveform File. If the simulation period is configured shorter than the end time, all signals beyond the simulation period are displayed as Unknown (X). Therefore, you can also shorten the simulation period or end the simulation earlier by selecting **End Simulation at** and specifying the time and selecting the time unit.
Automatically add pins to simulation output waveforms	The **Automatically add pins to simulation output waveforms** option automatically adds all outputs that are available in the design to the waveform reports. If your design has large amounts of outputs, turning on this option ensures all outputs are monitored during simulation.
Check outputs	**Check outputs** checks expected outputs against actual outputs in the simulation report. After turning on **Check outputs**, click the **Waveform Comparison Settings** button. The **Waveform Comparison Settings** dialog box appears. In the **Waveform Comparison Settings** dialog box, you can specify the waveform comparison time frame and the comparison options. You can also set the tolerance level for all the signals by specifying the tolerance limit in the **Default comparison timing tolerance** box. The **Maximum comparison mismatches** box is the amount of mismatches the Quartus II Simulator is allowed to accept before it stops simulating. You can also set the type of transition the comparison should trigger in the **Waveform Comparison Settings** dialog box. You can assign trigger comparisons based on **Input signal transition edges**, **All signal transition edges**, or **Selected Signal transition edges**.

Table 1–2. Quartus II Simulator Settings (Part 2 of 3)

Settings & Options	Description
Setup and hold time violation detection	This option detects setup and hold time violation. Setup time is the period required by a synchronous signal to stabilize before the arrival of a clock edge. Hold time is the time required by a synchronous signal to maintain after the same clock edge. If the **Setup and hold time violation detection** option is turned on, a warning in the Messages windows appears if any setup or hold time violation is detected during the simulation. This option is only for Timing and Timing using Fast Timing Model simulation modes.
Glitch detection	Racing conditions happen when two or more signals transition simultaneously and can cause glitches or unwanted short pulses. The **Glitch detection** option enables you to detect glitches and specify the time interval that defines a glitch. If two logic level transitions occur in a period shorter than the specified time period, the resulting glitch is detected and reported in the **Processing** tab of the Messages window. If you turn on the **Glitch detection** option, you can specify the acceptable glitch width. A Messages window appears when a pulse is smaller than the specified glitch width that is detected. The **Glitch detection** option is only available for Timing and Timing using Fast Timing Model simulation modes.
Simulation coverage reporting	This option reports the ratio of outputs (coverage) actually simulated to the number of outputs in the netlist and is expressed as a percentage. When you turn on the **Simulation coverage reporting** option, the **Report Settings** button is available. If you click **Report Settings**, the **Report Settings** dialog box appears. The three types of coverage reports you can select from are **Display complete 1/0 value coverage report**, **Display missing 1-value coverage report**, and **Display missing 0-value coverage report**.
Overwrite simulation input file with simulation results *(2)*	This option overwrites the vector source file with simulation results. This option is ignored when the **Check outputs** setting is turned on. This option adds the result to the vector file and generally, it can give you more visibility during the debugging process.
Disable setup and hold time violation detection for input registers of bi-directional pins	This option enables you to disable setup and hold time violations detection in input registers of all bidirectional pins in the simulated design during Timing or Timing using Fast Timing Model simulation.

Table 1–2. Quartus II Simulator Settings (Part 3 of 3)

Settings & Options	Description
More Settings	If you click **More Settings**, the **More Simulator Settings** dialog box appears. The following options are available under **Existing option settings**. **Glitch Filtering** This option determines whether or not to filter out the glitch when the **Generate Signal Activity File** option is turned off. You can filter glitches when generating a Signal Activity File for power analysis. For more information on Signal Activity Files and the **Generate Signal Activity File** option, refer to "Power Estimation" on page 1–20. **Group bus channels in simulation results** This option automatically groups bus channels in the output waveform that are shown in the simulation reports. By turning off this option, all output waveforms have a node to represent each bus signal. **Preserve fewer signal transition to reduce memory requirements** This option is effective on lower performance workstations because turning on this option flushes signal transitions from memory to disk for memory optimization.

Notes to Table 1–2:

(1) The Quartus II Simulator may flag an error message if zero-time oscillation happens in your design. Zero-time oscillation happens when a particular output signal does not achieve a stable output value at a particular fixed time, which may be due to your design containing combinational logic path loops.

(2) A backup copy of the source vector file is saved under the db folder with the name <*project*>**.sim_ori.**<*vector file format type*>.

Simulation Vectors

The Quartus II Simulator supports various stimulus files, including:

- Vector Waveform File (**.vwf**)
- Compressed Vector Waveform File (**.cvwf**)
- Vector Table Output File (**.tbl**)
- Vector File (**.vec**)
- Simulation Channel File (**.scf**)

Vector Table Output Files contain input vectors and output logic levels in tabular-format list. You can generate this file using a Vector Waveform File. However, if you would like to maintain, view, or update the vectors, Vector Waveform Files offer better visibility. Vector Waveform File or Vector Table Output File formats are interchangeable with each other. You can generate Table Output Files from Vector Waveform Files and vice versa. You can create a Vector Waveform File with the Waveform Editor. For more information on the Waveform Editor, refer to "Waveform Editor" on page 1–5.

The Quartus II software also supports MAX+PLUS® II simulation vector files, such as Vector Files (**.vec**) and Simulation Channel Files (**.scf**).

A Compressed Vector Waveform File is the simplified version, non-readable, format of the Vector Waveform File format. This file type is in binary format and is generally smaller in file size. You can use Compressed Vector Waveform Files in the Waveform Editor and simulation.

Power Estimation

When you perform your simulation with the Quartus II Simulator, you can generate a Signal Activity File, which is used by the PowerPlay Power Analyzer to assist you with power analysis. The Signal Activity File contains toggle rate and statistic probability. To generate a Signal Activity File, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, click the **+** icon to expand **Simulator Settings** and select **Simulation Power**. The **Simulation Power** page is shown.
3. Turn on **Generate Signal Activity File** and specify the name and location of the file.
4. Click **Signal Activity File Options**. The **Signal Activity File Options** dialog box appears.
5. Select your preferred option for the Signal Activity File.
6. Click **OK**.
7. In the **Settings** dialog box, in the **Category** list select **Simulator Settings** and specify the input stimuli and select the simulation options.
8. Click **OK**.
9. Run the simulation.

For more information on the PowerPlay Power Analyzer, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Simulation Report

Comprehensive reports are shown after the completion of each simulation. These reports are important to ensure designs meet timing and logical correctness. These simulation reports also play an important role in debugging.

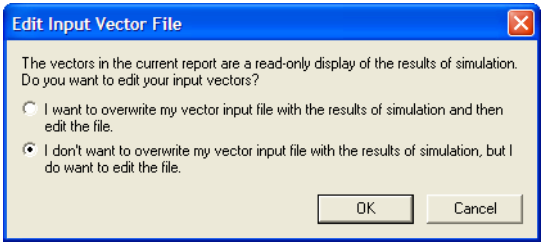
Simulation Waveform

Simulation Waveforms are part of the Simulation report. In this report, the stimuli and the results of the simulation are displayed. Any undefined vector source is automatically set to Unknown (X).

You can export the simulation waveform as a VHDL Test Bench File or a Verilog Test Bench File for use in other EDA tools. You can also save a simulation as a Vector Waveform File or Vector Table Output File for use with the Quartus II software.

When you try to edit the Simulation Waveform, the **Edit Input Vector File** dialog box appears asking whether you would like to edit the vector input file with the results of the simulation or if you would like to overwrite the vector input file with other vector inputs (Figure 1–12).

Figure 1–12. Edit Input Vector File



You can overwrite your simulation input file with the simulation results so that your input vector file is updated with the resulting waveform after a simulation. For more information, refer to the **Overwrite simulation input file with simulation results** option in Table 1–2.

Logical Memories Report

If you use memory cells in your design, you can analyze the contents of the logic memory structures in the device in the Logical Memories Report. The Logical Memories Report displays individual reports for each memory block and contains the data stored in the memory cell used at the end of simulation.

Simulation Coverage Reports

The **Coverage Summary** report contains the following summary information for the simulation:

- Total toggling coverage as a percentage
- Total nodes checked in the design
- Total output ports checked
- Total output ports with complete 1/0-value coverage
- Total output ports with no 1/0-value coverage
- Total output ports with no 1-value coverage
- Total output ports with no 0-value coverage

The **Complete 1/0-Value Coverage** report lists the following information:

- Node name
- Output port name
- Output port type for output ports that toggle between 1 and 0 during the simulation

The **Missing 0-Value Coverage** report and **Missing 1-Value Coverage** report list the following information:

- Node name
- Output port name
- Output port type for output ports that do not toggle to the designated value

For more information on the **Simulation Coverage** reports, refer to the **Simulation coverage reporting** option in Table 1–2.

The following are individual reports and their definition:

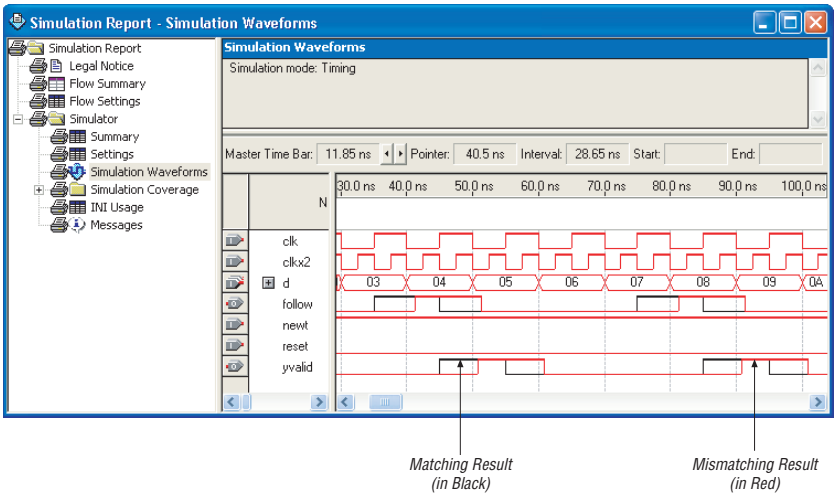
Complete 1/0 value coverage report
Displays all the nodes or buses that toggle between 1 and 0 during simulation.

Missing 1-value coverage and **Missing 0-value coverage reports**
Displays all the nodes that do not toggle to the designated value.

Comparing Two Waveforms

You can compare your simulation results against previous simulations using the compare option. To compare two waveforms in the **Simulation Report**, turn on the **Check outputs** option. For more information on the **Check outputs** option, refer to Table 1–2. With the **Check outputs** option turned on, the two comparable waveforms are visible in black and red. The black waveforms represent the matching output, and the red waveforms represent mismatches between expected output data versus the actual data. Figure 1–13 shows an example of expected data versus actual data.

Figure 1–13. Example of Simulation Waveform from the Simulation Report When Check Output is Turned On



Debugging with the Quartus II Simulator

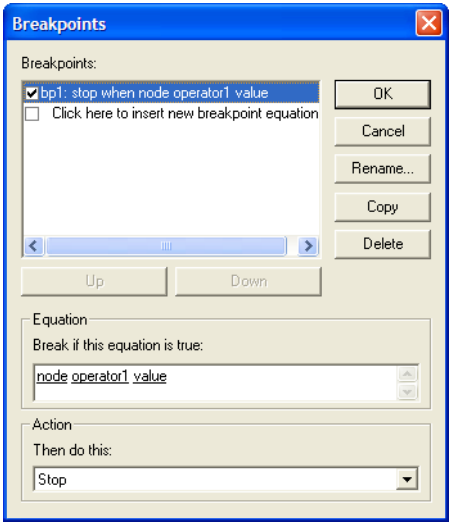
The Quartus II software includes tools to help with simulation debugging. This section covers some debugging tools and their use.

Breakpoints

Inserting breakpoints into the simulation process enables the simulator to break at the desired time or on the desired node or bus condition. You can monitor the activity of nodes or buses during specified times and pinpoint the cause of mismatched signal levels between expected and actual. To use breakpoints, perform the following steps:

1. On the Processing menu, point to Simulation Debug and click **Breakpoints**. The Breakpoints dialog box appears (Figure 1–14).

Figure 1–14. Breakpoints Dialog Box



2. Under **Equation**, click **condition**. You can configure the logical conditions of individual nodes or buses, or you can set the time.

3. After you configure the equation conditions, select the action for the Quartus II Simulator. In the **Then do this** list, select **Stop**, **Warning Message**, **Error Message**, or **Information Message**. This selection defines the action once the condition is met.

Updating Memory Content

If your design includes memories, when the simulator stops at a breakpoint, you can view and edit the contents of the memories. To view your memories during a breakpoint in the simulation, on the Processing menu, point to Simulation Debug and click **Embedded Memory**.

Last Simulation Vector Outputs

The Last Simulation Vector Outputs command opens the Output Simulation Waveforms report generated by the last simulation. To use this command, on the Processing menu, point to Simulation Debug and click **Last Simulation Vector Outputs**.

You can open the current input vectors that you defined in the **Simulator Settings** dialog box with the Current Vector Inputs command. To use this command, on the Processing menu, point to Simulation Debug and click **Current Vector Inputs**. Lastly, you can overwrite the vector source file with the simulation outputs which open the resulting file.

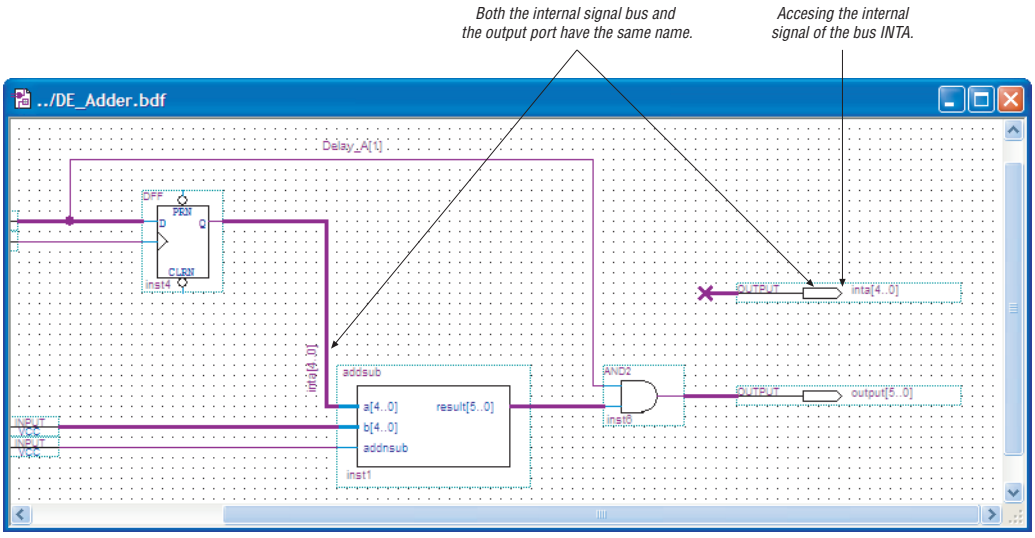
Conventional Debugging Process

During the design phase, tapping out internal signals is a common practice to debug simulation errors. Therefore, the Quartus II software enables you to tap out the signal for simulation debug and also enables you to pull out the internal signal to the physical I/O. The Quartus II software also offers SignalTap II and SignalProbe to further assist you with debugging.

Accessing Internal Signals for Simulation

You can conventionally debug by probing out the internal signals, which enables you to preserve the internal signals during synthesis. You can probe the internal signal by selecting the node or bus and specifying a name, and then adding an output port to the schematic with a similar name. Figure 1–15 shows an example of accessing internal signals for simulation from a schematic diagram.

Figure 1–15. Example of Tapping Out Internal Signal



For timing simulations, the simulation netlist is based on the Compilation post-Synthesis and post-Fitting netlist. Therefore, some of the internal nodes or buses are optimized away during compilation of the netlist. If an internal node is optimized away, the Quartus II software shows a warning in the **Warning** tab of the Messages window similar to the following message:

```
Warning: Compiler packed, optimized or synthesized away node "DataU". Ignored vector
source file node.
```

This internal node is ignored by the Quartus II Simulator.

If you would like to tap out the D and Q ports of registers, turn on **Add D and Q ports of register node to Simulation Output Waveform** from the Assignment Editor. This feature is only available for functional simulations.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The Scripting Reference Manual includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

You can change the Functional, Timing, or Timing using Fast Timing Model simulation modes with the following command:

```
simulation_mode <mode> ↵
```

To initializes the simulation for the current design, use the following command. During initialization, the Simulator builds the simulation netlist and sets the simulation time to zero.

The option `-ignore_vector_file` is set to Off by default, when the source vector file exists for simulation. The Quartus II software ignores the source vector file during simulation if the option `-ignore_vector_file` is set to On. The `-end_time` option is used only when the `-ignore_vector_file` option is set to On.

```
initialize_simulation [-h | -help] [-long_help] [-check_outputs <On | Off>] \
[-end_time <end_time>] [-glitch_filtering <On | Off>] [-ignore_vector_file <On | Off>] \
[-memory_limiter <On | Off>] [-read_settings_files <On | Off>] [-saf_output <target_file>] \
[-sim_mode <functional | timing | timing_using_fast_timing_model >] [-vector_source <vector_source_file>] \
[-write_settings_files <On | Off>] -simulation_results_format <VWF | CVWF> \
-vector_source <specify CVWF here>
```

To force the specified signal or group of signals to the specified value, type the following at a command prompt:

```
force_simulation_value [-h | -help] [-long_help] -node <hpath> <value> ↵
```

To turn on the simulator to simulate the design for a specified time, type the following at a command prompt:

```
run_simulation [-h | -help] [-long_help] [-time <time>] ↵
```

If you do not specify the length of time the simulation runs, it simulates until the simulation is complete.

To create a breakpoint with a specified equation and action, type the following at a command prompt:

```
create_simulation_breakpoint [-h | -help] [-long_help] \
-action [Give Warning | Give Info | Give Error] \
-breakpoint <breakpoint_name> -equation <equation> ↵
```

To deletes a breakpoint with a specified name, type the following at a command prompt:

```
delete_simulation_breakpoint [-h | -help] [-long_help] \
-breakpoint <breakpoint_name> ↵
```

Conclusion

Simulation plays an important role in ensuring the quality of a product. The Quartus II software offers various tools to assist you with simulation and helps reduce debugging time with the introduction of features like Glitch Filtering and Breakpoints.

2. Mentor Graphics ModelSim Support

QII53001-6.0.0

Introduction

An Altera® software subscription includes a license for the ModelSim-Altera software on a PC or UNIX platform. The ModelSim-Altera software can be used to perform functional register transfer level (RTL), post-synthesis, and gate-level timing simulations for either Verilog HDL or VHDL designs that target an Altera FPGA. This chapter provides detailed instructions on how to simulate your design in the ModelSim-Altera version or the Mentor Graphics® ModelSim® software version. This chapter gives you details on the specific libraries that are needed for a functional RTL simulation or a gate-level timing simulation.

This document describes using ModelSim-Altera software version 6.1d and the Mentor Graphics ModelSim software version 6.1d. It also contains references to features available in the Altera Quartus® II software version 6.0. For more information on the current Quartus II software version, refer to the Altera website at **www.altera.com**.

Background

The ModelSim-Altera software version 6.1d is included with your Altera software subscription and can be licensed for the PC, Solaris, HP-UX, or Linux platforms to support either Verilog HDL or VHDL hardware description language (HDL) simulation. The ModelSim-Altera software supports VHDL or Verilog functional RTL, post-synthesis, and gate-level timing simulations for all Altera devices. The ModelSim-Altera simulator has an instance limit of 250 instances for each design that you simulate.

Table 2–1 describes the differences between the Mentor Graphics ModelSim SE/PE and ModelSim-Altera software versions.

Table 2–1. Comparison of ModelSim Software Versions

Product Feature	ModelSim SE	ModelSim PE	ModelSim-Altera
VHDL, Verilog HDL, mixed-HDL support	Optional	Optional	Supports only single-HDL simulation
Complete HDL debugging environment	✓	✓	✓
Industry-standard scripting	✓	✓	✓
Flexible licensing	✓	Optional	✓
Verilog PLI *(1)* support. Interfaces Verilog HDL designs to customer C code and third-party software	✓	✓	✓
VHDL FLI support. Interfaces VHDL designs to customer C code and third-party software	✓		
Standard Delay Format File annotation	✓	✓	✓ *(2)*
Advanced debugging features and language-neutral licensing	✓		
Customizable, user-expandable graphical user interface GUI and integrated simulation performance analyzer	✓		
Integrated code coverage analysis and SWIFT support	✓		
Accelerated VITAL and Verilog HDL primitives (3 times faster), and register transfer level (RTL) acceleration (5 times faster)	✓		
Platform support	PC, UNIX, Linux	PC only	PC, UNIX, Linux

Notes to Table 2–1:

(1) See **www.altera.com/products/software/pld/products/partners/eda-ms.html**.

(2) Standard Delay Format File annotation is supported only for Altera libraries.

Software Compatibility

Table 2–2 shows which ModelSim-Altera software version is compatible with the Quartus II software versions. ModelSim versions provided directly from Mentor Graphics do not correspond to specific Quartus II software versions.

For help on ModelSim-Altera licensing set-up, refer to "Software Licensing & Licensing Set-Up" on page 2–49.

Table 2–2. Compatibility Between Software Versions

ModelSim-Altera Software	Quartus II Software *(1)*
ModelSim-Altera software version 6.1d	Quartus II software version 6.0
ModelSim-Altera software version 6.0e	Quartus II software version 5.1
ModelSim-Altera software version 6.0c	Quartus II software version 5.0
ModelSim-Altera software version 5.8.e ModelSim-Altera software version 5.8	Quartus II software version 4.2

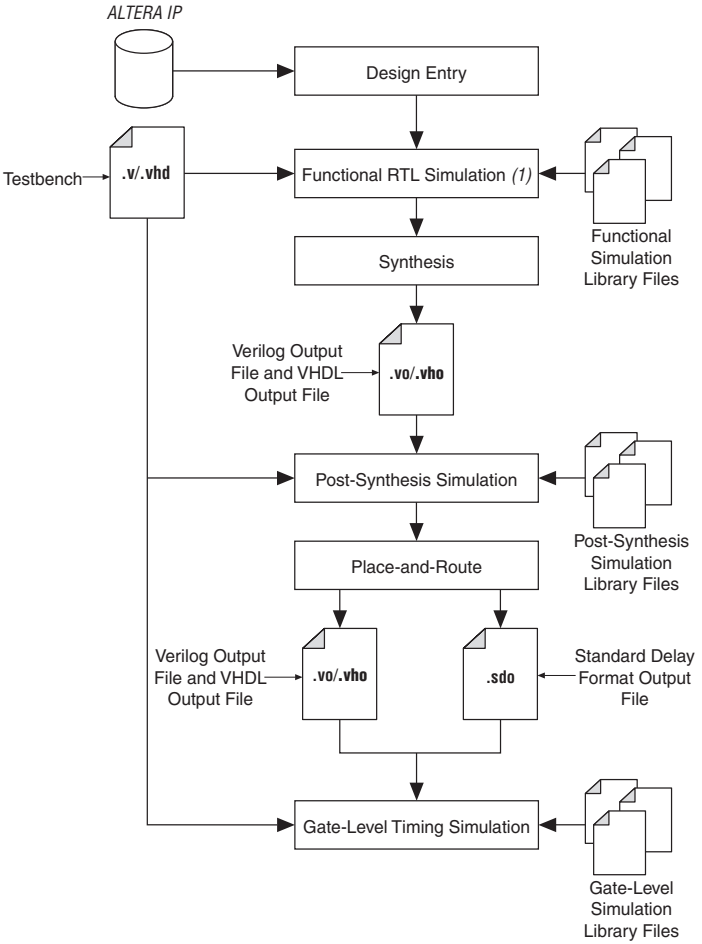
Note to Table 2–2:
(1) Updated ModelSim-Altera precompiled libraries are available for download on Altera's website for each release of the Quartus II service pack.

Altera Design Flow with ModelSim-Altera Software

Figure 2–1 illustrates an Altera design flow using the ModelSim-Altera software or Mentor Graphics ModelSim software version.

- Functional RTL simulations
- Post-synthesis simulations
- Gate-level timing simulations
- Using the NativeLink® feature with ModelSim

Figure 2–1. Altera Design Flow with ModelSim-Altera & Quartus II Software



Note to Figure 2–1:

(1) If you are performing a functional simulation through NativeLink, you must complete analysis and elaboration first.

Functional RTL Simulation

A functional RTL simulation is performed before a gate-level simulation or post-synthesis simulation. Functional RTL simulation verifies the functionality of the design before synthesis and place-and-route. This section provides detailed instructions on how to perform a functional RTL simulation in the ModelSim-Altera software and highlights some of the differences in performing similar steps in the Mentor Graphics ModelSim software versions for Verilog HDL and VHDL designs.

Functional Simulation Libraries

Pre-compiled libraries are available for functional simulation with the ModelSim-Altera software. These libraries include the **lpm** library and the **altera_mf** library. To create these libraries for simulation with the ModelSim SE/PE software, compile the library files described in the following sections.

lpm Simulation Models

To simulate designs containing lpm functions, use the following functional simulation models:

- **220model.v** (for Verilog HDL)
- **220pack.vhd** and **220model.vhd** (for VHDL)

When you are simulating a design that uses VHDL-1987, use the **220model_87.vhd** model file.

Table 2–3 shows the location of these simulation model files and precompiled libraries in the Quartus II software and the ModelSim-Altera software.

Table 2–3. Location of lpm Simulation Models Files & Pre-Compiled Libraries

Software	Location
Quartus II	<*Quartus II installation directory*>**\eda\sim_lib** *(1)*
ModelSim-Altera	<*ModelSim-Altera installation directory*>**\altera\<HDL>\220model** *(2)*, *(3)*

Notes to Table 2–3:
(1) For ModelSim SE/PE, compile the files provided with the Quartus II software.
(2) For ModelSim-Altera, use the precompiled libraries for simulation.
(3) <*HDL*> can be either Verilog HDL or VHDL.

For more information on LPM functions, refer to the Quartus II Help.

Altera Megafunction Simulation Models

To simulate a design that contains Altera megafunctions, use the following simulation models:

- **altera_mf.v** (for Verilog HDL)
- **altera_mf.vhd** and **altera_mf_components.vhd** (for VHDL)

When you are simulating a design that uses VHDL-1987, use **altera_mf_87.vhd.**

Table 2–4 shows the location of these simulation files and precompiled libraries in the Quartus II software and the ModelSim-Altera software.

Table 2–4. Location of Altera Megafunction Simulation Models Files & Precompiled Libraries

Software	Location
Quartus II	<*Quartus II installation directory*>**\eda\sim_lib** *(1)*
ModelSim-Altera	<*ModelSim-Altera installation directory*>**\altera**<***HDL***>**\altera_mf** *(2)*, *(3)*

Notes to Table 2–4:
(1) For ModelSim SE/PE, compile the files provided with the Quartus II software.
(2) For ModelSim-Altera, use the precompiled libraries for simulation.
(3) <*HDL*> can be either verilog or vhdl.

The following Altera megafunctions require device atom libraries to perform a functional simulation in a third-party simulator:

- `altclkbuf`
- `altclkctrl`
- `altdqs`
- `altdq`
- `altddio_in`
- `altddio_out`
- `altddio_bidir`
- `altufm_none`
- `altufm_parallel`
- `altufm_spi`
- `altmemmult`
- `altremote_update`

The device atom library files are located in the following directory:

<*Quartus II installation directory*>**/eda/sim_lib**

Low-Level Primitive Simulation Models

You can simulate a design that contains low-level Altera primitives with the following simulation models:

- **altera_primitives.v** (for Verilog HDL)
- **altera_primitives.vhd** and **altera_primitives_components.vhd** (for VHDL)

Table 2–5 shows the location of these simulation library files and precompiled libraries in the Quartus II software and the ModelSim-Altera software.

Table 2–5. Location of Altera Primitives Model Files & Precompiled Libraries

Software	Location
Quartus II	<*Quartus II installation directory*>\eda\sim_lib *(1)*
ModelSim-Altera	<*ModelSim-Altera installation directory*>\altera\<HDL>\altera *(2)*, *(3)*

Notes to Table 2–5:
(1) For ModelSim SE/PE, compile the files provided with the Quartus II software.
(2) For ModelSim-Altera, use the precompiled libraries for simulation.
(3) <*HDL*> can be either Verilog HDL or VHDL.

Simulating VHDL Designs

Use the following instructions to perform a functional RTL simulation for VHDL designs in the ModelSim software.

The steps in the following section assume you have already created a ModelSim project.

Create Simulation Libraries

Simulation libraries are required to simulate a design that contains an Altera primitive, lpm function, or Altera megafunction. These libraries have already been compiled if you are using the ModelSim-Altera software. However, if you are using the Mentor Graphics ModelSim software version, you must create the simulation libraries and link them to your design correctly.

Create Simulation Libraries Using the ModelSim GUI
Perform the following steps to create simulation libraries:

1. In the ModelSim software, on the File menu, point to New and click **Library**. The **Create a New Library** dialog box appears.
2. Select **a new library and a logical mapping to it**.
3. In the **Library Name** box, type the name of the newly created library.

   For example, the library name for Altera megafunctions should be altera_mf, and the library name for LPM should be lpm.
4. Click **OK**.

Create Simulation Libraries Using the ModelSim Command Prompt
Type the following commands at the ModelSim command prompt:

```
vlib altera_mf ↵
vmap altera_mf altera_mf ↵
vlib lpm ↵
vmap lpm lpm ↵
vlib altera ↵
vmap altera altera ↵
```

Compile Simulation Models into Simulation Libraries

The following steps are not required for the ModelSim-Altera software.

Compile Simulation Models into Simulation Libraries Using the ModelSim GUI
Perform the following steps to compile simulation models into simulation libraries:

1. On the File menu, point to Add to Project and click **Existing File**.
2. Browse to the <*Quartus II installation directory*>**/eda/sim_lib** and add the necessary simulation model files to your project.

The **altera_mf.vhd** model file should be compiled into the **altera_mf** library. The **220pack.vhd** and **220model.vhd** model file should be compiled into the **lpm** library.

3. In the Workspace window, select the simulation model file, and on the View menu, click **Properties**.

4. Choose the correct library from the **Compile to Library** list.
5. Click **OK**.
6. On the Compile menu, click **Compile selected**.

Compile Simulation Models into Simulation Libraries at the ModelSim Command Prompt
Type the following command lines at the ModelSim command prompt:

```
vcom -work altera_mf <Quartus II installation directory>/eda/sim_lib/altera_mf_components.vhd ↵
vcom -work altera_mf <Quartus II installation directory>/eda/sim_lib/altera_mf.vhd ↵
vcom -work lpm <Quartus II installation directory>/eda/sim_lib/220pack.vhd ↵
vcom -work lpm <Quartus II installation directory>/eda/sim_lib/220model.vhd ↵
vcom -work altera <Quartus II installation directory>/eda/sim_lib/altera_primitives_components.vhd ↵
vcom -work altera <Quartus II installation directory>/eda/sim_lib/altera_primitives.vhd ↵
```

Compile Test Bench & Design Files into Work Library

Compile a test bench and design files into a work library by clicking **Compile All** or by clicking the **Compile All** toolbar icon on the Compile menu.

Compile Test Bench & Design Files into Work Library Using the ModelSim Command Prompt
Type the following command at the ModelSim command prompt:

```
vcom -work work <my_test bench.vhd> <my_design_files.vhd>↵
```

Resolve compile-time errors before proceeding to the following section.

Loading the Design

To load a design, perform the following steps:

1. On the Simulate menu, click **Start Simulation**. The **Start Simulation** dialog box appears.
2. Expand the work library in the **Start Simulation** dialog box.
3. Select the top-level design unit (your test bench).
4. In the **Resolution** list, select **ps**.
5. Click **OK**.

Loading the Design Using the ModelSim Command Prompt
Type the following command at the ModelSim command prompt:

```
vsim work.<my_test bench> -t ps ↵
```

Running the Simulation

Perform the following steps to run a simulation:

1. On the View menu, point to Debug Windows and click **Objects**. This command displays all objects in the current scope.
2. On the View menu, point to Debug Windows and click **Wave**.
3. Drag signals to monitor from the Objects window and drop them into the Wave window.
4. At the ModelSim command prompt, type the following:

   ```
   run <time period> ↵
   ```

Running the Simulation Using the ModelSim Command Prompt
Type the following command line at the ModelSim command prompt:

```
add wave /<signal name> ↵
run <time period> ↵
```

Simulating Verilog HDL Designs

The following instructions provide step-by-step instructions to perform functional RTL simulation for Verilog HDL designs in the ModelSim software.

The following steps assume you have already created a ModelSim project.

Create Simulation Libraries

Simulation libraries are needed to properly simulate a design that contains an lpm function or an Altera megafunction. These libraries have already been compiled if you are using the ModelSim-Altera software. However, if you are using the Mentor Graphics ModelSim software version, you must create the simulation libraries and correctly link them to your design.

Create Simulation Libraries Using the ModelSim GUI
Perform the following steps to create simulation libraries:

1. On the File menu, point to New and click **Library**. The **Create a New Library** dialog box appears.
2. Select **a new library and a logical mapping to it**.
3. In the **Library Name** box, type the name of the newly created library.

   For example, the library name for Altera megafunctions should be altera_mf, and the library name for LPM should be lpm.
4. Click **OK**.

Create Simulation Libraries Using the ModelSim Command Prompt
Type the following command lines at the ModelSim command prompt:

```
vlib altera_mf ↵
vmap altera_mf altera_mf ↵
vlib lpm ↵
vmap lpm lpm ↵
vlib altera ↵
vmap altera altera ↵
```

Compile Simulation Models into Simulation Libraries

The following steps are not required for the ModelSim-Altera software.

Compile Simulation Models into Simulation Libraries Using the ModelSim GUI
Perform the following steps to compile simulation models into simulation libraries:

1. On the File menu, point to Add to Project and click **Existing File**.
2. Browse to the <*Quartus II installation directory*>**/eda/sim_lib** and add the necessary simulation model files to your project.

   Compile the **altera_mf.v** into the **altera_mf** library. Compile the **220model.v** into the **lpm** library.
3. Select the simulation model file and on the View menu, click **Properties**.
4. Choose the correct library from the **Compile to Library** list.

5. Click **OK**.

6. On the Compile menu, click **Compile selected**.

Compile Simulation Models into Simulation Libraries Using the ModelSim Command Prompt
Type the following command lines at the ModelSim command prompt:

```
vlog -work altera_mf <Quartus II installation directory>/eda/sim_lib/altera_mf.v ↵
vlog -work lpm <Quartus II installation directory>/eda/sim_lib/220model.v ↵
vlog -work altera <Quartus II installation directory>/eda/sim_lib/altera_primitives.v ↵
```

Compile Test Bench & Design Files into Work Library

Compile a test bench and design files into a work library on the Compile menu by clicking **Compile All** or clicking the **Compile All** toolbar icon on the Compile menu.

Compile Test Bench & Design Files into Work Library Using the ModelSim Command Prompt
Type the following command at the ModelSim command prompt:

```
vlog -work work <my_test bench.v> <my_design_files.v>↵
```

Resolve compile-time errors before proceeding to the following section.

Loading the Design

Perform the following steps to load a design:

1. On the Simulate menu, click **Start Simulation**. The **Start Simulation** dialog box appears.

2. Click the **Libraries** tab.

3. In the **Search Libraries** box, click **Add**.

4. Specify the location to the **lpm** or **altera_mf** simulation libraries.

If you are using the ModelSim-Altera version, refer to Table 2–3 on page 2–5 and Table 2–4 on page 2–6 for the location of the precompiled simulation libraries. If you are using the Mentor Graphics ModelSim software version, browse to the library that was created earlier.

5. In the **Load Design** dialog box, click the **Design** tab and expand the work library.
6. Select the top-level design unit (your test bench).
7. In the **Resolution** list, select **ps**.
8. Click **OK**.

Loading a Design Using the ModelSim Command Prompt
Type the following command at the ModelSim command prompt:

```
vsim -L <location of the altera_mf library> -L <location of the lpm library> work.<my_test bench> -t ps ↵
```

Running the Simulation

Perform the following steps to run a simulation:

1. On the View menu, point to Debug Windows and click **Objects**. This command displays all objects in the current scope.
2. On the View menu, point to Debug Windows and click **Wave**.
3. Drag the signals to monitor from the Objects window and drop them into the Wave window.
4. At the ModelSim command prompt, type the following:

   `run` <*time period*> ↵

Running the Simulation Using the ModelSim Command Prompt
Type the following commands at the ModelSim command prompt:

```
add wave /<signal name> ↵
run <time period> ↵
```

Verilog HDL Functional RTL Simulation with Altera Memory Blocks

Both ModelSim software products support simulating Altera memory megafunctions initialized with Hexadecimal (Intel-Format) File (**.hex**) or RAM initialization files (**.rif**).

Although synthesis is able to read a Memory Initialization File (**.mif**), this memory file is not supported with third-party tools and must be converted to either a Hexadecimal (Intel-Format) File or RAM Initialization File.

Table 2–6 summarizes the different types of memory initialization file formats that are supported with each RTL language.

Table 2–6. Simulation Support for Memory Initialization Files

File	Verilog HDL	VHDL
Hexadecimal (Intel-Format) File	Yes *(1)*	Yes
Memory Initialization File	No	No
RAM Initialization File	Yes *(2)*	No

Notes to Table 2–6:

(1) For memories and library files from the Quartus II software version 5.0 and earlier, you must use a PLI library containing the `convert_hex2ver` function.

(2) Requires the `USE_RIF` macro to be defined, described later in this section.

To simulate your design by converting your Memory Initialization File into either a Hexadecimal (Intel-Format) File or a RAM Initialization File, perform the following steps:

1. Convert a Memory Initialization File to a Hexadecimal (Intel-Format) File or RAM Initialization File in the Quartus II software.

   Converting a Memory Initialization File to a Hexidecimal (Intel-Format) File

   a. Open the Memory Initialization File. On the File menu, click **Save As**. The **Save As** dialog box appears.

   b. In the **Save as type** list, select **Hexadecimal (Intel-Format) File (*.hex)**.

   c. Click **OK**.

   Convert a Memory Initialization File to a RAM Initialization File

   a. Open the Memory Initialization File and on the File menu, click **Export**. The **Export** dialog box appears.

   b. In the **Save as type** list, select **RAM Initialization File (*.rif)**.

   c. Click **OK**.

Alternatively, you can convert a Memory Initialization File to a RAM Initialization File using the **mif2rif.exe** utility located in the <*Quartus II installation*>**/bin** directory.

```
mif2rif <mif_file> <rif_file> ↵
```

2. Modify the HDL file generated by the MegaWizard® Plug-In Manager.

   The Altera memory custom megafunction variation file includes the `lpm_file` parameter, for LPM memories such as `LPM_ROM`, or `init_file` for Altera specific memories such as an `altsyncram`, to point to the initialization file.

   In a text editor, open the custom megafunction variation file and edit the `lpm_file` or `init_file` to point to the Hexadecimal (Intel-Format) File or RAM Initialization File, as shown in the following example:

   ```
   lpm_ram_dp_component.lpm_file = "<path to HEX/RIF>"
   ```

3. Compile the functional library files with compiler directives.

   If you use a Hexadecimal (Intel-Format) File, then no compiler directives are required. If you use a RAM Initialization File, then you must define the **USE_RIF** macro when compiling the model library files. For example, you should enter the following when compiling the `altera_mf` library when RAM Initialization File memory initialization files are used:

   ```
   vlog -work altera_mf altera_mf.v +define+USE_RIF=1
   ```

   For the Quartus II software versions 5.0 and earlier, you must define the `NO_PLI` macro instead of `USE_RIF`. The `NO_PLI` macro is forward compatible with the Quartus II software.

Post-Synthesis Simulation

A post-synthesis simulation verifies the functionality of a design after synthesis has been performed. You can create a post-synthesis netlist in the Quartus II software and use this netlist to perform a post-synthesis simulation in ModelSim. Once the post-synthesis version of the design is verified, the next step is to place-and-route the design in the target device using the Quartus II Fitter.

Generating a Post-Synthesis Simulation Netlist

The following steps describe the process of generating a post-synthesis simulation netlist in the Quartus II software:

1. Perform Analysis and Synthesis. On the Processing menu, point to Start and click **Start Analysis & Synthesis** (you can also perform this after step 2).

2. Turn on the **Generate Netlist for Functional Simulation Only** option by performing the following steps:

    a. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.

    b. In the **Category** list, select **Simulation**. The **Simulation** page is shown.

    c. In the **Tool name** list:

    - If you are using the ModelSim-Altera software, select **ModelSim-Altera**.
    - If you are using the Mentor Graphics ModelSim software, select **ModelSim**.

    d. Under **EDA Netlist Writer options**, in the **Format for output netlist** list, select **VHDL** or **Verilog**. You can also modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.

    e. Click **More Settings**. The **More EDA Tools Simulation Settings** dialog box appears. In the **Existing options settings list**, click **Generate Netlist for Functional Simulation Only** and select **On** from the **Setting** list under **Option**.

    f. Click **OK**.

    g. In the **Settings** dialog box, click **OK**.

3. Run the EDA Netlist Writer. On the Processing menu, point to Start and click **Start EDA Netlist Writer**.

   During the EDA Netlist Writer stage, the Quartus II software produces a Verilog Output File (**.vo**) or VHDL Output File (**.vho**) that can be used for post-synthesis simulations in the ModelSim software. This netlist file is mapped to architecture-specific primitives. No timing information is included at this stage. The resulting netlist is located in the output directory you specified in the **Settings** dialog box, which defaults to the *<project directory>***/simulation/modelsim** directory.

Simulating VHDL Designs

The following instructions help you perform a post-synthesis simulation for a VHDL design in the ModelSim software.

The following steps assume you have already created a ModelSim project.

Create Simulation Libraries

Simulation libraries are required to simulate a design that is mapped to post-synthesis primitives. If you are using the Mentor Graphics ModelSim software version, you must create the simulation libraries and correctly link them to your design.

This process is not required with the ModelSim-Altera version because a set of pre-compiled libraries is installed with the software.

Create Simulation Libraries Using the ModelSim GUI
Perform the following steps to create simulation libraries:

1. On the File menu, click **New Library**. The **Create a New Library** dialog box appears.
2. Select **a new Library and a logical linking to it**.
3. In the **Library Name** box, type the name of the newly created library.
4. Click **OK**.

Create Simulation Libraries Using the ModelSim Command Prompt
Type the following commands to create simulation libraries:

```
vlib <device family name> ↵
vmap <device family name> <device family name> ↵
```

For more information on library names, refer to Table 2–8 on page 2–25.

Compile Simulation Models into Simulation Libraries

This process is not required for the ModelSim-Altera version because a set of pre-compiled libraries is created when you install the software.

Compile Simulation Models into Simulation Libraries Using the ModelSim GUI
Perform the following steps to compile simulation models into simulation libraries:

1. On the File menu, point to Add to Project and click **Existing File**.
2. Browse to the <*Quartus II installation directory*>**/eda/sim_lib** directory and add the necessary gate-level simulation files to your project.
3. Select the simulation model file and on the View menu, click **Properties**.
4. In the **Compile to Library** list, select the correct library.
5. Click **OK**.
6. On the Compile menu, click **Compile selected**.

Compile Simulation Models into Simulation Libraries Using the ModelSim Command Prompt
Type the following command lines at the ModelSim command prompt:

```
vcom -work <device family name> <Quartus II installation directory> \
/eda/sim_lib/<device family name>_atoms.vhd ↵
```

```
vcom -work <device family name> <Quartus II installation directory> \
/eda/sim_lib/<device family name>_components.vhd ↵
```

Compile Test Bench & VHDL Output File into Work Library

To compile test bench and VHDL Output Files into a work library, on the Compile menu, click **Compile All** or click the **Compile All** toolbar icon on the Compile menu.

Compile Test Bench & VHDL Output File into Work Library Using ModelSim Command Prompt
Type the following command line at the ModelSim command prompt:

```
vcom -work work <my_test bench.vhd> <my_vhdl_output_file.vho>↵
```

Resolve any compilation errors before proceeding to the following section.

Loading the Design

Perform the following steps to load a design:

1. On the Simulate menu, click **Simulate**.
2. Click the **Design** tab.
3. In the **Library** list, select the **work** library.
4. In the **Simulate** dialog box, expand the **work** library and select the top-level design unit (your test bench).
5. Click **OK**.

Loading the Design Using the ModelSim Command Prompt
Type the following command line at the ModelSim command prompt:

```
vsim work.<my test bench> -t 1ps↵
```

Set the time scale resolution to 1 ps when simulating Altera FPGA designs.

Running the Simulation

Perform the following steps to run a simulation:

1. On the View menu, point to Debug Windows and click **Objects**. This command displays all objects in the current scope.
2. On the View menu, point to Debug Windows and click **Wave**.
3. Drag the signals to monitor from the Objects window and drop them into the Wave window.
4. At the ModelSim command prompt, type the following:

   ```
   run <time period> ↵
   ```

Running the Simulation Using the ModelSim Command Prompt
Type the following command lines at the ModelSim command prompt:

```
add wave /<signal name> ↵
run <time period> ↵
```

Simulating Verilog HDL Designs

The following sections provide step-by-step instructions on performing post-synthesis simulation for Verilog HDL designs in the ModelSim software.

Create Simulation Libraries

The following steps assume you have already created a ModelSim project.

This process is not required for the ModelSim-Altera version because a set of pre-compiled libraries is created when you install the software. If you are using the Mentor Graphics ModelSim software version, you must create the simulation libraries and correctly link them to your design.

Create Simulation Libraries Using the ModelSim GUI
Perform the following steps to create simulation libraries:

1. In the ModelSim software, on the File menu, point to New and click **Library**. The **Create a New Library** dialog box appears.
2. Select **a new library and a logical mapping to it**.

The name of the libraries should be **altera_mf** (for Altera megafunctions) and **lpm** (for lpm and MegaWizard Plug-in Manager-generated entities).

3. In the **Library Name** box, type the name of the newly created library.
4. Click **OK**.

Create Simulation Libraries Using the ModelSim Command Prompt
Type the following command lines at the ModelSim command prompt:

```
vlib <device family name> ↵
vmap <device family name> <device family name> ↵
```

For more information on library names, refer to Table 2–8.

Compile Simulation Models into Simulation Libraries

This process is not required for the ModelSim-Altera version because a set of pre-compiled libraries is created when you install the software.

Compile Simulation Models into Simulation Libraries Using the ModelSim GUI
Perform the following steps to compile simulation models into simulation libraries:

1. On the File menu, click **Add to Project**, then select **Existing File**.
2. Browse to the <*Quartus II installation directory*>**/eda/sim_lib** directory and add the necessary simulation model files to your project.
3. Select the simulation model file and on the View menu, click **Properties**.
4. Specify the correct library in the **Compile to Library** box.

Compile Simulation Models into Simulation Libraries Using the ModelSim Command Prompt
Type the following command line at the ModelSim command prompt:

```
vlog -work <device family name> <Quartus II installation \
directory> /eda/sim_lib/<device family name>_atoms.v ↵
```

Compile Test Bench & Verilog Output File into Work Library

To compile test bench and Verilog Output Files into a work library, on the Compile menu, click **Compile All** or click the **Compile All** toolbar icon on the Compile menu.

Compile Test Bench & Verilog Output File into Work Library Using the ModelSim Command Prompt
Type the following command line at the ModelSim command prompt:

```
vlog -work work <my_test bench.v> <my_verilog_output_file.vo> ↵
```

Resolve any compilation errors before proceeding to the following section.

Loading the Design

Perform the following steps to load a design:

1. On the Simulate menu, click **Start Simulation**. The **Start Simulation** dialog box appears.
2. Click the **Libraries** tab.
3. In the **Search Libraries** box, click **Add**.
4. Specify the location to the device family simulation libraries.
5. In the **Load Design** dialog box, click the **Design** tab and expand the work library.
6. Select the top-level design unit (your test bench).
7. In the **Resolution** list, select **ps**.
8. Click **OK**.

Loading the Design Using the ModelSim Command Prompt
Type the following command line at the ModelSim command prompt:

`vsim -L` <*gate-level simulation library*> `work.`<*my_test bench*> `-t 1ps` ↵

Set the time scale resolution to 1 ps when simulating Altera FPGA designs.

Running the Simulation

Perform the following steps to run a simulation:

1. In the View menu, point to Debug Windows and click **Objects**. This command displays all objects in the current scope.
2. On the View menu, point to Debug Windows and click **Wave**.
3. Drag the signals to monitor from the Objects window and drop them into the Wave window.
4. At the ModelSim command prompt, type the following command:

   `run` <*time period*> ↵

Running the Simulation Using the ModelSim Command Prompt
Type the following commands at the ModelSim command prompt:

```
add wave /<signal name> ↵
run <time period> ↵
```

Gate-Level Timing Simulation

Gate-level timing simulation is a post place-and-route simulation to verify the operation of the design after the worst-case timing delays have been calculated. This section provides detailed instructions on how to perform gate-level timing simulation in the ModelSim-Altera software and highlights differences in performing similar steps in the Mentor Graphics ModelSim software versions for VHDL and Verilog HDL designs.

Generating a Gate-Level Timing Simulation Netlist

To perform gate-level timing simulation, the ModelSim-Altera software requires information on how the design was placed into device-specific architectural blocks. The Quartus II software provides this information in the form of a Verilog Output File for Verilog HDL designs and a VHDL Output File for VHDL designs. The accompanying timing information is stored in the Standard Delay File (**.sdf**), which annotates the delay for the elements found in the Verilog Output File or VHDL Output File.

The following steps describe the process of generating a gate-level timing simulation netlist in the Quartus II software:

1. Perform a full compilation. On the Processing menu, click **Start Compilation**.
2. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
3. In the **Category** list, select **Simulation**. The **Simulation** page is shown.
4. In the **Tool name** list:
   - If you are using the ModelSim-Altera software, select **ModelSim-Altera**.
   - If you are using the Mentor Graphics ModelSim software, select **ModelSim**.

5. Under **EDA Netlist Writer options**, in the **Format for output netlist** list, select **VHDL** or **Verilog**. You can also modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.

6. Click **OK**.

7. In the **Settings** dialog box, click **OK**.

8. Run the EDA Netlist Writer. On the Processing menu, point to Start and click **Start EDA Netlist Writer**.

   During the EDA Netlist Writer stage, the Quartus II software produces a Verilog Output File (**.vo**), VHDL Output File (**.vho**), and a Standard Delay Output file (**.sdo**) used for gate-level timing simulations in the ModelSim software. This netlist file is mapped to architecture-specific primitives. The timing information for the netlist is included in the Standard Delay Output file. The resulting netlist is located in the output directory you specified in the Settings dialog box, which defaults to the *<project directory>***/simulation/modelsim** directory.

Gate-Level Simulation Libraries

Table 2–7 provides a description of the ModelSim-Altera precompiled device libraries.

Table 2–7. ModelSim-Altera Precompiled Device Libraries (Part 1 of 2)

Library	Description
stratixii	Precompiled library for Stratix® II device designs.
stratixiigx	Precompiled library for Stratix II GX device designs.
stratixiigx_hssi	Precompiled library for Stratix II GX device designs using the Gigabit Transceiver Block (`alt2gxb` megafunction). This precompiled library is required for both functional and timing simulations.
stratix	Precompiled library for Stratix device designs.
stratixgx	Precompiled library for Stratix GX device designs.
stratixgx_gxb	Precompiled library for Stratix GX device designs using the Gigabit Transceiver Block. This precompiled library should be used for post-fit (timing) simulations.
altgxb	Precompiled library for Stratix GX device designs that include the `altgxb` megafunction. This precompiled library should be used for functional simulations.
cycloneii	Precompiled library for Cyclone™ II device designs.
cyclone	Precompiled library for Cyclone device designs.
maxii	Precompiled library for MAX® II device designs.

Table 2–7. ModelSim-Altera Precompiled Device Libraries (Part 2 of 2)	
Library	**Description**
max	Precompiled library for MAX 7000 and MAX 3000 device designs.
apexii	Precompiled library for APEX™ II device designs.
apex20k	Precompiled library for APEX 20K device designs.
apex20ke	Precompiled library for APEX 20KC, APEX 20KE, and Excalibur™ device designs.
mercury	Precompiled library for Mercury™ device designs.
flex10ke	Precompiled library for FLEX® 10KE and ACEX® 1K device designs.
flex6000	Precompiled library for FLEX 6000 device designs.

Table 2–8 shows the location of the timing simulation libraries in the ModelSim-Altera software for Verilog HDL.

Table 2–8. Location of Timing Simulation Libraries for ModelSim-Altera for Verilog HDL	
Library	**Verilog HDL**
stratixii	*<ModelSim-Altera installation directory>*\altera\verilog\stratixii\
stratixiigx	*<ModelSim-Altera installation directory>*\altera\verilog\stratixiigx\
stratixiigx hssi	*<ModelSim-Altera installation directory>*\altera\verilog\stratixiigx_hssi\ *(1)*
stratix	*<ModelSim-Altera installation directory>*\altera\verilog\stratix\
stratixgx	*<ModelSim-Altera installation directory>*\altera\verilog\stratixgx\
stratixgx_gxb	*<ModelSim-Altera installation directory>*\altera\verilog\stratixgx_gxb\
cycloneii	*<ModelSim-Altera installation directory>*\altera\verilog\cycloneii\
cyclone	*<ModelSim-Altera installation directory>*\altera\verilog\cyclone\
maxii	*<ModelSim-Altera installation directory>*\altera\verilog\maxii\
max	*<ModelSim-Altera installation directory>*\altera\verilog\max\
apexii	*<ModelSim-Altera installation directory>*\altera\verilog\apexii\
apex20k	*<ModelSim-Altera installation directory>*\altera\verilog\apex20k\
apex20ke	*<ModelSim-Altera installation directory>*\altera\verilog\apex20ke\
mercury	*<ModelSim-Altera installation directory>*\altera\verilog\mercury\
flex10ke	*<ModelSim-Altera installation directory>*\altera\verilog\flex10ke\
flex6000	*<ModelSim-Altera installation directory>*\altera\verilog\flex6000\

Note to Table 2–8:
(1) The **stratixiigx_hssi** precompiled library is required for functional and timing simulations.

Table 2–9 shows the location of the timing simulation libraries in the ModelSim-Altera software for VHDL.

Table 2–9. Location of Timing Simulation Library Files for ModelSim-Altera for VHDL

Library	VHDL
stratixii	*<ModelSim-Altera installation directory>*\altera\vhdl\stratixii\
stratixiigx	*<ModelSim-Altera installation directory>*\altera\vhdl\stratixiigx\
stratixiigx_hssi	*<ModelSim-Altera installation directory>*\altera\vhdl\stratixiigx_hssi\ *(1)*
stratix	*<ModelSim-Altera installation directory>*\altera\vhdl\stratix\
stratixgx	*<ModelSim-Altera installation directory>*\altera\vhdl\stratixgx\
stratixgx_gxb	*<ModelSim-Altera installation directory>*\altera\vhdl\stratixgx_gxb\
cycloneii	*<ModelSim-Altera installation directory>*\altera\vhdl\cycloneii\
cyclone	*<ModelSim-Altera installation directory>*\altera\vhdl\cyclone\
maxii	*<ModelSim-Altera installation directory>*\altera\vhdl\maxii\
max	*<ModelSim-Altera installation directory>*\altera\vhdl\max\
apexii	*<ModelSim-Altera installation directory>*\altera\vhdl\apexii\
apex20ke	*<ModelSim-Altera installation directory>*\altera\vhdl\apex20ke\
apex20k	*<ModelSim-Altera installation directory>*\altera\vhdl\apex20k\
flex10ke	*<ModelSim-Altera installation directory>*\altera\vhdl\flex10ke\
flex6000	*<ModelSim-Altera installation directory>*\altera\vhdl\flex6000\
mercury	*<ModelSim-Altera installation directory>*\altera\vhdl\mercury\

Note to Table 2–9:
(1) The **stratixiigx_hssi** precompiled library is required for functional and timing simulations.

If you are using the Mentor Graphics ModelSim software version for your timing simulation, libraries are available in the Quartus II software in the *<Quartus II installation directory>***eda****sim_lib**\ directory.
Mentor Graphics ModelSim software users must use the files provided with the Quartus II software.

Simulating VHDL Designs

The following section provides step-by-step instructions for performing gate-level timing simulation for VHDL designs.

The following steps assume you have already created a ModelSim project. For additional information, refer to "Altera Design Flow with ModelSim- Altera Software" on page 2–3.

Create Simulation Libraries

If you are using the Mentor Graphics ModelSim software version, create the gate-level simulation libraries and correctly link them to your design.

This process is not required for the ModelSim-Altera version because a set of pre-compiled libraries is created when you install the software.

Create Simulation Libraries Using the ModelSim GUI
Perform the following steps to create simulation libraries:

1. In the ModelSim software, on the File menu, point to New and click **Library**. The **Create a New Library** dialog box appears.
2. Select **a new library and a logical mapping to it**.

The name of the libraries should be **altera_mf** (for Altera megafunctions) and **lpm** (for lpm and MegaWizard Plug-in Manager-generated entities).

3. In the **Library Name** box, type the name of the newly created library.

The library name must be one of those listed in Table 2–9 on page 2–26.

4. Click **OK**.

Create Simulation Libraries Using the ModelSim Command Prompt
Type the following command lines at the ModelSim command prompt:

```
vlib <device family name> ↵
vmap <device family name> <device family name> ↵
```

For more information on library names, refer to Table 2–8

Compile Simulation Models into Simulation Libraries

This process is not required for the ModelSim-Altera version because a set of pre-compiled libraries is created when you install the software.

Compile Simulation Models into Simulation Libraries Using the ModelSim GUI
Perform the following steps to compile simulation models into simulation libraries:

1. On the File menu, point to Add to Project and click **Existing File**.
2. Browse to the <*Quartus II installation directory*>**/eda/sim_lib** directory, and add the necessary gate-level simulation files to your project.
3. Select the simulation model file, and on the View menu, click **Properties**.
4. In the **Compile to Library** list, select the correct library.
5. Click **OK**.
6. On the Compile menu, click **Compile selected**.

Compile Simulation Models into Simulation Libraries Using the ModelSim Command Prompt
Type the following command lines at the ModelSim command prompt:

```
vcom -work <device family name> <Quartus II installation directory> \
/eda/sim_lib/<device family name>_atoms.vhd ↵
```

```
vcom -work <device family name> <Quartus II installation directory> \
/eda/sim_lib/<device family name>_components.vhd ↵
```

Compile Test Bench & VHDL Output File into Work Library

Compile test bench and VHDL Output Files into a work library on the Compile menu by clicking **Compile All** or by clicking the **Compile All** toolbar icon on the Compile menu.

Compile Test Bench & VHDL Output File into Work Library Using the ModelSim Command Prompt
Type the following command line at the ModelSim command prompt:

```
vcom -work work <my_test bench.vhd> <my_vhdl_output_file.vho> ↵
```

Resolve any compilation errors before proceeding to the following section.

Loading the Design

Perform the following steps to load a design:

1. On the Simulate menu, click **Start Simulation**.
2. Click the **SDF** tab, and click **Add**.
3. In the **Add SDF Entry** dialog box, click **Browse** and select the Standard Delay Format Output File.
4. In the **Apply to Region** dialog box, type in the instance path to which the Standard Delay Format Output File should be applied. For example, if you are using a test bench exported in the Quartus II software from a Vector Waveform File, then the instance path should be set to `/i1`.

   You do not have to choose from the **Delay** list because the Quartus II EDA Netlist Writer generates the Standard Delay Format Output File using the same value for the triplet (minimum, typical, and maximum timing values). The value is derived from either the fast (minimum) timing model or worst case (maximum) timing model, depending on which timing model was used in the last timing analysis. In the standard compilation flow, the Quartus II software writes the Standard Delay Format Output File using timing values from the worst case (maximum) timing model.
5. Click **OK**.
6. Click the **Design** tab. In the **Resolution** list, select **ps**.
7. In the **Library** list, select the **work** library.
8. In the **Start Simulation** dialog box, expand the **work** library.
9. Select the top-level design unit (your test bench).
10. Click **OK**.

Loading a Design Using the ModelSim Command Prompt
Type the following command line at the ModelSim command prompt:

```
vsim -sdftyp <instance path to design>=<path to SDO> work. \
<my_test bench> -t ps ↵
```

Running the Simulation

Perform the following steps to run a simulation:

1. In the View menu, point to Debug Windows and click **Objects**. This command displays all objects in the current scope.
2. On the View menu, point to Debug Windows and click **Wave**.
3. Drag the signals to monitor from the Objects window and drop them into the Wave window.
4. At the ModelSim command prompt, type the following:

   `run` <*time period*> ↵

Running a Simulation Using the ModelSim Command Prompt
Type the following commands at the ModelSim command prompt:

`add wave /`<*signal name*> ↵
`run` <*time period*> ↵

Simulating Verilog HDL Designs

The following sections provide step-by-step instructions on performing gate-level timing simulation for Verilog HDL designs in the ModelSim-Altera software.

Create Simulation Libraries

If you are using the Mentor Graphics ModelSim software version, you must create the simulation libraries and correctly link them to your design.

This process is not required for the ModelSim-Altera version because a set of pre-compiled libraries is created when you install the software.

The following steps assume you have already created a ModelSim project. For additional information, refer to "Altera Design Flow with ModelSim- Altera Software" on page 2–3.

Create Simulation Libraries Using the ModelSim GUI
Perform the following steps to create simulation libraries:

1. In the ModelSim software, on the File menu, point to New and click **Library**. The **Create a New Library** dialog box appears.
2. Select **a new library and a logical mapping to it**.

   The name of the libraries should be **altera_mf** (for Altera megafunctions) and **lpm** (for lpm and MegaWizard Plug-in Manager-generated entities).

3. In the **Library Name** box, type the name of the newly created library.
4. Click **OK**.

Create Simulation Libraries Using the ModelSim Command Prompt
Type the following commands at the ModelSim command prompt:

```
vlib <library name> ↵
vmap <library name> <device family name> ↵
```

For more information on library names, refer to Table 2–8 on page 2–25.

Compile Simulation Models into Simulation Libraries

This process is not required for the ModelSim-Altera version because a set of pre-compiled libraries is created when you install the software.

Compile Simulation Models into Simulation Libraries Using the ModelSim GUI
Perform the following steps to compile simulation models into simulation libraries:

1. On the File menu, point to Add to Project and click **Existing File**.
2. Browse to the <*Quartus II installation directory*>**/eda/sim_lib**, and add the necessary simulation model files to your project.
3. Select the simulation model file, and on the View menu, click **Properties**.
4. In the **Compile to Library** list, select the correct library.

5. Click **OK**.

6. On the Compile menu, click **Compile selected**.

Compile Simulation Models into Simulation Libraries Using the ModelSim Command Prompt
Type the following command at the ModelSim command prompt:

```
vlog -work <device family name> <Quartus II installation directory> /eda/sim_lib/<device family name>_atoms.v ↵
```

Compile Test Bench & Verilog Output File into Work Library

Compile a test bench and Verilog Output File into a work library on the Compile menu by clicking **Compile All** or by clicking the **Compile All** toolbar icon on the Compile menu.

Compile Test Bench & Verilog Output File into Work Libraries Using the ModelSim Command Prompt
Type the following command at the ModelSim command prompt:

```
vlog -work work <my_test bench.v> <my_verilog_output_file.vo> ↵
```

Resolve any compilation errors before proceeding to the following section.

Loading the Design

Perform the following steps to load a design:

1. On the Simulate menu, click **Start Simulation**. The **Start Simulation** dialog box appears.

2. Click the **Libraries** tab.

3. In the **Search Libraries** box, click **Add**.

4. Specify the location to the **lpm** or **altera_mf** simulation libraries.

If you are using the ModelSim-Altera version, refer to Table 2–3 on page 2–5 and Table 2–4 on page 2–6 for the location of the precompiled simulation libraries. If you are using the Mentor Graphics ModelSim software version, browse to the library that you created earlier.

5. In the **Load Design** dialog box, click the **Design** tab and expand the work library.

6. Select the top-level design unit (your test bench).

7. In the **Resolution** list, select **ps**.

8. Click **OK**.

When simulating in Verilog HDL, the Standard Delay Format Output File does not have to be manually specified because in the Quartus II generated Verilog Output File, there is a `$sdf_annotate` task that ModelSim uses to look into the current directory from which VSIM was run and uses to look for the Standard Delay Format Output File. If your Standard Delay Format Output File is not in the same directory from which you ran VSIM, you can either copy the Standard Delay Format Output File into your current directory or comment out the `$sdf_annotate` line in the Verilog Output File and manually specify the Standard Delay Format Output File in the Load Design dialog box.

Loading the Design Using the ModelSim Command Prompt
Type the following command at the ModelSim command prompt:

`vsim -L <`*location of the gate level simulation library*`> -work.<`*my_test bench*`> -t ps` ↵

Running the Simulation

Perform the following steps to run a simulation:

1. On the View menu, point to Debug Windows and click **Objects**. This command displays all objects in the current scope.

2. On the View menu, point to Debug Windows and click **Wave**.

3. Drag the signals to monitor from the Objects window and drop them into the Wave window.

4. At the ModelSim command prompt, type the following:

   `run <`*time period*`>` ↵

Running the Simulation Using the ModelSim Command Prompt
Type the following commands at the ModelSim command prompt:

`add wave /<`*signal name*`>` ↵
`run <`*time period*`>` ↵

Simulating Designs that Include Transceivers

If your design includes a Stratix GX or Stratix II GX transceiver, then you must compile additional library files to perform functional or timing simulations.

Stratix GX Functional Simulation

To perform a functional simulation of your design that instantiates the `altgxb` megafunction which enables the gigabit transceiver block on Stratix GX devices, compile the **stratixgx_mf** model file into the **altgxb** library.

The **stratixiigx_mf** model file references the **lpm** and **sgate** libraries, so you must create these libraries to perform a simulation.

Example of Compiling Library Files for Functional Stratix GX Simulation in Verilog HDL

To compile the libraries necessary for a functional simulation of a Verilog HDL design targeting a Stratix GX device, type the following commands at the ModelSim command prompt:

```
vlib work ↵
vlib lpm ↵
vlib altera_mf ↵
vlib sgate ↵
vlib altgxb ↵
vlog -work lpm 220model.v ↵
vlog -work altera_mf altera_mf.v ↵
vlog -work sgate sgate.v ↵
vlog -work altgxb stratixgx_mf.v ↵
vsim -L lpm -L sgate-L altgxb work.<my design> ↵
```

This example assumes you are using ModelSim PE/SE. If you are using ModelSim-Altera, use the precompiled libraries instead of creating new libraries and compiling the library files by typing the following command:

```
vsim -L lpm -L sgate-L altgxb work.<my design> r ↵
```

Example of Compiling Library Files for Functional Stratix GX Simulation in VHDL

To compile the libraries necessary for functional simulation of a VHDL design targeting a Stratix GX device, type the following commands at the ModelSim command prompt:

```
vcom -work altera_mf altera_mf_components.vhd altera_mf.vhd ↵
vcom -work lpm 220pack.vhd 220model.vhd ↵
vcom -work sgate sgate_pack.vhd sgate.vhd ↵
vcom -work altgxb stratixgx_mf.vhd stratixgx_mf_components.vhd ↵
vsim -L lpm -L altera_mf -L sgate -L altgxb work.<my design> ↵
```

This example assumes you are using ModelSim PE/SE. If you are using ModelSim-Altera, type the following command:

```
vsim -L lpm_ver -L altera_mf_ver -L sgate_ver -L altgxb work.<my design> ↵
```

Stratix GX Post-Fit (Timing) Simulation

Perform a post-fit timing simulation of your design that includes a Stratix GX transceiver by compiling the **stratixgx_atoms** and **stratixgx_hssi_atoms** model files into the **stratixgx** and **stratixgx_gxb** libraries, respectively.

The **stratixgx_hssi_atoms** model file references the **lpm** and **sgate** libraries, so you must create these libraries to perform a simulation.

Example of Compiling Library Files for Timing Stratix GX Simulation in Verilog HDL

To compile the libraries necessary for a timing simulation of a Verilog HDL design targeting a Stratix GX device, type the following commands at the ModelSim command prompt:

```
vlog -work lpm 220model.v ↵
vlog -work altera_mf altera_mf.v ↵
vlog -work sgate sgate.v ↵
vlog -work stratixgx stratixgx_atoms.v ↵
vlog -work stratixgx_gxb stratixgx_hssi_atoms.v ↵
vsim -L lpm -L altera_mf -L sgate -L stratixgx -L stratixgx_gxb \
work.<my design> -t ps +transport_int_delays +transport_path_delays ↵
```

This example assumes you are using ModelSim PE/SE. If you are using ModelSim-Altera, type the following command to simulate:

```
vsim -L lpm_ver -L altera_mf_ver -L sgate_ver -L stratixgx_ver -L \
stratixgx_gxb work.<my design> -t ps +transport_int_delays \
+transport_path_delays ↵
```

Example of Compiling Library Files for Timing Stratix GX Simulation in VHDL

To compile the libraries necessary for a timing simulation of a VHDL design targeting a Stratix GX device, type the following commands at the ModelSim command prompt:

```
vcom -work lpm 220pack.vhd 220model.vhd ↵
vcom -work altera_mf altera_mf_components.vhd altera_mf.vhd ↵
vcom -work sgate sgate_pack.vhd sgate.vhd ↵
vcom -work stratixgx stratixgx_atoms.vhd stratixgx_components.vhd ↵
vcom -work stratixgx_gxb stratixgx_hssi_atoms.vhd \
stratixgx_hssi_components.vhd ↵
vsim -L lpm -L altera_mf -L sgate -L stratixgx -L stratixgx_gxb \
work. <my design> -t ps +transport_int_delays +transport_path_delays ↵
```

This example assumes you are using ModelSim PE/SE. If you are using ModelSim-Altera, type the following command to simulate:

```
vsim -L lpm -L altera_mf -L sgate -L stratixgx -L stratixgx_gxb \
work. <my design> -t ps - +transport_int_delays+transport_path_delays ↵
```

Stratix II GX Functional Simulation

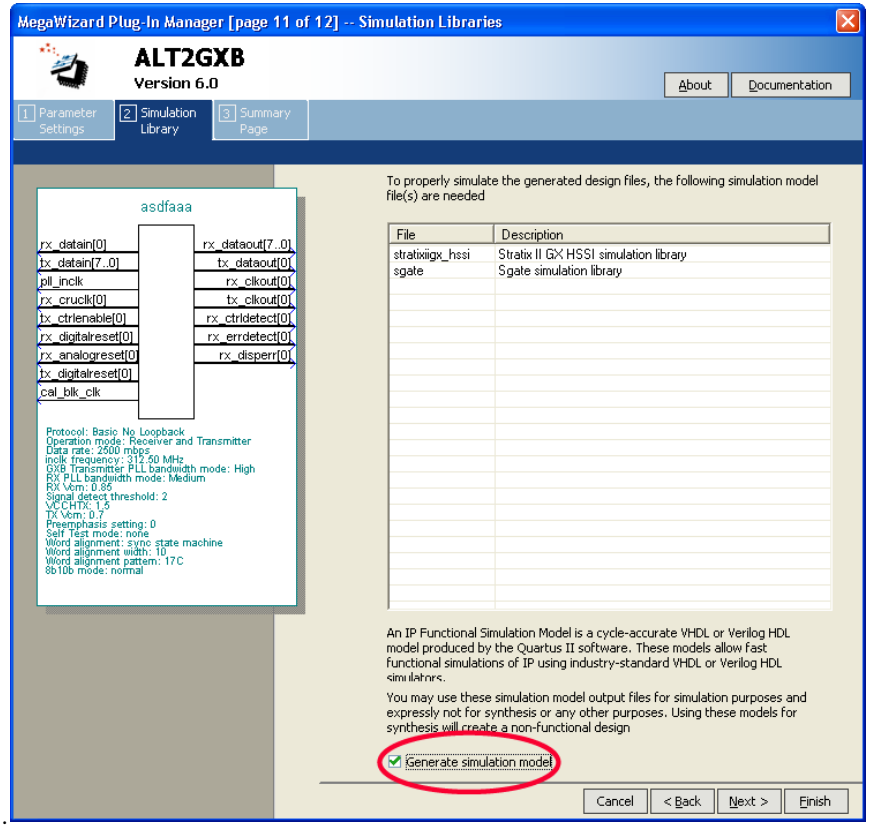
To perform a functional simulation of your design that instantiates the `alt2gxb` megafunction which enables the gigabit transceiver block on Stratix II GX devices, compile the **stratixiigx_hssi** model file into the **stratixiigx_hssi** library.

The **stratixiigx_hssi_atoms** model file references the **lpm** and **sgate** libraries, so you must create these libraries to perform a simulation.

Generate a functional simulation netlist by turning on **Generate Simulation Model** in the Simulation Library tab of the `alt2gxb` MegaWizard Plug-In Manager (Figure 2–2).

The Quartus II-generated `alt2gxb` functional simulation library file references `stratixiigx_hssi` wysiwyg atoms.

Figure 2–2. alt2gxb Megawizard



Example of Compiling Library Files for Functional Stratix II GX Simulation in Verilog HDL

To compile the libraries necessary for a functional simulation of a Verilog HDL design targeting a Stratix II GX device, type the following commands at the ModelSim command prompt:

```
vlog -work lpm 220model.v ↵
vlog -work altera_mf altera_mf.v ↵
vlog -work sgate sgate.v ↵
vlog -work stratixiigx_hssi stratixiigx_hssi_atoms.v ↵
vlog -work work <alt2gxb megafunction variable>.vo ↵
vsim -L lpm -L altera_mf -L sgate -L stratixgx_hssi work.<my design> ↵
```

This example assumes you are using ModelSim PE/SE. If you are using ModelSim-Altera, you do not need to compile any libraries and can type the following command:

```
vsim -L lpm_ver -L altera_mf_ver -L sgate_ver -L stratixgx_hssi_ver \
work.<my design> ↵
```

Instead of creating new libraries, you can map the library names to work using the vmap command.

Example of Compiling Library Files for Functional Stratix II GX Simulation in VHDL

To compile the libraries necessary for a functional simulation of a VHDL design targeting a Stratix II GX device, type the following commands at the ModelSim command prompt:

```
vcom -work lpm 220pack.vhd 220model.vhd ↵
vcom -work altera_mf altera_mf_components.vhd altera_mf.vhd ↵
vcom -work sgate sgate_pack.vhd sgate.vhd ↵
vcom -work stratixiigx_hssi stratixiigx_hssi_components.vhd \
stratixiigx_hssi_atoms.vhd ↵
vcom -work work <simulation_netlist_alt2gxb>.vho ↵
vsim -L lpm -L altera_mf -L sgate -L stratixgx_hssi work.<my design> ↵
```

This example assumes you are using ModelSim PE/SE. If you are using ModelSim-Altera, you do not need to compile any libraries and can type the following command:

```
vsim -L lpm -L altera_mf -L sgate -L stratixgx_hssi work.<my design> r ↵
```

Stratix II GX Post-Fit (Timing) Simulation

To perform a post-fit timing simulation of your design that includes a Stratix II GX transceiver, compile `stratixiigx_atoms` and `stratixiigx_hssi_atoms` into the **stratixiigx** and **stratixiigx_hssi** libraries, respectively.

The **stratixiigx_hssi_atoms** model file references the **lpm** and **sgate** libraries, so you must create these libraries to perform a simulation.

Example of Compiling Library Files for Timing Stratix II GX Simulation in Verilog HDL

To compile the libraries necessary for a timing simulation of a Verilog HDL design targeting a Stratix II GX device, type the following commands at the ModelSim command prompt:

```
vlog -work lpm 220model.v ↵
vlog -work altera_mf altera_mf.v ↵
vlog -work sgate sgate.v ↵
vlog -work stratixiigx  stratixiigx_atoms.v ↵
vlog -work stratixiigx_hssi stratixiigx_hssi_atoms.v ↵
vsim -L lpm -L altera_mf -L sgate -L stratixiigx -L stratixiigx_hssi \
work.<my design> -t ps +transport_int_delays +transport_path_delays ↵
```

This example assumes you are using ModelSim PE/SE. If you are using ModelSim-Altera, you do not need to compile any libraries and can type the following command:

```
vsim -L lpm -L altera_mf -L sgate -L stratixiigx -L stratixiigx_hssi \
work.<my design> -t ps +transport_int_delays +transport_path_delays ↵
```

Example of Compiling Library Files for Timing Stratix II GX Simulation in VHDL

To compile the libraries necessary to timing simulation of a VHDL design targeting a Stratix II GX device, type the following commands at the ModelSim command prompt:

```
vcom -work lpm 220pack.vhd 220model.vhd ↵
vcom -work altera_mf altera_mf_components.vhd altera_mf.vhd ↵
vcom -work sgate sgate_pack.vhd sgate.vhd ↵
vcom -work stratixiigx  stratixiigx_atoms.vhd stratixiigx_components.vhd ↵
vcom -work stratixiigx_hssi stratixiigx_hssi_components.vhd \
stratixiigx_hssi_atoms.vhd ↵
vcom -work work <alt2gxb megafunction variable>.vho ↵
vsim -L lpm -L altera_mf -L sgate -L stratixiigx -L stratixiigx_hssi \
work.<my design> -t ps +transport_int_delays +transport_path_delays ↵
```

This example assumes you are using ModelSim PE/SE. If you are using ModelSim-Altera, you do not need to compile any libraries and can type the following command:

```
vsim -L lpm -L altera_mf -L sgate -L stratixiigx -L stratixiigx_hssi \
work.<my design> -t ps +transport_int_delays +transport_path_delays ↵
```

Transport Delays

By default, the ModelSim software filters out all pulses that are shorter than the propagation delay between primitives. Turning on the transport delay options in the ModelSim software prevents the simulation tool from filtering out these pulses. Use the following options to ensure that all signal pulses are seen in the simulation results.

+transport_path_delays

Use this option when the pulses in your simulation may be shorter than the delay within a gate-level primitive.

+transport_int_delays

Use this option when the pulses in your simulation may be shorter than the interconnect delay between gate-level primitives.

For more information on either of these options, refer to the ModelSim Altera Command Reference installed with the ModelSim software.

The following ModelSim software command describes the command-line syntax to perform a gate-level timing simulation with the device family library:

```
vsim -t 1ps -L stratixii -sdftyp /i1=filtref_vhd.sdo work.filtref_vhd_vec_tst \
+transport_int_delays +transport_path_delays
```

Using the NativeLink Feature with ModelSim

The NativeLink feature in the Quartus II software facilitates the seamless transfer of information between the Quartus II software and EDA tools and allows you to run ModelSim within the Quartus II software.

Setting Up NativeLink

To run ModelSim automatically from the Quartus II software using the NativeLink feature, you must specify the path to your simulation tool by performing the following steps:

1. On the Tools menu, click **Options**. The **Options** dialog box appears.
2. In the **Category** list, select **EDA Tool Options**.
3. Double-click the entry under **Location of executable** beside the name of your EDA Tool.

4. Type or browse to the directory containing the executables of your EDA tool.

For ModelSim-Altera and ModelSim SE/PE, executable files are stored in the **win32aloem** and **win32** directories, respectively.

c:\<*ModelSim-Altera installation path***>\win32aloem**

c:\<*ModelSim installation path***>\win32**

5. Click **OK**.

You can also specify the path to the simulator's executables by using the `set_user_option` TCL command:

```
set_user_option -name EDA_TOOL_PATH_MODELSIM <path to executables>
set_user_option -name EDA_TOOL_PATH_MODELSIM_ALTERA <path to executables>
```

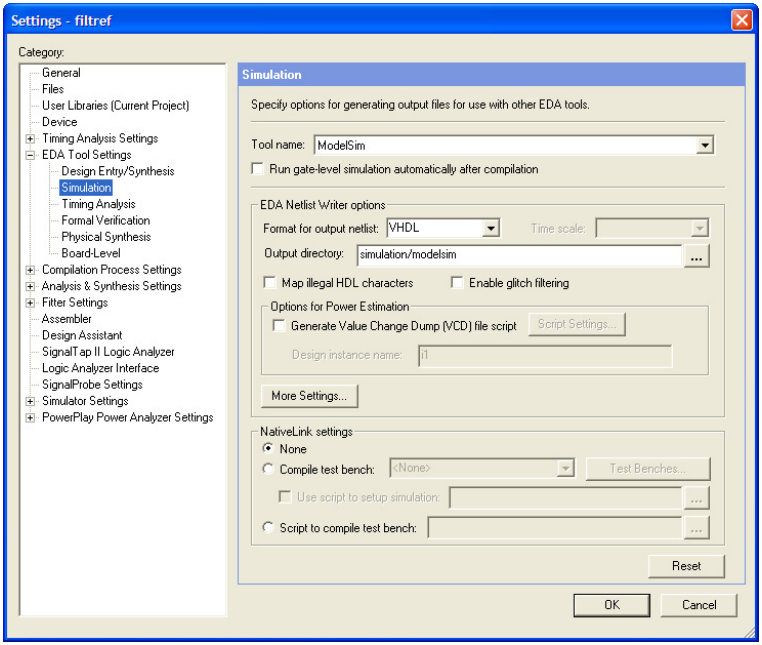
Performing an RTL Simulation Using NativeLink

To run a functional RTL simulation with the ModelSim software in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.

2. In the **Category** list, select **Simulation**. The **Simulation** page is shown (Figure 2–3).

Figure 2–3. Simulation Page in the Settings Dialog Box



3. In the **Tool name** list, select one of the following choices:
   - ModelSim
   - ModelSim-Altera
4. If your design is written entirely in Verilog HDL or in VHDL, then the NativeLink feature automatically chooses the correct language and Altera simulation libraries. If your design is written with mixed languages, then the NativeLink feature uses the default language specified in the **Format for output netlist** list. To change the default

language when there is a mixed language design, under **EDA Netlist Writer options**, in the **Format for output netlist** list, select **VHDL** or **Verilog**. Table 2–10 shows the design languages for output netlists and simulation models.

Table 2–10. NativeLink Design Languages

Design File	Format for Output Netlist	Simulation Models Used
Verilog	Any	Verilog
VHDL	Any	VHDL
Mixed	Verilog	Verilog
Mixed	VHDL	VHDL

For mixed language simulation, choose the same language that was used to generate your megafunctions to ensure correct parameter passing between the megafunctions and the Altera libraries. For example, if your `altsyncram` megafunction was generated in VHDL, choose VHDL as the format for the output netlist.

When creating mixed language designs, it is important to be aware of the following:

- EDA Simulation tools do not allow seamless passing of parameters when a VHDL entity is instantiated in Verilog designs.
- The ModelSim and ModelSim-Altera software do not allow the use of Verilog User Defined Primitives (UDPs) to be instantiated in VHDL designs.

5. If you have test bench files or macro scripts, enter the information under **NativeLink settings**.

   For more information on setting up a test bench with NativeLink, refer to the "Setting Up a Test Bench" on page 2–46.

6. Click **OK.**

7. On the Processing menu, point to Start and click **Start Analysis & Elaboration** to perform an analysis and elaboration. This command collects all your file name information and builds your design hierarchy in preparation for simulation.

8. On the Tools menu, point to **EDA Simulation Tool** and click **Run EDA RTL Simulation** to automatically launch ModelSim, compile all necessary design files, and complete a simulation.

Performing a Gate-Level Simulation Using NativeLink

To run a gate-level timing simulation with the ModelSim software in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.

2. In the **Category** list, select **Simulation**. The **Simulation** page is shown (Figure 2–3 on page 2–43).

3. In the **Tool name** list, select one of the following:

   - ModelSim
   - ModelSim-Altera

4. Under **EDA Netlist Writer options**, in the **Format for output netlist** list, choose **VHDL** or **Verilog**. You can also modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.

5. To perform a gate-level simulation after each full compilation, turn on **Run Gate Level Simulation automatically after compilation**.

6. If you have test bench files or macro scripts, enter the information under **NativeLink settings**.

7. Click **OK**.

8. On the Processing menu, point to Start and click **Start EDA Netlist Writer** to generate a simulation netlist of your design.

9. On the Tools menu, point to EDA Simulation Tool and click **Run EDA Gate Level Simulation** to automatically launch ModelSim, compile all necessary design files, and complete a simulation.

Setting Up a Test Bench

You can use NativeLink to compile your design files and test bench files, and launch an EDA simulation tool to automatically perform a simulation.

To set up NativeLink for simulation, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page is shown.
3. Under **NativeLink settings**, select **None**, **Compile test bench**, or **Script to compile test bench** (Table 2–11).

Table 2–11. NativeLink Settings

Settings	Description
None	Compile simulation models and design files.
Compile test bench	NativeLink compiles simulation models, design files, test bench files, and starts simulation.
Script to compile test bench	NativeLink compiles the simulation models and design files. The script you provide is sourced after design files compile. Use this option when you want to create your own script to compile your test bench and perform simulation.

4. If you select **Compile test bench**, select your test bench setup from the **Compile test bench** list. You can use different test bench setups to specify different test scenarios. If there are no test bench setups entered, create a test bench setup by performing the following steps:
    a. Click **Test Benches**. The **Test Benches** dialog box appears.
    b. Click **New**. The **New Test Bench Settings** dialog box appears.
    c. In the **Test Bench name** box, type in the test bench setup name that identifies the different test bench setups.
    d. In the **Test bench entity** box, type in the top-level test bench entity name. For example, for a Quartus II generated VHDL test bench, type in <*Vector Waveform File name*>`_vhd_vec_tst`.
    e. In the **Instance** box, type in the full instance path to the top level of your FPGA design. For example, for a Quartus II generated VHDL test bench, type in `i1`.

f. In the **Run for** box, specify how long you want your simulation to run.

g. Under **Test bench files**, browse and add all your test bench files in the **File name** box. Use the **Up** and **Down** button to reorder your files. The script used by NativeLink compiles the files in order from top to bottom.

h. Click **OK**.

i. In the **Test Benches** dialog box, click **OK**.

5. Under **NativeLink settings**, you can turn on **Use script to setup simulation** and browse to your script. Your script is executed to setup and run simulation after loading the design using the `vsim` command.

6. If you choose **Script to compile test bench**, browse to your script and click **OK**.

Creating a Test Bench

In the Quartus II software you can create a Verilog HDL or VHDL test bench from a Vector Waveform File. The generated test bench includes the behavior of the input stimulus and applies it to your instantiated top-level FPGA design.

1. On the File menu, click **Open**. The **Open** dialog box appears.

2. Click the **Files of type** arrow and select **Waveform/Vector Files**. Select your Vector Waveform File.

3. Click **Open**.

4. On the File menu, click **Export**. The **Export** dialog box appears.

5. Click the **Save as type** arrow and select **VHDL Test Bench File (*.vht)** or **Verilog Test Bench File (*.vt)**.

6. You can turn on **Add self-checking code to file** to check your simulation results against your Vector Waveform File.

7. Click **Export**. Your VHDL or Verilog test bench file is generated in your project directory.

Scripting Support

You can run procedures and create settings described in this chapter in a Tcl script. You can also run some procedures at the command-line prompt.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

For more information about command line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

For detailed information about scripting command options, refer to the **Qhelp** command line and Tcl API help browser.

Type this command to start the Qhelp help browser:

```
quartus_sh --qhelp
```

Generating a Post-Synthesis Simulation Netlist for ModelSim

You can use the Quartus II software to generate a post-synthesis simulation netlist with Tcl commands or with a command at the command-line prompt. The following example assumes that you are selecting ModelSim (Verilog HDL output from Quartus II software).

Tcl Commands

Use the following Tcl commands to set the output format to Verilog HDL, the simulation tool to ModelSim for Verilog HDL, and to generate a functional netlist.

```
set_global_assignment-name EDA_SIMULATION_TOOL "Modelsim (Verilog)"
set_global_assignment-name EDA_GENERATE_FUNCTIONAL_NETLIST ON
```

Command Prompt

Use the following command to generate a simulation output file for the ModelSim simulator. Specify VHDL or Verilog HDL for the format:

```
quartus_eda <project name> --simulation=on --format=<format> --tool=Modelsim \
--functional ↵
```

Generating a Gate-Level Timing Simulation Netlist for ModelSim

You can use the Quartus II software to generate a gate-level timing simulation netlist with Tcl commands or with a command at the command prompt.

Tcl Commands

Use one of the following Tcl commands:

```
set_global_assignment -name EDA_SIMULATION_TOOL "ModelSim-Altera (Verilog)"
set_global_assignment -name EDA_SIMULATION_TOOL "ModelSim-Altera (VHDL)"
set_global_assignment -name EDA_SIMULATION_TOOL "ModelSim (Verilog)"
set_global_assignment -name EDA_SIMULATION_TOOL "ModelSim (VHDL)"
```

Command Line

Generate a simulation output file for the ModelSim simulator by specifying VHDL or Verilog HDL for the format by typing the following:

```
quartus_eda <project name> --simulation=on --format=<format> --tool=Modelsim ↵
```

Software Licensing & Licensing Set-Up

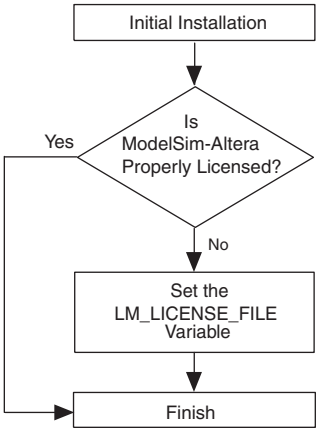
License the ModelSim-Altera software with a parallel port software guard (T-guard), USB guard, FIXEDPC license, or a network FLOATNET or FLOATPC license. Each Altera software subscription includes a license for either VHDL or Verilog HDL. Network licenses with multiple users may have their licenses split between VHDL and Verilog HDL in any ratio.

The USB software guard is not supported by versions earlier than Mentor Graphics ModelSim software 5.8d.

Obtain a license for the ModelSim-Altera software from the Altera website at **www.altera.com**. Get licensing information for the Mentor Graphics ModelSim software directly from Mentor Graphics. Refer to Figure 2–4 on page 2–50 for the set-up process.

For ModelSim-Altera versions prior to 5.5b, use the **PCLS** utility, included with the software, to set up the license.

Figure 2–4. ModelSim-Altera Licensing Set Up Process



LM_LICENSE_FILE Variable

Altera recommends setting the `LM_LICENSE_FILE` environment variable to the location of the license file.

Conclusion

Using the ModelSim-Altera simulation software within the Altera FPGA design flow enables Altera software users to easily and accurately perform functional RTL simulations, post-synthesis simulations, and gate-level simulations on their designs. Proper verification of designs at the functional, post-synthesis, and post place-and-route stages using the ModelSim-Altera software helps ensure design functionality and success and, ultimately, a quick time-to-market.

3. Synopsys VCS Support

QII53002-6.0.0

Introduction

This chapter is an overview on using the Synopsys VCS software to simulate designs that target Altera® FPGAs. It provides a step-by-step explanation of how to perform functional register transfer level (RTL) simulations, post-synthesis simulations, and gate-level timing simulations using the VCS software.

Software Requirements

To simulate your design using VCS, you must first set up the Altera libraries. These libraries are installed with the Quartus II software.

Table 3–1 shows the compatibility between versions of the Quartus II software and the Synopsys VCS software.

Table 3–1. Supported Quartus II & VCS Software Version Compatibility

Synopsys	Altera
VCS software version 2005.06-SP1	Quartus II software version 6.0
VCS software version 7.2	Quartus II software version 5.1
VCS software version 7.2	Quartus II software version 5.0
VCS software version 7.1.1	Quartus II software version 4.2

For more information on installing the software and the directories created during the Quartus II software installation, refer to the *Quartus II Installation & Licensing for PCs* or the *Quartus II Installation & Licensing for UNIX and Linux Workstation* manuals.

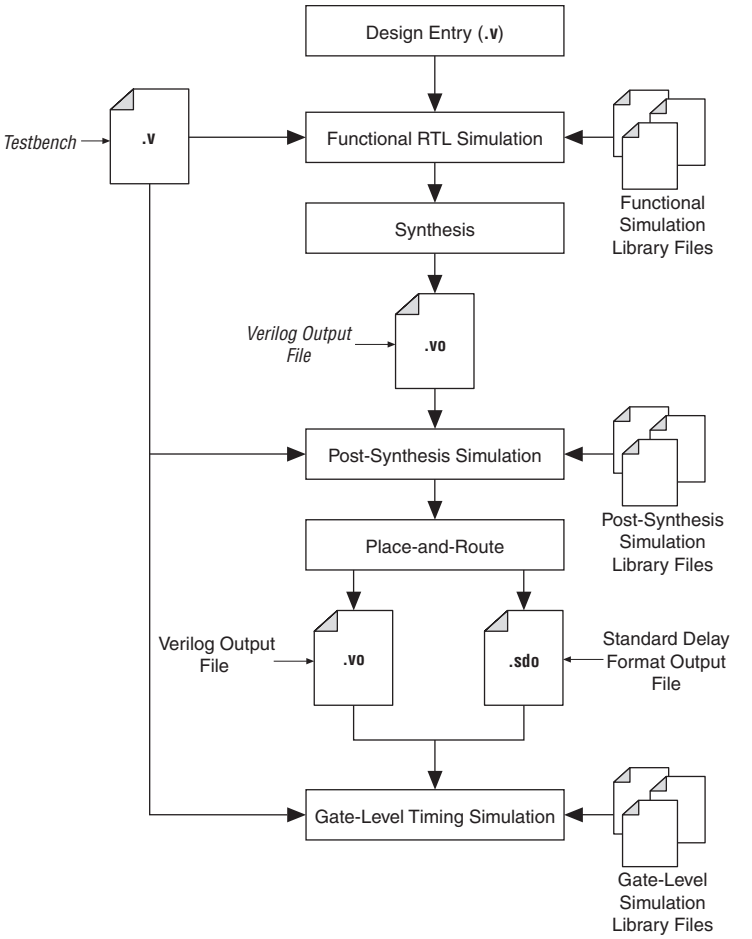
Using VCS in the Quartus II Design Flow

You can perform the following types of simulations using VCS:

- Functional RTL
- Post-synthesis
- Gate-level timing

Figure 3–1 shows the VCS and Quartus II software design flow.

Figure 3–1. Altera Design Flow with the VCS & Quartus II Software



Functional Simulations

Functional RTL simulations verify the functionality of the design before synthesis, placement, and routing. These simulations are independent of any Altera FPGA architecture implementation. Once the HDL designs are verified to be functionally correct, the next step is to synthesize the design and use the Quartus II software to place and route the design in an Altera device.

To functionally simulate an Altera FPGA design in the VCS software that uses Altera intellectual property (IP) megafunctions, or library of parameterized modules (LPM) functions, you must include certain libraries during the compilation. Table 3–2 summarizes the Verilog HDL library files that are required to compile LPM functions and Altera megafunctions.

Table 3–2. Altera Verilog HDL Functional/Behavioral Simulation Library Files

Library Name	Verilog HDL Libraries
LPM	**220model.v**
`altera_mf`	**altera_mf.v**
`altgxb`	**stratixgx_mf.v** *(1)*
`alt2gxb`	**stratixiigx_hssi_atoms.v** *(1)*
`sgate`	**sgate.v**
`altera`	**altera_primitives.v**

Notes to Table 3–2:

(1) The **stratix_mf.v** and **stratixiigx_hssi_atoms.v** library files require the LPM and SGATE libraries.

The library files in Table 3–2 are installed with the Quartus II software. These files are found in the <*path to Quartus II installation*>**\eda\sim_lib** directory.

The following is a VCS command for performing a functional RTL simulation with one of the libraries in Table 3–2:

`vcs -R` <*test bench*>`.v` <*design name*>`.v -v` <*library file*>`.v` ↵

Megafunctions Requiring Atom Libraries

The following Altera megafunctions require gate-level libraries to perform a functional simulation in a third-party simulator:

- `altclkbuf`
- `altclkctrl`
- `altdq`
- `altdqs`
- `altddio_in`
- `altddio_out`
- `altddio_bidir`
- `altufm_none`
- `altufm_parallel`
- `altufm_spi`
- `altmemmult`
- `altremote_update`

The gate-level library files are located in <*path to Quartus II installation*>**eda/sim_lib** directory (Table 3–3).

Functional RTL Simulation with Altera Memory Blocks

The VCS software supports functional simulation of complex Altera memory blocks such as `lpm_ram_dp` and `altsyncram`. You can create these memory blocks with the Quartus II MegaWizard® Plug-In Manager, which can be initialized with power-up data via a Hexadecimal (Intel-Format) File (**.hex**) or Memory Initialization File (**.mif**). The `lpm_file` parameter included in the file generated by the MegaWizard Plug-In Manager points to the path of the Hexadecimal (Intel-Format) File or Memory Initialization File that is used to initialize the memory block. You can create a Hexadecimal (Intel-Format) File or Memory Initialization File with the Quartus II software.

Compiling Functional Library Files with Compiler Directives

If you use a Hexadecimal (Intel-Format) File, then no compiler directives are required. If you use a RAM Initialization File, then the `USE_RIF` macro must be defined to compile the model library files. For example, enter the following when compiling the `altera_mf` library using RIF memory initialization files:

```
vcs -R -v <path to Quartus installation> /
\eda\sim_lib\altera_mf.v <test bench file> /
<design file (top-level)> +define+USE_RIF=1
```

For the Quartus II software versions 5.0 and earlier, the `NO_PLI` macro needs to be defined instead of `USE_RIF`. The `NO_PLI` macro is forward compatible with the Quartus II software.

Post-Synthesis Simulation

A post-synthesis simulation verifies the functionality of a design after synthesis has been performed. You can create a post-synthesis netlist in the Quartus II software and use this netlist to perform a post-synthesis simulation in the VCS software. Once the post-synthesis version of the design has been verified, the next step is to place-and-route the design in the target architecture using the Quartus II software.

Generating a Post-Synthesis Simulation Netlist

The following steps describe the process of generating a post-synthesis simulation netlist in the Quartus II software:

1. Perform Analysis and Synthesis. On the Processing menu, point to Start and click **Start Analysis & Synthesis**.

2. Turn on the **Generate Netlist for Functional Simulation Only** option by performing the following steps:

    a. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.

    b. In the **Category** list, select **Simulation**. The **Simulation** page is shown.

    c. In the **Tool name** list, select **VCS**.

    d. You can modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.

    e. Click **More Settings**. The **More EDA Tools Simulation Settings** dialog box appears. In the **Existing options settings list**, click **Generate Netlist for Functional Simulation Only** and select **On** from the **Setting** list under **Option**.

    f. Click **OK**.

    g. In the **Settings** dialog box, click **OK**.

3. Run the EDA Netlist Writer. On the Processing menu, point to Start and click **Start EDA Netlist Writer**.

During the EDA Netlist Writer stage, the Quartus II software produces a Verilog Output File (**.vo**) that can be used for the post-synthesis simulations in the VCS software. This netlist file is mapped to architecture-specific primitives. No timing information is included at this stage.

The resulting netlist is located in the output directory you specified in the **Settings** dialog box, which defaults to the *<project directory>* **/simulation/vcs** directory. This netlist, along with the device family library listed in Table 3–3, can be used to perform a post-synthesis simulation in the VCS software.

Table 3–3. Altera Gate-Level Simulation Library Files

Library Files	Description
stratixii_atoms.v	Atom libraries for Stratix® II designs
stratixiigx_atoms.v **stratixiigx_hssi_atoms.v**	Atom libraries for Stratix II GX designs
stratix_atoms.v	Atom libraries for Stratix designs
stratixgx_atoms.v **stratixgx_hssi_atoms.v**	Atom libraries for Stratix GX designs
hardcopyii_atoms.v	Atom libraries for HardCopy® II designs
hcstratix_atoms.v	Atom libraries for HardCopy Stratix designs
cycloneii_atoms.v	Atom libraries for Cyclone II designs
cyclone_atoms.v	Atom libraries for Cyclone™ designs
apexii_atoms.v	Atom libraries for APEX II designs
apex20ke_atoms.v	Atom libraries for APEX 20KE, APEX 20KC, and Excalibur™ designs
apex20k_atoms.v	Atom libraries for APEX™ 20K designs
flex10ke_atoms.v	Atom libraries for FLEX® 10KE and ACEX® 1K designs
flex6000_atoms.v	Atom libraries for FLEX 6000 designs
maxii_atoms.v	Atom libraries for MAX® II designs
max_atoms.v	Atom libraries for MAX 3000 and MAX 7000 designs
mercury_atoms.v	Atom libraries for Mercury™ designs

The following VCS software commands describe the command-line syntax used to perform a post-synthesis simulation with the appropriate device family library listed in Table 3–3:

```
vcs -R <test bench> <post synthesis netlist> -v <altera device family library> ↵
```

Gate-Level Timing Simulation

A gate-level timing simulation verifies the functionality of the design after placement and routing. You can create a post-fit netlist in the Quartus II software and use this netlist to perform a gate-level timing simulation in VCS software.

Generating a Gate-Level Timing Simulation Netlist in the Quartus II Software

Generating a gate-level timing simulation netlist in the Quartus II software by performing the following steps:

Generating a Gate-Level Timing Simulation Netlist

To perform gate-level timing simulation, the VCS software requires information on how the design was placed into device-specific architectural blocks. The Quartus II software provides this information in the form of a Verilog Output File for Verilog HDL designs. The accompanying timing information is stored in the Standard Delay File (**.sdf**), which annotates the delay for the elements found in the Verilog Output File.

The following steps describe the process of generating a gate-level timing simulation netlist in the Quartus II software:

1. Perform a full compilation. On the Processing menu, click **Start Compilation**.
2. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
3. In the **Category** list, select **Simulation**. The **Simulation** page is shown.
4. In the **Tool name** list, select **VCS**.
5. You can modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.
6. Click **OK**.
7. In the **Settings** dialog box, click **OK**.
8. Run the EDA Netlist Writer. On the Processing menu, point to Start and click **Start EDA Netlist Writer**.

During the EDA Netlist Writer stage, the Quartus II software produces a Verilog Output File (**.vo**) that can be used for post-synthesis simulations in the VCS software. This netlist file is mapped to architecture-specific primitives. No timing information is included at this stage. The resulting netlist is located in the output directory you specified in the Settings dialog box, which defaults to the <*project directory*>**/simulation/vcs** directory.

Common VCS Software Compiler Options

The VCS software has options that help you simulate your design. Table 3–4 lists some of the options that are available.

Table 3–4. VCS Software Compiler Options

Library	Description
`-R`	Runs the executable file immediately.
`-RI`	Once the compile has completed, instructs the VCS software to automatically launch VirSim.
`-v` <*library filename*>	Specifies a Verilog HDL library file (i.e., **220model.v** or **altera_mf.v**). The VCS software looks in this file for module definitions that are found in the source code. Only the relevant library files are compiled based on the modules found.
`-y` <*library directory*>	Specifies a Verilog HDL library directory. The VCS software looks for library files in this folder that contain module definitions that are instantiated in the source code.
`+compsdf`	Indicates that the VCS software compiler includes the back-annotated SDF file in the compilation.
`+cli`	The VCS software enters Command-Line Interface (CLI) mode upon successful compilation completion.
`+race`	Specifies that the VCS software generate a report that indicates all of the race conditions in the design. Default report name is **race.out**.
`-P`	Compiles user-defined Programming Language Interface (PLI) table files.
`-q`	Indicates the VCS software runs in quiet mode. All messages are suppressed.

For more information on any VCS software option, refer to the *VCS User Guide*.

Using VirSim

VirSim is the graphical debugging system for the VCS software. This tool is included with the VCS software and can be run by using the `-RI` compile-time compiler option when compiling a design. The following VCS software command describes the command-line syntax for compiling and loading a timing simulation in VirSim:

```
vcs -RI <test bench>.v <design name>.vo -v <path to Quartus II installation> \
\eda\sim_lib\<device family>_atoms.v +compsdf ↵
```

For more information on using VirSim, refer to the *VirSim User Manual* included in the VCS software installation.

Debugging Support Command-Line Interface

The VCS software has an interactive non-graphical debugging capability that is very similar to other UNIX debuggers such as the GNU debugger (GDB). The VCS software CLI can be used to halt simulations at user-defined break points, force registers with values, and display values of registers.

Enable the non-graphical capability by using the `+cli` run-time option. Use the VCS software CLI to debug your Altera FPGA design by typing the following command:

```
vcs -R <test bench>.v <design name>.vo
    -v <path to Quartus II installation> \
    \eda\sim_lib\<device family>_atoms.v +compsdf +cli ↵
```

The `+cli` command takes an optional number argument that specifies the level of debugging capability. As the optional debugging capability is increased, the overhead incurred by the simulation is increased, resulting in an increase in simulation times.

For more information on the `+cli` options, refer to the *VCS User Guide* included in the VCS software installation.

Simulating Designs that Include Transceivers

If your design includes a Stratix GX or Stratix II GX transceiver, then you must compile additional library files to perform functional or timing simulations.

Stratix GX Functional Simulation

To perform a functional simulation of your design that instantiates the `altgxb` megafunction, enabling the gigabit transceiver block (GXB) on Stratix GX devices, compile the **stratixgx_mf** model file into the **altgxb** library.

The **stratixiigx_mf** model file references the **lpm** and **sgate** libraries, so you must create these libraries to perform a simulation.

Example of Compiling Library Files for Functional Stratix GX Simulation in Verilog HDL

To compile the libraries necessary for functional simulation of a Verilog HDL design targeting a Stratix GX device, type the following commands at the VCS command prompt:

```
vcs -R <test bench>.v <design files>.v -v stratixgx_mf.v -v \
sgate.v -v 220model.v -v altera_mf.v ↵
```

Instead of creating new libraries, you can map the library names to work with the `vmap` command.

Stratix GX Post-Fit (Timing) Simulation

Perform a post-fit timing simulation of your design that includes a Stratix GX transceiver by compiling the **stratixgx_atoms** and **stratixgx_hssi_atoms** model files into the **stratixgx** and **stratixgx_gxb** libraries, respectively.

The **stratixgx_hssi_atoms** model file references the **lpm** and **sgate** libraries, so you must create these libraries to perform a simulation.

Example of Compiling Library Files for Timing Stratix GX Simulation in Verilog HDL

To compile the libraries necessary for timing simulation of a Verilog HDL design targeting a Stratix GX device, type the following commands at the VCS command prompt:

```
vcs -R <testbench>.v <gate-level netlist>.vo -v stratixgx_atoms.v -v \
stratixgx_hssi_atoms.v -v sgate.v -v 220model.v -v altera_mf.v \
+transport_int_delays +pulse_int_e/0 +pulse_int_r/0 \
+transport_path_delays +pulse_e/0 +pulse_r/0 ↵
```

Stratix II GX Functional Simulation

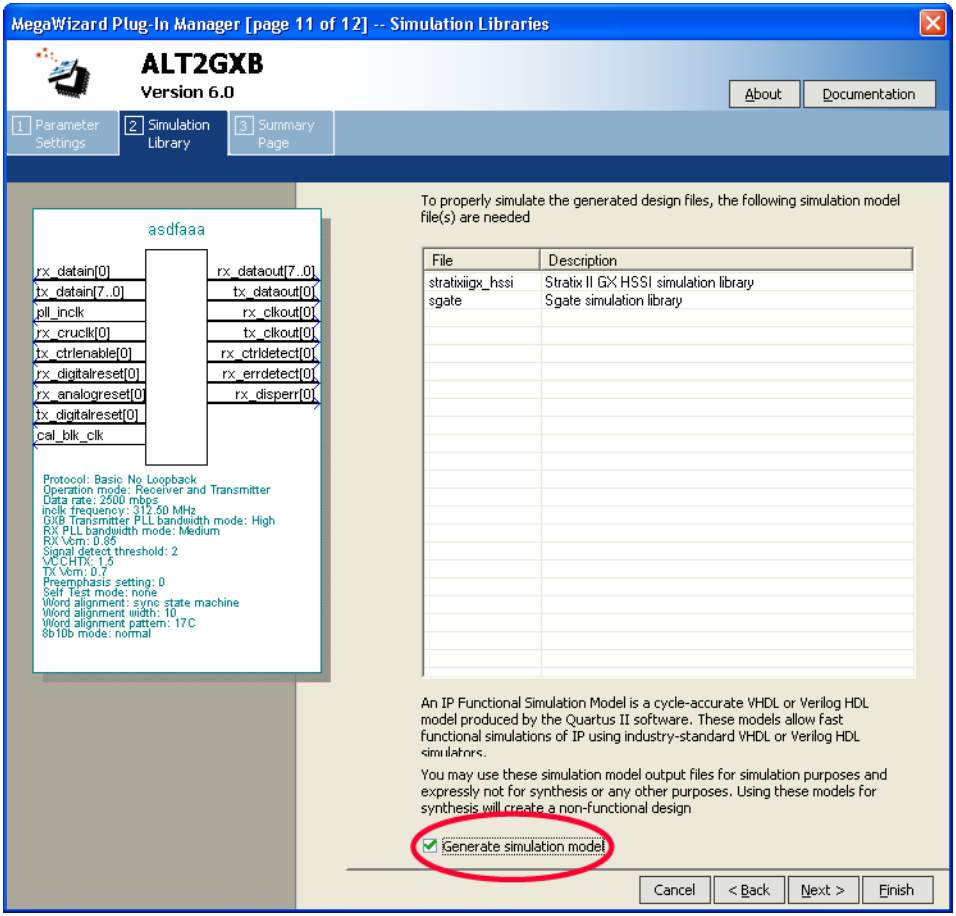
To perform a functional simulation of your design that instantiates the `alt2gxb` megafunction, enabling the gigabit transceiver block (GXB) on Stratix II GX devices, compile the **stratixiigx_hssi** model file into the **stratixiigx_hssi** library.

The **stratixiigx_hssi_atoms** model file references the **lpm** and **sgate** libraries, so you must create these libraries to perform a simulation.

Generate a functional simulation netlist by turning on **Generate Simulation Model in the Simulation Library** in the alt2gxb MegaWizard Plug-In Manager (Figure 3–2).

The Quartus II-generated `alt2gxb` functional simulation library file references `stratixiigx_hssi` wysiwyg atoms.

Figure 3–2. alt2gxb Megawizard



Example of Compiling Library Files for Functional Stratix II GX Simulation in Verilog HDL

To compile the libraries necessary for functional simulation of a Verilog HDL design targeting a Stratix II GX device, type the following commands at the VCS command prompt:

```
vcs -R <testbench>.v <alt2gxb simulation netlist>.vo -v stratixgx_hssi_atoms.v -v \
sgate.v -v 220model.v -v altera_mf.v↵
```

Instead of creating new libraries, you can map the library names to work with the vmap command.

Stratix II GX Post-Fit (Timing) Simulation

To perform a post-fit timing simulation of your design that includes a Stratix II GX transceiver, compile `stratixiigx_atoms` and `stratixiigx_hssi_atoms` into the **stratixiigx** and **stratixiigx_hssi** libraries, respectively.

The **stratixiigx_hssi_atoms** model file references the **lpm** and **sgate** libraries, so you must create these libraries to perform a simulation.

Example of Compiling Library Files for Timing Stratix II GX Simulation in Verilog HDL

To compile the libraries necessary for timing simulation of a Verilog HDL design targeting a Stratix II GX device, type the following commands at the VCS command prompt:

```
vcs -R <testbench>.v <gate-level netlist>.vo -v stratixiigx_atoms.v -v \
stratixiigx_hssi_atoms.v -v sgate.v -v 220model.v -v altera_mf.v \
+transport_int_delays +pulse_int_e/0 +pulse_int_r/0 \
+transport_path_delays +pulse_e/0 +pulse_r/0 ↵
```

Using PLI Routines with the VCS Software

The VCS software can interface your custom-defined C code with Verilog HDL source code. This interface is known as PLI. This interface is extremely useful because it allows advanced users to define their own system tasks that currently may not exist in the Verilog HDL.

Preparing & Linking C Programs to Verilog HDL Code

When compiling the source code, the C code must include a reference to the **vcsuser.h** file. This file defines PLI constants, data structures, and routines that are necessary for the PLI interface. This file is included with the VCS software installation and can be found in the **$VCS_HOME\lib** directory.

Once the C code is complete, you must create an object file (**.o**). Create the object file with the following command:

```
gcc -c my_custom_function.c ↵
```

Next, you must create a PLI table file (**.tab**). This file maps the C program task to the matching task `$task` in the Verilog HDL source code. You can create this file using a standard text editor. The following is an example of an entry in the PLI file:

```
$my_custom_function call=my_custom_function acc+=rw* ↵
```

The Verilog HDL code can now include a reference to the user-defined task. To compile an Altera FPGA design that includes a reference to a user-defined system task, type the following at the command-line prompt:

```
vcs -R <test bench>.v <design name>.v -v <Altera library file>.v -P <my_tabfile.tab> \
<my_custom_function.o> ↵
```

Transport Delays

By default, the VCS software filters out all pulses that are shorter than the propagation delay between primitives. Turning on the transport delay options in the VCS software prevents the simulation tool from filtering out these pulses. Use the following options to ensure that all signal pulses are seen in the simulation results.

+transport_path_delays

Use this option when the pulses in your simulation may be shorter than the delay within a gate-level primitive. For this option to work you must also include the `+pulse_e/number` and `+pulse_r/number` options.

+transport_int_delays

Use this option when the pulses in your simulation may be shorter than the interconnect delay between gate-level primitives. For this option to work you must also include the `+pulse_int_e/number` and `+pulse_int_r/number` options.

For more information on either of these options, refer to the *VCS User Guide* installed with the VCS software.

The following VCS software command describes the command-line syntax to perform a post-synthesis simulation with the device family library:

```
vcs -R <test bench>.v <gate-level netlist>.v -v <altera device family library>.v \
+transport_int_delays +pulse_int_e/0 +pulse_int_r/0 \
+transport_path_delays +pulse_e/0 +pulse_r/0 ↵
```

Using NativeLink with the VCS Software

The NativeLink® feature in the Quartus II software facilitates the seamless transfer of information between the Quartus II software and EDA tools and allows you to run VCS within the Quartus II software.

Setting Up NativeLink

To run VCS automatically from the Quartus II software using the NativeLink feature, you must specify the path to your simulation tool by performing the following steps:

1. On the Tools menu, click **Options.** The **Options** dialog box appears.
2. In the **Category** list, select **EDA Tool Options**. The **EDA Tool Options** page is shown.
3. Double-click the entry under the **Location of executable** column.
4. Type or browse to the directory containing the executables of your EDA tool.
5. Click **OK**.

You can also specify the path to the simulator's executables by using the `set_user_option` Tcl command:

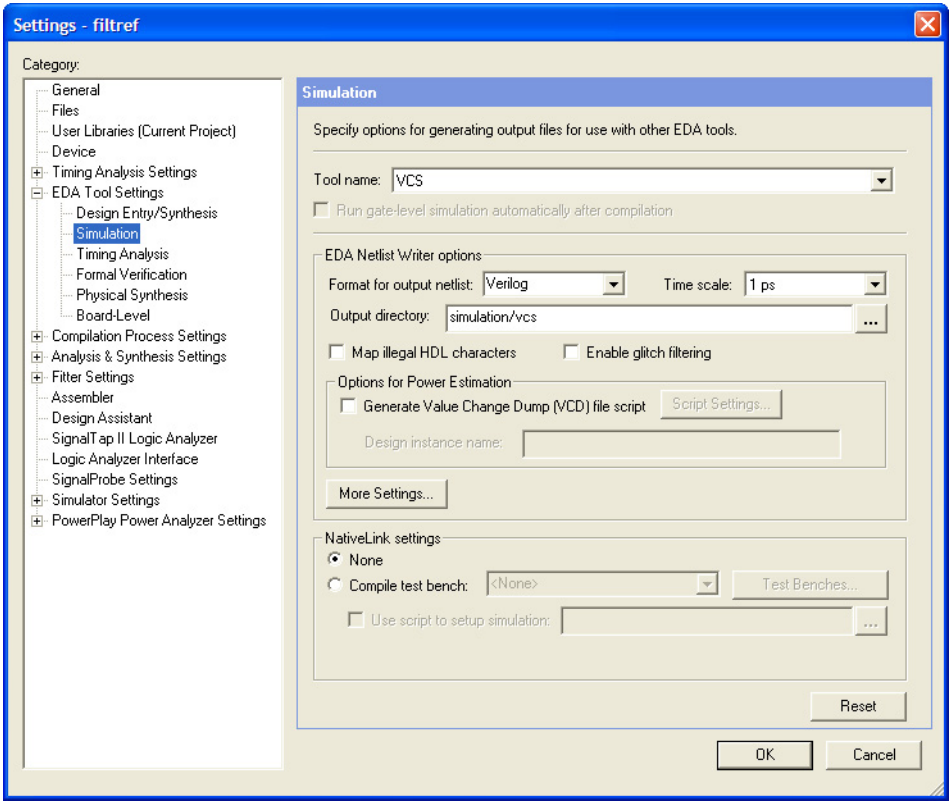
```
set_user_option -name EDA_TOOL_PATH_VCS <path to executables>
```

Performing an RTL Simulation Using NativeLink

To run a functional RTL simulation automatically with the VCS software in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page is shown (Figure 3–3).

Figure 3–3. Simulation Page in the Settings Dialog Box



3. In the **Tool name** list, select **VCS**. You can also modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.

4. If you have test bench files or macro scripts, enter the information under **NativeLink settings**.

For more information on setting up a test bench with NativeLink, refer to the "Setting Up a Test Bench" on page 3–18.

5. Click **OK.**

6. On the Processing menu, point to Start and click **Start Analysis & Elaboration** to perform an analysis and elaboration. This command collects all your file name information and builds your design hierarchy in preparation for simulation.

7. On the Tools menu, point to **EDA Simulation Tool** and click **Run EDA RTL Simulation** to automatically launch VCS, compile all necessary design files, and complete a simulation.

Performing a Gate Level Simulation Using NativeLink

To run a gate-level timing simulation with the VCS software automatically in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.

2. In the **Category** list, select **Simulation**. The **Simulation** page is shown (Figure 3–3).

3. In the **Tool name** list, select **VCS**.

4. You can modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.

5. To perform a gate level simulation after each full compilation, turn on **Run Gate Level Simulation automatically after compilation**.

6. If you have test bench files or macro scripts, enter the information under **NativeLink settings**.

7. Click **OK**.

8. Perform a full compilation. On the Processing menu, click **Start Compilation**.

9. On the Processing menu, point to Start and click **Start EDA Netlist Writer** to generate a simulation netlist of your design.

10. On the Tools menu, point to EDA Simulation Tool and click **Run EDA Gate Level Simulation** to automatically launch VCS, compile all necessary design files, and complete a simulation.

Setting Up a Test Bench

You can automatically launch your EDA simulator tool, compile your design files and test bench files, and perform a simulation automatically using the NativeLink feature.

To setup NativeLink with a test bench, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page is shown.
3. Under **NativeLink settings**, select **None** or **Compile test bench** (Table 3–5).

Table 3–5. NativeLink Settings

Settings	Description
None	Compile simulation models and design files.
Compile test bench	NativeLink compiles simulation models, design files, test bench files, and starts simulation.

4. If you select **Compile test bench**, select your test bench setup from the **Compile test bench** list. You can use different test bench setups to specify different test bench files for different test scenarios. If there are no test bench setups entered, create a test bench setup by performing the following steps:
   a. Click **Test Benches**. The **Test Benches** dialog box appears.
   b. Click **New**. The **New Test Bench Settings** dialog box appears.
   c. In the **Test Bench name** box, type in the test bench setup name which is used to identify between the different test bench setups.
   d. In the **Test bench entity** box, type in the top-level entity name. For example, for a Quartus II generated Verilog test bench, type in <*Vector Waveform File name*>`_vlg_vec_tst`.
   e. In the **Instance** box, type in the full instance path to the top level of your FPGA design. For example, for a Quartus II generated Verilog test bench, type in `i1`.

f. In the **Run for** box, specify in how long you want your simulation to run.

g. Under **Test bench files**, browse and add all your test bench files in the **File name** box. Use the **Up** and **Down** button to reorder your files. The script used by NativeLink compiles the files in the order from top to the bottom.

h. Click **OK**.

i. In the **Test Benches** dialog box, click **OK**.

Creating a Test Bench

In the Quartus II software you can create a Verilog HDL or VHDL test bench from a Vector Waveform File. The generated test bench includes the behavior of the input stimulus and applies it to your instantiated top-level FPGA design.

1. On the File menu, click **Open**. The **Open** dialog box appears.
2. Click the **Files of type** arrow and select **Waveform/Vector Files**. Select your file.
3. Click **Open**.
4. On the File menu, click **Export**. The **Export** dialog box appears.
5. Click the **Save as type** arrow and select **VHDL Test Bench File (*.vht)** or **Verilog Test Bench File (*.vt)**.
6. You can turn on **Add self-checking code to file** to check your simulation results against your Vector Waveform File.
7. Click **Export**.

Scripting Support

You can run procedures and create settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

For detailed information about scripting command options, refer to the **Qhelp** utility.

Type this command to start the Qhelp utility:

```
quartus_sh --qhelp ↵
```

Generating a Post-Synthesis Simulation Netlist for VCS

You can use the Quartus II software to generate a post-synthesis simulation netlist with Tcl commands or with a command at a command prompt.

Tcl Commands

Use the following Tcl commands:

```
set_global_assignment -name EDA_SIMULATION_TOOL "VCS"
set_global_assignment -name EDA_GENERATE_FUNCTIONAL_NETLIST ON
```

Command Prompt

Use the following command to generate a simulation output file for the VCS software simulator; specify VHDL or Verilog HDL for the format:

```
quartus_eda <project name> --simulation=on --format=<format> --tool=vcs
--functional ↵
```

Generating a Gate-Level Timing Simulation Netlist for VCS

You can use the Quartus II software to generate a gate-level timing simulation netlist with Tcl commands or with a command at a command prompt.

Tcl Commands

Use the following Tcl commands:

```
set_global_assignment -name EDA_SIMULATION_TOOL "VCS"
```

Command Prompt

Use the following command to generate a simulation output file for the VCS software simulator. Specify VHDL or Verilog HDL for the format.

```
quartus_eda <project name> --simulation=on --format=<format> --tool=vcs ↵
```

Conclusion

You can use the VCS software in your Altera FPGA design flow to easily and accurately perform functional RTL simulations, post-synthesis simulations, and gate-level functional timing simulations. The seamless integration of the Quartus II software and VCS software make this simulation flow an ideal method for fully verifying an FPGA design.

4. Cadence NC-Sim Support

QII53003-6.0.0

Introduction

This chapter is a getting started guide to using the Cadence Incisive verification platform software in Altera® FPGA design flows. The Incisive verification platform software includes NC-Sim, NC-Verilog, NC-VHDL, Verilog, and VHDL desktop simulators. This chapter provides step-by-step explanations of the basic NC-Sim, NC-Verilog, and NC-VHDL functional, post-synthesis, and gate-level timing simulations. It also describes the location of the simulation libraries and how to automate simulations.

Software Requirements

You must first install the Quartus® II software before using it with the Cadence Incisive verification platform software. The Cadence interface is installed automatically when you install the Quartus II software on your computer.

Table 4–1 shows the Cadence NC simulator versions compatible with specific Quartus II software versions.

Table 4–1. Compatibility Between Software Versions

Quartus II Software	Cadence NC Simulators (UNIX)	Cadence NC Simulators (PC)	Cadence NC Simulators (Linux)
Version 6.0	Version 5.5 s012	Version 5.4 s011	Version 5.5 s12
Version 5.1	Version 5.4 s011	Version 5.4 s011	Version 5.4 s011
Version 5.0	Version 5.4 s004	Version 5.4 p001	Version 5.4 s004
Version 4.2	Version 5.1 s017	Version 5.1 s017	Version 5.1 s017
Version 4.1	Version 5.1 s012	Version 5.1 s010	Version 5.0 p001
Version 4.0	Version 5.0 s005	Version 5.0 s006	Version 5.0 p001

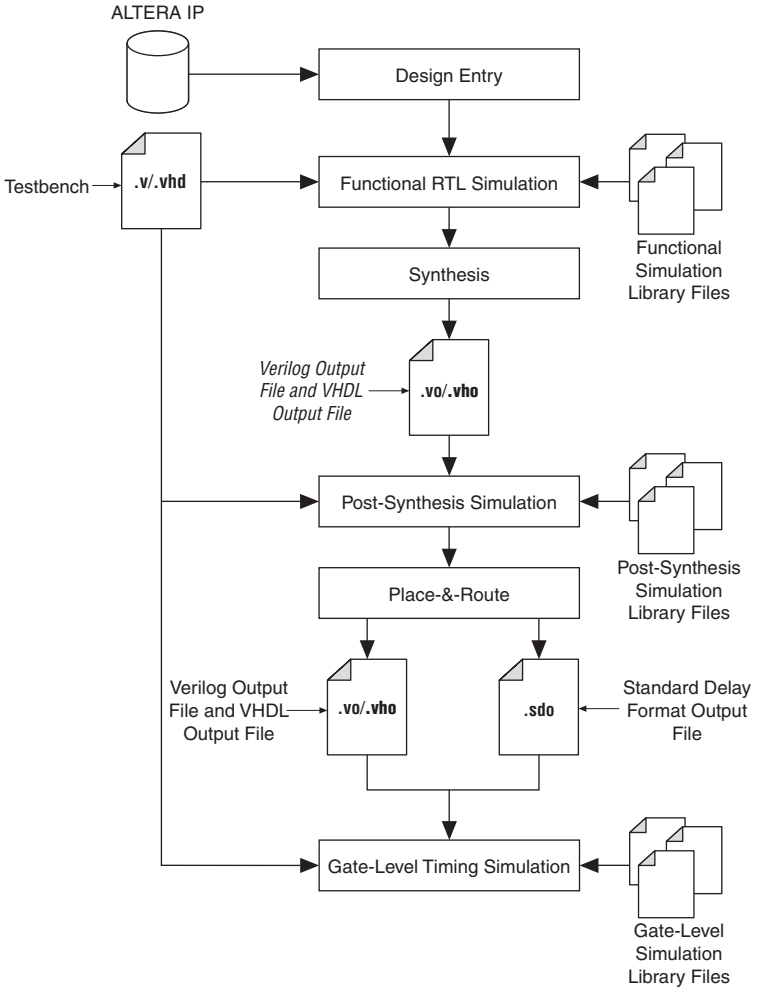
Simulation Flow Overview

The Incisive platform software supports the following simulation flows:

- Functional & RTL Simulation
- Post-Synthesis Simulation
- Gate-Level Timing Simulation
- Using the NativeLink Feature with NC-Sim

Figure 4–1 shows the Quartus II software and Cadence design flow.

Figure 4–1. Quartus II Software Design Flow with Cadence NC Simulators



Functional and RTL simulation verifies the functionality of your design. When you perform a functional simulation with Cadence Incisive simulators, you use your design files (Verilog HDL or VHDL) and the models provided with the Quartus II software. These Quartus II models are required if your design uses the library of parameterized modules (LPM) functions or Altera-specific megafunctions. Refer to "Functional & RTL Simulation" on page 4–5 for more information on how to perform this simulation.

A post-synthesis simulation verifies the functionality of a design after synthesis has been performed. You can create a post-synthesis netlist (**.vo** or **.vho**) in the Quartus II software and use this netlist to perform a post-synthesis simulation with the Incisive simulator. Refer to "Post-Synthesis Simulation" on page 4–20 for more information on how to perform this simulation.

After performing place-and-route, the Quartus II software generates a Verilog Output File (**.vo**) or VHDL Output File (**.vho**) and a Standard Delay Output file (**.sdo**) for gate-level timing simulation. The netlist files map your design to architecture-specific primitives. The Standard Delay Format Output File contains the delay information of each architecture primitive and routing element specific to your design. Together, these files provide an accurate simulation of your design with the selected Altera FPGA architecture. Refer to "Gate-Level Timing Simulation" on page 4–23 for more information on how to perform this simulation.

Operation Modes

In the NC simulators, you can use either the GUI mode or the command-line mode to simulate your design.

You launch the Incisive simulators in GUI mode in a PC or a UNIX environment by typing `nclaunch` ↵ at a command prompt.

To simulate in command-line mode, use the programs shown in Table 4–2.

Table 4–2. Command-Line Programs

Program	Function
ncvlog or **ncvhdl**	NC-Verilog (**ncvlog**) compiles your Verilog HDL code into a Verilog Syntax Tree (**.vst**) file. **ncvlog** also performs syntax and static semantics checks. NC-VHDL (**ncvhdl**) compiles your VHDL code into a VHDL Syntax Tree (**.ast**) file. **ncvhdl** also performs syntax and static semantics checks.
ncelab	NC-Elab (**ncelab**) elaborates the design. **ncelab** constructs the design hierarchy and establishes signal connectivity. This program also generates a Signature File (**.sig**) and a Simulation SnapShot File (**.sss**).
ncsim	NC-Sim (**ncsim**) performs mixed-language simulation. This program is the simulation kernel that performs event scheduling and executes the simulation code.

Quartus II Software & NC Simulation Flow Overview

An overview of the Quartus II software and Cadence NC simulation flow is described below. More detailed information is provided in "Functional & RTL Simulation" on page 4–5, "Post-Synthesis Simulation" on page 4–20, and "Gate-Level Timing Simulation" on page 4–23.

1. Set up your working environment (UNIX only).

   You must set several environment variables in UNIX to establish an environment that facilitates entering and processing designs.

2. Create user libraries.

   Create a file that maps logical library names to their physical locations. These library mappings include your working directory and any design-specific libraries, for example, Altera LPM functions or megafunctions.

3. Compile source code and test benches.

   You compile your design files at the command-line using **ncvlog** (Verilog HDL files) or **ncvhdl** (VHDL files), or on the Tools menu by clicking **Verilog Compiler** or **VHDL Compiler** in NCLaunch. During compilation, the NC software performs syntax and static semantic checks. If no errors are found, compilation produces an

internal representation for each HDL design unit in the source files. By default, these intermediate objects are stored in a single, packed, library database file in your working directory.

4. Elaborate your design.

   Before you can simulate your model, you must define the design hierarchy in a process called elaboration. Use **ncelab** in command-line mode or on the Tools menu, click **Elaborator** in NCLaunch to elaborate the design.

5. Add signals to your waveform.

   Before simulating, specify which signals to view in your waveform using a simulation history manager (SHM) database.

6. Simulate your design.

   Run the simulator with the **ncsim** program (command-line mode) or by clicking **Run** in the SimVision Console window.

Functional & RTL Simulation

The following sections provide detailed instructions for performing functional/RTL simulation using the Quartus II software and the Cadence Incisive platform software tools.

Create Libraries

Before simulating with the Incisive simulator, you must set up libraries with a file named **cds.lib**. The **cds.lib** file is an ASCII text file that maps logical library names—for example, your working directory or the location of resource libraries such as models for LPM functions—to their physical directory paths. When you launch the Incisive simulator, the tool reads **cds.lib** to determine which libraries are accessible and where they are located. There is also a default **cds.lib** file, which you can modify for your project settings.

You can use more than one **cds.lib** file. For example, you can have a project-wide **cds.lib** file that contains library settings specific to a project such as technology or cell libraries and a user **cds.lib** file.

The following sections describe how to create and edit a **cds.lib** file:

- Basic libraries setup
- LPM function, Altera megafunction, and Altera primitive library setup

Basic Library Setup

You can create a **cds.lib** file with any text editor. The following examples show how you use the DEFINE statement to bind a library name to its physical location. The logical and physical names can be the same or you can select different names. The DEFINE statement usage is:

DEFINE <*library name*> <*physical directory path*>

For example, a simple **cds.lib** file for Verilog HDL contains the following lines:

```
DEFINE lib_std /usr1/libs/std_lib
DEFINE worklib ../worklib
```

Using Multiple cds.lib Files

Use the INCLUDE or SOFTINCLUDE statement to reference another **cds.lib** file within a **cds.lib** file. The syntax is:

INCLUDE <*path to another cds.lib*>

or

SOFTINCLUDE <*path to another cds.lib*>

For the Windows operating system, enclose the path with quotation marks if there are spaces in the directory path.

For VHDL or mixed-language simulation, in addition to the DEFINE statements, you must include the default **cds.lib** file (included with NC-Sim). The syntax for including the default **cds.lib** file is:

INCLUDE <*path to NC installation*>/tools/inca/files/cds.lib

or

INCLUDE $CDS_INST_DIR/tools/inca/files/cds.lib

The default **cds.lib** file, provided with NC tools, contains a SOFTINCLUDE statement to include other **cds.lib** files such as **cdsvhdl.lib** and **cdsvlog.lib**. These files contain library definitions for IEEE libraries and Synopsys libraries.

Create a cds.lib File in Command-Line Mode

To create a **cds.lib** file at a the command prompt, perform the following steps:

1. Create a directory for the work library and any other libraries you need by typing the following command at a command prompt:

   `mkdir` <*library name*> ↵

   For example: `mkdir worklib` ↵

2. Using a text editor, create a **cds.lib** file and add the following line to it:

   `DEFINE` <*library name*> <*physical directory path*>

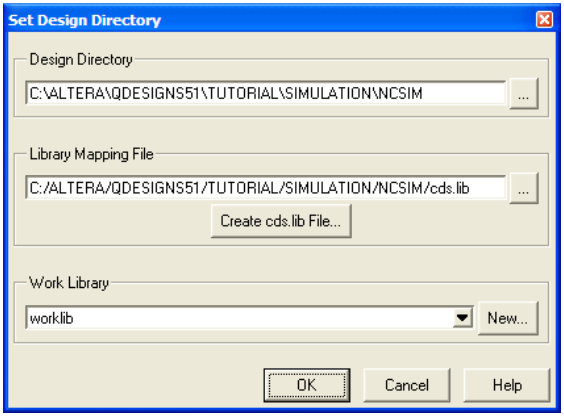
   For example: `DEFINE worklib ./worklib`

Create a cds.lib File in GUI Mode

To create a **cds.lib** file using the GUI, perform the following steps:

1. Type `nclaunch` ↵ at the command line to launch the GUI.
2. If the NCLaunch window is not in multiple step mode, on the File menu, click **Switch to Multiple Step**.
3. Change your design directory on the File menu by clicking **Set Design Directory**. The **Set Design Directory** dialog box appears (Figure 4–2).

Figure 4–2. Creating a Work Directory in GUI Mode



4. Click **Browse** to navigate to your design directory.
5. Click **Create cds.lib File** and in the **New cds.lib File** dialog box, click **Save** and choose the libraries you want to include.
6. Click **New** under **Work Library**.
7. Enter your new work library name, for example, `worklib`.
8. Click **OK**. The new library is displayed under **Work Library**. Figure 4–2 shows an example using the directory name **worklib**.
9. Repeat steps 7 and 8 for each functional simulation library. For example, `lpm`, `altera_mf`, and `altera`.
10. Click **OK** in the **Set Design Directory** dialog box.

You can edit your libraries by editing the **cds.lib** file. Edit the **cds.lib** file by right-clicking the **cds.lib** filename in the right side of the window and choosing **Edit**.

LPM Functions, Altera Megafunctions, & Altera Primitives Libraries

Altera provides behavioral descriptions for LPM functions, Altera-specific megafunctions, and Altera primitives. You can implement the megafunctions in a design using the Quartus II MegaWizard® Plug-In Manager or by instantiating them directly from your design file. You must set up resource libraries so that you can simulate your design in the Incisive simulator if your design uses LPM functions, Altera megafunctions, or Altera primitives.

Many LPM functions and Altera megafunctions use memory files. You must convert the memory files into a format the Incisive tools can read before simulating. Follow the instructions in "Compile Source Code & Test Benches" on page 4–12 to connect the memory files.

Altera provides megafunction behavioral descriptions in the files shown in Table 4–3. These library files are located in the following directory:

<path to Quartus II installation>/**eda**/**sim_lib** directory.

For more information on LPM functions and Altera megafunctions, refer to the Quartus II Help.

Table 4–3. Megafunction Behavioral Description Files

Library Description	Verilog HDL	VHDL
LPM	**220model.v**	**220model.vhd** *(1)* **220model_87.vhd** *(2)* **220pack.vhd**
Altera megafunction	**altera_mf.v**	**altera_mf.vhd** *(1)* **altera_mf_87.vhd** *(2)* **altera_components.vhd**
Altera primitives	altera_primatives.v	altera_primitives.vhd *(1)* altera_primitives_components.vhd
IP functional simulation model	**sgate.v**	**sgate.vhd** **sgate_pack.vhd**
`altgxb`	**stratixgx_mf.v** *(3)*	**stratixgx_mf.vhd** *(3)* **stratixgx_mf_components.vhd** *(3)*
`alt2gxb`	**stratixiigx_hssi_atoms.v** *(3)*, *(4)*	**stratixiigx_hssi_atoms.vhd** **stratixiigx_hssi_components.vhd** *(3)*, *(4)*

Notes to Table 4–3:
(1) Use this model with VHDL 93.
(2) Use this model with VHDL 87.
(3) The `alt2gxb` and `altgxb` library files require the **lpm** and **sgate** libraries.
(4) You must generate a functional simulation netlist for simulation.

If an `lpm` library does not exist, set up a library for LPM functions by creating a new directory and adding the following line to your **cds.lib** file:

```
DEFINE lpm <path>/<directory name>
```

If an `altera_mf` library does not exist, set up a library for Altera megafunctions by adding the following line to your **cds.lib** file:

```
DEFINE altera_mf <path>/<directory name>
```

Megafunctions Requiring Atom Libraries

The following Altera megafunctions require device atom libraries to perform a functional simulation in a third-party simulator:

- `altclkbuf`
- `altclkctrl`
- `altdq`
- `altdqs`
- `altddio_in`
- `altddio_out`
- `altddio_bidir`
- `altufm_none`
- `altufm_parallel`
- `altufm_spi`
- `altmemmult`
- `altremote_update`

The device atom library files are located in the following directory:

*<path to Quartus II installation>***/eda/sim_lib**

Simulating a Design with Memory

The NC-Sim simulator supports simulating Altera memory megafunctions initialized with Hexadecimal (Intel-Format) File (**.hex**) or RAM Initialization Files (**.rif**).

Although synthesis is able to read a Memory Initialization File (**.mif**), these files are not supported in simulations with third-party tools and must be converted to either a Hexadecimal (Intel-Format) File or RAM Initialization File.

Table 4–4 summarizes the different types of memory initialization file formats that are supported with each RTL language.

Table 4–4. Simulation Support for Memory Initialization Files

File	Verilog HDL	VHDL
Hexadecimal (Intel-Format) File	Yes *(1)*	Yes
Memory Initialization File	No	No
RAM Initialization File	Yes *(2)*	No

Notes to Table 4–4:

(1) For memories and library files from Quartus II software version 5.0 and earlier, you are required to use `PLI` library containing the `convert_hex2ver` task function.

(2) Requires the `USE_RIF` macro to be defined.

To covert your Memory Initialization File into either a Hexadecimal (Intel-Format) File or RAM Initialization File, perform the following steps:

1. Open the Memory Initialization File and on the File menu, click **Export**. The **Export** dialog box appears.

2. Select **Hexadecimal (Intel-Format) File (*.hex)** or **RAM Initialization File (*.rif)** from the **Save as type** list and click **OK**.

Alternatively, you can convert a Memory Initialization File to a RAM Initialization File using the `mif2rif.exe` executable located in the <*Quartus II installation*>**/bin** directory. An example of this executable is:

```
mif2rif <mif_file> <rif_file>
```

3. Modify the HDL file generated with the MegaWizard Plug-In Manager.

   The MegaWizard Plug-In Manager-generated Altera memory megafunction wrapper file includes the `lpm_file` parameter for LPM memories, or the `init_file` parameter for Altera-specific memories to point to the initialization file.

   In a text editor, open the MegaWizard Plug-In Manager generated wrapper file and edit the `lpm_file` or `init_file` parameters to point to the Hexadecimal (Intel-Format) File or RAM Initialization File, as shown below:

   ```
   lpm_ram_dp_component.lpm_file = "<path to HEX/RIF>"
   ```

4. Compile the functional library files with compiler directives.

   If you use a Hexadecimal (Intel-Format) File, then no compiler directives are required. If you use a RAM Initialization File, then the `USE_RIF` macro must be defined when compiling the model library files. For example, the following should be entered when compiling the `altera_mf` library when RAM Initialization Files are used:

   ```
   ncvlog -work altera_mf altera_mf.v -DEFINE
   "USE_RIF=1"
   ```

For Quartus II software versions 5.0 and earlier, you must define the `NO_PLI` macro instead of `USE_RIF`. The `NO_PLI` macro is forward compatible with the Quartus II software.

Compile Source Code & Test Benches

Compile your test bench and design files with **ncvlog** (for Verilog HDL files) and **ncvhdl** (for VHDL files). Both **ncvlog** and **ncvhdl** perform syntax checks and static semantic checks. A successful compilation produces an internal representation for each HDL design unit in the source files. By default, these intermediate objects are stored in a single, packed, library database file in your work library directory.

Compilation in Command-Line Mode

To compile from the command line, use one of the following commands:

You must create a work library before compiling.

- Verilog HDL:

```
ncvlog <options> -work <library name> <design files> ↵
```

- VHDL:

```
ncvhdl <options> -work <library name> <design files> ↵
```

If your design uses LPM, Altera megafunctions, or Altera primitives you must also compile the Altera-provided functional models. The following commands show an example of each.

- Verilog HDL:

```
ncvlog -WORK lpm 220model.v ↵
ncvlog -WORK altera_mf altera_mf.v ↵
ncvlog -WORK altera altera_primitives.v ↵
```

If you are using the Quartus II software versions 5.0 and earlier and your design uses a memory initialization file, compile the **nopli.v** file, which is located in the <*Quartus II installation*>/**eda**/**sim_lib** directory, before you compile your model. For example:

```
ncvlog -WORK lpm nopli.v 220model.v ↵
ncvlog -WORK altera_mf nopli.v altera_mf.v ↵
```

Another option is to define `NO_PLI` during compilation with the following command:

```
ncvlog -DEFINE "NO_PLI=1" -WORK lpm 220model.v ↵
ncvlog -DEFINE "NO_PLI=1" -WORK altera_mf altera_mf.v ↵
```

- VHDL:

```
ncvhdl -V93 -WORK lpm 220pack.vhd ↵
ncvhdl -V93 -WORK lpm 220model.vhd ↵
ncvhdl -V93 -WORK altera_mf altera_mf_components.vhd ↵
ncvhdl -V93 -WORK altera_mf altera_mf.vhd ↵
ncvhdl -V93 -WORK altera altera_primitives_components.vhd ↵
```

```
ncvhdl -V93 -WORK altera altera_primitives.vhd ↵
```

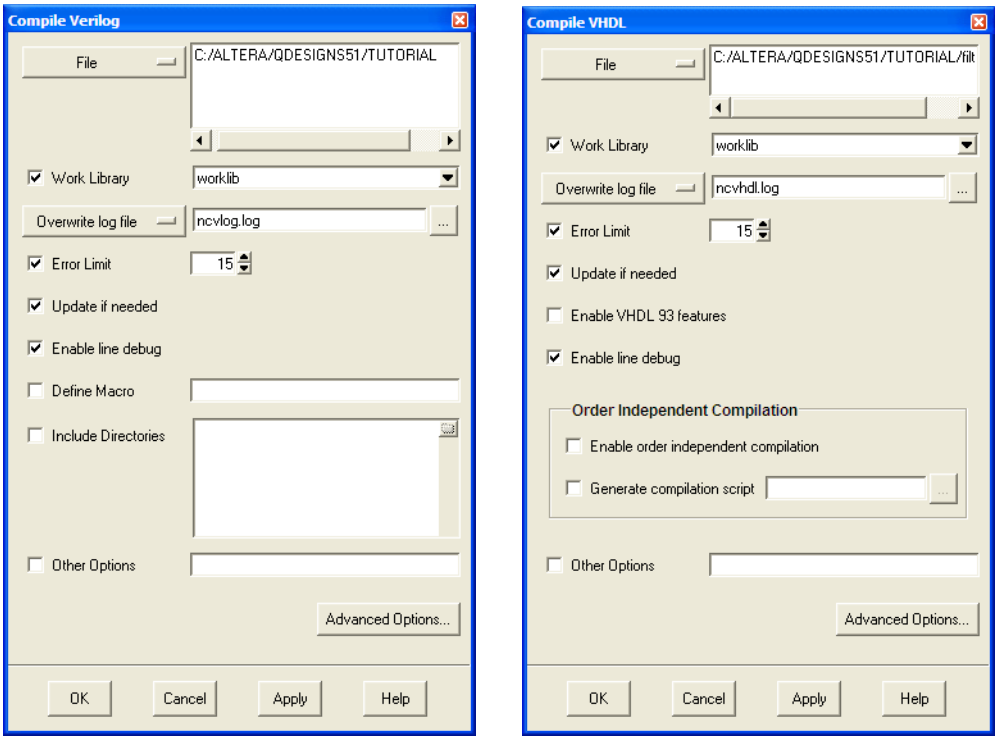
Compilation in GUI Mode

To compile using the NCLaunch GUI, perform the following steps:

1. Right-click a library filename in the NCLaunch window and click **NCVlog** (Verilog HDL) or **NCVhdl** (VHDL).

   Alternatively, on the Tools menu, click **Verilog Compiler** or **VHDL Compiler**. Figure 4–3 shows the **Compile Verilog** and **Compile VHDL** dialog boxes.

Figure 4–3. Compiling Verilog HDL & VHDL Files



2. Select the file and click **OK** in the **Compile Verilog** or **Compile VHDL** dialog box to begin compilation. The dialog box closes and returns you to NCLaunch.

The command-line equivalent argument is shown at the bottom of the NCLaunch window.

Elaborate Your Design

Before you can simulate your design, you must define the design hierarchy in a process called elaboration. When you use the Incisive simulator, you use the language-independent **ncelab** program to elaborate your design. The **ncelab** program constructs a design hierarchy based on the design's instantiation and configuration information, establishes signal connectivity, and computes initial values for all objects in the design. The elaborated design hierarchy is stored in a simulation snapshot, which is the representation of your design that the simulator uses to run the simulation. The snapshot is stored in the library database file along with the other intermediate objects generated by the compiler and elaborator.

If you are running the NC-Verilog simulator with the single-step invocation method (**ncverilog**), and want to compile your source files and elaborate the design with one command, use the `+elaborate` option to stop the simulator after elaboration. For example:

```
ncverilog +elaborate test.v ↵
```

Elaboration in Command-Line Mode

To elaborate your Verilog HDL or VHDL design from the command line, use the following command:

```
ncelab [options] [<library>.]<cell>[:<view>] ↵
```

You can set your simulation timescale using the `-TIMESCALE <arguments>` option. The following example elaborates a dual-port RAM with the time scale option:

```
ncelab -TIMESCALE 1ps/1ps worklib.lpm_ram_dp_test:entity ↵
```

If you specified a timescale of 1 ps in the Verilog HDL test bench, the `TIMESCALE` option is not necessary. Using a ps resolution ensures the correct simulation of your design.

If your design includes high speed signals, you may need to add the following pulse reject options with your ncelab command.

```
ncelab -TIMESCALE 1ps/1ps worklib.mydesign:entity -PULSE_R 0 -PULSE_INT_R 0 ↵
```

For more information on the pulse reject options, refer to the *SDF Annotate Guide* from Cadence.

To list the elements in your library and the available views, use the **ncls** program. The following command displays all of the cells and their views in your current **worklib** directory:

```
ncls -library worklib ↵
```

For more information on the **ncls** program, refer to the Cadence NC-Verilog Simulator Help or Cadence NC-VHDL Simulator Help.

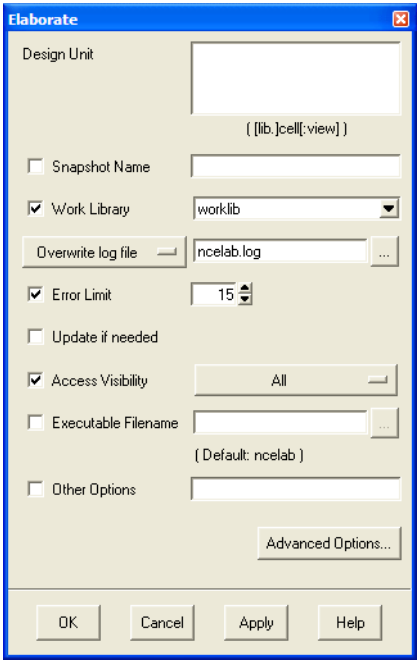
Elaboration in GUI Mode

To elaborate using the GUI, perform the following steps:

1. In the right side of the NCLaunch window, expand your current work library.
2. Select and expand (if necessary) the entity or module name you want to elaborate.
3. Right-click the view you want to display and click **NCElab**. The **Elaborate** dialog box appears (Figure 4–4). Optionally, on the Tools menu, click **Elaborator**.
4. In the **Other Options** box, set the simulation timescale by typing (Figure 4–4):

   ```
   -TIMESCALE 1ps/1ps
   ```

Figure 4–4. Elaborating the Design



5. Click **OK** in the **Elaborate** dialog box to begin elaboration. The dialog box closes and returns you to NCLaunch.

Add Signals to View

To view the stored selected signals, use an SHM database, which is a Cadence proprietary waveform database, to store the selected signals you want to view. Before you can specify which signals to view, you must create the database by adding commands to your code. Or you can create a Value Change Dump File (**.vcd**) to store the simulation history.

For more information on using a Value Change Dump File, refer to the Cadence NC-Sim User Manual included with the installation.

Adding Signals in Command-Line Mode

To create an SHM database, specify the system tasks, described in Table 4–5 in your Verilog HDL code.

For VHDL, you can use the Tcl command interface or C function calls to add signals to a database. Refer to the Cadence documentation included in the installation package for details.

Table 4–5. SHM Database System Tasks

System Task	Description
`$shm_open("<filename>.shm");`	Opens a database. If you do not specify a filename, the default **waves.shm** database is opened. If a database with the specified name does not exist, it is created for you.
`$shm_probe("[A|S|C]");`	Probe signals. You can specify the signals to probe; if you do not specify signals, the default is all ports in the current scope. `A` probes all nodes in the current scope. `S` probes all nodes below the current scope. `C` probes all nodes below the current scope and in libraries.
`$shm_save;`	Saves the database.
`$shm_close;`	Closes the database.

The following sample shows a simple example of how to add signals to an SHM database.

```
initial
    begin
        $shm_open ("waves.shm");
        $shm_probe ("AS");
    end
```

You can insert this code sample into your Verilog HDL file. It is applicable only for Verilog HDL files. For more information on these system tasks, refer to the Cadence NC-Sim software user manual included in the installation.

Adding Signals in GUI Mode

To add signals in GUI mode, perform the following steps:

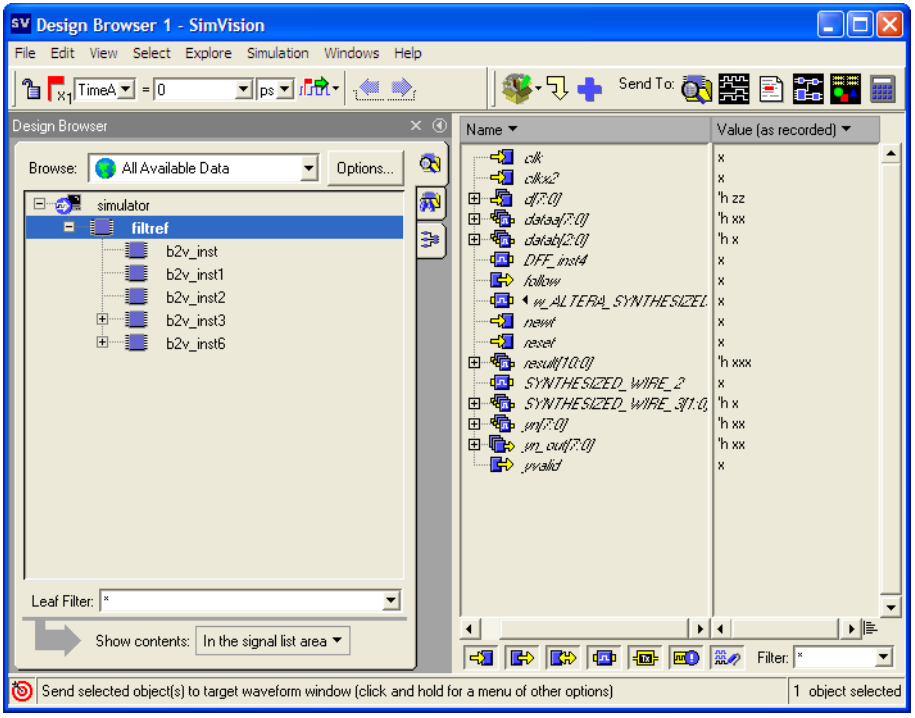
1. In the NC-Sim software, load the design.
    a. In the NCLaunch window, click the **+** icon to expand the **Snapshots** directory.
    b. Right-click on the **lib.cell:view** you want to simulate and click **NCSim**.

c. Click **OK** in the **Simulate** dialog box.

After you load the design, the SimVision Console and SimVision Design Browser windows are shown. Figure 4–5 shows the SimVision Design Browser window.

2. In the Design Browser window, select a module in the left side of the window to display the signal names (Figure 4–5).

Figure 4–5. SimVision Design Browser



3. To send the selected signals to the Waveform Viewer, perform one of the following steps:

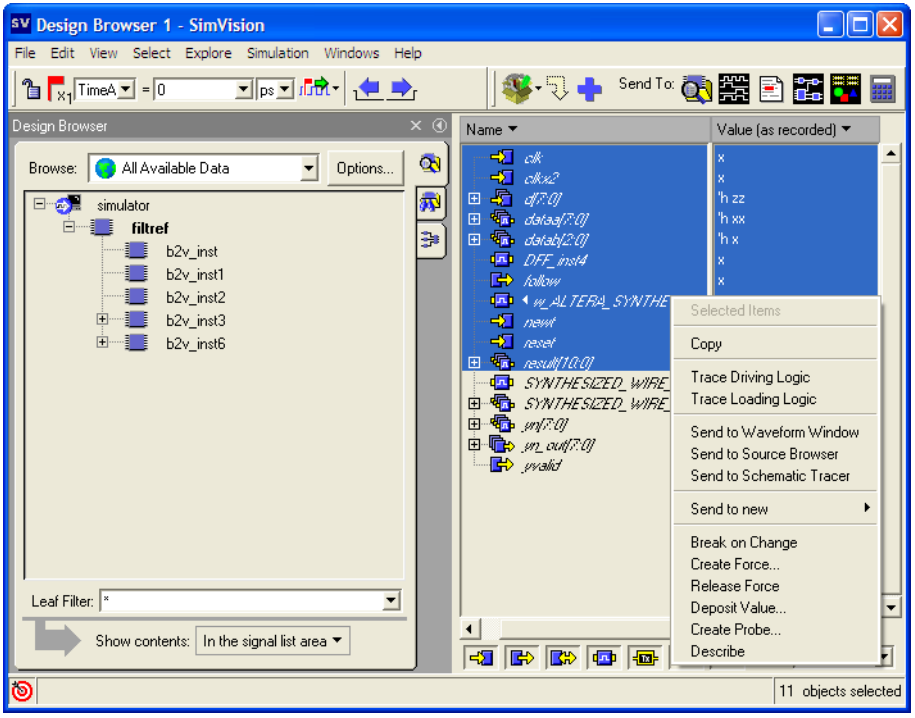
Select a group of signals from the right side of the Design Browser window and click the **Send to Waveform Viewer** icon in the **Send To** toolbar (the upper-right area of the Design Browser window).

or

Right-click the signals and click **Send to Waveform Window** (Figure 4–6).

A waveform window showing all of your signals is shown. You are now ready to simulate your test bench and design.

Figure 4–6. Selecting Signals in the Design Browser Window



Simulate Your Design

After you have compiled and elaborated your design, you can simulate it using **ncsim**. The **ncsim** program loads the file, or snapshot, generated by **ncelab** as its primary input. It then loads other intermediate objects referenced by the snapshot. If you enable interactive debugging, it may also load HDL source files and script files. The simulation output is controlled by the model or debugger. The output can include result files generated by the model, SHM database, or Value Change Dump File.

Functional/RTL Simulation in Command-Line Mode

To perform functional/RTL simulation of your Verilog HDL or VHDL design at the command line, type the following command:

```
ncsim [options] [<library>.]<cell>[:<view>] ↵
```

For example:

```
ncsim worklib.lpm_ram_dp:syn ↵
```

Table 4–6 shows some of the options you can use with **ncsim**.

Table 4–6. ncsim Options

Options	Description
-gui	Launch GUI mode
-batch	Used for non-interactive mode
-tcl	Used for interactive mode (not required when using `-gui`)

Functional/RTL Simulation in GUI Mode

You can run and step through simulation of your Verilog HDL or VHDL design in the GUI. In the Design Browser window, on the Simulation menu, click **Run** to begin the simulation.

You must load the design before simulating. If you have not done so, refer to step 1 in "Adding Signals in GUI Mode" on page 4–17 for instructions.

Post-Synthesis Simulation

The following sections provide detailed instructions for performing post-synthesis simulation using Quartus II output files, simulation libraries, and the Incisive platform software.

Quartus II Simulation Output Files

After performing synthesis with either a third-party synthesis tool or with the Quartus II integrated synthesis, you must generate a simulation netlist for functional simulations. To generate a simulation netlist for functional simulation, perform the following steps in the Quartus II software:

1. Perform Analysis and Synthesis. On the Processing menu, point to Start and click **Start Analysis & Synthesis**.

2. Turn on the **Generate Netlist for Functional Simulation Only** option by performing the following steps:

   a. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.

   b. In the **Category** list, select **Simulation**. The **Simulation** page is shown.

   c. In the **Tool name** list, select **NCSim**.

   d. Under **EDA Netlist Writer options**, in the **Format for output netlist** list, select **VHDL** or **Verilog**. You can also modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.

   e. Click **More Settings**. The **More EDA Tools Simulation Settings** dialog box appears. In the **Existing options settings list**, click **Generate Netlist for Functional Simulation Only** and select **On** from the **Setting** list under **Option**.

   f. Click **OK**.

   g. In the **Settings** dialog box, click **OK**.

3. Run the EDA Netlist Writer. On the Processing menu, point to Start and click **Start EDA Netlist Writer**.

During the EDA Netlist Writer stage, the Quartus II software produces a Verilog Output File (**.vo**) or VHDL Output File (**.vho**) that can be used for post-synthesis simulations in the NC-Sim software. This netlist file is mapped to architecture-specific primitives. No timing information is included at this stage. The resulting netlist is located in the output directory you specified in the Settings dialog box, which defaults to the *<project directory>***/simulation/NCSim** directory.

Create Libraries

Create the following libraries for your simulation:

- Work library
- Device family library targeting your design targets using the following files in the *<path to Quartus II installation>*/**eda**/**sim_lib** directory:
  - *<device_family>*_**atoms.v**
  - *<device_family>*_**atoms.vhd**
  - *<device_family>*_**components.vhd**

Compile Project Files & Libraries

Compile the project files and libraries into your work directory using the **ncvlog** or **ncvhdl** programs or the GUI. Include the following files:

- Test bench file
- The Quartus II software functional output netlist file (Verilog Output File or VHDL Output File)
- Atom library file for the device family *<device family>*_**atoms.***<**v**|**vhd**>*
- For VHDL, *<device family>*_**components.vhd**

Refer to the "Compile Source Code & Test Benches" on page 4–12 section for instructions on compiling.

Elaborate Your Design

Elaborate your design using the **ncelab** program as described in "Elaboration in GUI Mode" on page 4–15.

Add Signals to the View

Refer to the section "Add Signals to View" on page 4–16 for information on adding signals to the view.

Simulate Your Design

Simulate your design using the **ncsim** program as described in "Simulate Your Design" on page 4–19.

Gate-Level Timing Simulation

The following sections provide detailed instructions for performing timing simulation using the Quartus II output files, simulation libraries, and Cadence NC tools.

Generating a Gate-Level Timing Simulation Netlist

To perform gate-level timing simulation, the NC-Sim software requires information on how the design was placed into device-specific architectural blocks. The Quartus II software provides this information in the form of a Verilog Output File for Verilog HDL designs and a VHDL Output File for VHDL designs. The accompanying timing information is stored in the Standard Delay Output File (**.sdo**), which annotates the delay for the elements found in the Verilog Output File or VHDL Output File.

To generate the Verilog Output File or VHDL Output Files and the Standard Delay File, perform the following steps:

1. Perform a full compilation. On the Processing menu, click **Start Compilation**.
2. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
3. In the **Category** list, select **Simulation**. The **Simulation** page is shown.
4. In the **Tool name** list, select **NCSim**.
5. Under **EDA Netlist Writer options**, in the **Format for output netlist** list, select **VHDL** or **Verilog**. You can also modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.
6. Click **OK**.
7. Run the EDA Netlist Writer. On the Processing menu, point to Start and click **Start EDA Netlist Writer**.

   During the EDA Netlist Writer stage, the Quartus II software produces a Verilog Output File (**.vo**), VHDL Output File (**.vho**), and a Standard Delay Output file (**.sdo**) used for gate-level timing simulations in the NC-Sim software. This netlist file is mapped to architecture-specific primitives. The timing information for the netlist is included in the Standard Delay Output file. The resulting netlist is located in the output directory you specified in the Settings dialog box, which defaults to the following directory:

<project directory>/simulation/modelsim

Quartus II Timing Simulation Libraries

Altera device simulation library files are provided in the *<Quartus II installation>*/**eda**/**sim_lib** directory. The Verilog Output File or VHDL Output File requires the library for the device your design targets. For example, the Stratix® device family requires the following library files:

- stratix_atoms.v
- **stratix_atoms.vhd**
- **stratix_components.vhd**

If your design targets a Stratix device, you must set up the appropriate mappings in your **cds.lib** file. Refer to "Create Libraries" for more information.

Create Libraries

Create the following libraries for your simulation:

- Work library
- Device family libraries targeting using the following files in the *<path to Quartus II installation>*/**eda**/**sim_lib** directory:
  - *<device_family>***_atoms.v**
  - *<device_family>***_atoms.vhd**
  - *<device_family>***_components.vhd**

For step-by-step instructions on creating libraries, refer to "Basic Library Setup" on page 4–6 and "LPM Functions, Altera Megafunctions, & Altera Primitives Libraries" on page 4–8.

Compile the Project Files & Libraries

Compile the project files and libraries into your work directory using the **ncvlog** or **ncvhdl** programs or the GUI. Include the following files:

- Test bench file
- The Quartus II software functional output netlist file (Verilog Output File or VHDL Output File)
- Atom library file for the device family *<device family>***_atoms.***<v|vhd>*
- For VHDL, *<device family>***_components.vhd**

For instructions on compiling, refer to "Compile Source Code & Test Benches" on page 4–12.

Elaborate Your Design

When performing elaboration with the Quartus II-generated Verilog HDL netlist file, the Standard Delay Format Output File is read automatically. When you run **ncelab**, it recognizes the embedded system task $sdf_annotate and automatically compiles and annotates the Standard Delay Format Output File (runs **ncsdfc** automatically).

The Standard Delay Format Output File should be located in the same directory where you invoke an elaboration or simulation, because the `$sdf_annotate` task references the Standard Delay Format Output File without using a full path. If you are invoking an elaboration or simulation from a different directly, you can either comment out the `$sdf_annotate` and annotate the Standard Delay Format Output File with the GUI, or add the full path of the Standard Delay Format Output File.

Refer to "Elaborate Your Design" on page 4–14 for step-by-step instructions on elaboration.

For VHDL, the Quartus II software-generated VHDL netlist file does not contain system task calls to locate your SDF file; therefore, you must compile the Standard Delay Format Output File manually. Refer to "Compiling the Standard Delay Output File (VHDL Only) in Command-Line Mode" and "Compiling the Standard Delay Output File (VHDL Only) in GUI Mode" for information on compiling the Standard Delay Format Output File.

Compiling the Standard Delay Output File (VHDL Only) in Command-Line Mode

To annotate the Standard Delay Format Output File timing data from the command line, perform the following steps:

1. Compile the Standard Delay Format Output File using the **ncsdfc** program by typing the following command at the command prompt:

   `ncsdfc <project name>_vhd.sdo -output <output name>` ↵

   The **ncsdfc** program generates an <*output name*>**.sdf.X** compiled SDF output file.

   If you do not specify an output name, **ncsdfc** uses <*project name*>**.sdo.X**.

2. Specify the compiled Standard Delay Format Output File for the project by adding the following command to an ASCII SDF command file for the project:

```
COMPILED_SDF_FILE = "<project name>.sdf.X" SCOPE = <instance path>
```

The following is an example of an SDF command file:

```
// SDF command file sdf_file
COMPILED_SDF_FILE = "lpm_ram_dp_test_vhd.sdo.X",
SCOPE = :tb,
MTM_CONTROL = "TYPICAL",
SCALE_FACTORS = "1.0:1.0:1.0",
SCALE_TYPE = "FROM_MTM";
```

After you compile the Standard Delay Format Output File, run the following command to elaborate the design:

```
ncelab worklib.<project name>:entity -SDF_CMD_FILE <SDF Command File> ↵
```

Compiling the Standard Delay Output File (VHDL Only) in GUI Mode

To annotate the Standard Delay Format Output File timing data in the GUI, perform the following steps in the NCLaunch window:

1. On the Tools menu, click **SDF Compiler**. The **Compile SDF** dialog box appears.
2. In the **SDF File** box, type in the name of the Standard Delay Format Output File for the project.
3. Click **OK**.

   When the Standard Delay Format Output File compilation is complete, you can elaborate the design. Refer to "Elaboration in GUI Mode" on page 4–15 for step-by-step instructions.

   If you are performing a VHDL gate-level simulation, you must create an SDF command file before you begin elaboration. To create the SDF command file, perform steps 5 through 11.

4. On the Tools menu, click **Elaborator**. The **Elaborate** dialog box appears.
5. Click **Advanced Options**.
6. Click **Annotation**.

7. Turn on **Use SDF File**.
8. Click **Edit**.
9. Browse to the location of the SDF command file name.
10. Click **Add** and browse to the location of the Standard Delay Format Output File in the **Compiled SDF File** box and click **OK**.
11. Click **OK** to save and exit the **SDF Command File** dialog box.

Add Signals to View

Refer to the section "Add Signals to View" on page 4–16 for information on adding signals to view.

Simulate Your Design

Simulate your design using the **ncsim** program as described in "Simulate Your Design" on page 4–19.

Simulating Designs that Include Transceivers

If your design includes a Stratix II GX or Stratix GX transceiver, then you must compile additional library files to perform functional or timing simulations.

Stratix GX Functional Simulation

To perform a functional simulation of your design that instantiates the `altgxb` megafunction, enabling the gigabit transceiver block (GXB) on Stratix GX devices, compile the **stratixgx_mf** model file into the **altgxb** library.

The **stratixgx_mf** model file references the **lpm** and **sgate** libraries, so you will need to create these libraries to perform a simulation.

Example of Compiling Library Files for Functional Stratix GX Simulation in Verilog HDL

To compile the libraries necessary for a functional simulation of a Verilog HDL design targeting a Stratix GX device, type the following commands at the NC Sim command prompt:

```
ncvlog -work lpm 220model.v ↵
ncvlog -work altera_mf altera_mf.v ↵
ncvlog -work sgate sgate.v ↵
```

```
ncvlog -work altgxb stratixgx_mf.v ↵
ncsim work.<my design> ↵
```

Example of Compiling Library Files for Functional Stratix GX Simulation in VHDL

To compile the libraries necessary for functional simulation of a VHDL design targeting a Stratix GX device, type the following commands at the NC-Sim command prompt:

```
ncvhdl -work lpm 220pack.vhd 220model.vhd ↵
ncvhdl -work altera_mf altera_mf_components.vhd altera_mf.vhd ↵
ncvhdl -work sgate sgate_pack.vhd sgate.vhd ↵
ncvhdl -work altgxb stratixgx_mf.vhd stratixgx_mf_components.vhd ↵
ncsim work.<my design> ↵
```

Stratix GX Post-Fit (Timing) Simulation

To perform a post-fit timing simulation of your design that includes a Stratix GX transceiver, compile the **stratixgx_atoms** and **stratixgx_hssi_atoms** model files into the **stratixgx** and **stratixgx_gxb** libraries respectively.

You need to create these libraries to perform a simulation because the **stratixgx_hssi_atoms** model file references the **lpm** and **sgate** libraries.

Example of Compiling Library Files for Timing Stratix GX Simulation in Verilog HDL

To compile the libraries necessary to timing simulation of a Verilog HDL design targeting a Stratix GX device, type the following commands at the NC-Sim command prompt:

```
ncvlog -work lpm 220model.v ↵
ncvlog -work altera_mf altera_mf.v ↵
ncvlog -work sgate sgate.v ↵
ncvlog -work stratixgx stratixgx_atoms.v ↵
ncvlog -work stratixgx_gxb stratixgx_hssi_atoms.v ↵
ncelab work.<my design> -TIMESCALE 1ps/1ps -PULSE_R 0 \
-PULSE_INT_R 0 ↵
```

Example of Compiling Library Files for Timing Stratix GX Simulation in VHDL

To compile the libraries necessary for timing simulation of a VHDL design targeting a Stratix GX device, type the following commands at the NC-Sim command prompt:

```
ncvhdl -work lpm 220pack.vhd 220model.vhd ↵
ncvhdl -work altera_mf altera_mf_components.vhd altera_mf.vhd ↵
ncvhdl -work sgate sgate_pack.vhd sgate.vhd ↵
ncvhdl -work stratixgx stratixgx_atoms.vhd stratixgx_components.vhd ↵
ncvhdl -work stratixgx_gxb stratixgx_hssi_atoms.vhd \
stratixgx_hssi_components.vhd ↵
ncelab work.<my design> -TIMESCALE 1ps/1ps -PULSE_R 0 -PULSE_INT_R 0 ↵
```

Stratix II GX Functional Simulation

To perform a post-fit timing simulation of your design that instantiates the `alt2gxb` megafunction, edit your **cds.lib** file so that all the libraries point to the work library, and compile the **stratixiigx_hssi** model file into the **stratixiigx_hssi** library. When compiling the library files, you can safely ignore the following warning message:

```
"Multiple logical libraries mapped to a single location"
```

The following example is of the **cds.lib** file.

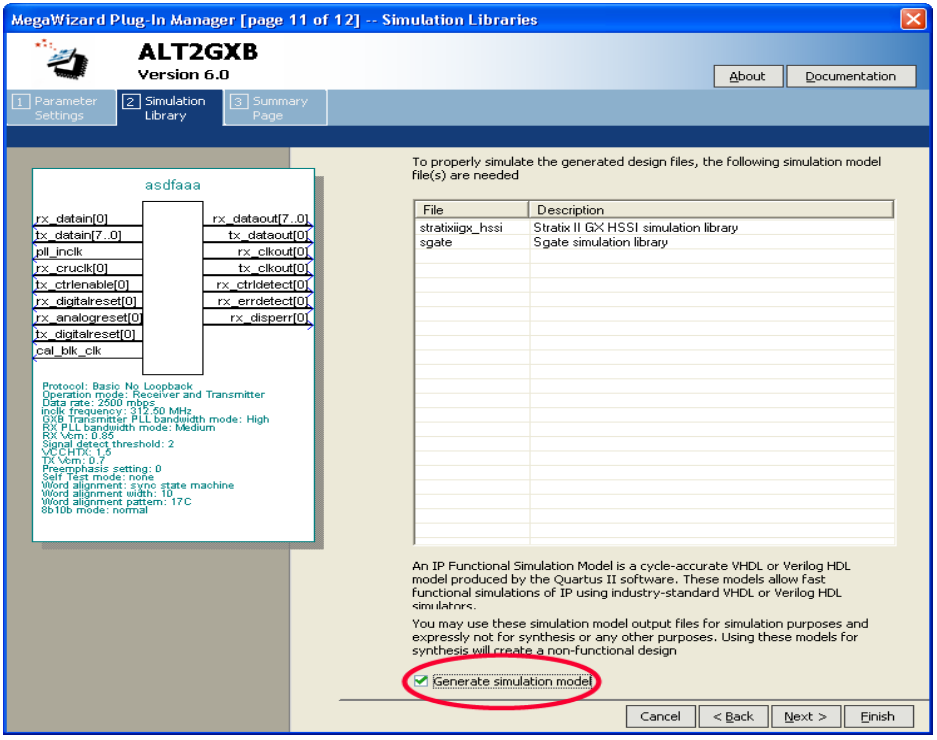
Example 4–1. Example of a cds.lib File

```
SOFTINCLUDE ${CDS_INST_DIR}/tools/inca/files/cdsvhdl.lib
SOFTINCLUDE ${CDS_INST_DIR}/tools/inca/files/cdsvlog.lib
DEFINE work ./ncsim_work
DEFINE stratixiigx_hssi ./ncsim_work
DEFINE stratixiigx ./ncsim_work
DEFINE lpm ./ncsim_work
DEFINE sgate ./ncsim_work
```

The **stratixiigx_hssi_atoms** model file references the **lpm** and **sgate** libraries, so you will need to create these libraries to perform a simulation.

Generate a functional simulation netlist by turning on **Create a simulation library for this design** in the last page of the `alt2gxb` MegaWizard (Figure 4–7).

Figure 4–7. alt2gxb Megawizard



The Quartus II generated `alt2gxb` functional simulation library file references `stratixiigx_hssi wysiwyg` atoms.

Example of Compiling Library Files for Functional Stratix II GX Simulation in Verilog HDL

To compile the libraries necessary to functional simulation of a Verilog HDL design targeting a Stratix II GX device, type the following commands at the NC-Sim command prompt:

```
ncvlog -work lpm 220model.v ↵
ncvlog -work altera_mf altera_mf.v ↵
ncvlog -work sgate sgate.v ↵
ncvlog -work stratixiigx_hssi stratixiigx_hssi_atoms.v ↵
ncvlog -work work <simulation_netlist_alt2gxb>.vo ↵
ncelab work.<my design> ↵
```

Example of Compiling Library Files for Functional Stratix II GX Simulation in VHDL

To compile the libraries necessary to functional simulation of a VHDL design targeting a Stratix II GX device, type the following commands at the NC-Sim command prompt:

```
ncvhdl -work lpm 220pack.vhd 220model.vhd ↵
ncvhdl -work altera_mf altera_mf_components.vhd altera_mf.vhd ↵
ncvhdl -work sgate sgate_pack.vhd sgate.vhd ↵
ncvhdl -work stratixiigx_hssi stratixiigx_hssi_components.vhd \
stratixiigx_hssi_atoms.vhd ↵
ncvhdl -work work <simulation_netlist_alt2gxb>.vho ↵
ncelab work.<my design> ↵
```

Stratix II GX Post-Fit (Timing) Simulation

To perform a post-fit timing simulation of your design that includes the `alt2gxb` megafunction, edit your **cds.lib** file so that all the libraries point to the work library and compile `stratixiigx_atoms` and `stratixiigx_hssi_atoms` into the **stratixiigx** and **stratixiigx_hssi** libraries, respectively. When compiling the library files, you can safely ignore the following warning message:

```
"Multiple logical libraries mapped to a single location"
```

For an example of a **cds.lib** file, refer to "Stratix II GX Functional Simulation" on page 4–29.

The **stratixiigx_hssi_atoms** model file references the **lpm** and **sgate** libraries, so you will need to create these libraries to perform a simulation.

Example of Compiling Library Files for Timing Stratix II GX Simulation in Verilog HDL

To compile the libraries necessary to timing simulation of a Verilog HDL design targeting a Stratix II GX device, type the following commands at the NC-Sim command prompt:

```
ncvlog -work lpm 220model.v ↵
ncvlog -work altera_mf altera_mf.v ↵
ncvlog -work sgate sgate.v ↵
ncvlog -work stratixiigx  stratixiigx_atoms.v ↵
ncvlog -work stratixiigx_hssi stratixiigx_hssi_atoms.v ↵
ncelab work.<my design> -TIMESCALE 1ps/1ps -PULSE_R 0 -PULSE_INT_R 0 ↵
```

Example of Compiling Library Files for Timing Stratix II GX Simulation in VHDL

To compile the libraries necessary to timing simulation of a VHDL design targeting a Stratix II GX device, type the following commands at the NC-Sim command prompt:

```
ncvhdl -work lpm 220pack.vhd 220model.vhd ↵
ncvhdl -work altera_mf altera_mf_components.vhd altera_mf.vhd ↵
ncvhdl -work sgate sgate_pack.vhd sgate.vhd ↵
ncvhdl -work stratixiigx stratixiigx_atoms.vhd \
stratixiigx_components.vhd ↵
ncvhdl -work stratixiigx_hssi stratixiigx_hssi_components.vhd \
stratixiigx_hssi_atoms.vhd ↵
ncvhdl -work work <alt2gxb>.vho ↵
ncelab work.<my design> -TIMESCALE 1ps/1ps -PULSE_R 0 -PULSE_INT_R 0 ↵
```

Pulse Reject Delays

By default, the NCSim software filters out all pulses that are shorter than the propagation delay between primitives. Setting the pulse reject delays (similar to transport delays) options in the NC-Sim software prevents the simulation tool from filtering out these pulses. Use the following options to ensure that all signal pulses are seen in the simulation results.

-PULSE_R

Use this option when the pulses in your simulation are shorter than the delay within a gate-level primitive. The argument is the percentage of delay for pulse reject limit for the path.

-PULSE_INT_R

Use this option when the pulses in your simulation are shorter than the interconnect delay between gate-level primitives. The argument is the percentage of delay for pulse reject limit for the path.

The following NC-Sim software command describes the command-line syntax to perform a gate-level timing simulation with the device family library:

```
ncelab worklib.<project name>:entity –SDF_CMD_FILE <SDF Command File> \
-TIMESCALE 1ps/1ps -PULSE_R 0 -PULSE_INT_R 0
```

Using the NativeLink Feature with NC-Sim

The NativeLink® feature in the Quartus II software facilitates the seamless transfer of information between the Quartus II software and EDA tools and allows you to run NC-Sim within the Quartus II software.

Setting Up NativeLink

To run NC-Sim automatically from the Quartus II software using the NativeLink feature, you must specify the path to your simulation tool by performing the following steps:

1. On the Tools menu, click **Options**. The **Options** dialog box appears.
2. In the **Category** list, select **EDA Tool Options**. The **EDA Tool Options** page is shown.
3. Double-click the entry under the **Location of executable** column beside the name of your **EDA Tool**, and type or browse to the directory containing the executables of your EDA tool.
4. Click **OK**.

You can also specify the path to the simulator's executables by using the `set_user_option` TCL command:

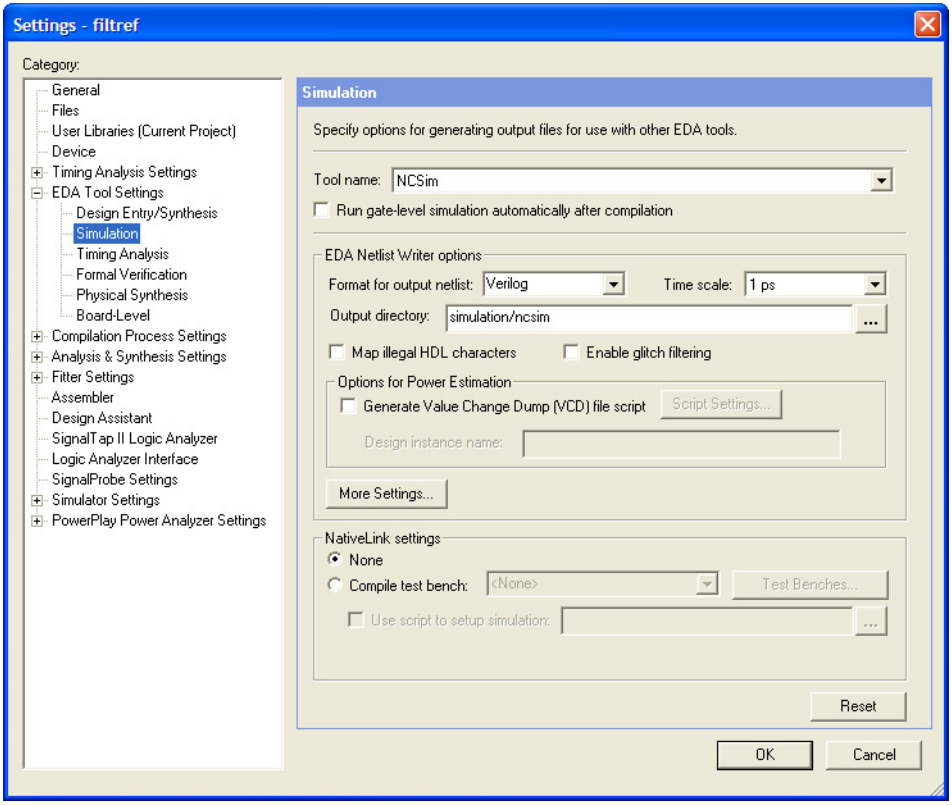
```
set_user_option -name EDA_TOOL_PATH_NCSIM <path to executables>
```

Performing an RTL Simulation Using NativeLink

To run a functional RTL simulation with the NC-Sim software automatically in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page is shown (Figure 4–8).

Figure 4–8. Simulation Page in the Settings Dialog Box



3. In the **Tool name** list, select **NCSim**.

4. If your design is written entirely in Verilog HDL or in VHDL, then the NativeLink feature automatically chooses the correct language and Altera simulation libraries. If your design is written with mixed languages, then the NativeLink feature uses the default language specified in the **Format for output netlist** list. To change the default

language when there is a mixed language design, under **EDA Netlist Writer options**, in the **Format for output netlist** list, select **VHDL** or **Verilog**. Table 4–7 shows the design languages for output netlists and simulation models.

Table 4–7. NativeLink Design Languages

Design File	Format for Output Netlist	Simulation Models Used
Verilog	Any	Verilog
VHDL	Any	VHDL
Mixed	Verilog	Verilog
Mixed	VHDL	VHDL

For mixed language simulation, choose the same language that was used to generate your megafunctions to ensure correct parameter passing between the megafunctions and the Altera libraries. For example, if your `altsyncram` megafunction was generated in VHDL, choose VHDL as the format for output netlist.

For mixed language simulations, it is important to be aware of the following:

- VHDL designs instantiating Verilog user-defined primitives (UDPs) are not supported.
- Parameters cannot be passed in Verilog modules that instantiate VHDL components.

5. If you have test bench files or macro scripts, enter the information under **NativeLink settings**.

For more information on setting up a test bench with NativeLink, refer to the "Setting Up a Test Bench" on page 4–36.

6. Click **OK.**

7. On the Processing menu, point to Start and click **Start Analysis & Elaboration** to perform an analysis and elaboration. This command collects all your file name information and builds your design hierarchy in preparation for simulation.

8. On the Tools menu, point to **EDA Simulation Tool** and click **Run EDA RTL Simulation** to automatically launch NC-Sim, compile all necessary design files, and complete a simulation.

Performing a Gate Level Simulation Using NativeLink

To run a gate-level timing simulation with the NC-Sim software in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page is shown (Figure 4–8).
3. In the **Tool name** list, select **NCSim**.
4. Under **EDA Netlist Writer options**, in the **Format for output netlist** list, choose **VHDL** or **Verilog**. You can also modify where you want the post-synthesis netlist generated by editing or browsing to a directory in the **Output directory** box.
5. To perform a gate level simulation after each full compilation, turn on **Run Gate Level Simulation automatically after compilation**.
6. If you have test bench files or macro scripts, enter the information under **NativeLink settings**.
7. Click **OK**.
8. On the Processing menu, point to Start and click **Start EDA Netlist Writer** to generate a simulation netlist of your design.
9. On the Tools menu, point to EDA Simulation Tool and click **Run EDA Gate Level Simulation** to automatically launch NC-Sim, compile all necessary design files, and complete a simulation.

Setting Up a Test Bench

You can compile your design files and test bench files, and launch EDA simulation tools to perform a simulation automatically using the NativeLink feature.

To setup NativeLink with a test bench, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page is shown.

3. Under **NativeLink settings**, select **None** or **Compile test bench** (Table 4–8).

Table 4–8. NativeLink Settings

Settings	Description
None	Compile simulation models and design files.
Compile test bench	NativeLink compiles simulation models, design files, test bench files, and starts simulation.

4. If you select **Compile test bench**, select your test bench setup from the **Compile test bench** list. You can use different test bench setups to specify different test bench files for different test scenarios. If there are no test bench setups entered, create a test bench setup by performing the following steps:

   a. Click **Test Benches**. The **Test Benches** dialog box appears.

   b. Click **New**. The **New Test Bench Settings** dialog box appears.

   c. In the **Test Bench name** box, type in the test bench setup name which is used to identify between the different test bench setups.

   d. In the **Test bench entity** box, type in the top-level entity name. For example, for a Quartus II generated VHDL test bench, type in `filtref_vhd_vec_tst`.

   e. In the **Instance** box, type in the full instance path to the top level of your FPGA design. For example, for a Quartus II generated VHDL test bench, type in `i1`.

   f. In the **Run for** box, type in how long you want your simulation to run.

   g. Under **Test bench files**, browse and add all your test bench files in the **File name** box. Use the **Up** and **Down** button to reorder your files. The script used by NativeLink compiles the files in the order from top to the bottom.

   h. Click **OK**.

   i. In the Test Benches dialog box, click **OK**.

5. Under **NativeLink settings**, you can turn on **Use script to setup simulation** and browse to your script. You can write a script to setup your waveforms before running the simulation.

The script should be a valid NC-Sim tcl script. NativeLink passes the script to ncsim command with command-line arguments to setup and launch simulation.

Creating a Test Bench

In the Quartus II software you can create a Verilog HDL or VHDL test bench from a Vector Waveform File. The generated test bench includes the behavior of the input stimulus and applies it to your instantiated top-level FPGA design.

1. On the File menu, click **Open**. The **Open** dialog box appears.
2. Click the **Files of type** arrow and select **Waveform/Vector Files**. Select your file.
3. Click **Open**.
4. On the File menu, click **Export**. The **Export** dialog box.
5. Click the **Save as type** arrow and select **VHDL Test Bench File (*.vht)** or **Verilog Test Bench File (*.vt)**.

4. You can turn on **Add self-checking code to file** to check your simulation results against your Vector Waveform File.

5. Click **Export**.

Incorporating PLI Routines

Designers frequently use PLI routines in Verilog HDL test benches to perform user- or design-specific functions that are beyond the scope of the Verilog HDL language. Cadence NC simulators include the PLI wizard, which helps you incorporate your PLI routines.

For example, if you are using the Quartus II software version 5.0 and before, and you are using a Hexadecimal (Intel-Format) File for memory, you can convert it for use with NC tools using the Altera-provided **convert_hex2ver** function. To use this function, you must build it and place it in your project directory using the PLI wizard.

This section describes how to dynamically link, dynamically load, and statically link a PLI library using the **convert_hex2ver** function as an example. The following **convert_hex2ver** source files are located in the *<path to Quartus II installation>*/**eda**/**cadence**/**verilog-xl** directory:

- convert_hex2ver.c
- veriuser.c

Dynamically Link a PLI Library

To create a PLI dynamic library (**.so** or **.sl**), perform the following steps:

1. Run the PLI wizard by typing `pliwiz` at the command prompt.
2. In the **Config Session Name and Directory** page, type the name of the session in the **Config Session Name** box and type the directory in which the file should be built in the **Config Session Directory** box.
3. Click **Next**.
4. In the **Select Simulator/Dynamic Libraries** page, turn on the **Dynamic Libraries Only** option.
5. Click **Next**.
6. In the **Select Components** page, select the **PLI 1.0 Applications** option, and then select **libpli**.
7. Click **Next**.
8. In the **Select PLI 1.0 Application Input** page, select **Existing VERIUSER** (source/object file).
9. Select **Source File** and click **Browse** to locate the **veriuser.c** file provided with the Quartus II software.

The **veriuser.c** file is located in the following directory:

<path to Quartus II installation>/**eda**/**cadence**/**verilog-xl**

10. Click **Next**.
11. In the **PLI 1.0 Application** page, click **Browse** under **PLI Source Files** to locate the **convert_hex2ver.c** file.
12. Click **Next**.
13. In the **Select Compiler** page, choose your **C** compiler from the **Select Compiler list** box.

    gcc is an example of a C compiler. To allow the **PLIWIZ** wizard to find your C compiler, ensure your path variable is set correctly.

14. Click **Next**.
15. Click **Finish**.
16. To build your targets now, click **Yes**.
17. Compilation creates the file **libpli.so** (**libpli.dll** for PCs), which is your PLI dynamic library, in your session directory. When you elaborate your design, the elaborator looks through the path specified in the `LD_LIBRARY_PATH` (UNIX) or `PATH` (PCs) environment variable, searches for the **.so** and **.dll** files, and loads them when needed.

You must modify `LD_LIBRARY_PATH` or `PATH` to include the directory location of your **.so** and **.dll** files.

Dynamically Load a PLI Library

To create a PLI library to be loaded with the NC-Sim software, perform the following steps:

1. Open the **veriuser.c** file located in the following directory:

   <path to Quartus II installation>/**eda**/**cadence**/**verilog-xl**

   The following two examples are sections of the original and modified **veriuser.c** file. The first example is the original **veriuser.c** file packaged with the Quartus II software. The second example is a **veriuser.c** file modified for dynamic loading.

Original veriuser.c File

```
s_tfcell veriusertfs[] =
{
    /*** Template for an entry:
    { usertask|userfunction, data,
      checktf(), sizetf(), calltf(), misctf(),
      "$tfname", forwref?, Vtool?, ErrMsg? },
    Example:
    {usertask, 0, my_check, 0, my_func, my_misctf, "$my_task" },
    ***/
/*** add user entries here ***/
    /* This Handles Binary bit patterns */
    {usertask, 0, 0, 0, convert_hex2ver, 0, "$convert_hex2ver",
1},

        {0} /*** final entry must be 0 ***/
};
```

Modified veriuser.c File

```
p_tfcell my_bootstrap ()
          {

static s_tfcell my_tfs[] =
/*s_tfcell veriusertfs[] = */
{
    /*** Template for an entry:
    { usertask|userfunction, data,
      checktf(), sizetf(), calltf(), misctf(),
      "$tfname", forwref?, Vtool?, ErrMsg? },
    Example:
    { usertask, 0, my_check, 0, my_func, my_misctf, "$my_task" },
    ***/
/*** add user entries here ***/
    /* This Handles Binary bit patterns */
    {usertask, 0, 0, 0, convert_hex2ver, 0, "$convert_hex2ver",
1},

        {0} /*** final entry must be 0 ***/
};
return(my_tfs);
          }
```

2. Run the PLI wizard by typing `pliwiz` at a command prompt, or on the Utilities menu by clicking **PLI Wizard** in the NCLaunch window.

3. In the **Config Session Name and Directory** page, type the name of the session in the **Config Session Name** box and type the directory in which the file should be built in the **Config Session Directory** box.

4. Click **Next**.

5. In the **Select Simulator/Dynamic Libraries** page, select the **Dynamic Libraries Only** option.

6. Click **Next**.

7. In the **Select Components** page, turn on the **PLI 1.0 Applications** option, and select **loadpli1**.

8. Click **Next**.

9. Type a name into the **Bootstrap Function(s)** box.

   For example, type `my_bootstrap` into the **Bootstrap Function(s)** box.

10. Type the name of your generated dynamic library into the **Dynamic Library** box.

    For example, type `convert_dyn_lib` into the **Dynamic Library** box to generate a dynamic library named **convert_dyn_lib.so**.

11. In the **PLI 1.0 Application** page, click **Browse** under **PLI Source Files** to locate the **convert_hex2ver.c** file and the modified **veriuser.c** file.

12. Click **Next**.

13. In the **Select Compiler** page, select your **C** compiler from the **Select Compiler** list box.

    gcc is an example of a C compiler. To allow the **PLIWIZ** wizard to find your C compiler, ensure your Path variable is set correctly.

14. Click **Next**.

15. Click **Finish**.

16. To build your targets now, click **Yes**.

Compilation generates your dynamic library, **cmd_file.nc**, and **cmd_file.xl** files into your local directory. The **cmd_file.nc** and **cmd_file.xl** files contain command line options to use with your newly generated dynamic library file.

- Use the **cmd_file.nc** command file with **ncelab** to perform your simulations as shown in the following example:

```
ncelab worklib.mylpmrom -FILE cmd_file.nc ↵
```

- Use the **cmd_file.xl** command file with **verilog-xl** or **ncverilog** to perform your simulations as shown in the following example:

```
ncverilog -f cmd_file.xl ↵
verilog -f cmd_file.xl ↵
```

Statically Link the PLI Library with NC-Sim

To statically link the PLI library with NC-Sim software, perform the following steps:

1. Run the PLI wizard by typing `pliwiz` at the command prompt or on the Utilities menu by clicking **PLI Wizard** in the NCLaunch window.
2. In the **Config Session Name** and **Directory** page, type the name of the session in the **Config Session Name** box and type the directory in which the file should be built in the **Config Session Directory** box.
3. Click **Next**.
4. Select **NC Simulators** and select **NC-verilog**.
5. Click **Next**.
6. In the **Select Components** page, turn on the **PLI 1.0 Applications option** and select **Static**.
7. In the **Select PLI 1.0 Application Input** page, select **Existing VERIUSER** (source/object file).

8. Select **Source File** and click **Browse** to locate the **veriuser.c** file provided with the Quartus II software.

   The **veriuser.c** file is found in the following location:

   <path to Quartus II installation>/**eda**/**cadence**/**verilog-xl**

9. Click **Next**.

10. In the **PLI 1.0 Application** page, click **Browse** under **PLI Source Files** to locate the **convert_hex2ver.c** file.

11. Click **Next**.

12. In the **Select Compiler** page, select your **C** compiler from the **Select Compiler** list box.

    gcc is an example of a C compiler. To allow the **PLIWIZ** to find your C compiler, ensure your Path variable is set correctly.

13. Click **Next**.

14. Click **Finish**.

15. To build your targets now, click **Yes**.

Compilation generates **ncelab** and **ncsim** executables into your local directory. These executables replace the original **ncelab** and **ncsim** executables.

ncverilog users can use the following command to perform simulation with the newly generated **ncelab** and **ncsim** executables.

```
ncverilog +ncelabexe+<path to ncelab> +ncsimexe+<path to ncelab> <design files> ↵
```

The following example shows how an **ncverilog** users can perform a simulation with the newly generated **ncelab** and **ncsim** executables:

```
ncverilog +ncelabexe+./ncelab +ncsimexe+./ncsim my_ram.vt my_ram.v -v altera_mf.v ↵
```

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp
```

The *Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Generate NC-Sim Simulation Output Files

You can generate Verilog Output File and Standard Delay Format Output File simulation output files with Tcl commands or at a command prompt.

For more information about generating Verilog Output File simulation output files and Standard Delay Format Output File simulation output files, refer to "Quartus II Simulation Output Files" on page 4–20.

Tcl Commands:

The following three assignments cause a Verilog HDL netlist to be written out when you run the Quartus II netlist writer. The netlist has a 1 ps timing resolution for the NC-Sim Simulation software.

```
set_global_assignment -name EDA_OUTPUT_DATA_FORMAT VERILOG -section_id eda_simulation
set_global_assignment -name EDA_TIME_SCALE "1 ps" -section_id eda_simulation
set_global_assignment -name EDA_SIMULATION_TOOL "NC-Verilog (Verilog)"
```

Use the following Tcl command to run the Quartus II netlist writer:

```
execute_module -tool eda ↵
```

Command Prompt

Use the following command to generate a simulation output file for the Cadence NC-Sim software simulator. Specify Verilog HDL or VHDL for the format.

```
quartus_eda <project name> --simulation --format=<verilog|vhdl> --tool=ncsim ↵
```

Conclusion

The Cadence NC family of simulators work within an Altera FPGA design flow to perform functional/RTL, post-synthesis and gate-level timing simulation easily and accurately.

Altera provides functional models of LPM and Altera-specific megafunctions that you can compile with your test bench or design. For timing simulation, use the atom netlist file generated by Quartus II compilation.

The seamless integration of the Quartus II software and Cadence NC tools make this simulation flow an ideal method for fully verifying an FPGA design.

References

For more information, refer to the following sources:

- Cadence NC-Verilog Simulator Help
- Cadence NC-VHDL Simulator Help
- *Cadence NC Launch User Guide*

5. Simulating Altera IP in Third-Party Simulation Tools

QII53014-6.0.0

Introduction

The capacity and complexity of Altera® FPGAs continues to increase and the need for intellectual property (IP) becomes increasingly critical. Using IP megafunctions reduces the design and verification time, allowing you to focus on design customization. Altera and the Altera Megafunction Partners Program (AMPP^{SM}) offer a broad portfolio of IP megafunctions optimized for Altera FPGAs. Through parameterization, these reusable blocks of IP can be customized to meet your design requirements.

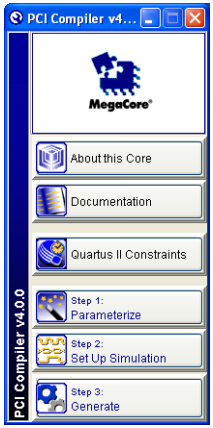
Even when the IP source code is encrypted or otherwise restricted, Altera's unique IP Toolbench allows you to easily simulate designs that contain Altera IP. With the IP Toolbench, you can custom configure IP designs, then generate a VHDL or Verilog HDL functional simulation model for use in your choice of simulation tools.

This chapter provides you with an overview of the process for generating an IP functional simulation model in IP Toolbench and simulating this model in an Altera-supported, third-party simulation tool.

Generating an IP Functional Simulation Model with IP Toolbench

IP megafunctions deployed with IP Toolbench allow you to quickly and easily view documentation, specify parameters, set up third-party tools, and generate all of the necessary files for integrating the parameterized IP megafunction in your design. You can launch the IP Toolbench from within the Quartus® II software via the MegaWizard® Plug-In Manager (Figure 5–1).

Figure 5–1. IP Toolbench GUI



The IP Toolbench graphical user interface (GUI) may appear differently depending on the IP megafunction you are using, or whether you select an IP megafunction from the MegaWizard Plug-In Manager or SOPC Builder. IP Toolbench GUIs from SOPC Builder do not include buttons for setting up simulation or generation, because those functions are performed by SOPC Builder when the entire system is generated. This section describes the procedure for using an IP Toolbench-supported IP megafunction chosen in the MegaWizard Plug-In Manager.

IP Toolbench, in conjunction with the Quartus II software, generates a Verilog Output File (**.vo**) or VHDL Output File (**.vho**) IP functional simulation model after you parameterize your megafunction. These high-level output files differ from the low-level Verilog Output File and VHDL Output File models generated by the Quartus II software for post-synthesis or post place-and-route simulations.

Low-Level Verilog Output File or VHDL Output File Simulation Models

The low-level Verilog Output File or VHDL Output File simulation model files (generated after synthesis or place-and-route) are mapped to atoms. An atom is a parameterized, device-family-dependent representation of a WYSIWYG primitive that corresponds to a device feature such as a logic element (LE), an I/O element (IOE), or memory. Altera-supported simulators include libraries of atoms for each device family. The Verilog

Output File or VHDL Output File models generated for post-synthesis or post place-and-route simulation are placed in the simulation folder under the Quartus II project folder.

High-Level Verilog Output File or VHDL Output File Simulation Models

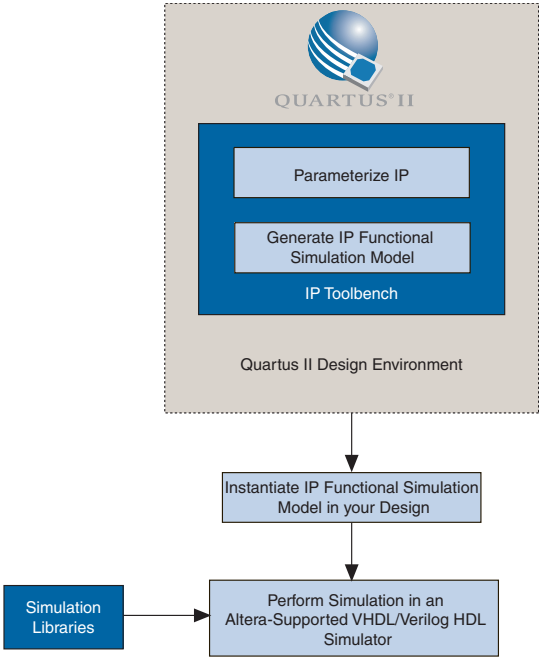
The IP functional simulation models generated through IP Toolbench are mapped to higher-level primitives such as adders, multipliers, and multiplexers. This higher level of abstraction results in much faster simulation times. Depending on the megafunction, the IP functional simulation model is up to 100 times faster than a Quartus II post-synthesis or post place-and-route simulation. The Verilog Output File or VHDL Output File models that are generated for IP functional simulation purposes are output to the directory that you specify in IP Toolbench (typically, the same folder as your Quartus II project). These simulation models can be used in your Altera-supported simulator along with other models and HDL source code.

You can use the IP functional simulation model only for simulation purposes, and not for synthesis or any other purpose. Attempting to synthesize the IP functional simulation model in the Quartus II software results in a non-functional design.

Generating an IP functional simulation model for Altera MegaCore® functions does not require a license. However, generating an IP functional simulation model for AMPP megafunctions may require a license. For more information, contact the IP megafunction vendor.

Figure 5–2 outlines the process of generating an IP functional simulation model and simulating your design in an Altera-supported VHDL or Verilog HDL simulator.

Figure 5–2. IP Functional Simulation Model Design Flow



Launch IP Toolbench

Launch IP Toolbench in the Quartus II software by performing the following steps:

1. On the Tools menu, click **MegaWizardPlug-In Manager**. The **MegaWizard Plug-In Manager** dialog box is shown.

   For more information on using the MegaWizard Plug-In Manager, refer to the Quartus II Help.

2. Select **Create a new custom megafunction variation** and click **Next**.

3. Select the megafunction you would like to create.

4. Select the output file type for your design, and specify the name and location of the file to be generated.

5. Click **Next** to launch IP Toolbench for the megafunction you have selected.

Step 1: Parameterize

Create a custom variation of the megafunction by performing the following steps:

1. In the IP Toolbench, click **Step 1: Parameterize** (Figure 5–3).

Figure 5–3. Step 1: Parameterize

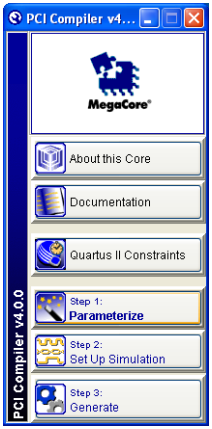


Figure 5–3 shows the IP Toolbench for the PCI Compiler, v4.0.0. The number of buttons in the IP Toolbench—and their names—may vary depending on the megafunction.

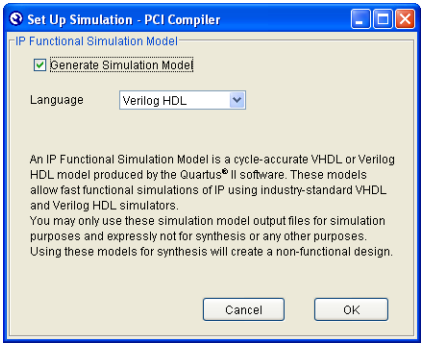
Step 2: Set Up Simulation

After the megafunction variation is parameterized, click the **Step 2: Set Up Simulation** button in IP Toolbench (Figure 5–4).

Figure 5–4. Step 2: Set Up Simulation

2. Turn on **Generate Simulation Model** (Figure 5–5).

Figure 5–5. Set Up Simulation Dialog Box



3. In the **Language** list, select the language.

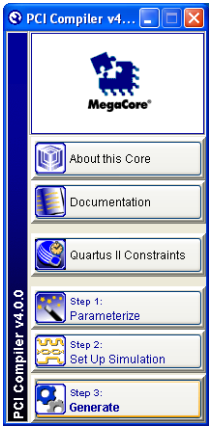
4. Click **Ok**.

Step 3: Generate

Generate your megafunction by performing the following steps:

1. Click **Step 3: Generate** to generate the custom megafunction variation and the IP functional simulation model (Figure 5–6).

Figure 5–6. Generate



When you click **Step 3: Generate**, IP Toolbench creates several new design files in the directory specified in the MegaWizard Plug-In Manager (Table 5–1). The files vary based on the HDL language selected for your custom megafunction and IP functional simulation model. IP Toolbench may generate additional files for other purposes, depending on the IP megafunction you are using.

Table 5–1. IP Toolbench-Generated Files (Part 1 of 2)

Extension	Description
.vhd or **.v**	A megafunction variation file, which defines a Verilog HDL or VHDL top-level description of the custom megafunction. Instantiate the entity defined by this file inside of your design. Include this file when compiling your design in the Quartus II software.
.cmp	A VHDL component declaration file for the megafunction variation. Add the contents of this file to any VHDL architecture that instantiates the megafunction.
.inc	An AHDL include declaration file for the megafunction variation. Include this file with any AHDL architecture that instantiates the megafunction.
_bb.v	A Verilog HDL black-box file for the megafunction variation. Use this file when using a third-party EDA tool to synthesize your design.

Table 5–1. IP Toolbench-Generated Files (Part 2 of 2)

Extension	Description
.bsf	A Quartus II symbol file for the megafunction variation. You can use this file in the Quartus II block diagram editor.
.html	A megafunction report file.
.vo or **.vho**	A VHDL or Verilog HDL IP functional simulation model.
_inst.vhd or **_inst.v**	A VHDL or Verilog HDL sample instantiation file.

Step 4: Instantiate the IP Functional Simulation Model in Your Design

When using the IP functional simulation model to simulate your design, you do not have to make any changes to your original design files. The only difference is which files you add to the simulation and synthesis projects. To perform the IP functional simulation, add the IP functional simulation model Verilog Output File or VHDL Output File to your simulation project.

To synthesize your design using the Quartus II software, add the IP Toolbench-generated Verilog HDL or VHDL custom variation file to your Quartus II project.

To synthesize your design using a third-party EDA tool, add the IP Toolbench-generated CMP file (<*megafunction variation*>**.cmp**) for your VHDL design or the Verilog HDL black-box file (<*megafunction variation*>**_bb.v**) for your Verilog HDL design to your third-party synthesis project.

Step 5: Perform Simulation

The IP functional simulation model that is generated by IP Toolbench instantiates high-level primitives such as adders, multipliers, and multiplexers, as well as the library of parameterized modules (LPM) functions and Altera megafunctions.

To properly compile, load, and simulate the IP functional simulation model generated by the Quartus II software, you must first compile the following libraries in your simulation tool:

- **sgate** includes the definition of the high-level primitives.
- **altera_mf** includes the definition of Altera megafunctions.
- **220model** includes the definition of LPM functions.

You can use these library files with any Altera-supported simulation tool. If you are using the ModelSim® Altera software, the libraries are already compiled and mapped; thus, you do not need to compile them.

To simulate a design containing a Nios® processor or Avalon™ peripherals, refer to *AN 189 Simulating Nios Embedded Processor Designs*.

Figure 5–7 shows library use in IP functional simulation.

Figure 5–7. IP Functional Simulation Library Usage

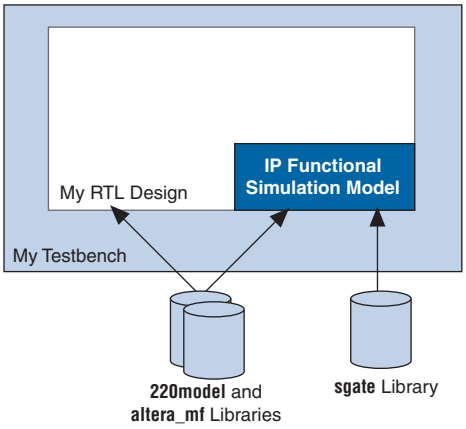


Table 5–2 lists the simulation library files, where <*path*> is the directory where the Quartus II software is installed.

Table 5–2. Simulation Library Files (Part 1 of 2)

Location	HDL Language	Description
<*path*>**/eda/sim_lib/sgate.v**	Verilog HDL	Libraries that contain simulation models for IP functional models
<*path*>**/eda/sim_lib/sgate.vhd**	VHDL	
<*path*>**/eda/sim_lib/sgate_pack.vhd**	VHDL	Libraries that contain VHDL component declarations for the **sgate.vhd** library
<*path*>**/eda/sim_lib/220model.v**	Verilog HDL	Libraries that contain simulation models for the Altera LPM version 2.2.0
<*path*>**/eda/sim_lib/220model.vhd**	VHDL	
<*path*>**/eda/sim_lib/220pack.vhd**	VHDL	Libraries that contain VHDL component declarations for the **220model.vhd** library

Table 5–2. Simulation Library Files (Part 2 of 2)

Location	HDL Language	Description
<*path*>**/eda/sim_lib/altera_mf.v**	Verilog HDL	Libraries that contain simulation models for Altera-specific megafunctions
<*path*>**/eda/sim_lib/altera_mf.vhd**	VHDL	
<*path*>**/eda/sim_lib/altera_mf_components.vhd**	VHDL	Libraries that contains VHDL component declarations for the **altera_mf.vhd** library

Design Language Examples

This section provides the following design language examples:

- ModelSim Verilog
- ModelSim VHDL
- NC-VHDL
- VCS

Verilog HDL Example: Simulating the IP Functional Simulation Model in the ModelSim Software

The following example shows the process of simulating a Verilog HDL-based megafunction. The example assumes that the megafunction variation and the IP functional simulation model are generated.

1. Create a ModelSim project by performing the following steps:
   a. In the ModelSim software, on the File menu, point to New and click **Project**. The **Create Project** dialog box is shown.
   b. Specify the name of your simulation project.
   c. Specify the desired location for your simulation project.
   d. Specify the default library name and click **OK**.
   e. Add relevant files to your simulation project:
      - Your design files.
      - The IP functional simulation model generated by IP Toolbench (If you are using the ModelSim-Altera software, skip to step 5).
      - The **sgate.v**, **220model.v**, and **altera_mf.v** library files.

2. Create the required simulation libraries by typing the following commands at the ModelSim prompt:

   ```
   vlib sgate ↵

   vlib lpm ↵

   vlib altera_mf ↵
   ```

3. Map to the required simulation libraries by typing the following commands at the ModelSim prompt:

   ```
   vmap sgate sgate ↵

   vmap lpm lpm ↵

   vmap altera_mf altera_mf ↵
   ```

4. Compile the HDL into libraries by typing the following commands at the ModelSim prompt:

   ```
   vlog -work altera_mf altera_mf.v ↵

   vlog -work sgate sgate.v ↵

   vlog -work lpm 220model.v ↵
   ```

5. Compile the IP functional simulation model by typing the following command at the ModelSim prompt:

   vlog -work work <*my_IPtoolbench_output_netlist*>.vo ↵

6. Compile your RTL by typing the following command at the ModelSim prompt:

   vlog -work work <*my_design*>.v ↵

7. Compile the test bench by typing the following command at the ModelSim prompt:

   vlog -work work <*my_testbench*>.v ↵

8. Load the test bench by typing the following command at the Modelsim prompt:

   vsim -L <*altera_mf library path*> -L <*lpm library path*> -L <*sgate library path*> work.<*my_testbench*> ↵

VHDL Example: Simulating the IP Functional Simulation Model in the ModelSim Software

The following example shows the process of performing a functional simulation of a VHDL-based, megafunction IP functional simulation model. The example assumes that the megafunction variation and the IP functional simulation model are generated.

1. Create a ModelSim project by performing the following steps:
   a. In the ModelSim software, on the File menu, point to new and click **Project**. The **Create Project** dialog box is shown.
   b. Specify the name for your simulation project.
   c. Specify the desired location for your simulation project.
   d. Specify the default library name and click **OK**.
   e. Add the relevant files to your simulation project:
      - Add your design files.
      - Add the IP functional simulation model generated by IP Toolbench (If you are using the ModelSim-Altera software, skip to step 5).
      - Add the **sgate.vhd**, **sgate.vhd**, **sgate_pack.vhd**, **220model.vhd**, **220pack.vhd**, **altera_mf.vhd**, and **altera_mf_components.vhd** library files.
2. Create the required simulation libraries by typing the following commands at the ModelSim prompt:

```
vlib sgate ↵

vlib lpm ↵

vlib altera_mf ↵
```

3. Map to the required simulation libraries by typing the following commands at the ModelSim prompt:

```
vmap sgate sgate ↵

vmap lpm lpm ↵

vmap altera_mf altera_mf ↵
```

4. Compile the HDL into libraries by typing the following commands at the ModelSim prompt:

```
vcom -work altera_mf -93 -explicit
altera_mf_components.vhd ↵

vcom -work altera_mf -93 -explicit altera_mf.vhd ↵

vcom -work lpm -93 -explicit 220pack.vhd ↵

vcom -work lpm -93 -explicit 220model.vhd ↵

vcom -work sgate -93 -explicit sgate_pack.vhd ↵

vcom -work sgate -93 -explicit sgate.vhd ↵
```

5. Compile the IP functional simulation model by typing the following command at the ModelSim prompt:

```
vcom -work work -93 -explicit <output netlist>.vho ↵
```

6. Compile the RTL by typing the following command at the ModelSim prompt:

```
vcom -work work -93 -explicit <RTL>.vhd ↵
```

7. Compile the test bench by typing the following command at the ModelSim prompt:

```
vcom -work work -93 -explicit <my testbench>.vhd ↵
```

8. Load the test bench by typing the following command at the ModelSim prompt:

```
vsim work.my_testbench ↵
```

NC-VHDL Example: Simulating the IP Functional Simulation Model in the NC-VHDL Software

The following example shows the process of performing a functional simulation of an NC-VHDL-based, megafunction IP functional-simulation model. The example assumes that the megafunction variation and the IP functional simulation model are generated.

1. Create a **cds.lib** file by typing the following entries:

```
DEFINE worklib ./worklib

DEFINE sgate ./sgate

DEFINE altera_mf ./altera_mf

DEFINE lpm ./lpm
```

2. Compile library files into appropriate libraries by typing the following commands at the command prompt:

```
ncvhdl –V93 –WORK lpm 220pack.vhd ↵

ncvhdl –V93 –WORK lpm 220model.vhd ↵

ncvhdl –V93 –WORK altera_mf
altera_mf_components.vhd ↵

rncvhdl –V93 –WORK altera_mf altera_mf.vhd ↵

ncvhdl –V93 –WORK sgate sgate_pack.vhd ↵

ncvhdl –V93 –WORK sgate sgate.vhd ↵
```

3. Compile source code and test bench files by typing the following commands at the command prompt:

```
ncvhdl –V93 –WORK worklib <my_design>.vhd ↵

ncvhdl –V93 –WORK worklib <my_testbench>.vhd ↵

ncvhdl –V93 –WORK worklib
<my_IPtoolbench_output_netlist>.vho ↵
```

4. Elaborate the design by typing the following command at the command prompt:

```
ncelab worklib.<my_testbench>:entity ↵
```

Verilog HDL Example: Simulating Your IP Functional Simulation Model in VCS

The following example illustrates the process of performing a functional simulation of a design that contains a Verilog HDL-based, megafunction IP functional simulation model. This example assumes that the megafunction variation and the IP functional simulation model are generated.

Single Step Process

For the single-step process, type the following at a command prompt:

```
vcs <testbench>.v <RTL>.v <output netlist>.v -v 220model.v
altera_mf.v sgate.v -R ↵
```

Two-Step Process (Compilation & Simulation)

For compilation and simulation, perform the following steps:

1. Compile your design files by typing the following at a command prompt:

```
vcs <testbench>.v <RTL>.v <output netlist>.v -v 220model.v
altera_mf.v sgate.v -o simulation_out ↵
```

2. Load your simulation by typing the following at a command prompt:

```
source simulation_out ↵
```

For more information on simulating a design in VCS, refer to the *Synopsys VCS Support* chapter in volume 3 of the *Quartus II Handbook*.

Conclusion

Using the Quartus II software and IP Toolbench, you can generate IP functional simulation models that enable you to efficiently simulate your design. The high level of abstraction of the IP functional simulation model—relative to post-synthesis or post place-and-route netlists—results in fast behavioral simulations of megafunctions. Using an IP functional simulation model is also transparent, requiring only adding different files to synthesis and simulation projects. These features enhance and simplify design verification.

Section II. Timing Analysis

As designs become more complex, the need for advanced timing analysis capability grows. Static timing analysis is a method of analyzing, debugging, and validating the timing performance of a design. The Quartus® II software provides the features necessary to perform advanced timing analysis for today's system-on-a-programmable-chip (SOPC) designs.

Synopsys PrimeTime is an industry standard sign-off tool, used to perform static timing analysis on most ASIC designs. The Quartus II software provides a path to enable you to run PrimeTime on your Quartus II software designs, and export a netlist, timing constraints, and libraries to the PrimeTime environment.

This section explains the basic principles of static timing analysis, the advanced features supported by the Quartus II Timing Analyzer, and how you can run PrimeTime on your Quartus designs.

This section includes the following chapters:

Revision History

The chapter *Simulating Altera IP in Third-Party Simulation Tools* was moved to *Section I. Simulation*, volume 3 of the *Quartus II Handbook*.

The table below shows the revision history for Chapters 6, 7, 8, and 9.

Chapter(s)	Date / Version	Changes Made
6	July 2006 v6.0.1	Updated for the Quartus II software version 6.0.1: • Fixed typo in report_clock_transfers command on page 6-15.
	May 2006 v6.0.0	Initial release.
7	July 2006 v6.0.1	Updated for the Quartus II software version 6.0.1: • Added section on Clock Objects on page 7-24. • Added examples of Netlist Names on page 7-29. • Replaced figure 7-23 and example 7-9 on page 7-36. • Added note 4 to table 7-6 on page 7-43. • Added "Display Entity Name" to table 7-11 on page 7-57. • Added information to Clock Conversion on pages 7-58 and 7-59. • Added note 3 to table 7-12 on page 7-60. • Added information to Clocks section on page 7-67. • Added Path Details and Unconstrained Paths sections on page 7-68. • Added information to Clock Network Delay Reporting on page 7-72. • Added hand paragraph in Conversion Utility section on page 7-73. • Changed "constraint" to "exception" in many places.
	May 2006 v6.0.0	Initial release.
8	May 2006 v6.0.0	Chapter title changed to *Classic Timing Analyzer*. Updated for the Quartus II software version 6.0.0: • Updated GUI information.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	Autust 2005 V5.0.1	Document revision 1.0.
	May 2005 V5.0.0	New functionality for Quartus II software 5.0
	Jan. 2005 v2.2	Updated information pertaining to realistic, optimistic, and pessimistic settings
	Dec. 2004 v2.1	• Chapter 5 was formerly Chapter 4. • Updates to tables and figures. • New functionality for Quartus II software 4.2.
	June 2004 v2.0	• Updates to tables and figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.
9	May 2006 v6.0.0	Chapter title changed to *Synopsys PrimeTime Support*. Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	August 2005 v5.0.1	Minor text updates.
	May 2005 v5.0.0	New functionality for Quartus II software 5.0.0
	Dec. 2004 v2.0	• Chapter 6 Synopsys PrimeTime moved to section III Volume 1. • New functionality for Quartus II software 4.2.

6. TimeQuest Timing Analyzer

QII53018-6.0.1

Introduction

The TimeQuest Timing Analyzer is a powerful ASIC-style timing analysis tool that validates the timing performance of all logic in your design using an industry-standard constraint, analysis, and reporting methodology. You can use the TimeQuest analyzer's GUI or command-line interface to constrain, analyze, and report results for all timing paths in your design.

Before running the TimeQuest analyzer, you must specify initial timing constraints that describe the clock characteristics, timing exceptions, and signal transition arrival and required times. You can specify timing constraints in the Synopsys Design Constraints (SDC) file format using the GUI or command-line interface. The Quartus® II Fitter optimizes the placement of logic to meet your constraints.

During timing analysis, the TimeQuest analyzer analyzes the timing paths in the design, calculates the propagation delay along each path, checks for timing constraint violations, and reports timing results as slack in the **Report** pane and in the **Console** pane. If the TimeQuest analyzer reports any timing violations, you can customize the reporting to view precise timing information about specific paths, and then constrain those paths to correct the violations. When your design is free of timing violations, you can be confident that the logic will operate as intended in the target device.

The TimeQuest Timing Analyzer is a complete static timing analysis tool that you can use as a sign-off tool for Altera® FPGAs and structured ASICs.

Setting Up the TimeQuest Timing Analyzer

The default timing analyzer in the Quartus II software is the Classic Timing Analyzer. Alternatively, you can specify the TimeQuest analyzer as the default timing analysis tool. When you specify the TimeQuest analyzer as the default timing analyzer, the TimeQuest analyzer guides the Fitter and analyzes timing results after compilation.

To specify the TimeQuest analyzer as the default timing analyzer, on the Assignments menu, click **Settings**. In the **Settings** dialog box, in the **Category** list, expand **Compilation Process Settings**, select **Timing Analysis Processing**, and turn on **Use TimeQuest Timing Analyzer during compilation**.

To add the TimeQuest analyzer icon to the Quartus II toolbar, on the Tools menu, click **Customize**. In the **Customize** dialog box, click the **Toolbars** tab and turn on **Processing**, and click **Close**.

Timing Analysis Overview

This section provides an overview of the TimeQuest timing analyzer concepts. Understanding these concepts allows you to take advantage of the powerful timing analysis features available in the TimeQuest analyzer.

The TimeQuest analyzer follows the flow shown in Figure 6–1 when it analyzes your design. Figure 6–1 lists some of the available commands for each step.

Figure 6–1. The TimeQuest Analyzer Flow

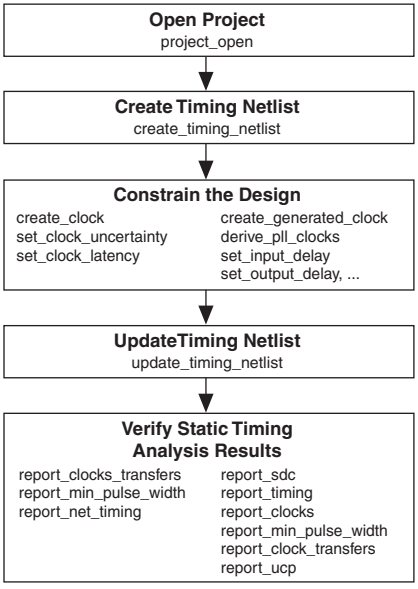


Table 6–1 describes the TimeQuest analyzer terminology.

Table 6–1. The TimeQuest Analyzer Terms

Terminology	Definition
Nodes	Most basic timing netlist unit. Use to represent ports, pins, registers, and keepers.
Keepers	Ports or registers. *(1)*
Cells	Look-up table (LUT), registers, DSP blocks, TriMatrix® memory, IOE, and so on. *(2)*
Pins	Inputs or outputs of cells.
Nets	Connections between pins.
Ports	Top-level module inputs or outputs, for example, device pins.
Clocks	Abstract objects outside of the design.

Notes to Table 6–1:

(1) Pins can indirectly refer to keepers. For example, when the value in the `-from` field of a constraint is a clock pin to a dedicated memory. In this case, the clock pin refers to a collection of registers.

(2) For Stratix® devices and other early device families, the LUT and registers are contained in logic elements (LE) and act as cells for these device families.

The TimeQuest analyzer requires a timing netlist before it can perform a timing analysis on any design. For example, for the design shown in Figure 6–2, the TimeQuest analyzer generates a netlist equivalent to the one shown in Figure 6–3.

Figure 6–2. Sample Design

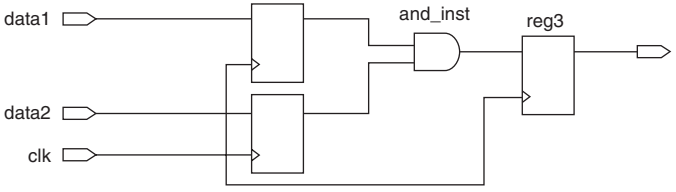


Figure 6–3. The TimeQuest Analyzer Timing Netlist

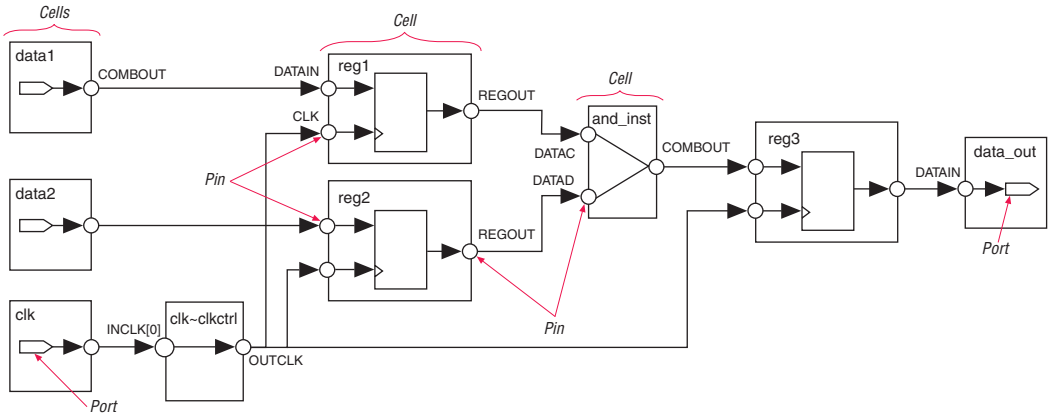


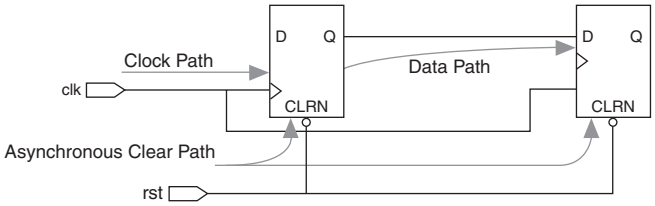
Figure 6–3 shows various cells, pins, nets, and ports. Sample cell names are `reg1`, `reg2`, and `and_inst`; sample pins are `data1|combout`, `reg1|regout`, and `and_inst|combout`; sample net names are `data1~combout`, `reg1`, and `and_inst`; and sample port names are `data1`, `clk`, and `data_out`.

Paths connect two design nodes, such as the output of a register to the input of another register. Timing paths play a significant role in timing analysis. Understanding the types of timing paths is important to timing closure and optimization. The following list shows some of the commonly analyzed paths that are described in this section:

- **Edges**—the connections from ports-to-pins, from pins-to-pins, and from pins-to-ports.
- **Clock paths**—the edges from device ports or internally generated clock pins to the clock pin of a register.
- **Data paths**—the edges from a port or the data output pin of a sequential element to a port or the data input pin of another sequential element.
- **Asynchronous paths**—the edges from a port or sequential element to the asynchronous set or clear pin of a sequential element.

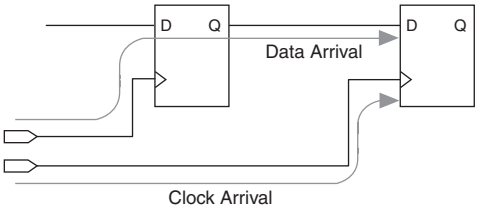
Figure 6–4 shows some of these commonly analyzed path types.

Figure 6–4. Path Types



Once the TimeQuest analyzer identifies the path type, it can report data and clock arrival times for valid register-to-register paths. The TimeQuest analyzer calculates data arrival time by adding the delay from the clock source to the clock pin of the source register, the micro clock-to-out (μt_{CO}) of the source register, and the delay from the source register's *Q* pin to the destination register's *D* pin, where the μt_{CO} is the intrinsic clock-to-out for the internal registers in the FPGA. The TimeQuest analyzer calculates clock arrival time by adding the delay from the clock source to the destination register's clock pin. Figure 6–5 shows a data arrival path and a clock arrival path. The TimeQuest analyzer calculates data required time by accounting for the clock arrival time and the micro setup time (μt_{SU}) of the destination register, where the μt_{SU} is the intrinsic setup for the internal registers in the FPGA.

Figure 6–5. Data Arrival & Clock Arrival

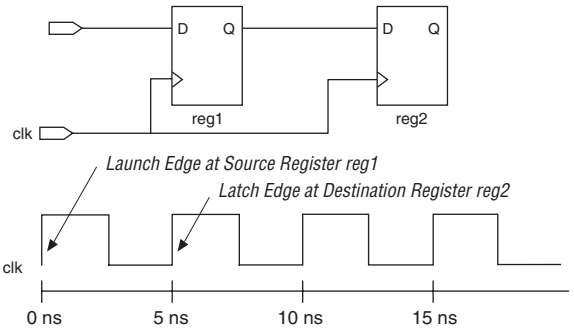


In addition to identifying various paths in a design, the TimeQuest analyzer analyzes clock characteristics to compute the worst-case requirement between any two registers in a single register-to-register path. You should constrain all clocks in your design before performing this analysis.

The launch edge is an active clock edge that sends data out of a sequential element, acting as a source for the data transfer. A latch edge is the active clock edge that captures data at the data port of a sequential element, acting as a destination for the data transfer.

Figure 6–6 shows a single-cycle system that uses consecutive clock edges to transfer and capture data, a register-to-register path, and the corresponding launch and latch edges timing diagram. In this example, the launch edge sends the data out of register `reg1` at 0 ns, and register `reg2` latch edge captures the data at 5 ns.

Figure 6–6. Launch Edge & Latch Edge



The TimeQuest analyzer validates clock setup and hold requirements relative to the launch and latch edges.

Constraints Files

The TimeQuest timing analyzer stores all timing constraints in an SDC file. You can create an SDC file with different constraints for place-and-route and for timing analysis.

The SDC file should contain only SDC and Tcl commands. Commands to manipulate the timing netlist or control the compilation flow should not be included in the SDC file.

The Quartus II software does not automatically update SDC files. You must explicitly write new or updated constraints in the TimeQuest GUI. Use the `write_sdc` command, or, in the TimeQuest analyzer, on the Constraints menu, click **Write SDC File** to write your constraints to an SDC file.

Fitter & Timing Analysis SDC Files

You can specify the same or different SDC files for the Quartus II Fitter for place-and-route, and the TimeQuest analyzer for static timing analysis. Using different SDC files allows you to have one set of constraints for place-and-route, and another set of constraints for final timing sign-off in the TimeQuest analyzer.

Specifying SDC Files for Place-and-Route

To specify an SDC file for the Fitter, you must add the SDC file to your Quartus II project. To add the file to your project, use the following command in the Tcl console:

```
set_global_assignment -name SDC_FILE <SDC file name>
```

Or, in the Quartus II GUI, on the Project menu, click **Add/Remove Files in Project**.

The Fitter optimizes your design based on the requirements in the SDC files in your project.

The results shown in the timing analysis report located in the Compilation Report are based on the SDC files added to the project.

You must specify the TimeQuest analyzer as the default timing analyzer to make the Fitter read the SDC file.

Specifying SDC Files for Static Timing Analysis

After you create a timing netlist in the TimeQuest analyzer, you must specify timing constraints and exceptions before you can perform a timing analysis. The timing requirements do not have to be identical to those provided to the Fitter. You can specify your timing requirements manually or you can read a previously created SDC file.

To manually enter your timing requirements, you can use constraint entry dialog boxes or SDC commands. If you have an SDC file that contains your timing requirements, you can use this file to apply your timing requirements. To specify the SDC file for timing analysis in the TimeQuest analyzer, use the following command:

```
read_sdc [<SDC file name>]
```

If you use the TimeQuest GUI, to apply SDC file for timing analysis, in the TimeQuest analyzer, on the Constraints menu, click **Read SDC File**.

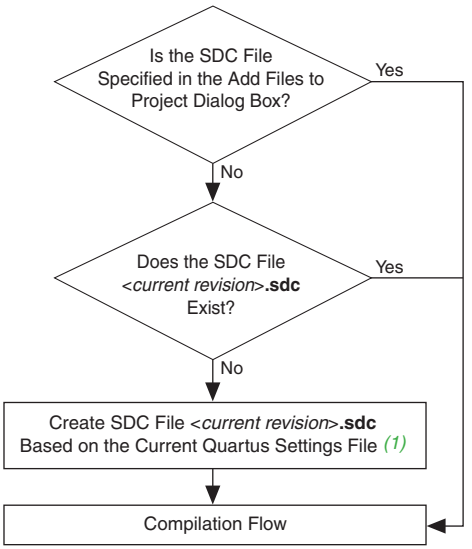
By default, the **Read SDC File** command in the **Tasks** pane reads the SDC files specified in the Quartus II Settings File (**.qsf**) (QSF), which are the same SDC files used by the Fitter.

Synopsys Design Constraints File Precedence

The Quartus II Fitter and the TimeQuest analyzer read the SDC files from the files list in the QSF file in the order they are listed, from top to bottom.

The Quartus II software searches for an SDC file as shown in Figure 6–7.

Figure 6–7. Synopsys Design Constraints File Order of Precedence



Notes for Figure 6–7:
(1) This occurs only in the TimeQuest analyzer, and not during compilation in the Quartus II software.

If you type the `read_sdc` command at the command line without any arguments, precedence order shown in Figure 6–7 is followed.

Launching the TimeQuest Analyzer

You can launch the TimeQuest analyzer in one of the following modes:

- Directly from the Quartus II software
- Stand-alone mode
- Command-line mode

This section explains each of the modes, and the behavior of the TimeQuest analyzer.

Directly from the Quartus II Software

To launch the TimeQuest analyzer from the Quartus II software, on the Tools menu, click **TimeQuest Timing Analyzer**. The TimeQuest analyzer is available after you have created a database for the current project. The database can either be a post-map or post-fit database; perform Analysis & Synthesis to create a post-map database, or a full compilation to create a post-fit database.

After a database is created in the Quartus II software, you can create a timing netlist based on that database. If you create a post-map database, you cannot create a post-fit timing netlist in the TimeQuest analyzer.

When you launch the TimeQuest analyzer directly from the Quartus II software, the current project is automatically opened.

Stand-Alone Mode

To launch the TimeQuest analyzer in stand-alone mode, type the following command at the command prompt:

```
quartus_staw ↵
```

In stand-alone mode, you can perform static analysis on any project that contains either a post-map or post-fit database. To open a project, double-click **Open Project** in the **Tasks** pane.

Command-Line Mode

You can use the command-line mode for easy integration with scripted design flows. Using the command-line mode avoids interaction with the user interface provided by the TimeQuest analyzer, but allows the automation of each step of the static timing analysis flow. Table 6–2 provides a summary of the various options available in the command-line mode.

To launch the TimeQuest analyzer in command-line mode, type the following command at the command prompt:

```
quartus_sta <options> ↵
```

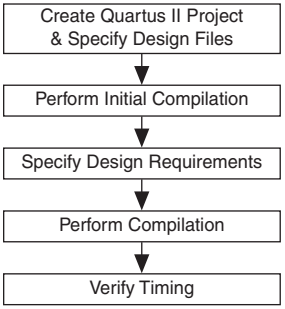
Table 6–2. Summary of Command Line Options

Command Line Option	Description
-h | --help	Provide help information on quartus_sta.
-t <*script file*> | --script=<*script file*>	Sources the <*script file*>.
-s | --shell	Enters shell mode.
--tcl_eval <*tcl command*>	Evaluates the Tcl command <*tcl command*>.
--do_report_timing	Runs the command: report_timing -npaths 1 -to_clock $clock for all clocks in the design.
--force_dat	Forces the Delay Annotator to annotate the new delays from the recently compiled design to the compiler database.
--lower_priority	Lowers the computing priority of the quartus_sta process.
--post_map	Uses the post-map database results.
--qsf2sdc	Converts assignments from the Quartus II Settings File format to the Synopsys Design Constraints File format.
--risefall	Turns on rise/fall support for analysis if the family supports it.
--sdc=<*SDC file*>	Specifies the SDC file to read.

The TimeQuest Analyzer Flow Guidelines

The TimeQuest timing analyzer plays an integral part in the Quartus II compilation flow from the specification of timing constraints to the verification of design requirements. This section describes the compilation flow when you specify the TimeQuest analyzer as the default timing analyzer as shown in Figure 6–8.

Figure 6–8. Design Flow with the TimeQuest Analyzer



Create Quartus II Project & Specify Design Files

You must create a project before you can compile design files. In this step you specify the target FPGA, any EDA tools used in the design cycle, and all design files.

You can also modify existing design files for design optimization and add additional design files. For example, you can add HDL files or schematics to the project.

To add or remove design files from your project, in the Quartus II software, on the Project menu, click **Add/Remove Files in Project**.

For more information on creating projects in the Quartus II software refer to the *Introduction to Quartus II Manual*.

Perform Initial Compilation

You must create an initial design database before you specify timing constraints for your design. Perform Analysis & Synthesis to create a post-map database, or perform a full compile to create a post-fit database.

Creating a Post-Map Database

To perform Analysis & Synthesis, in the Quartus II GUI, on the Processing menu, point to Start, and click **Start Analysis & Synthesis**, or type the following command at the command prompt:

```
quartus_map <project name> ↵
```

Creating a post-map database for the initial compilation is faster than creating a post-fit database, and a post-map database is sufficient for the initial database.

Creating a Post-Fit Database

To compile your design, in the Quartus II GUI, on the Processing menu, click **Start Compilation**, or type the following commands at the command prompt:

```
quartus_map <project name> ↵
quartus_fit <project name> ↵
```

Creating a post-fit database is recommended only if you previously created and specified an SDC file for the project. A post-map database is sufficient for the initial compilation.

Specify Design Timing Requirements

Next, specify timing constraints and exceptions for your design.

Timing requirements guide the Fitter as it places and routes your design. You must enter all timing constraints and exceptions in an SDC file. This file must be included as part of the project. To add this file to your project, on the Project menu, click **Add/Remove Files in Project**, and add the SDC file in the **Files** dialog box.

Refer to "Specify Timing Constraints" on page 6–14 for a list of timing constraints and exceptions.

After you create the initial database, follow these steps to create timing requirements:

1. Launch the TimeQuest analyzer.
2. Create a Timing Netlist.
3. Specify Timing Constraints.
4. Save Timing Constraints.

The following sections describe these steps in detail.

You cannot use the Assignment Editor to specify timing requirements for the TimeQuest analyzer.

Create a Timing Netlist

The TimeQuest analyzer requires a timing netlist before you can specify timing requirements. The TimeQuest analyzer creates a timing netlist based upon the netlist generated in the compilation step. It annotates the timing netlist with either the post-map or post-fit delay results.

You can create a timing netlist in the following ways:

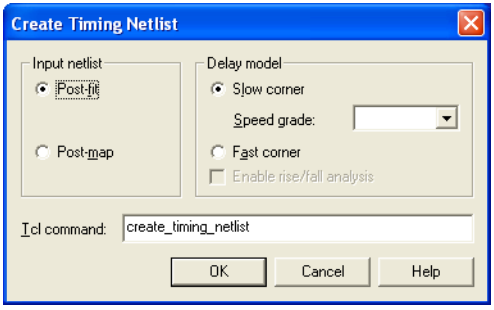
- In the **Tasks** pane, double-click **Create Timing Netlist**.

  By default, the **Create Timing Netlist** command generates a timing netlist based on the post-fit database. An error message displays if the initial database is a post-map database.

  or

- On the Netlist menu, click **Create Timing Netlist**. The Timing Netlist dialog box is shown (Figure 6–9).

Figure 6–9. Create Timing Netlist Dialog Box



In the Create Timing Netlist dialog box, specify the input netlist type and the delay model, and click **OK**.

or

- To create a timing netlist in the **Console** pane, type the following command at a Tcl prompt:

```
create_timing_netlist ↵
```

You can use the `-post_map` option to specify that the timing netlist is based on a post-map database, for example, you can type the following:

```
create_timing_netlist -post_map ↵
```

Specify Timing Constraints

Specify your timing constraints in the Constraints menu. The following constraints are available:

- Create Clock
- Create Generated Clock
- Set Clock Latency
- Set Clock Uncertainty
- Remove Clock
- Set Input Delay
- Set Output Delay
- Set False Path
- Set Multicycle Path
- Set Maximum Delay
- Set Minimum Delay

You can also type constraints and exceptions in the **Console** pane.

For more information on the supported SDC file constraints, refer to "Constraints" on page 6–62.

The specified constraints and exceptions guide the Fitter as it places and routes your design.

Generate SDC Constraint Reports

You can generate initial timing reports to verify that all constraints and exceptions have been entered. Because the constraints and exceptions have not been processed by the Fitter, do not use this step to verify that your timing requirements have been met.

You should verify the following items before continuing:

- All clocks are constrained
- Removal of any invalid clock-to-clock transfers
- All paths are constrained

You can use the **Report Clocks** command in the **Task** pane, or the `report_clocks` command to verify that all clocks have been properly defined and applied to the proper nodes in the design.

You can use the **Report Clock Transfers** command in the **Task** pane, or the `report_clock_transfers` command to verify all clock-to-clock transfers.

You can use the **Report Unconstrained Paths** command in the **Task** pane, or the `report_ucp` command to verify that all paths in the design have been properly constrained.

Save Timing Constraints

To save your constraints in an SDC file, on the Constraints menu, click **Write SDC File**. Enter the SDC file name and click **Save**.

You can also double-click the **Write SDC File** command in the **Task** pane to save your constraints in an SDC file, or you can enter the following command in the **Console** pane:

`write_sdc <file name>` ↵

The TimeQuest analyzer overwrites the entire contents of an SDC file if there is a file name conflict.

Compile the Design

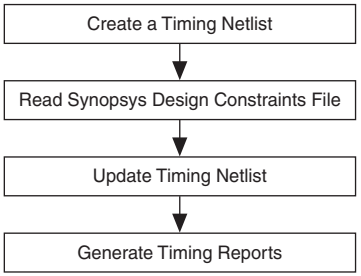
The steps discussed in "Specify Design Timing Requirements" on page 6–12 describe how to create and verify all timing constraints and exceptions in your design. These timing constraints and exceptions guide the Fitter during compilation. The compilation step synthesizes, places, and routes your design into the target FPGA.

When compilation is complete, the TimeQuest analyzer automatically generates summary clock setup and clock hold, recovery, and removal reports for all defined clocks in the design.

Verify Timing

Use the steps shown in Figure 6–10 to verify timing in the TimeQuest analyzer.

Figure 6–10. Timing Verification in the TimeQuest Analyzer



The following sections describe each of the steps shown in Figure 6–10.

Create a Timing Netlist

After you perform a full compilation, you must create a timing netlist based on the fully annotated database from the post-fit results.

To create the timing netlist, double-click **Create Timing Netlist** in the **Task** pane, or enter the following command in the **Console** pane:

```
create_timing_netlist ↵
```

Read the Synopsys Design Constraints File

After you create a timing netlist, you must read an SDC file. This step reads all constraints and exceptions defined in the SDC file.

You can read the SDC file with either the **Task** pane or the **Console** pane.

To read the SDC file from the **Task** pane, double-click the **Read SDC File** command.

The **Read SDC File** task reads the <*current revision*>**.sdc**.

To read the SDC file in the **Console** pane, type the following command in the **Console** pane:

```
read_sdc ↵
```

Update Timing Netlist

You must update the timing netlist after you read an SDC file. The TimeQuest analyzer applies all constraints to the netlist for verification, and removes any invalid or false paths in the design from verification.

To update the timing netlist, double-click **Update Timing Netlist** in the **Tasks** pane, or type the following command in the **Console** pane:

```
update_timing_netlist ↵
```

Generate Timing Reports

You can generate timing reports for any critical paths in your design. Table 6–3 describes the available reports that you can generate directly from the **Tasks** pane, and the equivalent Tcl commands you can enter in the **Console** pane.

Table 6–3. Reports from the Tasks Pane & Tcl Commands

Task Pane Report	Tcl Command	Description
Report Setup Summary	`create_timing_summary -setup`	Generates a clock setup summary for all defined clocks.
Report Hold Summary	`create_timing_summary -hold`	Generates a clock hold summary for all defined clocks.
Report Recovery Summary	`create_timing_summary -recovery`	Generates a clock recovery summary for all defined clocks.
Report Removal Summary	`create_timing_summary -removal`	Generates a clock removal summary for all defined clocks.
Report Clocks	`report_clocks`	Generates a clock summary for all defined clocks.
Report Clock Transfers	`report_clock_transfers`	Generates a clock transfer summary for all clock-to-clock transfers in the design.
Report SDC	`report_sdc`	Generates a summary of all SDC file commands read.
Report Unconstrained Paths	`report_ucp`	Generates a summary of all unconstrained paths in the design.
Report Timing	`report_timing`	Generates a detailed summary for specific paths in the design.
Report Net Timing	`report_net_timing`	Generates a detailed summary for specific nets in the design.
Report Minimum Pulse Width	`report_min_pulse_width`	Generates a detailed summary for specific registers in the design.
Create Slack Histogram	`create_slack_histogram`	Generates a detailed histogram for specific clock in the design.

For a full list of available report APIs, refer to the *SDC & TimeQuest API Reference Manual*.

As you verify timing, you may encounter failures along critical paths. If this occurs, you can refine the existing constraints or create new ones to change the effects of existing constraints. If you modify, remove, or add constraints, you should perform a full compilation. This allows the Fitter to re-optimize the design based upon the new constraints, and brings you back to the Perform Compilation step in the process. This iterative process allows you to resolve your timing violations in the design.

Refer to the *TimeQuest Quick Start Tutorial* for a sample Tcl script to automate the timing analysis flow.

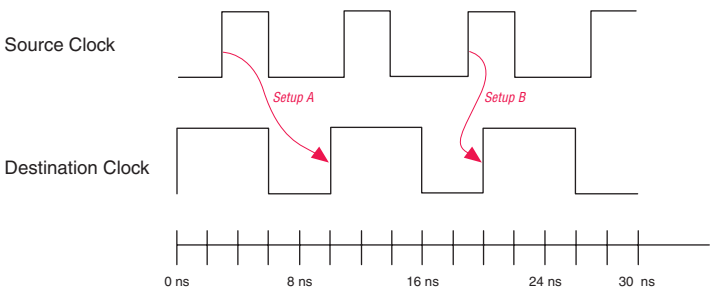
Clock Analysis

A comprehensive static timing analysis includes analysis of register-to-register, I/O, and asynchronous reset paths. The TimeQuest analyzer uses data required times, data arrival times, and clock arrival times to verify circuit performance and to detect possible timing violations. The TimeQuest analyzer determines the timing relationships that must be met for the design to correctly function, and checks arrival times against required times to verify timing.

Clock Setup Check

To perform a clock setup check, the TimeQuest analyzer determines a setup relationship by analyzing each launch and latch edge for each register-to-register path. For each latch edge at the destination register, the TimeQuest analyzer uses the closest previous clock edge at the source register as the launch edge. In Figure 6–11, two setup relationships are defined and are labeled Setup A and Setup B. For the latch edge at 10 ns, the closest clock that acts as a launch edge is at 3 ns and is labeled Setup A. For the latch edge at 20 ns the closest clock that acts as a launch edge is at 19 ns and is labeled Setup B.

Figure 6–11. Setup Check



The TimeQuest analyzer reports the result of clock setup checks as slack values. Slack is the margin by which a timing requirement is met or not met. Positive slack indicates the margin by which a requirement is met, and negative slack indicates the margin by which a requirement is not met. The TimeQuest analyzer determines clock setup slack as shown in Equation 1 for internal register-to-register paths.

(1)

Clock Setup Slack = Data Required Time – Data Arrival Time
Data Required = Clock Arrival Time – μt_{SU} – Setup Uncertainty
Clock Arrival Time = Latch Edge + Clock Network Delay to Destination Register
Data Arrival Time = Launch Edge + Clock Network Delay Source Register + μt_{CO} + Register-to-Register Delay

If the data path is from an input port to a internal register, the TimeQuest analyzer uses the equations shown in Equation 2 to calculate the hold slack time.

(2)

Clock Setup Slack Time = Data Required Time – Data Arrival Time

Data Arrival Time = Launch Edge + Clock Network Delay to Source Register + Input Maximum Delay of Pin + Pin to Register Delay

Data Required Time = Latch Edge + Clock Network Delay to Destination Register – µtsu

If the data path is an internal register to an output port, the TimeQuest analyzer uses the equations shown in Equation 3 to calculate the setup slack time.

(3)

Clock Setup Slack Time = Data Required Time – Data Arrival Time

Data Arrival Time = Launch Edge + Clock Network Delay to Source Register + µtco + Register to Pin Delay

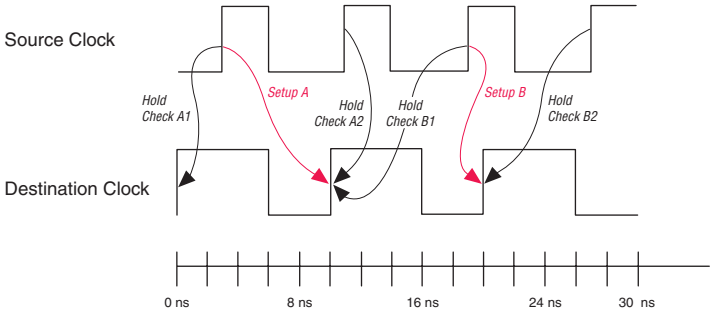
Data Required Time = Latch Edge + Clock Network Delay to Destination Register – Output Maximum Delay of Pin

Clock Hold Check

To perform a clock hold check, the TimeQuest analyzer determines a hold relationship for each possible setup relationship that exists for all source and destination register pairs. The TimeQuest analyzer checks all adjacent clock edges from all setup relationships to determine the hold relationships. The TimeQuest analyzer performs two hold checks for each setup relationship. The first hold check determines that the data launched by the current launch edge is not captured by the previous latch edge. The second hold check determines that the data launched by the next launch

edge is not captured by the current latch edge. Figure 6–12 shows two setup relationships labeled setup A and setup B. The first hold check is labeled hold check A1 and hold check B1 for setup A and setup B, respectively. The second hold check is labeled hold check A2 and hold check B2 for setup A and setup B, respectively.

Figure 6–12. Hold Checks



From the possible hold relationships, the TimeQuest analyzer selects the hold relationship that is the most restrictive. The hold relationship with the largest difference between the latch and launch edges (that is, latch – launch and not the absolute value of latch – launch) is selected because this determines the minimum allowable delay for the register-to-register path. For Figure 6–12, the hold relationship selected is hold check A2.

The TimeQuest analyzer determines clock hold slack as shown in Equation 4.

(4)

$$\begin{aligned}
&\text{Clock Hold Slack} &&= \text{Data Arrival Time} - \text{Data Required Time} \\
&\text{Data Required Time} &&= \text{Clock Arrival Time} + \mu t_H + \text{Hold Uncertainty} \\
&\text{Clock Arrival Time} &&= \text{Latch Edge} + \text{Clock Network Delay to Destination Register} \\
&\text{Data Arrival Time} &&= \text{Launch Edge} + \text{Clock Network Delay to Source Register} + \\
& && \quad \mu t_{CO} + \text{Register to Register Delay}
\end{aligned}$$

If the data path is from an input port to an internal register, the TimeQuest analyzer uses the equations shown in Equation 5 to calculate the setup slack time.

(5)

$$\text{Clock Setup Slack Time} = \text{Data Arrival Time} - \text{Data Required Time}$$

$$\text{Data Arrival Time} = \text{Launch Edge} + \text{Clock Network Delay to Source Register} + \text{Input Minimum Delay of Pin} + \text{Pin to Register Delay}$$

$$\text{Data Required Time} = \text{Latch Edge} + \text{Clock Network Delay to Destination Register} + \mu t_H$$

If the data path is an internal register to an output port, the TimeQuest analyzer uses the equations shown in Equation 6 to calculate the setup slack time.

(6)

$$\text{Clock Setup Slack Time} = \text{Data Arrival Time} - \text{Data Required Time}$$

$$\text{Data Arrival Time} = \text{Launch Edge} + \text{Clock Network Delay to Source Register} + \mu t_{CO} + \text{Register to Pin Delay}$$

$$\text{Data Required Time} = \text{Latch Edge} + \text{Clock Network Delay to Destination Register} - \text{Output Minimum Delay of Pin}$$

Recovery & Removal

Recovery time is the minimum length of time an asynchronous control signal, for example, `clear` and `preset`, must be stable before the next active clock edge. The recovery slack time calculation is similar to the clock setup slack time calculation, but it applies asynchronous control signals. If the asynchronous control is registered, the TimeQuest analyzer uses Equation 7 to calculate the recovery slack time.

(7)

$$\text{Recovery Slack Time} = \text{Data Required Time} - \text{Data Arrival Time}$$
$$\text{Data Arrival Time} = \text{Launch Edge} + \text{Clock Network Delay to Source Register} + \mu t_{CO} + \text{Register to Register Delay}$$
$$\text{Data Required Time} = \text{Latch Edge} + \text{Clock Network Delay to Destination Register} - \mu t_{SU}$$

If the asynchronous control is not registered, the TimeQuest analyzer uses the equations shown in Equation 8 to calculate the recovery slack time.

(8)

$$\text{Recovery Slack Time} = \text{Data Required Time} - \text{Data Arrival Time}$$
$$\text{Data Arrival Time} = \text{Launch Edge} + \text{Maximum Input Delay} + \text{Port to Register Delay}$$
$$\text{Data Required Time} = \text{Latch Edge} + \text{Clock Network Delay to Destination Register Delay} - \mu t_{SU}$$

If the asynchronous reset signal is from a port (device I/O), you must make an Input Maximum Delay assignment to the asynchronous reset pin for the TimeQuest Timing Analyzer to perform recovery analysis on that path.

Removal time is the minimum length of time an asynchronous control signal must be stable after the active clock edge. The TimeQuest analyzer removal time slack calculation is similar to the clock hold slack calculation, but it applies asynchronous control signals. If the asynchronous control is registered, the TimeQuest analyzer uses the equations shown in Equation 9 to calculate the removal slack time.

(9)

$$\begin{aligned}\text{Removal Slack Time} &= \text{Data Arrival Time} - \text{Data Required Time}\\ \text{Data Arrival Time} &= \text{Launch Edge} + \text{Clock Network Delay to Source Register} + \mu t_{CO} \text{ of Source Register} + \text{Register to Register Delay}\\ \text{Data Required Time} &= \text{Latch Edge} + \text{Clock Network Delay to Destination Register} + \mu t_{H}\end{aligned}$$

If the asynchronous control is not registered, the TimeQuest analyzer uses the equations shown in Equation 10 to calculate the removal slack time.

(10)

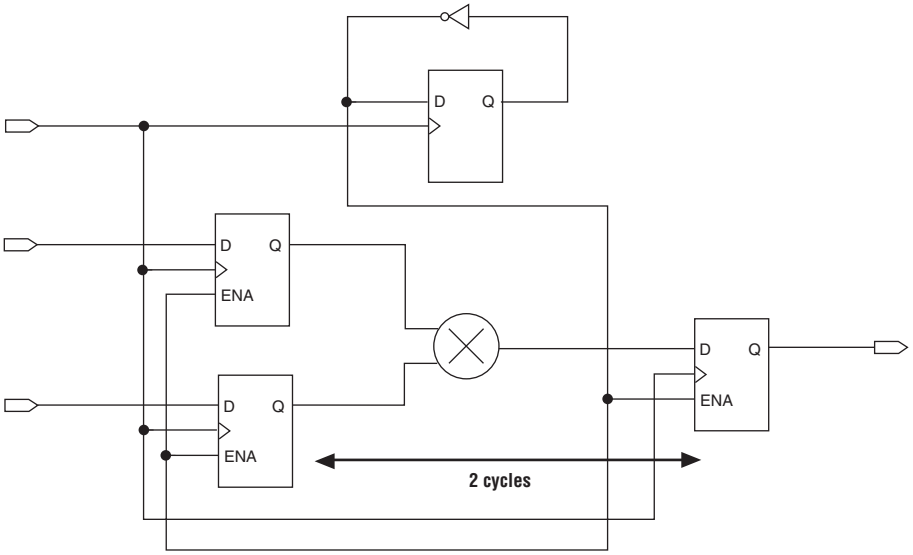
$$\begin{aligned}\text{Removal Slack Time} &= \text{Data Arrival Time} - \text{Data Required Time}\\ \text{Data Arrival Time} &= \text{Launch Edge} + \text{Input Minimum Delay of Pin} + \text{Minimum Pin to Register Delay}\\ \text{Data Required Time} &= \text{Latch Edge} + \text{Clock Network Delay to Destination Register} + \mu t_{H}\end{aligned}$$

If the asynchronous reset signal is from a device pin, you must specify the Input Minimum Delay constraint to the asynchronous reset pin for the TimeQuest analyzer to perform a removal analysis on this path.

Multicycle Paths

Multicycle paths are data paths that require more than one clock cycle to latch data at the destination register. For example, a register may be required to capture data on every second or third rising clock edge. Figure 6–13 shows an example of a multicycle path between a multiplier's input registers and output register where the destination latches data on every other clock edge.

Figure 6–13. Example Diagram of a Multicycle Path



Clock Specification

The specification of all clocks and any associated clock characteristics in your design is essential for accurate static timing analysis results. The TimeQuest analyzer provides many SDC file APIs that accommodate various clocking schemes and any clock characteristics.

This section describes the SDC file API available to create and specify clock characteristics.

Clocks

You can use the `create_clock` command to create a clock at any register, port, or pin. You can create each clock with unique characteristics. The following list shows the `create_clock` command and the available options:

```
create_clock
-period <period value>
[-name <clock name>]
[-waveform <edge list>]
[-add]
<source objects>
```

Table 6–4 describes the options for the `create_clock` command.

Table 6–4. Option Descriptions for create_clock

Option	Description
`-period` <*period value*>	Specifies the clock period. You can also specify the frequency as `-period` <*num*>`MHz`. *(1)*
`-name` <*clock name*>	Name of the specific clock, for example, `sysclock`. If you do not specify the clock name, the clock name is the same as the node to which it is assigned.
`-waveform` <*edge list*>	Specifies the clock's rising and falling edges. The edge list alternates between rising edge and falling edge. For example, a 10 ns period where the first rising edge occurs at 0 ns and the first falling edge occurs at 5 ns would be written as `waveform {0 5}`. The difference must be within one period unit, and the rise edge must come before the fall edge. The default edge list is `{0` <*period*>`/2}`, or a 50% duty cycle.
`-add`	Allows you to specify more than one clock to the same port or pin.
<*source objects*>	Specifies the port(s) or pin(s) to which the assignment applies. If source objects are not specified, the clock is a virtual clock. Refer to "Virtual Clocks" on page 6–27 for more information.

Note to Table 6–4:
(1) The default time unit in the TimeQuest analyzer is nanoseconds (ns).

Example 6–1 shows how to create a 10 ns clock with a 50% duty cycle, where the first rising edge occurs at 0 ns applied to port `clk`.

Example 6–1. 100MHz Clock Creation

```
create_clock -period 10 -waveform { 0 5 } clk
```

Example 6–2 shows how to create a 10 ns clock with a 50% duty cycle that is phase shifted by 90 degrees applied to port `clk_sys`.

Example 6–2. 100MHz Shifted by 90 Degrees Clock Creation

```
create_clock -period 10 -waveform { 2.5 7.5 } clk_sys
```

Clocks defined with the `create_clock` command have a default source latency value of zero. The TimeQuest analyzer automatically computes the clock's network latency for non-virtual clocks.

Generated Clocks

The TimeQuest analyzer considers clock dividers, ripple clocks, or circuits that modify or change the characteristics of the incoming or master clock as generated clocks. You should define the output of these circuits as generated clocks. This definition allows the TimeQuest analyzer to analyze these clocks and account for any network latency associated with them.

You can use the `create_generated_clock` command to create generated clocks. The following list shows the `create_generated_clock` command and the available options:

```
create_generated_clock
[-name <clock name>]
-source <master pin>
[-edges <edge list>]
[-edge_shift <shift list>]
[-divide_by <factor>]
[-multiply_by <factor>]
[-duty_cycle <percent>]
[-add]
[-invert]
[-master_clock <clock>]
[-phase <phase>]
[-offset <offset>]
<source objects>
```

Table 6–5 describes the options for the `create_generated_clock` command.

Table 6–5. Options Description for create_generated_clock (Part 1 of 2)

Option	Description
`-name` <*clock name*>	Name of the generated clock, for example, `clk_x2`. If you do not specify the clock name, the clock name is the same as the first node to which it is assigned.
`-source` <*master pin*>	The <*master pin*> specifies the node in the design from which the clock settings derive.
`-edges` <*edge list*> | `-edge_shift` <*shift list*>	The `-edges` option specifies the new rising and falling edges with respect to the master clock's rising and falling edges. The master clock's rising and falling edges are numbered `1..`<*n*> starting with the first rising edge, for example, edge 1. The first falling edge after that is edge number 2, the next rising edge number 3, and so on. The <*edge list*> must be in increasing order. The same edge may be used for two entries to indicate a clock pulse independent of the original waveform's duty cycle. `edge_shift` specifies the amount of shift for each edge in the <*edge list*>. The `-invert` option can be used to invert the clock after the `-edges` and `-edge_shifts` are applied. *(1)*

Table 6–5. Options Description for create_generated_clock (Part 2 of 2)

Option	Description
`-divide_by` <*factor*> | `-multiply_by` <*factor*>	The `divide_by` and `multiply_by` factors are based on the first rising edge of the clock, and extend or contract the waveform by the specified factors. For example, a `-divide_by 2` is equivalent to `-edges {1 3 5}`. For multiplied clocks, the duty cycle can also be specified. The TimeQuest analyzer supports specifying multiply and divide factors at the same time.
`-duty_cycle` <*percent*>	Specifies the duty cycle of the generated clock. The duty cycle is applied last.
`-add`	Allows you to specify more than one clock to the same pin.
`-invert`	Inversion is applied at the output of the clock after all other modifications are applied, except duty cycle.
`-master_clock` <*clock*>	`master_clock` is used to specify the clock if multiple clocks exist at the master pin.
`-phase` <*phase*>	Specifies the phase of the generated clock.
`-offset` <*offset*>	Specifies the offset of the generated clock.
<*source objects*>	Specifies the port(s) or pin(s) to which the assignment applies.

Note to Table 6–5:
(1) The TimeQuest analyzer supports a maximum of three edges in the edge list.

Source latencies are based on clock network delays from the master clock (not necessarily the master pin). You can use the `set_clock_latency -source` command to override the source latency.

Figure 6–14 shows how to create an inverted generated clock based on a 10 ns clock.

Figure 6–14. Generating an Inverted Clock

```
create_clock -period 10 [get_ports clk]
create_generated_clock -divide_by 1 -invert -source [get_registerss clk] [get_registers gen|clkreg]
```

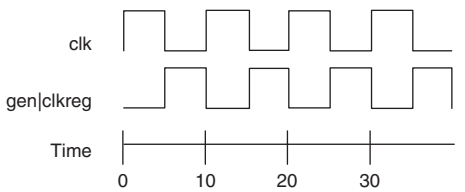


Figure 6–15 shows how to modify the generated clock using the `-edges` and `-edge_shift` options.

Figure 6–15. Edges & Edge Shifting a Generated Clock

```
create_clock -period 10 -waveform { 0 5 } [get_ports clk]
# Creates a divide-by-2 clock
create_generated_clock -source [get_ports clk] -edges { 1 3 5 } [get_registers clkdivA|clkreg]
# Creates a divide-by-2 clock independent of the master clock's duty cycle (now 50%)
create_generated_clock -source [get_ports clk] -edges { 1 1 5 } -edge_shift { 0 5 0 } [get_registers clkdivB|clkreg]
```

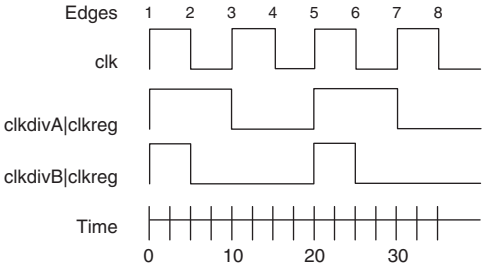
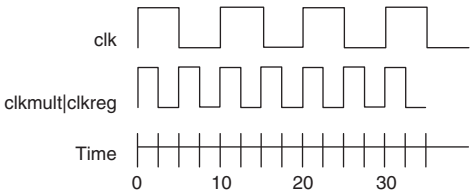


Figure 6–16 shows the effect of the `-multiply` option on the generated clock.

Figure 6–16. Multiplying a Generated Clock

```
create_clock -period 10 -waveform { 0 5 } [get_ports clk]
# Creates a multiply-by-2 clock
create_generated_clock -source [get_ports clk] -multiply_by 2 [get_registers clkmult|clkreg]
```



Virtual Clocks

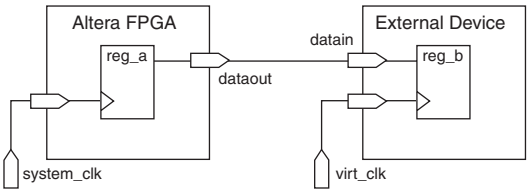
A virtual clock is a clock that does not have a real source in the design or that does not interact directly with the design. For example, if a clock feeds only an external device's clock port, and not a clock port in the design, and the external device then feeds (or is fed by) a port in the design, it is considered a virtual clock.

You can use the `create_clock` command to create virtual clocks, with no value specified for the `source` option.

You can use virtual clocks for `set_input_delay` and `set_output_delay` constraints.

Figure 6–17 shows an example where a virtual clock is required for the TimeQuest analyzer to properly analyze the relationship between the external register and those in the design. Because the oscillator labeled `virt_clk` does not interact with the Altera device, but acts as the clock source for the external register, the clock `virt_clk` must be declared. Example 6–3 shows the command to create a 10 ns virtual clock named `virt_clk` with a 50% duty cycle where the first rising edge occurs at 0 ns. The virtual clock is then used as the clock source for an output delay constraint.

Figure 6–17. Virtual Clock Board Topology



After you create the virtual clock, you can perform register-to-register analysis between the register in the Altera device and the register in the external device.

Example 6–3. Virtual Clock Example 1

```
#create base clock for the design
create_clock -period 5 [get_ports system_clk]
#create the virtual clock for the external register
create_clock -period 10 -name virt_clk -waveform { 0 5 }
#set the output delay referencing the virtual clock
set_output_delay -clock virt_clk -max 1.5 [get_ports dataout]
```

Example 6–4 shows the command to create a 10 ns virtual clock with a 50% duty cycle that is phase shifted by 90 degrees.

Example 6–4. Virtual Clock Example 2

```
create_clock -name virt_clk –period 10 –waveform { 2.5 7.5 }
```

Multi-Frequency Clocks

Certain designs have more than one clock source feeding a single clock port in the design. The additional clock may act as a low power clock, with a lower frequency than the primary clock. To analyze this type of design, the `create_clock` command supports the `-add` option that allows you to add more than one clock to a clock node.

Example 6–5 shows the command to create a 10 ns clock applied to clock port `clk`, and then add an additional 15 ns clock to the same clock port. The TimeQuest analyzer uses both clocks when it performs timing analysis.

Example 6–5. Multi-Frequency Example

```
create_clock -period 10 -name clock_primary -waveform { 0 5 } [get_ports clk]
create_clock -period 15 -name clock_secondary -waveform { 0 7.5 } [get_ports clk] -add
```

Automatic Clock Detection

To create clocks for all clock nodes in your design automatically, use the `derive_clocks` command. This command creates clocks on ports or registers to ensure every register in the design has a clock.

The following list shows the `derive_clocks` command including the available options:

`derive_clocks`
`-period` <*period value*>
`[-waveform` <*edge list*>`]`

Table 6–4 describes the options for the `derive_clocks` command.

Table 6–6. Options Description for derive_clocks

Option	Description
`-period` <*period value*>	Creates the clock period. You can also specify the frequency as `-period` <*num*>`MHz`. *(1)*
`-waveform` <*edge list*>	Creates the clock's rising and falling edges. The edge list alternates between rising edge and falling edge. For example, for a 10 ns period where the first rising edge occurs at 0 ns and first falling edge occurs at 5 ns, the edge list is `waveform {0 5}`. The difference must be within one period unit, and the rising edge must come before the falling edge. The default edge list is `{0 period/2}`, or a 50% duty cycle.

Note to Table 6–6:
(1) This option uses the default time unit nanoseconds (ns).

The derive_clocks command does not create clocks for the outputs of the PLLs.

The derive_clocks command is equivalent to using create_clock for each register or port feeding the clock pin of a register.

The use of the derive_clocks command for final timing signoff is not recommended. You should create clocks for all clock sources using the create_clock and create_generated_clock commands.

Derive PLL Clocks

PLLs are used for clock management and synthesis in Altera devices. You can customize the clocks generated from the outputs of the PLL based on the design requirements. Because a clock should be created for all clock nodes, all outputs of the PLL should have an associated clock.

You can manually create a clock for each output of the PLL with the create_generated_clock command, or you can use the derive_pll_clocks command, which automatically searches the timing netlist and creates generated clocks for all PLL outputs according to the settings specified for each PLL output.

You can use the derive_pll_clocks command to automatically create a clock for each output of the PLL as shown in the following list:

```
derive_pll_clocks
[-use_tan_name]
```

Table 6–7 describes the options for the derive_pll_clocks command.

Table 6–7. Options Description for derive_pll_clocks

Option	Description
-use_tan_name	By default, the clock name is the output clock name. This option uses the net name which is used by the Classic Timing Analyzer uses.

The derive_pll_clocks command calls the create_generated_clock command to create generated clocks on the outputs of the PLL. The source for the create_generated_clock command is the input clock pin of the PLL. Before or after the derive_pll_clocks command has been issued, you must manually create a base clock for the input clock port of the PLL. If a clock is not

defined for the input clock node of the PLL, no clocks are reported for the PLL outputs. Instead, the TimeQuest analyzer issues a warning message similar to Figure 6–18 when the timing netlist is updated.

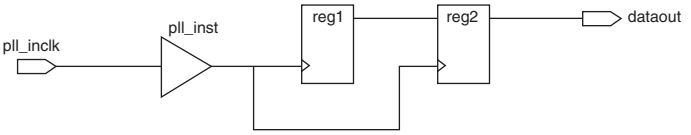
Figure 6–18. Warning Message

```
Warning: The master clock for this clock assignment could not be derived.
Clock: <name of PLL output clock pin name> was not created.
```

You can include the `derive_pll_clocks` command in your SDC file, that allows the `derive_pll_clocks` command to automatically detect any changes to the PLL. With the `derive_pll_clocks` command in your SDC file, each time the file is read, the appropriate `create_generated_clock` command for the PLL output clock pin is generated. If you use the `write_sdc` command after the `derive_pll_clock` command, the new SDC file contains the individual `create_generated_clock` commands for the PLL output clock pins and not the `derive_pll_clocks` command. Any changes to the properties of the PLL are not automatically reflected in the new SDC file. You must manually update the `create_generated_clock` commands in the new SDC file written by the `derive_pll_clocks` command, to reflect the changes to the PLL.

For example, Figure 6–19 shows a simple PLL design with a register-to-register path.

Figure 6–19. Simple PLL Design



You can use the `derive_pll_clocks` command to automatically constrain the PLL. When this command is issued for the design shown in Figure 6–19, the following messages are generated:

```
Info:
Info: Deriving PLL Clocks:
Info: create_generated_clock -source pll_inst|altpll_component|pll|INCLK[0] -divide_by 2 -name
pll_inst|altpll_component|pll|CLK[0] pll_inst|altpll_component|pll|CLK[0]
Info:
```

The node name pll_inst|altpll_component|pll|INCLK[0] used for the source option refers to the input clock pin of the PLL. In addition, the name of the output clock of the PLL is the name of the PLL output clock node, pll_inst|altpll_component|pll|CLK[0].

If the PLL is in clock switchover mode, multiple clocks are created for the output clock of the PLL; one for the primary input clock (for example, INCLK[0]), and one for the secondary input clock (for example, INCLK[1]).

Before you can generate any reports for this design, you must create a base clock for the PLL input clock port. You can use a command similar to the following:

```
create_clock -period 5 [get_ports pll_inclk]
```

You do not have to generate the base clock on the input clock pin of the PLL: pll_inst|altpll_component|pll|INCLK[0]. The clock created on the PLL input clock port propagates to all fan-out of the clock port, including the PLL input clock pin.

Clock Removal

You can use the remove_clock command to remove clocks that have been previously created.

The following list shows the remove_clock command including the available options:

```
remove_clock
[-name <clock name>]
```

Table 6–8 describes the options for the remove_clock command.

Table 6–8. Options Description for remove_clock

Option	Description
-name <*clock name*>	Specifies the clock to be removed.

Example 6–6 creates a 10 ns clock named CLK and then remove the clock CLK.

Example 6–6. remove_clock Example

```
create_clock -period 10 -name CLK -waveform { 0 5 }
remove_clock -name CLK
```

Clock Groups

Many clocks can exist in a design, however, not all of the clocks interact with one another, and certain clock interactions are not possible. Asynchronous clocks are unrelated clocks (asynchronous clocks have different ideal clock sources). Exclusive clocks are not active at the same time (for example, multiplexed clocks). The mutual exclusivity must be declared to the TimeQuest analyzer to prevent it from analyzing these clock interactions.

You can use the `set_clock_groups` command to specify clocks that are exclusive or asynchronous. The following list shows the `set_clock_groups` command, including the available options:

```
set_clock_groups
[-asynchronous | -exclusive]
-group <clock name>
-group <clock name>
[-group <clock name>] ...
```

Table 6–9 describes the options for the `set_clock_groups` command.

Table 6–9. Options Description for set_clock_groups

Option	Description
`-asynchronous | -exclusive`	Specifies mutually exclusive clocks.
`-group <clock name>`	Specifies valid destination clock names that are mutually exclusive. <*clock name*> is used to specify the clock names.

Example 6–7 shows a `set_clock_groups` command and the equivalent `set_false_path` commands.

Example 6–7. set_clock_groups Example

```
# Clocks A & C are never active when clocks B & D are active
set_clock_groups -exclusive -group {A C} -group {B D}

# Equivalent specification using false paths
set_false_path -from [get_clocks A] -to [get_clocks B]
set_false_path -from [get_clocks A] -to [get_clocks D]
set_false_path -from [get_clocks C] -to [get_clocks B]
set_false_path -from [get_clocks C] -to [get_clocks D]
set_false_path -from [get_clocks B] -to [get_clocks A]
set_false_path -from [get_clocks B] -to [get_clocks C]
set_false_path -from [get_clocks D] -to [get_clocks A]
set_false_path -from [get_clocks D] -to [get_clocks C]
```

Clock Effect Characteristics

The `create_clock` and `create_generated_clock` commands create ideal clocks that do not account for any board effects. This section describes how to account for clock effect characteristics with clock latency and clock uncertainty.

Clock Latency

There are two forms of clock latency: source and network. Source latency is the propagation delay from the origin of the clock to the clock definition point (for example, a clock port), and network latency is the propagation delay from a clock definition point to a register's clock pin. The total latency (or clock propagation delay) at a register's clock pin is the sum of the source and network latencies in the clock path.

You can use the `set_clock_latency` command to specify input delay constraints to ports in the design. The following list shows the `set_clock_latency` command including the available options:

```
set_clock_latency
-source
[-rise | -fall]
[-late | -early]
<delay>
<object list>
```

Table 6–10 describes the options for the `set_clock_latency` command.

Table 6–10. Options Description for set_clock_latency

Option	Description
`-source`	Specify a source latency.
`-rise | -fall`	Specify the rising or falling delays.
`-late | -early`	Specifies the earliest or the latest arrival times to the clock.
<*delay*>	Specifies the delay value.
<*object list*>	Specifies the clocks or clock sources if a clock is clocked by more than one clock.

The TimeQuest analyzer automatically computes network latencies, therefore, the `set_clock_latency` command specifies only the source latencies.

Clock Uncertainty

The `set_clock_uncertainty` command specifies clock uncertainty or skew for clocks or clock-to-clock transfers. You can specify the uncertainty separately for setup and hold, and you can specify separate rising and falling clock transitions. The TimeQuest analyzer subtracts the setup uncertainty from the data required time for each applicable path, and adds the hold uncertainty to the data required time for each applicable path.

You can use the `set_clock_uncertainty` command to specify any clock uncertainty to the clock port. The following list shows the `set_clock_uncertainty` command including the available options:

```
set_clock_uncertainty
[-from <from clock>]
[-rise_from <rise from clock>]
[-fall_from <fall from clock>]
[-to <to clock>]
[-rise_to <rise to clock>]
[-fall_to <fall to clock>]
[-setup | -hold]
<uncertainty value>
```

Table 6–11 describes each of the options for the `set_clock_uncertainty` command.

Table 6–11. Options Description for set_clock_uncertainty

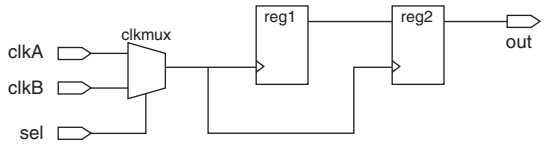
Option	Description
`-from` <*from clock*>	Specifies the from clock.
`-rise_from` <*rise from clock*>	Specifies the rise from clock.
`-fall_from` <*fall from clock*>	Specifies the fall from clock.
`-to` <*to clock*>	Specifies the to clock.
`-rise_to` <*rise to clock*>	Specifies the rise to clock.
`-fall_to` <*fall to clock*>	Specifies the fall to clock.
`-setup | -hold`	Specifies setup or hold.
<*uncertainty value*>	

Application Examples

This section describes specific examples for the `create_clock` and `create_generated_clock` commands.

Figure 6–20 shows a clock multiplexer design. Ports clkA (10 ns) and clkB (15 ns) feed the multiplexer, and the multiplexer feeds the clock pin of the registers.

Figure 6–20. Clock Multiplexer, Example 1



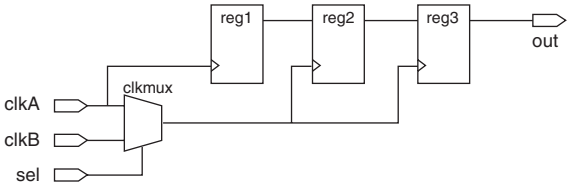
Use the constraints shown in Example 6–8 to fully constrain the clocking structure shown in Figure 6–20.

Example 6–8. Constraints

```
#create clocks for the clock ports
create_clock -period 10 [get_ports clkA]
create_clock -period 15 [get_ports clkB]
#cut all clock paths between clkA and clkB
#there are two ways to accomplish this
#first
set_clock_groups -exclusive -group {clkA} -group {clkB}
#Alternatively, the command can be specified as
set_false_path -from [get_clocks clkA] -to [get_clocks clkB]
set_false_path -from [get_clocks clkB] -to [get_clocks clkA]
```

Figure 6–21 shows a a clocking structure that is similar to the one shown in Figure 6–20, except that clkA now feeds the first register's clock pin.

Figure 6–21. Clock Multiplexer, Example 2



The constraints shown Example 6–8 cannot be used to constrain the design shown in Figure 6–21 because clkA and clkB can now interact.

The constraints shown in Example 6–9 fully constrains the clock structure shown in Figure 6–21.

Example 6–9. Constraints

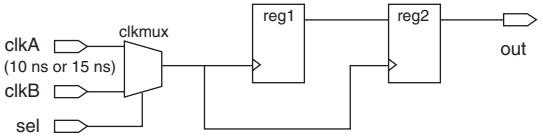
```
#create clocks for the clock ports
create_clock -period 10 [get_ports clkA]
create_clock -period 15 [get_ports clkB]
#create generated clocks for the output of the MUX
create_generated_clock -name clkmuxA -source [get_pins clkmux|INCLK[0]] \
    [get_pins clkmux|OUTCLK]
create_generated_clock -name clkmuxB -source [get_pins clkmux|INCLK[1]] \
    [get_pins clkmux|OUTCLK] -add
#cut all paths between clocks clkmuxA and clkmuxB
set_clock_groups -exclusive -group {clkmuxA} -group {clkmuxB}
```

Figure 6–22 shows a clocking structure that is similar to the one shown in Figure 6–20 except that `clkA` can act as either a 10 ns or 15 ns clock and `clkB` is a 5 ns clock. The constraints shown in Example 6–10 fully constrains the clock structure shown in Figure 6–22.

Example 6–10. Constraints

```
#create a 10 ns clock for clock port clkA
create_clock -name clkA10 -period 10 [get_ports clkA]
#create a 15 ns clock for clock port clkA with the add option
create_clock -name clkA15 -period 15 -add [get_ports clkA]
#create a 5 ns clock for clock port clkB
create_clock -period 5 [get_ports clkB]
#cut all paths between clock clkA and clkB
set_clock_groups -exclude -group {clkA10} -group {clkA15} -group {clkB}
```

Figure 6–22. Clock Multiplexer, Example 3



I/O Specifications & Analysis

The TimeQuest analyzer supports Synopsys Design Constraints that constrain the ports in your design. These constraints allow the TimeQuest analyzer to perform a system static timing analysis that includes not only the FPGA timing, but also any external device timing and board timing parameters.

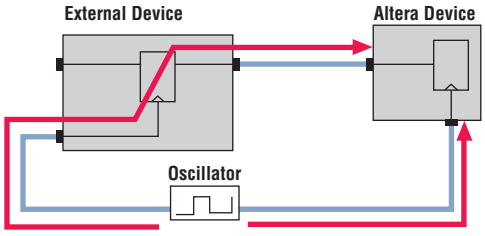
Input and Output Delay

Use input and output delay constraints to specify any external device or board timing parameters. When you apply these constraints, the TimeQuest analyzer performs static timing analysis on the entire system.

Set Input Delay

The `set_input_delay` constraint specifies the data arrival time at a port (a device I/O) with respect to a given clock. Figure 6–23 shows an input delay path.

Figure 6–23. Set Input Delay



You can use the `set_input_delay` command to specify input delay constraints to ports in the design. The following list shows the `set_input_delay` command including the available options:

```
set_input_delay
-clock <clock name>
[-clock_fall]
[-rise | -fall]
[-max | -min]
[-add_delay]
[-reference_pin <pin or port>]
<delay value>
<port pin list>
```

Table 6–12 describes the options for the `set_input_delay` command.

Table 6–12. Options Description for set_input_delay

Option	Description
`-clock` <*clock name*>	Specifies the source clock.
`-clock_fall`	Specifies the arrival time with respect to the falling edge of the clock.
`-rise	-fall`	Specifies either the rise or fall delay at the port.
`-max	-min`	Specifies the minimum or maximum data arrival time.
`-add_delay`	Adds the current delay to the constraint and does not replace any existing delay.
`-reference_pin` <*pin or port*>	Specifies a pin or port in the design from which to determine source and network latencies. This is useful to specify input delays relative to an output port fed by a clock.
<*delay value*>	Specifies the delay value.
<*port pin list*>	Specifies the destination ports or pins.

A warning message appears if you specify only a `–max` or `–min` value for the input delay value. The input minimum delay default value is the input maximum delay, and the input maximum delay default value is the input minimum delay, if only one is specified. Similarly, a warning message appears if you specify only a `-rise` or `-fall` value for the delay value, and the delay defaults in the same manner as the input minimum and input maximum delays.

The maximum value is used for setup checks, and the minimum value is used for hold checks.

By default, a set of input delays (min/max, rise/fall) is allowed for only one clock, `-clock_fall`, `-reference_pin` combination. Specifying an input delay on the same port for a different clock, `-clock_fall`, or `-reference_pin` removes any previously set input delays, unless you specify the `-add_delay` option. When you specify the `-add_delay` option, the worst-case values are used.

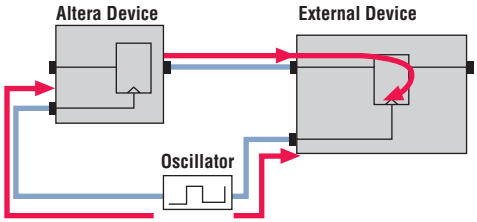
The `-rise` and `-fall` options are mutually exclusive. The `-min` and `-max` options are also mutually exclusive.

Set Output Delay

Specifies the data required time at a port (the device pin) with respect to a given clock.

You can use the set_output_delay command to specify output delay constraints to ports in the design. Figure 6–24 shows an output delay path.

Figure 6–24. Output Delay



The following list shows the set_output_delay command including the available options:

```
set_output_delay
-clock <clock name>
[-clock_fall]
[-rise | -fall]
[-max | -min]
[-add_delay]
[-reference_pin <pin or port>]
<delay value>
<port pin list>
```

Table 6–13 describes the options for the set_output_delay command.

Table 6–13. Options Description for set_output_delay

Option	Description
-clock <*clock name*>	Specifies the source clock.
-clock_fall	Specifies the required time with respect to the falling edge of the clock.
-rise | -fall	Specifies either the rise or fall delay at the port.
-max | -min	Specifies the minimum or maximum data arrival time.
-add_delay	Add to the current delay to the constraint and does not replace any existing delay.
-reference_pin <*pin or port*>	Specifies a pin or port in the design from which to determine source and network latencies. You can use this option to specify input delays relative to an output port fed by a clock.
<*delay value*>	Specifies the delay value.
<*port pin list*>	Specifies the destination ports or pins.

A warning message appears if you specify only a –max or –min value for the output delay value. The output minimum delay default value is the output maximum delay, and the output maximum delay default value is the output minimum delay, if only one is specified.

The maximum value is used for setup checks, and the minimum value is used for hold checks.

By default, a set of output delays (min/max, rise/fall) is allowed for only one clock, -clock_fall, port combination. Specifying an output delay on the same port for a different clock or -clock_fall removes any previously set output delays, unless you specify the -add_delay option. When you specify the -add_delay option, the worst-case values are used.

The -rise and -fall options are mutually exclusive, as are the -min and -max options.

Timing Exceptions

Timing exceptions modify the default analysis that is performed by the TimeQuest analyzer. This section describes the following available timing exceptions:

- False path
- Minimum delays
- Maximum delays
- Multicycle path

Precedence

If a conflict of node names occurs between timing exceptions, the following order of precedence applies:

1. False path
2. Minimum delays and maximum delays
3. Multicycle path

The false path timing exception has the highest precedence. Within each category, assignments to individual nodes have precedence over assignments to clocks. Finally, the remaining precedence for additional conflicts is order-dependent, such that the last assignments overwrite (or partially overwrite) earlier assignments.

False Path

False paths are paths that can be ignored during timing analysis.

You can use the `set_false_path` command to specify false paths in the design. The following list shows the `set_false_path` command including the available options:

```
set_false_path
[-from <from list>]
[-to <to list>]
[-thru <thru list>]
```

Table 6–14 describes the options for the `set_false_path` command.

Table 6–14. Options Description for set_false_path

Option	Description
`-from` <*from list*>	The <*from list*> is a collection or list of objects in the design.
`-to` <*to list*>	The <*to list*> is a collection or list of objects in the design.
`-thru` <*thru list*>	The <*thru list*> is a collection or list of objects in the design. The <*thru list*> acts as the thru point of the path.

When the objects are timing nodes, the false path only applies to the path between the two nodes. When an object is a clock, the false path applies to all paths where the source node (for `-from`) or destination node (for `-to`) is clocked by the clock.

Minimum Delay

You can use the `set_min_delay` command to specify an absolute minimum delay for a given path. The following list shows the `set_min_delay` command including the available options:

```
set_min_delay
[-from <from list>]
[-to <to list>]
[-thru <thru list>]
<delay value>
```

Table 6–15 describes the options for the set_min_delay command.

Table 6–15. Options Description for set_min_delay

Option	Description
-from <*from list*>	The <*from list*> is a collection or list of objects in the design. The <*from list*> acts as the start point of the path.
-to <*to list*>	The <*to list*> is a collection or list of objects in the design. The <*to list*> acts as the end point of the path.
-thru <*thru list*>	The <*thru list*> is a collection or list of objects in the design. The <*thru list*> acts as the thru point of the path.
<*delay value*>	Specifies the delay value.

If the source or destination node is clocked, then the clock paths are taken into account, allowing more or less delay on the data path. If the source or destination node has an input or output delay, that delay is also included in the minimum delay check.

When the objects are timing nodes, the minimum delay applies only to the path between the two nodes. When an object is a clock, the minimum delay applies to all paths where the source node (for -from) or destination node (for -to) is clocked by the clock.

You can apply the set_min_delay command exception to an output port that does not use a set_output_delay constraint. In this case, the setup summary and hold summary report the slack for these paths. Because there is no clock associated with the output port, no clock is reported for these paths and the **Clock** column is empty. In this case, you cannot report timing for these paths.

To report timing using clock filters for output paths with the set_min_delay command, you must use the set_output_delay command for the output port with a value of 0. You can use an existing clock from the design or a virtual clock as the clock reference in the set_output_delay command.

Maximum Delay

You can use the `set_max_delay` command to specify an absolute maximum delay for a given path. The following list shows the `set_max_delay` command including the available options:

```
set_max_delay
[-from <from list>]
[-to <to list>]
[-thru <thru list>]
<delay value>
```

Table 6–16 describes the options for the `set_max_delay` command.

Table 6–16. Options Description for set_max_delay

Option	Description
`-from` <*from list*>	The <*from list*> is a collection or list of objects in the design. The <*from list*> acts as the start point of the path.
`-to` <*to list*>	The <*to list*> is a collection or list of objects in the design. The <*to list*> acts as the end point of the path.
`-thru` <*thru list*>	The <*thru list*> is a collection or list of objects in the design. The <*thru list*> acts as the thru point of the path.
<*delay value*>	Specifies the delay value.

If the source or destination node is clocked, then the clock paths are taken into account, allowing more or less delay on the data path. If the source or destination node has an input or output delay, that delay is also included in the maximum delay check.

When the objects are timing nodes, the maximum delay only applies to the path between the two nodes. When an object is a clock, the maximum delay applies to all paths where the source node (for `-from`) or destination node (for `-to`) is clocked by the clock.

You can apply the `set_max_delay` command exception to an output port that does not use a `set_output_delay` constraint. In this case, the setup summary and hold summary report the slack for these paths. Because there is no clock associated with the output port, no clock is reported for these paths and the **Clock** column is empty. In this case, you cannot report timing for these paths.

To report timing using clock filters for output paths with the `set_max_delay` command, you must use the `set_output_delay` command for the output port with a value of 0. You can use an existing clock from the design or a virtual clock as the clock reference in the `set_output_delay` command.

Multicycle Path

By default, the TimeQuest analyzer uses a single-cycle analysis. When analyzing a path, the setup launch and latch edge times are determined by finding the closest two active edges in the respective waveforms. For a hold analysis, the timing analyzer analyzes the path against two timing conditions for every possible setup relationship, not just the worst-case setup relationship. Therefore, the hold launch and latch times may be completely unrelated to the setup launch and latch edges.

A multicycle constraint relaxes setup or hold relationships by the specified number of clock cycles based on the source (`-start`) or destination (`-end`) clock. An end multicycle constraint of 2 extends the worst-case setup latch edge by one destination clock period.

Hold multicycle constraints are based on the default hold position (the default value is 0). An end hold multicycle constraint of 1 effectively subtracts one destination clock period from the default hold latch edge.

You can use the `set_multicycle_path` command to specify the multicycle constraints in the design. The following list shows the `set_multicycle_path` command including the available options:

```
set_multicycle_path
[-setup | -hold]
[-start | -end]
[-from <from list>]
[-to <to list>]
[-thru <thru list>]
<path multiplier>
```

Table 6–17 describes the options for the `set_multicycle_path` command.

Table 6–17. Options Description for set_multicycle_path

Option	Description
`-setup | -hold`	Specifies the type of multicycle to be applied.
`-start | -end`	Specifies whether the start or end clock acts the source or destination for the multicycle.
`-from` <*from list*>	The <*from list*> is a collection or list of objects in the design. The <*from list*> acts as the start point of the path.
`-to` <*to list*>	The <*to list*> is a collection or list of objects in the design. The <*to list*> acts as the end point of the path.
`-thru` <*thru list*>	The <*thru list*> is a collection or list of objects in the design. The <*thru list*> acts as the thru point of the path.
<*path multiplier*>	Specifies the multicycle multiplier value.

When the objects are timing nodes, the multicycle constraint only applies to the path between the two nodes. When an object is a clock, the multicycle constraint applies to all paths where the source node (for `-from`) or destination node (for `-to`) is clocked by the clock.

Collections

The TimeQuest analyzer supports collection APIs that provide easy access to ports, pins, cells, or nodes in the design. You can use collection APIs with any valid constraints or Tcl commands specified in the TimeQuest analyzer.

Table 6–18 describes the collection commands supported by the TimeQuest analyzer.

Table 6–18. Collection Commands (Part 1 of 2)

Command	Description
`all_clocks`	Returns a collection of all clocks in the design.
`all_inputs`	Returns a collection of all input ports in the design.
`all_outputs`	Returns a collection of all output ports in the design.
`all_registers`	Returns a collection of all registers in the design.
`get_cells`	Returns a collection of cells in the design. All cell names in the collection match the specified pattern. Wildcards can be used to select multiple cells at the same time.

Table 6–18. Collection Commands (Part 2 of 2)

Command	Description
`get_clocks`	Returns a collection of clocks in the design. When used as an argument to another command, such as the `-from` or `-to` of `set_multicycle_path`, each node in the clock represents all nodes clocked by the clocks in the collection. The default uses the specific node (even if it is a clock) as the target of a command.
`get_keepers`	Returns a collection of keeper nodes (non-combinational nodes) in the design.
`get_nets`	Returns a collection of nets in the design. All net names in the collection match the specified pattern. You can use wildcards to select multiple nets at the same time.
`get_nodes`	Returns a collection of nodes in the design.
`get_pins`	Returns a collection of pins in the design. All pin names in the collection match the specified pattern. You can use wildcards to select multiple pins at the same time.
`get_ports`	Returns a collection of ports (design inputs and outputs) in the design.
`get_registers`	Returns a collection of registers in the design.

For more information on collections, refer to the SDC file and the *SDC & TimeQuest API Reference Manual*.

Application Examples

Example 6–11 shows various uses of the `create_clock` and `create_generated_clock` commands and specific design structures.

Example 6–11. create_clock & generate_clock Commands & Specific Design structures

```
# Create a simple 10 ns with clock with a 60 % duty cycle
create_clock -period 10 -waveform {0 6} -name clk [get_ports clk]
# The following multicycle applies to all paths ending at registers
# clocked by clk
set_multicycle_path -to [get_clocks clk] 2
```

Timing Reports

The TimeQuest analyzer provides real-time static timing analysis result reports. Reports are generated only when requested. Each report can be customized to display specific timing information, excluding those fields not required.

This section describes the various report generation commands supported by the TimeQuest analyzer.

report_timing

You can use the `report_timing` command to generate a setup, hold, recovery, or removal report.

The following list shows the `report_timing` command including the available options:

```
report_timing
[-append]
[-file <name>]
[-from <names>]
[-from_clock <names>]
[-hold]
[-less_than_slack <slack limit>]
[-npaths <number>]
[-panel_name <name>]
[-recovery]
[-removal]
[-setup]
[-stdout]
[-summary]
[-thru <names>]
[-to <names>]
[-to_clock <names>]
```

Table 6–19 describes the options for the `report_timing` command.

Table 6–19. Option Descriptions for report_timing (Part 1 of 2)

Option	Description
`-append`	Specifies that the current report be appended to the file specified by the `-file` option.
`-file <name>`	Indicates that the current report is written to the file <*name*>.
`-from <names>`	Specifies the from node for the analysis.
`-from_clock <names>`	Specifies the source clock for the analysis.
`-hold`	Specifies a clock hold analysis.

Table 6–19. Option Descriptions for report_timing (Part 2 of 2)

Option	Description
`-less_than_slack` <*slack limit*>	Limits the paths to be reported to those the <*slack limit*> value.
`-npaths` <*number*>	Specifies the number of paths to report.
`-panel_name` <*name*>	Specifies the name of the panel in the reports pane.
`-recovery`	Specifies a recovery analysis.
`-removal`	Specifies a removal analysis.
`-setup`	Specifies a clock setup analysis.
`-stdout`	Indicates the report be sent to `stdout`.
`-summary`	Creates a condensed version of the full report for each path specified by `-npaths`.
`-thru` <*names*>	Specifies the thru node for the analysis.
`-to` <*names*>	Specifies the to node for the analysis.
`-to_clock` <*names*>	Specifies the destination clock for the analysis.

Example 6–12 shows a sample report that results from typing the following:

```
report_timing -from_clock clk_async -to_clock \
clk_async -setup -npaths 1 ↵
```

Example 6–12. Sample report_timing Report

```
    Info:
============================================================
    Info: To Node      : dst_reg
    Info: From Node    : src_reg
    Info: Latch Clock  : clk_async
    Info: Launch Clock : clk_async
    Info:
    Info: Data Arrival Path:
    Info:
    Info: Total (ns)  Incr (ns)     Type  Node
    Info: ==========  ========= ==  ====  =========================
    Info:      0.000      0.000           launch edge time
    Info:      2.237      2.237  R        clock network delay
    Info:      2.410      0.173     uTco  src_reg
    Info:      2.410      0.000 RR  CELL  src_reg|REGOUT
    Info:      3.407      0.997 RR    IC  dataout|DATAIN
    Info:      3.561      0.154 RR  CELL  dst_reg
    Info:
    Info: Data Required Path:
    Info:
    Info: Total (ns)  Incr (ns)     Type  Node
    Info: ==========  ========= ==  ====  =========================
    Info:     10.000     10.000           latch edge time
    Info:     11.958      1.958  R        clock network delay
    Info:     11.610     -0.348     uTsu  dst_reg
    Info:
    Info: Data Arrival Time  :     3.561
    Info: Data Required Time :    11.610
    Info: Slack              :     8.049
    Info: ===========================================================
```

report_clock_transfers

You can use the `report_clock_transfers` command to generate a report that details all clock-to-clock transfers in the design. A clock-to-clock transfer is reported if a path exists between two registers that are clocked by two different clocks. Information such as the number of destinations and sources is also reported.

You can use the `report_clock_transfers` command to generate a setup, hold, recovery, or removal report.

The following list shows the `report_clock_transfers` command including the available options:

```
report_clock_transfers
[-matrix]
[-panel_name <name>]
```

Table 6–20 describes the options for the `report_clock_transfers` command.

Table 6–20. Option Descriptions for report_clock_transfers

Option	Description
`-matrix`	Formats the report such that the clocks in the design are reported in the row and columns of the report. The default is to have all clocks reported on the same row.
`-panel_name <name>`	Specifies the report name that is available in the **Reports** pane. The default is Clock Transfers.

report_clocks

You can use the `report_clocks` command to generate a report that details all clock in the design. The report contains information such as type, period, waveform (rise and fall), and targets for all clocks in the design.

The following list shows the `report_clocks` command along with the available options:

```
report_clocks
[-panel_name <name>]
[-desc]
```

Table 6–21 describes the options for the `report_clocks` command.

Table 6–21. Option Descriptions for report_clocks

Option	Description
`-panel_name <name>`	Specifies the report name that appears in **Reports** in the **Tasks** pane.
`-desc`	Specifies the clock names to sort in descending order. The default is ascending order.

report_min_pulse_width

A minimum pulse width checks that a clock high or low pulse is sustained enough to recognize an actual change in the clock signal. A failed minimum pulse width check indicates that the register may not recognize the clock transition. You can use the `report_min_pulse_width` command to generate a report that details the minimum pulse width for all clocks in the design. The report contains information for high and low pulses for all clocks in the design.

Each register in the design is reported twice per clock that clocks the register: once for the high pulse and once for the low pulse. The following list shows the report_min_pulse_width command including the available options:

```
report_min_pulse_width
[-append]
[-file <name>]
[-nworst <number>]
[-panel_name <name>]
[-stdout]
[-targets]
```

Table 6–22 describes the options for the report_min_pulse_width command.

Table 6–22. Option Descriptions for report_min_pulse_width

Option	Description
-append	If output is sent to a file, this option appends the result to that file. Otherwise, the file is overwritten.
-file <*name*>	Sends the results to a file.
-nworst <*number*>	Specifies the number of pulse width checks to report. The default is 1.
-panel_name <*name*>	Specifies the report name that appears in the **Reports** pane.
-stdout	Redirects the output to stdout via messages; only required if another output format, such as a file, has been selected and is also to receive messages.
-targets	Specifies registers.

report_net_timing

You can use the report_net_timing command to generate a report that details the delay and fan-out information about a net in the design. A net corresponds to a cell's output pin.

The following list shows the report_net_timing command including the available options:

```
report_net_timing
[-nworst_delay <number>]
[-nworst_fanout <number>]
```

Table 6–23 describes the options for the report_net_timing command.

Table 6–23. Option Descriptions for report_net_timing

Option	Description
-nworst_delay <*number*>	Specifies that <*number*> worst net delays be reported.
-nworst_fanout <*number*>	Specifies that <*number*> worst net fan-outs be reported.

report_sdc

You can use the use the report_sdc command to generate a report of all the Synopsys Design Constraints in the project.

The following list shows the report_sdc command including the available options:

```
report_sdc
[-panel_name <name>]
```

Table 6–24 describes the options for the report_sdc command.

Table 6–24. Option Descriptions for report_sdc

Option	Description
-panel_name <*name*>	Specifies the report name that appears in the **Report** pane. The default is Clock Transfers.

report_ucp

You can use the report_ucp command to generate a report of all unconstrained paths in the design.

The following list shows the report_ucp command including the available options:

```
report_ucp
[-hold]
[-panel_name <name>]
[-setup]
```

Table 6–25 describes the options for the report_ucp command.

Table 6–25. Option Descriptions for report_ucp

Option	Description
-hold	Report all unconstrained hold paths.
-panel_name <*name*>	Specifies the report name that appears in the **Reports** pane.
-setup	Report all unconstrained setup paths.

Timing Analysis Features

Fast Timing Model Analysis

Fast Corner Analysis uses timing models generated under best case conditions (voltage, process, and temperature) for the fastest speed-grade device.

To perform fast timing model timing analysis with the best-case timing models, use the option -fast_model when you create the timing netlist. The following command enables the fast timing models:

```
create_timing_netlist -fast_model
```

When you create a timing netlist, you can also specify the speed grade of the device with which the delays timing netlist will be annotated.

When you use the -fast_model option, you cannot specify a speed because the -fast_model option uses the fastest speed grade.

Wildcard Assignments

To simplify the task of applying constraints to many nodes in a design, the TimeQuest analyzer accepts the "*" and "?" wildcard characters. You can use these wildcard characters to reduce the number of individual constraints you must specify in your design.

The "*" wildcard character matches any string. For example, given an assignment made to a node specified as reg*, the TimeQuest analyzer searches for and applies the assignment to all design nodes that match the prefix reg with none, one, or several characters following, such as reg1, reg[2], regbank, and reg12bank.

The "?" wildcard character matches any single character. For example, given an assignment made to a node specified as `reg?`, the TimeQuest analyzer searches and applies the assignment to all design nodes that match the prefix "`reg`" and any single character following, for example, `reg1`, `rega`, and `reg4`.

Both the collection commands `get_cells` and `get_pins` have three options that allow you to refine searches that include the wildcard character. To refine your search results, select the default behavior, the `-hierarchical` option, or the `-compatibility` option.

The pipe character is used to separate one hierarchy level from the next in the TimeQuest analyzer. For example, <*absolute full cell name*>|<*pin suffix*> represents a hierarchical pin name with the "|" separating the hierarchy from the pin name.

When you use the collection commands `get_cells` and `get_pins` without an option, the default search behavior is performed on a per-hierarchical level of the pin name, that is, the search is performed level by level. A full hierarchical name may contain multiple hierarchical levels where a "|" is used to separate the hierarchical levels, and each wildcard character represents only one hierarchical level. For example, "*" represents the first hierarchical level and "*|*" represents the first and second hierarchical levels.

When you use the collection commands `get_cells` and `get_pins` with the `-hierarchical` option, a recursive match is performed on the relative hierarchical path name of the form <*short cell name*>|<*pin name*>. The search is performed on the node name, for example, the last hierarchy of the name, and not the hierarchy path. Unlike the default behavior, this option does not limit the search to each hierarchy level represented by the pipe character.

The pipe character cannot be used in the search with the `get_cells -hierarchical` option. The pipe character can be used with the `get_pins` collection search.

When you use the collection commands `get_cells` and `get_pins` with the `-compatibility` option, the search performed is similar to that of the Classic Timing Analyzer. This option searches the entire hierarchical path, and pipe characters are not treated as special characters.

Assuming the following cells exist in a design:

```
foo
foo|bar
```

and the following pin names:

```
foo|dataa
foo|datab
foo|bar|datac
foo|bar|datad
```

Table 6–26 shows the results of using these search strings.

Table 6–26. Sample Search Strings & Search Results

Search String	Search Result
`get_pins *|dataa`	`foo|dataa`
`get_pins *|datac`	*<empty>*
`get_pins *|*|datac`	`foo|bar|datac`
`get_pins foo*|*`	`foo|dataa, foo|datab`
`get_pins -hierarchy *|*|datac`	*<empty>* (1)
`get_pins -hierarchy foo|*`	`foo|dataa, foo|datab`
`get_pins -hierarchy *|datac`	`foo|bar|datac`
`get_pins -hierarchy foo|*|datac`	*<empty>* (1)
`get_pins -compatibility *|datac`	`foo|bar|datac`
`get_pins -compatibility *|*|datac`	`foo|bar|datac`

Note to Table 6–26:
(1) Due to the additional `*|*|` in the search string, the search result is *<empty>*.

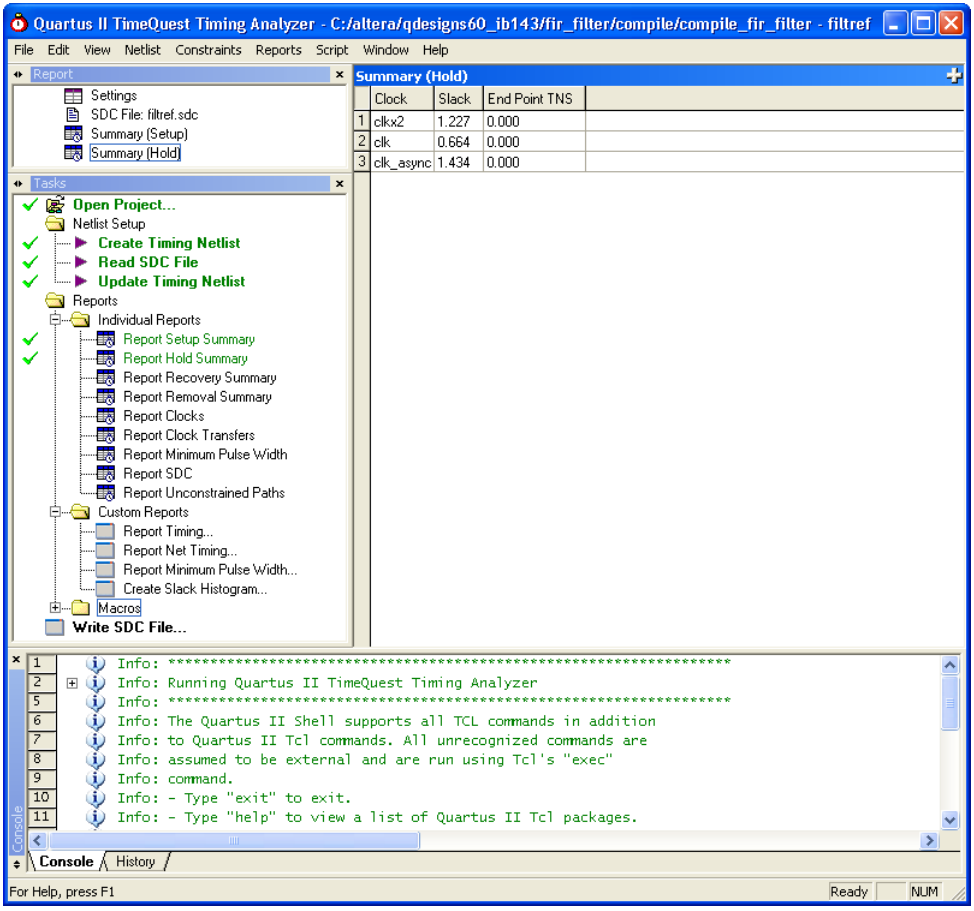
The TimeQuest Analyzer GUI

The TimeQuest analyzer provides an intuitive and easy-to-use GUI that allows you to efficiently constrain and analyze your designs. The GUI is divided into the following four panes:

- **View** pane
- **Tasks** pane
- **Console** pane
- **Report** pane

Each pane provides features that enhance productivity (Figure 6–25).

Figure 6–25. The TimeQuest Analyzer GUI

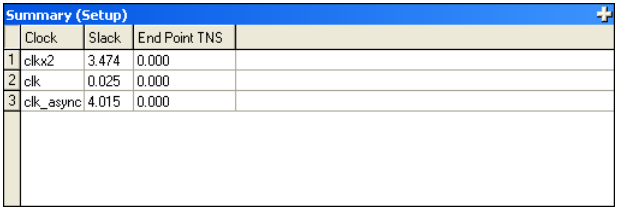


The following sections describe the four panes.

View Pane

The **View** pane is the main viewing area for the timing analysis results. You can use the **View** pane to view summary reports, custom reports, or histograms. Figure 6–26 shows the **View** pane after you select the Summary (Setup) report from the **Report** pane.

Figure 6–26. Summary (Setup) Report

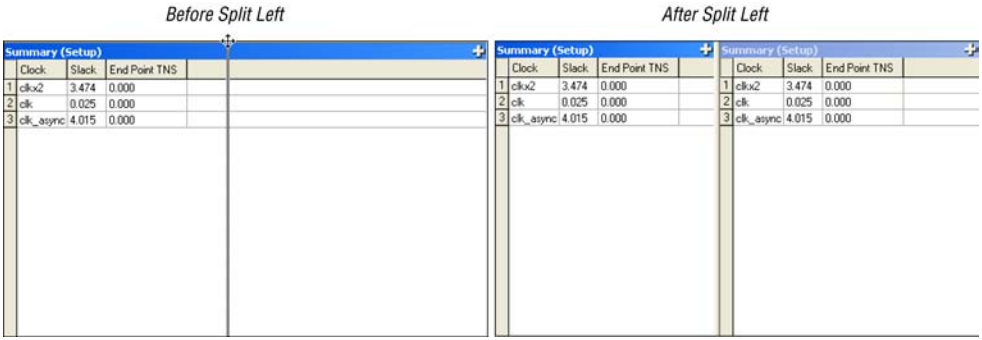


View Pane: Splitting

For the proper analysis of timing results, comparison of multiple reports is extremely important. To facilitate multiple report viewing, the **View** pane supports window splitting. Window splitting divides the **View** pane into multiple windows, allowing you to view different reports side-by-side.

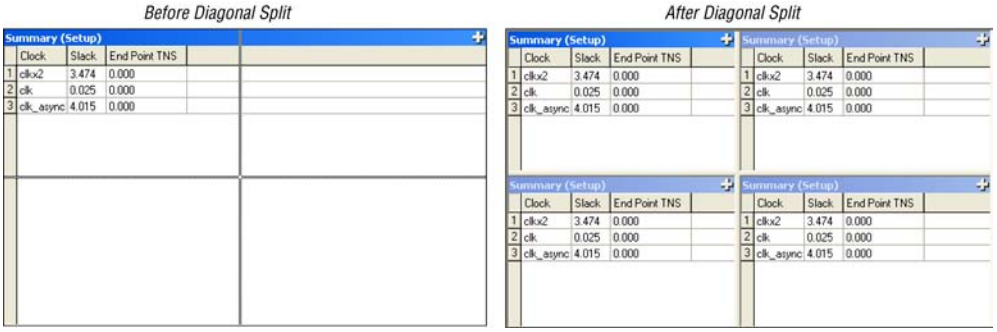
You can split the **View** pane into multiple windows using the split icon located in the upper right hand corner of the **View** pane. Drag the icon in different directions to generate additional window views in the **View** pane. For example, if you drag the split icon to the left, the **View** pane creates a new window to the right of the current window (Figure 6–27).

Figure 6–27. Splitting the View Pane to the Left



If you drag the split icon diagonally, the **View** pane creates three new windows in the **View** pane (Figure 6–28).

Figure 6–28. Splitting the View Pane Diagonally

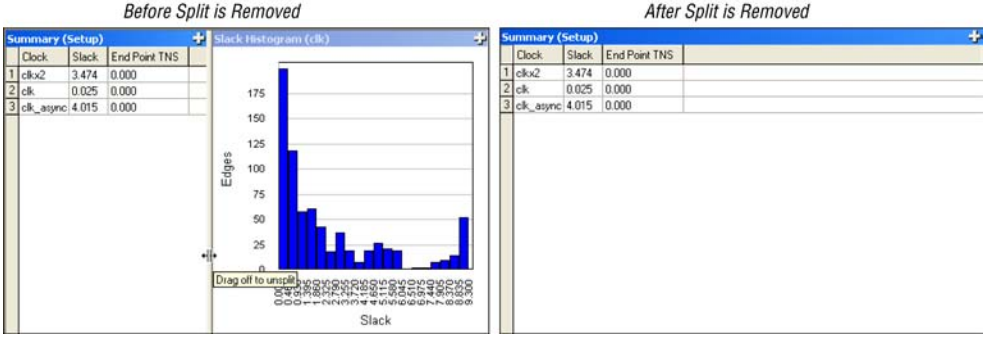


Drag the split icon downward to create a new window directly below the current window.

View Pane: Removing Split Windows

You can remove windows that you create in the **View** pane using the split icon by dragging the border of the window over the window you wish to remove (Figure 6–29).

Figure 6–29. Removing a Split Window



Tasks Pane

Use the **Tasks** pane to access common commands such as netlist setup report generation.

Two common commands are located in the **Tasks** pane: **Open Project** and **Write SDC File**. The other commands, including timing netlist setup and the generation of reports, are contained in the following folders:

- **Netlist Setup**
- **Reports**
- **Macros**

Each command in the **Tasks** pane has an equivalent Tcl command that is displayed in the **Console** pane when the command runs.

Opening a Project & Writing a Synopsys Design Constraints File

To open a project in the TimeQuest analyzer, double-click the **Open Project** task. If you launch the TimeQuest analyzer from the Quartus II software GUI, the project opens automatically.

You can add or remove constraints from the timing netlist after the TimeQuest analyzer reads the initial SDC file. After the file is read, the initial SDC file becomes outdated compared to the constraints in the TimeQuest analyzer. Use the **Write SDC File** command to generate an SDC file that is up-to-date and reflects the current state of constraints in the TimeQuest analyzer.

Netlist Setup Folder

The **Netlist Setup** folder contains tasks that are used to set up the timing netlist for timing analysis. The three tasks located in this folder are **Create Timing Netlist**, **Read SDC File**, and **Update Timing Netlist**.

Use the **Create Timing Netlist** task to create a netlist that the TimeQuest analyzer uses to perform static timing analysis. This netlist is used only for timing analysis by the TimeQuest analyzer.

You must always create a timing netlist before you perform static timing analysis with the TimeQuest timing analyzer.

You can use the **Read SDC File** command to apply constraints to the timing netlist. By default, the **Read SDC File** command reads the <*current revision*>**.sdc** file.

Use the `read_sdc` command to read an SDC file that is not associated with the current revision of the design.

You can use the **Update Timing Netlist** command to update the timing netlist after you enter constraints. You should use this command if any constraints are added or removed from the design.

Reports Folder

The **Reports** folder contains commands to generate timing summary reports of the static timing analysis results. The nine commands located in this folder are summarized in Table 6–27.

Table 6–27. Reports Folder Commands

Report Task	Description
Report Setup Summary	Generates a clock setup summary report for all clocks in the design.
Report Hold Summary	Generates a clock hold summary report for all clocks in the design.
Report Recovery Summary	Generates a recovery summary report for all clocks in the design.
Report Removal Summary	Generates a removal summary report for all clocks in the design.
Report Clocks	Generates a summary report of all created clocks in the design.
Report Clock Transfers	Generates a summary report of all clock transfers detected in the design.
Report Minimum Pulse Width	Generates a summary report of all minimum pulse widths in the design.
Report SDC	Generates a summary report of the constraints read from the SDC file.
Report Unconstrained Paths	Generates a summary report of all unconstrained paths in the design.

Macros Folder

The **Macros** folder contains commands that perform custom tasks available in the TimeQuest analyzer utility package. These commands are: **Report All Summaries**, **Report Top Failing Paths**, and **Create All Clock Histograms**.

Table 6–28 describes the commands available in the Macros folder.

Table 6–28. Macros Folder Commands

Macro Task	Description
Report All Summaries	This command runs the **Report Setup Summary**, **Report Hold Summary**, **Report Recovery Summary**, **Report Removal Summary**, and **Minimum Pulse Width** commands to generate all summary reports.
Report Top Failing Paths	This command generates a report containing a list of top failing paths.
Create All Clock Histograms	This command runs the **Create Slack Histogram** command to generate a clock histogram for all clocks in the design.

Console Pane

The **Console** pane is both a message center for the TimeQuest analyzer, and an interactive Tcl. The **Console** pane has two tabs: the **Console** tab and the **History** tab. All messages such as info and warning messages appear in this pane. Also, the **Console** tab allows you to enter and run Synopsys Design Constraints and Tcl commands. The **Console** tab shows the Tcl equivalent of all commands that you run in the **Tasks** pane. The **History** tab records all the Synopsys Design Constraints and Tcl commands that are run.

To run the commands located in the **History** tab after the timing netlist has been updated, right-click the command, and click **Rerun**.

You can copy Tcl commands from the **Console** and **History** tabs to easily generate Tcl scripts to perform timing analysis.

Report Pane

Use the **Report** pane to access all reports generated from the **Tasks** pane, and by any custom report commands. When you select a report in the **Report** pane, the report is shown in the active window in the **View** pane.

If a report is out-of-date with respect to the current constraints, a "?" icon is shown next to the report.

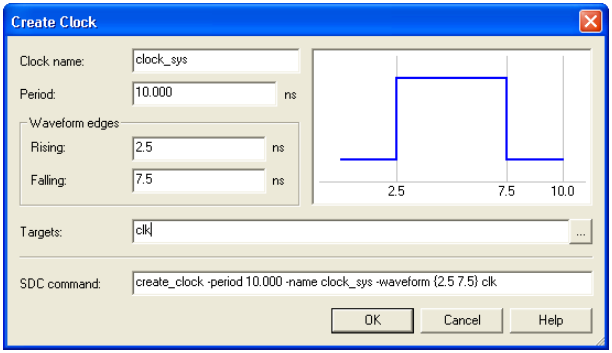
Constraints

You can use the Constraints menu to access commonly used constraints, exceptions, and commands. The following commands are available on the Constraints menu:

- **Create Clock**
- **Create Generated Clock**
- **Set Clock Latency**
- **Set Clock Uncertainty**
- **Remove Clock**

For example, you can use the **Create Clock** dialog box to create clocks in your design. Figure 6–30 shows the **Create Clock** dialog box.

Figure 6–30. Create Clock Dialog Box



The following commands specify timing exceptions, and are available on the Constraints menu:

- **Set False Path**
- **Set Multicycle Path**
- **Set Maximum Delay**
- **Set Minimum Delay**

All the dialog boxes used to specify timing constraints or exceptions from commands have an SDC command field. This field contains the SDC file constraint that is run when you click **OK**.

All commands and constraints created in the TimeQuest user interface are echoed in the **Console** pane.

The constraints specified with Constraints menu commands are not saved to the current SDC file automatically. You must run the **Write SDC File** command to save your constraints.

The following commands are available on the Constraints menu in the TimeQuest analyzer:

- **Generate SDC File from QSF**
- **Read SDC File**
- **Write SDC File**

The **Generate SDC File from QSF** command runs a Tcl script that converts the Classic Timing Analyzer constraints in a QSF file to an SDC file for the TimeQuest analyzer. The file <*current revision*>**.sdc** is created by this command.

For information about the **Generate SDC File from QSF** command, refer to the *Switching to the TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

The **Generate SDC File from QSF** command attempts to convert all timing constraints and exceptions in the QSF file to their equivalent SDC file constraints. However, not all QSF file constraints are convertible to SDC file constraints. Review the SDC file after it is created to ensure that all constraints have been successfully converted.

The **Read SDC File** command reads the <*current revision*>**.sdc** file.

When you select the **Write SDC File** command, an up-to-date SDC file that reflects the current state of constraints in the TimeQuest analyzer is generated.

Name Finder

Use the **Name Finder** dialog box to select the target for any constraints or exceptions in the TimeQuest analyzer GUI. The Name Finder allows you to specify collections, filters, and filter options. The **Collections** field in the **Name Finder** dialog box allows you to specify the type of name to select. To select the type, in the **Collection** list, select the desired collection API including:

- get_cells
- get_clocks
- get_keepers
- get_nets
- get_nodes
- get_pins
- get_ports
- get_registers

For more information on the various collection APIs, refer to "Collections" on page 6–46.

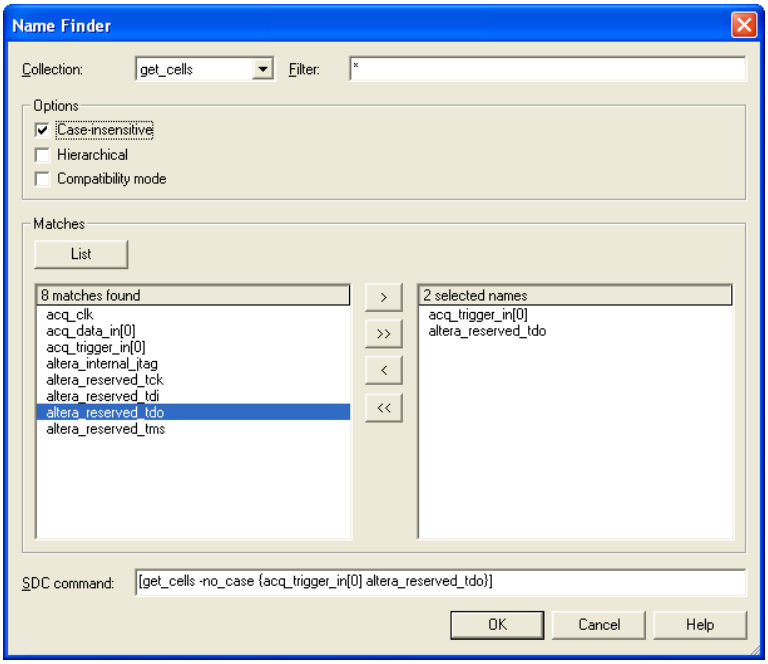
The **Filter** field allows you to filter names based on your own criteria including wildcards characters. You can further refine your results using the following filter options:

- Case-insensitive
- Hierarchical
- Compatibility mode

For more information on the filter options, refer to "Wildcard Assignments" on page 6–54.

The **Name Finder** dialog box also provides an SDC command field that displays the currently selected name search command. You can copy the value from this field and use it for other constraint target fields. The Name Finder dialog box is shown in Figure 6–31.

Figure 6–31. Name Finder Dialog Box



Conclusion

The Quartus II TimeQuest Timing Analyzer caters to the needs of complex designs–resulting in increased productivity and efficiency through its intuitive user interface, support of industry-standard constraints format, and scripting capabilities. TimeQuest is a next-generation timing analysis tool that supports the industry-standard SDC format and allows designers to create, manage, and analyze complex timing constraints, and to perform advanced timing verification.

7. Switching to the TimeQuest Timing Analyzer

QII53019-6.0.1

Introduction

The TimeQuest Timing Analyzer provides more powerful timing analysis features than the Classic Timing Analyzer. This chapter describes the benefits of switching to the TimeQuest Timing Analyzer, the differences between the TimeQuest and Classic Timing Analyzers, and the process you should follow to switch a design from the Classic Timing Analyzer to the TimeQuest Timing Analyzer.

Benefits of Switching to the TimeQuest Analyzer

Increasing design complexity requires a timing analysis tool with greater capabilities and flexibility. The TimeQuest Timing Analyzer offers the following benefits:

- Industry standard Synopsys Design Constraint (SDC) support makes you more productive.
- Simple, flexible reporting uses industry-standard terminology and makes timing sign-off faster.

For more detailed information about the features and capabilities of the TimeQuest Timing Analyzer, refer to the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

These features ease constraint and analysis of modern, complex designs. SDC constraints support complex clocking schemes, high-speed interfaces, and more logic. An example includes designs that have multiplexed clocks, regardless of whether they are switched on or off chip. Designs with source-synchronous interfaces, such as DDR memory interfaces, are much simpler to constrain and analyze with the TimeQuest Timing Analyzer.

To get started using the TimeQuest Timing Analyzer, there are three main differences between the Classic and TimeQuest analyzers. With the TimeQuest Timing Analyzer:

- All clocks are related by default. ("Related & Unrelated Clocks" on page 7–13.)
- The default hold multicycle value is zero. ("Hold Multicycle" on page 7–24.)
- You must constrain all ports and ripple clocks. ("Automatic Clock Detection" on page 7–19.)

Chapter Contents

Switching to the TimeQuest Analyzer

You should use the following process to switch a design from the Classic Timing Analyzer to the TimeQuest Timing Analyzer. The process is composed of the following steps, which are described in detail in the next sections:

1. Compile your design and perform timing analysis with the Classic Timing Analyzer (page 7–2).
2. Create an SDC file that contains timing constraints (page 7–3).
3. Perform timing analysis with the TimeQuest Timing Analyzer and examine the reports (page 7–4).
4. Set the default timing analyzer to TimeQuest (page 7–4).

Compile Your Design

To begin, compile your design with the Quartus® II software. You should run the Classic Timing Analyzer during compilation because it is easier to convert your assignments to SDC constraints when you create an SDC file. To run the Classic Timing Analyzer in the Quartus II GUI, from the Processing menu, click **Start**, then click **Start Timing Analyzer**. To run the Classic Timing Analyzer if you are a command-line user, type `quartus_tan` <*project*> ↵ at a system command prompt.

Create an SDC File

The TimeQuest Timing Analyzer supports SDC format constraints. If you are familiar with SDC terminology, you can create an SDC file with any text editor and skip to "Perform Timing Analysis with the TimeQuest Timing Analyzer" on page 7–4. Name the SDC file <*revision*>**.sdc** (<*revision*> is the current revision of your project) and save it in your project directory.

Refer to the *SDC and TimeQuest Tcl API Reference Manual* for a TimeQuest SDC command reference.

Alternately, you can use a TimeQuest conversion utility to help you convert the timing assignments in an existing QSF file to corresponding SDC constraints.

Conversion Utility

To run the conversion utility from the TimeQuest GUI, click **Generate SDC file from QSF** on the Constraints menu. To run the conversion utility from the Tcl prompt in the TimeQuest Tcl shell, type `tan2sdc::convert <revision>.sdc` ↵, where <*revision*> is the current revision of your project. You can also run the conversion utility from a system command prompt with the following command: `quartus_sta --qsf2sdc <project name>` ↵. The SDC file created by the conversion utility is named <*revision*>**.sdc**.

For information about how to run the TimeQuest Timing Analyzer, refer to "Run the TimeQuest Analyzer" on page 7–4.

If you use the conversion utility, you must review the SDC file to ensure it is correct and complete, and make changes if necessary. Refer to "Constraint File Priority" on page 7–10 for the recommended way to make changes.

The conversion utility cannot convert some types of Classic assignments because:

- No corresponding SDC constraint exists
- Multiple SDC constraints are valid, so correct conversion requires knowledge of the intended function of your design
- You have not performed timing analysis with the Classic Timing Analyzer, and the conversion utility cannot read some timing reports

You must manually convert any such assignments based on the guidelines in "Timing Assignment Conversion" on page 7–32.

Perform Timing Analysis with the TimeQuest Timing Analyzer

When your SDC file is complete, use the reporting capabilities in the TimeQuest Timing Analyzer. If you use the TimeQuest GUI, double-click any of the reports listed in the **Task** pane. You can also type commands in the TimeQuest Tcl shell to generate reports.

You should also review "Notes" on page 7–69 to ensure the TimeQuest Timing Analyzer supports all stages of your design flow.

For complete information about how to use the TimeQuest Timing Analyzer, and descriptions of commands and reports, refer to the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*, and the *SDC and TimeQuest Tcl API Reference Manual*.

Run the TimeQuest Analyzer

If you are using the Quartus II software, to open the TimeQuest GUI, on the Tools menu, click **TimeQuest Timing Analyzer**. The TimeQuest GUI automatically opens the project you have open in the Quartus II GUI.

If you use the system command prompt to open the TimeQuest Timing Analyzer, type `quartus_staw` ↵ to open the TimeQuest GUI, or type `quartus_sta -s` ↵ to start the TimeQuest Timing Analyzer in Tcl shell mode. Use the **project_open** command to open your project, or, on the File menu, click **Open Project**.

Set the Default Timing Analyzer

To use the TimeQuest Timing Analyzer as the default timing analyzer for your project, turn on **Use TimeQuest Timing Analyzer during compilation**. In the Quartus II GUI, click **Settings** in the Assignments menu, expand **Compilation Process Settings**, then click **Timing Analysis Processing** and turn on **Use TimeQuest Timing Analyzer during compilation**. You can make the same setting in your project's QSF file with the following Tcl command:

```
set_global_assignment -name \
USE_TIMEQUEST_TIMING_ANALYZER ON
```

This setting directs the Quartus II software to use the TimeQuest Timing Analyzer, instead of the Classic Timing Analyzer.

The setting to make the TimeQuest Timing Analyzer the default Timing Analyzer is specific to each project, so you can decide on a per-project basis whether to use the TimeQuest Timing Analyzer or the Classic Timing Analyzer.

If you want to use the Classic Timing Analyzer instead of the TimeQuest Timing Analyzer, ensure the **Use TimeQuest Timing Analyzer during compilation** setting is off. You can delete the <*revision*>**.sdc** file, because the Classic Timing Analyzer does not use it.

In the Quartus II software, a timing analyzer performs two functions:

- Processing timing constraints and exceptions that affect how your design is placed and routed
- Reporting after place and route is complete so you know whether the design meets timing requirements

Although you can use one timing analyzer to process timing constraints during place and route and the other for reporting, you should use the same timing analyzer for both. The Classic Timing Analyzer uses assignments in the QSF file, and the TimeQuest Timing Analyzer uses constraints in the SDC file. Any differences between the timing assignments in the two files may cause different results.

Differences Between TimeQuest & Classic Timing Analyzers

The TimeQuest Timing Analyzer is different from the Classic Timing Analyzer in the following ways:

- Terminology (page 7–5)
- Constraints (page 7–7)
- Clocks (page 7–13)
- Hold Multicycle (page 7–24)
- Fitter Behavior (page 7–27)
- Reporting (page 7–27)
- Scripting API (page 7–31)

Terminology

This section introduces the industry-standard SDC terminology that the TimeQuest Timing Analyzer uses.

For more detailed information on this terminology, refer to the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Netlist

The TimeQuest Timing Analyzer uses SDC naming conventions for netlists. Netlists consist of cells, pins, nets, ports, and clocks.

- Cells are instances of fundamental hardware elements in Altera® FPGAs (such as logic elements, look-up tables, and registers).
- Pins are inputs and outputs of cells.

- Nets are connections between output pins and input pins.
- Ports are top-level module inputs and outputs (device inputs and outputs).
- Clocks are abstract objects outside the netlist.

The terminology of pins and ports is opposite to that of the Classic Timing Analyzer. In the Classic Timing Analyzer, ports are inputs and outputs of cells, and pins are top-level module inputs and outputs (device inputs and outputs).

Figure 7–1 shows a simple design, and Figure 7–2 shows the TimeQuest netlist representation of the design. Netlist elements in Figure 7–2 are labeled to illustrate the SDC terminology.

Figure 7–1. Sample Design

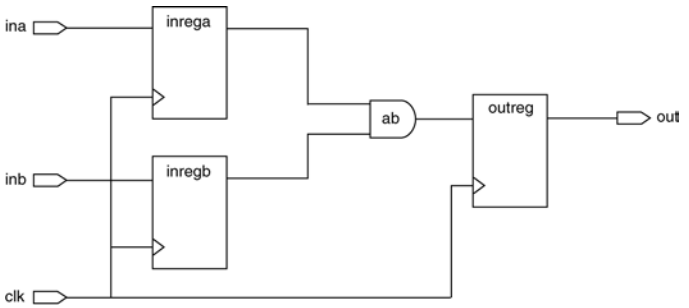
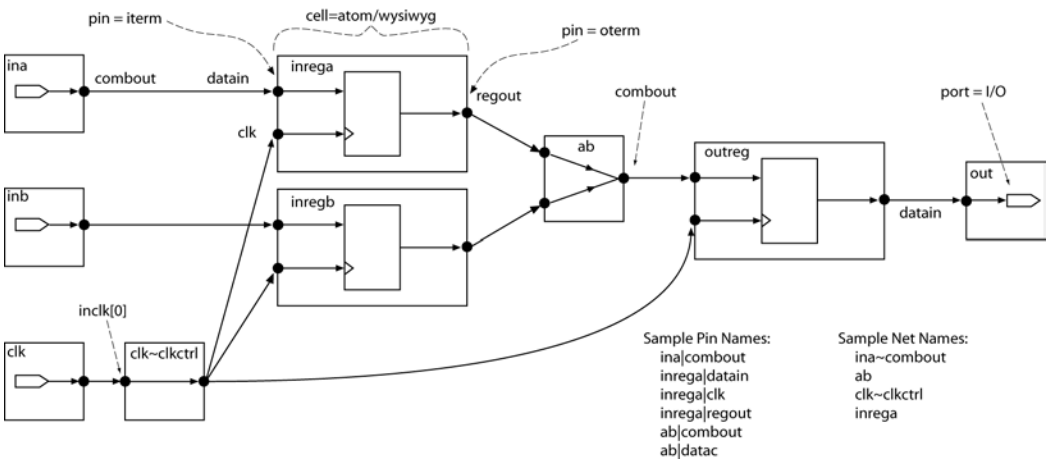


Figure 7–2. TimeQuest Timing Analyzer Netlist



Collections

In addition to standard SDC collections, the TimeQuest Timing Analyzer supports the following Altera-specific collection types:

- **Keepers**—Non-combinational nodes in a netlist
- **Nodes**—Nodes can be combinational, registers, latches, or ports (device inputs and outputs)
- **Registers**—Registers or latches in the netlist

You can use the **get_keepers**, **get_nodes**, or **get_registers** commands to access these collections.

Constraints

The Classic and TimeQuest Timing Analyzers store constraints in different files, support different methods for constraint entry, and prioritize constraints differently. The following sections detail these differences.

Constraint Files

The TimeQuest Timing Analyzer stores all SDC timing constraints in SDC files. The Classic Timing Analyzer stores all timing assignments in your project's Quartus II Settings File (QSF) file. The QSF file contains all your project's assignments and settings except for the TimeQuest constraints. The TimeQuest Timing Analyzer ignores the timing assignments in your QSF file except when the conversion utility converts Classic QSF timing assignments to TimeQuest SDC constraints. There is no automatic process that keeps timing constraints synchronized between your QSF and SDC files. If you want to keep the constraints synchronized, you must convert them manually.

Constraint Entry

In the Classic Timing Analyzer, you enter timing assignments with the Settings dialog box, the Assignment Editor, or with commands in Tcl scripts. The TimeQuest Timing Analyzer does not use the Assignment Editor for its constraints, and you cannot use the Assignment Editor to enter SDC constraints. You must use one of the following methods to enter TimeQuest constraints:

- Enter constraints at the Tcl prompt in the TimeQuest Timing Analyzer
- Enter constraints in an SDC file with a text editor
- Use the constraint entry commands on the Constraints menu in the TimeQuest GUI

You can enter timing assignments for the Classic Timing Analyzer even if no timing netlist exists for your design. The TimeQuest Timing Analyzer requires that a netlist exist for interactive constraint entry because the TimeQuest Timing Analyzer validates all names when you enter each constraint. You must create a timing netlist in the TimeQuest Timing Analyzer before you can enter constraints with either of the following interactive methods:

- At the Tcl console of the TimeQuest Timing Analyzer
- With commands on the Constraints menu in the TimeQuest GUI

If you enter constraints with a text editor separate from the TimeQuest Timing Analyzer, no timing netlist is required.

To create a timing netlist in the TimeQuest Timing Analyzer, use the **create_timing_netlist** command, or double-click **Create Timing Netlist** in the Task pane of the TimeQuest GUI.

If you have never compiled your design, and you want to use the TimeQuest Timing Analyzer to enter constraints interactively, you must synthesize your design before you create a timing netlist. To synthesize your design, type `quartus_map` <*project name*> ↵ at a system command prompt, or, if you use the Quartus II GUI, ensure that your project is open, then click **Start** on the Processing menu, and click **Start Analysis & Synthesis**.

To create the netlist, open the TimeQuest Timing Analyzer. Then, on the Netlist menu, click **Create Timing Netlist...**, select **Post-map**, and click **OK**. Alternately, type `create_timing_netlist -post_map` ↵ at the Tcl Console.

Time Units

Enter time values are in default time units of nanoseconds (ns) with up to three decimal places. Note that the TimeQuest Timing Analyzer does not display the default time unit when it displays time values.

You can specify a different default time unit with the **set_time_format -unit** <*default time unit*> command, or specify another unit when you enter a time value, for example, `300ps`.

Specifying time units with the value is not part of the standard SDC format. This is a TimeQuest extension.

You can specify clock constraints with period or frequency in the TimeQuest Timing Analyzer. For example, you can use either of the following constraints:

- `create_clock -period 10.000`
  (assuming default units and decimal places)
- `create_clock -period "100 MHz"`
- `create_clock -period "10 ns"`

MegaCore Functions

If you change any MegaCore function settings and regenerate the core after you convert your timing assignments to SDC constraints, you must manually update the SDC constraints or reconvert your assignments. You must update or reconvert, because changes to MegaCore function settings can affect timing assignments embedded in the hardware description language files of the core. The timing assignments are not converted automatically when the core settings change.

You should make a backup copy of your SDC file before reconverting assignments. If you made changes to the SDC file, you can manually copy the updated MegaCore timing constraints to your SDC file.

Bus Name Format

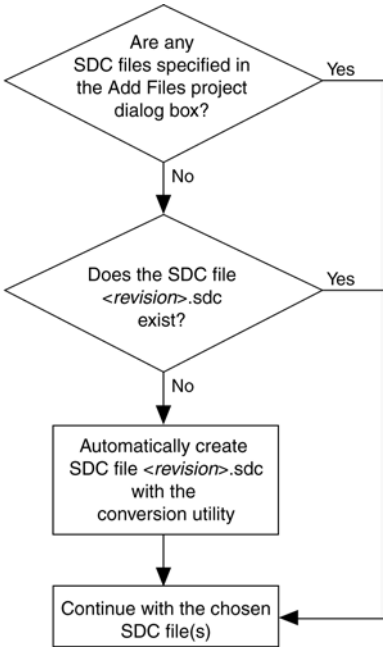
In the Classic Timing Analyzer, you can make a timing assignment to all bits in a bus with the bus name (or the bus name followed by an asterisk enclosed in square brackets) as the target. For example, to make an assignment to all bits of a bus called address, use `address` or `address[*]` as the target of the assignment.

In the TimeQuest Timing Analyzer, you must use the bus name followed by square brackets enclosing an asterisk, like this: `address[*]`.

Constraint File Priority

The TimeQuest Timing Analyzer searches for SDC files with a specific priority, shown in Figure 7–3.

Figure 7–3. SDC File Search Order



If you specify constraints in multiple SDC files, or if you use a single SDC file with a name other than <*revision*>**.sdc**, you must add the files to your project so the TimeQuest Timing Analyzer can find them. If you use the Quartus II software, click **Add/Remove Files in Project** on the Project menu, and add the appropriate SDC files. You can also add SDC files to your project with the following Tcl command in your QSF file, repeated once for each SDC file:

```
set_global_assignment -name SDC_FILE <SDC file name>
```

The TimeQuest Timing Analyzer reads constraint files from the files list in the order they are listed, first to last.

If you use an SDC file created by the conversion utility, you should place it before all other SDC files in the list of files. When conflicting constraints apply to the same node, the last constraint has the highest priority. Therefore, SDC files with your additions or changes should be listed after the SDC file created by the conversion utility, so your constraints have higher priority.

The TimeQuest Timing Analyzer automatically runs the conversion utility to create an SDC file when it must read an SDC file, and it cannot find one according to the priority shown in Figure 7–3 on page 7–10. When you use the TimeQuest GUI, the analyzer reads an SDC file in the Read SDC File task in the **Task** pane.

You must review the SDC file as you would when manually running the conversion utility. Refer to "Reviewing Conversion Results" on page 7–65 for information about how to review the converted constraints.

If no SDC file exists when you run the Quartus II Fitter, and you have turned on **Use TimeQuest Timing Analyzer during compilation**, the Fitter does not create an SDC file automatically, but it attempts to meet a default 1 GHz constraint on all clocks in your design.

Constraint Priority

The Classic Timing Analyzer prioritizes assignments based on the specificity of the nodes to which they are assigned. The more specific an assignment is, the higher its priority. The TimeQuest Timing Analyzer simplifies these precedence rules. When overlaps occur in the nodes to which the constraints apply, constraints at the bottom of the file take priority over constraints at the top of the file.

As an example, in the Classic Timing Analyzer, point-to-point multicycle assignments have higher priority than single point multicycle assignments. The two assignments in Example 7–1 result in a multicycle assignment of 2 between `A_reg` and all nodes beginning with B, including `B_reg`. The single point assignment does not apply to paths from `A_reg` to `B_reg`, because the specific point-to-point assignment takes priority over the general single point assignment.

Example 7–1. Classic Multicycle Assignments

```
set_instance_assignment -name MULTICYCLE -from A_reg -to B* 2
set_instance_assignment -name MULTICYCLE -to B_reg 3
```

Example 7–2 shows SDC versions of the Classic timing assignments above. However, the TimeQuest Timing Analyzer evaluates the constraints top to bottom (regardless of point-to-point or single point), so the path from A_reg to B_reg receives a multicycle exception of 3 because it is second in order.

Example 7–2. TimeQuest Multicycle Exceptions

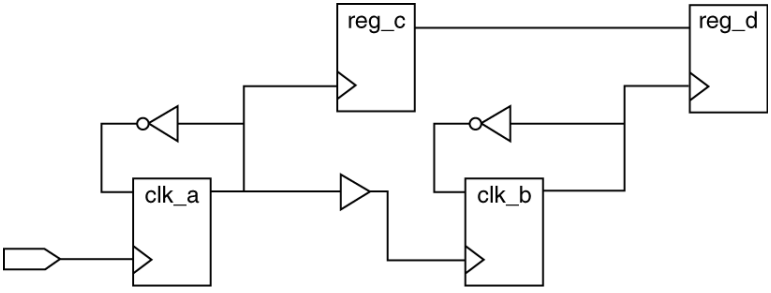
```
set_multicycle_path -from [get_keepers A_reg] -to [get_keepers B*] 2
set_multicycle_path -to [get_keepers B_reg] 3
```

Ambiguous Constraints

Because of new capabilities in the TimeQuest Timing Analyzer, some classic assignments can be ambiguous after the conversion utility converts them, and you should update them by hand using your knowledge of your design.

Figure 7–4 shows a ripple clock circuit, and the explanation that follows shows an ambiguous constraint for that circuit, and how to edit the constraint to remove the ambiguity in the TimeQuest Timing Analyzer.

Figure 7–4. Ripple Clock Circuit



In the Classic Timing Analyzer, the following QSF multicycle assignment from clk_a to clk_b with a value of 2 applies to paths transferring data from the clk_a domain to the clk_b domain.

```
set_instance_assingment -name MULTICYCLE -from clk_a -to clk_b 2
```

In Figure 7–4, this assignment applies to the path from reg_c to reg_d. In the TimeQuest Timing Analyzer, the use of the clock node names in the following equivalent multicycle exception is ambiguous.

```
set_multicycle_path -setup -from clk_a -to clk_b 2
```

The exception could apply to the path between clk_a and clk_b, or it could apply to paths from one ripple clock domain to the other ripple clock domain (reg_c to reg_d).

The TimeQuest exceptions shown in Example 7–3 are not ambiguous because they use collections to explicitly specify the targets of the exception.

Example 7–3. Unambiguous TimeQuest Exceptions

```
# Applies to path from reg_c to reg_d
set_multicycle_path -setup -from [get_clocks clk_a] \
    -to [get_clocks clk_b] 2
# Applies to path from clk_a to clk_b
set_multicycle_path -setup -from [get_registers clk_a] \
    -to [get_registers clk_b] 2
```

Clocks

The Classic and TimeQuest Timing Analyzers detect, analyze, and report clocks differently. The following sections describe these differences.

Related & Unrelated Clocks

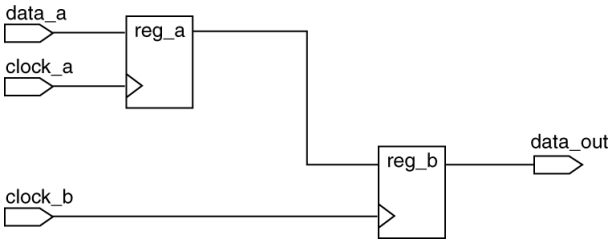
In the TimeQuest Timing Analyzer, all clocks are related by default, and you must add assignments to indicate unrelated clocks. However, in the Classic Timing Analyzer, all base clocks are unrelated by default. All derived clocks of a base clock are related to each other, but are unrelated to other base clocks and their derived clocks.

You can change the default behavior of the Classic Timing Analyzer to treat all clocks as related clocks. On the Assignments menu, click **Timing Analysis Settings**. Click **More Settings** and then select **Cut paths between unrelated clock domains**. Ensure that the setting is off.

Figure 7–5 on page 7–14 shows a simple circuit with a path between two clock domains. The TimeQuest Timing Analyzer analyzes the path from reg_a to reg_b because all clocks are related by default. The Classic Timing Analyzer does not analyze the path from reg_a to reg_b by default.

If you use the conversion utility to create an SDC file, and you have not changed the default Classic Timing Analyzer behavior, this difference may cause slack reporting discrepancies between the TimeQuest and Classic Timing Analyzers.

Figure 7–5. Cross Clock Domain Path



To make clocks unrelated in the TimeQuest Timing Analyzer, use the **set_clock_groups** command with the `-exclusive` option. For example, the following command makes `clock_a` and `clock_b` unrelated, so the TimeQuest Timing Analyzer does not analyze paths between the two clock domains.

```
set_clock_groups -exclusive -group {clock_a} -group {clock_b}
```

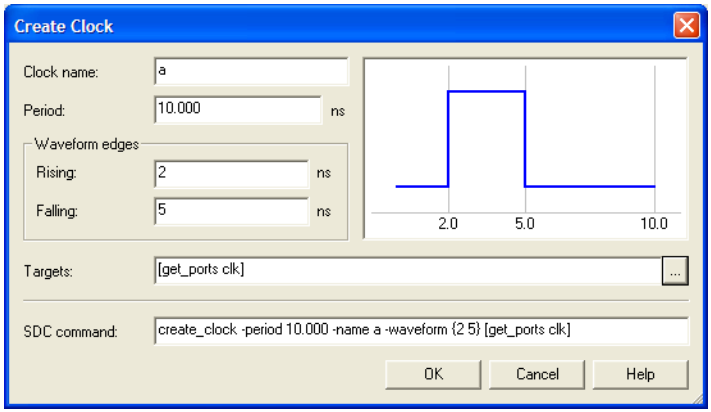
Clock Offset

In the TimeQuest Timing Analyzer, clocks can have non-zero values for the rising edge of the waveform, a feature that the Classic Timing Analyzer does not support. To specify an offset for your clock, use the waveform option for the **create_clock** command to specify the rising and falling edge times, as shown in this example:

`-waveform {`*<rising edge time>* *<falling edge time>*`}`

Figure 7–6 shows a clock constraint with an offset in the TimeQuest GUI.

Figure 7–6. Create Clock Screen



Clock offset affects setup and hold relationships. Launch and latch edges are evaluated after offsets are applied. Depending on the offset, the setup relationship can be the offset value, or the difference between the period and offset. You should not use clock offset to emulate latency. You should use the clock latency constraint instead. Refer to "Offset & Latency Example" on page 7–16 for an example that illustrates the different effects of offset and latency.

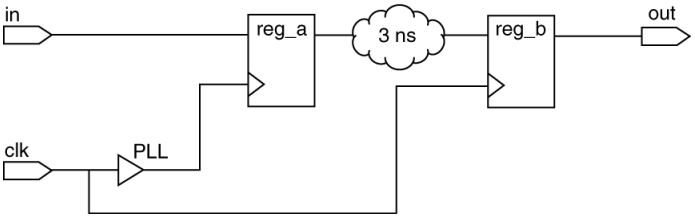
Clock Latency

The TimeQuest Timing Analyzer does not ignore early clock latency and late clock latency differences when the clock source is the same, as the Classic Timing Analyzer does. When you specify latencies, you should take common clock path pessimism into account and use uncertainty to control pessimism differences for clock-to-clock data transfers. Unlike clock offset, clock latency affects skew, and launch and latch edges are evaluated before latencies are applied, so the setup relationship is always equal to the period.

Offset & Latency Example

Figure 7–7 shows a simple register-to-register circuit to used to illustrate the different effects of offset and latency. The examples show why you should not use clock offset to emulate clock latency. You should always turn on "Enable Clock Latency" in the Classic analyzer. This option is in the **More Settings** part of the Timing Settings dialog box.

Figure 7–7. Simple Circuit for Offset & Latency Examples

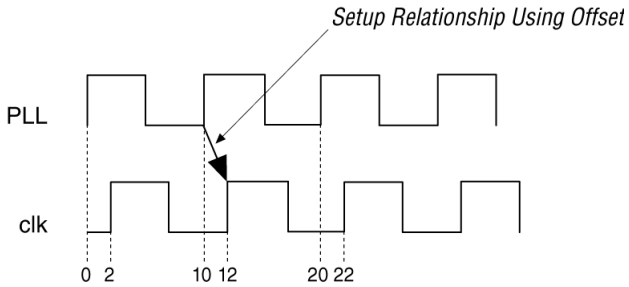


The period for `clk` is 10 ns, and the period for the PLL output is 10 ns. The PLL compensation value is –2 ns. The network delay from the PLL to `reg_a` equals the network delay from `clk` to `reg_b`. Finally, the delay from `reg_a` to `reg_b` is 3 ns.

Clock Offset Scenario

Treat the PLL compensation value of –2 ns as a clock offset of –2 ns with a clock skew of 0 ns. Launch and latch edges are evaluated after offsets are applied, so the setup relationship is 2 ns (Figure 7–8).

Figure 7–8. Setup Relationship Using Offset



Equation 1 shows how to calculate the slack value for the path from reg_a to reg_b.

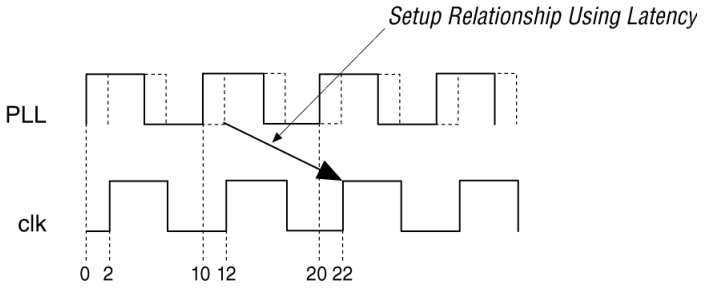
(1)
```
slack = clock arrival – data arrival
slack = setup relationship + clock skew – reg_to_reg delay
slack = 2 ns + 0 ns – 3 ns
slack = -1 ns
```

The negative slack requires a multicycle assignment with a value of 2 and a hold multicycle assignment with a value of 1 to correct. With these assignments from reg_a to reg_b, the setup relationship is then 12 ns, resulting in a slack of 9 ns.

Clock Latency Scenario

Treat the PLL compensation value of –2 ns as latency with a clock skew of 2 ns. Because launch and latch edges are evaluated before latencies are applied, the setup relationship is 10 ns (the period of clk and the PLL) (Figure 7–9).

Figure 7–9. Setup Relationship Using Latency



Equation 2 shows how to calculate the slack value for the path from reg_a to reg_b.

(2)
```
slack = clock arrival – data arrival
slack = setup relationship + clock skew – reg_to_reg delay
slack = 10 ns + 2 ns – 3 ns
slack = 9 ns
```

The slack of 9 ns is identical to the slack computed in the previous example, but because this example uses latency instead of offset, no multicycle assignment is required.

Clock Uncertainty

The Classic Timing Analyzer ignores **Clock Setup Uncertainty** and **Clock Hold Uncertainty** assignments when you specify a setup or hold relationship between two clocks. However, the TimeQuest Timing Analyzer does not ignore clock uncertainty when you specify a setup or hold relationship between two clocks. Figure 7–10 and Figure 7–11 illustrate the different behavior between the TimeQuest and Classic Timing Analyzers.

In both figures, the constraints are identical. There is a 20-ns period for `clk_a` and `clk_b`. There is a setup relationship (a **set_max_delay** exception in the TimeQuest Timing Analyzer) of 7 ns from `clk_a` to `clk_b`, and a clock setup uncertainty constraint of 1 ns from `clk_a` to `clk_b`. The actual setup relationship in the TimeQuest Timing Analyzer is 1 ns less than in the Classic Timing Analyzer because of the way they analyze clock uncertainty.

Figure 7–10. Classic Timing Analyzer Behavior

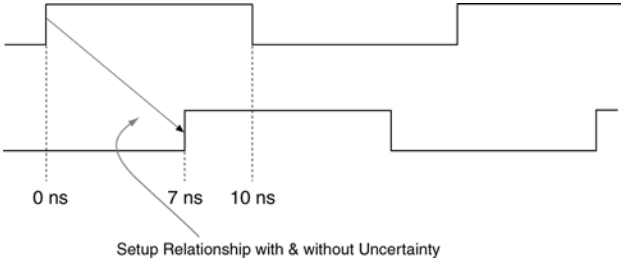
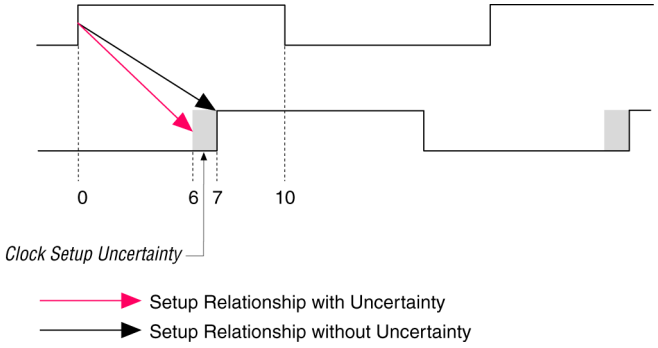


Figure 7–11. TimeQuest Timing Analyzer Behavior



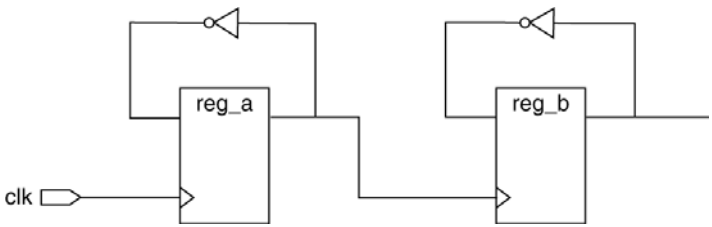
Derived & Generated Clocks

Generated clocks in the TimeQuest Timing Analyzer are different than derived clocks in the Classic Timing Analyzer. In the Classic Timing Analyzer, the source of a derived clock must be a base clock. However, in the TimeQuest Timing Analyzer, the source of a generated clock can be any other clock in the design (including virtual clocks), or any node to which a clock propagates through the clock network. Because generated clocks are related through the clock network, you can specify generated clocks for isolated modules, such as IP, without knowing the details of the clocks outside of the module.

In the TimeQuest Timing Analyzer, you can specify generated clocks relative to specific edges and edge shifts of a master clock, a feature that the Classic Timing Analyzer does not support.

Figure 7–12 shows a simple ripple clock that you should constrain with generated clocks in the TimeQuest Timing Analyzer.

Figure 7–12. Generated Clocks Circuit



The TimeQuest constraints shown in Example 7–4 constrain the clocks in the circuit above. Note that the source of each generated clock can be the input pin of the register itself, not the name of another clock.

Example 7–4. Generated Clock Constraints

```
create_clock -period 10 -name clk clk
create_generated_clock -divide_by 2 -source reg_a|CLK -name reg_a reg_a
create_generated_clock -divide_by 2 -source reg_b|CLK -name reg_b reg_b
```

Automatic Clock Detection

The Classic and TimeQuest Timing Analyzers identify clock sources of registers that do not have a defined clock source. The Classic Timing Analyzer traces back along the clock network, through registers and

logic, until it reaches a top-level port in your design. The TimeQuest Timing Analyzer also traces back along the clock network, but it stops at registers.

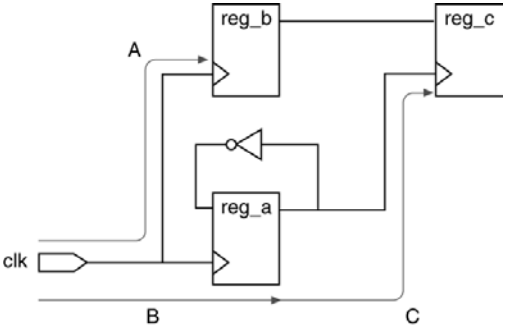
You can use two SDC commands in the TimeQuest Timing Analyzer to automatically detect and create clocks for unconstrained clock sources:

- **derive_clocks**—creates clocks on sources of clock pins that do not already have at least one clock sourcing the clock pin
- **derive_pll_clocks**—identifies PLLs and creates generated clocks on the clock output pins

derive_clocks Command

Figure 7–13 shows a simple circuit with a divide-by-2 register and indicates the clock network delays as A, B, and C. The following explanation describes how the Classic and TimeQuest Timing Analyzers detect the clocks in Figure 7–13.

Figure 7–13. Circuit for derive_clocks Example



The Classic Timing Analyzer detects that `clk` is the clock source for registers `reg_a`, `reg_b`, and `reg_c`. It detects that `clk` is the clock source for `reg_c` because it traces back along the clock network for `reg_c` through `reg_a`, until it finds the `clk` port. The Classic Timing Analyzer computes the clock arrival time for `reg_c` as B +C.

The **derive_clocks** command in the TimeQuest Timing Analyzer creates two base clocks, one on the `clk` port and one on `reg_a`, because the command does not trace through registers on the clock network. The clock arrival time for `reg_c` is C because the clock starts at `reg_a`.

To make the TimeQuest Timing Analyzer compute the same clock arrival time (B +C) as the Classic Timing Analyzer for **reg_c**, modify the clock constraints created by the **derive_clocks** command as follows:

- Change the base clock named `reg_a` to a generated clock
- Make the source the clock pin of `reg_a` (`reg_a|CLK`) or the port `clk`
- Add a `-divide_by 2` option

This makes the clock arrival times to `reg_c` match between the Classic Timing Analyzer and TimeQuest Timing Analyzer. However, the clock for `reg_c` is shown as `reg_a` instead of clk, and the launch and latch edges may change for some paths due to the divide-by-2.

You can use the **derive_clocks** command at the beginning of your design cycle when you do not know all of the clock constraints for your design, but you should not use it during timing sign-off. Instead, you should constrain each clock in your design with the **create_clock** or **create_generated_clocks** commands.

The **derive_clocks** command detects clocks in your design using the following rules:

1. An input clock port is detected as a clock only if there are no other clocks feeding the destination registers.

    a. Input clock ports are not detected automatically if they feed only other base clocks.

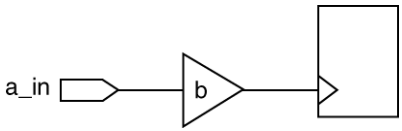
    b. If other clocks feed the port's register destinations, the port is assumed to be an enable or data port for a gated clock.

    c. When no clocks are defined, and multiple clocks feed a destination register, the auto-detected clock is selected arbitrarily.

2. All ripple clocks (registers in a clock path) are detected as clocks automatically using the same rules for input clock ports. If both an input port and a register feed register clock pins, the input port is selected as the clock.

The following examples show how the **derive_clocks** command detects clocks in the simple circuit shown in Figure 7–14.

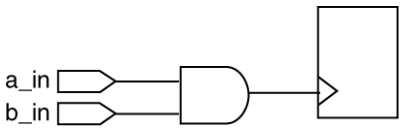
Figure 7–14. Simple Circuit 1



- If you do not make any clock settings, then you run **derive_clocks**, it detects `a_in` as a clock according to rule 1, because there are no other clocks feeding the register.
- If you create a clock with `b` as its target, then run **derive_clocks**, it does not detect `a_in` as a clock according to rule 1a, because `a_in` feeds only another clock.

The following examples show how the **derive_clocks** command detects clocks in the simple circuit shown in Figure 7–15.

Figure 7–15. Simple Circuit 2



- If you do not make any clock settings and you then run **derive_clocks**, it selects a clock arbitrarily, according to rule 1c.
- If you create a clock with `a_in` as its target and then run **derive_clocks**, it does not detect `b_in` as a clock according to rule 1b, because another clock (`a_in`) feeds the register.

derive_pll_clocks Command

The **derive_pll_clocks** command names the generated clocks according to the names of the PLL output pins by default, and you cannot change these generated clock names. If you want to use your own clock names, you must use the **create_generated_clock** command for each PLL output clock and specify the names with the `-name` option.

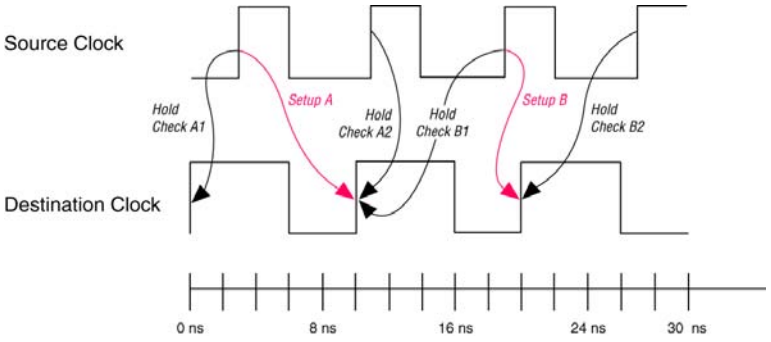
If you use the PLL clock-switchover feature, the **derive_pll_clocks** command creates additional generated clocks on each output clock pin of the PLL based on the secondary clock input to the PLL. This may require

set_clock_groups or **set_false_path** commands to cut the primary and secondary clock outputs. For information about how to make clocks unrelated, refer to "Related & Unrelated Clocks" on page 7–13.

Hold Relationship

The TimeQuest and Classic Timing Analyzers choose the worst-case hold relationship differently. Refer to Figure 7–16 for sample waveforms to illustrate the different effects.

Figure 7–16. Worst-Case Hold



The Classic Timing Analyzer first identifies the worst-case setup relationship. The worst-case setup relationship is **Setup B**. Then the Classic Timing Analyzer chooses the worst-case hold relationship (Hold Check B1 or Hold Check B2) for that specific setup relationship, Setup B. The Classic Timing Analyzer chooses Hold Check B2 for the worst-case hold relationship.

However, the TimeQuest Timing Analyzer calculates worst-case hold relationships for all possible setup relationships and chooses the absolute worst-case hold relationship. The TimeQuest Timing Analyzer checks two hold relationships for every setup relationship:

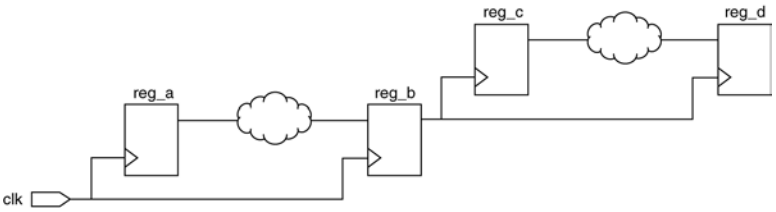
- Data launched by the current launch edge not captured by the previous latch edge (Hold Check A1 and Hold Check B1)
- Data launched by the next launch edge not captured by the current latch edge (Hold Check A2 and Hold Check B2)

The TimeQuest Timing Analyzer chooses Hold Check A2 as the absolute worst-case hold relationship.

Clock Objects

The Classic analyzer treats nodes with clock settings assigned to them as special objects in the timing netlist. Any node in the timing netlist with a clock setting is treated as a clock object, regardless of its actual type, such as a register. When a register has a clock setting assigned to it, the Classic analyzer does not analyze register-to-register paths beginning or ending at that register. Figure 7–17 shows a circuit that illustrates this situation.

Figure 7–17. Clock Objects



With no clock assignments on any of the registers, the Classic analyzer analyzes timing on the path from `reg_a` to `reg_b`, and from `reg_c` to `reg_d`. If you make a clock setting assignment to `reg_b`, `reg_b` is no longer considered a register node in the netlist, and the path from `reg_a` to `reg_b` is no longer analyzed.

In the TimeQuest analyzer, clocks are abstract objects that are associated with nodes in the timing netlist. The TimeQuest analyzer analyzes the path from `reg_a` to `reg_b` even if there is a clock assigned to `reg_b`.

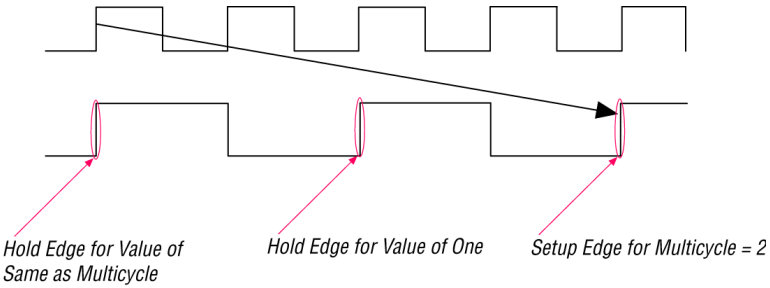
Hold Multicycle

The hold multicycle value numbering scheme different in the Classic and TimeQuest Timing Analyzers. Also, you can choose between two values for the default hold multicycle value in the Classic Timing Analyzer but you cannot change the default value in the TimeQuest Timing Analyzer. The hold multicycle value specifies which clock edge is used for hold analysis when you change the latch edge with a multicycle assignment.

In the Classic Timing Analyzer, the hold multicycle value is based on 1, and is the number of clock cycles away from the setup edge. In the TimeQuest Timing Analyzer, the hold multicycle value is based on zero, and is the number of clock cycles away from the default hold edge. In the TimeQuest Timing Analyzer, the default hold edge is one edge before or after the setup edges. Subtract 1 from any hold multicycle value in the Classic Timing Analyzer to compute the equivalent value for the TimeQuest Timing Analyzer.

In the Classic Timing Analyzer, you can set the default value of the hold multicycle assignment to **One** or **Same as Multicycle**. The default value applies to any multicycle assignment in your design that does not also have a multicycle hold assignment. Figure 7–18 illustrates the difference between **One** and **Same as Multicycle** for a multicycle assignment of 2 using the Classic Timing Analyzer.

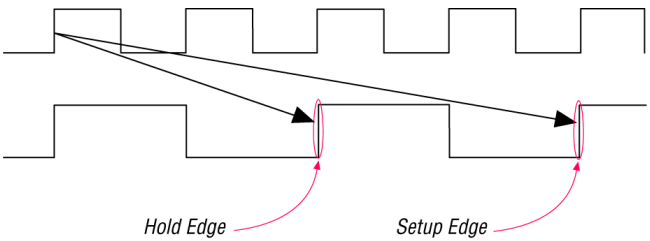
Figure 7–18. Difference Between One & Same As Multicycle



If the default value is **One**, the Classic Timing Analyzer uses the clock edge one before the setup edge for hold analysis. If the default value is **Same as Multicycle**, the Classic Timing Analyzer uses the clock edge that is <*value of multicycle assignment*> edges back from the setup edge.

Figure 7–19 shows simple waveforms for a cross-clock domain transfer with the indicated setup and hold edges.

Figure 7–19. First Relationship Example



In the TimeQuest Timing Analyzer, only a multicycle exception of 2 is required to constrain the design for the indicated setup and hold relationships.

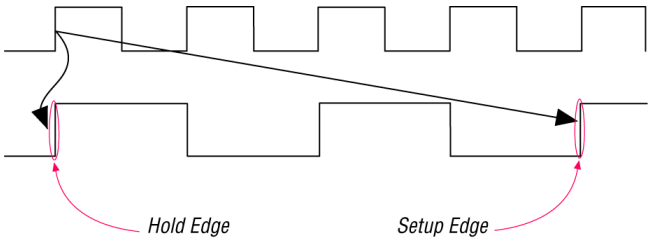
In the Classic Timing Analyzer, if the **Default Hold Multicycle** value is **One**, only a multicycle assignment of 2 is required to constrain the design.

In the Classic Timing Analyzer, if the **Default Hold Multicycle** value is **Same as Multicycle**, you must make two assignments to constrain the design:

- A multicycle assignment of 2
- A hold multicycle assignment of 1 to override the default value

Figure 7–20 shows simple waveforms for a different cross-clock domain transfer with indicated setup and hold edges. The following explanation shows what exceptions to apply to achieve the desired setup and hold relationships.

Figure 7–20. Second Relationship Example



In the TimeQuest Timing Analyzer, you must use the following two exceptions:

- A multicycle exception of 2
- A hold multicycle exception of 1, because the hold edge is one edge behind the default hold edge, which is one edge after the setup edge.

In the Classic Timing Analyzer, if the **Default Hold Multicycle** value is **One**, you must make two assignments to constrain the design:

- A multicycle assignment of 2
- A hold multicycle assignment of 2 to override the default value

In the Classic Timing Analyzer, if the **Default Hold Multicycle** value is **Same as Multicycle**, only a multicycle assignment of 2 is required to constrain the design.

You should always add a hold multicycle assignment for every multicycle assignment to ensure the correct exceptions are applied regardless of the timing analyzer you use, or, for the Classic Timing Analyzer, the **Default Hold Multicycle** setting.

Fitter Behavior

The behavior for one value of the **Optimize hold time** Fitter assignment differs between the TimeQuest Timing Analyzer and the Classic Timing Analyzer. When you set the TimeQuest Timing Analyzer as the default timing analyzer, the **I/O Paths and Minimum TPD Paths** value directs the Fitter to optimize all hold time paths, which has the same affect as the **All Paths** value.

Fitter Performance

If you use the TimeQuest Timing Analyzer as your default timing analyzer, the Fitter memory use and compilation time may increase. However, the timing analysis time may decrease.

Reporting

The TimeQuest Timing Analyzer provides a more flexible and powerful interface for reporting timing analysis results than the Classic Timing Analyzer does. Although the interface and constraints are more flexible and powerful, both analyzers use the same device timing models. This means that both analyzers report identical delays along identically constrained paths in your design. The TimeQuest Timing Analyzer allows you to constrain some paths that you could not constrain with the Classic Timing Analyzer. Differently constrained paths result in different reported values, but for identical paths in your design that are constrained the same way, the delays are exactly the same. Both timing analyzers use the same timing models.

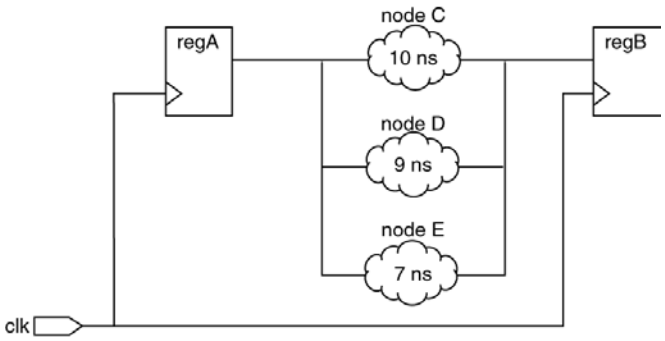
For information about reporting with the TimeQuest Timing Analyzer, refer to the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Paths & Pairs

In reporting, the most significant difference between the two analyzers is that the TimeQuest Timing Analyzer reports paths, while the Classic Timing Analyzer reports pairs. Path reporting means that the analyzer separately reports every path between two registers. Pair reporting means that the analyzer reports only the worst-case path between two registers. One benefit of path reporting over pair reporting is that you can more easily identify common points in failing paths that may be good targets for optimization.

If your design does not meet timing constraints, this reporting difference can give the impression that there are many more timing failures when you use the TimeQuest Timing Analyzer. Figure 7–21 shows a sample circuit followed by a description of the differences between path and pair reporting.

Figure 7–21. Failing Paths



There is an 8-ns period constraint on `clk`, resulting in two paths that fail timing: `regA` →`C` →`regB` and `regA` →`D` →`regB`. The Classic Timing Analyzer reports only worst-case path `regA` →`C`→`regB`. The TimeQuest Timing Analyzer reports both failing paths `regA` →`C` →`regB` and `regA` →`D` →`regB`. It also reports path `regA` →E →`regB` with positive slack.

Default Reports

The TimeQuest Timing Analyzer generates only a small number of reports by default, as compared to the Classic Timing Analyzer which generates every report by default. With the TimeQuest Timing Analyzer, you generate desired reports on demand.

To learn how to create custom reports, refer to the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Netlist Names

The Classic Timing Analyzer uses register names in reporting, but the TimeQuest Timing Analyzer uses register pin names (with the exception of port names of the top-level module). Buried nodes or register names are used when necessary.

Example 7–5 shows how register names are used in Classic Timing Analyzer reports.

Example 7–5. Netlist Names in the Classic Timing Analyzer

```
Info: + Shortest register to register delay is 0.538 ns
    Info: 1: + IC(0.000 ns) + CELL(0.000 ns) = 0.000 ns; Loc. =
    LCFF_X1_Y5_N1;

Fanout = 1; REG Node = 'inst'
    Info: 2: + IC(0.305 ns) + CELL(0.149 ns) = 0.454 ns; Loc. =

LCCOMB_X1_Y5_N20; Fanout = 1; COMB Node = 'inst3~feeder'
    Info: 3: + IC(0.000 ns) + CELL(0.084 ns) = 0.538 ns; Loc. =

LCFF_X1_Y5_N21; Fanout = 1; REG Node = 'inst3'
    Info: Total cell delay = 0.233 ns ( 43.31 % )
    Info: Total interconnect delay = 0.305 ns ( 56.69 % )
```

Example 7–6 shows the same information as presented in a TimeQuest Timing Analyzer report. In this example, register pin names are used in place of register names.

Example 7–6. Netlist Names in the TimeQuest Timing Analyzer

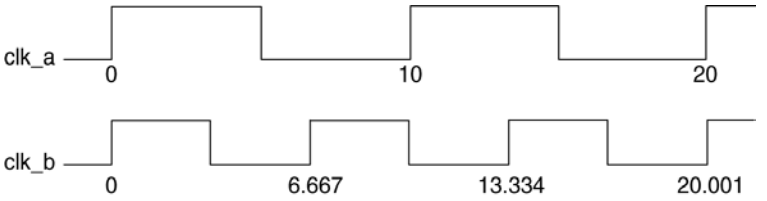
```
    Info:      3.788      0.250     uTco  inst
    Info:      3.788      0.000 RR  CELL  inst|regout
    Info:      4.093      0.305 RR    IC  inst3~feeder|datad
    Info:      4.242      0.149 RR  CELL  inst3~feeder|combout
    Info:      4.242      0.000 RR    IC  inst3|datain
    Info:      4.326      0.084 RR  CELL  inst3
```

Non-Integer Clock Periods

In some cases when related clock periods are not integer multiples of each other, a lack of precision in clock period definition in the TimeQuest Timing Analyzer can result in reported setup or hold relationships of a few picoseconds. In addition, launch and latch times for the relationships can be very large. If you experience this, use the **set_max_delay** and **set_min_delay** exceptions to specify the correct relationships. The Classic Timing Analyzer can maintain additional information about clock frequency that mitigates the lack of precision in clock period definition.

When the clock period cannot be expressed as an integer in terms of picoseconds, then you have the problem detailed in Figure 7–22. This figure shows two clocks: `clk_a` has a 10 ns period, and `clk_b` has a 6.667 ns period.

Figure 7–22. Very Small Setup Relationship



There is a 1 ps setup relationship at 20 ns because you cannot specify the 6.667 ns period beyond picosecond precision. You should apply the maximum and minimum delay exceptions shown in Example 7–7 between the two clocks to specify the correct relationships.

Example 7–7. Minimum & Maximum Delay Exceptions

```
set_max_delay -from [get_clocks clk_a] -to [get_clocks clk_b] 3.333
set_min_delay -from [get_clocks clk_a] -to [get_clocks clk_b] 0
```

Other Features

The TimeQuest Timing Analyzer reports time values without units. By default, the units are nanoseconds, and three decimal places are displayed. You can change the default time unit and decimal places with the **set_time_format** command.

When you use the TimeQuest Timing Analyzer in a Tcl shell, output is ASCII-formatted, and columns are aligned for easy reading on 80-column consoles. Example 7–8 shows sample output from a **report_timing** command from the TimeQuest Timing Analyzer.

Example 7–8. ASCII-Formatted TimeQuest Report

```
tcl> report_timing -from inst -to inst5
Info: Report Timing: Found 1 setup paths (0 violated).  Worst case slack is 3.634
    Info: -from [get_keepers inst]
    Info: -to [get_keepers inst5]
Info: Path #1: Slack is 3.634
    Info: ===================================================================
    Info: From Node    : inst
    Info: To Node      : inst5
    Info: Launch Clock : clk_a
    Info: Latch Clock  : clk_b
    Info:
    Info: Data Arrival Path:
    Info:
    Info: Total (ns)  Incr (ns)     Type  Node
    Info: ==========  ========= ==  ====  ==================================
    Info:      0.000      0.000           launch edge time
    Info:      2.347      2.347  R        clock network delay
    Info:      2.597      0.250     uTco  inst
    Info:      2.597      0.000 RR  CELL  inst|REGOUT
    Info:      3.088      0.491 RR    IC  inst6|DATAC
    Info:      3.359      0.271 RR  CELL  inst6|COMBOUT
    Info:      3.359      0.000 RR    IC  inst5|DATAIN
    Info:      3.443      0.084 RR  CELL  inst5
    Info:
    Info: Data Required Path:
    Info:
    Info: Total (ns)  Incr (ns)     Type  Node
    Info: ==========  ========= ==  ====  ==================================
    Info:      4.000      4.000           latch edge time
    Info:      7.041      3.041  R        clock network delay
    Info:      7.077      0.036     uTsu  inst5
    Info:
    Info: Data Arrival Time  :     3.443
    Info: Data Required Time :     7.077
    Info: Slack              :     3.634
    Info: ===================================================================
    Info:
1 3.634
```

Scripting API

In versions of the Quartus II software earlier than 6.0, the **::quartus::project** Tcl package contained the following SDC-like commands for making timing assignments:

- **create_base_clock**
- **create_relative_clock**
- **get_clocks**
- **set_clock_latency**
- **set_clock_uncertainty**
- **set_input_delay**
- **set_multicycle_assignment**

- **set_output_delay**
- **set_timing_cut_assignment**

These commands are not SDC-compliant. Beginning with version 6.0, these commands are in a new package called **::quartus::timing_assignment**. To ensure backwards compatibility with existing Tcl scripts, the **::quartus::timing_assignment** package is loaded by default in the following executables:

- **quartus**
- **quartus_sh**
- **quartus_cdb**
- **quartus_sim**
- **quartus_stp**
- **quartus_tan**

The **::quartus::timing_assignment** package is not loaded by default in the **quartus_sta** executable. The **::quartus::sdc** Tcl package includes SDC-compliant versions of the commands listed above. That package is available only in the **quartus_sta** executable, and it is loaded by default.

Timing Assignment Conversion

This section describes Classic QSF timing assignments and their equivalent TimeQuest constraints. You can convert many Classic timing assignments to SDC constraints. Some Classic timing assignments can be converted to two different SDC constraints, and you must understand the intended functionality of the design to make an appropriate conversion. You cannot convert some Classic timing assignments because there is no equivalent SDC constraint.

This section includes the following topics, arranged alphabetically:

Setup Relationship

The **Setup Relationship** assignment overrides the setup relationship between two clocks. By default, the Classic Timing Analyzer automatically calculates the setup relationship based on your clock settings. The QSF variable for the **Setup Relationship** assignment is SETUP_RELATIONSHIP. In the TimeQuest Timing Analyzer, use the **set_max_delay** command to specify the maximum setup relationship for a path.

The setup relationship value is the time between latch and launch edges before the TimeQuest Timing Analyzer accounts for clock latency, source μt_{CO}, or destination μt_{SU}.

Hold Relationship

The **Hold Relationship** assignment overrides the hold relationship between two clocks. By default, the Classic Timing Analyzer automatically calculates the hold relationship based on your clock settings. The QSF variable for the **Hold Relationship** assignment is

HOLD_RELATIONSHIP. In the TimeQuest Timing Analyzer, use the **set_min_delay** command to specify the minimum hold relationship for a path.

Clock Latency

The conversion for **Early Clock Latency** and **Late Clock Latency** assignments to SDC constraints is straightforward. Table 7–1 shows the equivalent constraints for each of these Classic assignments.

Table 7–1. Classic & SDC Equivalent Constraints

Classic Timing Assignment		SDC Constraint
Assignment Name	**QSF Variable**	
Early Clock Latency	EARLY_CLOCK_LATENCY	set_clock_latency -source -late
Late Clock Latency	LATE_CLOCK_LATENCY	set_clock_latency -source -early

For more information about clock latency support in the TimeQuest Timing Analyzer, refer to "Clock Latency" on page 7–15.

Clock Uncertainty

This section describes the conversion for the following Classic assignments:

- Clock Setup Uncertainty
- Clock Hold Uncertainty

The conversion to SDC constraints is straightforward. Table 7–2 shows the equivalent SDC constraints for each of these Classic assignments.

Table 7–2. Classic & SDC Equivalent Constraints

Classic Timing Assignment		SDC Constraint
Assignment Name	**QSF Variable**	
Clock Setup Uncertainty	CLOCK_SETUP_UNCERTAINTY	set_clock_uncertainty -setup
Clock Hold Uncertainty	CLOCK_HOLD_UNCERTAINTY	set_clock_uncertainty -hold

Inverted Clock

The Classic Timing Analyzer detects inverted clocks automatically when the clock inversion occurs at the input of the LCELL that contains the register specified in the assignment. You must make an **Inverted Clock** assignment in all other situations for Classic analysis. The QSF variable for the **Inverted Clock** assignment is INVERTED_CLOCK. The TimeQuest Timing Analyzer detects inverted clocks automatically, regardless of the type of inversion circuit, in designs that target device families that support unateness: Stratix® II, Cyclone® II, and HardCopy® II. For designs that target any other device family, you must create a generated clock with the `-invert` option on the output of the cell that inverts the clock.

For more information about unateness, refer to the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Not a Clock

The **Not a Clock** assignment directs the Classic Timing Analyzer that the specified node is not a clock source when it would normally be detected as a clock because of a global f_{MAX} requirement. The QSF variable for the **Not a Clock** assignment is NOT_A_CLOCK. This assignment is not supported in the TimeQuest Timing Analyzer and there is no equivalent constraint. Create appropriate clock constraints in the TimeQuest Timing Analyzer.

Default Required f_{MAX}

The **Default Required f_{MAX}** assignment allows you to specify an f_{MAX} requirement for the Classic Timing Analyzer for all unconstrained clocks in your design. The QSF variable for the **Default Required f_{MAX}** assignment is FMAX_REQUIREMENT. You can use the **derive_clocks** command to create clocks on sources of clock pins in your design that do not already have clocks assigned to them. You should constrain each individual clock in your design with the **create_clock** or **created_generated_clock** command, instead of using the **derive_clocks** command. Refer to "Automatic Clock Detection" on page 7–19 to learn why you should constrain individual clocks in your design.

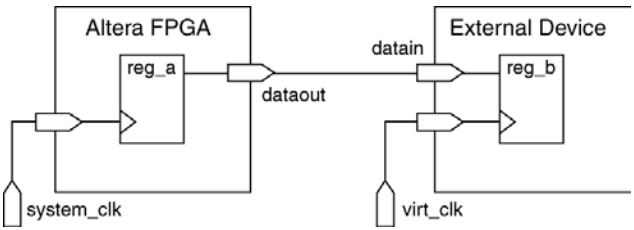
Virtual Clock Reference

The **Virtual Clock Reference** assignment allows you to define timing characteristics of a reference clock outside the FPGA. The QSF variable for the **Virtual Clock Reference** assignment is VIRTUAL_CLOCK_REFERENCE. The TimeQuest Timing Analyzer

supports virtual clocks by default, while the Classic Timing Analyzer requires the **Virtual Clock Reference** assignment to indicate that a clock setting is for a virtual clock. To create a virtual clock in the TimeQuest Timing Analyzer, use the **create_clock** or **create_generated_clock** commands with the `-name` option and no targets.

Figure 7–23 shows a simple circuit that requires a virtual clock, and the following example shows how to constrain the circuit. The circuit shows data transfer between an Altera FPGA and another device, and the clocks for the two devices are not related. You can constrain the path with an output delay assignment, but that assignment requires a virtual clock that defines the clock characteristics of the destination device.

Figure 7–23. Virtual Clock Sample Circuit



Assume the circuit has the following assignments in the Classic Timing Analyzer:

- Clock period of 10 ns on `system_clk` (Clock for the Altera FPGA)
- Clock period of 8 ns on `virt_clk` (Clock for the other device)
- Virtual Clock Reference setting for `virt_clk` is on (Indicates that `virt_clk` is a virtual clock)
- Output Maximum Delay of 5 ns on `dataout` with respect to `virt_clk` (Constrains the path between the two devices)

The SDC commands shown in Example 7–9 constrain the circuit the same way.

Example 7–9. SDC Constraints

```
# Clock for the Altera FPGA
create_clock -period 10 -name system_clk [get_ports system_clk]
# Virtual clock for the other device, with no targets
create_clock -period 8 -name virt_clk
# Constrains the path between the two devices
set_output_delay -clock virt_clk 5 [get_ports dataout]
```

Clock Settings

The Classic Timing Analyzer includes a variety of assignments to describe clock settings. These include duty cycle, f_{MAX}, offset, and others. In the TimeQuest Timing Analyzer, use the **create_clock** and **create_generated_clock** commands to constrain clocks.

Multicycle

The conversion from the QSF variable to the SDC exception is straightforward for the following Classic assignments:

- Multicycle
- Source Multicycle
- Multicycle Hold
- Source Multicycle Hold

Table 7–3 shows the equivalent SDC exceptions for each of these Classic timing assignments.

Table 7–3. Classic & SDC Equivalent Exceptions

Classic Timing Assignment		SDC Exception
Assignment Name	**QSF Variable**	
Multicycle *(1)*	MULTICYCLE	set_multicycle_path -setup -end
Source Multicycle *(2)*	SRC_MULTICYCLE	set_multicycle_path -setup -start
Multicycle Hold *(3)*	HOLD_MULTICYCLE	set_multicycle_path -hold -end
Source Multicycle Hold	SRC_HOLD_MULTICYCLE	set_multicycle_path -hold -start

Notes to Table 7–3:
(1) A multicycle assignment is also known as a "destination multicycle setup" assignment.
(2) A source multicycle assignment is also known as a "source multicycle setup" assignment.
(3) A multicycle hold is also known as a "destination multicycle hold" assignment.

The default value and numbering scheme for the hold multicycle value is different in the Classic and TimeQuest Timing Analyzers. Refer to "Hold Multicycle" on page 7–24 for more information about the difference between the default value and numbering scheme for the hold multicycle value and the Classic and TimeQuest Timing Analyzers.

For more information about how to convert the hold multicycle value, see the *TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Clock Enable Multicycle

The Classic Timing Analyzer supports the following clock enable multicycle assignments. Corresponding types of multicycle assignments are applied to all registers enabled by the targets of the specified clock enable multicycle assignments.

- Clock Enable Multicycle
- Clock Enable Source Multicycle
- Clock Enable Multicycle Hold
- Clock Enable Source Multicycle Hold

The TimeQuest Timing Analyzer does not support any types of clock enable multicycle assignments. You must assign the multicycle to a collection to achieve the same functionality. For example, you can use the **get_registers** command to create a collection of registers with names matching a specific pattern.

I/O Constraints

FPGA I/O timing assignments have typically been made with FPGA-centric t_{SU} and t_{CO} requirements for the Classic Timing Analyzer. However, the Classic Timing Analyzer also supports input and output delay assignments to accommodate industry-standard, system-centric timing constraints. Where possible, you should use system-centric constraints to constrain your designs for the TimeQuest Timing Analyzer. Table 7–4 includes Classic I/O assignments, the equivalent FPGA-centric SDC constraints, and recommended system-centric SDC constraints.

For setup checks (t_{SU} and t_{CO}), <*latch –launch*> equals the clock period for same-clock transfers. For hold checks (t_H and Minimum t_{CO}), <*latch – launch*> equals 0 for same clock transfers. Conversions from Classic assignments to **set_input_delay** and **set_output_delay** constraints work well only when the source and destination registers' clocks are the same (same clock and polarity). If the source and destination registers' clocks are different, the conversion may not be straightforward and you should take extra care when converting to **set_input_delay** and **set_output_delay** constraints.

Table 7–4. Classic & TimeQuest Equivalent I/O Constraints (Part 1 of 2)

Classic	FPGA-centric SDC	System-centric SDC
t_{SU} Requirement	set_max_delay <t_{SU} *requirement*>	set_input_delay -max <*latch –launch –* t_{SU} *requirement*>
t_H Requirement	set_min_delay –<t_H *requirement*> *(1)*	set_input_delay -min <*latch – launch +*t_H *requirement*>

Table 7–4. Classic & TimeQuest Equivalent I/O Constraints (Part 2 of 2)

Classic	FPGA-centric SDC	System-centric SDC
t_{CO} Requirement	set_max_delay <*t_{CO} requirement*>	set_output_delay -max <*latch – launch –t_{CO} requirement*>
Minimum t_{CO} Requirement	set_min_delay <*minimum t_{CO} requirement*>	set_output_delay -min <*latch – launch –minimum t_{CO} requirement*>
t_{PD} Requirement	set_max_delay <*t_{PD} requirement*>	*(2)*
Minimum t_{PD} Requirement	set_min_delay <*minimum t_{PD} requirement*>	*(2)*

Notes to Table 7–4:
(1) Refer to "tH Requirement" on page 7–43 for an explanation about why this exception uses the negative t_H requirement.
(2) The input and output delays can be used for t_{PD} paths, such that they will be analyzed as a system f_{MAX} path. This is a feature unique to the TimeQuest Timing Analyzer.

Input & Output Delay

The conversion to SDC exceptions is straightforward for the following Classic assignments:

- Input Maximum Delay
- Input Minimum Delay
- Output Maximum Delay
- Output Minimum Delay

Table 7–5 shows the equivalent SDC exceptions for each of these Classic timing assignments.

Table 7–5. Classic & SDC Equivalent Exceptions

Classic Timing Assignment		SDC Exception
Assignment Name	QSF Variable	
Input Maximum Delay	INPUT_MAX_DELAY	set_input_delay -max
Input Minimum Delay	INPUT_MIN_DELAY	set_input_delay -min
Output Maximum Delay	OUTPUT_MAX_DELAY	set_output_delay -max
Output Minimum Delay	OUTPUT_MIN_DELAY	set_output_delay -min

In some circumstances, you may receive the following warning message when you update the SDC netlist:

```
Warning: For set_input_delay/set_output_delay, port
"<port>" does not have delay for flag (<rise|fall>,
<min|max>)
```

This warning occurs whenever port constraints have maximum or minimum delay assignments, but not both. In the Classic Timing Analyzer, device inputs can have **Input Maximum Delay** assignments, **Input Minimum Delay** assignments, or both, and device outputs can have **Output Maximum Delay** assignments, **Output Minimum Delay** assignments, or both.

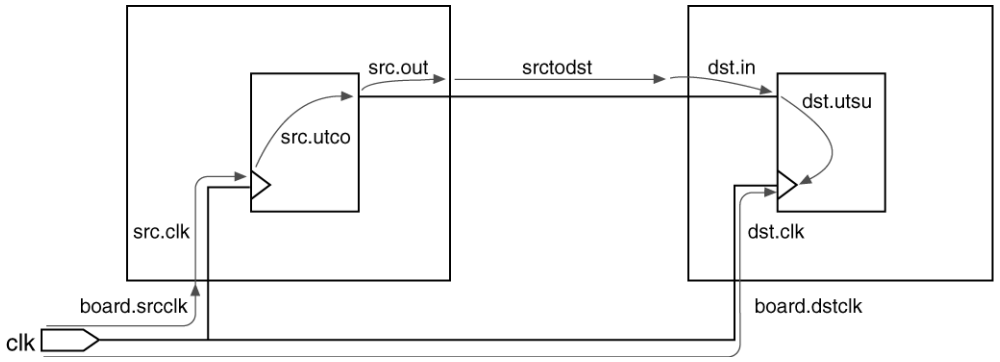
To avoid receiving the warning, your SDC file must specify both the `-max` and `-min` options for each port, or specify neither. If a device I/O in your design includes both the maximum and minimum delay assignments in the Classic Timing Analyzer, the conversion utility converts both, and no warning appears about that device I/O. If a device I/O has only maximum or minimum delay assignments in the Classic Timing Analyzer, you have the following options:

- Add the missing minimum or maximum delay assignment to the device I/O before performing the conversion.
- Modify the SDC constraint after the conversion to add appropriate `-max` or `-min` values.
- Modify the SDC constraint to remove the `-max` or `-min` option so the value is used for both by default.

t_{SU} Requirement

The **t_{SU} Requirement** assignment specifies the maximum acceptable clock setup time for the input (data) pin. The QSF variable for the **t_{SU} Requirement** assignment is TSU_REQUIREMENT. You can convert the **t_{SU} Requirement** assignment to the **set_max_delay** command or the **set_input_delay** command with the `-max` option. The delay value for the **set_input_delay** command is <*latch* –*launch* –t_{SU} *requirement*>. Refer to the labeled paths in Figure 7–24 to understand the names in Equations 3 and 4.

Figure 7–24. Path Names



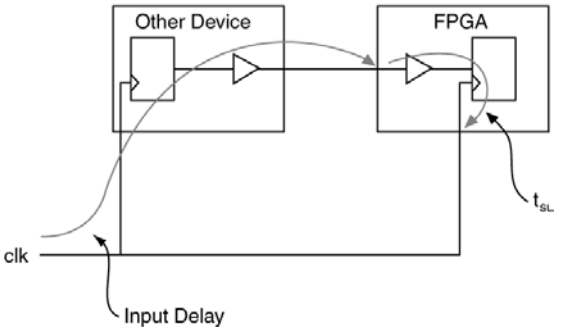
Equation 3 shows the derivation of this conversion.

(3)

```
required - arrival > 0
required = latch + board.dstclk + dst.clk - dst.utsu
arrival = launch + board.srcclk + src.clk + src.utco +
src.out + srctodst + dst.in

input_delay = board.srcclk + src.clk + src.utcu +
src.out + srctodst - board.dstclk

required = latch + dst.clk - dst.utsu
arrival = launch + input_delay + dst.in
(latch + dst.clk - dst.utsu) - (launch + input_delay +
dst.in) > 0

tSU requirement - actual tSU > 0
actual tSU = dst.in + dst.utsu - dst.clk
tSU requirement - (dst.in + dst.utsu - dst.clk) > 0

tSU requirement == latch - launch - input_delay
input_delay == latch - launch - tSU requirement
```

The delay value is the difference between the period of the clock source of the register and the **t_{SU} Requirement** value, as shown in Figure 7–25.

Figure 7–25. t_{SU} Requirement



The delay value for the **set_max_delay** command is the **t_{SU} Requirement** value. Equation 4 shows the derivation of this conversion.

(4)

```
required - arrival > 0
required = latch + board.dstclk + dst.clk - dst.utsu
arrival = launch + board.srcclk + src.clk + src.utco +
src.out + srctodst + dst.in
max_delay = latch + board.dstclk - launch -
board.srcclk - src.clk - src.utco - src.out - srctodst

required = max_delay + dst.clk - dst.utsu
arrival = dst.in
(max_delay + dst.clk - dst.utsu) - (dst.in) > 0

tSU requirement - tSU > 0
actual tSU = dst.in + dst.utsu - dst.clk
tSU requirement - (dst.in + dst.utsu - dst.clk) > 0

set_max_delay == tSU requirement
```

Table 7–6 shows the different ways you can make t_{SU} assignments in the Classic Timing Analyzer, and the corresponding options for the **set_max_delay** exception.

Table 7–6. t_{SU} Requirement & set_max_delay Equivalence (Part 1 of 2)

t_{SU} Requirement Options	set_max_delay Options	Supported in TimeQuest?
-to <*pin*>	-from [get_ports <*pin*>] -to [all_registers]	Yes *(1)*
-to <*clock*>	-from [all_inputs] -to [get_clocks <*clock*>]	No *(2) (4)*

Table 7–6. t_{SU} Requirement & set_max_delay Equivalence (Part 2 of 2)

t_{SU} Requirement Options	set_max_delay Options	Supported in TimeQuest?
-to <*register*>	-from [all_inputs] -to [get_registers <*register*>]	Yes *(4)*
-from <*pin*> -to <*register*>	-from [get_ports <*pin*>] -to [get_registers <*register*>]	Yes *(1)*
-from <*clock*> -to <*pin*>	-from [get_ports <*pin*>] -to [get_clocks <*clock*>]	No *(2) (3) (4)*

Notes to Table 7–6:

(1) These cases are handled by the QSF conversion utility. Refer to "tSU & tH Requirement Conversion" on page 7–73 for more information about how the conversion utility converts this type of assignment

(2) Refer to "Constraint Target Types" on page 7–70 for an explanation about why the TimeQuest Timing Analyzer does not support this option.

(3) If the pin in this assignment feeds registers clocked by the same clock, it is equivalent to the first option, `-to` <*pin*>. If the pin feeds registers clocked by different clocks, you should use **set_input_delay** to constrain the paths properly.

(4) The conversion utility automatically converts this assignment, but the conversion is incorrect. You must fix it manually.

To convert a global t_{SU} assignment to an equivalent SDC exception, use the command shown in Example 7–10.

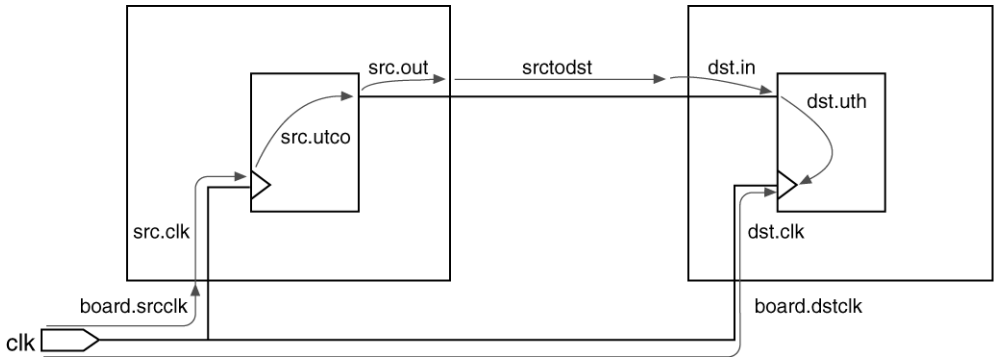
Example 7–10. Converting a Global t_{SU} Assignment to an Equivalent SDC Exception

```
set_max_delay -from [all_inputs] -to [all_registers] <tSU value>
```

t_H Requirement

The **t_H Requirement** specifies the maximum acceptable clock hold time for the input (data) pin. The QSF variable for the **t_H Requirement** assignment is TH_REQUIREMENT. You can convert the **t_H Requirement** assignment to the **set_min_delay** command, or the **set_input_delay** command with the `-min` option. The delay value for the **set_input_delay** command is <*latch –launch +t_H requirement*>. Refer to the labeled paths in Figure 7–26 on page 7–44 to understand the names in Equations 5 and 6.

Figure 7–26. Path Names



Equation 5 shows the derivation of this calculation.

(5)
```
arrival - required > 0
arrival = launch + board.srcclk + src.clk + src.utco +
src.out + srctodst + dst.in
required = latch + board.dstclk + dst.clk + dst.uth
input_delay = board.srcclk + src.clk + src.utcu +
src.out + srctodst - board.dstclk

arrival = launch + input_delay + dst.in
required = latch + dst.clk + dst.uth
(launch + input_delay + dst.in) - (latch + dst.clk +
dst.uth) > 0

tH requirement - actual tH > 0
actual tH = dst.clk + dst.uth - dst.in
tH requirement - (dst.clk + dst.uth - dst.in) > 0

tH requirement == launch - latch + input_delay
input_delay == latch - launch + tH requirement
```

The delay value for the **set_min_delay** command is the **t_H Requirement** value. Equation 6 shows the derivation of this conversion.

(6)
```
arrival - required > 0
arrival = dst.in
required = min_delay + dst.clk + dst.uth

(dst.in) - (min_delay + dst.clk + dst.uth)
```

```
tH requirement - actual tH > 0
actual tH = dst.clk + dst.uth - dst.in
tH requirement - (dst.clk + dst.uth - dst.in) > 0

set_min_delay == - tH requirement
```

Table 7–7 shows the different ways you can make t_H assignments in the Classic Timing Analyzer, and the corresponding options for the **set_min_delay** command.

Table 7–7. t_H Requirement & set_min_delay Equivalence

t_H Requirement Options	set_min_delay Options	Supported in TimeQuest?
-to <*pin*>	-from [get_ports <*pin*>] -to [all_registers]	Yes *(1)*
-to <*clock*>	-from [all_inputs] -to [get_clocks <*clock*>]	No *(2)*
-to <*register*>	-from [all_inputs] -to [get_registers <*register*>]	Yes
-from <*pin*> -to <*register*>	-from [get_ports <*pin*>] -to [get_registers <*register*>]	Yes *(1)*
-from <*clock*> -to <*pin*>	-from [get_ports <*pin*>] -to [get_clocks <*clock*>]	No *(2) (3)*

Notes to Table 7–7:

(1) These cases are handled by the QSF conversion utility. Refer to "tSU & tH Requirement Conversion" on page 7–73 for more information about how the conversion utility converts this type of assignment

(2) Refer to "Constraint Target Types" on page 7–70 for an explanation about why the TimeQuest Timing Analyzer doesn't support this option.

(3) If the pin in this assignment feeds registers clocked by the same clock, it is equivalent to the first option, `-to` <*pin*>. If the pin feeds registers clocked by different clocks, you should use **set_input_delay** to constrain the paths properly.

To convert a global t_H assignment to an equivalent SDC exception, use the command shown in Example 7–11.

Example 7–11. Converting a Global t_H Assignment to an Equivalent SDC Exception

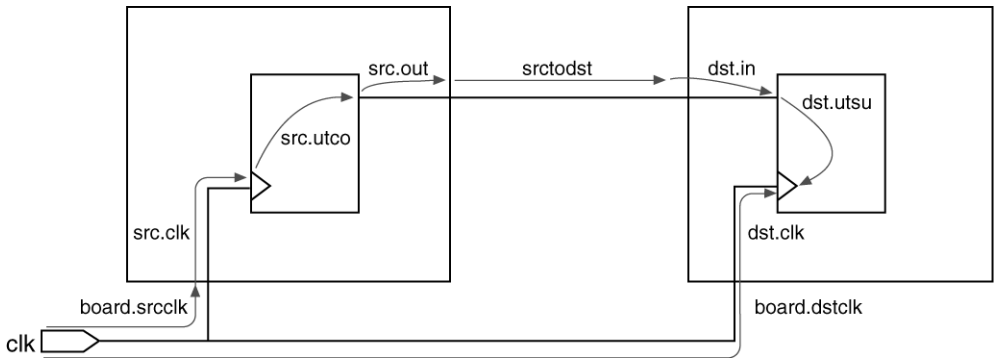
```
set_min_delay -from [all_inputs] -to [all registers] <negative TH value>
```

t_{CO} Requirement

The **t_{CO} Requirement** assignment specifies the maximum acceptable clock to output delay to the output pin. The QSF variable for the **t_{CO} Requirement** assignment is TCO_REQUIREMENT. You can convert the **t_{CO} Requirement** assignment to the **set_max_delay** command or the **set_output_delay** with the -max option. The delay value for the

set_output_delay command is <*latch –launch +*t_{CO} *requirement*>. Refer to the labeled paths in Figure 7–27 to understand the names in Equations 7 and 8.

Figure 7–27. Path Names



Equation 7 shows the derivation of this conversion.

(7)

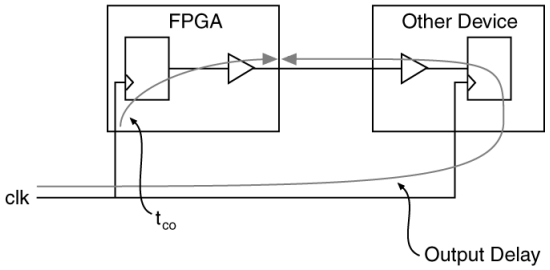
```
required - arrival > 0
required = latch - output_delay
arrival = launch + src.clk + src.utco + src.out
output_delay = srctodst + dst.in + dst.utsu - dst.clk
- board.dstclk + board.srcclk

(latch - output_delay) - (launch + src.clk + src.utco
+ src.out) > 0
```

t_{CO} requirement - actual t_{CO} > 0
actual t_{CO} = src.clk + src.utco + src.out
t_{CO} requirement - (src.clk + src.utco + src.out) > 0

t_{CO} requirement == latch - launch - output_delay
output_delay == latch - launch - t_{CO} requirement

The delay value is the difference between the period of the clock source of the register and the **t_{CO} Requirement** value, as illustrated in Figure 7–28.

Figure 7–28. t_{CO} Requirement



The delay value for the **set_max_delay** command is the **t_{CO} Requirement** value. Equation 8 shows the derivation of this conversion.

(8)
```
required - arrival > 0
required = set_max_delay
arrival = src.clk + src.utco + src.out
set_max_delay - (src.clk + src.utco + src.out) > 0

tCO requirement - actual tCO > 0
actual tCO = src.clk + src.utco + src.out
tCO requirement - (src.clk + src.utco + src.out) > 0

set_max_delay == tCO requirement
```

Table 7–8 shows the different ways you can make t_{CO} assignments in the Classic Timing Analyzer, and the corresponding options for the **set_max_delay** exception.

Table 7–8. t_{CO} Requirement & set_max_delay Equivalence (Part 1 of 2)

t_{CO} Requirement Options	set_max_delay Options	Supported in TimeQuest?
-to <*pin*>	-from [all_registers] -to [get_ports <*pin*>]	Yes *(1)*
-to <*clock*>	-from [get_clocks <*clock*>] -to [all_outputs]	No *(2)*
-to <*register*>	-from [get_registers <*register*>] -to [all_outputs]	Yes
-from <*register*> -to <*pin*>	-from [get_registers <*register*>] -to [get_ports <*pin*>]	Yes *(1)*

Table 7–8. t_{CO} Requirement & set_max_delay Equivalence (Part 2 of 2)

t_{CO} Requirement Options	set_max_delay Options	Supported in TimeQuest?
-from <*clock*> -to <*pin*>	-from [get_clocks <*clock*>] -to [get_ports <*pin*>]	No *(2) (3)*

Notes to Table 7–8:
(1) These cases are handled by the QSF conversion utility.
(2) Refer to "Constraint Target Types" on page 7–70 for an explanation about why the TimeQuest Timing Analyzer doesn't support this option.
(3) If the pin in this assignment feeds registers clocked by the same clock, it is equivalent to the first option, `-to` <*pin*>. If the pin feeds registers clocked by different clocks, you should use **set_output_delay** to constrain the paths properly.

To convert a global t_{CO} assignment to an equivalent SDC exception, use the command in Example 7–12.

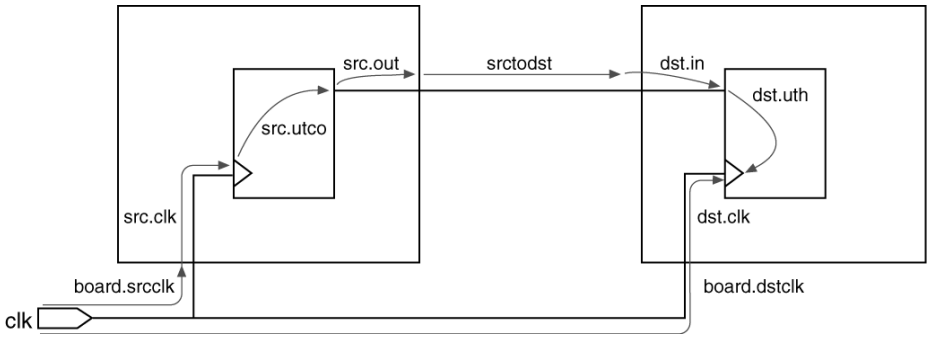
Example 7–12. Converting a Global t_{CO} Assignment to an Equivalent SDC Exception

```
set_max_delay -from [all registers] -to [all_outputs] <t_CO value>
```

Minimum t_{CO} Requirement

The **Minimum t_{CO} Requirement** assignment specifies the minimum acceptable clock to output delay to the output pin. The QSF variable for the **Minimum t_{CO} Requirement** assignment is MIN_TCO_REQUIREMENT. You can convert the **Minimum t_{CO} Requirement** assignment to the **set_min_delay** command or the **set_output_delay** command with the `-min` option. The delay value for the **set_output_delay** command is <*latch –launch +minimum t_{CO} requirement*>. Refer to the labeled paths in Figure 7–29 to understand the names in Equations 9 and 10.

Figure 7–29. Path Names



Equation 9 shows the derivation of this conversion.

(9)
```
arrival - required > 0
arrival = launch + src.clk + src.utco + src.out
required = latch - output_delay
output_delay = srctodst + dst.in - dst.uth - dst.clk -
board.dstclk + board.srcclk

(launch + src.clk + src.utco + src.out) - (latch -
output_delay) > 0

Minimum tCO - Minimum tCO requirement > 0
Minimum tCO = src.clk + src.utco + src.out
(src.clk + src.utco + src.out) - Minimum tCO requirement
> 0

Minimum tCO requirement == latch - launch - output_delay
output_delay == latch - launch - Minimum tCO requirement
```

The delay value for the **set_min_delay** command is the **Minimum t_{CO} Requirement**. Equation 10 shows the derivation of this conversion.

(10)
```
arrival - required > 0
arrival = src.clk + src.utco + src.out
required = min_delay
(src.clk + src.utco + src.out) - (set_min_delay) > 0

Minimum tCO - Minimum tCO requirement > 0
Minimum tCO = src.clk + src.utco + src.out
(src.clk + src.utco + src.out) - Minimum tCO requirement
> 0

set_min_delay == Minimum tCO requirement
```

Table 7–9 shows the different ways you can make minimum t_{CO} assignments in the Classic Timing Analyzer, and the corresponding options for the **set_min_delay** exception.

Table 7–9. Minimum t_{CO} Requirement & set_min_delay Equivalence

Minimum t_{CO} Requirement Options	set_min_delay Options	Supported in TimeQuest?
-to <*pin*>	-from [all_registers] -to [get_ports <*pin*>]	Yes *(1)*
-to <*clock*>	-from [get_clocks <*clock*>] -to [all_outputs]	No *(2)*
-to <*register*>	-from [get_registers <*register*>] -to [all_outputs]	Yes
-from <*register*> -to <*pin*>	-from [get_registers <*register*>] -to [get_ports <*pin*>]	Yes *(1)*
-from <*clock*> -to <*pin*>	-from [get_clocks <*clock*>] -to [get_ports <*pin*>]	No *(2) (3)*

Notes to Table 7–9:
(1) These cases are handled by the QSF conversion utility.
(2) Refer to "Constraint Target Types" on page 7–70 for an explanation about why the TimeQuest Timing Analyzer doesn't support this option.
(3) If the pin in this assignment feeds registers clocked by the same clock, it is equivalent to the first option, `-to` <pin>. If the pin feeds registers clocked by different clocks, you should use **set_output_delay** to constrain the paths properly.

To convert a global **Minimum t_{CO} Requirement** to an equivalent SDC exception, use the command shown in Example 7–13.

Example 7–13. Converting a Global minimum t_{CO} Requirement to an Equivalent SDC Exception

```
set_min_delay -from [all_registers] -to [all_outputs] <Minimum tCO value>
```

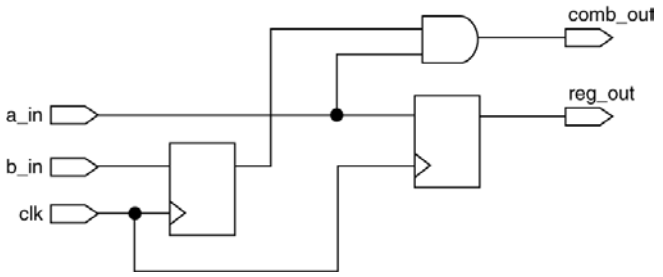
t_{PD} Requirement

The **t_{PD} Requirement** assignment specifies the maximum acceptable input to non-registered output delay, that is, the time required for a signal from an input pin to propagate through combinational logic and appear at an output pin. The QSF variable for the **t_{PD} Requirement** assignment is TPD_REQUIREMENT. You can use the **set_max_delay** command in the TimeQuest Timing Analyzer as an equivalent constraint as long as you account for input and output delays. The **t_{PD} Requirement** assignment does not take into account input and output delays, but the **set_max_delay** exception does, so you must modify the **set_max_delay** value to take into account input and output delays.

Combinational Path Delay Scenario

Figure 7–30 shows a simple circuit followed by an example of a **t_{PD} Requirement** to **set_max_delay** conversion.

Figure 7–30. t_{PD} Example



Assume the circuit has the following assignments in the Classic Timing Analyzer:

- Clock period of 10 ns
- **t_{PD} Requirement** from `a_in` to `comb_out` of 10 ns
- **Input Max Delay** on `a_in` relative to `clk` of 2 ns
- **Output Max Delay** on `comb_out` relative to `clk` of 2 ns

The path from `a_in` to `comb_out` is not affected by the input and output delays. The slack is equal to the <*t_{PD} Requirement from* `a_in` *to* `comb_out`> –<*path delay from* `a_in` *to* `comb_out`>.

Assume the circuit has the SDC constraints shown in Example 7–14 in the TimeQuest Timing Analyzer:

Example 7–14. SDC Constraints

```
create_clock -period 10 -name clk [get_ports clk]
set_max_delay -from a_in -to comb_out 10
set_input_delay -clk clk 2 [get_ports a_in]
set_output_delay -clk clk 2 [get_ports comb_out]
```

The path from `a_in` to `comb_out` is affected by the input and output delays. The slack is equal to:

<*set_max_delay value from* `a_in` *to* `comb_out`> – <*input delay*> – <*output delay*> – <*path delay from* `a_in` *to* `comb_out`>

To convert a global **t_{PD} Requirement** assignment to an equivalent SDC exception, use the command shown in Example 7–15. You should add the input and output delays to the value of your converted **t_{PD} Requirement** (**set_max_delay** exception value) to achieve an equivalent SDC exception.

Example 7–15. Converting a Global t_{PD} Requirement Assignment to an Equivalent SDC Exception

```
set_max_delay -from [all_inputs] -to [all_outputs] <value>
```

Minimum t_{PD} Requirement

The **Minimum t_{PD} Requirement** assignment specifies the minimum acceptable input to non-registered output delay, that is, the minimum time required for a signal from an input pin to propagate through combinational logic and appear at an output pin. The QSF variable for the **Minimum t_{PD} Requirement** assignment is MIN_TPD_REQUIREMENT. You can use the **set_min_delay** command in the TimeQuest Timing Analyzer as an equivalent constraint as long as you account for input and output delays. The **Minimum t_{PD} Requirement** assignment does not take into account input and output delays, but the **set_min_delay** exception does.

Refer to "Combinational Path Delay Scenario" on page 7–51 to see how input and output delays affect minimum and maximum delay exceptions.

To convert a global **Minimum t_{PD} Requirement** assignment to an equivalent SDC exception, use the following command:

Example 7–16. Converting a Global Minimum t_{PD} Requirement Assignment to an Equivalent SDC Exception

```
set_min_delay -from [all_inputs] -to [all_outputs] <value>
```

Cut Timing Path

The **Cut Timing Path** assignment in the Classic Timing Analyzer is equivalent to the **set_false_path** command in the TimeQuest Timing Analyzer. The QSF variable for the **Cut Timing Path** assignment is CUT.

Maximum Delay

The **Maximum Delay** assignment specifies the maximum required delay for the following types of paths:

- Pins to registers
- Registers to registers
- Registers to pins

The QSF variable for the **Maximum Delay** assignment is MAX_DELAY. This requirement overwrites the requirement computed from the clock setup relationship and clock skew. There is no equivalent constraint in the TimeQuest Timing Analyzer.

The **Maximum Delay** assignment for the Classic Timing Analyzer is not related to the **set_max_delay** exception in the TimeQuest Timing Analyzer.

Minimum Delay

The **Minimum Delay** assignment specifies the minimum required delay for the following types of paths:

- Pins to registers
- Registers to registers
- Registers to pins

The QSF variable for the **Minimum Delay** assignment is MIN_DELAY. This requirement overwrites the requirement computed from the clock hold relationship and clock skew. There is no equivalent constraint in the TimeQuest Timing Analyzer.

The **Minimum Delay** assignment for the Classic Timing Analyzer is not related to the **set_min_delay** exception in the TimeQuest Timing Analyzer.

Maximum Clock Arrival Skew

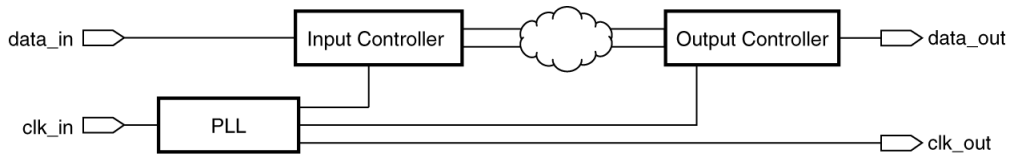
The **Maximum Clock Arrival Skew** assignment specifies the maximum clock skew between a set of registers. The QSF variable for the **Maximum Clock Arrival Skew** assignment is MAX_CLOCK_ARRIVAL_SKEW. In the Classic Timing Analyzer, this assignment is specified between a clock node name and a set of registers. **Maximum Clock Arrival Skew** is not supported in the TimeQuest Timing Analyzer.

Maximum Data Arrival Skew

The **Maximum Data Arrival Skew** assignment specifies the maximum data arrival skew between a set of registers, pins, or both. The QSF variable for the **Maximum Data Arrival Skew** assignment is MAX_DATA_ARRIVAL_SKEW. In this case, the data arrival delay represents the t_{CO} from the clock to the given register, pin, or both. This assignment is specified between a clock node and a set of registers, pins, or both.

The TimeQuest Timing Analyzer does not support a constraint to specify maximum data arrival skew, but you can specify setup and hold times relative to a clock port to constrain an interface like this. Figure 7–31 shows a simplified source-synchronous circuit that is used in the following example.

Figure 7–31. Source-Synchronous Interface Diagram

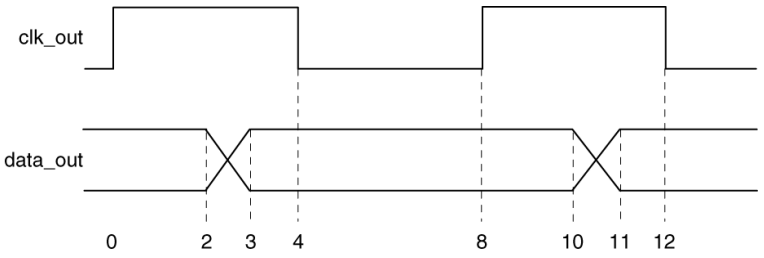


Constraining Skew on an Output Bus

This example constrains the interface so that all bits of the `data_out` bus go off-chip between 2 and 3 ns after the `clk_out` signal. Assume that `clock_in` and `clock_out` have a period of 8 ns.

The following equations and example shows how to create timing requirements that satisfy the timing relationships shown in Figure 7–32.

Figure 7–32. Source-Synchronous Timing Diagram



Equation 11 shows how to compute the value for the **set_output_delay -min** command that creates the 2 ns hold requirement on the destination. For hold requirement calculations in which source and destination clocks are the same, <*latch*> – <*launch*> = 0.

(11)
```
latch - launch = 0 ns
output delay = latch - launch - 2 ns
output delay = -2 ns
```

Equation 12 shows how to compute the value for the **set_output_delay** command that creates the 3 ns setup requirement on the destination. For setup requirement calculations in which source and destination clocks are the same, <*latch*> – <*launch*> = clock period.

(12)
```
latch - launch = 8 ns
output delay = latch - launch - 3 ns
output delay = 5 ns
```

Refer to "I/O Constraints" on page 7–38 for an explanation of the above equations.

Example 7–17 shows the three constraints together.

Example 7–17. Constraining a DDR Interface

```
set period 8.000
create_clock -period $period \
             -name clock_in \
             clock_in
derive_pll_clocks

set_output_delay -add_delay \
    -clock ddr_pll_1_inst|altpll_component|pll|CLK[0] \
    -reference_pin clk_out \
    -min -2.000 \
    [get_ports data_out*]

set_output_delay -add_delay \
    -clock ddr_pll_1_inst|altpll_component|pll|CLK[0] \
    -reference_pin clk_out \
    -max [expr $period - 3.000] \
    [get_ports data_out*]
```

Conversion Utility

The TimeQuest Timing Analyzer includes a conversion utility to help you convert Classic timing assignments in a QSF file to SDC constraints in an SDC file. The utility can use information from your project report database (in the **\db** folder), if it exists, so you should compile your design before the conversion.

The conversion utility ignores all disabled QSF assignments. Disabled assignments say **No** in the **Enabled?** column of the Assignment Editor, and include the `-disable` option in the QSF file.

Refer to "Conversion Utility" on page 7–3 to learn how to run the conversion utility.

Unsupported Global Assignments

First, the conversion utility checks whether any of the global timing assignments in Table 7–10 exist in your project. These global assignments are ignored during the conversion. Refer to the indicated page for information about each assignment, and how to manually convert these global assignments to SDC commands.

Table 7–10. Global Timing Assignments

Assignment Name	QSF Variable	More Information
t_{SU} Requirement	TSU_REQUIREMENT	page 7–40
t_{H} Requirement	TH_REQUIREMENT	page 7–43
t_{CO} Requirement	TCO_REQUIREMENT	page 7–45
Minimum t_{CO} Requirement	MIN_TCO_REQUIREMENT	page 7–48
t_{PD} Requirement	TPD_REQUIREMENT	page 7–50
Minimum t_{PD} Requirement	MIN_TPD_REQUIREMENT	page 7–52

Recommended Global Assignments

Then the conversion utility checks the global assignments in Table 7–11 to ensure they match the specified values.

Table 7–11. Recommended Global Assignments (Part 1 of 2)

Classic Assignment Name	QSF Variable	Value
Cut off clear and preset signal paths	CUT_OFF_CLEAR_AND_PRESET_PATHS	ON
Cut off feedback from I/O pins	CUT_OFF_IO_PIN_FEEDBACK	ON

Table 7–11. Recommended Global Assignments (Part 2 of 2)

Classic Assignment Name	QSF Variable	Value
Cut off read during write signal paths	CUT_OFF_READ_DURING_WRITE_PATHS	ON
Default hold multicycle	DEFAULT_HOLD_MULTICYCLE	ONE
Analyze latches as synchronous elements	ANALYZE_LATCHES_AS_SYNCHRONOUS_ELEMENTS	ON
Enable Clock Latency	ENABLE_CLOCK_LATENCY	ON
Cut paths between unrelated clock domains	CUT_OFF_PATHS_BETWEEN_CLOCK_DOMAINS	OFF
Display Entity Name	PROJECT_SHOW_ENTITY_NAME	ON

The assignments are checked because the functionality of the Classic Timing Analyzer with the specified values corresponds to the behavior of the TimeQuest Timing Analyzer.

- **Cut off clear and preset signal paths**—The TimeQuest Timing Analyzer does not support this functionality. You should use Recovery and Removal analysis instead to analyze register control paths. The Classic Timing Analyzer does not support this option.
- **Cut off feedback from I/O pins**—The TimeQuest Timing Analyzer does not match the functionality of the Classic Timing Analyzer when this assignment is OFF.
- **Cut off read during write signal paths**—The TimeQuest Timing Analyzer does not match the functionality of the Classic Timing Analyzer when this assignment is OFF.
- **Default hold multicycle**—A value of **One** matches the analysis the TimeQuest Timing Analyzer performs based on a value of zero. The TimeQuest Timing Analyzer does not match the functionality of the Classic Timing Analyzer when this assignment value is **Same as Multicycle**. If your **Default hold multicycle** assignment value is **Same as Multicycle**, and that is correct for your design, you must add appropriate hold multicycle exceptions for each multicycle exception in your SDC file. Refer to "Hold Multicycle" on page 7–24 for a comparison of the hold relationship analysis in the Classic and TimeQuest Timing Analyzers.
- **Analyze latches as synchronous elements**—The TimeQuest Timing Analyzer analyzes latches as synchronous elements by default and does not match the functionality of the Classic Timing Analyzer when this assignment is OFF. Beginning with version 5.1 of the Quartus II software, the Classic Timing Analyzer analyzes latches as synchronous elements by default.

- **Enable Clock Latency**—The TimeQuest Timing Analyzer includes clock latency in its calculations. The TimeQuest Timing Analyzer does not match the functionality of the Classic Timing Analyzer when this assignment is OFF. Latency on a clock can be viewed as a simple delay on the clock path, and affects clock skew. This is in contrast to an offset, which alters the setup and hold relationship between two clocks. Refer to "Offset & Latency Example" on page 7–16 for an example of the different effects of offset and latency. When you turn on **Enable Clock Latency** in the Classic Timing Analyzer, it affects the following aspects of timing analysis:
  - **Early Clock Latency** and **Late Clock Latency** assignments are honored
  - The compensation delay of a PLL is analyzed as latency
  - For clock settings where you do not specify an offset, the automatically computed offset is treated as latency.
- **Cut paths between unrelated clock domains**—The TimeQuest Timing Analyzer does not cut paths between unrelated clock domains. The TimeQuest Timing Analyze does not match the functionality of the Classic Timing Analyzer when this assignment is ON. Refer to "Related & Unrelated Clocks" on page 7–13 for information about this setting.
- **Display Entity Name**—Any entity-specific assignments are ignored in the TimeQuest Timing Analyzer because they do not include the entity name when this option is ON.

If your design meets timing requirements in the Classic Timing Analyzer without all of the settings recommended in Table 7–11 on page 7–56, you should perform one of the following actions.

- Change the settings and re-constrain and re-verify as necessary.
  or
- Add or modify SDC constraints as appropriate because analysis in the TimeQuest Timing Analyzer may be different after conversion.

Clock Conversion

Next, the conversion utility adds the **derive_pll_clocks** command to the SDC file. This command creates generated clocks on all PLL outputs in your design each time the SDC file is read. The command does not add a clock on the FPGA port that drives the PLL input.

The conversion utility includes the **derive_pll_clocks -use_tan_name** command in the SDC file it creates. The `-use_tan_name` option overrides the default clock naming behavior (the PLL pin name) so the clock name is the same as the net name in the Classic Timing Analyzer.

Including the `-use_tan_name` option ensures that the conversion utility converts clock-to-clock exceptions properly. If you remove the `-use_tan_name` option, you must also edit references to the clock names in other SDC commands so that they match the PLL pin names.

If your design includes a global f_{MAX} assignment, the assignment is converted to a **derive_clocks** command. The behavior of a global f_{MAX} assignment is different from the behavior of clocks created with the **derive_clocks** command, and you should use the **report_clocks** command when you review conversion results to evaluate the clock settings. Refer to "Automatic Clock Detection" on page 7–19 for an explanation of the differences. As soon as you know the appropriate clock settings, you should use **create_clock** or **create_generated_clock** commands instead of the **derive_clocks** command.

The conversion utility adds a **post_message** command before the **derive_clocks** command to remind you that the clocks are derived automatically. The TimeQuest Timing Analyzer displays the reminder every time it reads the SDC file. Remove or comment out the **post_message** command to prevent the message from displaying.

Next, the conversion utility identifies and converts clock settings in the QSF file. If a project database exists, the utility also identifies and converts any additional clocks in the report file that are not in the QSF, such as PLL base clocks.

If you change the PLL input frequency, you must modify the SDC constraint manually.

The conversion utility ignores clock offsets on generated clocks. Refer to "Clock Offset" on page 7–14 for information about how to use offset values in the TimeQuest Timing Analyzer.

Instance Assignment Conversion

Next, the conversion utility converts the following instance assignments in Table 7–12. Refer to the indicated page for information about each assignment.

Table 7–12. Instance Timing Assignments (Part 1 of 2)

Assignment Name	QSF Variable	More Information
Late Clock Latency	LATE_CLOCK_LATENCY	page 7–34
Early Clock Latency	EARLY_CLOCK_LATENCY	

Table 7–12. Instance Timing Assignments (Part 2 of 2)

Assignment Name	QSF Variable	More Information
Clock Setup Uncertainty	CLOCK_SETUP_UNCERTAINTY	page 7–34
Clock Hold Uncertainty	CLOCK_HOLD_UNCERTAINTY	
Multicycle *(1)*	MULTICYCLE	page 7–37
Source Multicycle *(2)*	SRC_MULTICYCLE	
Multicycle Hold *(3)*	HOLD_MULTICYCLE	
Source Multicycle Hold	SRC_HOLD_MULTICYCLE	
Cut Timing Path	CUT	page 7–52
Input Maximum Delay	INPUT_MAX_DELAY	page 7–39
Input Minimum Delay	INPUT_MIN_DELAY	
Output Maximum Delay	OUTPUT_MAX_DELAY	
Output Minimum Delay	OUTPUT_MIN_DELAY	

Notes to Table 7–12:
(1) A multicycle assignment can also be known as a "destination multicycle setup" assignment.
(2) A source multicycle assignment can also be known as a "source multicycle setup" assignment.
(3) A multicycle hold can also be known as a "destination multicycle hold" assignment.

Depending on input and output delay assignments, you may receive a warning message when the SDC file is read. The message warns that the **set_input_delay** commands, **set_output_delay** commands, or both are missing the `-max` option, `-min` option, or both. Refer to "Input & Output Delay" on page 7–39 for an explanation of why the warning occurs and how to avoid it.

Next, the conversion utility converts the following instance assignments in Table 7–13. Refer to the indicated page for information about each assignment. If the t_{PD} and minimum t_{PD} assignment targets also have input or output delays that apply to them, the t_{PD} and Minimum t_{PD} conversion values may be incorrect. This is described in more detail on the indicated pages for the appropriate assignments.

Table 7–13. Instance Timing Assignments (Part 1 of 2)

Assignment Name	QSF Variable	More Information
t_{PD} Requirement *(1)*	TPD_REQUIREMENT	page 7–50
Minimum t_{PD} Requirement *(1)*	MIN_TPD_REQUIREMENT	page 7–52
Setup Relationship	SETUP_RELATIONSHIP	page 7–33

Table 7–13. Instance Timing Assignments (Part 2 of 2)

Assignment Name	QSF Variable	More Information
Hold Relationship	HOLD_RELATIONSHIP	page 7–33

Notes Table 7–13:
(1) Refer to "tPD & Minimum tPD Requirement Conversion" on page 7–75 for more information about how the conversion utility converts single-point t_{PD} and minimum t_{PD} assignments.

Then the conversion utility converts Classic I/O timing assignments to FPGA-centric SDC constraints. Table 7–14 includes Classic assignments, the equivalent FPGA-centric SDC constraints, and recommended system-centric SDC constraints.

Table 7–14. Classic & TimeQuest Equivalent Constraints

Classic	FPGA-Centric SDC	System-Centric SDC	More Information
t_{SU} Requirement *(1)*	set_max_delay	set_input_delay -max	page 7–40
t_H Requirement *(1)*	set_min_delay	set_input_delay -min	page 7–43
t_{CO} Requirement *(2)*	set_max_delay	set_output_delay -max	page 7–45
Minimum t_{CO} Requirement *(2)*	set_min_delay	set_output_delay -min	page 7–48

Notes Table 7–14:
(1) Refer to "tSU & tH Requirement Conversion" on page 7–73 for more information about how the conversion utility converts this type of assignment.
(2) Refer to "tCO Requirement Conversion" on page 7–63 for more information about how the conversion utility converts this type of assignment.

The conversion utility can convert Classic I/O timing assignments only to the FPGA-centric constraints without additional information about your design. Making system-centric constraints requires information about the external circuitry interfacing with the FPGA such as external clocks, clock latency, board delay, and clocking exceptions. You cannot convert classic timing assignments to system-centric constraints without that information. If you use the conversion utility, you can modify the SDC constraints to change the FPGA-centric constraints to system-centric constraints as appropriate.

I/O Timing Assignment Target Type Conversion

The conversion utility uses simple rules to determine whether to treat the targets of t_{SU}, t_H, t_{CO} and minimum t_{CO} assignments as ports or not. Table 7–15 shows the conversion rules, which depend on whether the assignment is single-point or point-to-point. If there is any value in the `-from` field, including `*`, the assignment is assumed to be point-to-point.

If the conversion result is not what you intend (for example, a single-point **t_{SU} Requirement** assignment target is actually a register name), refer to the indicated table for more information about how to manually correct the SDC constraint.

Table 7–15. I/O Timing Assignment Conversion Rules

Assignment Name	Single-Point	Point-to-Point		More Information
	-to <name>	-from <name>	-to <name>	
t_{SU} Requirement	[get_ports <*name*>]	[get_ports <*name*>]	<*name*>	Table 7–6 on page 7–42
t_H Requirement	[get_ports <*name*>]	[get_ports <*name*>]	<*name*>	Table 7–7 on page 7–45
t_{CO} Requirement	[get_ports <*name*>]	<*name*>	[get_ports <*name*>]	Table 7–8 on page 7–47
Minimum t_{CO} Requirement	[get_ports <*name*>]	<*name*>	[get_ports <*name*>]	Table 7–9 on page 7–50

PLL Phase Shift Conversion

The conversion utility does not account for PLL phase shifts when it converts values of the following FPGA-centric I/O timing assignments:

- **t_{SU} Requirement**
- **t_H Requirement**
- **t_{CO} Requirement**
- **Minimum t_{CO} Requirement**

If any of your paths go through PLLs with a phase shift, you must correct the converted values for those paths according to the following formula:

$$\text{<correct value>} = \text{<converted value>} - \frac{(\text{<pll output period>} \times \text{<phase shift>})}{360} \quad (13)$$

Example 7–18 shows the incorrect conversion result for a t_{CO} assignment and how to correct it. For the example, assume the PLL output frequency is 200 MHz (period is 5 ns), the phase shift is 90 degrees, the **t_{CO} Requirement** value is 1 ns, and it is made to `data[0]`. The QSF file contains the following assignment:

Example 7–18. Assignment

```
set_instance_assignment -name TCO_REQUIREMENT -to data[0] 1.0
```

The conversion utility generates the following SDC command:

Example 7–19. SDC Command

```
set_max_delay -from [get_registers *] -to [get_ports data[0]] 1.0
```

To correct the value, use the formula and values above, as shown in the following example:

$$1.0 - \frac{(5 \times 90)}{360} = -0.25$$

Then, change the value so the SDC command looks like Example 7–20:

Example 7–20. SDC Command with Correct Values

```
set_max_delay -from [get_registers *] -to [get_ports data[0]] -0.25
```

t_{CO} Requirement Conversion

The conversion utility uses a special process to convert **t_{CO} Requirement** and **Minimum t_{CO} Requirement** assignments. In addition to the **set_max_delay** or **set_min_delay** commands, the conversion utility adds a **set_output_delay** constraint relative to a virtual clock named N/C, which stands for Not a Clock. It also creates the virtual clock named N/C with a period of 10 ns. Adding the virtual clock allows you to report timing on the output paths. Without the virtual clock N/C, the clock used for reporting would be blank. Example 7–21 shows how the conversion utility converts a **t_{CO} Requirement** assignment of 5.0 ns to **data[0]**.

Example 7–21. Converting a t_{CO} Requirement Assignment of 5.0 ns to data[0]

```
set_max_delay -from [get_registers *] -to [get_ports data[0]]
set_output_delay -clock "N/C" 0 [get_ports data[0]]
```

Entity-Specific Assignments

Next, the conversion utility converts the entity-specific assignments listed in Table 7–16 that exist in the **Timing Analyzer Settings** report panel. This usually occurs if you have any timing assignments in your Verilog HDL or VHDL source, which can include MegaCore function files. These entity-specific assignments cannot be automatically converted unless your project is compiled and a **\db** directory exists.

Table 7–16. Entity-Specific Timing Assignments

Classic	QSF Variable	More Information
Multicycle	MULTICYCLE	page 7–37
Source Multicycle	SRC_MULTICYCLE	
Multicycle Hold	HOLD_MULTICYCLE	
Source Multicycle Hold	SRC_HOLD_MULTICYCLE	
Setup Relationship	SETUP_RELATIONSHIP	page 7–33
Hold Relationship	HOLD_RELATIONSHIP	page 7–33
Cut Timing Path	CUT	page 7–52

You must manually convert all other entity-specific timing assignments.

Unsupported Instance Assignments

Finally, the conversion utility checks for the following unsupported instance assignments listed in Table 7–17 and warns you if any of them exist. Refer to the indicated page for information about each assignment. You can manually convert some of the assignments to SDC constraints.

Table 7–17. Instance Timing Assignments

Assignment Name	QSF Variable	More Information
Clock Enable Multicycle	CLOCK_ENABLE_MULTICYCLE	page 7–38
Clock Enable Multicycle Hold	CLOCK_ENABLE_MULTICYCLE_HOLD	
Clock Enable Source Multicycle	CLOCK_ENABLE_SOURCE_MULTICYCLE	
Clock Enable Source Multicycle Hold	CLOCK_ENABLE_SOURCE_MULTICYCLE_HOLD	
Inverted Clock	INVERTED_CLOCK	page 7–35
Maximum Clock Arrival Skew	MAX_CLOCK_ARRIVAL_SKEW	page 7–53
Maximum Data Arrival Skew	MAX_DATA_ARRIVAL_SKEW	page 7–54
Maximum Delay	MAX_DELAY	page 7–53
Minimum Delay	MIN_DELAY	page 7–53
Virtual Clock Reference	VIRTUAL_CLOCK_REFERENCE	page 7–35

Reviewing Conversion Results

You must review the messages that are generated during the conversion process, and review the SDC file for correctness and completeness. Warning and critical warning messages identify significant differences between the Classic and TimeQuest Timing Analyzer behaviors. In some cases, warning messages indicate that the conversion utility ignored assignments because it could not determine the intended functionality of your design. You must add to or modify the SDC constraints as necessary based on your knowledge of the design.

The conversion utility creates an SDC file with the same name as your current revision, <*revision*>**.sdc**, and it overwrites any existing <*revision*>**.sdc** file. If you use the conversion utility to create an SDC file, you should make additions or corrections in a separate SDC file, or a copy of the SDC file created by the conversion utility. That way, you can re-run the conversion utility later without overwriting your additions and changes. If you have constraints in multiple SDC files, refer to"Constraint File Priority" on page 7–10 to learn how to add them to your project.

Warning Messages

The conversion utility may generate any of the following warning messages. Refer to the information provided for each warning message to learn what to do in that instance.

Ignored QSF Variable <*assignment*>
The conversion utility ignored the specified assignment. Determine whether an equivalent constraint is necessary and manually add one if appropriate. Refer to "Timing Assignment Conversion" on page 7–32 for information about conversions for all QSF timing assignments.

Global <*name*> = <*value*>
The conversion utility ignored the global assignment <*name*>. Manually add an equivalent constraint if appropriate. Refer to "Unsupported Global Assignments" on page 7–56 for information about conversions for these assignments.

QSF: Expected <*name*> to be set to <*expected value*> but it is set to <*actual value*>
The behavior of the TimeQuest Timing Analyzer is closest to the Classic Timing Analyzer when the value for the specified assignment is the expected value. Because the actual assignment value is not the expected value in your project, the TimeQuest analysis may be different from the Classic Timing Analyzer analysis. Refer to "Recommended Global Assignments" on page 7–56 for an explanation about the indicated QSF variable names.

QSF: Found Global Fmax Requirement. Translation will be done using derive_clocks
Your design includes a global f_{MAX} requirement, and the requirement is converted to the **derive_clocks** command. Refer to "Default Required fMAX" on page 7–35 for information about how to convert to an SDC constraint.

TAN Report Database not found. HDL based assignments will not be migrated
You did not analyze your design with the Classic Timing Analyzer before running the conversion utility. As a result, the conversion utility did not convert any timing assignments in your HDL source code to SDC constraints. If you have timing assignments in your HDL source code, you must find and convert them manually, or analyze your design with the Classic Timing Analyzer and rerun the conversion utility.

Ignoring OFFSET_FROM_BASE_CLOCK assignment for clock <*clock*>
In some cases, this assignment is used to work around a limitation in how the Classic Timing Analyzer handles some forms of clock inversion. The conversion script ignores the assignment because it cannot determine whether the assignment is used as a workaround. Review your clock setting and add the assignment in your SDC file if appropriate. Refer to "Clock Offset" on page 7–14 for more information about converting clock offset.

Clock <*clock*> has no FMAX_REQUIREMENT - No clock was generated
The conversion script did not convert the clock named <*clock*> because it has no f_{MAX} requirement. You should add a clock constraint with an appropriate period to your SDC file.

No Clock Settings defined in QSF file
If your QSF file has no clock settings, ignore this message. You must add clock constraints in your SDC file manually.

Can't find clock settings <*name*> in current project - ignoring clock settings
Your design has a clock setting name assigned to a node, but no clock setting for that name exists. Add the appropriate clock constraints or remove the clock setting assignment.

TAN Report Database not found. Some clocks may not be migrated successfully
You did not analyze your design with the Classic Timing Analyzer before running the conversion utility. As a result, clocks in your design that are not defined in your QSF are not converted to SDC constraints. If your design contains clocks that are not defined in the QSF, you must find and convert them manually, or analyze your design with the Classic Timing Analyzer and re-run the conversion utility.

Clock's offset value will be ignored: <*clock*>
Clocks that are not defined in your QSF file can have a non-zero offset, or an offset that is not auto-computed. The conversion utility ignores the offset value. Refer to "Offset & Latency Example" on page 7–16 for information about offset and latency.

Clock Settings Summary Panel not found
You did not analyze your design with the Classic Timing Analyzer before using the conversion utility or there are no clocks in your design. As a result, any timing assignments reported in the **Clock Settings Summary** panel that do not exist in your QSF file are ignored. You must find and convert them manually, or analyze your design with the Classic Timing Analyzer and re-run the conversion utility.

No clocks were found in QSF or TAN.RPT files
If you have not made any clock assignments for your design, ignore this message. Otherwise, you must manually add clock constraints in your SDC file.

Clocks

Ensure that the conversion utility converted all clock assignments correctly. Run **report_clocks**, or double-click **Report Clocks** in the Tasks pane in the TimeQuest GUI. Make sure that the right number of clocks is reported. If any clock constraints are missing, you must add them manually with the appropriate SDC commands (**create_clock** or **create_generated_clock**). Confirm that each option for each clock is correct.

The TimeQuest Timing Analyzer can create more clocks, such as:

- `derive_clocks` selecting ripple clocks
- `derive_pll_clocks`, adding
  - Extra clocks for PLL switchover
  - Extra clocks for LVDS pulse-generated clocks (~load_reg)

Clock Transfers

After you confirm that all clock assignments are correct, run **report_clock_transfers**, or double-click **Report Clock Transfers** in the Tasks pane in the TimeQuest GUI. The command generates a summary table with the number of paths between each clock domain. If the number of cross-clock domain paths seems high, remember that all clock domains are related in the TimeQuest Timing Analyzer. You must cut unrelated clock domains. Refer to "Related & Unrelated Clocks" on page 7–13 for information about how to cut unrelated clock domains.

Path Details

If you have unexpected differences between the Classic and TimeQuest analyzers on some paths, follow these steps to identify the cause of the difference.

1. List the path in the Classic analyzer.
2. Report timing on the path in the TimeQuest analyzer.
3. Compare slack values.
4. Compare source and destination clocks.
5. Compare the launch/latch times in the TimeQuest analyzer to the setup/hold relationship in the Classic analyzer. The times are absolute in the TimeQuest analyzer and relative in the Classic analyzer.
6. Compare clock latency values.

Unconstrained Paths

Next, run `report_ucp`, or double-click **Report Unconstrained Paths** in the Tasks pane in the TimeQuest GUI. This command generates a series of reports that detail any unconstrained paths in your design. If your design was completely constrained in the Classic analyzer but there are unconstrained paths in the TimeQuest analyzer, some assignments may not have been converted properly. Also, some of the assignments could be ambiguous. The TimeQuest analyzer analyzes more paths than the Classic analyzer does, so any unconstrained paths might be paths you could not constrain in the Classic analyzer.

Bus Names

If your design includes Classic timing assignments to buses, and the bus names do not include square brackets enclosing an asterisk, such as: `address[*]`, you should review the SDC constraints to ensure the conversion is correct. Refer to "Bus Name Format" on page 7–9 for more information.

Other

Review the notes listed in "Conversion Utility" on page 7–73.

Rerunning the Conversion Utility

You can force the conversion utility to run even if it can find an SDC file according to the priority described in "Constraint File Priority" on page 7–10. Any method described in "Conversion Utility" on page 7–3 forces the conversion utility to run even if it can find an SDC file.

Notes

This section describes notes for the TimeQuest Timing Analyzer. Refer to the FindAnswers search on **www.altera.com** for the most up-to-date information.

LVDS Megafunction

The TimeQuest Timing Analyzer reports more clocks in the LVDS megafunction than the Classic Timing Analyzer does. This because the TimeQuest Timing Analyzer detects clocks differently than the Classic Timing Analyzer does. Refer to "Automatic Clock Detection" on page 7–19 for more information about how the TimeQuest Timing Analyzer detects clocks. The slack values are identical in the TimeQuest and Classic Timing Analyzers even though the TimeQuest Timing Analyzer detects more clocks.

Output Pin Load Assignments

The TimeQuest Timing Analyzer takes **Output Pin Load** values into account when it analyzes your design. If you change **Output Pin Load** assignments and do not recompile before you analyze timing, you must use the `-force_dat` option when you create the timing netlist. Type the following command at the Tcl console of the TimeQuest Timing Analyzer:

```
create_timing_netlist -force_dat ↵
```

If you change **Output Pin Load** assignments and do recompile before you analyze timing, you should not use the `-force_dat` option when you create the timing netlist. You can create the timing netlist with the **create_timing_netlist** command, or with the **Create Timing Netlist** task in the Tasks pane.

Constraint Target Types

The TimeQuest Timing Analyzer does not support constraints between clocks and non-clocks (such as ports and registers). In the current version of the TimeQuest Timing Analyzer, you can make constraints between clocks and clocks, and between non-clocks and non-clocks.

DDR Constraints with the DDR Timing Wizard

The DDR Timing Wizard (DTW) creates an SDC file that contains constraints for a DDR interface. You can use that SDC file with the TimeQuest Timing Analyzer to analyze only the DDR interface part of a design.

You should use the SDC file created by DTW for constraining a DDR interface in the TimeQuest Timing Analyzer. Additionally, your QSF should not contain timing assignments for the DDR interface if you plan to use the conversion utility to create an SDC file. You should run the conversion utility before you use DTW, and you should choose not to apply assignments to the QSF.

However, if you used DTW and chose to apply assignments to a QSF, before you used the conversion utility, you should remove the DTW-generated QSF timing assignments and re-run the conversion utility. The conversion utility creates some incompatible SDC constraints from the DTW QSF assignments.

HardCopy Stratix Device Handoff

If you target the HardCopy device family, you should not use the TimeQuest Timing Analyzer. The TimeQuest Timing Analyzer is not supported for the HardCopy Stratix design process. The TimeQuest Timing Analyzer supports HardCopy II series devices.

Unsupported SDC Features

Some SDC commands and features are not supported by the current version of the TimeQuest Timing Analyzer. These include:

- The **get_designs** command, because the Quartus II software supports a single design, so this command is not necessary

- True latch analysis with time-borrowing feature; it can, however, convert latches to negative-edge-triggered registers
- Commands to specify operating conditions and silicon characteristics
- The case analysis feature
- Loads, clock transitions, input transitions, and other features

Design Space Explorer Support

Some exploration settings in Design Space Explorer (DSE) are not supported if you use the TimeQuest Timing Analyzer. Table 7–18 shows which exploration settings are supported by the Classic and TimeQuest Timing Analyzers.

Table 7–18. Supported DSE Exploration Settings

DSE Exploration Setting	Timing Analyzer Support	
	Classic	TimeQuest
Search for Best Area	Yes	Yes
Search for Best Performance	Support based on effort level	
Low-Effort Level (Seed Sweep)	Yes	Yes
Medium-Effort Level (Extra Effort Space)	Yes	Yes
High-Effort Level (Physical Synthesis Space)	Yes	Yes
Highest-Effort Level (Physical Synthesis with Retiming Space)	Yes	No
Search for Lowest Power	Yes	Yes
Advanced Search	Yes	No

Constraint Passing

The Quartus II software can read constraints generated by other EDA software, and write constraints to be read by other EDA software.

Other synthesis software can generate constraints that target the QSF file. If you change timing constraints in synthesis software after creating an SDC file for the TimeQuest Timing Analyzer, you must update the SDC constraints. You can use the conversion utility, or update the SDC file manually.

The Quartus II software can export a timing netlist and SDC file for use in the PrimeTime software. That SDC file is generated from the timing assignments in the project's QSF file. If you use the TimeQuest Timing Analyzer, you may have no timing assignments in the QSF file, but have

them all in the SDC file. The SDC file used by the TimeQuest Timing Analyzer is not compatible with the SDC file generated specifically for use with the PrimeTime software, due to name differences in the netlist. If you use the TimeQuest Timing Analyzer and want to generate files for use with the PrimeTime software, you should enter timing assignments in the Assignment Editor that correspond to your SDC constraints, or manually create constraints for the PrimeTime software.

Optimization

Gate-level retiming is not supported if you turn on the TimeQuest Timing Analyzer as your default timing analyzer.

If you use physical synthesis with the TimeQuest Timing Analyzer, the design may have lower performance.

Clock Network Delay Reporting

In the Quartus II software version 6.0, the TimeQuest Timing Analyzer reports delay on the clock network as a single number, rather than node-to-node segments, as the Classic Timing Analyzer does. Beginning with version 6.0 SP1, the TimeQuest Timing Analyzer reports delay on the clock network by node-to-node segments.

PowerPlay Power Analysis

You must perform the following steps to generate an **Early Power Estimator** output file when you use the TimeQuest Timing Analyzer and your design targets one of the following device families:

- Cyclone
- Stratix
- HardCopy Stratix

To generate an **Early Power Estimator** output file for designs targeting those families, you must perform the following steps.

1. Turn off the TimeQuest Timing Analyzer. Refer to "Set the Default Timing Analyzer" on page 7–4 to learn how to turn off the TimeQuest Timing Analyzer.

2. Manually convert your TimeQuest timing constraints in the SDC file to Classic timing assignments. You can use the Assignment Editor to enter your Classic timing assignments in your QSF file.

3. Perform Classic timing analysis.

4. Generate an **Early Power Estimator** output file.

5. Turn on the TimeQuest Timing Analyzer again.

Project Management

If you use the **project_open** Tcl command in the TimeQuest Timing Analyzer to open a project compiled with an earlier version of the Quartus II software, the TimeQuest Timing Analyzer overwrites the compilation results (**\db** folder) without warning. Opening a project any other way results in a warning, and you can choose not to open the project.

Conversion Utility

This section describes the notes for the QSF assignment to SDC constraint conversion utility.

Virtual Clock Conversion

The conversion utility may not convert virtual clock assignments for the Classic Timing Analyzer correctly. You should manually correct any SDC constraints that should define virtual clocks.

t_{SU} & t_H Requirement Conversion

The situation described in this section only applies to the Quartus II software version 6.0. It has been corrected in the Quartus II software version 6.0 SP1.

If you use the Assignment Editor to make **t_{SU} Requirement** and **t_H Requirement** assignments to device inputs, those assignments may include a value of `*` in the **From** field (the `-from` option in the QSF), as shown in Figure 7–33.

Figure 7–33. From Field with Value

	From	To	Assignment Name	Value	Enabled
1	*	data_a	tsu Requirement	3 ns	Yes

If the **t_{SU} Requirement** and **t_H Requirement** assignment targets are `-from * -to` <*name*>, the conversion utility converts the targets to `-from [get_ports *] -to` <*name*>, which may not be what you intend if it should be a single-point assignment.

Refer to "I/O Timing Assignment Target Type Conversion" on page 7–61 for an explanation about why the conversion occurs this way.

You can edit **t_{SU} Requirement** and **t_H Requirement** assignments in the Assignment Editor to avoid this behavior, or use a script to pre-process the QSF before you run the conversion utility.

If you want to edit your assignments in the Assignment Editor, click in the **From** field for each **t_{SU} Requirement** and **t_H Requirement** assignment to a device input, and delete the asterisk (*), so each assignment looks like Figure 7–34.

Figure 7–34. No From Field Value

	From	To	Assignment Name	Value	Enabled
1		data_a	tsu Requirement	3 ns	Yes

Save your assignments when you are done. When you run the conversion utility, it will correctly convert **t_{SU} Requirement** and **t_H Requirement** assignments made to device inputs.

If you want to use a script to pre-process the QSF, save the script shown in Example 7–22 in your project directory in a file named **remove_from_star.tcl**.

Example 7–22. remove_from_star.tcl Script

```
foreach req { TSU_REQUIREMENT TH_REQUIREMENT } {
    set assignments [get_all_assignments -type instance -name $req]
    foreach_in_collection asgn_id $assignments {
        set from   [get_assignment_info $asgn_id -from]
        set to     [get_assignment_info $asgn_id -to]
        set name   [get_assignment_info $asgn_id -name]
        set value  [get_assignment_info $asgn_id -value]
        set entity [get_assignment_info $asgn_id -entity]
        if { [string equal {*} $from] } {
            set_instance_assignment -from $from -to $to -name $name \
                -entity $entity -remove $value
            set_instance_assignment -to $to -name $name \
                -entity $entity $value
            post_message "Removed -from * for $name assignment to $to"
        }
    }
}
```

Then, open your project and run the Tcl script. To run the script, type `source remove_from_star.tcl` ↵ at the Quartus II Tcl prompt. If you use the Quartus II GUI and the Tcl Console is not open, click **Utility Windows** on the View menu, and click **Tcl Console**. When you run the conversion utility, it will correctly convert **t_{SU} Requirement** and **t_H Requirement** assignments made to device inputs.

t_{PD} & Minimum t_{PD} Requirement Conversion

The conversion utility treats the targets of single-point t_{PD} and minimum t_{PD} assignments as device outputs. It does not correctly convert targets of single-point t_{PD} and minimum t_{PD} assignments that are device inputs. The following QSF assignment applies to an a device input named `d_in`.

```
set_intance_assignment -name TPD_REQUIREMENT -to d_in "3 ns"
```

The conversion utility creates the following SDC command, regardless of whether `d_in` is a device input or device output.

```
set_max_delay "3 ns" -from [get_ports *] -to [get_ports d_in]
```

You must update any incorrect SDC constraints manually.

8. Classic Timing Analyzer

QII53004-6.0.0

Introduction

Static timing analysis is a method for analyzing, debugging, and validating the timing performance of a design. The Classic Timing Analyzer analyzes the delay of every design path and analyzes all timing requirements to ensure correct circuit operation. Static timing analysis, used in conjunction with functional simulation, allows you to verify overall design operation.

For information on switching to the TimeQuest Timing Analyzer for, refer to the *Switching to the TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

As part of the compilation flow, the Quartus® II software automatically performs a static timing analysis so that you do not need to launch a separate timing analysis tool. The Classic Timing Analyzer checks every path in the design against your timing constraints for timing violations and reports results in the Timing Analysis reports, giving you immediate access to the data.

This chapter assumes you have some Tcl expertise; Tcl commands are used throughout this chapter to describe alternative methods for making timing analysis assignments. Refer to "Timing Analysis Using the Quartus II GUI" on page 8–40 for GUI-equivalent timing constraints.

This chapter discusses the following aspects of timing analysis:

- Static timing analysis overview
- Clock settings
- Clock types
- Clock uncertainty
- Clock latency
- Timing exceptions
- I/O analysis
- Asynchronous paths
- Skew management
- Generating timing analysis reports with the `report_timing` command
- Other timing analyzer features
- Timing analysis using the Quartus II GUI
- Scripting support
- MAX+PLUS® II timing analysis methodology

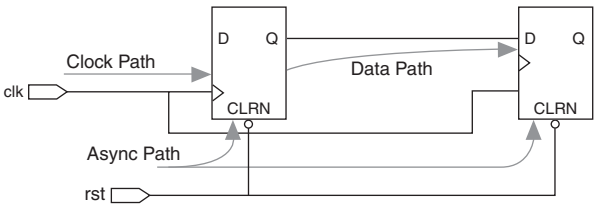
Static Timing Analysis Overview

This section provides information about static timing analysis concepts that are used throughout this chapter and by the Classic Timing Analyzer. A complete understanding of the concepts presented in this section allows you to take advantage of the powerful static timing analysis features available in the Quartus II software.

Various paths exist within any given design which connect design elements together, including the path from an output of a register to the input of another register. Timing paths play a significant role during a static timing analysis. Understanding the types of timing paths is important for timing closure and optimization. Some of the commonly analyzed paths are described in this section, and are shown in Figure 8–1.

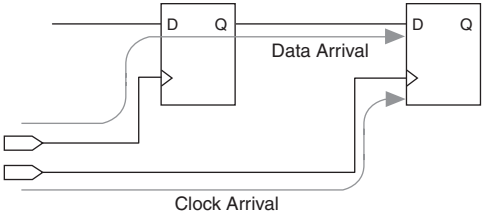
- **Clock paths**—Clock paths are the paths from device pins or internally generated clocks (nodes designated as a clock via a clock setting) to the clock ports of sequential elements such as registers.
- **Data paths**—Data paths are the paths from the data output port of a sequential element to the data input port of another sequential element.
- **Asynchronous paths**—Asynchronous paths are paths from a node to the asynchronous set or clear port of a sequential element.

Figure 8–1. Path Types



Once the path types are identified, the Classic Timing Analyzer computes data and clock arrival times for all valid register-to-register paths. Data arrival time is the delay from the source clock to the destination register. The Classic Timing Analyzer calculates this delay by adding the clock path delay to the source register, the micro clock-to-out (μt_{CO}) of the source register, and the data path delay from the source register to the destination register. Clock arrival time is the delay from the destination clock node to the destination register. Figure 8–2 shows a data arrival path and a clock arrival path.

Figure 8–2. Data Arrival & Clock Arrival

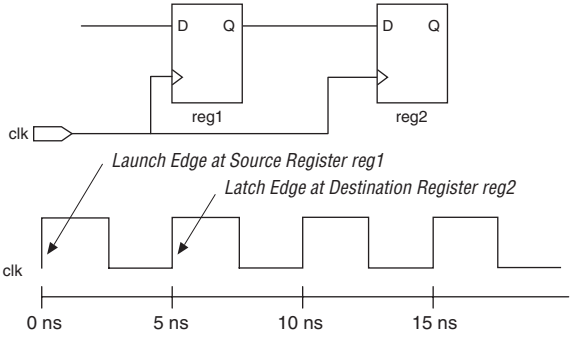


In addition to identifying various paths within a design, the Classic Timing Analyzer analyzes clock characteristics to compute the worst-case requirement between any two registers in a single register-to-register path. You must use timing constraints to specify the characteristics of all clock signals in the design before this analysis occurs.

The active clock edge that sends data out of a sequential element, acting as a source for the data transfer, is the launch edge. The active clock edge that captures data at the data port of a sequential element, acting as a destination for the data transfer, is the latch edge.

Figure 8–3 shows a single-cycle system that uses consecutive clock edges to transmit and capture data, a register-to-register path, and the corresponding launch and latch edges timing diagram. In this example, the launch edge sends the data out of register `reg1` at 0 ns, and register `reg2` latch edge captures the data at 5 ns.

Figure 8–3. Launch Edge & Latch Edge



By analyzing specific paths relative to the launch and latch edges, the Classic Timing Analyzer performs clock setup and clock hold checks, validating them against your timing assignments.

Clock Analysis

A comprehensive static timing analysis includes analysis of register-to-register, I/O, and asynchronous reset paths. Static Timing Analysis tools use data required times, data arrival times, and clock arrival times to verify circuit performance and detect possible timing violations. The Classic Timing Analyzer determines the timing relationships that must be met for the design to correctly function, and checks arrival times against required times to verify timing.

Clock Setup Check

To determine if a design meets performance, the Classic Timing Analyzer calculates clock timing, timing requirements, and timing exceptions to perform a clock setup check at each destination register based on the source and destination clocks and timing constraints, or exceptions that are applicable to those paths. A clock setup check ensures that data launched by a source register is latched correctly by the destination register. To perform a clock setup check, the Classic Timing Analyzer determines the clock arrival time and data arrival time at the destination register by using the longest path for the data arrival time and the shortest path for the clock arrival time. The Classic Timing Analyzer then checks that the difference is greater than or equal to the micro setup (t_{SU}) of the destination register as shown in Equation 1.

(1) $$\text{Clock Arrival Time} - \text{Data Arrival Time} \geq \text{micro } t_{SU}$$

By default, the Classic Timing Analyzer assumes the launched and latched edges happen on consecutive active clock edges.

The results of clock setup checks are reported in terms of slack. Slack is the margin by which a timing requirement is met or not met. Positive slack indicates the margin by which a requirement is met, and negative slack indicates the margin by which a requirement is not met. The Classic Timing Analyzer determines clock setup slack using Equations 2 through 5.

(2) $$\text{Clock Setup Slack} = \text{Data Required Time} - \text{Data Arrival Time}$$

(3) $$\text{Data Required} = \text{Clock Arrival Time} - \text{micro } t_{SU} - \text{Setup Uncertainty}$$

(4) $$\text{Clock Arrival Time} = \text{Latch Edge} + \text{Shortest Clock Path to Destination Register}$$

(5) $$\text{Data Arrival Time} = \text{Launch Edge} + \text{Longest Clock Path to Source Register} + \text{micro } t_{CO} + \text{Longest Data Delay}$$

The Classic Timing Analyzer reports clock setup slack using Equations 6 through 9 (which are equivalent to Equations 2 through 5).

(6) Clock Setup Slack = Largest Register-to-Register Requirement – Longest Register-to-Register Delay

(7) Largest Register-to-Register Requirement = Setup Relationship Between Source & Destination + Largest Clock Skew – micro t_{CO} of Source Register – micro t_{SU} of Destination Register

(8) Setup Relationship Between Source & Destination Register = Latch Edge – Launch Edge – Setup Uncertainty

(9) Largest Clock Skew = Shortest Clock Path to Destination Register – Longest Clock Path to Source Register

Both sets of equations can be used to determine the slack value of any path.

Clock Hold Check

To prevent hold violations, the Classic Timing Analyzer calculates clock timing, timing requirements, and timing exceptions to perform a clock hold check at each destination register. A clock hold check ensures data launched from the source register is not captured by an active clock edge earlier than the setup latch edge, and that the destination register does not capture data launched from the next active launch edge. To perform a clock hold check, the Classic Timing Analyzer determines the clock arrival time and data arrival time at the destination register using the shortest path for the data arrival time and the longest path for the clock arrival time. The Classic Timing Analyzer checks that the difference is greater than or equal to the micro hold time (t_H) of the destination register as shown in Equation 10.

(10) Data Arrival Time – Clock Arrival Time $\geq t_H$

The Classic Timing Analyzer determines clock hold slack using Equations 11 through 14.

(11) Clock Hold Slack = Data Arrival Time – Data Required Time

(12)

(13) Clock Arrival Time = Latch Edge + Longest Clock Path to Destination Register

(14) Data Arrival Time = Launch Edge + Shortest Clock Path to Source Register + micro t_{CO} + Shortest Data Delay

The Classic Timing Analyzer reports clock hold slack using Equations 15 through 18.

(15) Clock Hold Slack = Shortest Register-to-Register Delay – Smallest Register-to-Register Requirement

(16) Smallest Register-to-Register Requirement = Hold Relationship Between Source & Destination + Smallest Clock Skew – micro t_{CO} of Source Register + micro t_H of Destination Register

(17) Hold Relationship Between Source and Destination Register = Latch – Launch + Hold Uncertainty

(18) Smallest Clock Skew = Longest Clock Path from Clock to Destination Register – Shortest Clock Path from Clock to Source Register

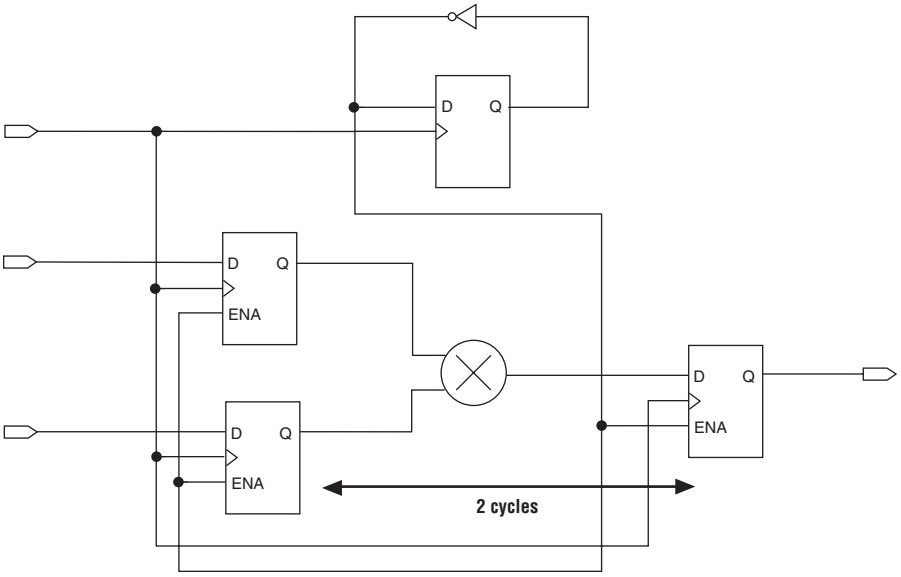
These equations can be used to determine the slack value of any path.

Multicycle Paths

Multicycle paths are data paths that require more than one clock cycle to latch data at the destination register. For example, a register may be required to capture data on every second or third rising clock edge. Figure 8–4 shows an example of a multicycle path between a multiplier's input registers and output register where the destination latches data on every other clock edge.

Refer to "Multicycle" on page 8–14 for more information on multicycle exceptions.

Figure 8–4. Example Diagram of a Multicycle Path



Clock Settings

You can use individual and default clock settings to define the clocks in your design. These clock settings can be based on other clock settings already defined in the design.

To ensure the Quartus II Fitter achieves the desired performance requirements and the Classic Timing Analyzer performs a thorough static timing analysis, you must specify all timing assignments prior to compiling the design.

Individual Clock Settings

Individual clock settings allow you to specify clock properties including performance requirements, offsets, duty cycles, and other properties for individual clock signals in your design.

You can define individual clock settings using the `create_base_clock` Tcl command. The following example defines an individual clock setting named `sys_clk` with a requirement of 100 MHz (10 ns), and assigns it to clock node `clk`.

```
create_base_clock -fmax 100MHz -target clk sys_clk
```

Default Clock Settings

You can assign a project-wide clock requirement to constrain all detected clocks in a design that do not have individual clock settings.

The `set_global_assignment -name FMAX_REQUIREMENT` Tcl command specifies a global default requirement assignment. The following example defines a 100 MHz default clock requirement:

```
set_global_assignment -name FMAX_REQUIREMENT "100.0 MHz"
```

For best placement and routing results, apply individual clock settings to all clocks in your design. All clocks adopting the default F_{MAX} are by default unrelated.

Clock Types

This section describes the types of clocks recognized by the Timing Analyzer:

- Base clocks
- Derived clocks
- Undefined clocks
- PLL clocks

Base Clocks

A base clock is independent of other clocks in a design. For example, a base clock is typically a clock signal driven directly by a device pin. A base clock is defined by individual clock settings, or automatically detected using the default clock setting.

You can use the `create_base_clock` Tcl command to define a base clock setting and assign the clock setting to a clock node. The following Tcl command creates a clock setting called `sys_clk` with a requirement of 5 ns (200 MHz) and applies the clock setting to clock node `main_clk`:

```
create_base_clock -fmax 5ns -target main_clk sys_clk
```

Derived Clocks

A derived clock is based on a previously defined base clock. For a derived clock, you can specify the phase shift, offset, multiplication and division factors, and duty cycle relative to the base clock.

You can use the create_relative_clock Tcl command to define and assign a derived clock setting. The following example creates a derived clock setting named system_clockx2 that is twice as fast as the base clock system_clock applied to clock node clkx2.

```
create_relative_clock -base_clock system_clock -duty_cycle 50 -multiply 2 -target clkx2\
system_clockx2
```

Undefined Clocks

The Classic Timing Analyzer detects undeclared clocks in your design and displays a warning similar to the following:

```
Warning: Found pins functioning as undefined clocks and/or memory enables
    Info: Assuming node "clk_src" is an undefined clock
    Info: Assuming node "clk_dst" is an undefined clock
```

The Classic Timing Analyzer reports actual data delay for undefined clocks, but because no clock requirements exist for undefined clocks, the Classic Timing Analyzer does not report slack for any register-to-register paths driven by an undefined clock.

PLL Clocks

Phase-locked loops (PLLs) are used for clock synthesis in Altera® devices. This device feature is configured and connected to your design using the altpll megafunction included with the Quartus II software. Using the MegaWizard® Plug-In Manager, you can customize the input clock frequency, multiplication factors, division factors, and other parameters of the altpll megafunction.

For more information on using the PLL feature in your design, refer to the *altpll Megafunction User Guide* or the handbook for the targeted device family.

For PLLs, the Classic Timing Analyzer automatically creates derived clock settings based on the parameterization of the PLL, and automatically creates a base clock setting for the input clock pin. For example, if the input clock frequency to a PLL is 100 MHz and the multiplication and division ratio is 5:2, the clock period of the PLL clock is set to 4.0 ns and is automatically calculated by the Classic Timing Analyzer.

For the Stratix® and Cyclone™ device families, you can override the PLL input clock frequency by applying a clock setting to the input clock pin of the PLL. For example, if the PLL input clock period is set to 10 ns (100 MHz) with a multiplication and division ratio of 5:2, but a clock

setting of 20 ns (50 MHz) is applied to the input clock pin of the PLL, the setup relationship is 8.0 ns (125 MHz) and not 4.0 ns (250 MHz). The Classic Timing Analyzer issues a message similar to the following:

```
Warning: ClockLock PLL "mypll_test:inst|altpll:altpll_component|_clk1" input frequency
requirement of 200.0 MHz overrides default required fmax of 100.0 MHz -- Slack information
will be reported
```

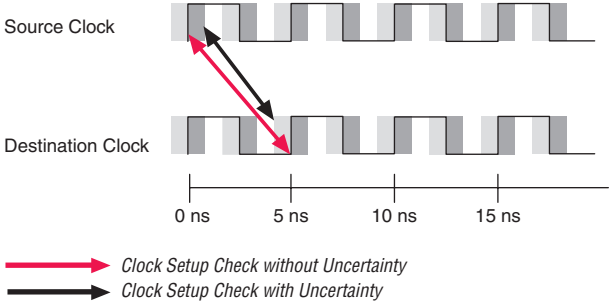
You cannot override the PLL output clock frequency with a clock setting in the Classic Timing Analyzer.

Clock Uncertainty

You can use **Clock Setup Uncertainty** and **Clock Hold Uncertainty** assignments to model jitter, skew, or add a guard band associated with clock signals.

When a clock uncertainty assignment exists for a clock signal, the Timing Analyzer performs the most conservative setup and hold checks. For clock setup check, the setup uncertainty is subtracted from the data required time. Figure 8–5 shows an example of clock sources with a clock setup uncertainty applied.

Figure 8–5. Clock Setup Uncertainty

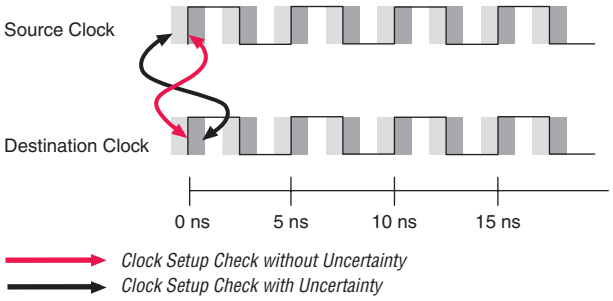


You can create clock uncertainty assignments using the Tcl command `set_clock_uncertainty`. The `set_clock_uncertainty` assignment used with the switch `–setup` specifies a clock setup uncertainty assignment. The following example creates a **Clock Setup Uncertainty** assignment with a value of 2 ns applied to clock signal `clk`:

```
set_clock_uncertainty -to clk -setup 2ns
```

For the clock hold check, the hold uncertainty is added to the data required time. Figure 8–6 shows an example of clock setup check with a clock setup uncertainty and clock hold uncertainty applied.

Figure 8–6. Clock Hold Uncertainty



You can use the `set_clock_uncertainty` Tcl command with the option `-hold` to specify a **Clock Hold Uncertainty** assignment. The following example creates a **Clock Hold Uncertainty** assignment with a value of 2 ns for clock signal `clk`.

```
set_clock_uncertainty -to clk -hold 2ns
```

You can also apply the clock uncertainty assignments between two clock sources. The following example creates a **Clock Setup Uncertainty** for clock setup checks where `clk1` is the source clock and `clk2` is the destination clock:

```
set_clock_uncertainty -from clk1 -to clk2 -setup 2ns
```

Clock Latency

You can use clock latency assignments to model delays from the clock source. For example, you can use clock latency to model an external delay from an ideal clock source, such as an oscillator, to the clock pin or port of the device.

The **Early Clock Latency** assignment allows you to specify the shortest or earliest delay of the clock source. Conversely, the **Late Clock Latency** assignment allows you to specify the longest or latest delay of the clock source.

During setup analysis, the Classic Timing Analyzer adds the **Late Clock Latency** assignment value to the source clock path delay and adds the **Early Clock Latency** assignment value to the destination clock path delay when determining clock skew for the path. During clock hold analysis, the Classic Timing Analyzer adds the **Early Clock Latency** assignment value to the source clock path delay and adds the **Late Clock Latency** assignment value to the destination clock path delay when determining clock skew for the path.

The **Early Clock Latency** and **Late Clock Latency** assignments do not change the latch and launch edges defined by the clock setting, and therefore does not change the setup or hold relationships between source and destination clocks. The clock latency assignments add only delay to the clock network, and therefore only affects clock skew.

Figure 8–7 shows the clock edges used to calculate clock skew for a setup check when the **Early Clock Latency** and **Late Clock Latency** assignments are used.

Figure 8–7. Clock Setup Check Clock Skew

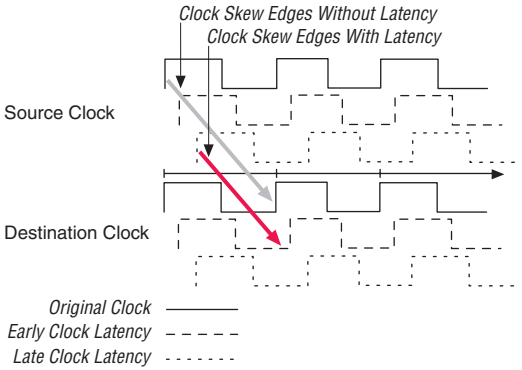
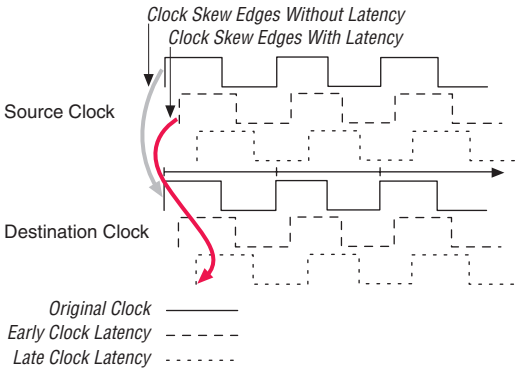


Figure 8–8 shows the clock edges used to calculate clock skew for a hold check when the **Early Clock Latency** and **Late Clock Latency** assignments are used.

Figure 8–8. Clock Hold Check Clock Skew



The Classic Timing Analyzer ignores clock latency if the clock signal at the source and destination registers are the same.

You can use the `set_clock_latency` Tcl command with the switches `-early` or `-late` to specify an **Early Clock Latency** assignment or **Late Clock Latency** assignment, respectively. The following example specifies that the clock signal at `clk2` arrives as early as 1.8 ns and as late as 2.0 ns.

```
set_clock_latency -early -to clk2 1.8ns
set_clock_latency -late -to clk2 2ns
```

The early clock latency default value is the same as the late clock latency delay, and the late clock latency default value is the same as the early clock latency delay, if only one is specified.

The Enable Clock Latency option must be set to `ON` for the Classic Timing Analyzer to analyze clock latency. When this option is set to `ON`, the Classic Timing Analyzer reports clock latency as part of the clock skew calculation for either the source or destination clock path depending upon the analysis performed. To set the Enable Clock Latency option to `ON`, you can use the following Tcl command:

```
set_global_assignment -name ENABLE_CLOCK_LATENCY ON
```

When the Enable Clock Latency option is enabled, the Classic Timing Analyzer automatically calculates latencies for derived clocks instead of automatically calculating offsets, for example, PLL compensation delays. These clock path delays are accounted for as clock skew instead of part of the setup or hold relationship as done with offsets.

Timing Exceptions

Timing exceptions allow you to modify the default behavior of the Classic Timing Analyzer. This section describes the following timing exceptions:

- Multicycle
- Setup relationship and hold relationship
- Maximum delay and minimum delay
- False paths

Not all timing exceptions presented in this chapter are applicable to the HardCopy II devices. If you are designing for the HardCopy II device family, refer to the *Timing Constraint for HardCopy II* chapter in the *HardCopy II Handbook*.

Multicycle

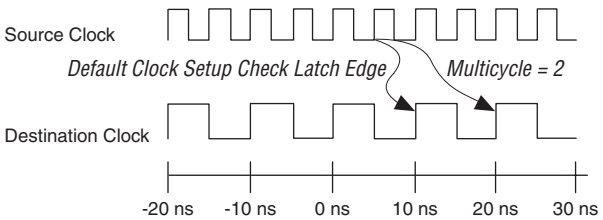
By default, the Classic Timing Analyzer performs a single-cycle analysis for all valid register-to-register paths in the design. Multicycle assignments specify the number of clock periods before a source register launches the data or a destination register latches the data. Multicycle assignments adjust the latch or launch edges, which relaxes the required clock setup check or clock hold check between the source and destination register pairs. You can specify multicycles separately for setup and hold, and multicycles can be based on the source clock or destination clock. Apply **Multicycle** exception to time groups, clock nodes, or common clock enables.

Destination Multicycle Setup Exception

A destination multicycle setup, referred to as a **Multicycle** exception, specifies the minimum number of clock cycles required before a register should latch a value. A **Multicycle** exception changes the latch edge by relaxing the required setup relationship. Figure 8–9 shows a timing diagram for a multicycle path that exists in a design with related clocks, with the latch edge label for a clock setup check.

By default, the **Multicycle** exception value is 1.

Figure 8–9. Multicycle Setup



You can apply **Multicycle** exception between any two registers or between any two clock domains. Use the Tcl command `set_multicycle_assingment`, and the switch `-setup` and `-end`. For example, to apply a **Multicycle** exception of 2 between all registers clocked by source clock `clk_src`, and all registers clocked by destination clock `clk_dst`, enter the following Tcl command:

```
set_multicycle_assignment -setup -end -from clk_src -to clk_dst 2
```

To apply a **Multicycle** exception of 2 between the source register `reg1` and the destination register `reg2`, enter the following Tcl command:

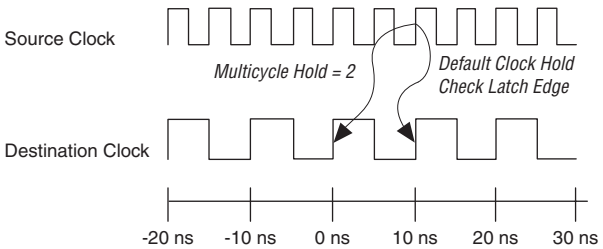
```
set_multicycle_assignment -setup -end -from reg1 -to reg2 2
```

Destination Multicycle Hold Exception

A destination multicycle hold, referred to as a **Multicycle Hold** exception, modifies the latch edge used for a clock hold check for the register-to-register path based on the destination clock. A **Multicycle Hold** exception changes the latch edge by relaxing the required hold relationship. Figure 8–10 shows a timing diagram labeling the latching edge for a clock setup check.

If no **Multicycle Hold** value is specified, the **Multicycle Hold** value defaults to the value of the multicycle exception.

Figure 8–10. Multicycle Hold



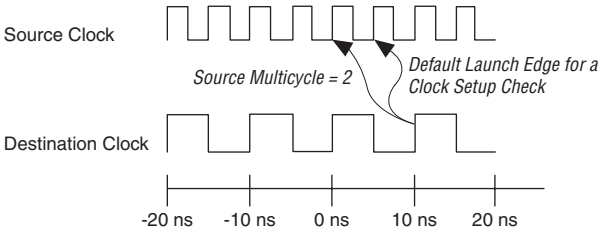
You can create **Multicycle Hold** exceptions with the Tcl command `set_multicycle_assingment` and the switch `-hold` and `-end`. The following example specifies a **Multicycle Hold** exception of 3 from register `reg1` to register `reg2`:

```
set_multicycle_assignment -hold -end -from reg1 -to reg2 3
```

Source Multicycle Setup Exception

A source multicycle setup, referred to as **Source Multicycle Setup** exception, is used to extend the required delay by adjusting the source clock's launch edge rather than the destination clock's latch edge, for example, multicycle setup. **Source Multicycle** exceptions are useful when the source and destination registers are clocked by related clocks at different frequencies. Figure 8–11 shows an example of a **Source Multicycle** exception with the launch edge labeled for a clock setup check.

Figure 8–11. Source Multicycle



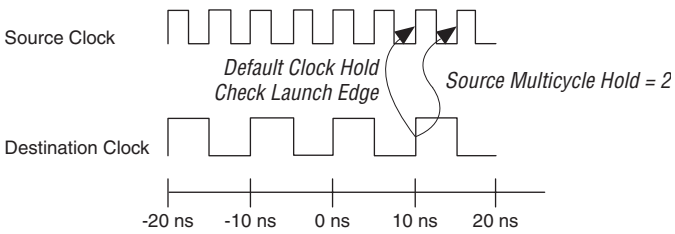
You can create **Source Multicycle Setup** exceptions with the Tcl command `set_multicycle_assignment` and the switches `-setup` and `-start`. The following example specifies a **Source Multicycle** exception of 3 from register `reg1` to register `reg2`:

```
set_multicycle_assignment -setup -start -from reg1 -to reg2 3
```

Source Multicycle Hold Exception

The **Source Multicycle Hold** exception modifies the latch edge used for a clock hold check for the register-to-register path based on the source clock. **Source Multicycle Hold** exceptions increase the required hold delay by adding source clock cycles. Figure 8–12 shows an example of a source multicycle hold with launch edge labeled for a clock hold check.

Figure 8–12. Source Multicycle Hold



You can create **Source Multicycle Hold** exceptions with the Tcl command `set_multicycle_assingment` and the switch `-setup` and `-start`. The following example specifies a **Source Multicycle Hold** exception of 3 from register `reg1` to register `reg2`:

```
set_multicycle_assignment -hold -start -from reg1 -to reg2 3
```

Default Hold Multicycle

The Classic Timing Analyzer sets the hold multicycle value to equal the multicycle value when a multicycle exception has been entered without a corresponding hold multicycle. The behavior can be changed with the `DEFAULT_HOLD_MULTICYCLE` assignment. The value of the assignment can either be `"ONE"` or `"SAME AS MULTICYCLE"`.

The assignment has the following syntax:

```
set_global_assignment -name DEFAULT_HOLD_MULTICYCLE "<value>"
```

Clock Enable Multicycle

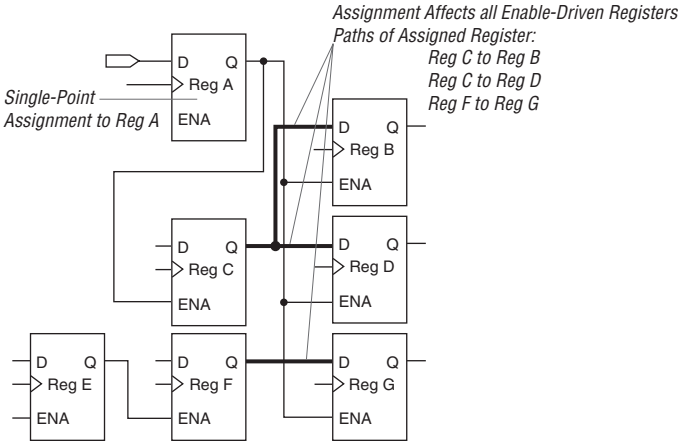
For all enable-driven registers, the setup relationship or hold relationship can be modified with the **Clock Enable Multicycle**, **Clock Enable Multicycle Hold**, **Clock Enable Source Multicycle**, or **Clock Enable Multicycle Source Hold**.

The Clock Enable Multicycle modifies the latching edge when a clock setup check is performed for all registers driven by the specified clock enables, and the Clock Enable Multicycle Hold modifies the latching edge when a clock hold check is performed for all registers driven by the specified clock enable. The Clock Enable Source Multicycle modifies the launching edge when a clock setup check is performed for all enabled driven registers, and the Clock Enable Source Multicycle Hold modifies the launching edge when a clock hold check is performed for all enabled driven registers.

Clock Enable-based multicycle exceptions apply only to registers using dedicated clock enable circuitry. If the enable is synthesized into a logic cell, for example, due to signal prioritization, the multicycle does not apply.

The **Clock Enable Multicycle**, **Clock Enable Multicycle Hold**, **Clock Enable Source Multicycle**, and **Clock Enable Multicycle Source Hold** can be either a single-point or a point-to-point assignment. Figure 8–13 shows an example of a single-point assignment. In this example, register `Reg A` has the single-point assignment applied. This has the affect of modifying a register-to-register latching edge whose enable port is driven by register `Reg A`. All register-to-register paths with enables driven by the single-point assignment are affected, even those driven by different clock sources.

Figure 8–13. Single-Point Clock Enable Multicycle



Point-to-point assignments apply to all paths where the source registers' enable ports are driven by the source (from) node and the destination registers' enable ports are driven by the destination (to) node. Figure 8–14 shows an example of a point-to-point assignment made to different source and destination registers. In this example, register `Reg A` is specified as the source, and register `Reg B` is specified as the destination for the assignment. Only register-to-register paths that have their enables driven by the assigned point-to-point registers have their latching edges modified.

Figure 8–14. Different Source & Destination Point-to-Point Assignment Clock Enable Multicycle

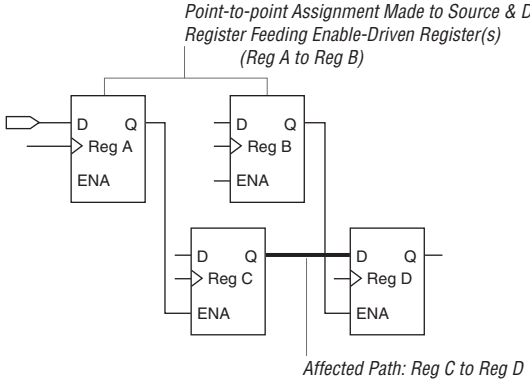
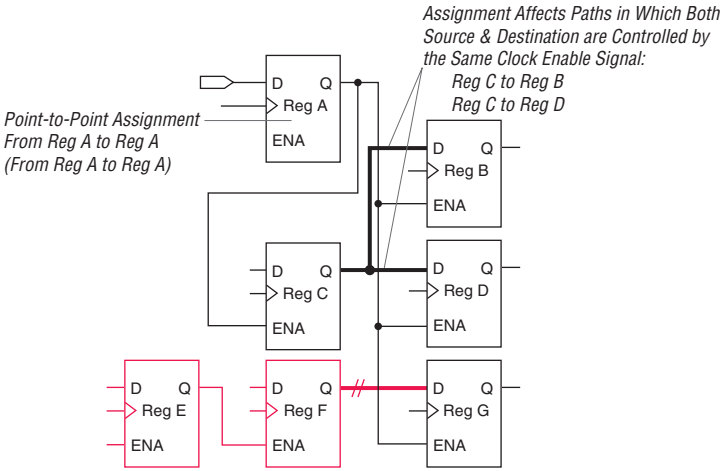


Figure 8–15 shows an example of a point-to-point assignment made to the same source and destination register. In this example, register `Reg A` has been specified as both the source and register for the assignment. Only register-to-register paths that have both the source enable port and destination enable port has the latching edge modified by the assigned point-to-point assignment.

Figure 8–15. Same Source & Destination Point-to-Point Assignment Clock Enable Multicycle



You can use the `set_instance_assignment -name CLOCK_ENABLE_MULTICYCLE` and `set_instance_assignment -name CLOCK_ENABLE_MULTICYCLE_HOLD` Tcl commands to specify either a **Clock Enable Multicycle** or a **Clock Enable Multicycle Hold** assignment, respectively. The following example specifies a single-point **Clock Enable Multicycle** assignment of 2 ns to `reg1`:

```
set_instance_assignment -name CLOCK_ENABLE_MULTICYCLE 2 -to reg1
```

The following example specifies a point-to-point **Clock Enable Multicycle Hold** assignment of 2 from register `reg1` to register `reg2`:

```
set_instance_assignment -name CLOCK_ENABLE_MULTICYCLE_HOLD 2 -from reg1 -to reg2
```

You can use the `set_instance_assignment -name CLOCK_ENABLE_SOURCE_MULTICYCLE` and `set_instance_assignment -name CLOCK_ENABLE_MULTICYCLE_SOURCE_HOLD` Tcl commands to specify either a **Clock Enable Multicycle** or **Clock Enable Multicycle Hold** assignment, respectively. The following example specifies a single-point **Clock Enable Multicycle** assignment of 2 ns to `reg1`:

```
set_instance_assignment -name CLOCK_ENABLE_SOURCE_MULTICYCLE 2 -to reg1
```

The following example specifies a point-to-point **Clock Enable Multicycle Hold** assignment of 2 from register `reg1` to register `reg2`:

```
set_instance_assignment -name CLOCK_ENABLE_SOURCE_MULTICYCLE_HOLD 2 -from reg1 -to reg2
```

Setup Relationship & Hold Relationship

By default, the Classic Timing Analyzer determines all setup and hold relationships based on clock settings. The **Setup Relationship** and **Hold Relationship** exceptions allow you to override any default setup or hold relationships. Example 8–1 shows the path details of a register-to-register path that has a 10 ns clock setting applied to the clock signal driving the 2 registers.

Example 8–1. Default Setup Relationship with 10 ns Clock Setting

```
Info: Slack time is 9.405 ns for clock "data_clk" between source register "reg9" and
destination register "reg10"
    Info: Fmax is restricted to 500.0 MHz due to tcl and tch limits
    Info: + Largest register to register requirement is 9.816 ns
        Info: + Setup relationship between source and destination is 10.000 ns
            Info: + Latch edge is 10.000 ns
            Info: - Launch edge is 0.000 ns
        Info: + Largest clock skew is 0.000 ns
        Info: - Micro clock to output delay of source is 0.094 ns
        Info: - Micro setup delay of destination is 0.090 ns
    Info: - Longest register to register delay is 0.411 ns
```

In Example 8–2, a 15 ns **Setup Relationship** exception is applied to the register-to-register path, overriding the default 10 ns setup relationship.

Example 8–2. Setup Relationship Assignment of 15 ns

```
Info: Slack time is 14.405 ns for clock "data_clk" between source register "reg9" and
destination register "reg10"
  Info: Fmax is restricted to 500.0 MHz due to tcl and tch limits
  Info: + Largest register to register requirement is 14.816 ns
    Info: + Setup relationship between source and destination is 15.000 ns
    Info: Setup Relationship assignment value is 15.000 ns between source "reg9" and
    destination "reg10"
    Info: + Largest clock skew is 0.000 ns
    Info: Total interconnect delay = 1.583 ns ( 51.31 % )
  Info: - Micro clock to output delay of source is 0.094 ns
  Info: - Micro setup delay of destination is 0.090 ns
Info: - Longest register to register delay is 0.411 ns
```

You can create a **Setup Relationship** exception with the Tcl command `set_instance_assignment -name SETUP_RELATIONSHIP`. The following example specifies a **Setup Relationship** exception of 5 ns from register `reg1` to register `reg2`:

```
set_instance_assignment -name SETUP_RELATIONSHIP 5ns -from reg1 -to reg2
```

You can use **Hold Relationship** exception to override the default hold relationship of any register-to-register paths.

You can use the `set_instance_assignment -name HOLD_RELATIONSHIP` Tcl command to specify a hold relationship assignment. The following example specifies a **Hold Relationship** exception of 1 ns from register `reg1` to register `reg2`:

```
set_instance_assignment -name HOLD_RELATIONSHIP 1ns -from reg1 -to reg2
```

Maximum Delay & Minimum Delay

You can use **Maximum Delay** and **Minimum Delay** assignments to specify delay requirements for pin-to-register, register-to-register, and register-to-pin paths. The **Maximum Delay** assignment overrides any setup relationship for any path. The **Minimum Delay** assignment overrides any hold relationship for any path.

The Classic Timing Analyzer ignores the effects of clock skew when checking a design against **Maximum Delay** and **Minimum Delay** assignments.

You can use the `set_instance_assignment -name MAX_DELAY` and `set_instance_assignment -name -MIN_DELAY` Tcl commands to specify a **Maximum Delay** assignment or a **Minimum Delay** assignment, respectively. The following example specifies a maximum delay of 2 ns between source register `reg1` and destination register `reg2`:

```
set_instance_assignment -name MAX_DELAY 2ns -from reg1 -to reg2
```

The following example specifies a minimum delay of 1 ns between input pin `data_in` to destination register `dst_reg`:

```
set_instance_assignment -name MIN_DELAY 1ns -from data_in -to dst_reg
```

False Paths

A false path is any path that is not relevant to a circuit's operation, such as test logic. There are several global assignments to cut different classes of paths, such as unrelated clock domains and paths through bidirectional pins, but you can also cut an individual timing path to a specific false paths.

The Timing Analyzer provides the following three global options that allow you to remove false paths from your design:

- Cut off feedback from I/O pins
- Cut off read during write signal paths
- Cut paths between unrelated clock domains

You can use the `set_global_assignment -name CUT_OFF_IO_PIN_FEEDBACK ON` Tcl command to cut the feedback path when a bidirectional I/O pin is connected directly or indirectly to both the input and the output of a latch.

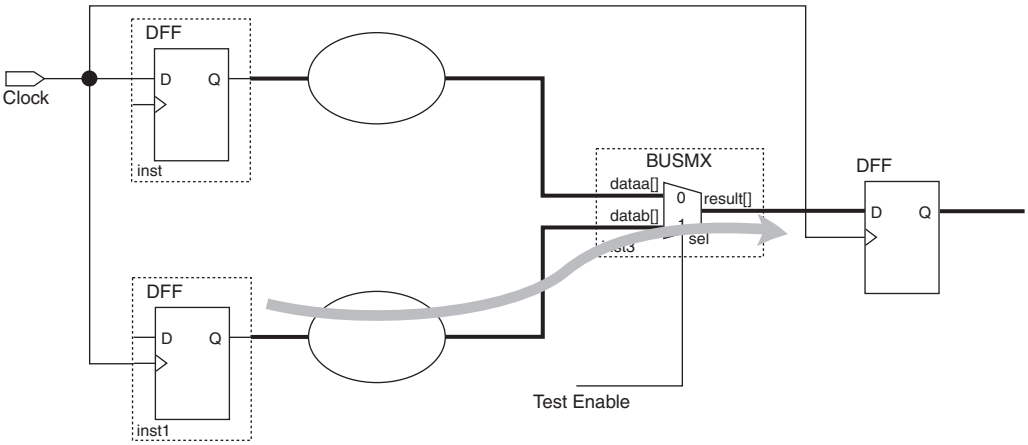
You can use the `set_global_assignment -name CUT_OFF_READ_DURING_WRITE_PATHS ON` Tcl command to cut the path from the write enable register through memory element to a destination register.

You can use the `set_global_assignment -name CUT_OFF_PATHS_BETWEEN_CLOCK_DOMAINS ON` Tcl command to cut paths between register-to-register where the source and destination clocks are different.

You can use the `set_timing_cut_assignment` Tcl command to cut specific timing paths. In Figure 8–16, the path from `inst1` through the multiplexer to `inst2` is used only for design testing. This false path is not

required under normal operation and does not need to be analyzed during static timing analysis. Figure 8–16 shows an example of a false path.

Figure 8–16. False Path Signal



To cut the timing path from source register `inst1` to destination register `inst2`, enter the following Tcl command:

```
set_timing_cut_assignment -from inst1 -to inst2
```

The `set_timing_cut_assignment` Tcl command can also be used as a single point assignment. When the single point assignment is used, all fanout of the node is cut. For example, the following Tcl command cuts all timing paths originating for node `src_reg`:

```
set_timing_cut_assignment -to src_reg
```

I/O Analysis

The I/O analysis performed by the Classic Timing Analyzer ensures your Altera FPGA design meets all timing specifications for interfacing with external devices. This section describes assignments relevant to I/O analysis and other I/O Analysis features and options available with the Classic Timing Analyzer.

External Input Delay & Output Delay Assignments

External input and output delays represent delays from or to external devices or boards traces. You can make Input Delay and Output Delay assignments to ensure the Classic Timing Analyzer can perform a full

system analysis. By providing Input Delays and Output Delays, the Classic Timing Analyzer is able to perform clock setup and clock hold checks for these paths. This also allows other timing assignments, such as multicycle or clock uncertainty, to be applied to input and output paths.

Do not combine individual or global t_{SU}, t_H, t_{PD}, t_{CO}, minimum t_{CO}, or minimum t_{PD} assignments with Input Delay or Output Delay assignments.

Input Delay Assignment

External input delays are specified with either **Input Maximum Delay** or **Input Minimum Delay** assignments. Make **Input Maximum Delay** assignments to specify the maximum delay of a signal from an external register to a specified input or bidirectional pin on the FPGA relative to a specified clock source. Make **Input Minimum Delay** assignments to specify the minimum delay of a signal from an external register to a specified input or bidirectional pin on the FPGA relative to a specified clock source.

When performing a clock setup check, the Classic Timing Analyzer adds the **Input Maximum Delay** assignment value to the data arrival time (or subtracts the assignment value from the point-to-point requirement).

When performing a clock hold check, the Classic Timing Analyzer adds the **Input Minimum Delay** assignment value to the data arrival time (or subtracts the assignment value from the point-to-point requirement).

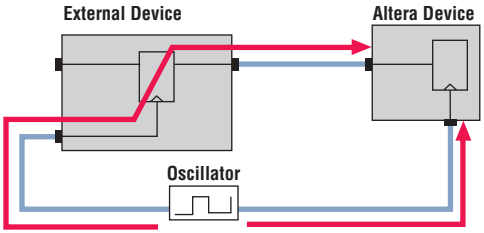
The value of the input delay assignment usually represents the sum of the t_{CO} of the external device, the actual board delay to the input pin of the Altera device, and the board clock skew.

The Input Minimum Delay defaults to the Input Maximum Delay and the Input Maximum Delay defaults to the Input Minimum Delay if only one is specified.

For example, the Input Maximum Delay and Input Minimum Delay can be used to model the delay associated with an external device driving into an Altera FPGA. Figure 8–17 shows an example of the input delay path. For Figure 8–17, the Input Maximum Delay can be calculated as shown in Equation 19.

(19)
$$\text{Input Maximum Delay} = \text{External Device Board Clock Path} + \text{External Device } t_{CO} + \text{External Device to Altera Device Board Delay} - \text{External Clock Path to Altera Device}$$

Figure 8–17. Input Delay



Use the Tcl command `set_input_delay` to specify an input delay. The following example specifies an Input **Maximum Delay** assignment of 1.5 ns from clock node `clk` to input pin `data_in`:

```
set_input_delay -clk_ref clk -to "data_in" -max 1.5ns
```

The following example specifies an **Input Minimum Delay** assignment of 1 ns from clock node `clk` to input pin `data_in`:

```
set_input_delay -clk_ref clk -to "data_in" -min 1ns
```

When using Input Delay assignments, specify a specific clock reference. This allows the Classic Timing Analyzer to perform the proper analysis for the input path.

The t_{SU}, t_H, t_{PD}, and min t_{PD} timing paths reported for input pins, where input delay internal to the Altera FPGA assignments has been applied, include only the data delay from these pins and do not account for any clock setup relationships, clock hold relationships, or slack.

Output Delay Assignment

You can specify external output delays with either **Output Maximum Delay** or **Output Minimum Delay** assignments. Make **Output Maximum Delay** assignments to specify the maximum delay of a signal from the specified FPGA output pin to an external register, relative to a specified clock source. Make **Output Minimum Delay** assignments to specify the minimum delay of a signal from the specified FPGA output pin to an external register, relative to a specified clock source.

When performing a clock setup check, the Classic Timing Analyzer subtracts the **Output Maximum Delay** assignment value from the data required time (or subtracts the assignment value from the point-to-point requirement).

When performing a clock hold check, the Classic Timing Analyzer subtracts the **Output Minimum Delay** assignment value from the data required time (or subtracts the assignment value from the point-to-point requirement).

The value of this assignment usually represents the sum of the t_{SU} of the external device, the actual board delay from the output pin of the Altera device, and the board clock skew.

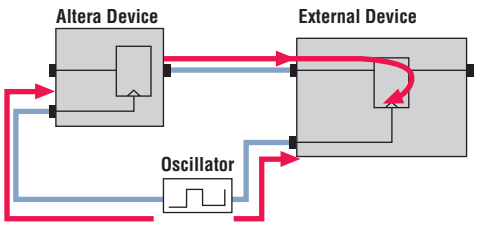
The **Output Minimum Delay** default value is the same as the **Output Maximum Delay**, and the **Output Maximum Delay** default value is the same as the **Output Minimum Delay** if only one is specified.

For example, use the **Output Maximum Delay** and **Output Minimum Delay** to model the delay associated with outputs for an Altera FPGA driving into an external device. Figure 8–18 shows an example of an output delay path. For Figure 8–18 the **Output Maximum Delay** can be calculated as shown in Equation 20.

(20)

$$\text{Output Maximum Delay} = \text{Altera Device to External Device Board Delay} + \text{External Device } t_{SU} + \text{External Clock Path to Altera Device} - \text{External Device Board Clock Path}$$

Figure 8–18. Output Delay



The Tcl command `set_output_delay` specifies an **Output Delay** assignment. The following example specifies an **Output Maximum Delay** assignment of 2 ns from clock `clk` to output pin `data_out`:

```
set_output_delay -clk_ref clk -to data_out -max 2ns
```

The following example specifies an **Output Minimum Delay** assignment of 1 ns from clock `clk` to output pin `data_out`:

```
set_output_delay -clk_ref clk -to data_out -min 1ns
```

When using output delay assignments, specify a specific clock reference. This allows the Classic Timing Analyzer to perform the correct static timing analysis on the output path.

The t_{CO}, minimum t_{CO}, t_{PD}, and minimum t_{PD} timing paths reported for output pins, where output delay assignments have been applied include only the data delay internal to the Altera FPGA to those pins, and do not account for any clock setup relationships, clock hold relationships, or slack.

Virtual Clocks

Virtual clocks can be used to model clock signals outside of the Altera FPGA, that is, clocks that do not directly drive anything within the Altera FPGA. For example, a virtual clock can be used to model a clock signal feeding an external output register that feeds the Altera FPGA.

Using the `-virtual` option of the `create_base_clock` Tcl command specifies a virtual clock assignment.

Before a virtual clock can be used for either an input or output delay assignment, the virtual clock must have the **Virtual Clock Reference** assignment enabled for the virtual clock setting.

The code in Example 8–3 creates a virtual clock named `virt_clk`, with a 200 MHz requirement, and uses the virtual clock setting as the clock reference for the input delay assignment.

Example 8–3. Creating a Virtual Clock Named virt_clk

```
#create the virtual clock setting
create_base_clock -fmax 200MHz -virtual virt_clk

#enable the virtual clock reference for the virtual clock setting
set_instance_assignment -name VIRTUAL_CLOCK_REFERENCE On -to virt_clk

#use the virtual clock setting as the clock reference for the input delay assignment
set_input_delay -clk_ref virt_clk -to data_in -max 2ns
```

Asynchronous Paths

The Classic Timing Analyzer can analyze asynchronous signals that connect to the clear, preset, or load ports of a register. This section explains how the Classic Timing Analyzer analyzes asynchronous paths.

Recovery & Removal

Recovery time is the minimum length of time an asynchronous control signal, for example, clear and preset, must be stable before the active clock edge. Removal time is the minimum length of time an asynchronous control signal must be stable after the active clock edge. The **Enable Recovery/Removal** analysis option reports the results of recovery and removal checks for paths that end at an asynchronous clear, preset, or load signal of a register.

Enable the recovery and removal analysis with the following Tcl command:

```
set_global_assignment -name ENABLE_RECOVERY_REMOVAL_ANALYSIS ON
```

With this option enabled, the Classic Timing Analyzer reports the result of the recovery analysis and removal analysis.

By default, the recovery and removal analysis is disabled. This option should be enabled for all designs that contain asynchronous controls signals.

Recovery Report

When you set `ENABLE_RECOVERY_REMOVAL_ANALYSIS` to `ON`, the Classic Timing Analyzer determines the recovery time as the minimum amount of time required between an asynchronous control signal becoming inactive and the next active clock edge, compares this to your design, and reports the results as slack. The Recovery report alerts you to conditions where an active clock edge occurs too soon after the asynchronous input becomes inactive, rendering the register's data uncertain.

The recovery slack time calculation is similar to the calculation for clock setup slack, which is based on data arrival time and data required time except for asynchronous control signals. If the asynchronous control is registered, the Classic Timing Analyzer calculates the recovery slack time using Equations 21 through 23.

(21) Recovery Slack Time = Data Required Time – Data Arrival Time

(22) Data Arrival Time = Launch Edge + Longest Clock Path to Source Register + micro t_{CO} of Source Register + Longest Register-to-Register Delay

(23) Data Required Time = Latch Edge + Shortest Clock Path to Destination Register – micro t_{SU} of Destination Register

Example 8–4 shows recovery time as reported by the Timing Analyzer.

Example 8–4. Recovery Time Reporting for a Registered Asynchronous Reset Signal

```
Info: Slack time is 8.947 ns for clock "a_clk" between source register "async_reg1" and destination
register "reg_1"
    Info: Requirement is of type recovery
    Info: - Data arrival time is 4.028 ns
        Info: + Launch edge is 0.000 ns
              Info: + Longest clock path from clock "a_clk" to source register is 3.067 ns
        Info: + Micro clock to output delay of source is 0.094 ns
        Info: + Longest register to register delay is 0.867 ns
    Info: + Data required time is 12.975 ns
        Info: + Latch edge is 10.000 ns
              Info: + Shortest clock path from clock "a_clk" to destination register is 3.065 ns
        Info: - Micro setup delay of destination is 0.090 ns
```

If the asynchronous control is not registered, the Classic Timing Analyzer uses Equations 24 through Equations 26 to calculate the recovery slack time.

(24) Recovery Slack Time = Data Required Time – Data Arrival Time

(25) Data Arrival Time = Launch Edge + Maximum Input Delay + Maximum Pin to Register Delay

(26) Data Required Time = Latch Edge + Shortest Clock Path to Destination Register Delay – micro t_{SU} of Destination Register

Example 8–5 shows recovery time as reported by the Timing Analyzer.

Example 8–5. Recovery Time Reporting for a Non-Registered Asynchronous Reset Signal

```
Info: Slack time is 8.744 ns for clock "a_clk15" between source pin "a_arst2" and
destination register "inst5"
          Info: Requirement is of type recovery
          Info: - Data arrival time is 4.787 ns
                    Info: + Launch edge is 0.000 ns
                    Info: + Max Input delay of pin is 1.500 ns
                    Info: + Max pin to register delay is 3.287 ns
          Info: + Data required time is 13.531 ns
    Info: + Latch edge is 10.000 ns
    Info: + Shortest clock path from clock "a_clk15" to destination register
    is 3.542 ns
                  Info: - Micro setup delay of destination is 0.011 ns
```

If the asynchronous reset signal is from a device pin, an **Input Maximum Delay** assignment must be made to the asynchronous reset pin for the Classic Timing Analyzer to perform recovery analysis on that path.

Removal Report

When you set ENABLE_RECOVERY_REMOVAL_ANALYSIS to ON, the Classic Timing Analyzer determines the removal time as the minimum amount of time required between an active clock edge that occurs while an asynchronous input is active, and the deassertion of the asynchronous control signal. The Classic Timing Analyzer then compares this to your design, and reports the results as slack. The Removal report alerts you to a condition in which an asynchronous input signal goes inactive too soon after a clock edge, thus rendering the register's data uncertain.

The removal time slack calculation is similar to the one used to calculate clock hold slack, which is based on data arrival time and data required time except for asynchronous control signals. If the asynchronous control is registered, the Classic Timing Analyzer uses Equations 27 through 29 to calculate the removal slack time.

(27) $$\text{Removal Slack Time} = \text{Data Arrival Time} - \text{Data Required Time}$$

(28) $$\text{Data Arrival Time} = \text{Launch Edge} + \text{Shortest Clock Path From Source Register Delay} + \text{Micro } t_{CO} \text{ of Source Register} + \text{Shortest Register-to-Register Delay}$$

(29) $$\text{Data Required Time} = \text{Latch Edge} + \text{Longest Clock Path to Destination Register Delay} + \text{micro } t_{H} \text{ of Destination Register}$$

Example 8–6 shows removal time as reported by the Classic Timing Analyzer.

Example 8–6. Removal Time Reporting for a Registered Asynchronous Reset Signal

```
Info: Minimum slack time is 814 ps for clock "a_clk" between source register "async_reg1"
and destination register "reg_1"
    Info: Requirement is of type removal
    Info: + Data arrival time is 4.028 ns
        Info: + Launch edge is 0.000 ns
        Info: + Shortest clock path from clock "a_clk" to source register is 3.067 ns
        Info: + Micro clock to output delay of source is 0.094 ns
        Info: + Shortest register to register delay is 0.867 ns
    Info: - Data required time is 3.214 ns
        Info: + Latch edge is 0.000 ns
       Info: + Longest clock path from clock "a_clk" to destination register is 3.065 ns
        Info: + Micro hold delay of destination is 0.149 ns
```

If the asynchronous control is not registered, the Classic Timing Analyzer uses Equations 30 through 32 to calculate the removal slack time.

(30) Removal Slack Time = Data Arrival Time – Data Required Time

(31) Data Arrival Time = Launch Edge + Input Minimum Delay of Pin + Minimum Pin to Register Delay

(32) Data Required Time = Latch Edge + Longest Clock Path to Destination Register Delay + micro t_H of Destination Register

Example 8–7 shows removal time as reported by the Classic Timing Analyzer.

Example 8–7. Removal Time Reporting for a Non-Registered Asynchronous Reset Signal

```
Info: Minimum slack time is 1.131 ns for clock "a_clk15" between source pin "a_arst2" and
destination register "inst5"
          Info: Requirement is of type removal
          Info: + Data arrival time is 4.787 ns
    Info: + Launch edge is 0.000 ns
    Info: + Min Input delay of pin is 1.500 ns
    Info: + Min pin to register delay is 3.287 ns
          Info: - Data required time is 3.656 ns
    Info: + Latch edge is 0.000 ns
    Info: + Longest clock path from clock "a_clk15" to destination register
    is 3.542 ns
        Info: + Micro hold delay of destination is 0.114 ns
```

If the asynchronous reset signal is from a device pin, an **Input Minimum Delay** assignment must be made to the asynchronous reset pin for the Classic Timing Analyzer to perform a removal analysis on this path.

Skew Management

Clock skew is the difference in the arrival times of a clock signal at two different registers, which can be caused by path length differences between two clock paths, or by using gated or rippled clocks. As clock periods become shorter and shorter, the skew between data arrival times and clock arrival times becomes more significant. The Classic Timing Analyzer provides two assignments for analyzing and constraining skew for data and clock signals.

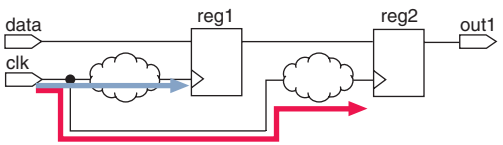
Maximum Clock Arrival Skew

Make **Maximum Clock Arrival Skew** assignments to specify the maximum allowable clock arrival skew between a clock signal and various destination registers. The Classic Timing Analyzer compares the longest clock path to the registers' clock port and the shortest clock path to the registers' clock port to determine if your maximum clock arrival skew is achieved. Maximum clock arrival skew is calculated using Equation 33.

(33) Maximum Clock Arrival Skew = Longest Clock Path – Shortest Clock Path

For example, if the delay from clock pin `clk` to the clock port of register `reg1` is 1.0 ns, and the delay from clock pin `clk` to the clock port of register `reg2` is 3.0 ns, as shown in Figure 8–19, the Classic Timing Analyzer provides a clock skew slack time of 2.0 ns.

Figure 8–19. Clock Arrival Paths



You should apply the **Maximum Clock Arrival Skew** assignment to a clock node and a group of registers. When you make a **Maximum Clock Arrival Skew** assignment, the Fitter attempts to satisfy the skew requirement.

You can use the `set_instance_assignment -name max_clock_arrival_skew` Tcl command to specify a **Maximum Clock Arrival Skew** assignment. The following example specifies a maximum clock arrival skew of 1 ns from clock signal `clk` to the bank of registers matching `reg*`:

```
set_instance_assignment -name max_clock_arrival_skew 1ns -from clk -to reg*
```

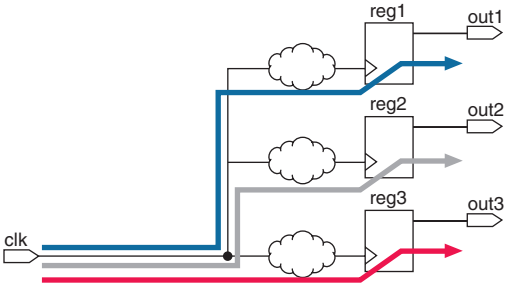
Maximum Data Arrival Skew

Make **Maximum Data Arrival Skew** assignments to specify the maximum allowable data arrival skew to various destination registers or pins. The Classic Timing Analyzer compares the longest data arrival path to the shortest data arrival path to determine if your specified maximum data arrival skew is achieved. Maximum data arrival skew is calculated using Equation 34.

(34) Maximum Data Arrival Skew = Longest Data Arrival Path – Shortest Data Arrival Path

For example, if the data arrival time to output pin `out1` is 2.0 ns, the data arrival time to output pin `out2` is 1.5 ns, and the data arrival time to output pin `out3` is 1.0 ns, as shown in Figure 8–20, the Classic Timing Analyzer provides a maximum data arrival skew slack time of 1.0 ns.

Figure 8–20. Data Arrival Paths



When you make a **Maximum Data Arrival Skew** assignment, the Fitter attempts to satisfy the skew requirement.

You can use the set_instance_assignment -name max_data_arrival_skew Tcl command to specify a maximum data arrival skew value. The following example specifies a maximum data arrival skew of 1 ns from clock signal clk to the bank of output pins dout:

```
set_instance_assignment -name max_data_arrival_skew 1ns -from clk -to dout[*]
```

Generating Timing Analysis Reports with report_timing

The Classic Timing Analyzer includes the report_timing Tcl command for generating text-based timing analysis reports. You can customize the output of report_timing using multiple switches that allow the generation of both detailed and general timing reports on any path in the design.

The report_timing Tcl command is available in the quartus_tan executable.

Prior to using the report_timing Tcl command, you must open a Quartus II project and create a timing netlist. For example, the following two Tcl commands accomplish this:

```
project_open my_project
create_timing_netlist
```

The report_timing Tcl command provides -from and -to switches for filtering specific source and destination nodes. For example, the following report_timing Tcl command reports all clock setup paths, with the switch –clock_setup, between registers src_reg* and dst_reg*. The –npaths 20 switch limits the report to 20 paths.

```
report_timing –clock_setup –from src_reg* -to dst_reg* -npaths 20
```

The switches -clock_filter and -src_clock_filter are also available for filtering based on specific clock sources. For example, the following report_timing Tcl command reports all clock setup paths where the destination registers are clocked by clk:

```
report_timing -clock_setup -clock_filter clk
```

The following example reports clock setup paths where the destination registers are clocked by clk, and the source registers are clocked by src_clock.

```
report_timing -clock_setup -clock_filter clk -src_clock_filter src_clk
```

The following provides an example script that can be sourced by the quartus_tan executable:

```
# Open a project
project_open my_project
# Always create the netlist first
create_timing_netlist
# List clock setup paths for clock clk
# from registers abc* to registers xyz*
report_timing -clock_setup -clock_filter clk -from abc* -to xyz*
# List the top 5 pin-to-pin combinational paths
report_timing -tpd -npaths 5
# List the top 5 pin-to-pin combinational paths and
# write output to an out.tao file
report_timing -tpd -npaths 5 -file out.tao
# Compute min tpd and append results to existing out.tao
report_timing -min_tpd -npaths 5 -file out.tao -append
# Show longest path (register to register data path) between a* and b*
report_timing -longest_paths -npaths 1
delete_timing_netlist
project close
```

Other Timing Analyzer Features

The Classic Timing Analyzer provides many features for customizing and increasing the efficiency of static timing analysis, including:

- Wildcard assignments
- Assignment groups
- Fast corner analysis
- Early timing estimation
- Timing constraint checker
- Latch analysis

Wildcard Assignments

To simplify the tasks of making assignments to many node assignments, the Quartus II software accepts the * and ? wildcard characters. Use these wildcard characters to reduce the number of individual assignments you need to make for your design.

The "*" wildcard character matches any string. For example, given an assignment made to a node specified as reg*, the Classic Timing Analyzer searches and applies the assignment to all design nodes that match the prefix reg with none, one, or several characters following, such as reg1, reg[2], regbank, and reg12bank.

The "?" wildcard character matches any single character. For example, given an assignment made to a node specified as reg?, the Classic Timing Analyzer searches and applies the assignment to all design nodes that match the prefix reg and any single character following, such as reg1, rega, and reg4.

Assignment Groups

Assignment groups, also known as time groups, allow you to define a custom group of nodes to which you can assign timing assignments. You can also exclude specific nodes, wildcards, and time groups from a time group.

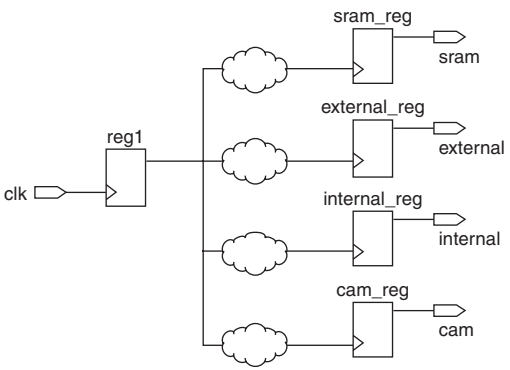
Use the `timegroup` Tcl command to create an assignment group. The following example creates an assignment group `srcgrp` and adds nodes with names that match `src1*` to the group:

```
timegroup srcgrp -add_member src1*
```

For example, Figure 8–21 has false paths between source register `reg1` and destination register bank `sram_reg`, `external_reg`, `internal_reg`, and `cam_reg` that need to be cut. Without the use of assignment groups, the assignments required are:

```
set_timing_cut_assignment -from reg1 to sram_reg
set_timing_cut_assignment -from reg1 to external_reg
set_timing_cut_assignment -from reg1 to internal_reg
set_timing_cut_assignment -from reg1 to cam_reg
```

Figure 8–21. False Path



With an assignment group called `dst_reg_bank`, the assignments required are:

```
#create a time group called dst_reg
timegroup dst_reg_bank -add_member sram_reg
timegroup dst_reg_bank -add_member external_reg
timegroup dst_reg_bank -add_member internal_reg
timegroup dst_reg_bank -add_member cam_reg
#cut timing paths
set_timing_cut_assignment -from reg1 to dst_reg_bank
```

Once an assignment group has been defined, applicable timing assignment can be made to the time group without redefining the assignment group.

Assigning individual nodes to time groups and applying timing assignments to these time groups can improve the performance of the Classic Timing Analyzer.

Fast Corner Analysis

Fast Corner Analysis uses timing models generated under best case conditions (voltage, process, and temperature) for the fastest speed-grade device.

Both Fast Corner and Slow Corner static timing analysis reports are saved to the <*project name*>**.tan.rpt** file, potentially overwriting previous timing analysis reports. To preserve a copy of your reports, save the file with a new name before the next compilation or static timing analysis, or use the Combined Fast/Slow Analysis report feature.

The Quartus II software also reports minimum delay checks after a slow corner (default) analysis. These results are generated by reporting minimum delay checks using the worst-case timing models.

To perform fast corner static timing analysis with the best-case timing models, you can use the `switch --fast_model=on` with the `quartus_tan` executable. The following Tcl command enables the fast timing models:

```
quartus_tan <project_name> --fast_model=on
```

Early Timing Estimation

The majority of Quartus II software compilation time is consumed by the place-and-route process used to obtain optimal design results. To accelerate the design process for large designs, the Quartus II software provides early timing estimation. This feature provides a quick static timing analysis in a fraction of the time required for a full compilation by performing a preliminary place-and-route on the design without full optimizations, which reduces total compile time by up to five times compared to a fully fitted design.

An **Early Timing Estimate** fit is not fully optimized or legally routed. The timing delay report is only an estimate. Typically, the estimated delays are within 10% of those obtained with a full fit when the realistic setting is used.

The **Early Timing Estimate** has three settings for generating timing estimates: Realistic, Optimistic, and Pessimistic. Table 8–1 describes these settings.

Table 8–1. Early Timing Estimate Setting Options

Setting	Description
Realistic (default setting: estimates final timing using standard fitting)	Generates timing estimates that are likely to be closest to full compilation results.
Optimistic (estimates best case final timing)	Generates timing estimates that are unlikely to be exceeded by full compilation.
Pessimistic (estimates worst case final timing)	Generates timing estimates that are likely to be exceeded by full compilation.

To use the Early Timing Estimate feature, enter the following Tcl command when performing a fit:

```
quartus_fit --early_timing_estimate[=<realistic|optimistic|pessimistic>]
```

After the Early Timing Estimate is complete, a full timing report is generated based on the early placement and routing delays. In addition, you can view the preliminary logic placement in the Timing Closure floorplan. The early timing placement allows you to perform initial placement and view the timing interaction of various placement topology.

Timing Constraint Checker

Altera recommends that you enter all timing constraints into the Quartus II software prior to performing a full compilation. This ensures that the Fitter targets the correct timing requirements and ensures that the Classic Timing Analyzer reports the correct violations for all timing paths in the design. To ensure that all constraints have been applied to design nodes, the Timing Constraint Check feature reports all unconstraint paths in your design. Example 8–8 shows the timing constraint check summary generated after a full compilation.

Example 8–8. Timing Constraint Check Summary

```
+-------------------------------------------------------------------------------------------+
; Timing Constraint Check Summary                                                          ;
+---------------------------------------+---------------------------------------------------+
; Timing Constraint Check Status        ; Analyzed - Tue Feb 28 11:42:31 2006              ;
; Quartus II Version                    ; 6.0 Internal Build 143 02/20/2006 SJ Full Version ;
; Revision Name                         ; test                                             ;
; Top-level Entity Name                 ; Block1                                           ;
; Unconstrained Clocks                  ; 0                                                ;
; Unconstrained Paths (Setup)           ; 22                                               ;
; Unconstrained Reg-to-Reg Paths (Setup) ; 0                                               ;
; Unconstrained I/O Paths (Setup)       ; 22                                               ;
; Unconstrained Paths (Hold)            ; 12                                               ;
; Unconstrained Reg-to-Reg Paths (Hold) ; 0                                                ;
; Unconstrained I/O Paths (Hold)        ; 12                                               ;
+---------------------------------------+---------------------------------------------------+
```

To perform a timing constraint check, use the `switch --check_constraints` with the `quartus_tan` executable. The following Tcl command performs a timing constraint check on both setup and hold on the design system:

```
quartus_tan block1 --check_constraints=both
```

Latch Analysis

Latches are implemented in the Quartus II software as look-up-tables (LUT) feeding back onto themselves. The Classic Timing Analyzer can analyze these latches as synchronous elements rather than as combinational elements. The clock enables are analyzed as inverted clocks. The Classic Timing Analyzer reports the results of setup and hold analysis on these latches.

You can turn on the **Analyze Latches As Synchronous Elements** option with the following Tcl command:

```
set_global_assignment -name ANALYZE_LATCHES_AS_SYNCHRONOUS_ELEMENTS ON
```

Timing Analysis Using the Quartus II GUI

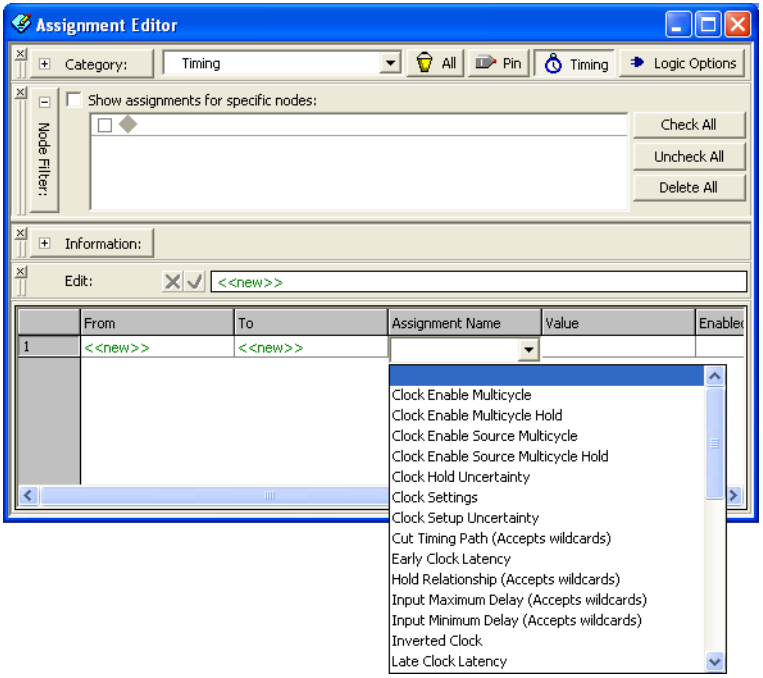
In addition to the extensive scripting support available in the Classic Timing Analyzer, the Quartus II software provides the Assignment Editor and other user interface tools, giving you access to the Classic Timing Analyzer features and assignments.

Assignment Editor

The Assignment Editor is a spreadsheet-style interface used for adding, modifying, and deleting timing assignments.

To make timing assignments in the Assignment Editor, choose **Timing** from the category list to cause the Assignment Name column to display only timing assignments. Double-click **<<new>>** in the **Assignment Name** field, the **Assignment Name** list displays. Figure 8–22 shows the Assignment Editor with the Assignment Name list displaying timing assignment types.

Figure 8–22. Assignment Editor

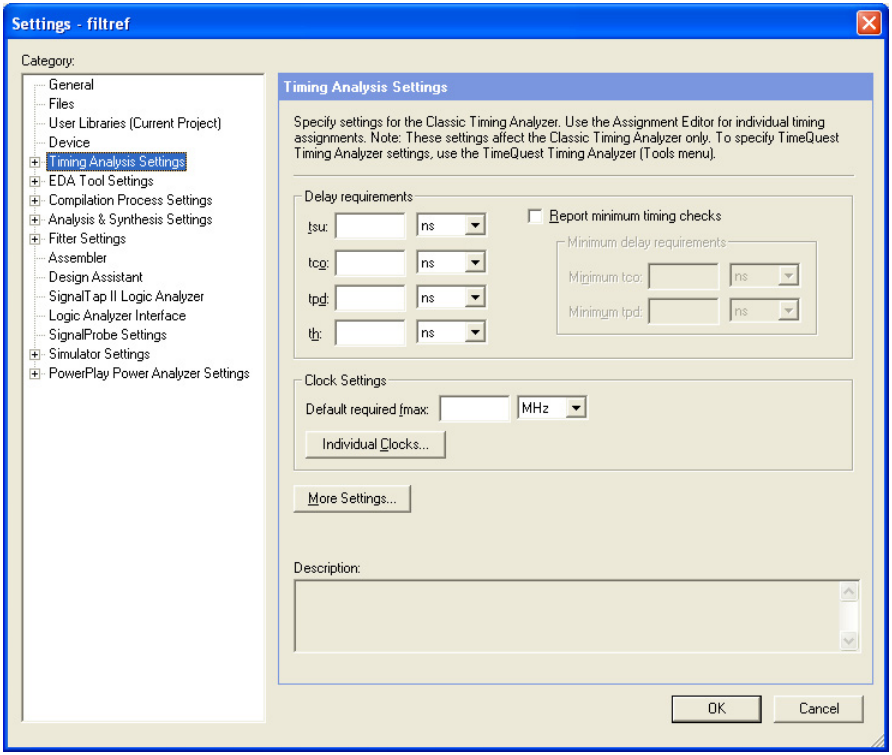


For more information on the Assignment Editor, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Timing Settings

You can specify delay requirements and clock settings with the **Timing Analysis Settings** page of the **Settings** dialog box. To access this page, on the Assignments menu, click **Timing Analysis Settings**. The Timing **Analysis Settings** page displays (Figure 8–23).

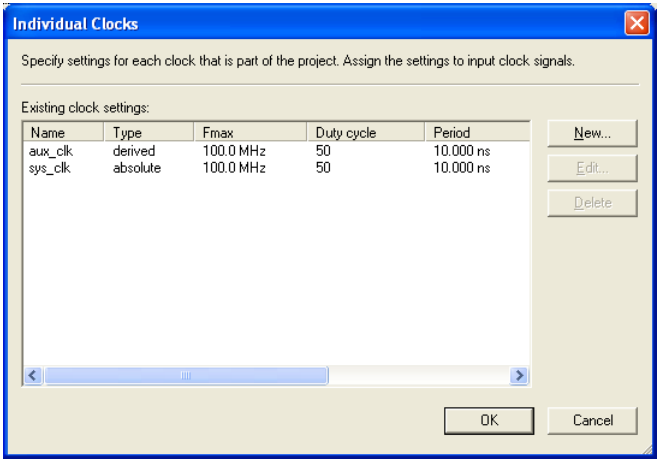
Figure 8–23. Timing Analysis Settings Dialog Box



Clock Settings Dialog Box

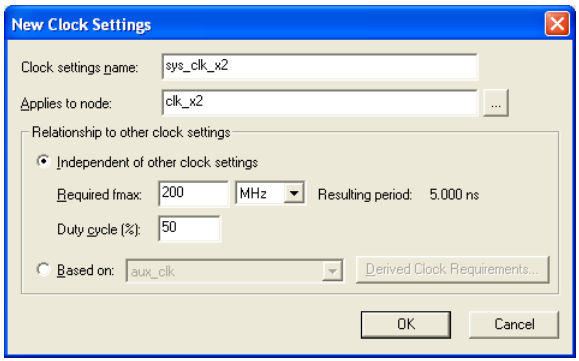
You can create or modify base clock settings or derived clock settings using the **Clock Settings** dialog box. On the Assignments menu, click **Timing Analysis Settings**. The **Timing Analysis Settings** page displays. Under **Clock Settings**, click **Individual Clocks**. The **Individual Clock** dialog box is shown (Figure 8–24).

Figure 8–24. Individual Clocks Dialog Box



Click the **New** button in the **Individual Clocks** dialog box to access the **New Clock Settings** dialog box and create a base or derived clock setting (Figure 8–25).

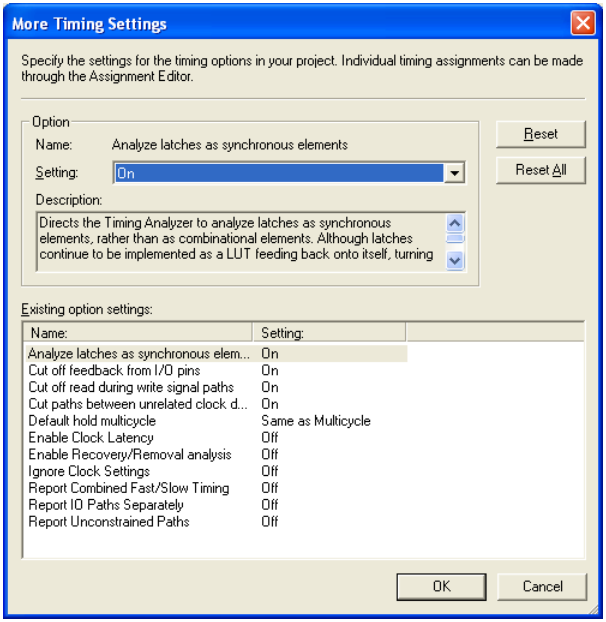
Figure 8–25. New Settings Dialog Box



More Timing Settings Dialog Box

On the **Timing Analysis Settings** page of the **Settings** dialog box, click **More Settings** to display the **More Timing Settings** dialog box (Figure 8–26). The **More Timing Settings** dialog box provides access to many global timing analysis options.

Figure 8–26. More Timing Settings Dialog Box



Timing Reports

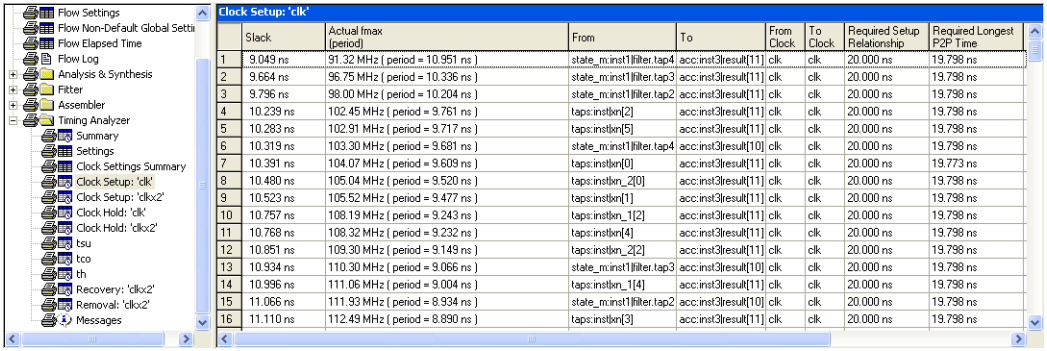
The Classic Timing Analyzer report is a section of the Compilation Report containing the static timing analysis results. The Classic Timing Analyzer report includes clock setup and clock hold measurements for all clock sources. The report also shows t_{CO} for all output pins, t_{SU} and t_H for all input pins, and t_{PD} for any pin-to-pin combinational paths in the design. Other reports are created for different analyses and device features.

If there are no timing assignments for the design, the Classic Timing Analyzer does not generate slack reports for any detected clock nodes. The Classic Timing Analyzer only reports slack measurements for pins with individual or global t_{SU}, t_H, or t_{CO} assignments. A positive slack indicates the margin by which the path surpasses the clock timing requirements. A negative slack indicates the margin by which the path fails the clock timing requirements.

This timing analysis report is also available in text format located in the design directory with the file name *<revision name>*.**tan.rpt**.

In the Compilation Report, select an analysis type under the Timing Analyzer folder to display the analysis report, for example, Clock Setup or Clock Hold. Figure 8–27 shows an example of a clock setup report for clock signal `clk`.

Figure 8–27. Timing Analysis Report



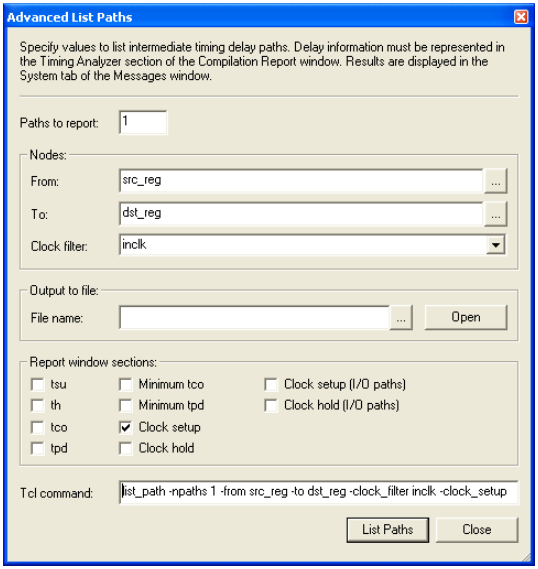
	Slack	Actual fmax (period)	From	To	From Clock	To Clock	Required Setup Relationship	Required Longest P2P Time
1	9.049 ns	91.32 MHz (period = 10.951 ns)	state_m:inst1|filter.tap4	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
2	9.664 ns	96.75 MHz (period = 10.336 ns)	state_m:inst1|filter.tap3	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
3	9.796 ns	98.00 MHz (period = 10.204 ns)	state_m:inst1|filter.tap2	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
4	10.239 ns	102.45 MHz (period = 9.761 ns)	taps:inst|xn[2]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
5	10.283 ns	102.91 MHz (period = 9.717 ns)	taps:inst|xn[5]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
6	10.319 ns	103.30 MHz (period = 9.681 ns)	state_m:inst1|filter.tap4	acc:inst3|result[10]	clk	clk	20.000 ns	19.798 ns
7	10.391 ns	104.07 MHz (period = 9.609 ns)	taps:inst|xn[0]	acc:inst3|result[11]	clk	clk	20.000 ns	19.773 ns
8	10.480 ns	105.04 MHz (period = 9.520 ns)	taps:inst|xn_2[0]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
9	10.523 ns	105.52 MHz (period = 9.477 ns)	taps:inst|xn[1]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
10	10.757 ns	108.19 MHz (period = 9.243 ns)	taps:inst|xn_1[2]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
11	10.768 ns	108.32 MHz (period = 9.232 ns)	taps:inst|xn[4]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
12	10.851 ns	109.30 MHz (period = 9.149 ns)	taps:inst|xn_2[2]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
13	10.934 ns	110.30 MHz (period = 9.066 ns)	state_m:inst1|filter.tap3	acc:inst3|result[10]	clk	clk	20.000 ns	19.798 ns
14	10.996 ns	111.06 MHz (period = 9.004 ns)	taps:inst|xn_1[4]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns
15	11.066 ns	111.93 MHz (period = 8.934 ns)	state_m:inst1|filter.tap2	acc:inst3|result[10]	clk	clk	20.000 ns	19.798 ns
16	11.110 ns	112.49 MHz (period = 8.890 ns)	taps:inst|xn[3]	acc:inst3|result[11]	clk	clk	20.000 ns	19.798 ns

Advanced List Path

The **Advanced List Paths** dialog box provides detailed information on a specific path, such as interconnect and cell delays between any two valid register-to-register paths (Figure 8–28).

The **Advanced List Paths** dialog box allows you to select the type of paths you want listed. For example, you can obtain detailed information for Clock Setup and Clock Hold for a specific clock. In addition, the Tcl command field in the window matches the equivalent Tcl command you can use in either a custom Tcl script or in the Tcl console.

Figure 8–28. Advanced List Paths Dialog Box

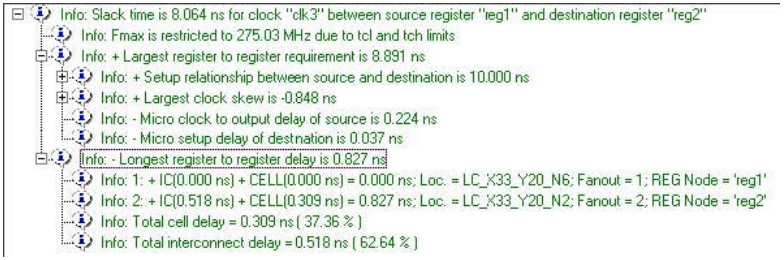


You can perform a list path command directly from the Timing Analysis report. To do this, right click a path and click **List Path** (Figure 8–29).

The **Advanced List Paths** dialog box display only paths that are visible in the Timing Analysis report. To increase the amount of paths reported by the Classic Timing Analyzer, on the Assignments menu, click **Timing Analysis Settings**. In the **Category** list, expand **Timing Analysis Settings**, and select **Timing Analyzer Reporting**. In the **Timing Analyzer Reporting** page, specify the range of information to be reported by the Classic Timing Analyzer.

Both the **Advanced List Paths** and the **List Path** command display the path information in the System message window.

Figure 8–29. List Path in the Message Window



If the **Combined Fast/Slow Timing** option is enabled, the List Path Tcl command displays only path delays reported in the Slow Model section.

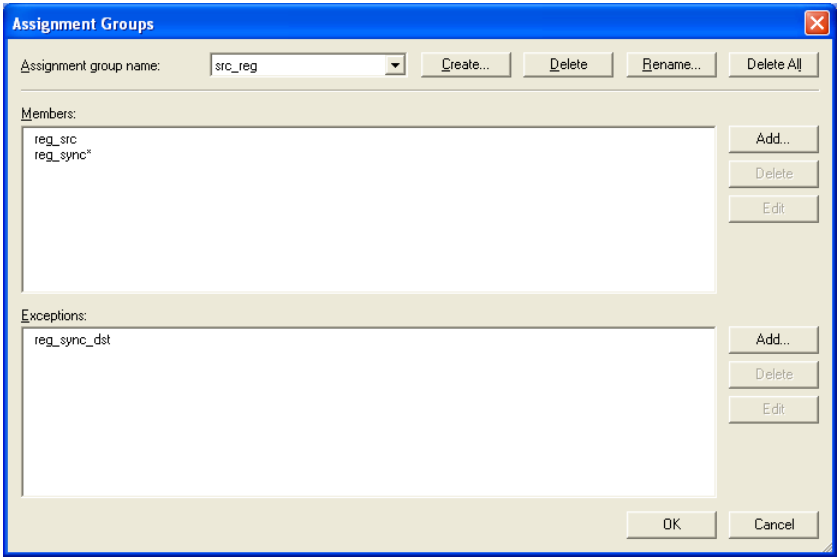
Early Timing Estimate

To start an Early Timing Estimate, on the Processing menu, point to Start and click **Start Early Timing Estimate**. To specify the **Early Timing Estimate** mode, on the Assignments menu, click **Settings**. In the **Category** list, select **Compilation Processes Settings**, select **Early Timing Estimate**, and click the desired timing estimate mode. For more information on the Early Timing Estimate feature, refer to "Early Timing Estimation" on page 8–37.

Assignment Groups

To define, modify, and delete assignment groups, also known as time groups, from a single dialog box, on the Assignments menu, click **Assignment (Time) Groups**. The **Assignment Groups** dialog box displays (Figure 8–30).

Figure 8–30. Assignment Groups Dialog Box



Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp
```

Refer to the *Scripting Reference Manual* to view this information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Creating Clocks

There are two Tcl commands that allow you to define clocks in a design, `create_base clock` and `create_relative_clock`.

Base Clocks

Use the `create_base_clock` Tcl command to define a base clock:

```
create_base_clock [-h | -help] [-long_help] -fmax <fmax> [-duty_cycle <integer>]
[-virtual] [-target <name>] [-no_target] [-entity <entity>] [-disable]
[-comment <comment>] <clock_name>
```

To define a base clock setting named `sys_clk` with a 100 MHz requirement applied to node `clk_src`, enter the following Tcl command:

```
create_base_clock –fmax 100MHz –target clk_src sys_clk
```

Derived Clocks

Use the `create_relative_clock` Tcl command to define a relative clock:

```
create_relative_clock [-h | -help] [-long_help] -base_clock <Base clock>
[-duty_cycle <integer>] [-multiply <integer>] [-divide <integer>] [-offset <offset>]
[-phase_shift <integer>] [-invert] [-virtual] [-target <name>] [-no_target]
[-entity <entity>] [-disable] [-comment <comment>] <clock_name>
```

To define a relative clock named `aux_clk` based upon base clock setting `sys_clk` with a multiplication factor of two applied to node `rel_clk`, enter the following Tcl command:

```
create_relative_clock –base_clock sys_clk –multiply 2 –target rel_clk aux_clk
```

Clock Latency

You can use the `set_clock_latency` Tcl command to create either an early or late clock latency assignment:

```
set_clock_latency [-h | -help] [-long_help] [-early] [-late] -to <to> [<value>]
```

To apply an early clock latency of 1 ns and a late clock latency of 2 ns to clock node `clk`, enter the following Tcl commands:

```
set_clock_latency -early -to clk 2ns
```

Clock Uncertainty

You can use the `set_clock_uncertainty` Tcl command to create clock uncertainty assignments as shown in the following example:

```
set_clock_uncertainty [-h] [-help] [-long_help [-from <source clock name> ] -to
<destination clock name> [-setup] [-hold] [-remove] [-disable] [-comment <comment>] <value>
```

To apply a clock setup uncertainty of 50 ps between source clock node `clk_src` and destination clock node `clk_dst`, enter the following Tcl command:

```
set_clock_uncertainty -from clk_src -to clk_dst -setup 50ps
```

To apply a clock hold uncertainty of 25 ps between to clock node `clk_sys`, enter the following Tcl command:

```
set_clock_uncertainty -to clk_sys -setup 25ps
```

Cut Timing Paths

You can use the `set_timing_cut_assignment` Tcl command to create cut timing assignments:

```
set_timing_cut_assignment [-h | -help] [-long_help] [-from <from_node_list>]
[-to <to_node_list>] [-remove] [-disable] [-comment <comment>]
```

To cut the timing path between from source register `reg1` to destination register `reg2`, enter the following Tcl command:

```
set_timing_cut_assignment -from reg1 -to reg2
```

Input Delay Assignment

You can use the Tcl command `set_input_delay` to create input delay assignments:

```
set_input_delay [-h | -help] [-long_help] [-clk_ref <clock>] -to <input_pin> [-min] [-max]
[-clock_fall] [-remove] [-disable] [-comment <comment>] [<value>]
```

To apply an input maximum delay of 2 ns to an input pin named `data_in` that feeds a register clocked by clock source `clk`, enter the following Tcl command:

```
set_input_delay -clk_ref clk -to data_in –max 2ns
```

Maximum & Minimum Delay

The following Tcl commands create the **Maximum Delay** and **Minimum Relationship** assignments, respectively:

```
set_instance_assignment -name MAX_delay <value> -from <node> -to <node>
set_instance_assignment -name MIN_delay <value> -from <node> -to <node>
```

To apply a **Maximum Delay** of 8 ns and a minimum of 5 ns between source register `reg1` and destination register `reg2`, enter the following Tcl command:

```
set_instance_assignment -name MAX_DELAY 8ns -from reg1 -to reg2
set_instance_assignment -name MIN_DELAY 5ns -from reg1 -to reg2
```

To apply a **Maximum Delay** of 10 ns for all paths from source clock `clk_src` to destination clock `clk_dst`, enter the following Tcl command:

```
set_instance_assignment -name MAX_DELAY 10ns -from clk_src -to clk_dst
```

Maximum Clock Arrival Skew

The following Tcl command defines the **Maximum Clock Arrival Skew** assignment:

```
set_instance_assignment -name max_clock_arrival_skew <value> -from <clock> -to <node>
```

To apply a **Maximum Clock Arrival Skew** of 1 ns for clock source `clk` to a predefined timegroup called `reg_group`, enter the following Tcl command:

```
set_instance_assignment -name max_clock_arrival_skew 1ns -from clk -to reg_group
```

Maximum Data Arrival Skew

Use the Tcl command `set_instance_assignment -name max_data_arrival` to create **Maximum Data Arrival Skew** assignments:

```
set_instance_assignment -name max_data_arrival_skew <value> -from <clock> -to <node>
```

To apply a **Maximum Data Arrival Skew** of 1 ns for clock source `clk` to a predefined timegroup of pins called `pin_group`, enter the following Tcl command:

```
set_instance_assignment -name max_data_arrival_skew 1ns -from clk -to pin_group
```

Multicycle

Use the `set_multicycle_assignment` Tcl command to create **Multicycle** assignments:

```
set_multicycle_assignment [-h | -help] [-long_help] [-setup] [-hold] [-start] [-end]
[-from <from_list>] [-to <to_list>] [-remove] [-disable] [-comment <comment>]
<path_multiplier>
```

To apply a **Multicycle Setup** of two and a **Hold Multicycle** of one between source register `reg1` and destination register `reg2`, enter the following Tcl commands:

```
set_multicycle_assignment –setup -end –from reg1 –to reg2 2
set_multicycle_assignment –hold -end –from reg1 –to reg2 1
```

To apply a **Source Multicycle Setup** of two between source register `reg1` and destination register `reg2`, enter the following Tcl command:

```
set_multicycle_assignment –setup -start –from reg1 –to reg2 1
```

To apply a **multicycle setup** of two for all paths from source clock `clk_src` to destination clock `clk_dst`, enter the following Tcl command:

```
set_multicycle_assignment –setup –end –from clk_src –to clk_dst 2
```

Output Delay Assignment

Use the Tcl command `set_output_delay` to create **Output Delay** assignments:

```
set_output_delay [-h | -help] [-long_help] [-clk_ref <clock>] -to <output_pin> [-min]
[-max] [-clock_fall] [-remove] [-disable] [-comment <comment>] [<value>]
```

To apply an **Output Maximum Delay** of 3 ns to an output pin named `data_out` that is fed a register clocked by clock source `clk`, enter the following Tcl command:

```
set_output_delay -clk_ref clk -to data_out –max 3ns
```

Report Timing

Use the report_timing Tcl command to generate timing reports:

```
report_timing [-h | -help] [-long_help] [-npaths <number>] [-tsu] [-th] [-tco] [-tpd]
[-min_tco] [-min_tpd] [-clock_setup] [-clock_hold] [-clock_setup_io] [-clock_hold_io]
[-clock_setup_core] [-clock_hold_core] [-recovery] [-removal] [-dqs_read_capture]
[-stdout] [-file <name>] [-append] [-table <name>] [-from <names>] [-to <names>]
[-clock_filter <names>] [-src_clock_filter <names>] [-longest_paths] [-shortest_paths]
[-all_failures]
```

The following example generates a list of all clock setup paths for clock source clk from registers src_reg* to registers dst_reg*:

```
report_timing -clock_setup -clock_filter clk -from src_reg* -to dst_reg*
```

Setup & Hold Relationships

The following Tcl commands create **Setup Relationship** and **Hold Relationship** assignments, respectively:

```
set_instance_assignment -name SETUP_RELATIONSHIP <value> -from <node> -to <node>
set_instance_assignment -name HOLD_RELATIONSHIP <value> -from <node> -to <node>
```

To apply a **Setup Relationship** of 12 ns and a **Hold Relationship** of 2 ns between source register reg1 and destination registers reg2, enter the following Tcl command:

```
set_instance_assignment -name SETUP_RELATIONSHIP 12ns -from reg1 -to reg2
set_instance_assignment -name HOLD_RELATIONSHIP 2ns -from reg1 -to reg2
```

To apply a setup relationship of 10 ns for all paths from source clock clk_src to destination clock clk_dst, enter the following Tcl command:

```
set_instance_assignment -name SETUP_RELATIONSHIP 10ns -from clk_src -to clk_dst
```

Assignment Group

Use the timegroup Tcl command to create assignment groups:

```
timegroup [-h | -help] [-long_help] [-add_member <name>] [-add_exception <name>]
[-remove_member <name>] [-remove_exception <name>] [-get_members] [-get_exceptions]
[-overwrite] [-remove] [-disable] [-comment <comment>] <group_name>
```

The following example creates an assignment group called reg_bank with members dst_reg*, and excludes register dst_reg5.

```
timegroup reg_bank -add_member dst_reg* -add_exception dst_reg5
```

Virtual Clock

Use the `create_relative_clock` with the `-virtual` switch to create **Virtual Clock** assignments:

```
create_relative_clock [-h | -help] [-long_help] -base_clock <Base clock>
[-duty_cycle <integer>] [-multiply <integer>] [-divide <integer>] [-offset <offset>]
[-phase_shift <integer>] [-invert] [-virtual] [-target <name>] [-no_target]
[-entity <entity>] [-disable] [-comment <comment>] <clock_name>
```

To define a virtual clock derived from the base clock setting `clk_aux` named `brd_sys`, enter the following Tcl command:

```
create_relative_clock -base_clock clk_aux -virtual brd_sys
```

MAX+PLUS II Timing Analysis Methodology

This section describes the basic static timing analysis and assignments available in the Quartus II software that originated in the MAX+PLUS II design software.

f_{MAX} Relationships

Maximum clock frequency is the fastest speed at which the design clock can run without violating internal setup and hold time requirements. The Quartus II software performs static timing analysis on both single and multiple clock designs.

Apply clock settings to all clock nodes in a design to ensure performance requirements are met. Refer to "Clock Settings" on page 8–7 for more information.

Slack

Slack is the margin by which a timing requirement such as f_{MAX} is met or not met. Positive slack indicates the margin by which a requirement is met. Negative slack indicates the margin by which a requirement is not met. The Quartus II software determines slack using Equations 35 through 38.

(35) Clock Setup Slack = Longest Register-to-Register Requirement – Longest Register-to-Register Delay

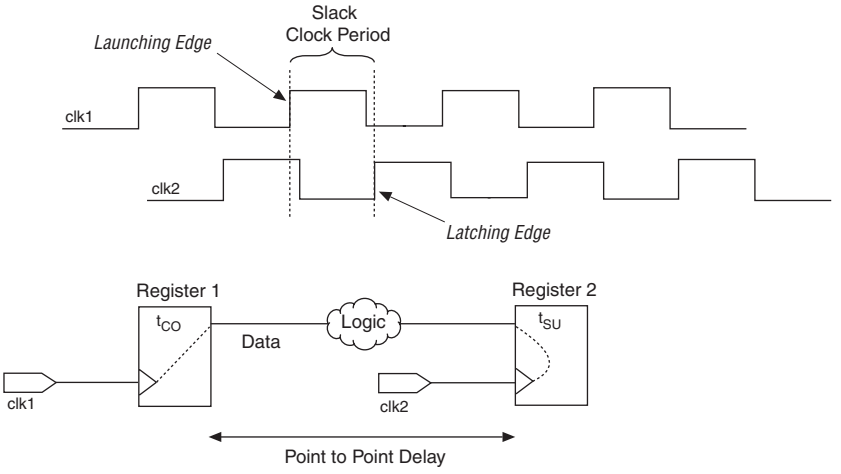
(36) Register-to-Register Requirement = Setup Relationship + Largest Clock Skew – micro t_{CO} of Source Register – micro t_{SU} of Destination Register

(37) Clock Hold Slack = Shortest Register-to-Register Delay – Smallest Register-to-Register Requirement

(38) Shortest Register-to-Register Requirement = Hold Relationship + Smallest Clock Skew – micro t_{CO} of Source Register – micro t_H of Destination Register

Figure 8–31 shows a slack calculation diagram.

Figure 8–31. Slack Calculation Diagram



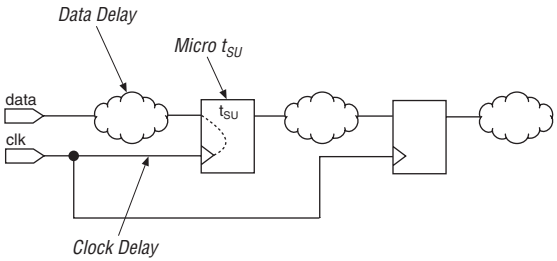
I/O Timing

This section describes the basic measurements made for I/O timing in the Quartus II software.

t_{SU}

t_{SU} specifies the length of time data needs to arrive and be stable at an external input pin prior to a clock transition on an associated clock I/O pin. A t_{SU} requirement describes this relationship for an input register relative to the I/O pins of the FPGA. Figure 8–32 shows a diagram of clock setup time.

Figure 8–32. Clock Setup Time (t_{SU})



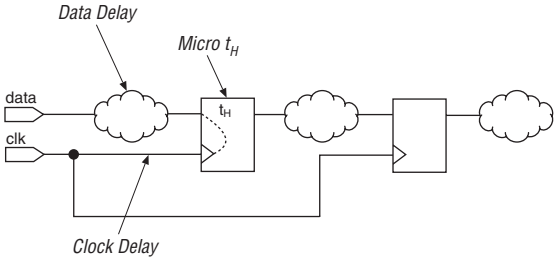
Micro t_{SU} is the internal setup time of the register. It is a characteristic of the register and is unaffected by the signals feeding the register. Equation 39 calculates the t_{SU} of data with respect to `clk` for the circuit shown in Figure 8–32.

(39) t_{SU} = Longest Data Delay – Shortest Clock Delay + micro t_{SU} of Input Register

t_H

t_H specifies the length of time data needs to be held stable on an external input pin after a clock transition on an associated clock I/O pin. A t_H requirement describes this relationship for an input register relative to the I/O pins of the FPGA. Figure 8–33 shows a diagram of clock hold time.

Figure 8–33. Clock Hold Time (t_H)



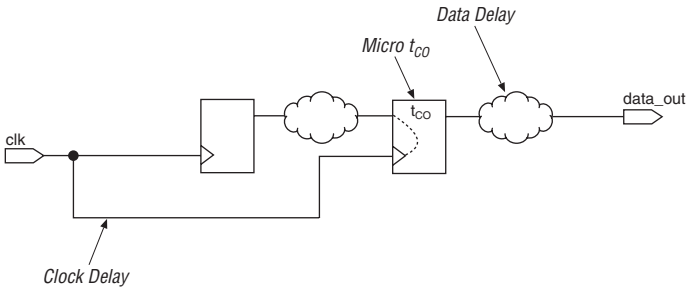
Micro t_H is the internal hold time of the register. Equation 40 calculates the t_H of data with respect to `clk` for the circuit shown in Figure 8–33.

(40) t_H = Longest Clock Delay – Shortest Data Delay + micro t_H of Input Register

t_{CO}

Clock-to-output delay is the maximum time required to obtain a valid output at an output pin fed by a register, after a clock transition on the input pin that clocks the register. Micro t_{CO} is the internal clock-to-output delay of the register. Figure 8–34 shows a diagram of clock-to-output delay.

Figure 8–34. Clock-to-Output Delay (t_{CO})



Equation 41 calculates the t_{CO} for output pin `data_out` with respect to clock node `clk` for the circuit shown in Figure 8–34.

(41) t_{CO} = Longest Clock Delay + Longest Data Delay + micro t_{CO} of Output Register

Minimum t_{CO}

Minimum clock-to-output delay is the minimum time required to obtain a valid output at an output pin fed by a register, after a clock transition on the input pin that clocks the register. Micro t_{CO} is the internal clock-to-output delay of registers in Altera FPGAs. Unlike the t_{CO} assignment, the min t_{CO} assignment looks at the shortest delay paths (Equation 42).

(42) $\text{min } t_{CO} = \text{Shortest Clock Delay} + \text{Shortest Data Delay} + \text{micro } t_{CO} \text{ of Output Register}$

t_{PD}

Pin-to-pin delay (t_{PD}) is the time required for a signal from an input pin to propagate through combinational logic and appear at an external output pin (Equation 43).

(43) $t_{PD} = \text{Longest Pin-to-Pin Delay}$

In the Quartus II software, you can make t_{PD} assignments between an input pin and an output pin.

Minimum t_{PD}

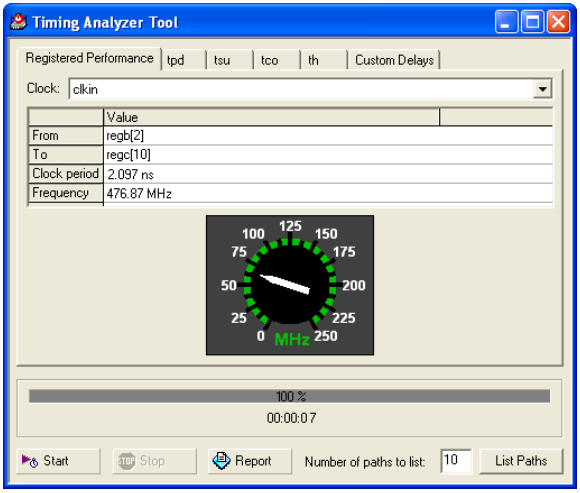
The minimum pin-to-pin delay (t_{PD}) is the time required for a signal from an input pin to propagate through combinational logic and appear at an external output pin. Unlike the t_{PD} assignment, the min t_{PD} assignment applies to the shortest pin-to-pin delay (Equation 44).

(44) $\text{min } t_{PD} = \text{Shortest Pin-to-Pin Delay}$

The Timing Analyzer Tool

To facilitate the classic static timing analysis flow and constraint, the Quartus II software provides a MAX+PLUS II-style Timing Analyzer Tool available on the Tools menu. The Timing Analyzer Tool provides a simple interface, similar to the Timing Analyzer tool in MAX+PLUS II, that reports register-to-register performance, I/O timing, and custom delay values (Figure 8–35).

Figure 8–35. Timing Analyzer Tool



Conclusion

Evolving design and aggressive process technologies require larger and higher-performance FPGA designs. Increasing design complexity demands enhanced static timing analysis tools that aid designers in verifying design timing requirements. Without advanced static timing analysis tools, you risk circuit failure in complex designs. The Classic Timing Analyzer incorporates a set of powerful static timing analysis features critical in enabling system-on-a-programmable-chip (SOPC) designs.

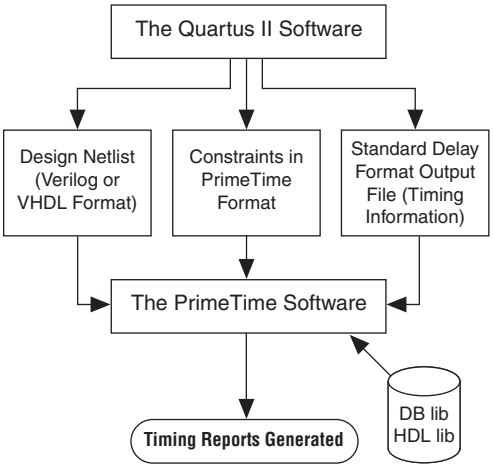
9. Synopsys PrimeTime Support

QII53005-6.0.0

Introduction

The PrimeTime software is a widely used sign-off tool used to perform static timing analysis on ASIC designs. The Quartus® II software makes it easy for designers to analyze their Quartus II projects using the PrimeTime software. The Quartus II software exports a netlist, design constraints (in the PrimeTime format), and libraries to the PrimeTime software environment. Figure 9–1 shows the PrimeTime flow diagram.

Figure 9–1. The PrimeTime Software Flow Diagram



This chapter describes the following:

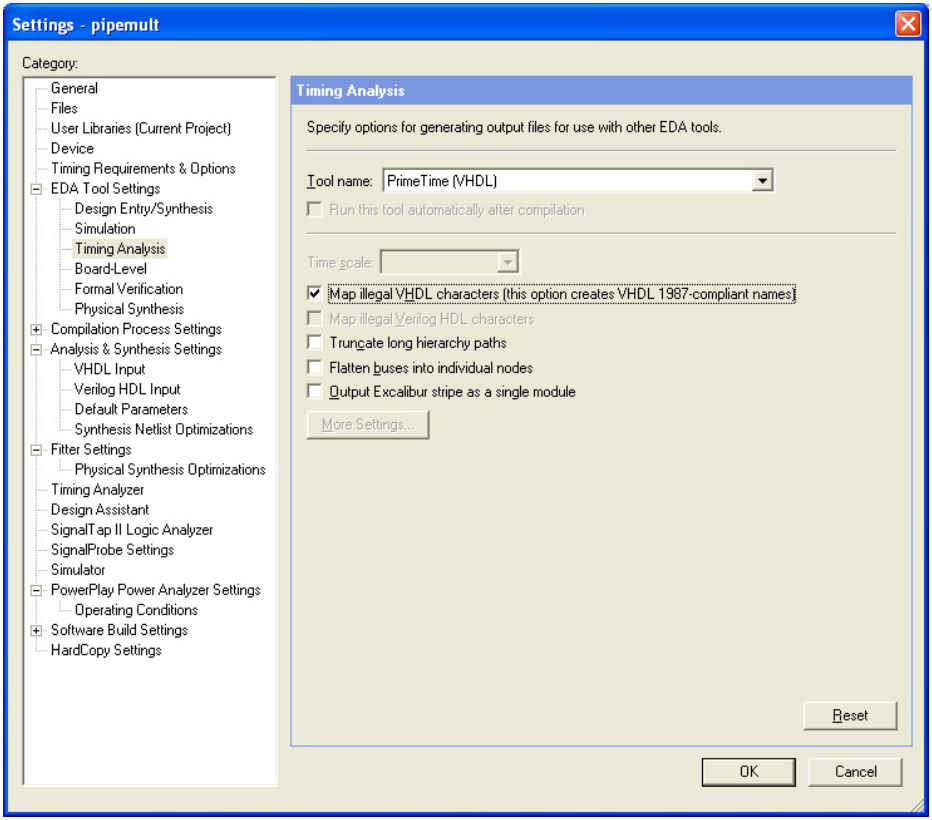
- How to set parameters in the Quartus II software to generate files for use by the PrimeTime software
- How to interpret the contents and the intended use of the files generated by the Quartus II software
- How to run the PrimeTime software
- How to read the output of the PrimeTime software
- Static timing analysis differences between the Quartus II software and the PrimeTime software

Quartus II Settings for Generating the PrimeTime Software Files

To set the Quartus II software to generate files for the PrimeTime software, perform the following steps:

1. In the Quartus II software, on the Assignments menu, click **EDA Tool Settings**.
2. In the **Category** list, select **Timing Analysis** under **EDA Tool Settings**.
3. In the **Tool name** list, select **PrimeTime (Verilog)** or **PrimeTime (VHDL)**, depending on the HDL language chosen for use with the PrimeTime software (Figure 9–2).

Figure 9–2. Setting the Quartus II Software to Generate the PrimeTime Software Files



After making these settings, when you compile your project, the Quartus II software creates three files for the PrimeTime software. These files are saved in the <*revision_name*>**/timing/primetime**, where <*revision_name*> is the location of your Quartus II project.

Files Generated for the PrimeTime Software Environment

The Quartus II software generates a flat netlist, a Standard Delay Output File, and a Tcl script that prepares the PrimeTime software for timing analysis of the Quartus II project. These files are saved in the *<project directory>*/**timing/primetime** directory.

The Netlist

The netlist is written and saved as either *<project name>*.**vo** or *<project name>*.**vho**, depending on whether **PrimeTime (Verilog)** or **PrimeTime (VHDL)** is selected in the **Tool name** list on the **Timing Analysis** page of the **Settings** dialog box. This file contains the flat netlist representing the entire design.

The Standard Delay Output File

The Quartus II software saves the Standard Delay Format Output file as either *<revision_name>*_**v.sdo** or *<revision_name>*_**vhd.sdo**, depending on whether **PrimeTime (Verilog)** or **PrimeTime (VHDL)** is selected in the **Tool name** list on the **Timing Analysis** page of the **Settings** dialog box.

This file contains the timing information for each timing arc (a timing path between any two nodes) in the design. The Quartus II software generates this file using worst-case delay values for the timing arcs. The Quartus II Timing Analyzer uses these worst-case timing models by default, to give conservative results.

To generate the Standard Delay Format Output File using fast corner (best-case) timing analysis, perform the following steps:

1. In the Quartus II software, on the Processing menu, point to Start and click **Start Timing Analyzer (Fast Timing Model)**.

2. After best-case timing analysis is complete, on the Processing menu, point to Start and click **Start EDA Netlist Writer** to create a *<revision_name>*_**v_min.sdo** or *<revision_name>*_**vhd_min.sdo** file, which contains the best-case delay values for each timing arc.

If you are running a fast-corner (best-case) timing analysis, the Quartus II software generates a Tcl script similar to the following: *<revision_name>*_**pt_v_min.tcl**.

The Tcl Script

The Tcl Script generated by the Quartus II software contains information required by PrimeTime to analyze the timing of your post-fit design including PrimeTime setup commands as well as design. This script specifies the `search_path` and the names of the PrimeTime database library files provided with the Quartus II software. The `search_path` and `link_path` are defined at the beginning of the Tcl file. The `link_path` is a space-delimited list containing the names of all database files used by the PrimeTime software.

The Quartus II software saves the script as either *<revision_name>*_**pt_v.tcl** or *<revision_name>*_**pt_vhd.tcl**, depending on whether **PrimeTime (Verilog)** or **PrimeTime (VHDL)** is selected in the **Tool name** list on the **Timing Analysis** page of the **Settings** dialog box. To access the **EDA Settings** dialog box, on the Assignments menu, click **EDA Settings**.

The script also directs the PrimeTime software to refer to the file *<device family>*_**all_pt.v** or *<device family>*_**all_pt.vhd**, which contains the Verilog/VHDL description of library cells for the targeted device family.

Following is an example of the `search_path` and `link_path` defined in the Tcl script:

```
set quartus_root "c:/altera/quartus51/"
set search_path [list . [format "%s%s" $quartus_root "eda/synopsys/primetime/lib"]  ]

set link_path [list *  stratixii_lcell_comb_lib.db  stratixii_lcell_ff_lib.db
stratixii_asynch_io_lib.db  stratixii_io_register_lib.db  stratixii_termination_lib.db
bb2_lib.db  stratixii_ram_internal_lib.db  stratixii_memory_register_lib.db
stratixii_memory_addr_register_lib.db  stratixii_mac_out_internal_lib.db
stratixii_mac_mult_internal_lib.db  stratixii_mac_register_lib.db
stratixii_lvds_receiver_lib.db stratixii_lvds_transmitter_lib.db
stratixii_asmiblock_lib.db stratixii_crcblock_lib.db  stratixii_jtag_lib.db
stratixii_rublock_lib.db  stratixii_pll_lib.db  stratixii_dll_lib.db alt_vtl.db]

read_vhdl  -vhdl_compiler  stratixii_all_pt.vhd
```

The Quartus II software converts any Quartus II timing assignments to PrimeTime assignments when generating the PrimeTime netlist. The Tcl script also includes a PrimeTime command that is used to read the Standard Delay Format Output (**.sdo**) file generated by the Quartus II software. You can place additional PrimeTime commands in the Tcl script to analyze or report on timing paths.

Table 9–1 shows some of the timing assignments converted by the Quartus II software for the PrimeTime software. For example, the `set_input_delay -max` command sets the input delay on an input pin.

Table 9–1. Equivalent Quartus II & PrimeTime Software Constraints

Quartus II Equivalent	PrimeTime Constraint
Clock defined on input pin, clock of 10 ns period and 50% duty cycle	`create_clock -period 10.000 -waveform {0 5.000} \ [get_ports clk] -name clk`
Input maximum delay of 1 ns on input pin, **din**	`set_input_delay -max -add_delay 1.000 -clock \ [get_clocks clk] [get_ports din]`
Input minimum delay of 1 ns on input pin, **din**	`set_input_delay -min -add_delay 1.000 -clock \ [get_clocks clk] [get_ports din]`
Output maximum delay of 3 ns on output pin, **out**	`set_output_delay -max -add_delay 3.000 -clock \ [get_clocks clk] [get_ports out]`

Running the PrimeTime Software

The PrimeTime software runs only on UNIX operating systems. If the Quartus II output files for the PrimeTime software were generated by running the Quartus II software on a PC/Windows based system then follow these steps to run the PrimeTime software using Quartus II output files:

1. Install the PrimeTime libraries on a Unix System by installing Quartus II software on UNIX. The PrimeTime libraries are located in the <*Quartus II installation directory*>**/eda/synopsys/primetime/lib** directory.

2. Copy the Quartus II output files to the appropriate UNIX directory. You may need to run a PC to UNIX program such as `dos2unix` to remove any control characters.

3. Modify the Quartus II path in Tcl scripts to point to the PrimeTime libraries, as described in Step 1.

Analyzing Quartus II Projects

The PrimeTime software is controlled with Tcl scripts and can be run through the `pt_shell`. You can run the <*revision_name*>**_pt_v.tcl** script file, for example, by typing the following at a UNIX system command prompt:

```
pt_shell -f revision_name_pt_v.tcl ↵
```

After all Tcl commands in the script are interpreted, the PrimeTime software returns control to the **pt_shell** prompt, which allows the use of other commands.

Other pt_shell Commands

Additional **pt_shell** commands can be executed at the **pt_shell** prompt, including the **man** program. For example, to read documentation about the `report_timing` command, type the following at the **pt_shell** prompt:

```
man report_timing ↵
```

List all commands available in the **pt_shell** by typing the following at the **pt_shell** prompt:

```
help ↵
```

Type `quit ↵` at the **pt_shell** prompt to close **pt_shell**.

You can also activate **pt_shell** without a script file by typing `pt_shell↵` at the UNIX command line prompt.

PrimeTime Timing Reports

Sample of the PrimeTime Software Timing Report

After executing the script, the PrimeTime software generates a timing report. If the timing constraints are not met, `Violated` is displayed at the end of the timing report. The timing report also gives the negative slack.

The PrimeTime software report is similar to the sample that follows. The starting point in this report is a register clocked by clock signal, `clock`, the endpoint is another register, `inst3-I.lereg`.

```
Startpoint: inst2~I.lereg
  (rising edge-triggered flip-flop clocked by clock)
Endpoint: inst3~I.lereg
  (rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: min
Point                                                 Incr    Path
-------------------------------------------------------------------
clock clock (rise edge)                               0.000   0.000
clock network delay (propagated)                      3.166   3.166
inst2~I.lereg.clk (stratix_lcell_register)            0.000   3.166r
inst2~I.lereg.regout (stratix_lcell_register)      <-0.176*3.342r
inst2~I.regout (stratix_lcell)                        0.000*  3.342r
inst3~I.datac (stratix_lcell)                         0.000*  3.342r
inst3~I.lereg.datac (stratix_lcell_register)          3.413*  6.755r
data arrival time                                             6.755
clock clock (rise edge)                               0.000   0.000
clock network delay (propagated)                      3.002   3.002
inst3~I.lereg.clk (stratix_lcell_register)                    3.002r
library hold time                                     0.100*  3.102
data required time                                            3.102
-------------------------------------------------------------------
data required time                                            3.102
data arrival time                                            -6.755
-------------------------------------------------------------------
slack (MET)                                                   3.653
```

Comparing Timing Reports From the Quartus II & the PrimeTime Software

The Quartus II Timing Analyzer generates a static timing report for every successful design compilation. The timing report lists all analyzed timing paths in your design and indicates whether or not these paths have met or violated their timing requirements. Violations are reported only if timing constraints were specified. The timing report generated by the Quartus II software differs from those found in the PrimeTime software. Both applications provide the same data but it is presented in a different

format by each application. The following sections show how the PrimeTime software reports the following slack values differently from the Quartus II Timing report:

- Clock Setup Slack
- Clock Hold Slack
- Input and Output Delay Slack

Clock Setup Relationship & Slack

The Quartus II Timing Analyzer performs a setup check that ensures that the data launched by source registers is latched correctly at the destination registers. The Timing Analyzer does this by determining the data arrival time and clock arrival time at the destination registers, and compares this data with the setup time delay of the destination register. The equation below expresses the inequality that is used for a setup check. The data arrival time includes the longest path from the clock to the source register, the clock-to-out micro delay of the source register, and the longest path from the source register to the destination register. The clock arrival time is the shortest delay from the clock to the destination register.

$$\text{Clock Arrival} - \text{Data Arrival} \geq t_{su}$$

Slack is the margin by which a timing requirement is met or not met. Positive slack indicates the margin by which a requirement is met. Negative slack indicates the margin by which a requirement was not met. The Quartus II Timing Analyzer determines the clock setup slack, with the following equation:

$$\text{Clock Setup Slack} = \text{Largest Register-to-Register Requirement} - \text{Longest Register-to-Register Delay}$$

The longest register-to-register delay in the previous equation is equal to the register-to-register data delay.

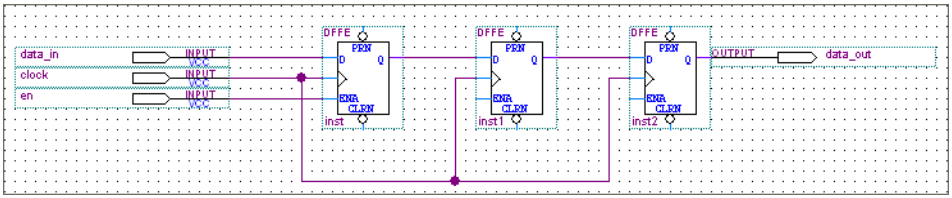
$$\text{Largest Register-To-Register Requirement} = \text{Setup Relationship Between Source and Destination} + \text{Largest Clock Skew} - \text{Micro } t_{co} \text{ of Source Register} - \text{Micro } t_{su} \text{ of Destination Register}$$

$$\text{Setup Relationship Between Source and Destination} = \text{Latch edge} - \text{Launch Edge}$$

$$\text{Clock Skew} = \text{Shortest Clock Path to Destination} - \text{Longest Clock Path to Source}$$

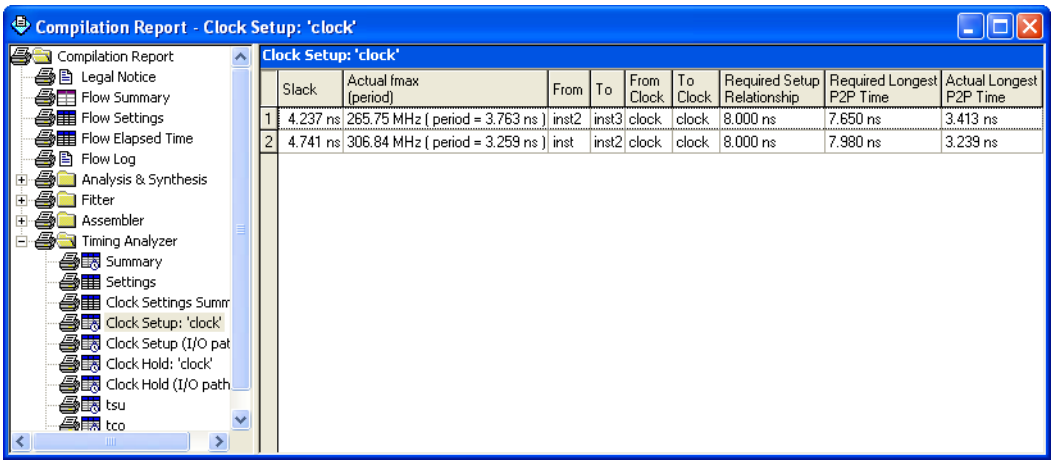
For a simple three register design, refer to Figure 9–3.

Figure 9–3. Simple Three Register Design



The Quartus II Timing Analyzer generates a report for the design, as shown in Figure 9–3.

Figure 9–4. Timing Analyzer Report from Figure 9–3



	Slack	Actual fmax (period)	From	To	From Clock	To Clock	Required Setup Relationship	Required Longest P2P Time	Actual Longest P2P Time
1	4.237 ns	265.75 MHz (period = 3.763 ns)	inst2	inst3	clock	clock	8.000 ns	7.650 ns	3.413 ns
2	4.741 ns	306.84 MHz (period = 3.259 ns)	inst	inst2	clock	clock	8.000 ns	7.980 ns	3.239 ns

The equations shown above are similar to those found in other static timing analysis tools, such as, the PrimeTime software. The following equations, used by the PrimeTime software, are essentially the same as those used by the Quartus II software, but they are rearranged.

Slack = Data Required - Data Arrival

Clock Arrival = Latch Edge + Shortest Clock Path to Destination

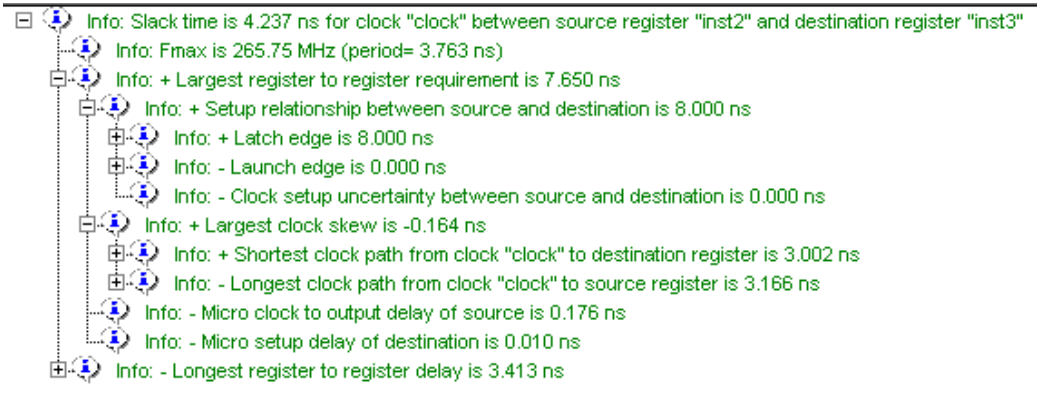
Data Required = Clock Arrival – Micro t_{su}

Data Arrival = Launch Edge + Longest Clock Path to Source + Micro t_{CO} + Longest Data Delay

The longest data delay in the previous equation is equal to register-to-register data delay.

Figure 9–5 shows a clock setup check in the Quartus II software.

Figure 9–5. Clock Setup Check for the Quartus II Software



The following results are obtained by extracting the numbers from the Timing Analysis report and applying to the clock setup slack equations from the Quartus II software:

Setup Relationship Between Source and Destination = Latch Edge – Launch Edge – Clock Setup Uncertainty
= 8.0 – 0.0 – 0.0 = 8.0 ns

Clock Skew = Shortest Clock Path To Destination – Longest Clock Path To Source
= 3.002 – 3.166 = -0.164 ns

Largest Register-to-Register Requirement = Setup Relationship Between Source and Destination + Largest Clock Skew – Micro t_{CO} of Source Register - Micro t_{SU} of Destination Register
= 8 + (-0.164) – 0.176 – 0.010 = 7.650 ns

Clock Setup Slack = Largest Register-to-Register Requirement – Longest Register-to-Register Delay
= 7.650 – 3.413 = 4.237 ns

For the same register-to-register path, the PrimeTime software generates a clock setup report as shown below:

```
Startpoint: inst2~I.lereg
  (rising edge-triggered flip-flop clocked by clock)
Endpoint: inst3~I.lereg
  (rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: max  Point                                Incr    Path
-----------------------------------------------------------------
clock clock (rise edge)                             0.000   0.000
clock network delay (propagated)                    3.166   3.166
inst2~I.lereg.clk (stratix_lcell_register)          0.000   3.166r
inst2~I.lereg.regout (stratix_lcell_register) <-0.176*  3.342r
inst2~I.regout (stratix_lcell) <-                   0.000*  3.342r
inst3~I.datac (stratix_lcell) <-                    0.000*  3.342r
inst3~I.lereg.datac (stratix_lcell_register)        3.413*  6.755r
data arrival time                                           6.755
clock clock (rise edge)                             8.000   8.000
clock network delay (propagated)                    3.002  11.002
inst3~I.lereg.clk (stratix_lcell_register)                 11.002r
library setup time                                 -0.010* 10.992
data required time                                         10.992
-----------------------------------------------------------------
data required time                                        10.992
data arrival time                                         -6.755
-----------------------------------------------------------------
slack (MET)                                                4.237
```

Clock Hold Relationship & Slack

The Quartus II Timing Analyzer performs a hold time check along every register-to-register path in the design to ensure that no hold time violations have occurred. The hold time check verifies that data from the source register does not reach the destination until after the hold time of the destination register. The condition used for a hold check is shown in the following equation:

$$\text{Data Arrival} - \text{Clock Arrival} \geq t_H$$

Slack is the margin by which a timing requirement is met or not met. Positive slack indicates the margin by which a requirement is met, and negative slack indicates the margin by which a requirement was not met. The Quartus II software determines the clock hold slack with the following equations:

Clock Hold Slack = Shortest Register-To-Register Delay – Smallest Register-To-Register Requirement

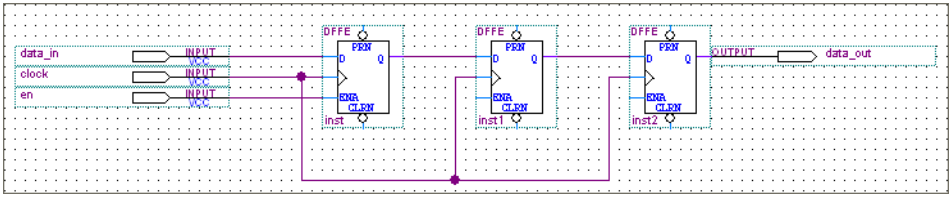
Smallest Register-To-Register Requirement = Hold Relationship Between Source and Destination + Smallest Clock Skew – Micro t_{CO} of Source + Micro t_H of Destination

Hold relationship between source and destination = Latc edge – Launch edge

Smallest clock skew = longest clock path from clock to destination register – shortest clock path from clock to source register

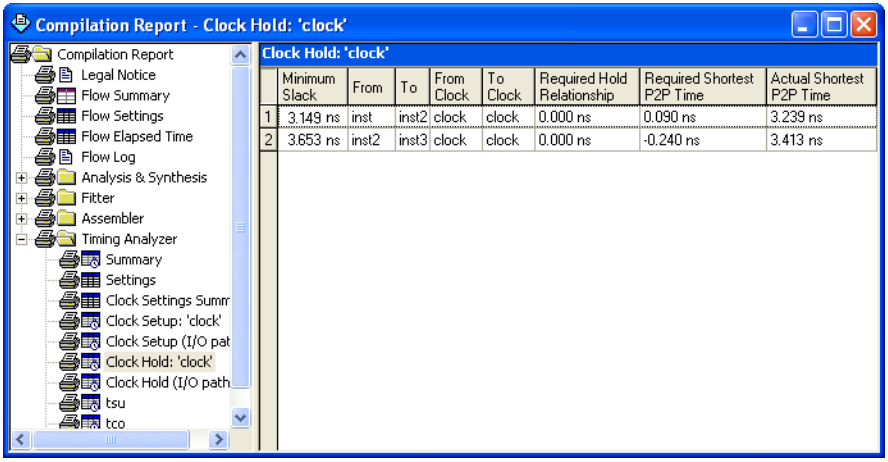
Figure 9–6 shows a simple three register design.

Figure 9–6. A Simple Three Register Design



The Quartus II Timing Analyzer generates a report as shown in Figure 9–7.

Figure 9–7. Timing Analyzer Report Generated from the Three Register Design



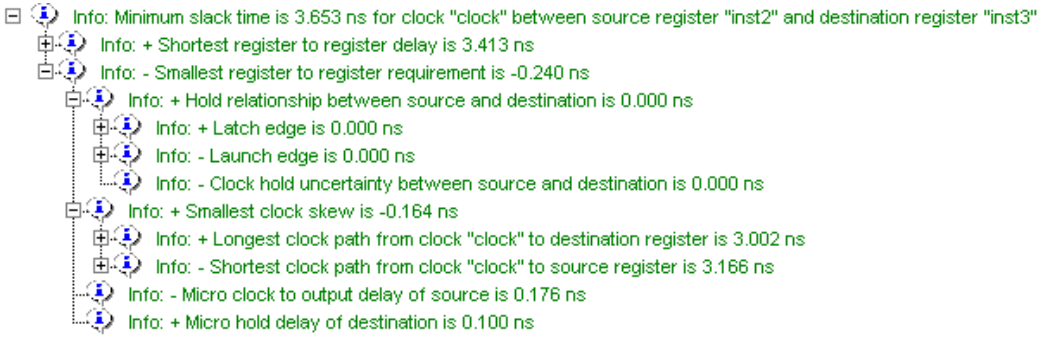
The previous equations are similar to those found in the Quartus II software. The following equations are the same equations that are used by the PrimeTime software, but they are rearranged.

Slack = Data Required – Data Arrival
Clock Arrival = Latch Edge + Longest Clock Path to Destination
Data Required = Clock Arrival + Micro t_H
Data Arrival = Launch Edge + Shortest Clock Path to Source + Micro t_{CO} + Shortest Data Delay

The shortest register-to-register delay in the previous equation is equal to register-to-register data delay.

Figure 9–8 shows a clock setup check in the Quartus II software.

Figure 9–8. Clock Hold Check for the Quartus II Timing Analyzer



The following results are obtained by extracting the numbers from the Timing Analysis report and applying the clock setup slack equations from the Quartus II software.

Clock Hold Slack = Shortest Register-To-Register Delay – Smallest Register-To-Register Requirement
= 3.413 – (-0.240) = 3.653 ns

Smallest Register-To-Register Requirement = Hold Relationship Between Source and Destination + Smallest Clock Skew – Micro t_{CO} of Source + Micro t_H of Destination
= 0 + (-0.164) – 0.176 + 0.100 = – 0.240 ns

Hold Relationship Between Source and Destination = Latch – Launch
= 0.0 – 0.0 ns

Smallest Clock Skew = Longest Clock Path From Clock to Destination Register – Shortest Clock Path from Clock to Source Register
= 3.002 – 3.166 = -0.164 ns

For the same register-to-register path, the PrimeTime software generates the following report:

```
Startpoint: inst2~I.lereg
  (rising edge-triggered flip-flop clocked by clock)
Endpoint: inst3~I.lereg
  (rising edge-triggered flip-flop clocked by clock)
Path Group: clock
Path Type: min
Point                                              Incr    Path
  ------------------------------------------------------------
  clock clock (rise edge)                          0.000   0.000
  clock network delay (propagated)                 3.166   3.166
  inst2~I.lereg.clk (stratix_lcell_register)       0.000   3.166r
  inst2~I.lereg.regout (stratix_lcell_register)<-0.176* 3.342r
  inst2~I.regout (stratix_lcell)                   0.000*  3.342r
  inst3~I.datac (stratix_lcell)                    0.000*  3.342r
  inst3~I.lereg.datac (stratix_lcell_register)     3.413*  6.755r
  data arrival time                                        6.755

  clock clock (rise edge)                          0.000   0.000
  clock network delay (propagated)                 3.002   3.002
  inst3~I.lereg.clk (stratix_lcell_register)               3.002r
  library hold time                                0.100*  3.102
  data required time                                       3.102
  ------------------------------------------------------------
  data required time                                       3.102
  data arrival time                                       -6.755
  ------------------------------------------------------------
  slack (MET)                                              3.653
```

Both sets of hold slack equations can be used to determine the hold slack value of any path.

Input Delay & Output Delay Relationships & Slack

Input delay and output delay reports generated by the Quartus II Timing Analyzer are similar to the clock setup and clock hold relationship reports. Figure 9–9 shows the input delay and output delay report for the design shown in Figure 9–3 on page 9–9.

Figure 9–9. Input & Output Delay Report

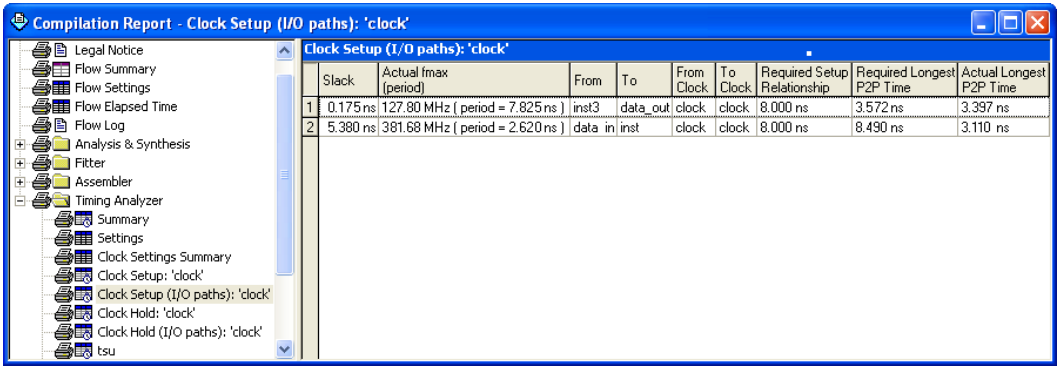
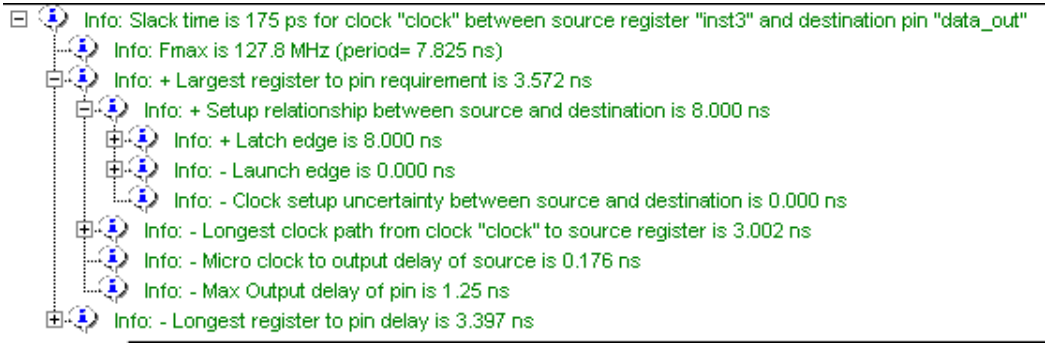


Figure 9–10 shows the fully expanded view for the output delay path.

Figure 9–10. Output Delay Path



For the same output delay path, the PrimeTime software generates a report similar to the following:

```
Startpoint: inst3~I.lereg
   (rising edge-triggered flip-flop clocked by clock)
Endpoint: data_out
   (output port clocked by clock)
Path Group: clock
Path Type: max  Point                              Incr    Path
-----------------------------------------------------------------
clock clock (rise edge)                            0.000   0.000
clock network delay (propagated)                   3.002   3.002
inst3~I.lereg.clk (stratix_lcell_register)         0.000   3.002r
inst3~I.lereg.regout (stratix_lcell_register)<- 0.176*3.178r
inst3~I.regout (stratix_lcell)<-                   0.000   3.178r
data_out~I.datain (stratix_io)<-                   0.000   3.178r
data_out~I.out_mux3.A (mux21) <-                   0.000   3.178r
data_out~I.out_mux3.MO (mux21)<-                   0.000   3.178r
data_out~I.and2_22.IN1 (AND2)<-                    0.000   3.178r
data_out~I.and2_22.Y (AND2)<-                      0.000   3.178r
data_out~I.out_mux1.A (mux21)<-                    0.000   3.178r
data_out~I.out_mux1.MO (mux21)<-                   0.000   3.178r
data_out~I.inst1.datain (stratix_asynch_io)<-  0.902*  4.080r
data_out~I.inst1.padio (stratix_asynch_io)<-   2.495*  6.575r
data_out~I.padio (stratix_io)<-                    0.000   6.575r
data_out (out)                                     0.000   6.575r
data arrival time                                          6.575
clock clock (rise edge)                            8.000   8.000
clock network delay (propagated)                   0.000   8.000
output external delay                              1.250   6.750
data required time                                         6.750
-----------------------------------------------------------------
data required time                                         6.750
data arrival time                                          6.575
-----------------------------------------------------------------
slack (MET)                                                0.175
```

To generate a list of the 100 worst paths, and place this data into a file called **file.timing**, type the following at the `pt_shell` prompt:

```
report_timing -nworst 100 > file.timing ↵
```

Timing paths in the PrimeTime software are listed in the order of most-negative-slack to most-positive-slack. PrimeTime does not categorize failing paths by default. Timing setup (t_{SU}) and timing hold (t_H) times are not listed separately. In the PrimeTime software, each path is shown with a start and end point, for example, if it is a register-to-register or input-to-register type of path. If you only use the **`report_timing`** part of the command without adding a `-delay` option, only the `setup-time-related` timing paths are reported.

The following command is used to create a minimum timing report or a list of hold-time-related violations.

```
report_timing -delay_type min ↵
```

Ensure that the correct SDO file, either minimum or maximum delays, is loaded before issuing this command.

Static Timing Analysis Differences

Under certain design conditions several static timing analysis differences can exist between the Quartus II Timing Analyzer and the PrimeTime software. The following section explains the differences between the two static timing analysis tools.

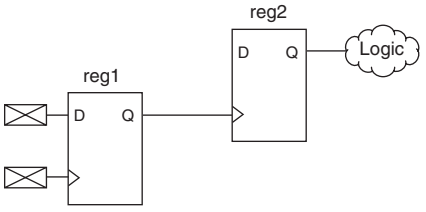
Encrypted Intellectual Property Blocks

The Quartus II software has the capability to decrypt all Intellectual Property (IP) blocks, designed for Altera devices, which have been encrypted by their vendors. The decryption process allows the Quartus II software to perform a full compilation on the design containing an encrypted IP block. This also allows the Quartus II Timing Analyzer to perform a thorough static timing analysis on the design. However, when the PrimeTime software is designated as the static timing analysis tool, the Quartus II EDA Netlist Writer does not generate either a VHO or VO netlist file for designs containing encrypted IP blocks whose license does not permit generation of output netlists for third-party tools.

Registered Clock Signals

Registered clock signals are clock signals that pass through a register prior to reaching the clock port of a sequential element. Figure 9–11 shows an example of a registered clock signal.

Figure 9–11. Registered Clock Signal



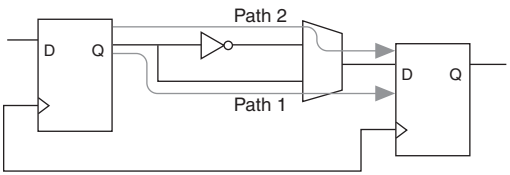
If no clock setting is applied to the register on the clock path (shown as register reg1 in Figure 9–11), the Quartus II Timing Analyzer treats the register in the clock path as a buffer. The delay of the buffer is equal to the CELL delay of the register plus the t_{CO} of the register. The PrimeTime software does not treat the register as a buffer.

For more information on creating clock settings, refer to the *Timing Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Multiple Source & Destination Register Pairs

In any design there may exist multiple paths from a source register to a destination register. Each path from the source register to the destination register may have a different delay value due to the different routes taken. For example, Figure 9–12 shows a sample design that contains multiple path pairs between the source register and destination register.

Figure 9–12. Multiple Source & Destination Pairs



The Quartus II Timing Analyzer analyzes all source and destination pairs, but only reports the source and destination register pair with the worst slack. For example, if the Path 2 pair delay is greater than the Path 1 pair delay in Figure 9–12, the Quartus II Timing Analyzer reports the slack value of the Path 2 pair and not the Path 1 pair. The PrimeTime software reports all possible source and destination register pairs.

Latches

By default, the Quartus II software implements all latches as combinational loops. The Quartus II Timing Analyzer can analyze such latches by treating them as registers with inverted clocks. The Quartus II Timing Analyzer analyzes latches as a combinational loop modeled as a combinational delay.

For more information on latch analysis, refer to the *Quartus II Timing Analysis* chapter in volume 3 of the *Quartus II Handbook*.

The PrimeTime software, on the other hand, always analyzes these latches as combinational loops, as defined in the netlist file.

LVDS I/O

When implementing the dedicated LVDS transceivers in your design the Quartus II Timing Analyzer generates the Receiver Skew Margin (RSKM) report and a Channel-to-Channel Skew (TCCS) report. The PrimeTime software does not generate these reports.

Clock Latency

When a single clock signal feeds both the source and destination registers of a register-to-register path, and either an Early Clock Latency or a Late Clock Latency assignment has been applied to the clock signal, the Quartus II Timing Analyzer does not factor in the clock latency values when calculating the clock skew between the two registers. The Quartus II Timing Analyzer factors in the clock latency values when the clock signal to the source and destination registers of a register-to-register path are different. The PrimeTime software applies the clock latency values when a single clock signal or different clock signals feeds the source and destination registers of a register-to-register path.

Input & Output Delay Assignments

When a purely combinational (non-registered) path exists between an input pin and output pin of the Altera FPGA have both an input delay and an output delay assignments applied, respectively, the Quartus II Timing Analyzer does not perform a clock setup or clock hold analysis. The PrimeTime software analyzes these paths.

Conclusion

The Quartus II software can export a netlist, constraints, and timing information for use with the PrimeTime software. The PrimeTime software can use data from either best-case or worst case Quartus II timing models to measure timing. The PrimeTime software is controlled using a Tcl script generated by the Quartus II software that you can customize to direct the PrimeTime software to produce violation and slack reports.

Section III. Power Estimation & Analysis

As FPGA designs grow larger and processes continue to shrink, power becomes an ever-increasing concern. When designing a printed circuit board, the power consumed by a device needs to be accurately estimated to develop an appropriate power budget, and to design the power supplies, voltage regulators, heat sink, and cooling system.

The Quartus® II software allows you to estimate the power consumed by your current design during timing simulation. The power consumption of your design can be calculated using the Microsoft Excel-based power calculator, or the Simulation-Based Power Estimation features in the Quartus II software. This section explains how to use both.

This section includes the following chapter:

- Chapter 10, PowerPlay Power Analysis

Revision History

Chapter *PowerPlay Early Power Estimator* was removed from the *Quartus II Handbook* v6.0.

Chapter *Simulation-Based Power Estimation* was removed from the *Quartus II Handbook* v5.1.

The table below shows the revision history for Chapter 10.

Chapter(s)	Date / Version	Changes Made
10	May 2006 v6.0.0	Chapter title changed to *PowerPlay Power Analysis*. Updated for for the Quartus II software version 6.0.0: • Added information about the EPE tools. • Added information about the power analyzer.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	• Updated information. • Updated figures. • New functionality for Quartus II software 5.0.
	Dec. 2004 v1.0	Initial release.

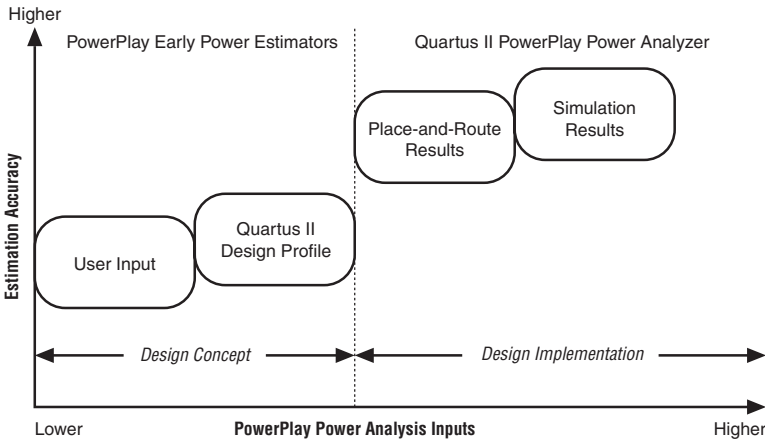
10. PowerPlay Power Analysis

QII53013-6.0.0

Introduction

As designs grow larger and process technology continues to shrink, power becomes an increasingly important design consideration. When designing a printed circuit board (PCB), the power consumed by a device needs to be accurately estimated to develop an appropriate power budget and to design the power supplies, voltage regulators, heat sink, and cooling system. The PowerPlay power analysis tools, made available by Altera®, provide improved power consumption accuracy and the ability to estimate power consumption from early design concept through design implementation, as shown in Figure 10–1.

Figure 10–1. PowerPlay Power Analysis



Depending where you are in your design cycle and the accuracy of the estimation required, you can either use the PowerPlay Early Power Estimator spreadsheet or the PowerPlay Power Analyzer Tool in the Quartus® II software. You can use the PowerPlay Early Power Estimator spreadsheet during the board design and layout phase to obtain a power estimate and then design for proper power management. The PowerPlay Power Analyzer Tool is used to obtain an accurate estimation of power after the design is complete, ensuring that thermal and supply budgets are not violated.

You can estimate power consumption for Stratix® II, Stratix II GX, Stratix, Stratix GX, Cyclone™ II, Cyclone, HardCopy® II, and MAX® II devices with the Microsoft Excel-based PowerPlay Early Power Estimator spreadsheet or the PowerPlay Power Analyzer Tool.

For more information on acquiring the PowerPlay Power Estimator spreadsheet for Stratix II, Stratix II GX, Stratix, Stratix GX, Cyclone II, Cyclone, HardCopy II, and MAX II devices and its use, refer to **www.altera.com/support/devices/estimator/pow-powerplay.html**.

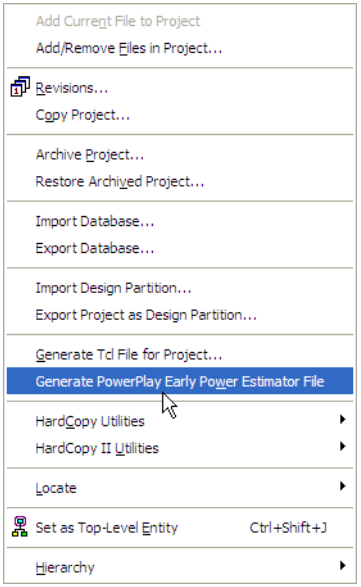
Quartus II Early Power Estimator File

When entering data into the Early Power Estimator spreadsheet, you must enter the device resources, operating frequency, toggle rates, and other parameters. This requires familiarity with the design. If you do not have an existing design, then you must estimate the number of device resources used in your design and enter it manually.

If you already have an existing design or a partially completed design, the power estimator file that is generated by the Quartus II software can aid in completing the PowerPlay Early Power Estimator spreadsheet.

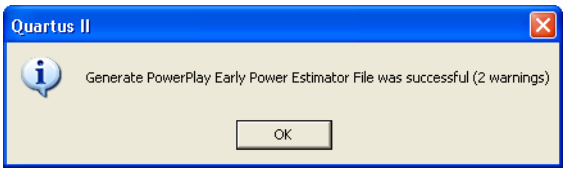
To generate the power estimation file, you must first compile your design in the Quartus II software. After compilation is complete, on the Project menu, click **Generate PowerPlay Early Power Estimator File**. This command instructs the Quartus II software to write out a power estimator Comma-Separated Value (**.csv**) file (or a text **[.txt]** file for older device families) (Figure 10–2).

Figure 10–2. Generate PowerPlay Early Power Estimator File Option



After the Quartus II software successfully generates the power estimator file, a message is displayed (Figure 10–3).

Figure 10–3. Generate PowerPlay Early Power Estimator File Message



The power estimator file is named <*name of Quartus II project*> **_early_pwr.csv**. Figure 10–4 is an example of the contents of a power estimation file generated by the Quartus II software version 6.0 using a Stratix II device.

Figure 10–4. Example of Power Estimation File

EARLY_POWER_ESTIMATOR_FILE_FORMAT_VERSION	4										
QUARTUS_II_VERSION	6.0 Internal Build 147 02/26/2006 SJ Full Version										
PROJECT	Multaccum										
REVISION	Multaccum										
PROJECT_FILE	C:/test/Section1-b/Multaccum/Multaccum.qpf										
TIME	Thu Mar 09 18:27:49 2006										
TIME_SECONDS	1141957669										
FAMILY	Stratix II										
DEVICE	EP2S60										
PACKAGE	FBGA										
PART	EP2S60F1020C3										
POWER_USE_DEVICE_CHARACTERISTICS	TYPICAL										
POWER_AUTO_COMPUTE_TJ	ON										
POWER_TJ_VALUE	25										
POWER_USE_CUSTOM_COOLING_SOLUTION	OFF										
POWER_PRESET_COOLING_SOLUTION	23 MM HEAT SINK WITH 200 LFPM AIRFLOW										
POWER_BOARD_THERMAL_MODEL	NONE (CONSERVATIVE)										
POWER_USE_TA_VALUE	25										
POWER_BOARD_TEMPERATURE	-1										
POWER_OJC_VALUE	0.13										
POWER_OCS_VALUE	0.1										
POWER_OSA_VALUE	1.8										
POWER_OJB_VALUE	-1										
BLOCK	I/O	count	5	avg_toggle	3.04E+08	avg_toggle	5.956863	fmax	51	io_mode	input
BLOCK	I/O	count	35	avg_toggle	22514286	avg_toggle	0.441457	fmax	51	io_mode	output
BLOCK	I/O	count	3	avg_toggle	2.31E+08	avg_toggle	4.522876	fmax	51	io_mode	input
BLOCK	I/O	count	8	avg_toggle	2.91E+08	avg_toggle	5.698529	fmax	51	io_mode	input
BLOCK	I/O	count	1	avg_toggle	24000000	avg_toggle	0.470588	fmax	51	io_mode	output
BLOCK	I/O	count	10	avg_toggle	15700000	avg_toggle	0.157789	fmax	99.5	io_mode	output
BLOCK	DSP block output	count	4	avg_toggle	517241.4	avg_toggle	0.005198	fmax	99.5	mac_mode	Simple Multiplie
BLOCK	DSP block output	count	15	avg_toggle	0	avg_toggle	0	fmax	99.5	mac_mode	Simple Multiplie
BLOCK	Combinational cell	count	966	avg_toggle	62387787	avg_toggle	0.627013	fmax	99.5		
BLOCK	Combinational cell	count	846	avg_toggle	58879704	avg_toggle	1.154504	fmax	51		
BLOCK	Register cell	count	403	avg_toggle	2565757	avg_toggle	0.025787	fmax	99.5		
BLOCK	Register cell	count	576	avg_toggle	22967014	avg_toggle	0.450334	fmax	51		
BLOCK	Clock control block	count	1	avg_toggle	1.99E+08	avg_toggle	2	fmax	99.5	global_type	Global Clock

The power estimator file is named <*name of Quartus II project*> **_early_pwr.txt** in older device families.

The PowerPlay Early Power Estimator spreadsheet includes the Import Data macro that parses the information in the power estimation file and transfers it into the spreadsheet. If you do not want to use the macro, you can transfer the data into the Early Power Estimator spreadsheet manually.

If the existing Quartus II project represents only a portion of your full design, you should enter the additional resources used in the final design manually. Therefore, you can edit the spreadsheet and add additional device resources after importing the power estimation file information.

PowerPlay Early Power Estimator File Generator Compilation Report

After a successful generation of the power estimation file, a PowerPlay Early Power Estimator File Generator report is created under the Compilation Report section. This report is divided into the different sections, such as Summary, Settings, Generated Files, Confidence Metric Details, and Signal Activities.

For more information on PowerPlay Early Power Estimator File Generator report, refer to "PowerPlay Power Analyzer Compilation Report" on page 10–35.

Table 10–1 lists the main differences between the PowerPlay Early Power Estimator and the PowerPlay Power Analyzer.

Table 10–1. Comparison of PowerPlay Early Power Estimator & PowerPlay Power Analyzer

Characteristic	PowerPlay Early Power Estimator	PowerPlay Power Analyzer
Phase in the design cycle	Any time	After fitting
Tool requirements	Spreadsheet program/Quartus II software	Quartus II software
Accuracy	Medium	Medium to very high
Data inputs	• Resource usage estimates • Clock requirements • Environmental conditions • Toggle Rate	• Design after fitting • Clock requirements • Register transfer level (RTL) simulation results (optional) • Post-fitting simulation results (optional) • Signal activities per node or entity (optional) • Signal activity defaults • Environmental conditions
Data outputs *(1)*	• Total thermal power dissipation • Thermal static power • Thermal dynamic power • Off-chip power dissipation • Voltage supply currents *(2)*	• Total thermal power • Thermal static power • Thermal dynamic power • Thermal I/O power • Thermal power by design hierarchy • Thermal power by block type • Thermal power dissipation by clock domain • Off-chip (non-thermal) power dissipation • Voltage supply currents *(2)*

Notes for Table 10–1:
(1) Early Power Estimator output varies by device family as some features may not be available.
(2) Available only for Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II device families.

The results of the Power Analyzer are only an estimation of power, not a specification. The purpose of the estimation is to help establish a guide for the design's power budget. Altera recommends that the actual power be measured on the board. You must measure the device's total dynamic current during device operation, because the estimate is very design dependent and depends on many variable factors including input vector quantity, quality, and exact loading conditions of a PCB design. Static

power consumption must not be based on empirical observation. The values reported by the Power Analyzer or datasheet must be used because the devices tested may not exhibit worst-case behavior.

Types of Power Analyses

Understanding the uses of power analysis and the factors affecting power consumption help you use the Power Analyzer effectively. Power analysis meets two significant planning requirements:

- **Thermal planning**: The designer must ensure that the cooling solution is sufficient to dissipate the heat generated by the device. In particular, the computed junction temperature must fall within normal device specifications.
- **Power supply planning**: Power supplies must provide adequate current to support device operation.

The two types of analyses are closely related because much of the power supplied to the device is dissipated as heat from the device. However, in some situations, the two types of analyses are not identical. For example, when you use terminated I/O standards, some of the power drawn from the FPGA device power supply is dissipated in termination resistors, rather than in the FPGA.

Power analysis also addresses the activity of the design over time as a factor that impacts the power consumption of the device. Static power is defined as the power consumed regardless of design activity. Dynamic power is the additional power consumed due to signal activity or toggling.

Factors Affecting Power Consumption

This section describes the factors affecting power consumption. Understanding these factors lets you use the Power Analyzer and interpret its results effectively.

Device Selection

Different device families have different power characteristics. Many parameters affect the device family power consumption, including choice of process technology, supply voltage, electrical design, and device architecture. For example, the Cyclone II device family architecture was designed to consume less static power than the high-performance, full-featured, Stratix II device family.

Power consumption also varies within a single device family. A larger device typically consumes more static power than a smaller device in the same family, due to its larger transistor count. Dynamic power can also increase with device size in devices that employ global routing

architectures such as the MAX device family. Stratix, Cyclone, and MAX II devices do not exhibit significantly increased dynamic power as device size increases.

The choice of device package also affects the device's ability to dissipate heat. This can impact your cooling solution choice required to meet junction temperature constraints.

Finally, process variation can affect power consumption. Process variation primarily impacts static power, since sub-threshold leakage current varies exponentially with changes in transistor threshold voltage. As a result, it is critical to consult device specifications for static power and not rely on empirical observation. Process variation weakly affects dynamic power.

Environmental Conditions

Operating temperature primarily affects device static power consumption. Higher junction temperatures result in higher static power consumption. The device thermal power and cooling solution that you use must result in the device junction temperature remaining within the maximum operating range for that device.

The main environmental parameters affecting junction temperature are the cooling solution and ambient temperature.

Air Flow

Air flow is a measure of how quickly heated air is removed from the vicinity of the device and replaced by air at ambient temperature. This can either be specified as "still air" when no fan is used, or as the linear feet per minute rating of the fan used in the system. Higher air flow decreases thermal resistance.

Heat Sink & Thermal Compound

A heat sink allows more efficient heat transfer from the device to the surrounding because of its large surface area exposed to the air. The thermal compound that interfaces the heat sink to the device also influences the rate of heat dissipation. The case-to-ambient thermal resistance (θ_{CA}) parameter describes the cooling capacity of the heat sink and thermal compound employed at a given airflow. Larger heat sinks and more effective thermal compounds reduce θ_{CA}.

Ambient Temperature

The junction temperature of a device is equal to:

$$T_{Junction} = T_{Ambient} + P_{Thermal} \cdot \theta_{JA}$$

where θ_{JA} is the total thermal resistance from the device transistors to the environment, having units of degrees Celsius per Watt. The value θ_{JA} is equal to the sum of the junction-to-case (package) thermal resistance (θ_{JC}) and the case-to-ambient thermal resistance (θ_{CA}) of your cooling solution.

Board Thermal Model

The thermal resistance of the path through the board is referred to as the junction-to-board thermal resistance (θ_{JB}) (the units are in degrees Celsius per Watt). This is used in conjunction with the board temperature, as well as the top-of-chip θ_{JA} and ambient temperatures, to compute junction temperature.

Design Resources

The design resource used greatly affects power consumption.

Number, Type & Loading of I/O Pins

Output pins drive off-chip components, resulting in high-load capacitance that leads to a high-dynamic power per transition. Terminated I/O standards require external resistors that generally draw constant (static) power from the output pin.

Number & Type of Logic Elements, Multiplier Elements & RAM Blocks

A design with more logic elements (LEs), multiplier elements, and memory blocks tends to consume more power than a design with fewer such circuit elements. Also, the operating mode of each circuit element affects its power consumption. For example, a digital signal processing (DSP) block performing 18×18 multiplications and a DSP block performing multiply-accumulate operations consume different amounts of dynamic power due to different amounts of internal capacitance being charged on each transition. Static power is also affected, to a small degree, by the operating mode of a circuit element.

Number & Type of Global Signals

Global signal networks span large portions of the device and have high capacitance, resulting in significant dynamic power consumption. The type of global signal is important as well. For example, Stratix II devices support several kinds of global clock networks that span either the entire device or a specific portion of the device (a regional clock network covers a quarter of the device). Clock networks that span smaller regions have

lower capacitance and therefore, tend to consume less power. In addition, the location of the logic array blocks (LABs) that are driven by the clock network can have an impact, because the Quartus II software automatically disables unused branches of a clock.

Signal Activities

The final important factor in estimating power consumption is the behavior of each signal in the design. The two vital statistics are the toggle rate and the static probability.

The toggle rate of a signal is the average number of times that the signal changes value per unit time. The units for toggle rate are transitions per second and a transition is a change from 1 to 0 or 0 to 1.

The static probability of a signal is the fraction of time that the signal is logic 1 during the period of device operation that is being analyzed. Static probability ranges from 0 (always at ground) to 1 (always at logic high).

Dynamic power increases linearly with the toggle rate as the capacitive load is charged more frequently for the logic and routing. The Quartus II models assume full rail-to-rail switching. For high toggle rates, especially on circuit output I/O pins, the circuit can transition before fully charging downstream capacitance. The result is a slightly conservative prediction of power by the Quartus II PowerPlay Power Analyzer.

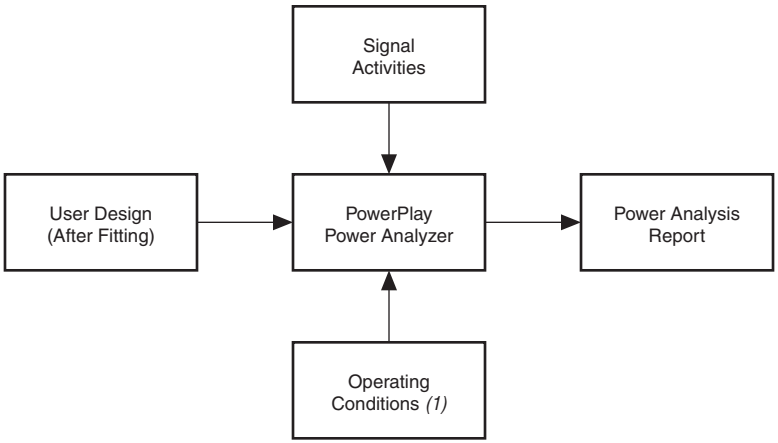
The static power consumed by both routing and logic can sometimes be affected by the static probabilities of their input signals. This effect is due to state-dependent leakage, and has a larger affect on smaller process geometries. The Quartus II software models this effect on devices at 90 nm (or smaller) if it is deemed important to the power estimate. The static power also varies with the static probability of a logic 1 or 0 on the I/O pin when output I/O standards drive termination resistors.

To get accurate results from power analysis, the signal activities that are used for the analysis must be representative of the actual operating behavior of the design. Inaccurate signal toggle rate data is the largest source of power estimation error.

PowerPlay Power Analyzer Flow

The PowerPlay Power Analyzer supports accurate and representative power estimation by letting you specify all the important design factors affecting power consumption. Figure 10–5 shows the high-level Power Analyzer flow.

Figure 10–5. PowerPlay Power Analyzer High-Level Flow



Note for Figure 10–5:
(1) Operating condition specifications are available only for the Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II device families.

The PowerPlay Power Analyzer requires that your design is synthesized and fit to the target device. Therefore, the Power Analyzer knows both the target device and how the design is placed and routed on the device. The electrical standard used by each I/O cell and the capacitive load on each I/O standard must be specified in the design to obtain accurate I/O power estimates.

Operating Conditions

For the Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II device families, you can specify the operating conditions for power analysis in the Quartus II software.

The following settings are available in the **Settings** dialog box:

- **Device power characteristics**— Should the Power Analyzer assume typical silicon or maximum power silicon? The typical setting is useful for comparing to empirical data measured on an average unit. Worst-case data provides a boundary to the worst-case device that you could receive.

- **Environmental conditions and junction temperature**— By default, the Power Analyzer automatically computes the junction temperature based on the specified ambient temperature and the cooling solution that you selected from a list. For a more accurate analysis, enter the thermal resistance of your cooling solution. For some cooling solutions, such as a heat sink with no forced airflow, the thermal resistance varies with the amount of thermal power that is dissipated. Air convection increases as the difference between the device temperature and the ambient temperature increases, reducing thermal resistance. When entering a thermal resistance in such cases, it is important to use the thermal resistance that occurs when the heat flow (Q) is equal to the thermal power generated by the device. You can also specify a junction temperature in the PowerPlay Power Analyzer. However, Altera does not recommend this because the PowerPlay Power Analyzer provides more accurate results by computing the junction temperature.

- **Board Thermal Modeling**— If you want the Power Analyzer thermal model to take the θ_{JB} into consideration, set the board thermal model to either **Typical** or **Custom**. This feature produces more accurate thermal power estimation.

  A **Typical** board thermal model automatically sets θ_{JB} to a value based on the package and device selected. You only need to specify a board temperature. If you choose a **Custom** board thermal model, you must specify a value for θ_{JB} and a board temperature. If you do not want the PowerPlay Power Analyzer thermal model to take the θ_{JB} resistance into consideration, set the **Board thermal model** option to **None** (conservative). In this case, the path through the board and power dissipation is not considered, and a more conservative thermal power estimate is obtained.

  The **Board thermal model** option is only available if you select the **Auto compute junction temperature** option with the pre-set cooling solution set to some heat sink solution option or custom solution. This option is disabled when a cooling solution with no heat sink is selected, as thermal conduction through the board is included in the θ_{JA} value used to compute a junction temperature in that case.

Signal Activities Data Sources

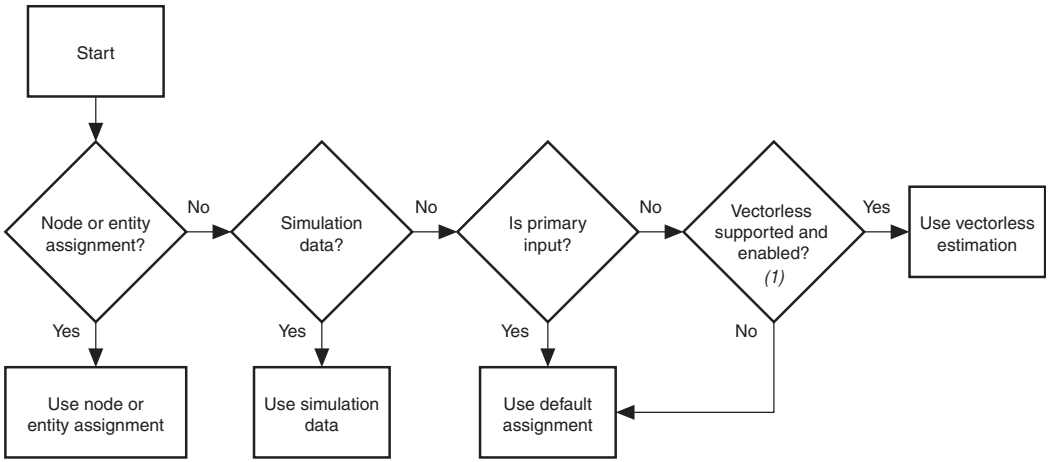
The Power Analyzer provides a flexible framework for specifying signal activities. This reflects the importance of using representative signal activity data during power analysis. You can use the following sources to provide information on signal activity:

- Simulation results

- User-entered node, entity, and clock assignments
- User-entered default toggle rate assignment
- Vectorless estimation

The PowerPlay Power Analyzer lets you mix and match the signal activity data sources on a signal-by-signal basis. Figure 10–6 shows the priority scheme. The data sources are described in the following sections.

Figure 10–6. Signal Activity Data Source Priority Scheme



Note to Figure 10–6:

(1) Vectorless estimation is available only for the Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II device families.

Simulation Results

The Power Analyzer directly reads the waveforms generated by a design simulation. The static probability and toggle rate for each signal is calculated from the simulation waveform. Power analysis is most accurate when simulations are generated using representative input stimuli.

The Power Analyzer reads the results generated by the following simulators:

- Quartus II Simulator
- ModelSim® VHDL, ModelSim Verilog HDL, ModelSim-Altera VHDL, ModelSim-Altera Verilog
- NC-Verilog, NC-VHDL
- VCS

Signal activity and static probability information are stored in a Signal Activity File (**.saf**), described in the "Signal Activities" section. The Quartus II simulator generates a Signal Activity File which is then read by the Power Analyzer.

For third-party simulators, use the Quartus II EDA Tool Settings for Simulation to specify a **Generate Value Change Dump** file script. These scripts instruct the third-party simulators to generate a Value Change Dump File (**.vcd**) that encodes the simulated waveforms. The Quartus II Power Analyzer reads this file directly to derive toggle rate and static probability data for each signal.

Third-party EDA simulators, other than those listed above, can generate a Value Change Dump File that can then be used with the Power Analyzer. For those simulators, it is necessary to manually create a simulation script to generate the appropriate Value Change Dump File.

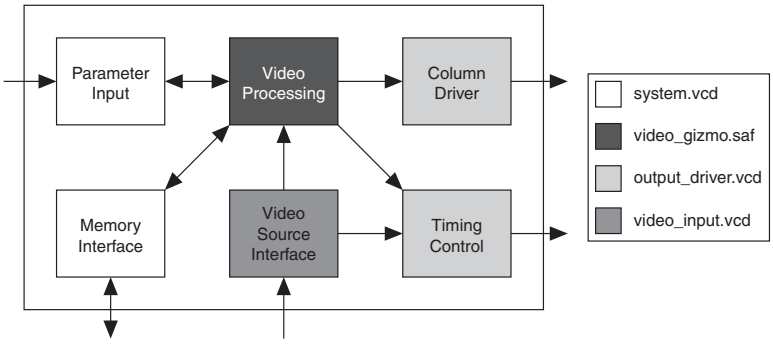
You can use the Signal Activity File or a Value Change Dump File created for Power Analysis to guide PowerPlay Optimization during Fitting in order to reduce design power.

For more information on power optimization, refer to the *Power Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Using Simulation Files in Modular Design Flows

A common design practice is to create modular or hierarchical designs in which you develop each design entity separately and then instantiate it in a higher-level entity, forming a complete design. Simulation is performed on a complete design or on each modular design for verification. The Quartus II PowerPlay Power Analyzer Tool supports modular design flows when reading the signal activities generated from these simulation files, as shown in Figure 10–7.

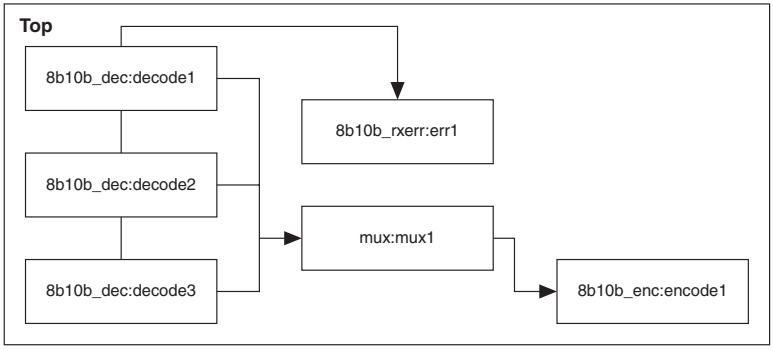
Figure 10–7. Modular Simulation Flow



When specifying a simulation file, an associated design entity name may be given, such that the signal activities derived from the simulation file (Value Change Dump File or Signal Activity File) can be imported into the Power Analyzer for that particular design entity. The PowerPlay Power Analyzer Tool also supports the specification of multiple signal activity files for power analysis with each having an associated design entity name to allow the integration of partial design simulations into a complete design power analysis. When specifying multiple signal activity files for your design, it is possible that more than one simulation file will contain signal activity information for the same signal. In the case where multiple signal activity files are applied to the same design entity, the signal activity used in the power analysis is the equal-weight arithmetic average of each signal activity file. Also in the case where multiple simulation files are applied to design entities at different levels in the design hierarchy, the signal activity used in the power analysis is derived from the simulation file that is applied to the most specific design entity.

Figure 10–8 shows an example of a hierarchical design. The design Top consists of three 8b/10b Decoders, followed by a multiplexer whose output is then encoded again before being output from the design. There is also an error-handling module that handles any 8b/10b decoding errors. The top-level module, called Top, automatically contains the design's top-level entity and any logic not defined as part of another module. The design file for the top-level may be just a wrapper for the hierarchical entities below it, or it may contain its own logic. The following usage scenarios show common ways that you may simulate your design and import signal activity files into the PowerPlay Power Analyzer Tool.

Figure 10–8. Example Hierarchical Design



Complete Design Simulation

You can simulate the entire design Top, generating a Value Change Dump File if you use a third-party simulator, or generating a Signal Activity File if you use the Quartus II Simulator. The Value Change Dump File or Signal Activity File can then be imported (specifying Entity Top) into the power analyzer. The resulting power analysis uses all the signal activities information from the generated Value Change Dump File or Signal Activity File, including those that apply to submodules such as `decode[1-3]`, `err1`, `mux1`, and `encode1`.

Modular Design Simulation

You can simulate submodules of the design Top independently, and then import all of the resulting signal activity files into the Power Analyzer. For example, you may simulate the `8b10b_dec` independent of the entire design, as well as mux, `8b10b_rxerr`, and `8b10b_enc`. You can then import the Value Change Dump File or Signal Activity File generated from each simulation by specifying the appropriate instance name. For example, if the files produced by the simulations are **8b10b_dec.vcd**, **8b10b_enc.vcd**, **8b10b_rxerr.vcd**, and **mux.saf**, the import specifications in Table 10–2 would be used:

Table 10–2. Import Specifications

File Name	Entity
8b10b_dec.vcd	`Top|8b10b_dec:decode1`
8b10b_dec.vcd	`Top|8b10b_dec:decode2`
8b10b_dec.vcd	`Top|8b10b_dec:decode3`
8b10b_rxerr.vcd	`Top|8b10b_rxerr:err1`
8b10b_enc.vcd	`Top|8b10b_enc:encode1`
mux.saf	`Top|mux:mux1`

The resulting power analysis applies the simulation vectors found in each file to the assigned entity. Simulation provides signal activities for the pins and for the outputs of functional blocks. Unless the inputs to an entity instance are input pins for the entire design, the simulation file associated with that instance does not provide signal activities for the inputs of that instance. For example, an input to an entity such as `mux1` has its signal activity specified at the output of one of the decode entities.

Multiple Simulations on the Same Entity

You can perform multiple simulations of an entire design or specific modules of a design. For example, in the process of verifying the Top design, you may have three different simulation test benches: one for normal operation, and two for corner cases. Each of these simulations produces a separate Value Change Dump File or Signal Activity File. In this case, apply the different Value Change Dump File or Signal Activity File names to the same top-level entity (Table 10–3).

Table 10–3. Multiple Simulation File Names & Entities

File Name	Entity
normal.saf	`Top`
corner1.vcd	`Top`
corner2.vcd	`Top`

The resulting power analysis uses an arithmetic average of the signal activities calculated from each simulation file to obtain the final signal activities used. Thus, if a signal `err_out` has a toggle rate of 0 toggles per second in **normal.saf**, 50 toggles per second in **corner1.vcd**, and 70 toggles per second in **corner2.vcd**, the final toggle rate that is used in the power analysis is 40 toggles per second.

Overlapping Simulations

You can perform a simulation on the entire design Top and more exhaustive simulations on a submodule such as `8b10b_rxerr`. Table 10–4 shows the import specification for overlapping simulations.

Table 10–4. Overlapping Simulation Import Specifications

File Name	Entity
full_design.vcd	`Top`
error_cases.vcd	`Top|8b10b_rxerr:err1`

In this case, signal activities from **error_cases.vcd** are used for all of the nodes in the generated signal activity file, and signal activities from **full_design.vcd** are used for only those nodes that do not overlap with nodes in **error_cases.vcd**. In general, the more specific hierarchy (the most bottom-level module) is used to derive signal activities for overlapping nodes.

Partial Simulations

You can perform a simulation where the entire simulation time is not applicable to signal activity calculation. For example, suppose you run a simulation for 10,000 clock cycles and you reset the chip for the first 2,000 clock cycles. If the signal activity calculation is performed over all 10,000 cycles, the toggle rates are typically only 80% of their steady state value (since the chip is in reset for the first 20% of the simulation). In this case, you should specify the useful parts of Value Change Dump File for the purpose of power analysis. The Limit VCD Period option enables you to specify a start and end time to be used when performing signal activity calculations.

Node Name Matching Considerations

Node name mismatches happen when you have Signal Activity Files or Value Change Dump Files applied to entities other than the top-level entity. In a modular design flow, the gate-level simulation files created in different Quartus II software projects may not match their node names properly with the current Quartus II project.

For example, if you have a file named **8b10b_enc.vcd**, which was generated in a separate project called **8b10b_enc** and is simulating the `8b10b` encoder, and you import that Value Change Dump File into another project called **Top**, you may encounter name mismatches when applying the Value Change Dump File to the `8b10b_enc` module in the **Top** project. This is because all of the combinational nodes in the **8b10b_enc.vcd** file may be named differently in the **Top** project.

You can avoid name mismatching by using only register transfer level (RTL) simulation data, where register names usually don't change, or by using an incremental compile flow that preserves node names in conjunction with a gate-level simulation. To ensure the best accuracy, Altera recommends using an incremental compile flow to preserve your design's node names.

For more information on the incremental compile flow, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

Glitch Filtering

The Power Analyzer defines a glitch as two signal transitions that are so closely spaced in time that the pulse, or glitch, occurs faster than the logic and routing circuitry can respond. The output of a transport delay model simulator (the default mode of the Quartus II simulator) generally

contains glitches for some signals. The device's logic and routing structures form a low-pass filter that filters out glitches that are tens to hundreds of picoseconds long, depending on the device family.

Some third-party simulators use different simulator models than the transport delay model as default. Different models cause differences in signal activity estimation and power estimation. The inertial delay model, which is the ModelSim default model, filters out many more glitches than the transport delay model; therefore, it usually yields a lower power estimate. Altera recommends using the transport simulation model when using the Quartus II glitch filtering support with third-party simulators. If the inertial simulation model is used, simulation glitch filtering has little effect.

For more information on how to set the simulation model type for your specific simulator, refer to the Quartus II Help.

Glitch filtering in a simulator can also filter a glitch on one LE (or other circuit element) output from propagating to downstream circuit elements so that the glitch will not affect simulated results. This prevents a glitch on one signal from producing non-physical glitches on all downstream logic, which would result in a signal toggle rate that is too high and a power estimate that is too high. Circuit elements in which every input transition produces an output transition, including multipliers and logic cells configured to implement XOR functions, are especially prone to glitches. Hence, circuits with many such functions can have power estimates that are too high when glitch filtering is not used.

Altera recommends that the glitch filtering feature be used to obtain the most accurate power estimates. For third-party simulators, the Power Analyzer flows support two types of glitch filtering, both of which are recommended for power estimation. In the first, glitches are filtered during simulation. To enable this level of glitch filtering in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulation**. The **Simulation** page is shown.
3. Turn on the **Enable glitch filtering** option.

The second level of glitch filtering occurs while the Power Analyzer is reading the Value Change Dump File generated by the third-party simulator. Enable this level of glitch filtering by performing the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **PowerPlay Power Analyzer Settings**. The **PowerPlay Power Analyzer Settings** page is shown.
3. Under **Input File(s)**, turn on the **Perform glitch filtering on VCD files** option.

Altera recommends that you use both forms of glitch filtering.

The Value Change Dump File reader performs complementary filtering to the filtering performed during simulation, and is often not as effective. While the Value Change Dump File reader can remove glitches on logic blocks, it has no way of determining how downstream logic and routing are affected by a given glitch, and may not eliminate the impact of the glitch completely. Filtering the glitches during simulation avoids switching downstream routing and logic automatically. See Table 10–5 for simulator support.

When running simulation for design verification (rather than to produce input to the Quartus PowerPlay Power Analyzer), Altera recommends leaving glitch filtering turned off. This produces the most rigorous and conservative simulation from a functionality viewpoint. When performing simulation in order to produce input for the Quartus II PowerPlay Power Analyzer, Altera recommends turning on glitch filtering to produce the most accurate power estimates.

Table 10–5. Simulator Support for Glitch Filtering

Simulators	Glitch Filtering Support *(1)*
Quartus II simulator	During simulation
Third Party simulators	During simulation and reading Value Change Dump Files

Note to Table 10–5:
(1) Glitch filtering only for Stratix II, Stratix II GX, Stratix, Stratix GX, Cyclone II, Cyclone, HardCopy II, and MAX II device families.

Node & Entity Assignments

You can assign specific toggle rates and static probabilities to individual nodes and entities in the design. These assignments have the highest priority, overriding data from all other signal activity sources.

Use the Assignment Editor or tool command language (Tcl) commands to make "Power Toggle Rate" and "Power Static Probability" assignments.

For more information about how to use the assignment editor in the Quartus II software, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

This method is appropriate for special-case signals where you have specific knowledge of the signal or entity being analyzed. For example, if you know that a 100-MHz data bus or memory output produces data that is essentially random (uncorrelated in time), you can directly enter a 0.5 static probability and a toggle rate of 50 million transitions per second.

Bidirectional I/O pins are treated specially. The combinational input port and the output pad for a given pin share the same name. However, those ports might not share the same signal activities. For the purpose of reading signal activity assignments, the Power Analyzer creates a distinct name `<node_name~output>` when the bidirectional signal is configured as an output and `<node_name~result>` when the signal is configured as an input. For example, if a design has a bidirectional pin named `MYPIN`, assignments for the combinational input use the name `MYPIN~result`, and the assignments for the output pad use the name `MYPIN~output`.

Timing Assignments to Clock Nodes

For clock nodes, the Power Analyzer uses the timing requirements to derive the toggle rate when neither simulation data nor user entered signal activity data is available.

f_{MAX} requirements specify full cycles per second, but each cycle represents a rising transition and a falling transition. For example, a clock f_{MAX} requirement of 100 MHz corresponds to 200 million transitions per second.

Default Toggle Rate Assignment

You can specify a default toggle rate for primary inputs and all other nodes in the design. The default toggle rate is used when no other method has specified the signal activity data.

The toggle rate can be specified in absolute terms (transitions per second) or as a fraction of the clock rate in effect for each particular node. The toggle rate for a given clock is derived from the timing settings for the clock. For example, if a clock is specified with an f_{MAX} constraint of 100 MHz and a default relative toggle rate of 20%, nodes in this clock domain transition in 20% of the clock periods, or 20 million transitions

occur per second. In some cases, the Power Analyzer cannot determine the clock domain for a given node because there is either no clock domain for the node or it is ambiguous. In these cases, the Power Analyzer substitutes and reports a toggle rate of zero.

Vectorless Estimation

For some device families, the Power Analyzer automatically derives estimates for signal activity on nodes with no simulation or user-entered signal-activity data. Vectorless estimation is available and enabled by default for Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II device families. Vectorless estimation statistically estimates the signal activity of a node based on the signal activities of all nodes feeding that node, and on the actual logic function that is implemented by the node. The PowerPlay Power Analyzer **Settings** dialog box lets you disable vectorless estimation. When enabled, vectorless estimation takes priority over default toggle rates. Vectorless estimation does not override clock assignments.

Vectorless estimation cannot derive signal activities for primary inputs. Vectorless estimation is generally accurate for combinational nodes, but not for registered nodes. Therefore, simulation data for at least the registered nodes and I/O nodes is needed for good accuracy.

Using the PowerPlay Power Analyzer

For all flows that use the PowerPlay Power Analyzer, synthesize your design first and then fit it to the target device. You must either provide timing assignments for all clocks in the design or use a simulation-based flow to generate activity data. The I/O standard used on each device input or output and the capacitive load on each output must be specified in the design.

Common Analysis Flows

You can use the analysis flows in this section with the PowerPlay Power Analyzer. However, vectorless activity estimation is only available for some device families.

Signal Activities from Full Post-Fit Netlist (Timing) Simulation

This flow provides the highest accuracy because all node activities reflect actual design behavior, provided that supplied input vectors are representative of typical design operation. Results are better if the simulation filtered glitches. The disadvantage with this method is that simulation times can be long.

Signal Activities from RTL (Functional) Simulation, Supplemented by Vectorless Estimation

In this flow, simulation provides toggle rates and static probabilities for all pins and registers in the design. Vectorless estimation fills in the values for all the combinational nodes between pins and registers. This method yields good results, since vectorless estimation is accurate, given that the proper pin and register data is provided. This flow usually provides a compilation time benefit to the user in the third-party RTL Simulator.

RTL simulation may not provide signal activities for all registers in the post-fitting netlist because some register names may be lost during synthesis. For example, synthesis may automatically transform state machines and counters, thus changing the names of registers in those structures.

Signal Activities from Vectorless Estimation, User-Supplied Input Pin Activities

This option provides a low level of accuracy, because vectorless estimation for registers is not entirely accurate.

Signal Activities From User Defaults Only

This option provides the lowest degree of accuracy.

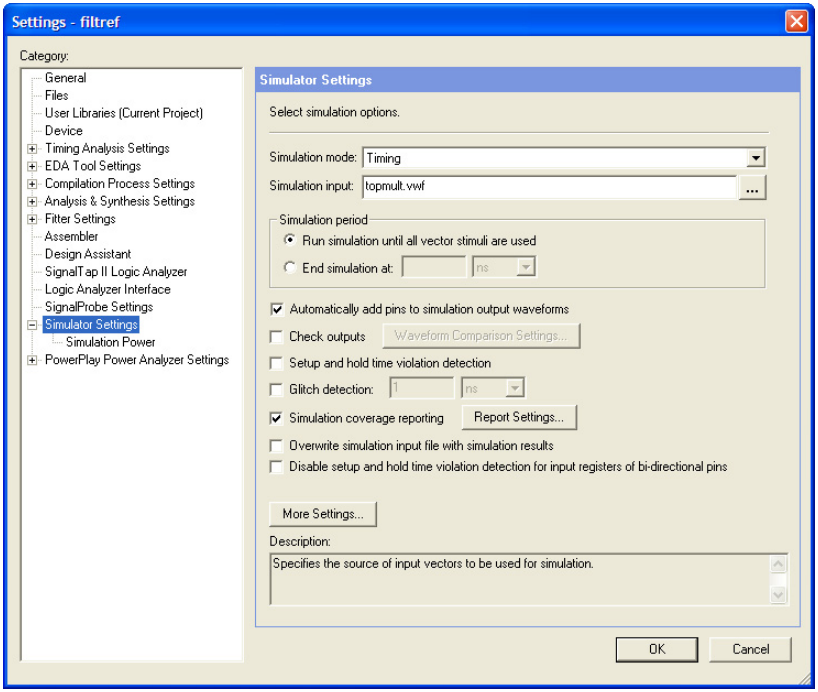
Generating a Signal Activity File Using the Quartus II Simulator

While performing a timing or functional simulation using the Quartus II Simulator, you can generate a Signal Activity File. This file stores the toggle rate and static probability for each connected output signal based on the simulation vectors that are entered in the Vector Waveform File (**.vwf**) or the Vector File (**.vec**). You can use the Signal Activity File(s) as input to the PowerPlay Power Analyzer to estimate power for your design.

To create a Signal Activity File for your design, perform the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **Simulator Settings**. The **Simulator Settings** page is shown (Figure 10–9).

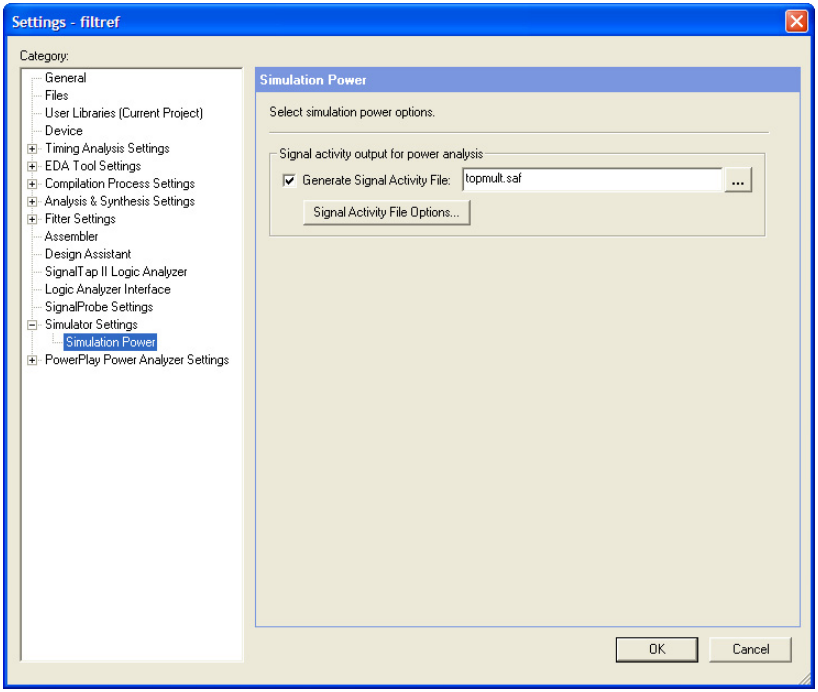
Figure 10–9. Simulator Settings



3. In the **Simulation mode** list, select either **Timing** or **Functional**. Refer to "Common Analysis Flows" on page 10–21 for a description of the difference in accuracy between the two types of simulation modes.

4. In the **Category** list, select **Simulation Power** by selecting **Simulator Settings** (Figure 10–10).

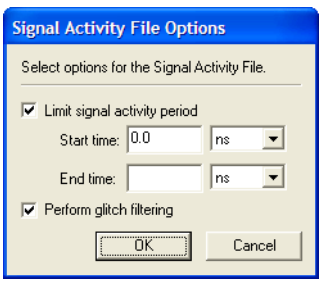
Figure 10–10. Simulator Power Page of the Settings Dialog Box



5. Turn on **Generate Signal Activity File** and enter the file name for the Signal Activity File.

6. (Optional) Click **Signal Activity File Options**. The **Signal Activity File Options** dialog box appears (Figure 10–11).

Figure 10–11. Signal Activity File Options Dialog Box



7. (Optional) Turn on the **Limit signal activity period** option to specify the simulation period to use when calculating the signal activities.

   Power estimation can be performed for the entire simulation time or for a portion of the simulation time. This allows you to look at the power consumption at different points in your overall simulation without having to rework your test benches. This feature is also useful when multiple clock cycles are necessary to initialize the state of the design, but you want to measure the signal activity only during the normal operation of the design, not during its initialization phase. You can specify the start time and end time in the **Signal Activity File Options** dialog box by turning on the **Limit signal activity period** option. Simulation information is used during this time interval only to calculate toggle rates and static probabilities. If no time interval is specified, the whole simulation is used to compute signal activity data.

8. (Optional) In the **Signal Activity File Options** dialog box, turn on **Perform glitch filtering**. For more information on glitch filtering, refer to "Glitch Filtering" on page 10–17.

9. After the simulation is complete, a Signal Activity File is generated with the specified filename and stored in the main project directory.

For more information about how to perform simulations in the Quartus II software, see the Quartus II Help.

Generating a Value Change Dump File Using a Third-Party Simulator

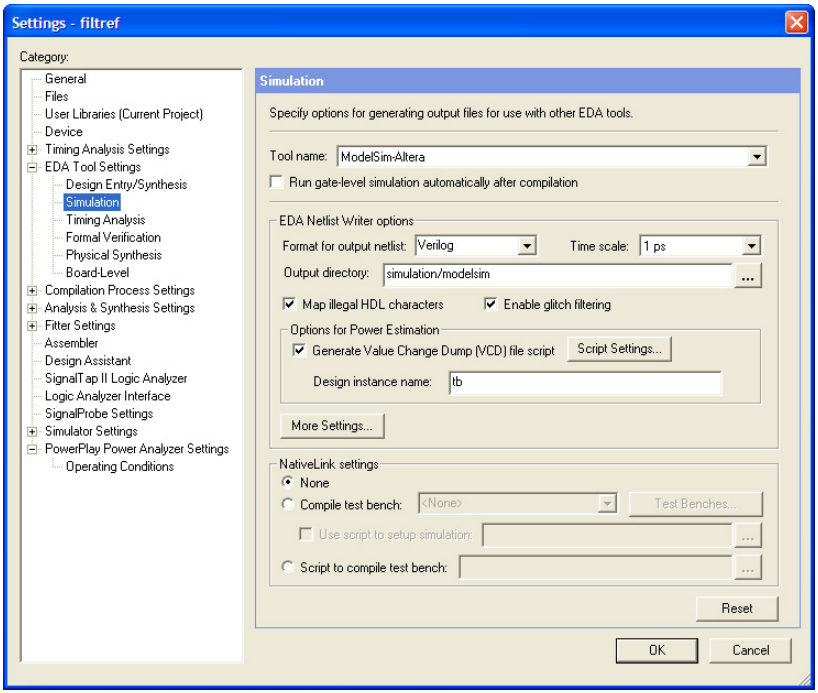
You can use other EDA simulation tools, such as the Model Technology™ ModelSim software, to perform a simulation and create a Value Change Dump File. You can use this file as input to the PowerPlay Power Analyzer to estimate power for your design. To do this, you must tell the Quartus II software to generate a script file that is used as input to the third-party simulator. This script tells the third-party simulator to generate a Value Change Dump File that contains all the output signals. For more information on the supported third-party simulators, refer to the "Simulation Results" on page 10–12.

To create a Value Change Dump File for your design, perform the following steps:

1. On the Assignments menu, click **EDA Tool Settings**. The **Settings** dialog box appears.

2. In the **Category** list, select **Simulation**. The **Simulation** page is shown (Figure 10–12).

Figure 10–12. EDA Tool Simulation Setting Window



3. In the **Tool name** list, select the appropriate EDA simulation tool.

4. In the **Format for output netlist** list, select **VHDL** or **Verilog**.

5. Turn on **Generate Value Change Dump (VCD) file script**.

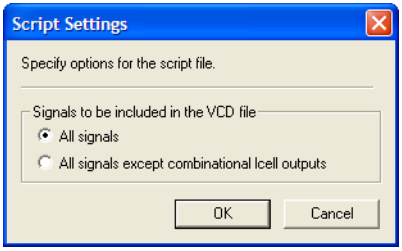
By default, the **Map illegal HDL character** and **Enable glitch filtering** options will be turned on.

6. (Optional) **Map illegal HDL character** ensures that all signals have legal names and that signal toggle rates are available later in the PowerPlay Power Analyzer.

7. (Optional) By turning on **Enable glitch filtering**, glitch filtering logic is the output when you generate an EDA netlist for simulation. This option is always available, regardless of whether or not you want to generate the Value Change Dump File scripts. For more information on glitch filtering, refer to "Glitch Filtering" on page 10–17.

8. Click **Script Settings**. The **Script Settings** dialog box appears (Figure 10–13).

Figure 10–13. Script Settings Dialog Box



Select which signals should be output to the Value Change Dump File. With **All signals** selected, the generated script instructs the third-party simulator to write all connected output signals to the Value Change Dump File. With **All signals except combinational lcell outputs** selected, the generated script tells the third-party simulator to write all connected output signals to the Value Change Dump File, except logic cell combinational outputs. You may not want to write all output signals to the file because the file can become extremely large (since its size depends on the number of output signals being monitored and the number of transitions that occur).

9. Click **OK**.

10. Type a name for your test bench in the **Design instance name** box.

11. Compile your design with the Quartus II software and generate the necessary EDA netlist and script that tells the third-party simulator to generate a Value Change Dump File.

For more information on NativeLink use, refer to *Section I. Design Flows* in volume 3 of the *Quartus II Handbook*.

12. Perform a simulation with the third-party EDA simulation tool. Call the generated script in the simulation tool before running the simulation. The simulation tool generates the Value Change Dump File and places it in the project directory.

For more information on how to call the Value Change Dump File generation script in the respective third-party EDA simulation tools, refer to the Quartus II Help. For more information about how to perform simulations in other EDA simulation tools, see the relevant documentation for that tool.

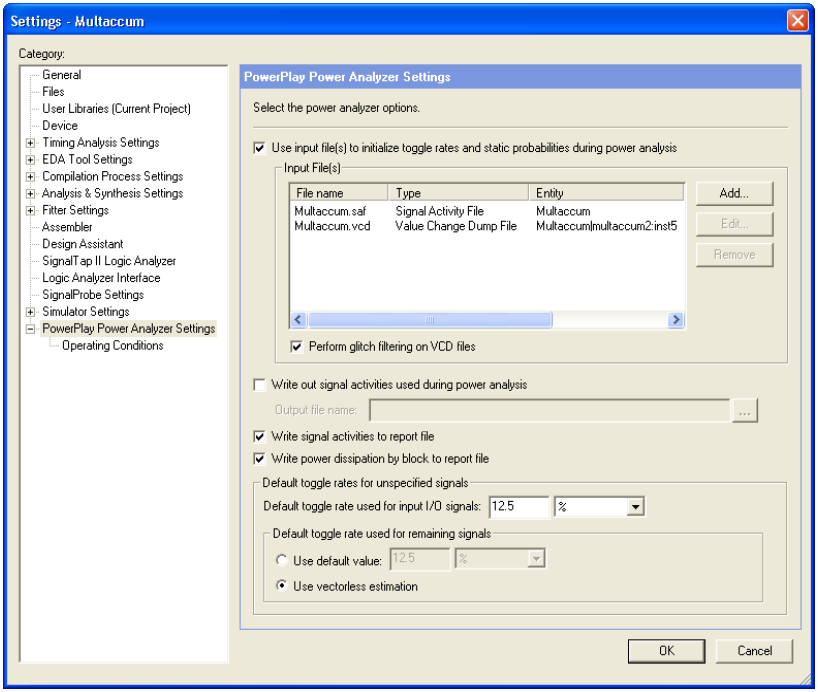
Running the PowerPlay Power Analyzer Using the Quartus II GUI

To run the PowerPlay Power Analyzer using the Quartus II GUI, perform the following steps:

1. In the Assignments menu, click **Settings**. The **Settings** dialog box appears.

2. In the **Category** list, select **PowerPlay Power Analyzer Settings** (Figure 10–14).

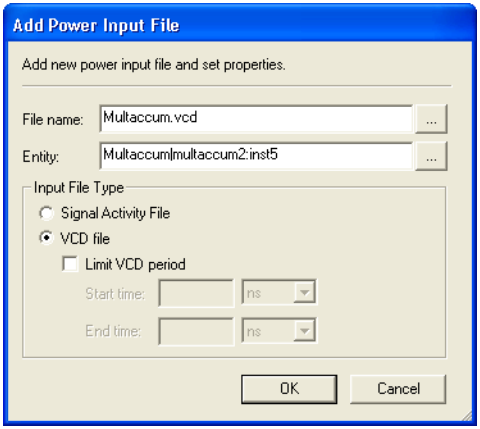
Figure 10–14. PowerPlay Power Analyzer Settings



3. (Optional) If you want to use either Signal Activity File(s) or Value Change Dump File(s) or both as an input to the PowerPlay Power Analyzer, turn on **Use input file(s) to initialize toggle rates and static probabilities during power analysis**.

4. Click **Add**. The **Add Power Input File** dialog box appears (Figure 10–15).

Figure 10–15. Add Power Input File Dialog Box



5. Add your Signal Activity File(s) or Value Change Dump File(s) file by clicking on browse button (**...**) for the **File name** box.

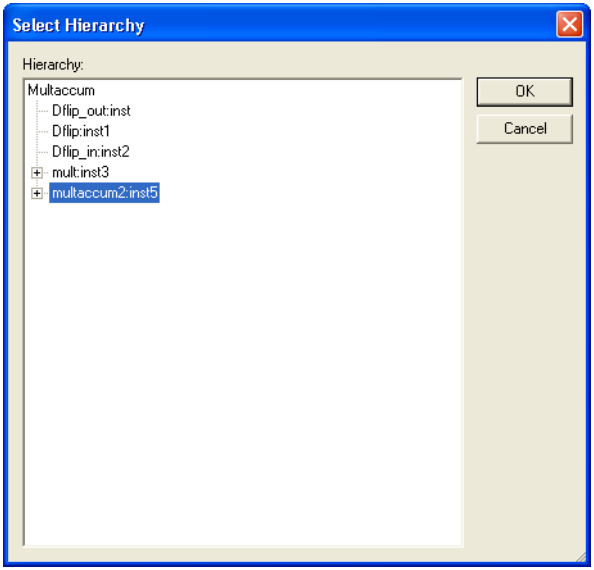
   (Optional) The **Edit** button enables you to change the settings for the selected file from the list. The **Remove** button enables you to remove a selected file from the list.

6. You can specify whether the input file is a VCD File or Signal Activity File under **Input File Type**.

7. (Optional) **Limit VCD period** is enabled only when the **VCD file** is selected. This enables you to specify the simulation period to use when calculating the signal activities. For more information, refer to step 6 of "Generating a Signal Activity File Using the Quartus II Simulator" on page 10–22.

8. The **Entity** box enables you to specify the design entity (hierarchy) to which the entered signal activity file applies. To enter the entity, you can type in the box or by browse through the list of your design entities. To browse your design entities, click the browse button (**...**). The **Select Hierarchy** dialog box appears (Figure 10–16). You can specify multiple entities in the entity text box by using comma delimiters.

Figure 10–16. Select Hierarchy Dialog Box



9. Click **OK**.

10. Click **OK**.

11. (Optional) Turn on **Perform glitch filtering on VCD files**. This option is recommended. For more information, refer to "Glitch Filtering" on page 10–17.

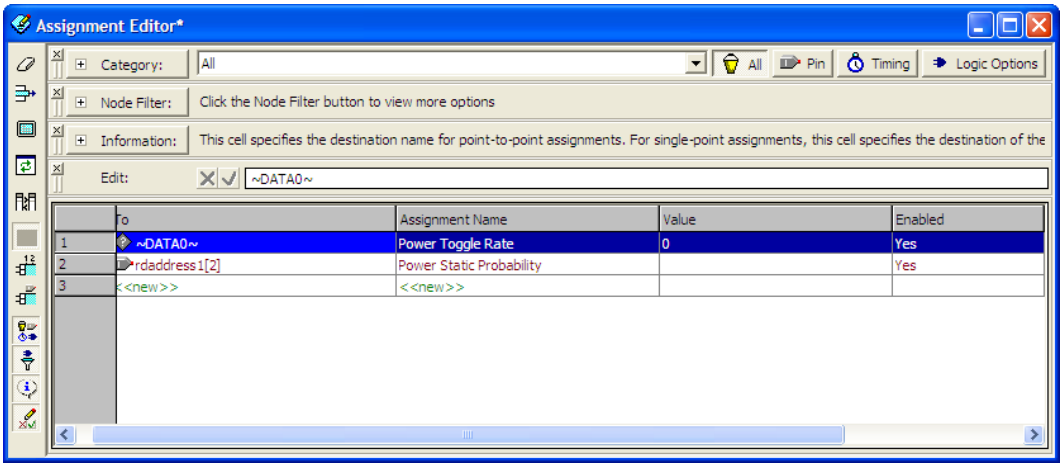
12. (Optional) Turn on **Write out signal activities used during power analysis**. In the **Output file name** list, select the output file name. This file contains all the signal activities information used during the power estimation of your design. This is recommended if you used a Value Change Dump File as input into the PowerPlay Power Analyzer, because it reduces the run time of any subsequent power estimation. You can use the generated Signal Activity File as input instead of the original Value Change Dump File.

13. (Optional) Turn on **Write signal activities to report file**.

14. (Optional) Turn on **Write power dissipation by block to report file** to enable the output of detailed thermal power dissipation by block to be included in the PowerPlay Power Analyzer report.

15. (Optional) You can also use the Assignment Editor to enter the Power Toggle Rate and Power Static Probability for a node or entity in your design (Figure 10–17).

Figure 10–17. Assignment Editor *Notes (1), (2)*



Notes to Figure 10–17:

(1) The assignments made with the Assignment Editor override the values already existing in the Signal Activity File or Value Change Dump File.

(2) You can also use Tcl script commands to make these assignments.

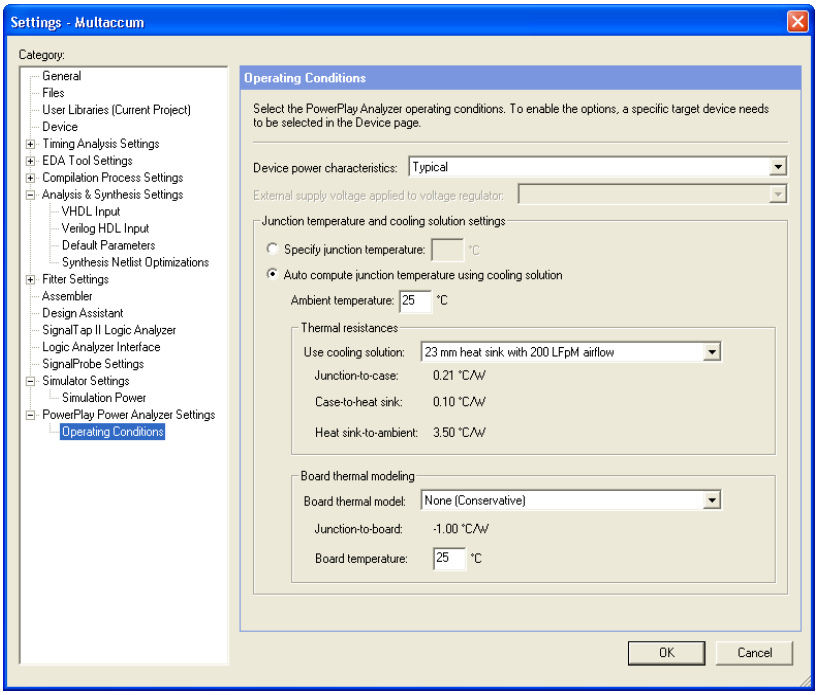
For more information about how to use the assignment editor in the Quartus II software, see the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*. For information on scripting, see the *Scripting* chapter in volume 2 of the *Quartus II Handbook*.

16. Specify the toggle rate in the **Default toggle rate used for input I/O signals** field. This toggle rate is used for all unspecified input I/O signal toggle rates regardless of whether or not the device family supports vectorless estimation. By default, its value is set to 12.5%. The default static probability for unspecified input I/O signals is 0.5 and cannot be changed.

17. Select either **Use default value** or **Use vectorless estimation** for Stratix II, Stratix II GX, Cyclone II, HardCopy II, or MAX II device families. For all other device families, only **Use default value** is available. This setting controls how the remainder of the unspecified signal activities are calculated. For more information, refer to the "Vectorless Estimation" on page 10–21 and "Default Toggle Rate Assignment" on page 10–20.

18. In the **Category** list, click the **+** icon to expand **PowerPlay Power Analyzer Settings** and select **Operating Conditions**. This option is available only for the Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II device families (Figure 10–18).

Figure 10–18. Operating Conditions



19. In the **Device power characteristics** list, select **Typical** or **Maximum**. The default is **Typical**.

20. Specify the junction temperature and cooling solution settings. You can select **Specify junction temperature** or **Auto compute junction temperature using cooling solution**.

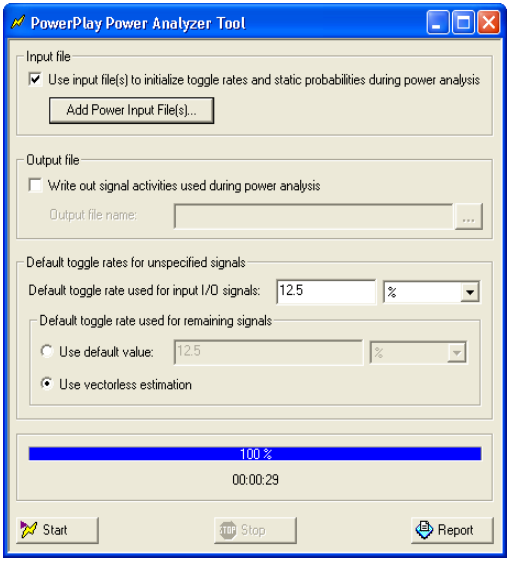
21. (Optional) Under **Board thermal modeling**, select the **Board thermal model** and type the **Board temperature**. This feature can only be turned on when you have selected **Auto compute junction temperature using cooling solution**.

    For more information on how to use the operating condition settings, refer to "Operating Conditions" on page 10–10.

22. Click **OK** to close the **Settings** dialog box.

23. On the Processing menu, click **PowerPlay Power Analyzer Tool**. The **PowerPlay Power Analyzer Tool** dialog box appears (Figure 10–19).

Figure 10–19. PowerPlay Power Analyzer Tool Dialog Box

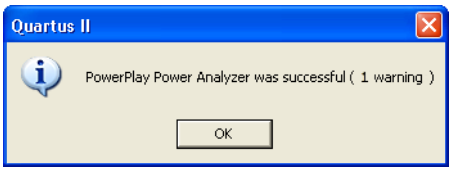


24. Click **Start** to run the PowerPlay Power Analyzer. Be sure that all the settings are correct.

You can also make changes to some of your settings in this dialog box. For example, you can click the **Add Power Input File(s)** button to make changes to your input file(s).

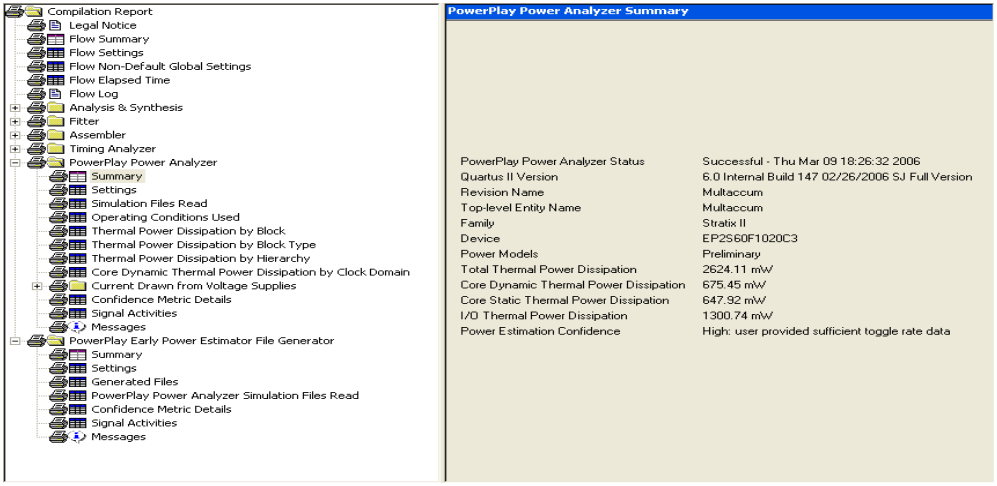
25. After the PowerPlay Power Analyzer successfully runs, a message appears (Figure 10–20).

Figure 10–20. PowerPlay Power Analyzer Message



26. In the **PowerPlay Power Analyzer Tool** dialog box, click **Report** to open the PowerPlay Power Analyzer Summary window. You can also view the summary in the **PowerPlay Power Analyzer Summary** page of the **Compilation Report** dialog box (Figure 10–21).

Figure 10–21. PowerPlay Power Analyzer Summary



PowerPlay Power Analyzer Compilation Report

The PowerPlay Power Analyzer section of Compilation Report is divided into the following sections.

Summary

This section of the report shows your design's estimated total thermal power consumption. This includes dynamic, static, and I/O thermal power consumption. The report also includes a confidence metric that reflects the overall quality of the data sources for the signal activities.

Settings

This section of the report shows your design's PowerPlay Power Analyzer settings information. This includes default input toggle rates, operating conditions and other relevant setting information.

Simulation Files Read

This section of the report lists simulation output files (Value Change Dump File or Signal Activity File) used for power estimation.

Operating Conditions Used

This section shows device characteristics, voltages, and cooling solution, if any, that were used during the power estimation. It also shows the entered junction temperature or auto-computed junction temperature that was used during the power analysis. This page is created only for Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II device families.

Thermal Power Dissipated by Block

This section shows estimated thermal dynamic power and thermal static power consumption categorized by atoms. This is very useful as this information provides designers with an estimated power consumption for each atom in their design.

Thermal Power Dissipation by Block Type (Device Resource Type)

This section shows the estimated thermal dynamic power and thermal static power consumption categorized by block types. This information is further categorized by estimated dynamic and static power that was used, as well as providing an average toggle rate by block type. Thermal power is the power dissipated as heat from the FPGA device.

Thermal Power Dissipation by Hierarchy

This section shows an estimated thermal dynamic power and thermal static power consumption categorized by design hierarchy. This is further categorized by the dynamic and static power that was used by the blocks and routing within that hierarchy. This information is very useful in locating problem modules in your design.

Core Dynamic Thermal Power Dissipation by Clock Domain

This section shows the estimated total core dynamic power dissipation by each clock domain. This provides designs with estimated power consumption for each clock domain in their design. If the clock frequency for some domain is unspecified by a constraint, the clock frequency is listed as "unspecified." For all the combinational logic, the clock domain is listed as no clock with 0 MHz.

Current Drawn From Voltage Supplies

This section lists the current that was drawn from each voltage supply. The V_{CCIO} voltage supply is further categorized by I/O bank and by voltage. The minimum safe power supply size (current supply ability) is also listed for each supply voltage. This page is created only for Stratix II, Stratix II GX, Cyclone II, HardCopy II, and MAX II device families.

Confidence Metric Details

The confidence metric indicates the quality of the signal toggle rate data used to compute a power estimate. If the signal toggle rate data comes from sources that are considered poor predictors of real signal toggle rates in the device during in operation, then the confidence metric will be low. Toggle rate data that comes from simulation, or user-entered assignments on specific signals, or entities are considered reliable. Toggle rate data from default toggle rates (for example, 12.5% of the clock period) or vectorless estimation are considered relatively inaccurate. This section gives an overall confidence rating in the toggle rate data, from low to high. It also summarizes how many pins, registers, and combinational nodes obtained their toggle rates from each of simulation, user entry, vectorless estimation, or default toggle rate estimations. This detailed information can let you understand how to increase the confidence metric, letting you decide on your own confidence in the toggle rate data.

Signal Activities

This section lists toggle rate and static probabilities assumed by power analysis for all signals with fan-out and pins. The signal type is provided (Pin, Registered, or Combinational), as well as the data source for the

toggle rate and static probability. By default, all signal activities are reported. This may be turned off on the Power Analyzer settings page by turning off the **Write signal activities to report file** option. Turning this option off may be advisable for a large design because of the large number of signals present. You can use the Assignment Editor to specify that activities for individual nodes or entities are reported by assigning an on value to those nodes for the Power Report Signal Activities assignment.

Messages

This section lists any messages generated by the Quartus II software during the analysis.

Specific Rules for Reporting

In the Stratix GX device, the XGM II State Machine block is always used together with GXB transceivers, so its power is lumped into the power for the transceivers. Therefore, the power for the XGM II State Machine block is reported as 0 Watts.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp
```

The *Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Running the PowerPlay Power Analyzer from the Command Line

The separate executable that can be used to run the PowerPlay Power Analyzer is **quartus_pow**. For a complete listing of all command line options supported by **quartus_pow**, type the following at a system command prompt:

```
quartus_pow --help or quartus_sh --qhelp ↵
```

Example of using the `quartus_pow` executable with project **sample.qpf**:

- To instruct the PowerPlay Power Analyzer to generate a PowerPlay Early Power Estimator file, type the following at a system command prompt:

```
quartus_pow  sample  --output_epe=sample.csv ↵
```

- To instruct the PowerPlay Power Analyzer to generate a PowerPlay Early Power Estimator file without doing the power estimate, type the following command at a system command prompt:

```
quartus_pow sample --output_epe=sample.csv --estimate_power=off ↵
```

- To instruct the PowerPlay Power Analyzer to use a Signal Activity File as input (**sample.saf**), type the following at a system command prompt:

```
quartus_pow sample --input_saf=sample.saf ↵
```

- To instruct the PowerPlay Power Analyzer to use two Value Change Dump Files as input (**sample1.vcd** and **sample2.vcd**), perform glitch filtering on the Value Change Dump File, and to use a default input I/O toggle rate of 10,000 transitions/second, type the following at a system command prompt:

```
quartus_pow sample --input_vcd=sample1.vcd
--input_vcd=sample2.vcd --vcd_filter_glitches=on
--default_input_io_toggle_rate=10000transitions/s ↵
```

- To instruct the PowerPlay Power Analyzer to not use any input file, a default input I/O toggle rate of 60%, no vectorless estimation, and a default toggle rate of 20% on all remaining signals, type the following at a system command prompt:

```
quartus_pow sample --no_input_file --default_input_io_toggle_rate=60%
--use_vectorless_estimation=off --default_toggle_rate=20% ↵
```

There are no command line options to specify the information found on the PowerPlay Power Analyzer Settings Operating Conditions page. The easiest way to specify these options is to use the Quartus II GUI.

A report file, <*revision name*>**.pow.rpt**, is created by the **quartus_pow** executable and saved in the main project directory. The report file contains the same information as described in the "PowerPlay Power Analyzer Compilation Report" on page 10–35.

Conclusion

PowerPlay power analysis tools are designed for accurate estimation of power consumption from early design concept through design implementation. Designers can use the PowerPlay Early Power Estimator to estimate power consumption during the design concept stage. Power estimations can be refined during design implementation using the Quartus II PowerPlay Power Analyzer feature. The Quartus II PowerPlay Power Analyzer produces detailed reports that you can use to optimize designs for lower power consumption and verify that the design is within your power budget.

Section IV. In-System Design Debugging

Debugging today's FPGA designs can be a daunting task. As your product requirements continue to increase in complexity, the time you spend on design verification continues to rise. To get your product to market as quickly as possible, you must minimize design verification time. To help alleviate the time-to-market pressure, you need a set of verification tools that are powerful, yet easy to use.

The Quartus® II software SignalTap® II Logic Analyzer and the SignalProbe™ features analyze internal device nodes and I/O pins while operating in-system and at system speeds. The SignalTap II Logic Analyzer uses an embedded logic analyzer to route the signal data through the JTAG port to either the SignalTap II Logic Analyzer or an external logic analyzer or oscilloscope. The SignalProbe feature uses incremental routing on unused device routing resources to route selected signals to an external logic analyzer or oscilloscope. A third Quartus II software feature, the Chip Editor, can be used in conjunction with the SignalTap II and SignalProbe debugging tools to speed up design verification and incrementally fix bugs uncovered during design verification. This section explains how to use each of these features.

This section includes the following chapters:

Revision History

The table below shows the revision history for Chapters 11 to 15.

Chapter(s)	Date / Version	Changes Made
11	May 2006 v6.0.0	Updated for the Quartus II software version 6.0.0: • Documented new SiginalTap features.
	December 2005 v5.1.1	Added SMART_RECOMPILE assignment.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	• Minor updates for Quartus II software 5.0
	Dec. 2004 v2.1	• Chapter 9 was formerly Chapter 8. • Updates to tables and figures. • New functionality for Quartus II software 4.2.
	June 2004 v2.0	• Updates to tables, figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.
12	May 2006 v6.0.0	Chapter title changed. Updated for the Quartus II software version 6.0.0: • Added the MEX lab function. • Added plug-in information. • Added information on power triggers.
	December 2005 v5.1.1	Added ALTGXB to list of untappable signals.
	October 2005 v5.1.0	Updated for the Quartus II software version 5.1.
	May 2005 v5.0.0	• Updates to tables and figures for Quartus II software 5.0. • New functionality for Quartus II software 5.0
	Dec. 2004 v2.1	• Chapter 10 was formerly Chapter 9. • Updates to tables and figures. • New functionality for Quartus II software 4.2.
	June 2004 v2.0	• Updates to tables and figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.
13	May 2006 v6.0.0	Chapter title changed. Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	Initial release.

Chapter(s)	Date / Version	Changes Made
14	May 2006 v6.0.0	Chapter title changed. Updated for the Quartus II software version 6.0.0: • Updated Chip Editor Chip View Update, • Added information about the Resource Property Editor Update. • Updated the Change Manager section.
	December 2005 v5.1.1	• Minor typographic update.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 12 was formerly Chapter 11 in version 5.0.
	May 2005 v5.0.0	• Updated information. • Updated figures. • Removed figures and tables. • New functionality for Quartus II software 5.0.
	Jan. 2005 v2.2	Change Manager section update
	Dec. 2004 v2.1	• Chapter 11 was formerly Chapter 10. • New figures added. • Reorganized the chapter and updated information and figures. • New functionality for Quartus II software 4.2.
	June 2004 v2.0	• Updates to tables and figures. • New functionality for Quartus II software 4.1.
	Feb. 2004 v1.0	Initial release.
15	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 13 was formerly Chapter 12 in version 5.0.
	May 2005 v5.0.0	• Chapter 12 was formerly in Section V of Vol 3 in 4.2.
	Dec. 2004 v1.2	• Chapter 12 was formerly Chapter 11. • Updated tables. • Corrected the Verilog code for the `lpm_hint` parameter. • Re-organized the “Making Changes” segment into the Editing Data Displayed in the Hex Editor and Importing & Exporting Memory Files segments. Added the Edit value menu. • Added Example: Using the In-System Memory Content Editor with the SignalTap II Embedded Logic Analyzer.
	Aug. 2004 v1.1	Minor typographical corrections.
	June 2004 v1.0	Initial release.

11. Quick Design Debugging Using SignalProbe

QII53008-6.0.0

Introduction

Hardware verification can be a lengthy and expensive process. The SignalProbe™ incremental routing feature helps reduce the hardware verification process and time-to-market for System-On-a-Programmable-Chip (SOPC) designs.

Easy access to internal device signals is important in the debugging of a design. The SignalProbe feature makes design verification more efficient by quickly routing internal signals to I/O pins without affecting the design. Starting with a fully routed design, you can select and route signals for debugging to either previously reserved or currently unused I/O pins.

You can use the SignalProbe feature with the Stratix® series, Cyclone™ series, MAX® II, and APEX™ series device families.

This chapter is divided into two sections. If you are using SignalProbe to debug your Stratix series, Cyclone series, and MAX II device, then refer to "Debugging Using the SignalProbe Feature" on page 11–3. If you are using SignalProbe to debug your APEX series device, refer to "Using SignalProbe with the APEX Device Family" on page 11–14.

On-Chip Debugging Tool Comparison

The Quartus® II software provides a number of different methods to help debug your FPGA design after programming the device. The SignalTap® II Logic Analyzer, SignalProbe, and the External Logic Analyzer Interface share some similar features, but each has its own advantages over the others. In some debugging situations, it might be

difficult to decide which tool is best to use, or whether multiple tools are required. Table 11–1 compares these debugging tools and lists situations and requirements for each one.

Table 11–1. On-Chip Debugging Tools Comparison (Part 1 of 2)

Feature	SignalProbe	External Logic Analyzer Interface (LAI)	SignalTap II Embedded Logic Analyzer
Sample Depth—An external logic analyzer has a bigger buffer to store more captured data than SignalTap II logic analyzer. No data is captured or stored with SignalProbe.	–	✓	–
Ease In Debugging Timing Issues—An external logic analyzer used with the LAI provides access to a "timing" mode, enabling you to debug combined streams of data.	–	✓	–
Performance—The external LAI adds minimal logic to a design, requiring fewer device resources. The SignalTap II logic analyzer has little affect on performance when it is specified as a separate design partition using incremental compilation. SignalProbe incrementally routes nodes to pins, using previously unused routing resources and pins.	✓	✓*(1)*	✓*(2)*
Compile and Recompile Time—SignalProbe attaches incrementally routed signals to previously reserved pins, requiring very little recompilation time to make changes to source signal selections. You can use the SignalTap II logic analyzer and the external LAI to take advantage of incremental compilation to refit design partitions to decrease recompilation time.	✓	✓*(2)*	✓*(2)*
Triggering Capability—Although advanced triggering is available with the SignalTap II logic analyzer, many additional triggering options are available on an external logic analyzer when used with the LAI.	–	✓	–
I/O Usage—No additional output pins are required with the SignalTap II logic analyzer. Both the external LAI and SignalProbe require I/O pin assignments.	–	–	✓
Acquisition Speed—The SignalTap II logic analyzer can acquire data at speeds of over 200 MHz used with the LAI. The same acquisition speeds are obtainable with an external logic analyzer, but signal integrity issues may limit this ability.	–	–	✓
No JTAG Connection Required—An FPGA design with the SignalTap II logic analyzer or LAI requires an active JTAG connection to a host running the Quartus II software. SignalProbe does not require a host for debugging purposes.	✓	–	–

Table 11–1. On-Chip Debugging Tools Comparison (Part 2 of 2)

Feature	SignalProbe	External Logic Analyzer Interface (LAI)	SignalTap II Embedded Logic Analyzer
External Equipment—The SignalTap II logic analyzer is completely internal to the programmed FPGA device, so no extra equipment other than a JTAG connection is required. SignalProbe and the external LAI require the use of external debugging equipment, such as multimeters, oscilloscopes, or logic analyzers.	–	–	✓

Note to Table 11–1:
(1) Like SignalTap II, you need to use QIC with the LAI to get the performance benefit by having the LAI as a separate design partition.
(2) When used with incremental compilation.

Debugging Using the SignalProbe Feature

The SignalProbe feature enables you to reserve available pins and route internal signals to those reserved pins, while preserving the behavior of your design. SignalProbe is an effective debugging tool providing visibility into your FPGA.

This section describes the SignalProbe process for the Stratix series, Cyclone series, and MAX II device families. Using SignalProbe with APEX devices that do not support engineering change orders (ECOs) is described later in this chapter.

Reserving pins for SignalProbe and assigning I/O standards are performed before or after a full compilation. Each SignalProbe source to SignalProbe pin connection is implemented as an ECO change that is applied to your netlist after a full compilation.

To use SignalProbe to perform in-system debugging, perform the following tasks:

1. Reserve SignalProbe pins.
2. Perform a full compilation.
3. Assign a SignalProbe source.
4. Add registers to pipeline the path between the SignalProbe source and pin.
5. Perform a SignalProbe compilation.

6. Analyze the results of the SignalProbe compilation.

7. Generate the programming file.

Reserving SignalProbe Pins

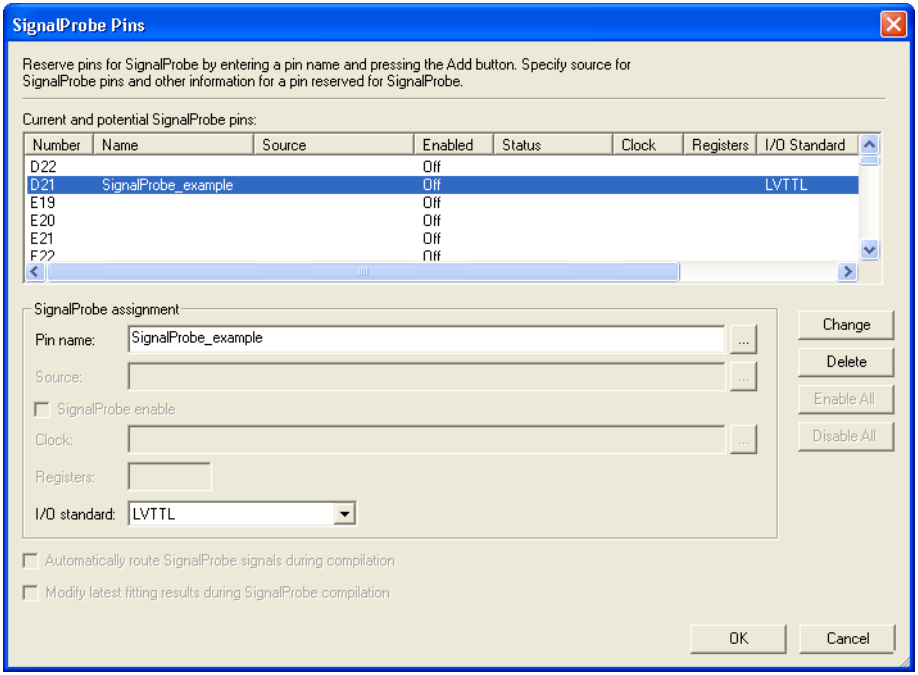
Reserving SignalProbe pins before a compilation is optional because you can reserve any unused I/Os to SignalProbe pins after compilation. You can easily assign sources to probe after reserving your SignalProbe pins.

Although you can reserve SignalProbe pins using many features within the Quartus II software, including the Pin Planner and the Tcl interface, you should use the **SignalProbe Pins** dialog box to create and edit your SignalProbe pins.

To reserve an available package pin as a SignalProbe pin using the **SignalProbe Pins** dialog box, perform the following steps:

1. On the Tools menu, click **SignalProbe Pins**. The **SignalProbe Pins** dialog box appears (Figure 11–1). The SignalProbe pin name and I/O standard appear as the only fields that are editable if a place and route, or fit, has not been performed.

Figure 11–1. Reserving a SignalProbe Pin in the SignalProbe Pins Dialog Box



2. In the **Current and potential SignalProbe pins** list, click on a pin from the **Number** column and type your SignalProbe pin name into the **Pin name** box.
3. Select an I/O standard from the **I/O standard** list.
4. Click **Add** to add the new SignalProbe pin or **Change** if you are editing a previously reserved pin for SignalProbe.
5. Click **OK**.

Perform a Full Compilation

You must complete a full compilation to generate an internal netlist containing a list of internal nodes to probe to a SignalProbe outpin.

To perform a full compilation, on the processing menu, click **Start Compilation**.

Assign a SignalProbe Source

A SignalProbe source can be any combinational node, register, or pin in your post-compilation netlist. To find a SignalProbe source, use the SignalProbe filter in the Node Finder to filter out all sources that cannot be probed. You may not be able to find a particular internal node because the node may be optimized away, or the node is unable to route to the SignalProbe pin. For example, internal nodes and register within the Gigabit transceivers can not be probed because there are no physical routes to the pins available.

To assign a SignalProbe source to your SignalProbe reserved pin, perform the following steps:

1. On the Tools menu, click **SignalProbe Pins**. The **SignalProbe Pins** dialog box appears (Figure 11–1).
2. If a SignalProbe reserved pin is shown, click on the pin in the **Current and potential SignalProbe pins** list. Or you can click on an available pin number in the **Current and potential SignalProbe pins** list and type a new SignalProbe pin name into the **Pin name** box.
3. In the **Source** box, specify the source name. Click the browse button. The **Node Finder** dialog box appears.
4. When you open the **Node Finder** dialog box from the **SignalProbe Pins** dialog box, **SignalProbe** is selected by default in the **Filter** list. Click **List** to show a set of nodes that can be probed in the **Nodes Found** list.
5. Select your source node in the **Nodes Found** list and click the ">" button. The selected node appears in the **Selected Nodes** list.
6. Click **OK**.
7. After a source is selected, the **SignalProbe enable** option is turned on. Click **Change** or **Add** to accept the changes.

Turning the **SignalProbe enable** option on or off is the same as selecting Apply Selected Change or Restore Selected Change in the Change Manager window. Since making SignalProbe connections are ECO changes, you must reapply each SignalProbe pin in the **SignalProbe Pins** dialog box after performing a full fit.

For more information about the Change Manager, refer to the *Design Analysis & Engineering Change Management with Chip Editor* chapter in volume 3 of the *Quartus II Handbook*.

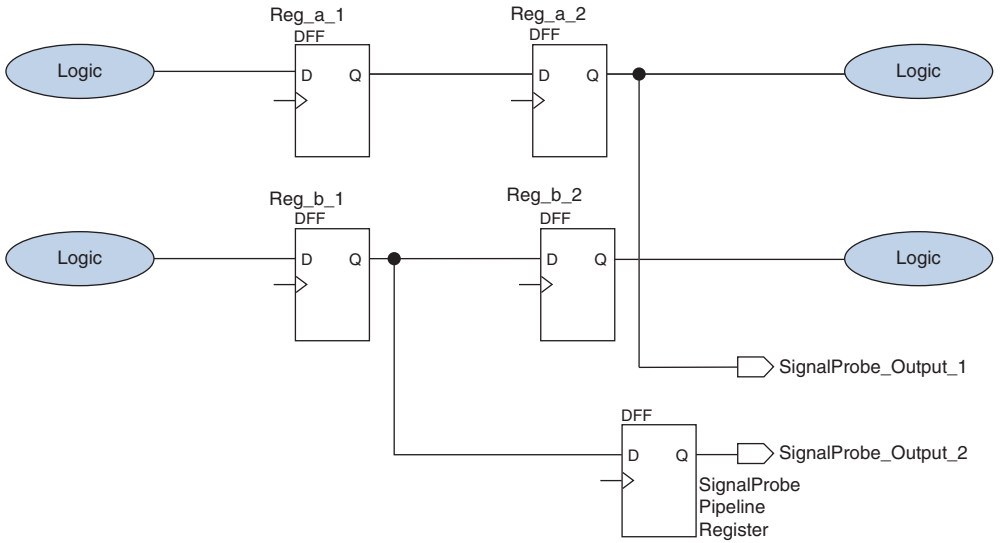
Add Registers to Pipeline Path to SignalProbe Pin

You can specify the number of registers placed between a SignalProbe source and a SignalProbe pin to synchronize the data with a clock and to control the latency of the SignalProbe outputs. The SignalProbe feature automatically inserts the number of registers specified into the SignalProbe path.

Figure 11–2 shows a single register between the SignalProbe source `Reg_b_1` and SignalProbe `SignalProbe_Output_2` output pin added to synchronize the data between the two SignalProbe output pins.

When you add a register to a SignalProbe pin, the SignalProbe compilation attempts to place the register to best fit timing requirements. You can place SignalProbe registers near the SignalProbe source to meet f_{MAX} requirements, or you can place the register near the I/O to meet t_{CO} requirements.

Figure 11–2. Synchronizing SignalProbe Outputs with a SignalProbe Register



To pipeline an existing SignalProbe, perform the following steps:

1. On the Tools menu, click **SignalProbe Pins**. The **SignalProbe Pins** dialog box appears.
2. Select a SignalProbe pin and in the **Clock** box, type the clock name used to drive your registers, or click the browse button to use the Node Finder to select your clock source.
3. In the **Registers** box, specify the number of registers you want to add in between the SignalProbe source and the SignalProbe output.
4. Click **Change.**
5. Click **OK**.

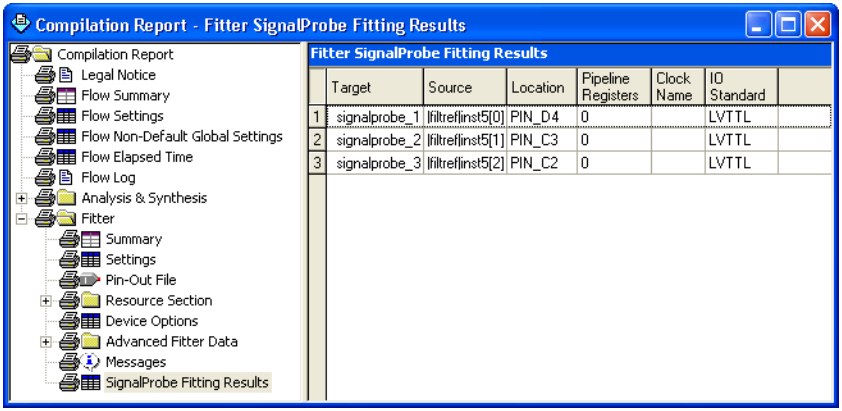
Perform a SignalProbe Compilation

Perform a SignalProbe compilation to route your SignalProbe pins. On the Processing menu, point to Start and click **Start SignalProbe Compilation**. A SignalProbe compilation saves and checks all netlist changes and completes compilation in a fraction of the time of a full compilation because the design's current placement and routing are not touched.

Analyze the Results of the SignalProbe Compilation

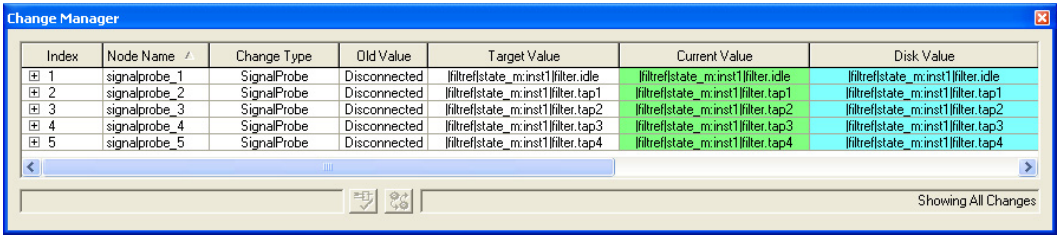
After a SignalProbe compilation, you can view the results in the compilation report file. Each SignalProbe pin is displayed in the SignalProbe Fitting Result page in the Fitter section of the Compilation Report (Figure 11–3). To view the status of each SignalProbe pin in the **SignalProbe Pins** dialog box, click **SignalProbe Pins** on the Tools menu.

Figure 11–3. SignalProbe Fitting Results Page in the Compilation Report Window



You can also view the status of each SignalProbe pin the Change Manager window (Figure 11–4).

Figure 11–4. Change Manager Window with SignalProbe Pins



For more information about how to use the Change Manager, refer to the *Design Analysis & Engineering Change Management with Chip Editor* chapter in volume 3 of the *Quartus II Handbook*.

To view the timing results of each successfully routed SignalProbe pin, on the Processing menu, point to Start and click **Start Timing Analysis**. The clock to output timing results of each pin is located in the t_{CO} page of the Timing Analyzer report.

Generate Programming File

After a SignalProbe compilation, generate the new programming file containing your successfully routed SignalProbe pins. To generate a programming file, on the Processing menu, point to Start and click **Start Assembler**.

Common Questions About the SignalProbe Feature

The following are common questions about the SignalProbe feature.

Why Did I Get the Following Error Message, "Error: There are No Enabled SignalProbes to Process"?

This error message is generated when a SignalProbe compilation was attempted with either no SignalProbe pins to route, or with all SignalProbe pins disabled.

For example, this may occur if you perform a SignalProbe compilation after a full compilation. When a full compilation is performed, all SignalProbe pins are disabled. You can create or re-enable your SignalProbe pins in the **SignalProbe Pins** dialog box.

Why Did My SignalProbe Source Disappear in the Change Manager?

The SignalProbe source information for each SignalProbe is stored in the project database (**db** directory). SignalProbe pins are essentially last minute changes to your netlist and are interpreted as ECOs. These changes are stored in the project **db** and if the project database is removed, the SignalProbe source information is lost and will not appear in the **SignalProbe Pins** dialog box. To restore your SignalProbe pins, source the **signalprobe_qsf.tcl** script located in your project directory.

You can restore your SignalProbe source information by typing the following command from a command prompt:

```
quartus_cdb -t signalprobe_qsf.tcl
```

What is an ECO & Where Can I Find More Information on ECO?

ECOs are late design cycle changes done to your design that do not alter functionality and timing. For more information about ECO and using the Change Manager, refer to the *Design Analysis & Engineering Change Management with Chip Editor* chapter in volume 3 of the *Quartus II Handbook*.

How Do I Migrate My Previous SignalProbe Assignments in the Quartus II Software Versions 5.1 & Below to Versions 6.0 & Higher?

In earlier versions of the Quartus II software, SignalProbe pins were stored in the Quartus II Settings File (**.qsf**). These assignments are automatically converted into ECO changes when you open the **SignalProbe** dialog box or when you start a SignalProbe compilation in the Quartus II software versions 6.0 and higher.

For example, the SignalProbe source assignment from a Quartus II Settings File is removed and added to the Change Manager as an ECO after the **SignalProbe** dialog box is opened, or when you perform a SignalProbe compilation.

Example 11–1. SignalProbe Assignments in the Quartus II Settings File

```
set_location_assignment PIN_C22 -to my_signalprobe_pin
set_instance_assignment -name RESERVE_PIN "AS SIGNALPROBE OUTPUT" -to my_signalprobe_pin
set_instance_assignment -name IO_STANDARD LVTTL -to my_signalprobe_pin
set_instance_assignment -name SIGNALPROBE_ENABLE ON -to my_signalprobe_pin
set_instance_assignment -name SIGNALPROBE_SOURCE inst5[0] -to my_signalprobe_pi
```

Example 11–2. SignalProbe Assignments in the Quartus II Settings File After Opening the SignalProbe Pins Dialog Box

```
set_location_assignment PIN_C22 -to my_signalprobe_pin
set_instance_assignment -name RESERVE_PIN "AS SIGNALPROBE OUTPUT" -to my_signalprobe_pin
set_instance_assignment -name IO_STANDARD LVTTL -to my_signalprobe_pin
set_instance_assignment -name SIGNALPROBE_ENABLE ON -to my_signalprobe_pin
```

What are all the Changes for the SignalProbe Feature between the Quartus II Software Version 5.1 & Earlier, & Version 6.0 & Later?

The following list of changes affect users of the SignalProbe feature in the Quartus II software versions 5.1 and below with Stratix series, Cyclone series, and MAX II device families.

- Previously, the **SignalProbe Pins** dialog box was accessed on the Assignments menu. To access it with the Quartus II software version 6.0, on the Tools menu, click **SignalProbe Pins**.
- A full compilation is required before making SignalProbe connections. However, you can still reserve pins before compilation for later use by SignalProbe. You can reserve pins by creating a SignalProbe in the **SignalProbe** dialog box without specifying a source. This is the same behavior as in the Quartus II software version 5.1.

- To route the SignalProbe pins, you must perform a SignalProbe compilation after a full compilation. The **Automatically route SignalProbe signals during compilations** and **Modify latest fitting results during SignalProbe compilation** options are no longer supported.
- After subsequent compiles, full or incremental, existing SignalProbes are disabled and are not present in the post-compilation netlist. To add them back, enable the SignalProbes and perform a SignalProbe compilation.
- SignalProbes are not controlled via assignments in the Quartus II Settings File because they are now ECOs. Existing Quartus II Settings Files automatically convert to ECOs when a SignalProbe compilation is performed or when the **SignalProbe** dialog box is opened.
- The Tcl interface for creating SignalProbes has improved and is a part of the Chip Editor package `::quartus::chip_editor`. "Scripting Support" on page 11–12.
- Previously, the `quartus_fit --signalprobe` command was used to perform a SignalProbe compilation. This is not supported in the Quartus II software version 6.0 and is replaced by the improved Tcl interface and the `check_netlist_and_save` Tcl command.
- The SignalProbe timing report generated after a successful SignalProbe compilation is not available in the Quartus II software version 6.0. You can view the timing results of your SignalProbe pins in the SignalProbe Fitting Results, under the Fitter report, or in the t_{CO} results page of the Timing report.
- You can not make SignalProbe pins in the Assignment Editor. Use the **SignalProbe Pins** dialog box to make and edit your SignalProbe pins.

Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II command-line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The *Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

For more information about all settings and constraints in the Quartus II software, refer to the *Quartus II Settings File Reference Manual*.

For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Make a SignalProbe Pin

You can make a SignalProbe pin by typing the following command:

```
make_sp [-h | -help] [-long_help] [-clk <clk>] [-io_std <io_std>] -loc <loc> -pin_name \ <pin name> [-regs <regs>] [-reset <reset>] -src_name <source name> ↵
```

Delete a SignalProbe Pin

You can delete a SignalProbe pin by typing the following command:

```
delete_sp [-h | -help] [-long_help] -pin_name <pin name> ↵
```

Enable a SignalProbe Pin

You can enable a SignalProbe pin by typing the following command:

```
enable_sp [-h | -help] [-long_help] -pin_name <pin name> ↵
```

Disable a SignalProbe Pin

You can disable a SignalProbe pin by typing the following command:

```
disable_sp [-h | -help] [-long_help] -pin_name <pin name> ↵
```

Perform a SignalProbe Compilation

You can perform a SignalProbe compilation by typing the following command:

```
check_netlist_and_save ↵
```

The `quartus_fit --signalprobe` and `execute_flow -signalprobe` commands do not function in the Quartus II software version 6.0.

Migrating Previous SignalProbe Pins to the Quartus II Software Versions 6.0 & Later

You can migrate previous SignalProbe pins to the Quartus II software versions 6.0 and later by typing the following command:

```
convert_signal_probes
```

Script Example

Example 11–3 is a script that creates a SignalProbe pin called `sp1` and connecting it to source node `reg1` in a project that was already compiled.

Example 11–3. Creating a SignalProbe Pin Called sp1

```
Package require ::quartus::chip_editor
Project_open project
Read_netlist
Make_sp -pin_name sp1 -src_name reg1
Check_netlist_and_save
Project_close
```

Using SignalProbe with the APEX Device Family

You can use SignalProbe compilation to incrementally route internal signals to output pins. This process completes in a fraction of the time required to recompile the entire design. The SignalProbe incremental routing feature does not affect design behavior.

To use the SignalProbe feature, follow these steps:

1. Reserve SignalProbe pins. For more information, refer to "Reserving SignalProbe Pins" on page 11–4.
2. Assign a SignalProbe source to each SignalProbe pin.
3. Perform a SignalProbe compilation.
4. Analyze the results of a SignalProbe compilation.

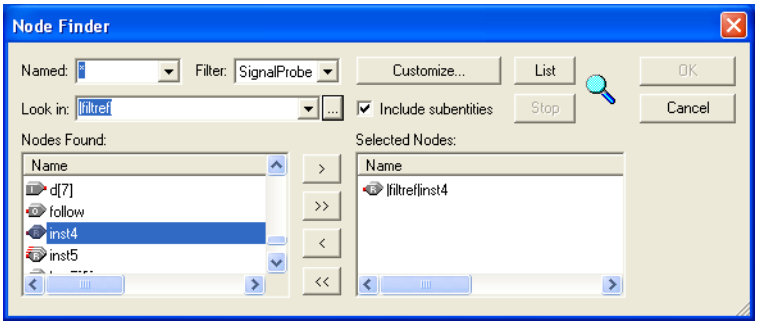
Adding SignalProbe Sources

A SignalProbe source is a signal in the post-compilation design database with a possible route to an output pin. You can assign a SignalProbe source to a SignalProbe pin, or an unused output pin by performing the following steps:

1. On the Tools menu, click **SignalProbe Pins**. The **SignalProbe Pins** dialog box appears.
2. In the **Current and potential SignalProbe pins** list, select the SignalProbe pin to which you want to add a SignalProbe source.
3. Click **Browse** and select a SignalProbe source.
4. Click **OK**.

The **Node Finder** dialog box displays with the SignalProbe filter selected (Figure 11–5). Click **List** to view all of the available SignalProbe sources. If you cannot find a specific node with the SignalProbe filter, then the node either has either been removed by the Quartus II software during optimization, or placed in the device where there are no possible routes to a pin.

Figure 11–5. Available SignalProbe Sources in the Node Finder



5. In the **Assign SignalProbe Pins** dialog box, click **Add** if a source has not been assigned to the SignalProbe pin.

   or

   Click **Change** for a SignalProbe pin that has a source already assigned.

When the source of the SignalProbe pin is added or changed, the SignalProbe pin is automatically enabled. To disable a SignalProbe pin, turn off **SignalProbe enable**.

6. Click **OK.**

Performing a SignalProbe Compilation

You can start a SignalProbe compilation manually or automatically after a full compilation. A SignalProbe compilation includes the following:

- Validates SignalProbe pins.
- Validates your specified SignalProbe sources.
- If applicable, adds registers into SignalProbe paths.
- Attempts to route from SignalProbe sources through registers to SignalProbe pins.

To run the SignalProbe compilation automatically after a full compilation, on the Tools menu, click **SignalProbe Pins**. In the **SignalProbe Pins** dialog box, turn on **Automatically route SignalProbe signals during compilation**.

To run a SignalProbe compilation manually after a full compilation, on the Processing menu, point to Start and click **Start SignalProbe Compilation**.

You must run the Fitter before a SignalProbe compilation. The Fitter generates a list of all internal nodes that can be used as SignalProbe sources.

You can enable and disable each SignalProbe pin by turning the **SignalProbe enable** option on and off in the **SignalProbe Pins** dialog box.

Running SignalProbe with Smart Compilation

Optimally, you can run a smart compilation, which reduces compilation time by running only necessary modules during compilation. However, a full compilation is required if any design files, **Analysis and Synthesis** settings, or **Fitter** settings have changed.

To turn on smart compilation, on the Assignments menu, click **Settings**. In the **Category** list, select **Compilation Process Settings and** turn on **Use Smart compilation**.

If you run a SignalProbe compilation with smart compilation turned on, and there are changes to a design file or settings related to the Analysis and Synthesis or Fitter modules, the following message is displayed:

```
Error: Can't perform SignalProbe compilation because design requires a full compilation.
```

You should turn smart compilation on, which allows you to work with the latest settings and design files.

Understanding the Results of a SignalProbe Compilation

After a SignalProbe compilation, the results appear in two sections of the compilation report file. The fitting results and status (Table 11–2) of each SignalProbe pin is displayed in the SignalProbe Fitting Result page in the Fitter section of the compilation report (Figure 11–6).

The timing results of each successfully routed SignalProbe pin is displayed in the **SignalProbe source to output delays** page in the Timing Analysis section of the compilation report (Figure 11–7).

After a SignalProbe compilation, the processing page of the Messages window also provides the results of each SignalProbe pin and displays slack information for each successfully routed SignalProbe pin.

Table 11–2. Status Values

Status	Description
Routed	Connected and routed successfully
Not Routed	Not enabled
Failed to Route	Failed routing during last SignalProbe compilation
Need to Compile	Assignment changed since last SignalProbe compilation

Figure 11–6. SignalProbe Fitting Results Page in the Compilation Report Window

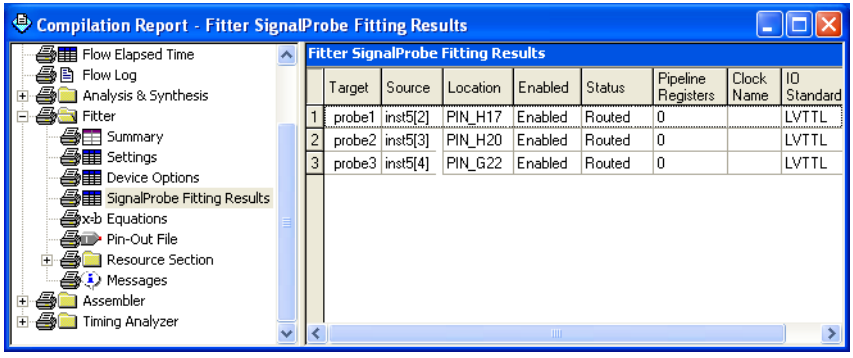
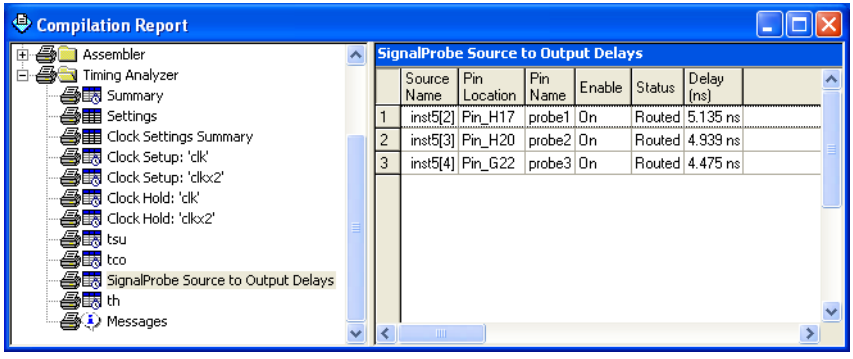


Figure 11–7. SignalProbe Source to Output Delays Page in the Compilation Report Window



Analyzing SignalProbe Routing Failures

The SignalProbe compilation can start but can fail to complete because of one of the following reasons:

- **Route unavailable**—the SignalProbe compilation failed to find a route from the SignalProbe source to the SignalProbe pin because of routing congestion
- **Invalid or nonexistent SignalProbe source**—you entered a SignalProbe source that does not exist or is invalid
- **Unusable output pin**—the output pin selected is found to be unusable

Routing failures can occur if the SignalProbe pin's I/O standard conflicts with other I/O standards in the same I/O bank.

If routing congestion prevents a successful SignalProbe compilation, you can allow the compiler to modify the routing to the specified SignalProbe source. On the Tools menu, click **SignalProbe Pins** and turn on **Modify latest fitting results during SignalProbe compilation**. This setting allows the Fitter to modify existing routing channels used by your design.

Turning on **Modify latest fitting results during SignalProbe compilation** can change the performance of your design.

SignalProbe Scripting Support for APEX Devices

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The *Scripting Reference Manual* includes the same information in PDF form.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Reserving SignalProbe Pins

Use the following Tcl commands to reserve a SignalProbe pin.

```
set_location_assignment <location> -to <SignalProbe pin name>

set_instance_assignment -name RESERVE_PIN \
"AS SIGNALPROBE OUTPUT" -to <SignalProbe pin name> ↵
```

Valid locations are pin location names, such as `Pin_A3`.

For more information about reserving SignalProbe pins, refer to "Reserving SignalProbe Pins" on page 11–4.

Adding SignalProbe Sources

Use the following Tcl commands to add SignalProbe sources. For more information about adding SignalProbe sources, refer to "Adding SignalProbe Sources" on page 11–14. The following command assigns the node name to a SignalProbe pin:

```
set_instance_assignment -name SIGNALPROBE_SOURCE \
<node name> -to <SignalProbe pin name> ↵
```

The next command turns on the SignalProbe routing. You can turn off individual SignalProbe pins by specifying `OFF` instead of `ON` with the following command:

```
set_instance_assignment -name SIGNALPROBE_ENABLE ON \
-to <SignalProbe pin name> ↵
```

Assigning I/O Standards

Use the following Tcl command to assign an I/O standard to a pin:

```
set_instance_assignment -name IO_STANDARD \
<I/O standard> -to <SignalProbe pin name> ↵
```

For a list of valid I/O standards, refer to the I/O Standards general description in the Quartus II Help.

Adding Registers for Pipelining

Use the following Tcl commands to add registers for pipelining:

```
set_instance_assignment -name SIGNALPROBE_CLOCK \
<clock name> -to <SignalProbe pin name>
```

```
set_instance_assignment \
-name SIGNALPROBE_NUM_REGISTERS <number of registers> \
-to <SignalProbe pin name> ↵
```

For more information about adding registers for pipelining, refer to "Adding Registers for Pipelining" on page 11–19.

Run SignalProbe Automatically

Use the following Tcl command to run SignalProbe automatically after a full compile.

```
set_global_assignment -name SIGNALPROBE_DURING_NORMAL_COMPILATION ON
```

For more information about running SignalProbe automatically, refer to "Performing a SignalProbe Compilation" on page 11–15.

Run SignalProbe Manually

You can run SignalProbe manually with a Tcl command or the `quartus_fit` command at a command prompt.

```
execute_flow -signalprobe ↵
```

The `execute_flow` command is in the flow package. At a command prompt, type the following command:

```
quartus_fit <project name> --signalprobe ↵
```

For more information about running SignalProbe manually, refer to "Performing a SignalProbe Compilation" on page 11–15.

Enable or Disable All SignalProbe Routing

Use the Tcl command in Example 11–4 to turn on or turn off SignalProbe routing. In the `set_instance_assignment` command, specify `ON` to turn on SignalProbe routing or `OFF` to turn off SignalProbe routing.

Example 11–4. Turning SignalProbe On or Off with Tcl

```
set spe [get_all_assignments -name SIGNALPROBE_ENABLE] \
foreach_in_collection asgn $spe {
   set signalprobe_pin_name [lindex $asgn 2]
   set_instance_assignment -name SIGNALPROBE_ENABLE -to \
$signalprobe_pin_name <ON|OFF> } ↵
```

For more information about enabling or disabling SignalProbe routing, refer to page 11–15.

Running SignalProbe with Smart Compilation

Use the following Tcl command to turn on **Smart Compilation**:

```
set_global_assignment -name SMART_RECOMPILE ON ↵
```

For more information, refer to "Running SignalProbe with Smart Compilation" on page 11–16.

Allow SignalProbe to Modify Fitting Results

Use the following Tcl command to turn on **Modify latest fitting results**.

```
set_global_assignment -name SIGNALPROBE_ALLOW_OVERUSE ON ↵
```

For more information, refer to "Analyzing SignalProbe Routing Failures" on page 11–18.

Conclusion

Using the SignalProbe feature can significantly reduce the time required compared to a full recompilation. You can use the SignalProbe feature to get quick access to internal design signals to perform system-level debugging.

12. Design Debugging Using the SignalTap II Embedded Logic Analyzer

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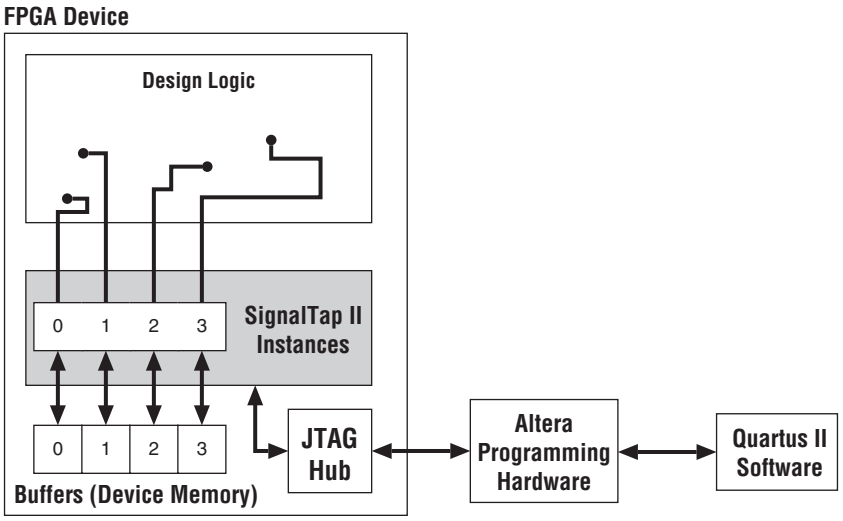
Introduction

The phenomenal growth in design size and complexity continues to make design verification a critical bottleneck for today's FPGA systems. Limited access to internal signals, complex FPGA packages, and PCB electrical noise all contribute to making design debugging the most challenging process of the design cycle. More than 50% of the design cycle time can easily be spent on debugging and verifying the design. To help with the process of design debugging, Altera® provides a solution that enables a designer to examine the behavior of internal signals, without using extra I/O pins, while the design is running at full speed on an FPGA device.

The SignalTap® II Embedded Logic Analyzer is scalable, easy to use, and is included with the Quartus® II software subscription. This logic analyzer helps debug an FPGA design by probing the state of the internal signals in the design without the use of external equipment. Defining custom trigger-condition logic provides greater accuracy and improves the ability to isolate problems. The SignalTap II Embedded Logic Analyzer does not require external probes, or changes to the design files to capture the state of the internal nodes or I/O pins in the design. All captured signal data is conveniently stored in device memory until the designer is ready to read and analyze the data.

The SignalTap II Embedded Logic Analyzer is a second-generation system-level debugging tool that captures and displays real-time signal behavior in a system on a programmable chip (SOPC). The SignalTap II Embedded Logic Analyzer supports the highest number of channels, sample depth, and clock speeds of any embedded logic analyzer in the programmable logic market. Figure 12–1 shows a block diagram of the components that make up the SignalTap II Embedded Logic Analyzer.

Figure 12–1. SignalTap II Logic Analyzer Block Diagram (1)



Notes to Figure 12–1:

(1) This diagram assumes that the SignalTap II Logic Analyzer was compiled with the design as a separate design partition using the Quartus II Incremental Compilation feature. If incremental compilation is not used, the SignalTap II logic is integrated with the design. For information about the use of incremental compilation with SignalTap II, refer to "Faster Compilations Using SignalTap II Incremental Compilation" on page 12–40.

This chapter is intended for any designer who wants to debug their FPGA design during normal device operation without the need for external lab equipment. Due to the SignalTap II Embedded Logic Analyzer's similarity to traditional external logic analyzers, familiarity with external logic analyzer operations is helpful but not necessary. To take advantage of faster compile times when making changes to the SignalTap II Logic Analyzer, knowledge of the Quartus II Incremental Compilation feature is helpful.

For information about using the Quartus II Incremental Compilation feature, refer to the *Incremental Compilation for Hierarchical & Team-Based Design* chapter in the *Quartus II Handbook*.

Hardware & Software Requirements

The following components are required to perform logic analysis with the SignalTap II Embedded Logic Analyzer:

- Quartus II design software

  or

Quartus II Web Edition (with TalkBack feature enabled)

or

SignalTap II Logic Analyzer standalone software

- Download/Upload Cable
- Altera development kit or user design board with JTAG connection to device under test

Captured data is stored in the device's memory blocks and transferred to the Quartus II software waveform display with a JTAG communication cable such as EthernetBlaster or USB-Blaster™. Table 12–1 summarizes some of the features and benefits of the SignalTap II Embedded Logic Analyzer.

Table 12–1. SignalTap II Features & Benefits

Feature	Benefit
Multiple logic analyzers in a single device	Capture data from multiple clock domains in a design at the same time
Multiple logic analyzers in multiple devices in a single JTAG chain	Simultaneously capture data from multiple devices in a JTAG chain
Plug-In Support	Easily specify nodes, triggers, and signal mnemonics for IP such as the Nios® II embedded processor
Up to 10 basic or advanced trigger levels for each analyzer	Enables more complex data capture commands to be sent to the logic analyzer, providing greater accuracy and problem isolation
Power-Up Trigger	Capture signal data for triggers that occur after device programming but before manually starting the logic analyzer
Incremental Compilation	Modify the SignalTap II Logic Analyzer monitored signals and triggers without performing a full compilation, saving time
Flexible buffer acquisition modes	Allows more accurate data collection by setting each trigger to sample at different ranges relative to the triggering event, in circular or segmented modes
MATLAB integration with included MEX function	Acquire the SignalTap II Logic Analyzer captured data into a MATLAB integer matrix
Up to 1,024 channels in each device	Sample many signals and wide bus structures
Up to 128K samples in each device	Capture a large sample set for each channel
Clock frequencies up to 270 MHz	Collect sample data at up to 270 MHz
Resource usage estimator	Provides estimate of logic and memory device resources used by SignalTap II Embedded Logic Analyzer configurations
No additional cost	The SignalTap II Logic Analyzer is included with a Quartus II subscription

The SignalTap II Logic Analyzer supports the following device families:

- Stratix® II
- Stratix II GX
- Stratix
- Stratix GX
- Cyclone II
- Cyclone™
- APEX™ II
- APEX 20KE
- APEX 20KC
- APEX 20K
- Mercury™

On-Chip Debugging Tool Comparison

The Quartus II software provides a number of different ways to help debug your FPGA design after programming the device. The SignalTap II Logic Analyzer, SignalProbe™, and the Logic Analyzer Interface (LAI) share some similar features, but each has advantages. In some debugging situations, it can be difficult to decide which tool is best to use or whether multiple tools are required. Table 12–2 compares these debugging tools and lists situations and requirements for the use of each.

Table 12–2. On-Chip Debugging Tools-Comparison (Part 1 of 2)

Feature	SignalProbe	Logic Analyzer Interface (LAI)	SignalTap II Embedded Analyzer
Sample Depth—An external logic analyzer used with the LAI has a bigger buffer to store more captured data than SignalTap II Logic Analyzer. No data is captured or stored with SignalProbe.		✓	
Ease in Debugging Timing Issue—An external logic analyzer used with the LAI provides you with access to a "timing" mode, enabling you to debug combined streams of data.	N/A	✓	
Performance—The LAI adds minimal logic to a design, requiring fewer device resources. The SignalTap II Logic Analyzer has little affect on performance when it is set as a separate design partition using incremental compilation. SignalProbe incrementally routes nodes to pins, not affecting the design at all.	✓	✓ *(1)*	✓ *(1)*

Table 12–2. On-Chip Debugging Tools-Comparison (Part 2 of 2)

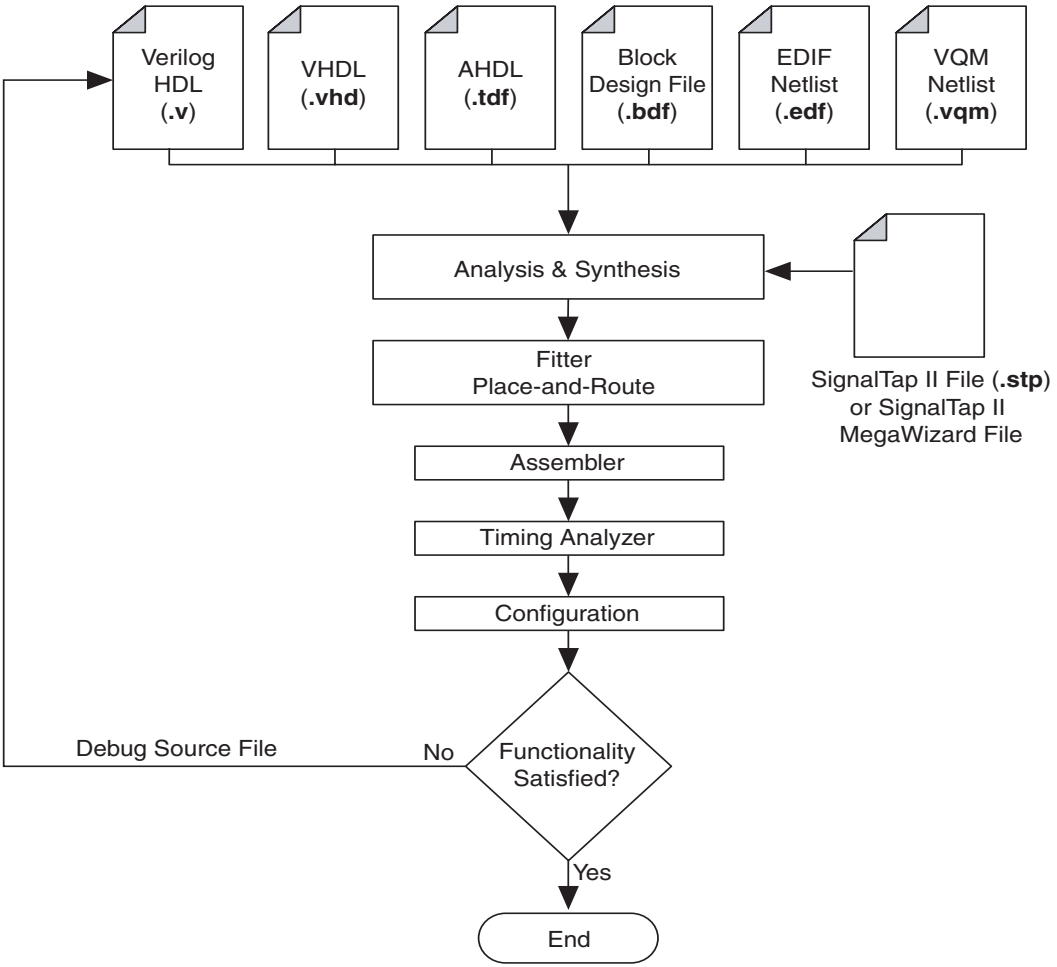
Feature	SignalProbe	Logic Analyzer Interface (LAI)	SignalTap II Embedded Analyzer
Compile and Recompile Time—SignalProbe attaches incrementally routed signals to previously reserved pins, requiring very little recompilation time to make changes to source signal selections. The SignalTap II Logic Analyzer and the LAI can take advantage of incremental compilation to refit their own design partitions to decrease recompilation time.	✓	✓ *(1)*	✓*(1)*
Triggering Capability—Although advanced triggering is available in the SignalTap II Logic Analyzer, many additional triggering options are available on an external logic analyzer when used with the LAI.	N/A	✓	
I/O Usage—No additional output pins are required with the SignalTap II Logic Analyzer. Both the LAI and SignalProbe require I/O pin assignments.			✓
Acquisition Speed—The SignalTap II Logic Analyzer can acquire data at speeds of over 200 MHz. The same acquisition speeds are obtainable with an external logic analyzer used with the LAI, but signal integrity issues may limit this.	N/A		✓
No JTAG Connection Required—An FPGA design with the SignalTap II Logic Analyzer or the LAI requires an active JTAG connection to a host running the Quartus II software. SignalProbe does not require a host for debugging purposes.	✓		
External Equipment—The SignalTap II Logic Analyzer is completely internal to the programmed FPGA device, so no extra equipment other than a JTAG connection is required. SignalProbe and the LAI requires the use of external debugging equipment such as multimeters, oscilloscopes, or logic analyzers.			✓

Note to Table 12–2:
(1) Applies when used with incremental compilation.

Design Flow Using the SignalTap II Logic Analyzer

Figure 12–3 shows a typical overall FPGA design flow for using the SignalTap II Logic Analyzer in your design. A SignalTap II file (**.stp**) is added to and enabled in your project, or a SignalTap II HDL function, created with the MegaWizard® Plug-in Manager, is instantiated in your design. The diagram shows the flow of operations from initially adding the SignalTap II Logic Analyzer to your design to the final device configuration, testing, and debugging.

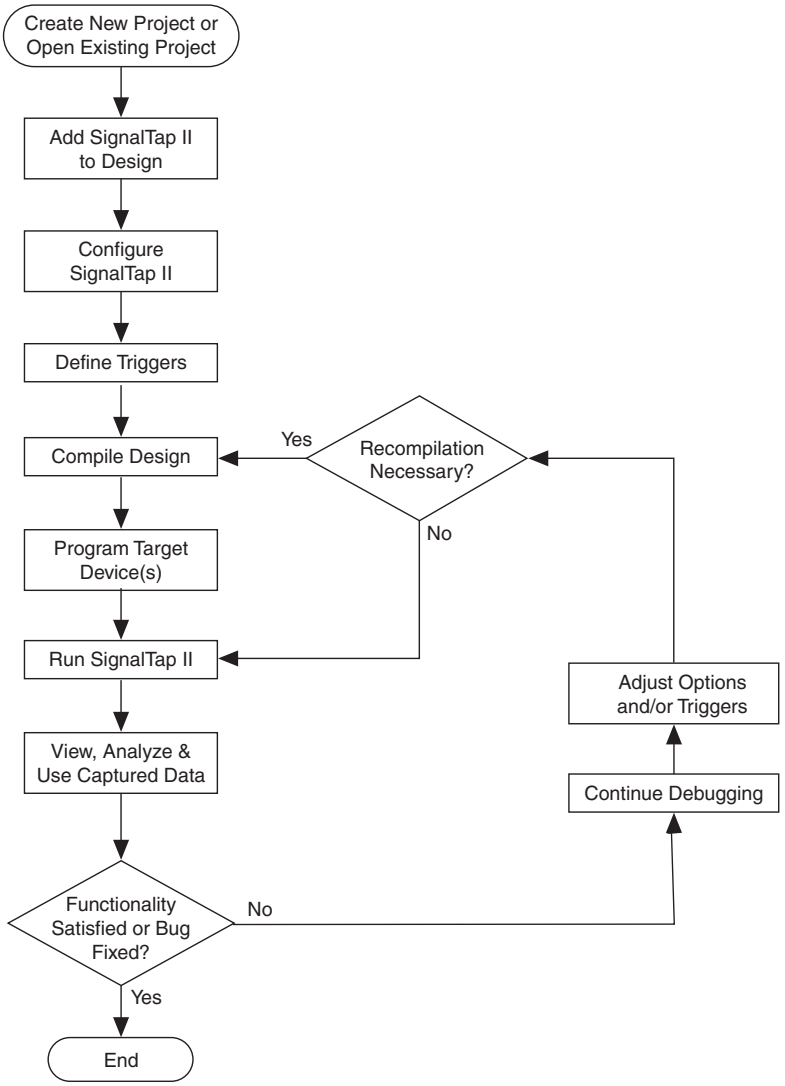
Figure 12–2. SignalTap II FPGA Design & Debugging Flow



SignalTap II Logic Analyzer Task Flow

To use the SignalTap II Logic Analyzer to debug your design, you perform a number of tasks to add, configure, and run the logic analyzer. Figure 12–3 shows a typical flow of the tasks you complete to debug your design. Refer to the appropriate section of this chapter for more information about each of these tasks.

Figure 12–3. SignalTap II Logic Analyzer Task Flow



Add the SignalTap II Logic Analyzer to Your Design

Create a SignalTap II file or create a parameterized HDL instance representation of the logic analyzer using the MegaWizard Plug-In Manager. If you want to monitor multiple clock domains simultaneously, you can add additional instances of the logic analyzer to your design, limited only by the available resources in your device.

Configure the SignalTap II Logic Analyzer

Once the SignalTap II Logic Analyzer is added to your design, you configure it to monitor the signals you want. You can manually add signals or use a plug-in, such as the Nios II plug-in, to quickly add entire sets of associated signals. You can also specify settings for the data capture buffer such as its size, the method in which data is captured and stored, and the device memory type to use for the buffer in devices that support memory type selection.

Define Triggers

To capture signal data, you set up triggers that tell the logic analyzer under what conditions to begin the capture. The SignalTap II Logic Analyzer lets you define Run-Time Triggers that range from very simple, such as the rising edge of a single signal, to very complex, involving groups of signals, extra logic, and multiple conditions. Power-Up Triggers give you the ability to capture data from trigger events occurring immediately after the device enters user-mode after configuration.

Compile the Design

With the SignalTap II file configured and triggers defined, you compile your project as usual to include the logic analyzer in your design. Since you may need to frequently change monitored signal nodes or adjust trigger settings during debugging, you can use the incremental compilation feature built-in to the SignalTap II Logic Analyzer along with Quartus II incremental compilation to reduce recompile times.

Program the Target Device(s)

When you are debugging a design with the SignalTap II Logic Analyzer, you program a target device directly from the SignalTap II file without using the Quartus II Programmer. You can also program multiple devices with different designs and simultaneously debug them.

Run the SignalTap II Logic Analyzer

In normal device operation, you control the logic analyzer through the JTAG connection, specifying when to start looking for your trigger conditions to begin capturing data. With Run-Time or Power-Up Triggers, you read and transfer the captured data from the on-chip buffer to the SignalTap II file for analysis.

View, Analyze & Use Captured Data

Once you have captured data and read it into the SignalTap II file, it is available for analysis and use in the debugging process. You can set up mnemonic tables, either manually or with a plug-in, to make it easier to read and interpret the captured signal data. You can use the locate feature in the SignalTap II node list to quickly find the locations of problem nodes in other tools in the Quartus II software to speed up debugging. Save the captured data for later analysis or convert it to other formats for sharing and further study.

Add the SignalTap II Logic Analyzer to Your Design

Since the SignalTap II Logic Analyzer is implemented in logic on your target device, it must be added to your FPGA design as another part of the design itself. There are two ways to generate the SignalTap II Logic Analyzer and add it to your design for debugging. The first method is to create a SignalTap II file (**.stp**) and use the SignalTap II file window to configure the details of the logic analyzer. The second method is to create and configure the SignalTap II file with the MegaWizard Plug-in Manager and instantiate it in your design.

Creating & Enabling a SignalTap II File

To create an embedded logic analyzer, you can use an existing SignalTap II file or create a new file. Once a file is created or selected, it must be enabled in the project where it is used.

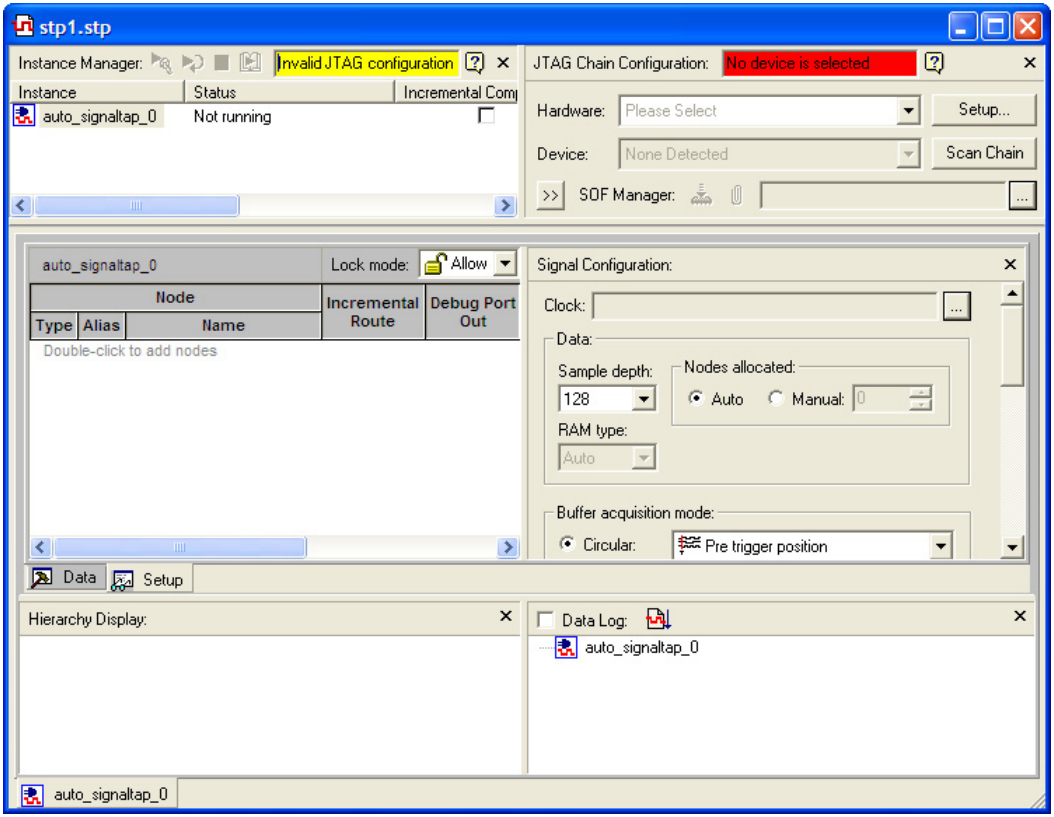
Creating a SignalTap II File

The SignalTap II file contains the SignalTap II Logic Analyzer settings and the captured data for viewing and analysis. To create a new SignalTap II file, perform the following steps:

1. On the File menu, click **New**.
2. In the **New** dialog box, click the **Other Files** tab, and select **SignalTap II File**.
3. Click **OK**.

To open an existing SignalTap II file already associated with your project, on the Tools menu, click **SignalTap II Logic Analyzer**. You can also use this method to create a new SignalTap II file if no SignalTap II file exists for the current project, or, to open an existing file, on the File menu, click **Open** and select a SignalTap II file (Figure 12–4).

Figure 12–4. SignalTap II File Window



Enabling & Disabling a SignalTap II File for the Current Project

Whenever you save a new SignalTap II file, the Quartus II software asks you if you want to enable the file for the current project. However, you can add this file manually, change the selected SignalTap II file, or completely disable the logic analyzer by performing the following steps:

1. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
2. In the **Category** list, select **SignalTap II Logic Analyzer.** The **SignalTap II Logic Analyzer** page appears.
3. Turn on **Enable SignalTap II Logic Analyzer.** Turn off this option to disable the logic analyzer, completely removing it from your design.
4. In the **SignalTap II File name** box, type the name of the SignalTap II file you want to include with your design, or browse to and select a file name.
5. Click **OK**.

Using the MegaWizard Plug-In Manager to Create Your Embedded Logic Analyzer

Alternatively, you can create a SignalTap II Logic Analyzer instance by using the MegaWizard Plug-In Manager. The MegaWizard Plug-In Manager generates an HDL file that you instantiate in your design. You can also use a hybrid approach in which you instantiate the MegaWizard Plug-In Manager file in your HDL, and then use the method described in "Creating & Enabling a SignalTap II File" on page 12–9.

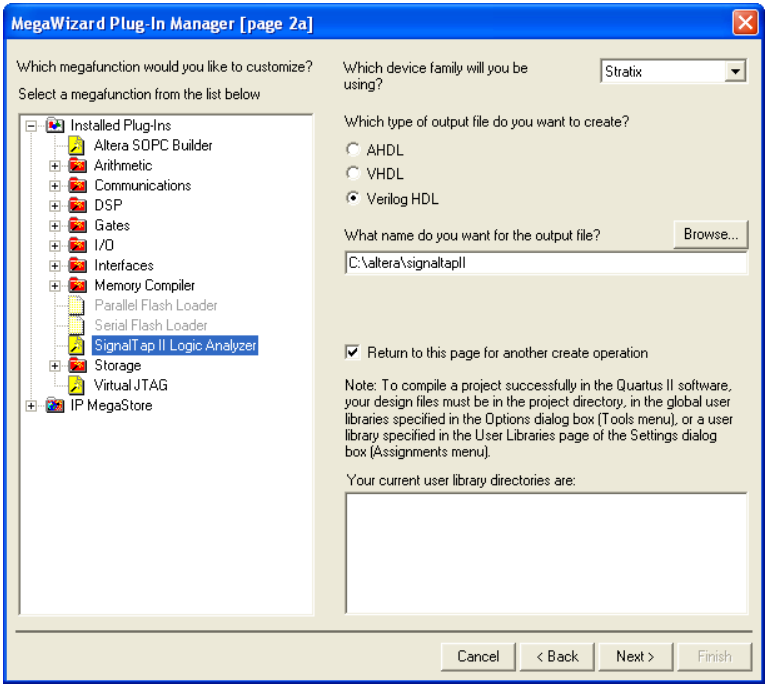
Creating an HDL Representation Using the MegaWizard Plug-In Manager

The Quartus II software allows you to easily create your SignalTap II Logic Analyzer using the MegaWizard Plug-In Manager. To implement the SignalTap II megafunction, perform the following steps:

1. On the Tools menu, click **MegaWizard Plug-In Manager**. The **MegaWizard Plug-In Manager** dialog box appears.
2. Select **Create a new custom megafunction variation**.
3. Click **Next**.

4. In the **Installed Plug-In** list, select **SignalTap II Logic Analyzer**. Select an output file type and enter the desired name of the SignalTap II megafunction. You can choose AHDL (**.tdf**), VHDL (**.vhd**), or Verilog HDL (**.v**) as the output file type (Figure 12–5).

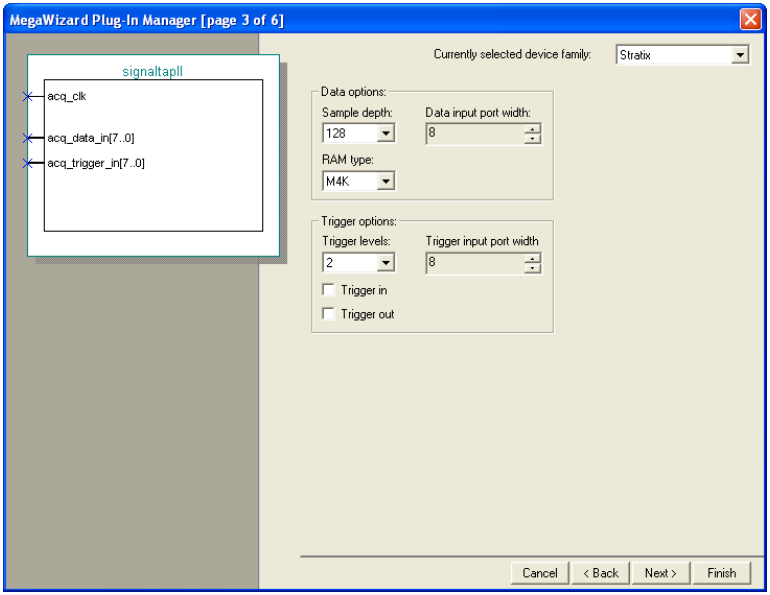
Figure 12–5. Creating the SignalTap II Logic Analyzer in the MegaWizard Plug-In Manager



5. Click **Next**.

6. Configure the analyzer by specifying the **Sample depth**, **RAM Type**, **Data input port width**, **Trigger levels**, **Trigger input port width**, and whether to enable an external **Trigger in** or **Trigger out** (Figure 12–6).

Figure 12–6. Select Logic Analyzer Parameters

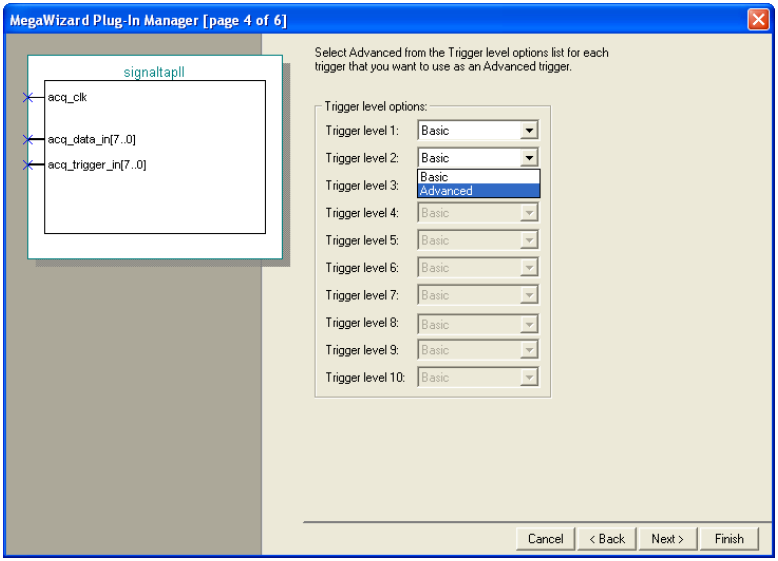


7. Click **Next**.

8. Set the **Trigger level** options by selecting **Basic** or **Advanced** (Figure 12–7).

You cannot define a Power-Up Trigger using the MegaWizard Plug-In Manager. Refer to "Define Triggers" on page 12–28 to learn how to do this using the SignalTap II file.

Figure 12–7. MegaWizard Basic & Advanced Trigger Options



9. Click **Finish** to create an HDL representation of the SignalTap II Logic Analyzer.

For information about the configuration settings options in the MegaWizard Plug-In Manager, refer to "Configure the SignalTap II Logic Analyzer" on page 12–17. For information about defining triggers, refer to "Define Triggers" on page 12–28.

SignalTap II Megafunction Ports

Table 12–3 provides information on the SignalTap II megafunction ports.

For the most current information on the ports and parameters for this megafunction, refer to the latest version of the Quartus II Help.

Table 12–3. SignalTap II Megafunction Ports

Port Name	Type	Required	Description
acq_data_in	Input	No	This set of signals represents the set of signals that are monitored in the SignalTap II Logic Analyzer.
acq_trigger_in	Input	No	This set of signals represents the set of signals that are used to trigger the analyzer.
acq_clk	Input	Yes	This port represents the sampling clock that the SignalTap II Logic Analyzer uses to capture data.
trigger_in	Input	No	This signal is used to trigger the SignalTap II Logic Analyzer.
trigger_out	Output	No	This signal is enabled when the trigger event occurs.

Instantiating the SignalTap II Logic Analyzer in Your HDL

Instantiating the logic analyzer in your HDL is similar to instantiating any other Verilog HDL or VHDL megafunction in your design. You can instantiate up to 127 analyzers in your design, or as many as physically fit in the FPGA. Once you have instantiated the SignalTap II file in your HDL file, compile your Quartus II project to fit the logic analyzer in the target FPGA.

To capture and view the data, you must create a SignalTap II file from your SignalTap II HDL output file. To do this, select Create/Update on the File menu, and click **Create SignalTap II File from Design Instance(s)**.

Embedding Multiple Analyzers in One FPGA

The SignalTap II Logic Analyzer includes support for multiple logic analyzers in an FPGA device. This feature allows you to create a unique logic analyzer for each clock domain in the design. As multiple instances of the analyzer are added to the SignalTap II file, the resource usage increases proportionally.

In addition to debugging multiple clock domains, this feature allows you to apply the same SignalTap II settings to a group of signals in the same clock domain. For example, if you have a set of signals that must use a

sample depth of 64K, while another set of signals in the same clock domain requires a sample depth of 1K, you can create two instances to meet these needs.

To create multiple analyzers, on the Edit menu, click **Create Instance**, or right-click in the Instance Manager window and click **Create Instance**.

Monitoring FPGA Resources Used by the SignalTap II Logic Analyzer

The SignalTap II Logic Analyzer has a built-in resource estimator that calculates the logic resources and amount of memory that each SignalTap II Logic Analyzer uses. You can see the resource usage of each logic analyzer instance and the total resources used in the columns of the Instance Manager section of the SignalTap II file window. This feature is useful when device resources are limited and you must know what device resources the SignalTap II Logic Analyzer uses. The value reported in the resource usage estimator may vary by as much as 5% from the actual resource usage.

Table 12–4 shows the SignalTap II Logic Analyzer M4K memory block resource usage for these devices per signal width and sample depth.

Table 12–4. SignalTap II Logic Analyzer M4K Block Utilization for Stratix II, Stratix, Stratix GX, & Cyclone Devices *Note (1)*

Signals (Width)	Samples (Width)			
	256	512	2,048	8,192
8	< 1	1	4	16
16	1	2	8	32
32	2	4	16	64
64	4	8	32	128
256	16	32	128	512

Note to Table 12–4:

(1) When you configure a SignalTap II Logic Analyzer, the Instance Manager reports an estimate of the memory bits and logic elements required to implement the given configuration.

Configure the SignalTap II Logic Analyzer

The SignalTap II file provides many options for configuring instances of the logic analyzer. Some of the settings are similar to those found on traditional external logic analyzers. Other settings are unique to the SignalTap II Logic Analyzer because of the properties of configuring an embedded logic analyzer. All settings give you the ability to configure the logic analyzer the way you want to help debug your design.

Some settings can only be adjusted when you are viewing Run-Time Trigger conditions instead of Power-Up Trigger conditions. To learn about Power-Up Triggers and viewing different trigger conditions, refer to "Creating a Power-Up Trigger" on page 12–33.

Assigning an Acquisition Clock

You must assign a clock signal to control the acquisition of data by the SignalTap II Logic Analyzer. The logic analyzer samples data on every rising edge of the acquisition clock. You can use any signal in your design as the acquisition clock. However, for best results, Altera recommends that you use a global clock for data acquisition and not a gated clock. Using a gated clock as your acquisition clock can result in unexpected data that does not accurately reflect the behavior of your design. The Quartus II Timing Analyzer shows the maximum acquisition clock frequency at which you can run your design.

To assign an acquisition clock, perform the following steps:

1. In the SignalTap II Logic Analyzer window, click the **Setup** tab.
2. Click **Browse** next to the **Clock** field in the Signal Configuration pane. The **Node Finder** dialog box appears.
3. If you are not using the SignalTap II incremental compilation feature, select **SignalTap II: pre-synthesis** in the **Filter** list.
   or
   If you are using incremental compilation, select **SignalTap II: post-fitting** in the **Filter** list.

   You cannot insert a clock signal that is shown in the **SignalTap II: post-fitting** filter unless you are using incremental compilation. The opposite is true as well. If you are using incremental compilation, you cannot use a clock signal shown in the **SignalTap II: pre-synthesis** filter. For more information about the use of incremental compilation with SignalTap II, refer to "Compile the Design" on page 12–39.

4. In the **Named** field, type or select the name of the signal that you would like to use as your sample clock.

5. To start the node search, click **List**.

6. In the **Node Finder** dialog box, select the node representing the design's global clock signal.

7. To copy the selected node name to the **Selected Nodes** list, click ">"
   or
   Double-click the node name.

8. Click **OK**. The node is now specified as the clock in the SignalTap II window.

If you do not assign an acquisition clock in the SignalTap II window, the Quartus II software automatically creates a clock pin called `auto_stp_external_clk`.

You must make a pin assignment to this pin independently from the design. You must ensure that a clock signal in your design drives the acquisition clock.

For information on assigning signals to pins, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Adding Signals to the SignalTap II File

While configuring the logic analyzer, you add signals to the node list in the SignalTap II file to select which signals in your design you want to monitor. Selected signals are also used to define triggers. You can assign the following two types of signals to your SignalTap II file:

- **Pre-synthesis**—A pre-synthesis signal exists after design elaboration, but before any synthesis optimizations are done. This set of signals should reflect your Register Transfer Level (RTL) signals.
- **Post-fitting**—A post-fitting signal exists after physical synthesis optimizations and place-and-route.

If you are not using incremental compilation, add only pre-synthesis signals to your SignalTap II file. This is particularly useful if you want to quickly add a new node after you have made design changes. To do this, on the Processing menu, click **Start Analysis & Elaboration**.

After successful Analysis and Elaboration, the signals shown in red text are invalid signals, and you must remove them from the SignalTap II file for correct operation. This can happen if, for example, you added pre-synthesis signals to the SignalTap II file and then enabled incremental compilation. Because only post-fitting signals are used with SignalTap II incremental compilation, the pre-synthesis signals are invalid. The SignalTap II Health Monitor also indicates if an invalid node name exists in the SignalTap II file.

For more information about the use of incremental compilation with the SignalTap II Logic Analyzer, refer to "Faster Compilations Using SignalTap II Incremental Compilation" on page 12–40.

Signal Preservation

Many of your RTL signals are optimized during the process of synthesis and place-and-route. This can lead to issues when you debug your design, because the post-fitting signal names differ significantly from your RTL names. This can also cause a problem if you are using incremental compilation. Since only post-fitting signals can be added to the SignalTap II Logic Analyzer if incremental compilation is used, RTL signals that you want to monitor may not be available post-fit, preventing their usage. To avoid this issue, you can use synthesis attributes to preserve signals during synthesis and place-and-route. When the Quartus II software encounters these synthesis attributes, it does not perform any optimization on the specified signals, forcing them to continue to exist in the post-fit netlist. However, if you do this, you could see an increase in resource utilization or a decrease in timing performance. The two attributes you can use are:

- **Keep—**This attribute ensures that combinational signals are not removed.
- **Preserve—**This attribute ensures that registers are not removed.

For more information on using these attributes, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

If you are debugging an IP core, such as the Nios II CPU, you may need to preserve nodes from these cores to make them available for debugging with the SignalTap II Logic Analyzer. This is often necessary when a plug-in is used to add a group of signals for a particular IP. To do this, on the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**. Turn on **Create debugging nodes for IP cores** to make these nodes available to the SignalTap II Logic Analyzer.

Assigning Data Signals

To assign data signals, perform the following steps:

1. Perform Analysis and Elaboration, Analysis and Synthesis, or compile your design.
2. In the SignalTap II Logic Analyzer window, click the **Setup** tab.
3. Double-click anywhere in the node list of the SignalTap II window to open the **Node Finder** dialog box.
4. In the **Fitter** list, select **SignalTap II: pre-synthesis** or **SignalTap II: post-fitting**.

   If you use the SignalTap II Incremental Compilation feature, you can only add post-fitting nodes to the node list.

5. In the **Named** field, type a node name, partial node name, or wildcard characters. To start the node name search, click **List.**
6. In the **Nodes Found** list, select the node or bus you want to add to the SignalTap II file.
7. To copy the selected node names to the **Selected Nodes** list, double-click the names or click "**>**".
8. To insert the selected nodes in the SignalTap II file, click **OK**. With the default colors set for the SignalTap II Logic Analyzer, a pre-synthesis signal in the list is shown in black while a post-fitting signal is shown in blue.

   You can also drag and drop signals from the **Node Finder** dialog box into a SignalTap II file.

Node List Signal Use Options

Once a signal is added to the node list, you can specify options about how the signal is used with the logic analyzer. You can turn off the ability of a signal to trigger the analyzer by disabling the **Trigger Enable** for that signal in the node list in the SignalTap II file. This option is useful when you want to see only the captured data for a signal, and you are not using that signal as part of a trigger.

You can turn off the ability to view data for a signal by disabling the **Data Enable** column. This option is useful when you want to trigger on a signal, but have no interest in viewing data for that signal.

For information about using signals in the node list to create SignalTap II trigger conditions, refer to "Define Triggers" on page 12–28.

Untappable Signals

Not all of the post-fitting signals in your design are available in the **SignalTap II: post-fitting** filter in the **Node Finder** dialog box. The following signal types cannot be tapped:

- Signals that are part of a carry chain—You cannot tap the carry out (`cout0` or `cout1`) signal of a logic element. Due to architectural restrictions, the carry out signal can only feed the carry in of another logic element (LE).
- Phase-locked loop (PLL) `clkout`—You cannot tap the output clock of a PLL. Due to architectural restrictions, the `clkout` signal can only feed the clock port of a register.
- JTAG Signals—You cannot tap the JTAG control (`TCK`, `TDI`, `TDO`, and TMS) signals.
- `ALTGXB` megafunction—You can not directly tap any ports of an `ALTGXB` instantiation.
- LVDS—You cannot tap the data output from a serializer/deserializer (SERDES) block.

Adding Signals with a Plug-In

Instead of adding individual or grouped signals through the **Node Finder** dialog box, you can add groups of relevant signals of a particular type of IP through the use of a plug-in. The SignalTap II Logic Analyzer comes with one plug-in already installed for the Nios II processor. Besides easy signal addition, plug-ins also provide a number of other features such as pre-designed mnemonic tables, useful for trigger creation and data viewing, as well as the ability to disassemble code in captured data.

The Nios II plug-in, for example, creates one mnemonic table in the **Setup** tab, and two tables in the **Data** tab:

- **Nios II Instruction** (**Setup** tab) —Capture all the required signals for triggering on a selected instruction address.
- **Nios II Instance Address** (**Data** tab)—Display address of executed instructions in hexadecimal format or as a programming symbol name if defined in an optional Executable and Linking Format (**.elf**) file.
- **Nios II Disassembly** (**Data** tab)—Displays disassembled code from the corresponding address.

For information about the other features plug-ins provide, refer to "Define Triggers" on page 12–28 and "View, Analyze & Use Captured Data" on page 12–50.

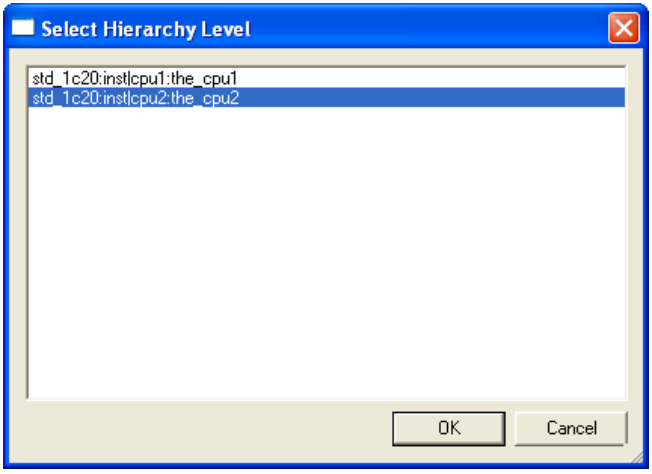
To add signals to the SignalTap II file using a plug-in, perform the following steps:

1. Right-click in the node list. On the **Add Nodes with Plug-In** submenu, click the name of the plug-in you want to use, such as the included plug-in named **Nios II**.

   If the intellectual property (IP) for the selected plug-in does not exist in your design, a message appears informing you that you cannot use the selected plug-in.

2. A dialog box appears with the IP hierarchy of your design (Figure 12–8). Select the **IP** that has the signals you want to monitor with the plug-in, and click **OK**.

Figure 12–8. IP Hierarchy Selection



3. If all the signals in the plug-in are available, a dialog box may appear, depending on the plug-in selected, where you can set any available options for the plug-in. With the Nios II plug-in, you can optionally select an Executable and Linking Format (**.elf**) file containing program symbols from your Nios II Integrated Development Environment (IDE) software design. Set options for the selected plug-in as desired, and click **OK**.

To make sure all the required signals are available, turn on the **Create debugging nodes for IP cores** option in the Quartus II Analysis & Synthesis settings.

All the signals included in the plug-in are added to the node list.

Enabling Debug Ports to Preserve FPGA Memory

You can configure the SignalTap II Logic Analyzer to store captured data in the device RAM or route captured data to I/O pins to analyze with an external logic analyzer. The following factors can affect the mode of operation you choose:

- The availability of device RAM and I/O pins
- The number of trigger levels in use in the analysis
- Whether the SignalTap II Logic Analyzer is used in conjunction with external test equipment

When device RAM is limited, you can route internal signals to unused I/O pins for capture by an external logic analyzer. This method is useful for memory-intensive applications in which the amount of saved data exceeds the available device RAM. The Quartus II software automatically generates debugging port signals that connect internal FPGA signals to output pins. You must assign these signals to I/O pins. To use the SignalTap II Logic Analyzer debugging port configuration, perform the following steps:

1. In the SignalTap II file window, select one or more signals in the node list.
2. On the Edit menu, click **Enable Debug Port**, or right-click in the **Debug Port Out** column of the node list, and click **Enable Debug Port**.

If you want to rename the debugging port pins, type the new name in the **Debug Port Out** column. The default signal name for the debugging ports is `auto_stp_debug_out_<m>_<n>`, where *m* refers to the instance number and *n* refers to the signal number. For example, if you enable the debugging port in the second instance for the fourth signal, the resulting signal name is `auto_stp_debug_out_2_4`.

3. Manually assign the debugging port signal name to an unused I/O pin.

For information on assigning signals to pins, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

You can use this feature in conjunction with an external trigger out to synchronize an external logic analyzer with the SignalTap II Logic Analyzer.

To set up an external trigger out signal, refer to "Using External Triggers" on page 12–36.

Specifying the Sample Depth

The sample depth specifies the number of samples that are captured and stored for each signal. To set the sample depth, select the desired number of samples in the **Sample Depth** list. The sample depth ranges from 0 to 128K.

Capturing Data to a Specific RAM Type

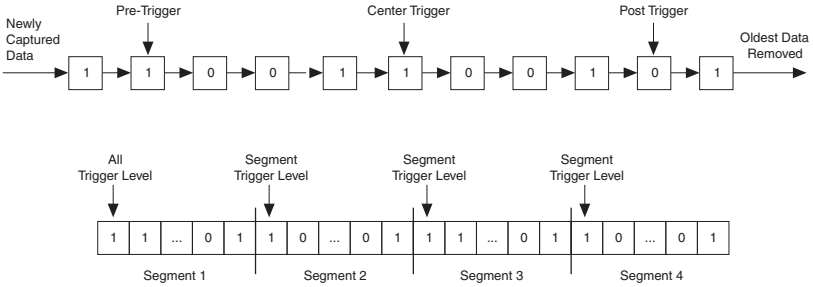
When you use the SignalTap II Logic Analyzer with some devices, you have the option to select the RAM type where acquisition data is stored. RAM selection allows you to preserve a specific memory block for your design and allocate another portion of memory for SignalTap II data acquisition. For example, if your design implements a large buffering application such as a system cache, it is ideal to place this application into M-RAM blocks so that the remaining M512 or M4K blocks are used for SignalTap II data acquisition.

To select the RAM type to use for the SignalTap II buffer, select it from the **RAM type** list. Use this feature when the acquired data (as reported by the SignalTap II resource estimator) is not larger than the available memory of the memory type that you have selected in the FPGA.

Choosing the Buffer Acquisition Mode

The buffer acquisition type selection feature in the SignalTap II Logic Analyzer lets you choose how the captured data buffer is organized and can potentially reduce the amount of memory that is required for SignalTap II data acquisition. You can choose to use either a circular buffer, specifying how much data is captured before and after a trigger occurs, or a segmented buffer, useful for capturing triggers that occur periodically. Figure 12–9 illustrates the differences between the two buffer types.

Figure 12–9. Buffer Type Comparison in the SignalTap II Logic Analyzer



Circular Buffer

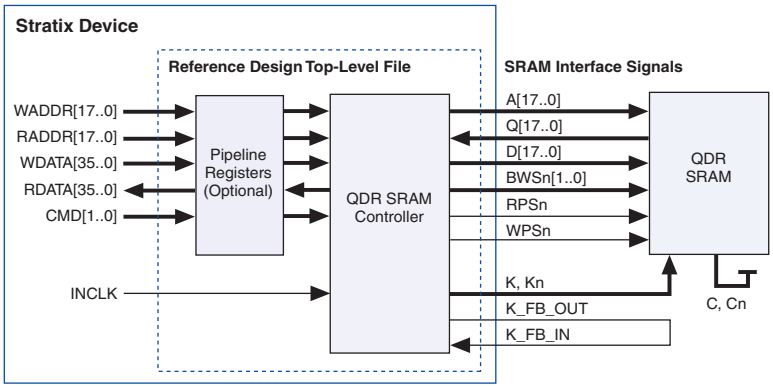
The circular buffer is the default buffer type used by the SignalTap II Logic Analyzer. While the logic analyzer is running, data is stored in the buffer until it fills up, at which point new data replaces the oldest data. This continues until a specified trigger event occurs. When this happens, the logic analyzer continues to capture data after the trigger event until the buffer is full, based on the circular buffer trigger position setting in the Signal Configuration pane in the SignalTap II file. Select a setting from the list to choose whether to capture the majority of the data before (**Post trigger position**) or after (**Pre trigger position**) the trigger occurs or to center the trigger position in the data (**Center trigger position).** You can also choose to continuously capture data until the logic analyzer is stopped.

For more information, refer to "Specifying the Trigger Position" on page 12–36.

Segmented Buffer

The segmented buffer organizes the buffer into a number of separate, evenly sized segments. This type of buffer organization makes it easier to debug systems that contain relatively infrequent periodic events. Figure 12–10 shows an example of this type of buffer system.

Figure 12–10. Example System that Generates Periodic Events



The SignalTap II Logic Analyzer verifies the functionality of the design shown in Figure 10–9 to ensure that the correct data is written to the SRAM controller. The buffer acquisition in the SignalTap II Logic Analyzer allows you to monitor the `RDATA` port when `H'0F0F0F0F` is sent into the `RADDR` port. You can monitor multiple read transactions from the SRAM device without running the SignalTap II Logic Analyzer again. The buffer acquisition feature allows you to segment the memory so that you can capture the same event multiple times without wasting the allocated memory. The number of cycles that are captured depends on the number of segments that you have specified in the **Signal Configuration** settings.

To enable and configure buffer acquisition, select **Segmented** in the SignalTap II window, and select the number of segments to use. In the example, selecting sixty-four 64-bit segments allows you to capture 64 read cycles when the `RADDR` signal is `H'0F0F0F0F`.

For more information on the buffer acquisition mode, refer to *Setting the Buffer Acquisition Mode* in the Quartus II Help.

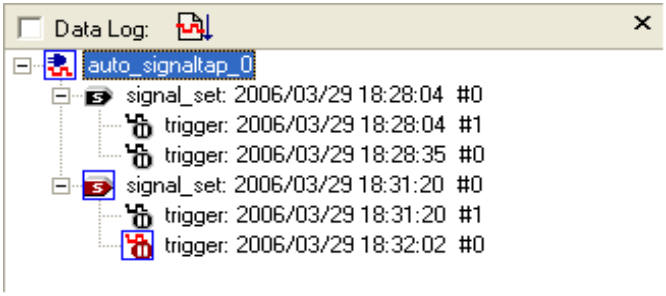
Managing Multiple SignalTap II Files & Configurations

In many instances, you can have more than one SignalTap II file in one design. Each file potentially has a different group of monitored signals. These signals groups make it possible to debug different blocks in your design. Along with each SignalTap II file, there is an associated programming file (SRAM Object File (SOF)). Managing all of the

SignalTap II files and their associated programming files is a challenging task. To help you manage these files, you can use the **Data Log** feature and the **SOF Manager**.

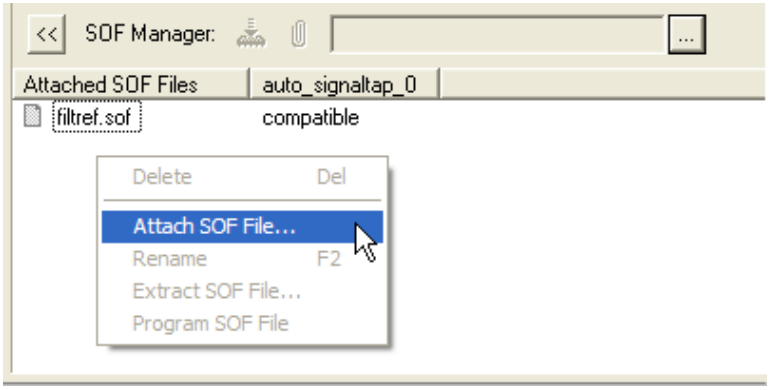
The **Data Log** allows you to store multiple SignalTap II configurations. Figure 12–11 shows two signal set configurations with multiple trigger conditions in one SignalTap II file. To toggle between the active configurations, double-click on an entry in the **Data Log**. As you toggle between the different configurations, the signal list and trigger conditions change in the **Setup** tab of the SignalTap II file. The active configuration displayed in the SignalTap II file is indicated by the blue square around the signal set in the **Data log**. To store a configuration in the data log, on the Edit menu, click **Save to Data Log,** or click **Save to Data Log** at the top of the Data Log.

Figure 12–11. Data Log



The SOF Manager allows you to embed multiple SOF into one SignalTap II file. To embed a new SOF in the SignalTap II file, right-click in the SOF Manager, and click **Attach** SOF **File** (Figure 12–12).

Figure 12–12. SOF Manager



As you switch between configurations in the Data Log, you can extract the SOF associated with that particular configuration and use the programmer in the SignalTap II Logic Analyzer to download the new SOF to the FPGA.

Define Triggers

To capture the data you want at the right time, you need to specify conditions under which the signals you are monitoring display that data. In the SignalTap II Logic Analyzer, these conditions are referred to as triggers, just as they are in conventional external logic analyzers and oscilloscopes. You have many options for creating different types of triggers to help in your debugging.

Creating Basic Triggers

The simplest kind of trigger you can use is a basic trigger. You select this from the list at the top of the **Trigger Levels** column in the node list in the SignalTap II file window. With the trigger type set to **Basic**, you must set the trigger pattern for each signal you've added in the SignalTap II file. To set the trigger pattern, right-click in the **Trigger Levels** column and click the desired pattern. You can set the trigger pattern to any of the following conditions:

- Don't Care
- Low
- High
- Falling Edge
- Rising Edge
- Either Edge

For buses, you can type in a pattern in binary, or right-click and select **Insert Value** to enter the pattern in other number formats. For signals added to the SignalTap II file through the use of a plug-in or any signals with an associated mnemonic table, you can right-click and select a mnemonic to set pre-defined conditions for the trigger. Data capture begins when the logical `AND` of all the signals for a given level evaluates to `TRUE`.

Creating Advanced Triggers

Along with the SignalTap II Logic Analyzer's basic triggering capabilities, you can build more complex triggers utilizing extra logic that enable you to capture data when a particular combination of conditions exist. If you set the trigger type to **Advanced** at the top of the **Trigger Levels** column in the node list of the SignalTap II file window, a new tab named **Advanced Trigger** appears where you can build a complex trigger expression using a simple GUI. You can drag and drop operators into the Advanced Trigger Configuration Editor window to build the complex trigger condition in an expression tree. Table 12–5 lists the operators you can use.

Table 12–5. Advanced Triggering Operators *Note (1)* ***(Part 1 of 2)***

Name of Operator	Type
Less Than	Comparison
Less Than or Equal To	Comparison
Equality	Comparison
Inequality	Comparison

Table 12–5. Advanced Triggering Operators Note (1) *(Part 2 of 2)*

Name of Operator	Type
Greater Than	Comparison
Greater Than or Equal To	Comparison
Logical NOT	Logical
Logical AND	Logical
Logical OR	Logical
Logical XOR	Logical
Reduction AND	Reduction
Reduction OR	Reduction
Reduction XOR	Reduction
Left Shift	Shift
Right Shift	Shift
Bitwise Complement	Bitwise
Bitwise AND	Bitwise
Bitwise OR	Bitwise
Bitwise XOR	Bitwise
Edge and Level Detector	Signal Detection
Continuous Counter	Counter
State Counter	Counter
Event Counter	Counter

Note to Table 12–5:
(1) For more information on each of these operators, refer to the Quartus II Help.

You can configure some of the operators at run time. This enables you to change one operator type to another operator type without recompiling your design. Operators that have a white background are run-time configurable.

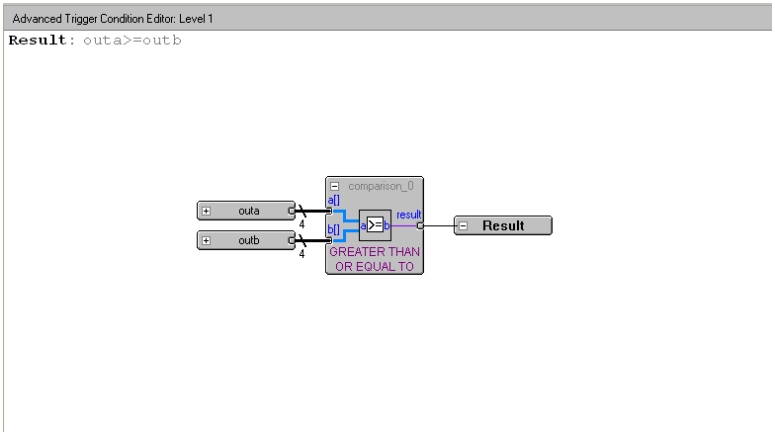
Adding many objects to the Advanced Trigger Condition Editor can make the workspace cluttered and difficult to read. To keep objects organized while you build your advanced trigger condition, use the right-click menu and select **Arrange All Objects**. You can also use the **Zoom-Out** command to fit more objects into the Advanced Trigger Condition editor window.

Examples of Advanced Triggering Expressions

The following examples show how to use Advanced Triggering:

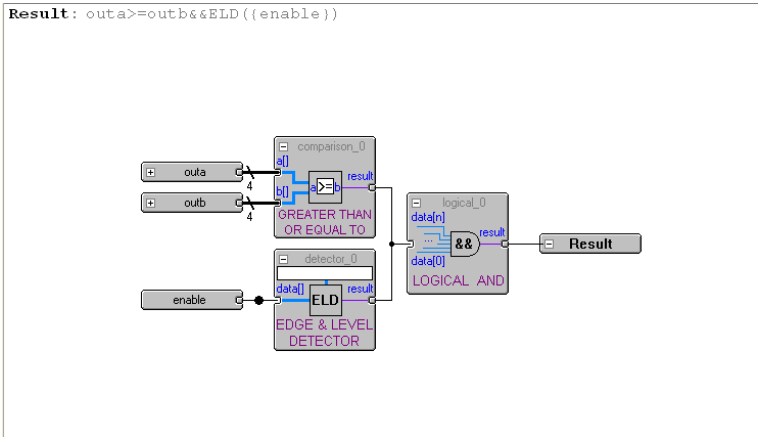
- Trigger when bus `outa` is greater than or equal to `outb` (Figure 12–13).

Figure 12–13. Bus outa is Greater Than or Equal to Bus outb



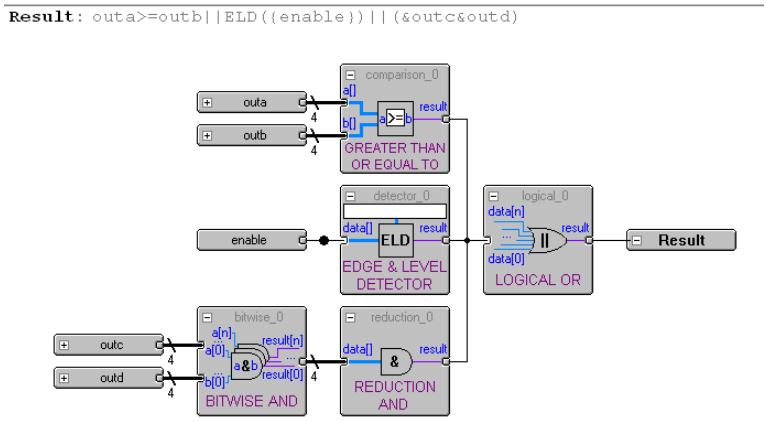
- Trigger when bus `outa` is greater than or equal to bus `outb`, and when the enable signal has a rising edge (Figure 12–14).

Figure 12–14. Enable Signal has a Rising Edge



- Trigger when bus `outa` is greater than or equal to bus `outb`, or when the enable signal has a rising edge. Or, when a bitwise `AND` operation has been performed with bus `outc` and bus `outd`, and all bits of the result of that operation are equal to 1 (Figure 12–15).

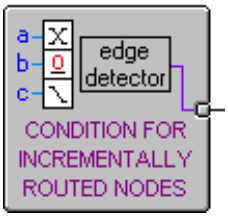
Figure 12–15. Bitwise AND Operation



Advanced Triggering Using Post-Fitting & Incrementally Routed Pre-Synthesis Nodes

If you are not using the Quartus II Incremental Compilation feature on your design, you can use the advanced triggering capability only with pre-synthesis nodes that are not set to be incrementally routed. Post-fitting nodes and incrementally routed pre-synthesis nodes are only used for basic trigger operations. However, you can create an advanced trigger that uses the results of a basic trigger created with post-fitting and incrementally routed pre-synthesis nodes. Set the trigger type to **Basic** and create basic trigger settings for the post-fitting and incrementally routed pre-synthesis nodes, then set the trigger type to **Advanced**. The post-fitting and incrementally routed pre-synthesis nodes are not shown in the node list in the **Advanced Trigger** tab, but a special symbol is automatically placed in the Advanced Trigger Condition Editor that represents the basic trigger you created (Figure 12–16).

Figure 12–16. Symbol for SignalTap II File Containing Post-Fitting Nodes



The output of this node can be combined with any of the operators listed in Table 12–5.

The special symbol for post-fitting and incrementally routed pre-synthesis nodes is only shown when you are not using the Quartus II incremental compilation feature on your design. If you are using incremental compilation, pre-synthesis nodes that were not preserved through synthesis to become post-fitting nodes are not available for monitoring or triggering. However, with incremental compilation, all post-fitting nodes are available for advanced triggering and appear in the node list in the **Advanced Trigger** tab. To learn about the use of incremental compilation with SignalTap II, refer to "Faster Compilations Using SignalTap II Incremental Compilation" on page 12–40.

For information about using the incremental routing feature in the SignalTap II Logic Analyzer, refer to the Quartus II Help.

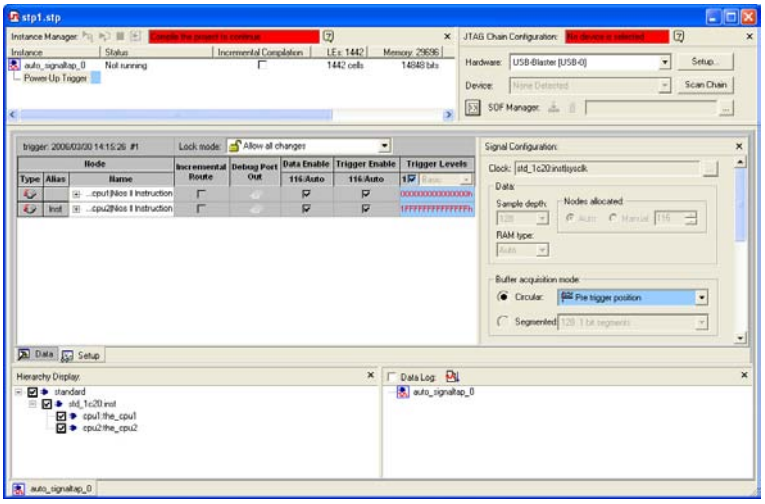
Creating a Power-Up Trigger

Typically, the SignalTap II Logic Analyzer is used to trigger on events that occur during normal device operation. You start an analysis manually once the target device is fully powered on and the device's JTAG connection is available. However, there may be cases when you would like to capture trigger events that occur during device initialization immediately after the FPGA is powered on or reset. With the SignalTap II Power-Up Trigger feature, you can capture data from triggers that occur after device programming but before the logic analyzer is started manually.

Enabling a Power-Up Trigger

A different Power-Up Trigger can be added to each logic analyzer instance in the SignalTap II Instance Manager. To enable the Power-Up Trigger for a logic analyzer instance, right-click the instance, and click **Enable Power-Up Trigger**, or select the instance, and on the Edit menu, click **Enable Power-Up Trigger**. To disable a Power-Up Trigger, click **Disable Power-Up Trigger in** the same locations. **Power-Up Trigger** is shown as a child instance below the name of the selected instance with the default trigger conditions set in the node list. Figure 12–17 shows the SignalTap II file window when a Power-Up Trigger is enabled.

Figure 12–17. SignalTap II File Window with Power-Up Trigger Enabled



Managing & Configuring Power-Up & Run-Time Trigger Conditions

When the Power-Up Trigger is enabled for a logic analyzer instance, you create basic and advanced trigger conditions for it in the same way you do with the regular trigger, also called the Run-Time Trigger. Power-Up Trigger conditions that you can adjust are color coded light blue, while Run-Time Trigger conditions remain white. Since each instance now has two sets of trigger conditions, the Power-Up Trigger and the Run-Time Trigger, you can differentiate between the two with the color coding. To switch between the trigger conditions of the Power-Up Trigger and the Run-Time Trigger, double-click the instance name or the Power-Up Trigger name in the Instance Manager.

When setting the trigger conditions for the Power-Up Trigger, you can only make changes that would not normally require recompilation when made in the Run-Time Trigger conditions. You cannot make changes that would require a full recompile, such as adding signals, deleting signals, or changing between basic and advanced triggers. To perform these actions, switch to the Run-Time Trigger conditions. However, any change made to the Power-Up Trigger conditions requires the SignalTap II Logic Analyzer to be recompiled even if such a change in the Run-Time Trigger conditions does not require a recompilation.

While creating or making changes to the trigger conditions for the Run-Time Trigger or the Power-Up Trigger, you may want to copy these conditions to the other trigger. This makes it easy to look for the same trigger during both power-up and run-time. To do this, right-click the instance name or the Power-Up Trigger name in the Instance Manager, and click **Duplicate Trigger**, or select the instance name or the Power-Up Trigger name and, on the Edit menu, click **Duplicate Trigger**. For information about running the SignalTap II Logic Analyzer instance with a Power-Up Trigger enabled, refer to "Running with a Power-Up Trigger" on page 12–47.

Using Multiple Trigger Levels

The multiple trigger level feature gives you precise control over the trigger conditions that you build. This feature enables you to give more complex data capture commands to the logic analyzer, providing greater accuracy and problem isolation. You can create up to ten trigger levels.

The SignalTap II Logic Analyzer first evaluates the trigger patterns associated with **trigger level 1**. When the expression for **trigger level 1** evaluates to `TRUE`, the logic analyzer evaluates the expression for **trigger level 2**. This process continues until all trigger levels are processed and the final trigger level evaluates to `TRUE`. You can use the multiple trigger level feature with basic triggers, advanced triggers, or a mix of both.

Select the desired number of trigger levels in the **Trigger Levels** list when viewing Run-Time Trigger conditions. You cannot adjust the number of trigger levels when viewing a Power-Up Trigger. Switch to the Run-Time Trigger conditions to make this change. The number of Trigger levels is always the same between the Run-Time Trigger and a Power-Up Trigger. If you do not require an extra trigger level in either the Run-Time or Power-Up Triggers, disable the trigger level. To disable a level, turn off the desired **Trigger Level** column by clicking on the checkbox at the top of the column in the node list.

Specifying the Trigger Position

When using the circular buffer acquisition mode, you can specify the amount of data that is acquired before and after a trigger event. You can set the trigger position independently between a Run-Time and Power-Up Trigger. Select the desired ratio of pre-trigger data to post-trigger data by selecting one of the following ratios:

- **Pre—**This selection saves signal activity that occurred after the trigger (12% pre-trigger, 88% post-trigger).
- **Center—**This selection saves 50% pre-trigger and 50% post-trigger data.
- **Post—**This selection saves signal activity that occurred before the trigger (88% pre-trigger, 12% post-trigger).
- **Continuous**—This selection saves signal activity indefinitely (until stopped manually).

Using External Triggers

You can create a trigger input that allows you to trigger the SignalTap II Logic Analyzer from an external source. The analyzer can also supply a signal to trigger external devices or other SignalTap II instances. These features enable you to synchronize external logic analysis equipment with the internal logic analyzer. Power-Up Triggers can use the external triggers feature, but they must use the same source or target signal as their associated Run-Time Trigger.

Trigger In

To use Trigger In, perform the following steps:

1. In the **SignalTap II** window, click the **Setup** tab.
2. If a Power-Up Trigger is enabled, make sure you are viewing the Run-Time Trigger conditions.
3. In the Signal Configuration pane, turn on **Trigger In**.
4. In the **Pattern** list, select the condition you want to act as your trigger event. You can set this separately for a Run-Time or a Power-Up Trigger.
5. Click **Browse** next to the **Source** field in the Trigger In pane (Figure 12–19 on page 12–39). The **Node Finder** dialog box appears.

6. In the **Node Finder** dialog box, select the signal (either an input pin or an internal signal) that you want to drive the Trigger In source, and click **OK**.

Trigger Out

To use Trigger Out, perform the following steps:

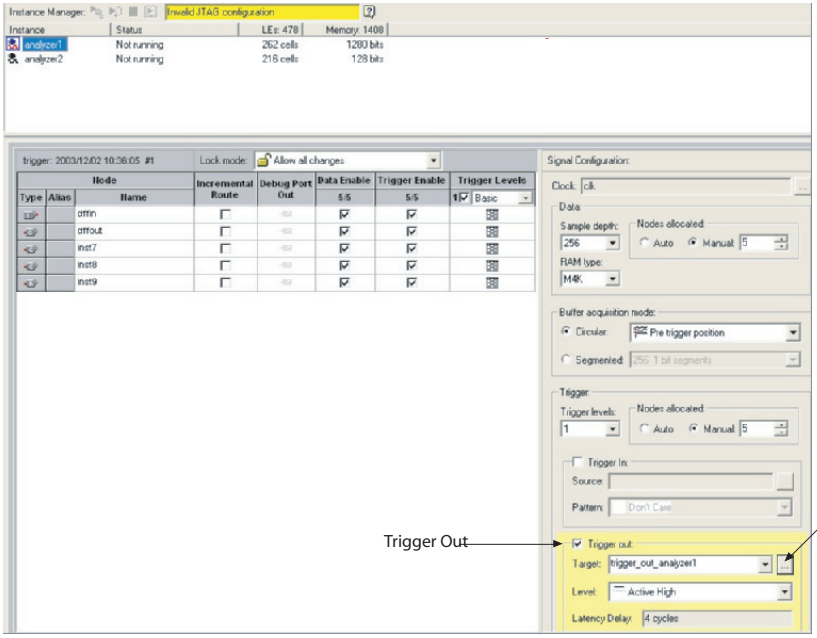
1. In the **SignalTap II** dialog box, click the **Setup** tab.
2. If a Power-Up trigger is enabled, make sure you are viewing the Run-Time Trigger conditions.
3. In the Signal Configuration pane, turn on **Trigger Out**.
4. In the **Level** list, select the condition you want to signify that the trigger event is occurring. You can set this separately for a Run-Time or a Power-Up Trigger.
5. Click **Browse** next to the **Target** field in the Trigger Out pane (Figure 12–18). The **Node Finder** dialog box appears.
6. In the **Node Finder** dialog box, select the signal (either an output pin or an internal signal) that you want to drive the Trigger Out, and click **OK**.

Using the Trigger Out of One Analyzer as the Trigger In of Another Analyzer

An advanced feature of the SignalTap II Logic Analyzer is the ability to use the Trigger Out of one analyzer as the Trigger In to another analyzer. This feature allows you to synchronize and debug events that occur across multiple clock domains.

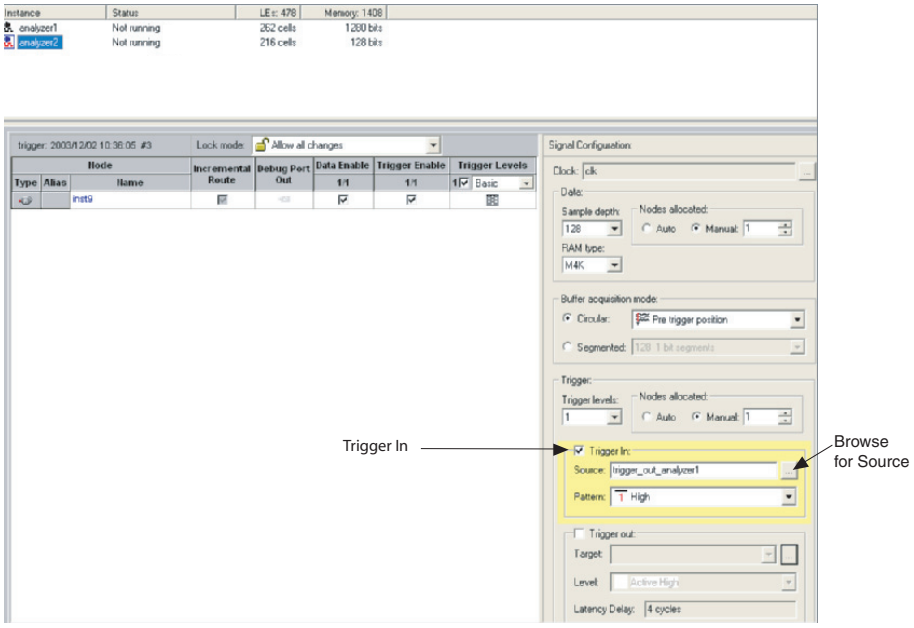
To perform this operation, first enable the **Trigger Out** of the first analyzer and specify the name for the Trigger Out signal (Figure 12–18).

Figure 12–18. Enabling the Trigger Out Signal



Next, turn on the **Trigger In** of the second analyzer, and specify the name of the Trigger In of the second analyzer as the Trigger Out of the first analyzer (Figure 12–19).

Figure 12–19. Enabling the Trigger In Signal



Compile the Design

When you add a SignalTap II file to your project, the SignalTap II Logic Analyzer becomes part of your design. Because of this, you must compile your project to incorporate the SignalTap II logic and enable the JTAG connection that is used to control the logic analyzer. When you are debugging with a traditional external logic analyzer, it is often necessary to make changes to the signals monitored as well as the trigger conditions. Since these types of adjustments often translate into recompilation time when using the SignalTap II Logic Analyzer, you can use the SignalTap II Incremental Compilation feature along with incremental compilation in the Quartus II software to reduce time spent recompiling.

Compiling without Incremental Compilation

Once you've configured your SignalTap II file and defined triggers, compile your project to incorporate the SignalTap II Logic Analyzer. On the Processing menu, click **Start Compilation,** or click **Start Compilation** on the toolbar to begin the compilation.

When you compile your design with a SignalTap II file, the `sld_signaltap` and `sld_hub` entities are automatically added to the compilation hierarchy. These two entities are the main components of the SignalTap II Logic Analyzer, providing the JTAG interface required for operation.

You can prevent full recompilations when incremental compilation is not used by using the SignalTap II incremental routing feature. With this feature, you add extra post-fitting nodes to the node list during the debugging process by reserving them ahead of time for incremental routing. You can also replace existing pre-synthesis nodes later with post-fitting nodes by enabling the pre-synthesis nodes for incremental routing.

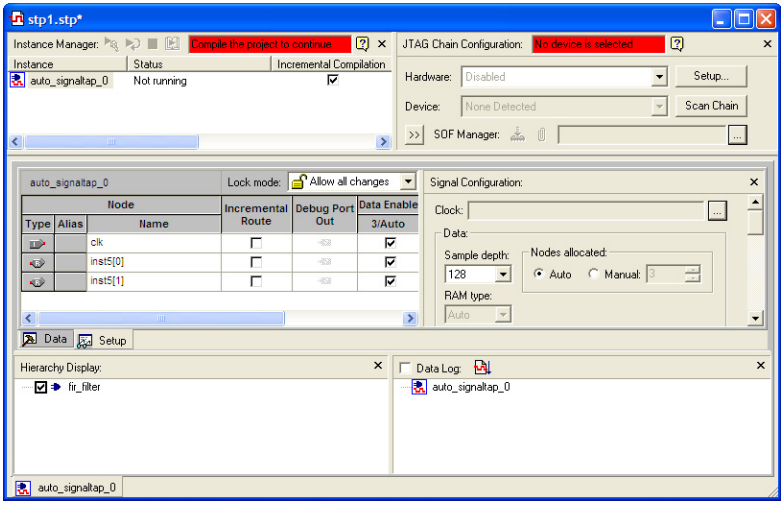
For information about using the SignalTap II Incremental Routing feature, refer to the Quartus II Help.

Faster Compilations Using SignalTap II Incremental Compilation

SignalTap II Incremental Compilation enables you to preserve the synthesis and fitting results of your original design and add the SignalTap II Logic Analyzer to your design without recompiling your original source code. This feature is also useful when you want to modify the configuration of the SignalTap II file. For example, you can modify the buffer sample depth or memory type without performing a full compilation after the change is made. Only the SignalTap II Logic Analyzer, configured as its own design partition, needs to be recompiled.

To use SignalTap II Incremental Compilation, you must first enable Full Incremental Compilation for your design and assign design partitions. Once your design is set up to use full incremental compilation, you enable the SignalTap II Incremental Compilation function in the SignalTap II file (Figure 12–20). This turns the SignalTap II Logic Analyzer into its own separate design partition.

Figure 12–20. SignalTap II File with Incremental Compilation



Enable Incremental Compilation for your Design

To enable Incremental Compilation, perform the following steps:

1. On the Assignments menu, click **Design Partitions window**.
2. In the **Incremental Compilation** list, select **Full Incremental Compilation**.
3. Create user-defined partitions and set the **Netlist Type** to **Post-fit**.
4. On the Processing menu, click **Start Compilation,** or click **Start Compilation** on the toolbar.

Your project is fully compiled the first time, establishing the design partitions you've created.

For more information on performing Incremental Compilation, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*.

Enable SignalTap II Incremental Compilation

To enable the SignalTap II Incremental Compilation, perform the following steps:

1. For each instance in your SignalTap II file, turn on **Incremental Compilation** in the Instance Manager.

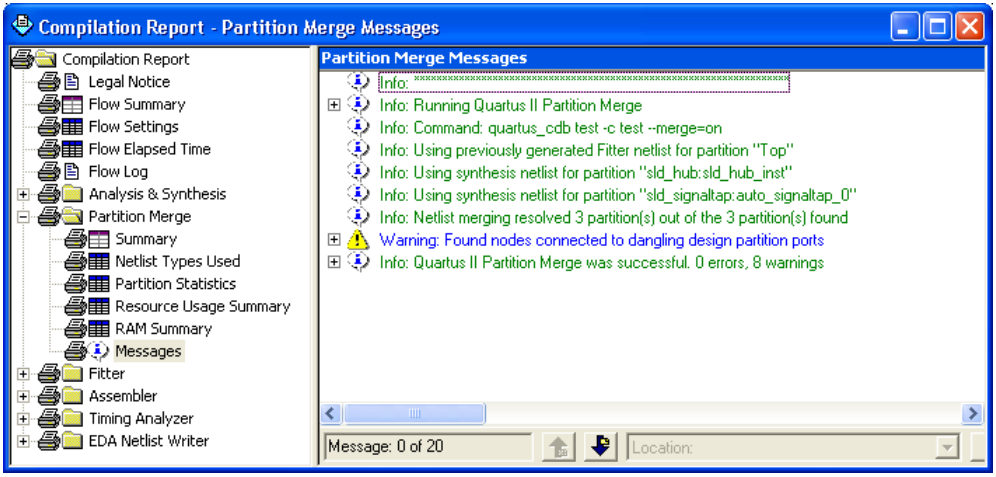
When you enable Incremental Compilation, all existing pre-synthesis signals are converted into post-fitting signals. You can use only post-fitting signals with the SignalTap II Incremental Compilation feature. Any pre-synthesis signals that do not have post-fitting equivalents or have not been preserved with synthesis attributes become invalid, indicated by the signal name color changing to red. Invalid signals must be removed from the node list before you can perform a successful compilation.

2. Add SignalTap II Post-Fitting nodes to your SignalTap II file.

3. On the Processing menu, click **Start Compilation**, or click **Start Compilation** on the toolbar.

To verify that your original design was not modified, examine the messages in the Partition Merge section of the Compilation Report. Figure 12–21 shows an example of the messages displayed.

Figure 12–21. Compilation Report Messages



Unless you make changes to your design partitions that require recompilation, only the SignalTap II design partition is recompiled. If you make subsequent changes to only the SignalTap II file, only the SignalTap II design partition must be recompiled, reducing your recompilation time.

Preventing Changes Requiring Recompilation

You can configure the SignalTap II file to prevent changes that normally require a recompilation. You do this by setting a lock mode in the node list in the **Setup** tab. If you are not using incremental compilation, you can lock your configuration by choosing to allow only incremental routing changes or only trigger condition changes. With incremental compilation enabled, there are no incrementally routed nodes, so the only lock mode available prevents any configuration changes other than changes to the basic trigger conditions.

For more information about the use of lock modes, see Quartus II Help.

Timing Preservation with the SignalTap II Logic Analyzer

In addition to verifying functionality, timing closure is one of the most crucial processes in successfully completing a design. When you compile a project with a SignalTap II Logic Analyzer without the use of incremental compilation, you add IP to your existing design. Therefore, you can affect the existing placement, routing, and timing of your design. To minimize the effect that the SignalTap II Logic Analyzer has on your design, Altera recommends that you use incremental compilation for your project. With the SignalTap II Logic Analyzer in its own design partition, it has little to no affect on your design. If incremental compilation cannot be implemented in your design, back-annotate your design prior to inserting the SignalTap II Logic Analyzer. Back-annotation minimizes the impact of the logic analyzer on your design performance.

Besides back-annotating your design, you can use the following techniques to help maintain timing:

- Avoid adding critical path signals to your SignalTap II file.
- Minimize the number of signals that have Trigger Enable selected. By default, all of the signals that you add to the SignalTap II file have the Trigger Enable turned on. Turn off Trigger Enable for signals you do not plan to use as triggers.
- Use the Basic Trigger whenever possible. Using the Advanced Trigger increases the amount of logic, which may add extra delay to your circuit.

- Minimize the number of combinational signals you add to your SignalTap II file, and add registers whenever possible.
- Specify an f_{MAX} constraint for each clock in your design.
- Back-annotate your design prior to compiling with the SignalTap II Logic Analyzer.

For an example of timing preservation with the SignalTap II Logic Analyzer, refer to *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

Program the Target Device(s)

Once your project including the SignalTap II Logic Analyzer is compiled, you must configure the FPGA target device. When you are using the SignalTap II Logic Analyzer for debugging, you configure the device from the SignalTap II file instead of the Quartus II Programmer. Because you configured from the SignalTap II file, you can open more than one SignalTap II file and program multiple devices to debug multiple designs simultaneously.

Programming a Single Device

To configure a single device for use with the SignalTap II Logic Analyzer perform the follow steps:

1. In the **JTAG Chain Configuration** pane in the SignalTap II file window, select the connection you use to communicate with the device from the **Hardware** list. If you need to add your communication cable to the list, click **Setup** to configure your connection.
2. **Browse** to and select the SOF file that includes the SignalTap II Logic Analyzer in the **JTAG Chain Configuration** panel.
3. Click **Scan Chain**.
4. In the **Device** list, select the device to which you want to download the design.
5. Click the **Program Device** icon.

Programming Multiple Devices to Debug Multiple Designs

You can simultaneously debug multiple designs using one instance of the Quartus II software by performing the following steps:

1. Create, configure, and compile each project that includes a SignalTap II file.

2. Open each SignalTap II file.

   You do not have to open a Quartus II project to open a SignalTap II file.

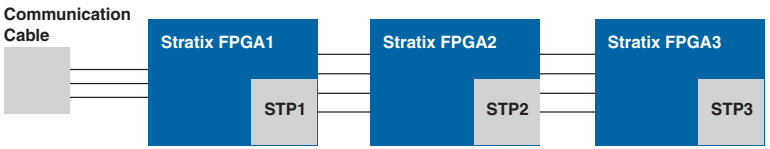
3. Use the **JTAG Chain Configuration** panel controls to select the target device in each SignalTap II file.

4. Program each FPGA.

5. Run each analyzer independently.

Figure 12–22 shows a JTAG chain and its associated SignalTap II files.

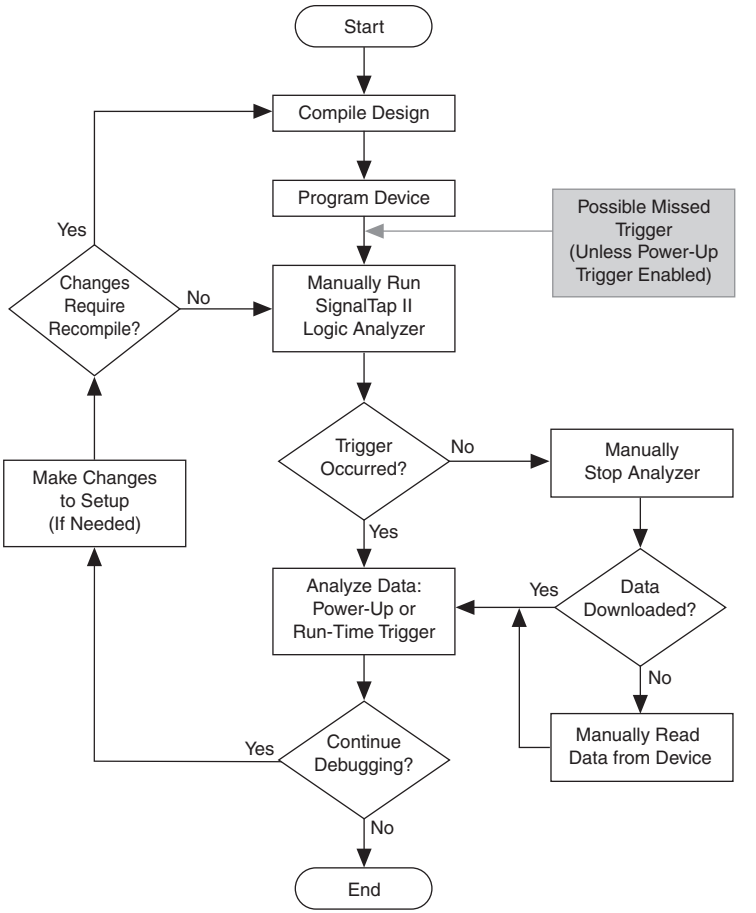
Figure 12–22. JTAG Chain



Run the SignalTap II Logic Analyzer

After the device is configured with your design that includes the SignalTap II Logic Analyzer, you can perform debugging operations in a manner similar to the use of an external logic analyzer. You "arm" the logic analyzer by starting an analysis. When your trigger event occurs, the captured data is stored in the memory buffer on the device and then transferred to the SignalTap II file over the JTAG connection. You can also perform the equivalent of a "force trigger" that lets you view the captured data currently in the buffer without a trigger event occurring. Figure 12–23 illustrates a flow that shows how you operate the SignalTap II Logic Analyzer. The flowchart indicates where Power-Up and Run-Time Trigger events occur and when captured data from these events is available for analysis.

Figure 12–23. Power-Up & Run-Time Trigger Events Flowchart



The SignalTap II toolbar in the Instance Manager has four options for running the analyzer:

- **Run Analysis**—The SignalTap II Logic Analyzer runs until the trigger event occurs. When the trigger event occurs, monitoring and data capture stops once the acquisition buffer is full.
- **AutoRun Analysis**—The SignalTap II Logic Analyzer continuously captures data until the **Stop Analysis** button is clicked, ignoring all trigger event conditions.
- **Stop Analysis**—SignalTap II analysis stops. The acquired data does not appear automatically if the trigger event has not occurred.
- **Read Data**—Captured data is displayed. This button is useful if you want to view the acquired data even if the trigger has not occurred.

Running with a Power-Up Trigger

If you have enabled and set up a Power-Up Trigger for an instance of the SignalTap II Logic Analyzer, the captured data may already be available for viewing if the trigger event occurred after device configuration. To download the captured data or to check if the Power-Up Trigger is still running, click **Run Analysis** in the Instance Manager. If the Power-Up Trigger occurred, the logic analyzer immediately stops, and the captured data is downloaded from the device. The data can now be viewed on the **Data** tab of the SignalTap II file window. If the Power-Up Trigger did not occur, no captured data is downloaded, and the logic analyzer continues to run. You can wait for the Power-Up Trigger event to occur, or, to stop the logic analyzer, click **Stop Analysis**.

Running with Run-Time Triggers

You can arm and run the SignalTap II Logic Analyzer manually after device configuration to capture data samples based on the Run-Time Trigger. You can do this immediately if there is no Power-Up Trigger enabled. If a Power-Up Trigger is enabled, you can do this after the Power-Up Trigger data is downloaded from the device or once the logic analyzer is stopped because the Power-Up Trigger event did not occur. Click **Run Analysis** in the SignalTap II window to start monitoring for the trigger event. You can start multiple SignalTap II instances at the same time by selecting all of the required instances before you click **Run Analysis** on the toolbar.

Unless the logic analyzer is stopped manually, data capture begins when the trigger event evaluates to `TRUE`. When this happens, the captured data is downloaded from the buffer. You can view the data in the **Data** tab of the SignalTap II file window.

Performing a Force Trigger

Sometimes when you use an external logic analyzer or oscilloscope, you want to see the current state of signals without setting up or waiting for a trigger event to occur. This is referred to as a "force trigger" operation because you are forcing the test equipment to capture data without regard to any set trigger conditions. With the SignalTap II Logic Analyzer, you can choose to run the analyzer and capture data immediately or run the analyzer and capture data when you want.

To run the analyzer and immediately capture data, disable the trigger conditions in all trigger levels by turning off each **Trigger Level** column in the node list. This operation does not require a recompilation. Click **Run Analysis** in the Instance Manager. The SignalTap II Logic Analyzer immediately triggers, captures, and downloads the data to the **Data** tab of the SignalTap II file window. If the data does not download automatically, click **Read Data** in the Instance Manager.

If you want to choose when to capture data manually, it is not required that you disable the trigger conditions. Click **Autorun Analysis** to start the logic analyzer, and click **Stop Analysis** to capture data. If the data does not download to the **Data** tab of the SignalTap II file window automatically, click **Read Data**.

Finally, you can choose to capture data manually after a trigger event has occurred. This is useful if you still want the trigger event to occur, but you want to capture data about the signals at some point after the trigger without capturing the trigger event itself. To do this, set the **Buffer acquisition mode** to **Circular** and **Continuous**, and click **Run Analysis**. When the trigger event occurs, the status in the SignalTap II Health Monitor is shown as `Acquiring post-trigger data`, but the logic analyzer does not stop. When you want to capture and download the data, click **Stop Analysis**. If the data does not download automatically, click **Read Data**.

SignalTap II Status Messages

Table 12–6 describes the text messages that may appear in the SignalTap II Health Monitor in the Instance Manager before, during, and after a data acquisition. Use these messages to know the state of the logic analyzer or what operation it is performing.

Table 12–6. Text Messages in the SignalTap II Health Monitor

Message	Message Description
`Not running`	The SignalTap II Logic Analyzer is not running. There is no connection to a device or the device is not configured.
`(Power-Up Trigger) Waiting for clock` *(1)*	The SignalTap II Logic Analyzer is performing a Run-Time or Power-Up Trigger acquisition and is waiting for the clock signal to transition.
`Acquiring (Power-Up) pre-trigger data` *(1)*	The trigger condition has not been evaluated yet. A full buffer of data is collected if the circular buffer acquisition mode is selected.
`Trigger In conditions met`	Trigger In condition has occurred. The SignalTap II Logic Analyzer is waiting for the condition of the first trigger level to occur. This can appear if Trigger In is specified.
`Waiting for (Power-up) trigger` *(1)*	The SignalTap II Logic Analyzer is now waiting for the trigger event to occur.
`Trigger level <x> met`	The condition of trigger level x has occurred. The SignalTap II Logic Analyzer is waiting for the condition specified in level x+1 to occur.
`Acquiring (power-up) post-trigger data` *(1)*	The whole trigger event has occurred. The SignalTap II Logic Analyzer is acquiring the post-trigger data. The amount of post-trigger data collected is user-defined between 12%, 50%, and 88% when the circular buffer acquisition mode is selected.
`Offload acquired (Power-Up) data` *(1)*	Data is being transmitted to the Quartus II software through the JTAG chain.
`Ready to acquire`	The SignalTap II Logic Analyzer is waiting for the user to arm the analyzer.

Note to Table 12–6:
(1) This message can appear for both Run-Time and Power-Up Trigger events. When referring to a Power-Up Trigger, the text in parentheses is added.

In segmented acquire mode, pre-trigger and post-trigger do not apply.

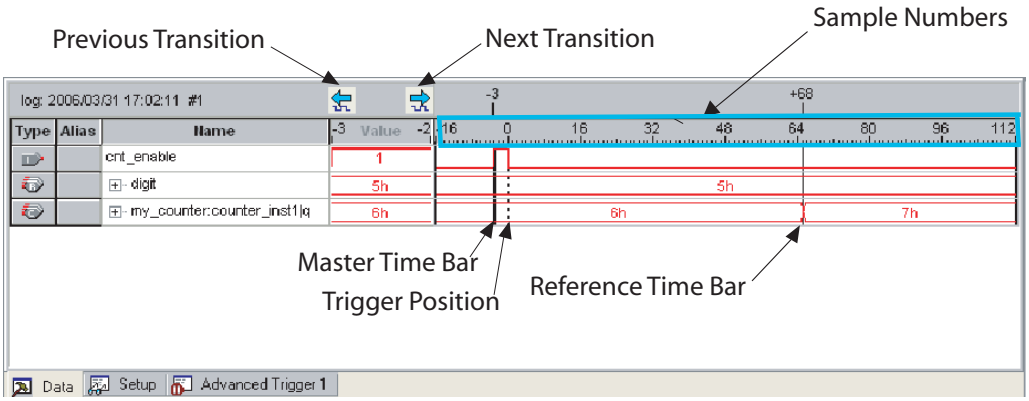
View, Analyze & Use Captured Data

Once a trigger event has occurred or you capture data manually, you can use the SignalTap II interface to examine the data, and use your findings to help debug your design. The SignalTap II Logic Analyzer provides a number of features that makes it easy to do this.

Viewing Captured Data

You can view captured SignalTap II data in the **Data** tab of the SignalTap II file (Figure 12–24). Each row of the **Data** tab displays the captured data for one signal or bus. Buses can be expanded to show the data for each individual signal on the bus. Click on the data waveforms to zoom in on the captured data samples, and right-click to zoom out.

Figure 12–24. Captured SignalTap II Data



When you are viewing captured data, it is often useful to know the time interval between two events. Time bars enable you to see the number of clock cycles between two samples of captured data in your system. There are two types of time bars:

- **Master Time Bar**—The master time bar's label displays the absolute time of its location in bold. The master time bar is a thick black line in the **Data** tab. The captured data has only one master time bar.
- **Reference Time Bar**—The reference time bar's label displays the time relative to the master time bar. You can create an unlimited number of reference time bars.

To help you find a transition of signals relative to the master time bar location, use either the **Next Transition** or the **Previous Transition** button. This lines the master time bar up with the next or previous

transition of a selected signal or group of selected signals. This feature is very useful when the sample depth is very large and the rate at which signals toggle is very low.

Creating Mnemonics for Bit Patterns

The mnemonic table feature allows you to assign a meaningful name to a set of bit patterns, such as a bus. To create a mnemonic table, right-click in the **Setup** or **Data** tab of a SignalTap II file, and click **Mnemonic Table Setup**. You create a mnemonic table by entering sets of bit patterns and specifying a label to represent each pattern. Once you have created a mnemonic table, you assign it to a group of signals. To assign a mnemonic table, right-click on the group, click **Bus Display Format**, and select the desired mnemonic table.

Automatic Mnemonics with a Plug-In

When you use a plug-in to add signals to a SignalTap II file, mnemonic tables for the added signals are automatically created and assigned to the signals defined in the plug-in. If you ever need to manually enable these mnemonic tables, right-click on the name of the signal or signal group. On the **Bus Display Format** submenu, click the name of the mnemonic table that matches the plug-in.

Locating a Node in the Design

When you find the source of a bug in your design using the SignalTap II Logic Analyzer, you can use the node locate feature to locate that signal in many of the tools found in the Quartus II software, as well as in your design files. This lets you find the source of the problem quickly so you can modify your design to correct the flaw. To locate a signal from the SignalTap II Logic Analyzer in one of the Quartus II software tools or your design files, right-click on the signal in the SignalTap II file, and click **Locate in** <*tool name*>. You can locate a signal from the node list in any of the following locations:

- Assignment Editor
- Pin Planner
- Timing Closure Floorplan
- Chip Editor
- Resource Property Editor
- Technology Map Viewer
- RTL Viewer
- Design File

For more information on using these tools, refer to the appropriate chapters in the *Quartus II Handbook*.

Saving Captured Data

The data log shows the history of captured data and the triggers used to capture the data. The analyzer acquires data, stores it in a log, and displays it as waveforms. When the logic analyzer is in auto-run mode and a trigger event occurs more than once, captured data for each time the trigger occurred is stored as a separate entry in the data log. This makes it easy to go back and review the captured data for each trigger event. The default name for a log is based on the time when the data was acquired. Altera recommends that you rename the data log with a more meaningful name.

The logs are organized in a hierarchical manner; similar logs of captured data are grouped together in trigger sets. To enable data logging, turn on the checkbox in the **Data Log** of the SignalTap II file. To recall a data log for a given trigger set and make it active, double-click the name of the data log in the list.

The Data Log feature is useful for organizing different sets of trigger conditions and different sets of signal configurations. Refer to "Managing Multiple SignalTap II Files & Configurations" on page 12–26.

Converting Captured Data to Other File Formats

You can export captured data in the following file formats, some of which can be used with other EDA simulation tools:

- Comma Separated Values File (**.csv**)
- Table File (**.tbl)**
- Value Change Dump File (**.vcd**)
- Vector Waveform File (**.vwf**)
- Graphics format files (**.jpg**, **.bmp**)

To export the SignalTap II Logic Analyzer's captured data, on the File menu, click **Export** and specify the **File Name**, the **Export Format**, and the **Clock Period**.

Creating a SignalTap II List File

Captured data can also be viewed in a SignalTap II list file. A SignalTap II list file is a text file that lists all the data captured by the logic analyzer for a trigger event. Each row of the list file corresponds to one captured sample in the buffer. Columns correspond to the value of each of the captured signals or signal groups for that sample. If a mnemonic table was created for the captured data, the numerical values in the list are replaced with a matching entry from the table. This is especially useful with the use of a plug-in that includes instruction code disassembly. You can immediately see the order by which the instruction code was executed around the time of the trigger event. To create a SignalTap II list file, on the File menu, select **Create/Update,** and click **Create SignalTap II List File**.

Other Features

The SignalTap II Logic Analyzer has a number of other features that do not necessarily belong to a particular task in the task flow.

Using the SignalTap II MATLAB MEX Function to Capture Data

If you use MATLAB for DSP design, you can call the MATLAB MEX function `alt_signaltap_run`, built into the Quartus II software, to acquire data from the SignalTap II Logic Analyzer directly into a matrix in the MATLAB environment. If you use the MEX function repeatedly in a loop, you can perform as many acquisitions as you can when using SignalTap II in the Quartus II software environment in the same amount of time.

The SignalTap II MATLAB MEX function is available only in the Windows version of the Quartus II software.

To set up the Quartus II software and the MATLAB environment to perform SignalTap II acquisitions, perform the following steps:

1. In the Quartus II software, create a SignalTap II file.
2. In the node list in the **Data** tab of the SignalTap II file window, organize the signals and groups of signals into the order in which you want them to appear in the MATLAB matrix. Each row of the imported matrix represents a single SignalTap II acquisition sample, while each column represents a signal or group of signals in the order they are organized in the **Data** tab.

Signal groups acquired into the MATLAB environment with the MEX function are limited to a width of 32 bits. If you want to use the MEX function with a bus or signal group that is more than 32 bits wide, split the group up into smaller groups that do not exceed the 32 signal limit.

3. Save the SignalTap II file and compile your design. Program your device and run the SignalTap II Logic Analyzer to make sure your trigger conditions and signal acquisition are working correctly.

4. In the MATLAB environment, add the Quartus II binary directory to your path with the following command:

```
addpath <Quartus install directory>\win ↵
```

You can view the help file for the MEX function by entering `alt_signaltap_run` in MATLAB without any operators.

You use the MEX function in the MATLAB environment to open the JTAG connection to the device and run the SignalTap II Logic Analyzer to acquire data. When you finish acquiring data, you must close the connection.

To open the JTAG connection and begin acquiring captured data directly into a MATLAB matrix called **.stp**, use the following command:

```
stp = alt_signaltap_run('<stp filename>'[,('signed'|'unsigned')[,'<instance names>'[,/
'<signalset name>'[,'<trigger name>']]]]); ↵
```

When capturing data, you want to use a SignalTap II file named <*stp filename*>. This is required for using the MEX function. The other MEX function options are defined in Table 12–7.

Table 12–7. SignalTap II MATLAB MEX Function Options (Part 1 of 2)

Option	Usage	Description
`signed` `unsigned`	`'signed'` `'unsigned'`	The **signed** option turns signal group data into two's complement signed integers.The most significant bit of the group as defined in the SignalTap II **Data** tab is the sign bit.The **unsigned** option keeps the data as an unsigned integer. The default is **signed**.

Table 12–7. SignalTap II MATLAB MEX Function Options (Part 2 of 2)

Option	Usage	Description
<instance name>	'auto_signaltap_0'	Specify a SignalTap II instance if more than one instance is defined. The default is the first instance in the SignalTap II file, auto_signaltap_0.
<signal set name> *<trigger name>*	'my_signalset' 'my_trigger'	Specify the signal set and trigger from the SignalTap II data log if multiple configurations are present in the SignalTap II file. The default is the active signal set and trigger in the file.

You can enable or disable verbose mode to see the status of the logic analyzer while it is acquiring data. To enable or disable verbose mode, use the following commands:

```
alt_signaltap_run('VERBOSE_ON'); ↵
alt_signaltap_run('VERBOSE_OFF'); ↵
```

When you finish acquiring data, you must close the JTAG connection. Use the following command to close the connection:

```
alt_signaltap_run('END_CONNECTION'); ↵
```

For more information about the use of MEX functions in MATLAB, refer to the MATLAB Help.

Using SignalTap II in a Lab Environment

You can install a stand-alone version of the SignalTap II Logic Analyzer. This version is particularly useful in a lab environment where you do not have a workstation that meets the requirements for a complete Quartus II installation, or if you do not have a license for a full installation of the Quartus II software. The stand-alone version of the SignalTap II Logic Analyzer is included with the Quartus II stand-alone Programmer and is available from the Downloads page of the Altera web site, **www.altera.com**.

Remote Debugging Using the SignalTap II Logic Analyzer

You can use the SignalTap II Logic Analyzer to debug a design that is running on a device attached to a PC in a remote location.

To perform a remote debugging session, you must have the following setup:

- The Quartus II software installed on the local PC
- Stand-alone SignalTap II Logic Analyzer installed on the remote PC
- Programming hardware connected to the device on the PCB at the remote location
- TCP/IP protocol connection

Equipment Setup

On the PC, in the remote location, install the stand-alone version of the SignalTap II Logic Analyzer. This remote computer must have Altera programming hardware connected, such as the EthernetBlaster or USB-Blaster.

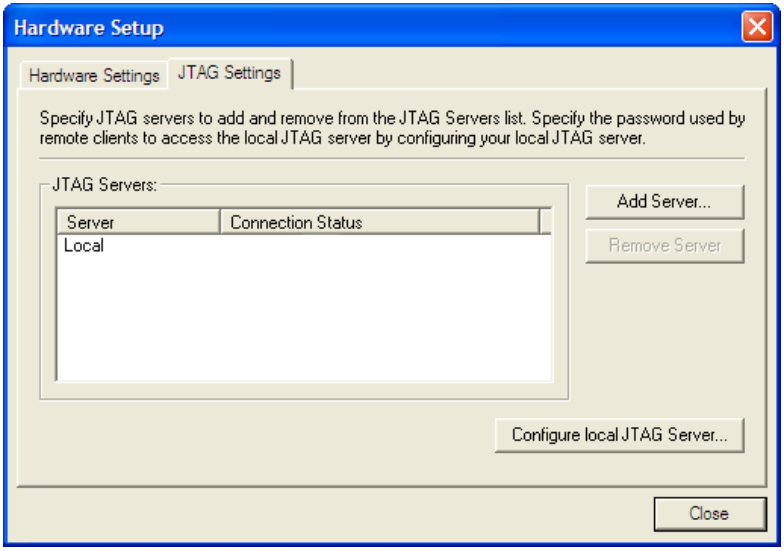
On the local PC, install the full version of the Quartus II software. This local PC must be connected to the remote PC across a LAN with the TCP/IP protocol.

Software Setup on the Remote PC

To setup the software on the remote PC, perform the following steps:

1. In the Quartus II programmer, click **Hardware Setup**.
2. Click the **JTAG Settings** tab (Figure 12–25).

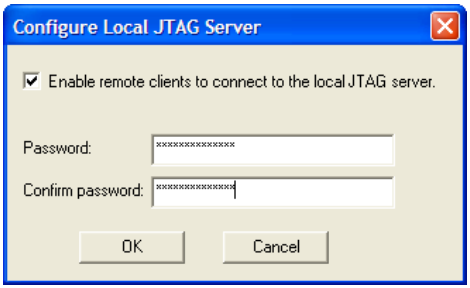
Figure 12–25. Configure JTAG on Remote PC



3. Click **Configure local JTAG server**.

4. In the **Configure Local JTAG Server** dialog box (Figure 10–25), turn on **Enable remote clients to connect to the local JTAG server,** and type your password in the password box. Type your password again in the **Confirm Password** box and click **OK**.

Figure 12–26. Configure Local JTAG Server on Remote



Software Setup on the Local PC

To set up your software on your local PC, perform the following steps:

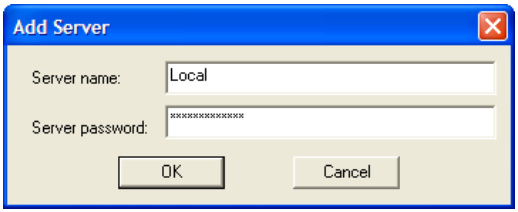
1. Launch the Quartus II programmer.

2. Click **Hardware Setup.**

3. On the **JTAG settings** tab, click **Add server**.

4. In the **Add Server** dialog box (Figure 12–27), type the network name or IP address of the server you want to use and the password for the JTAG server that you created on the remote PC.

Figure 12–27. Add Server Dialog Box



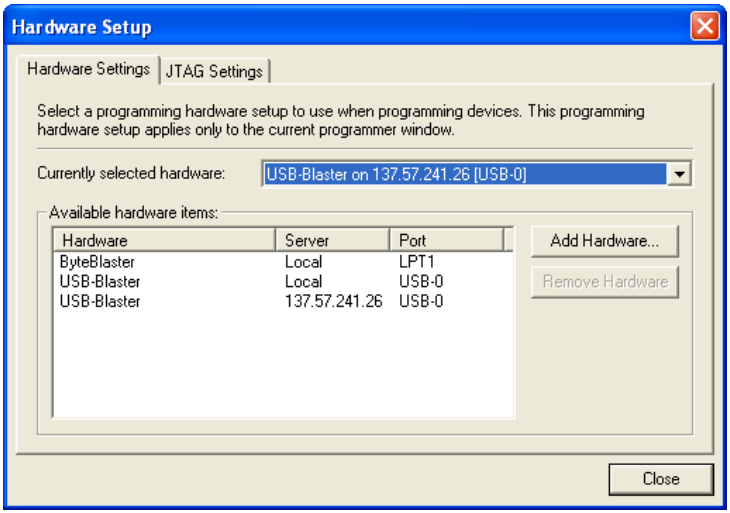
5. Click **OK**.

SignalTap II Setup on the Local PC

To connect to the hardware on the remote PC, perform the following steps:

1. Click the **Hardware Setup** tab and select the hardware on the remote PC (Figure 12–28).

Figure 12–28. Selecting Hardware on Remote PC



2. Click **Close**.

SignalTap II Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The *Quartus II Software Command-Line Operation & TCL Scripting Manual* includes the same information in PDF form. For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

SignalTap II Command Line Options

To compile your design with the SignalTap II Logic Analyzer using the command prompt, you must use the `quartus_stp` command. Table 10–8 shows the options that help you better understand how to use the **quartus_stp** executable.

Table 12–8. SignalTap II Command-Line Options (Part 1 of 2)

Option	Usage	Description
`stp_file`	`quartus_stp --stp_file <stp_filename>`	Assigns the specified SignalTap II file to the `USE_SIGNALTAP_FILE` in the Quartus II Settings File (QSF).
`enable`	`quartus_stp --enable`	Creates assignments to the specified SignalTap II file in the QSF, and changes `ENABLE_SIGNALTAP` to `ON`. The SignalTap II Logic Analyzer is included in your design the next time the project is compiled. If no SignalTap II file is specified in the QSF, the `--stp_file` option must be used. If the `--enable` option is omitted, the current value of `ENABLE_SIGNALTAP` in the QSF is used.
`disable`	`quartus_stp --disable`	Removes the SignalTap II file reference from the QSF and changes `ENABLE_SIGNALTAP` to `OFF`. The SignalTap II Logic Analyzer is removed from the design database the next time you compile your design. If the `--disable` option is omitted, the current value of `ENABLE_SIGNALTAP` in the QSF is used.

Table 12–8. SignalTap II Command-Line Options (Part 2 of 2)

Option	Usage	Description
verify_connections	quartus_stp --verify_connections	Once a compilation with SignalTap II Logic Analyzer is complete, you must use this option to ensure that all signals that you wanted to tap in your design were properly connected to the logic analyzer.
create_signaltap_hdl_file	quartus_stp --create_signaltap_hdl_file	Creates a SignalTap II file representing the SignalTap II instance in the design generated by the SignalTap II Logic Analyzer megafunction created with the MegaWizard Plug-in Manager. The file is based on the last compilation. You must use the --stp_file option to properly create a SignalTap II file. Analogous to **Create SignalTap II File from Design Instance(s)** command in the Quartus II software.

The following example illustrates how to compile a design with the SignalTap II Logic Analyzer at the command line:

```
quartus_stp filtref --stp_file stp1.stp --enable ↵
quartus_map filtref --source=filtref.bdf --family=CYCLONE ↵
quartus_fit filtref --part=EP1C12Q240C6 --fmax=80MHz --tsu=8ns ↵
quartus_tan filtref ↵
quartus_asm filtref ↵
quartus_stp filtref --verify_connections ↵
```

The `quartus_stp --stp_file stp1.stp --enable` command creates the QSF variable and instructs the Quartus II software to compile the **stp1.stp** file with your design.

The `quartus_stp --verify_connections` command must be run after the `quartus_fit` command. The `--verify_connections` option verifies that all signals in the SignalTap II file were routed correctly to the logic analyzer.

Use the following example command to create a new SignalTap II file after building the SignalTap II Logic Analyzer instance with the MegaWizard Plug-In Manager:

```
quartus_stp filtref --create_signaltap_hdl_file --stp_file stp1.stp ↵
```

For information on the other command line executables and options refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

SignalTap II Tcl Commands

The **quartus_stp** executable supports a Tcl interface that allows you to capture data without running the Quartus II GUI. To run a Tcl file that has SignalTap II Tcl commands, use the following command:

```
quartus_stp -t <Tcl file> ↵
```

Table 12–9 shows the Tcl commands that you can use with SignalTap II.

Table 12–9. SignalTap II Tcl Commands (Part 1 of 2)

Command	Argument	Description
`open_session`	`--name` <*stp_filename*>	Opens the specified SignalTap II file. All captured data is stored in this file.
`run`	`--instance` <*instance_name*> `--signal_set` <*signal_set*> (optional) `--trigger` <*trigger_name*> (optional) `--data_log` <*data_log_name*> (optional) `--timeout` <*seconds*> (optional)	Starts the analyzer. This command must be followed by all the required arguments to properly start the analyzer. You can optionally specify the name of the data log you want to create. If the Trigger condition is not met, you can specify a timeout value to stop the analyzer.
`run_multiple_start`	None	Defines the start of a set of `run` commands. Use this command when multiple instances of data acquisition are started simultaneously. Add this command before the set of `run` commands that specify data acquisition. You must use this command with the `run_multiple_end` command. If the `run_multiple_end` command is not included, the `run` commands will not execute.

Table 12–9. SignalTap II Tcl Commands (Part 2 of 2)

Command	Argument	Description
run_multiple_end	None	Defines the end of a set of run commands. Use this command when multiple instances of data acquisition are started simultaneously. Add this command after the set of run_commands.
stop	None	Stops data acquisition
close_session	None	Closes the currently open SignalTap II file. You cannot run the analyzer after the SignalTap II file is closed.

For more information on SignalTap II Tcl commands, refer to the Quartus II Help.

The following example is an excerpt from a script that is used to continuously capture data. Once the trigger condition is met, the data is captured and stored in the data log.

```
#opens signaltap session
open_session -name stp1.stp
#start acquisition of instance auto_signaltap_0 and
#auto_signaltap_1 at the same time
#calling run_multiple_end will start all instances
#run after run_multiple_start call
run_multiple_start
run -instance auto_signaltap_0 -signal_set signal_set_1 -trigger /
trigger_1 -data_log log_1 -timeout 5
run -instance auto_signaltap_1 -signal_set signal_set_1 -trigger /
trigger_1 -data_log log_1 -timeout 5
run_multiple_end
#close signaltap session
close_session
```

Once the script is completed, you should open the SignalTap II file that you used to capture data to examine the contents of the Data log.

Design Example: Using SignalTap II Logic Analyzers in SOPC Builder Systems

Altera Application Note, *AN 323: Using SignalTap II Embedded Logic Analyzers in SOPC Builder Systems* describes how to use the SignalTap II Logic Analyzer to monitor signals located inside a system module generated by SOPC Builder. The system in this example contains many components, including a Nios processor, a direct memory access (DMA) controller, on-chip memory, and an interface to external SDRAM memory. In this example, the Nios processor executes a simple C program from on-chip memory and waits for a button push. After a button is pushed, the processor initiates a DMA transfer, which you analyze using the SignalTap II Logic Analyzer.

For more information on this example, refer to *AN 323: Using SignalTap II Embedded Logic Analyzers in SOPC Builder Systems* which is available on the Literature page of the Altera website at www.altera.com.

Conclusion

As the FPGA industry continues to make technological advancements, outdated methodologies need to be replaced with new technologies that maximize productivity. The SignalTap II Logic Analyzer gives you the same benefits as a traditional logic analyzer, without the many shortcomings of a piece of dedicated test equipment. This version of the SignalTap II Logic Analyzer provides many new and innovative features that allow you to capture and analyze internal signals in your FPGA, allowing you to find the source of a design flaw in the shortest amount of time.

13. In-System Debugging Using External Logic Analyzers

QII53016-6.0.0

Introduction

The phenomenal growth in design size and complexity continues to make the process of design verification a critical bottleneck for today's FPGA systems. Limited access to internal signals, advanced FPGA packages, and printed circuit board (PCB) electrical noise are all contributing factors in making design debugging and verification the most difficult process of the design cycle. You can easily spend more than 50% of your design cycle time debugging and verifying your design. To help you with the process of design debugging and verification, Altera® provides a solution that allows you to examine the behavior of internal signals using an external logic analyzer and using a minimal number of FPGA I/O pins, while your design is running at full speed on your FPGA.

The Logic Analyzer Interface is an application within the Quartus II software used to connect a large set of internal device signals to a small number of output pins. You can connect these output pins to an external logic analyzer for debugging purposes. The Logic Analyzer Interface enables you to connect to and transmit internal signals buried within your FPGA to an external logic analyzer for analysis. The Quartus II Logic Analyzer Interface allows you to debug a large set of internal signals using a small number of output pins. In the Quartus II Logic Analyzer Interface, the internal signals are grouped together, distributed to a user-configurable multiplexer, and then output to available I/O pins on your FPGA. Instead of having a one-to-one relationship between internal signals to output pins, the Quartus II Logic Analyzer Interface enables you map many internal signals to a smaller number of output pins. The exact number of internal signals that you can map to an output pin varies based on the multiplexer settings in the Quartus II Logic Analyzer Interface.

Optionally, you can use the Logic Analyzer Interface with the Quartus II Incremental Compilation.

Choosing a Logic Analyzer

During the debugging phase of your project, you have the choice of using:

- SignalTap® II, the embedded logic analyzer.
- An external logic analyzer, which connects to internal signals in your FPGA, by using the Quartus II Logic Analyzer Interface.

Table 13–1 describes the advantages to both debugging technologies.

Table 13–1. Comparing the SignalTap II Embedded Logic Analyzer with the Logic Analyzer Interface

Feature	Logic Analyzer Interface	SignalTap II Embedded Logic Analyzer
Sample Depth—You will have access to a wider sample depth with an external logic analyzer. In SignalTap II, the maximum sample depth is set to 128 Kb, which is a device constraint. However, with an external logic analyzer, there are no device constraints, providing you a wider sample depth.	✓	
Debugging Timing Issues—Using an external logic analyzer provides you with access to a "timing" mode, which enables you to debug combined streams of data.	✓	
Performance—You frequently have limited routing resources available to place-and-route when you use SignalTap II with your design. An external logic analyzer adds minimal logic, which removes resource limits on place-and-route.	✓	
Triggering Capability—Although advanced triggering is available in SignalTap II, many additional triggering options are available on an external logic analyzer.	✓	
Use of Output Pins—Using the SignalTap II Logic Analyzer, no additional output pins are required. Using an external logic analyzer requires the use of additional output pins.		✓
Acquisition Speed—With the SignalTap II Logic Analyzer, you can acquire data at speeds of over 200 MHz. You can achieve the same acquisition speeds with an external logic analyzer, however you have to consider signal integrity issues.		✓

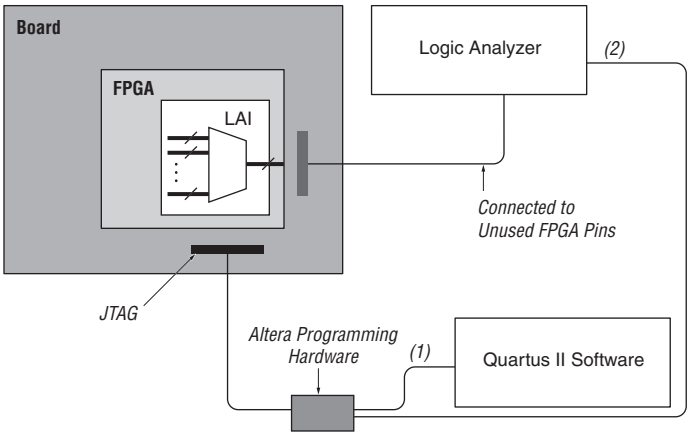
Required Components

You must have the following components to perform analysis using the Quartus II Logic Analyzer Interface:

- The Quartus II software starting with version 5.1 and later
- The device under test
- An external logic analyzer
- An Altera communications cable
- A cable to connect the FPGA to the external logic analyzer

Figure 13–1 shows the Logic Analyzer Interface and the hardware setup.

Figure 13–1. Logic Analyzer Interface & Hardware Setup



Notes to Figure 13–1:
(1) Configuration and control of the LAI using computer loaded with Quartus II via the JTAG port.
(2) Configuration and control of the LAI using a third-party vendor logic analyzer via the JTAG port. Support varies by vendor.

FPGA Device Support

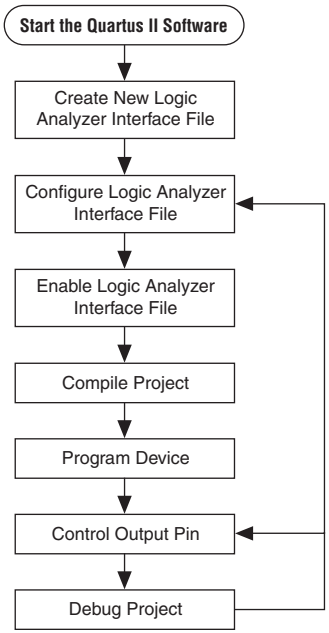
You can use the Quartus II Logic Analyzer Interface with the following FPGA device families:

- Stratix® II
- Stratix
- Stratix II GX
- Stratix GX
- Cyclone™ II
- Cyclone
- MAX® II
- APEX™ 20K
- APEX II
- Excalibur™

Debugging Your Design Using the Logic Analyzer Interface

Figure 13–2 shows the steps you must follow to debug your design with the Quartus II Logic Analyzer Interface.

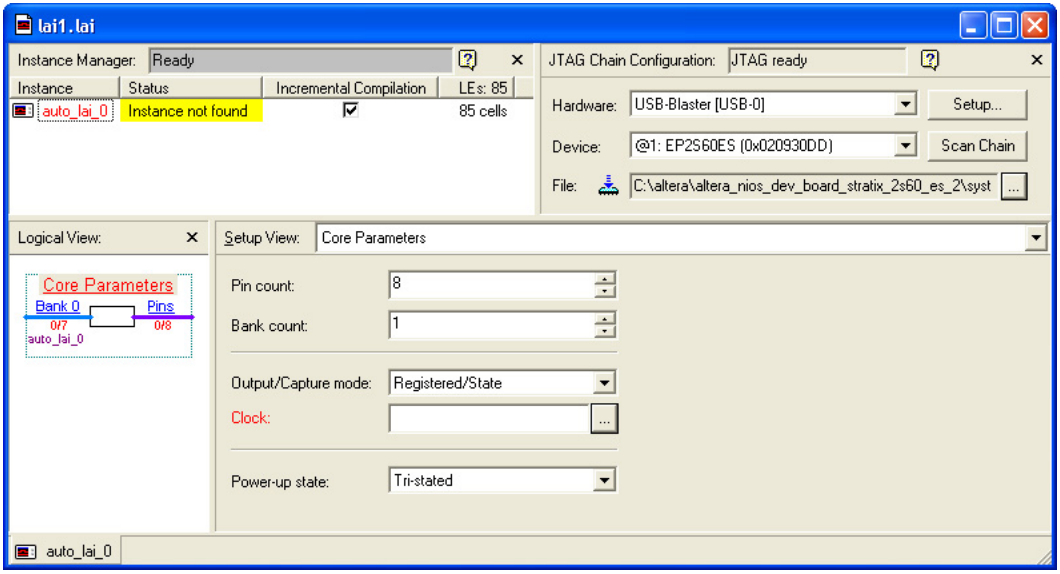
Figure 13–2. Logic Analyzer Interface Process Flow



Creating a Logic Analyzer Interface File

The Logic Analyzer Interface File (**.lai**), defines the interface that builds a connection between internal FPGA signals and your external logic analyzer. An example of a Logic Analyzer Interface File is shown in Figure 13–3.

Figure 13–3. Example of a Logic Analyzer Interface Editor



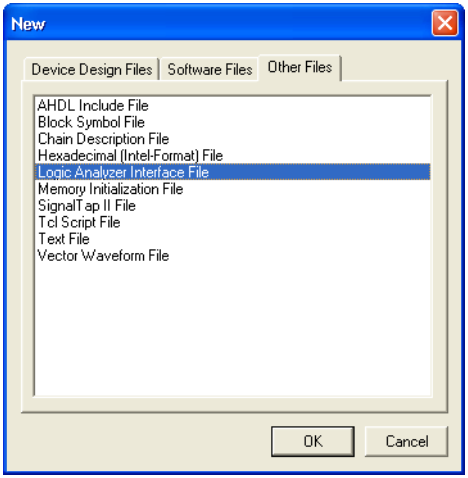
To define the Quartus II Logic Analyzer Interface, you can create a new Logic Analyzer Interface File or use an existing Logic Analyzer Interface File.

Creating a New Logic Analyzer Interface File

To create a new Logic Analyzer Interface File, perform the following steps:

1. In the Quartus II software, on the File menu, click **New**. The **New** dialog box opens.
2. Click the **Other Files** tab and select **Logic Analyzer Interface File** (Figure 13–4).

Figure 13–4. Creating a New Logic Analyzer File



3. Click **OK**. The Logic Analyzer Interface editor opens. The file name is assigned by the Quartus II software (refer to Figure 13–3 on page 13–5). When you save the file, you will be prompted for a file name. Refer to "Saving the External Analyzer Interface File" on page 13–7.

Opening an Existing External Analyzer Interface File

To open an existing Logic Analyzer Interface File, on the Tools menu, click **Logic Analyzer Interface Editor**. If no Logic Analyzer Interface File is enabled for the current project, the editor automatically creates a new Logic Analyzer Interface File. If a Logic Analyzer Interface File is currently enabled for the project, that file opens when you select the **Logic Analyzer Interface Editor**.

Another way to open an existing Logic Analyzer Interface File is on the File Menu, click **Open**, and select the Logic Analyzer Interface File you want to open.

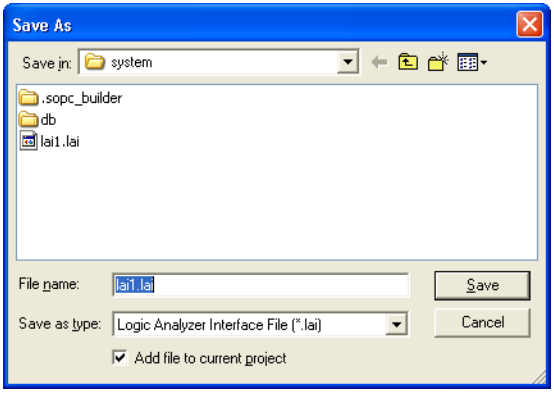
Saving the External Analyzer Interface File

To save your Logic Analyzer Interface File, perform the following steps:

1. In the Quartus II software, on the File menu, click **Save As**, The **Save As** dialog box opens (Figure 13–5).

2. In the **File name** box, enter the desired file name. Click Save (Figure 13–5).

Figure 13–5. Saving the Logic Analyzer Interface File



Configuring the Logic Analyzer Interface File Core Parameters

After you have created your Logic Analyzer Interface File, you must configure the Logic Analyzer Interface File core parameters.

To configure the Logic Analyzer Interface File core parameters, select Core Parameters from the Setup View list. Refer to Figure 13–6.

Figure 13–6. Logic Analyzer Interface File Core Parameters

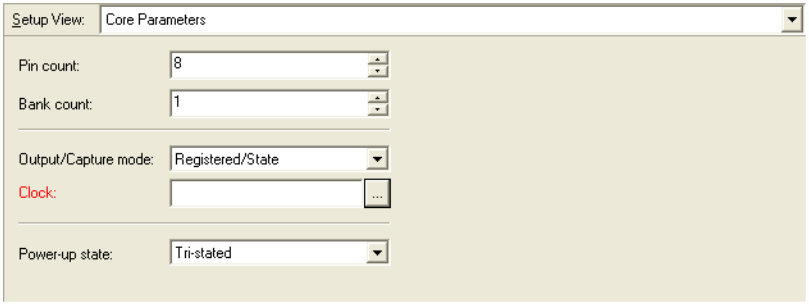


Table 13–2 lists the Logic Analyzer Interface File core parameters.

Table 13–2. Logic Analyzer Interface File Core Parameters (Part 1 of 2)

Parameter	Description
Pin Count	The Pin Count parameter signifies the number of pins you want dedicated to your Logic Analyzer Interface. The pins need to be connected to a debug header on your board. Within the FPGA, each pin is mapped to a user-configurable number of internal signals. The Pin Count parameter can range from 1 to 256 pins.
Bank Count	The Bank Count parameter signifies the number of internal signals that you want to map to each pin. For example, a Bank Count of 8 implies that you will connect eight internal signals to each pin. The Bank Count parameter can range from 1 to 256 banks.
Output/ Capture Mode	The Output/Capture Mode parameter signifies the type of acquisition you perform. There are two options that you can select: Combinational/Timing—This acquisition uses your external logic analyzer's internal clock to determine when to sample data. Because Combinational/Timing acquisition samples data asynchronously to your FPGA, you need to properly determine the sample frequency you should use to debug and verify your system. This mode is effective if you want to measure timing information such as channel-to-channel skew. For more information on the sampling frequency, and what speeds it can run at refer to the data sheet for your external logic analyzer. Registered/State—This acquisition uses a signal from your system under test to determine when to sample. Because Registered/State acquisition samples data synchronously with your FPGA, it provides you with a functional view of your FPGA while it is running. This mode is effective when you want to verify the functionality of your design.

Table 13–2. Logic Analyzer Interface File Core Parameters (Part 2 of 2)

Parameter	Description
Clock	The clock parameter is available only when Output/Capture Mode is set to Registered State. You must specify the sample clock in the Core Parameters view. The sample clock can be any signal in your design. However, for best results, Altera recommends that you use a clock with an operating frequency fast enough to sample the data you would like to acquire.
Power-Up State	The Power-Up State parameter specifies the power-up state of the pins you have designated for use with the Logic Analyzer Interface. You have the option of selecting tri-stated for all pins, or selecting a particular bank that you have enabled.

Mapping the Logic Analyzer Interface File Pins to Available I/O Pins

To configure the Logic Analyzer Interface File I/O pins parameters, select Pins from the Setup View list (Figure 13–7).

Figure 13–7. Logic Analyzer Interface File Pins Parameters

Setup View: Pins

Pin				I/O Standard
Type	Index	Name	Location	
	0	altera_reserved_lai_0_0		
	1	altera_reserved_lai_0_1		
	2	altera_reserved_lai_0_2		
	3	altera_reserved_lai_0_3		
	4	altera_reserved_lai_0_4		
	5	altera_reserved_lai_0_5		
	6	altera_reserved_lai_0_6		
	7	altera_reserved_lai_0_7		

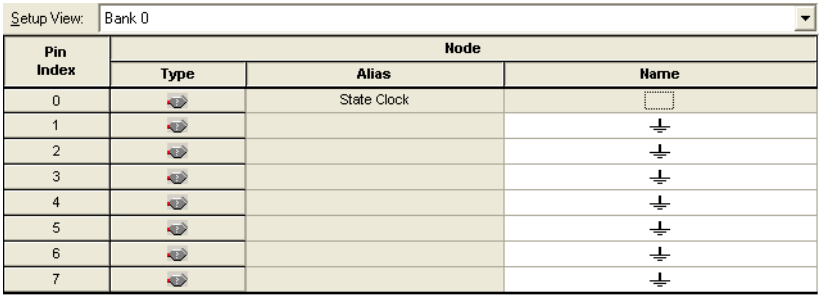
To assign pin locations for the Logic Analyzer Interface, double-click the **Location** column next to the reserved pins in the **Names** column. This opens the Pin Planner.

For information on how to use the Pin Planner, refer to the *Pin Planner* section in the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Mapping Internal Signals to the Logic Analyzer Interface Banks

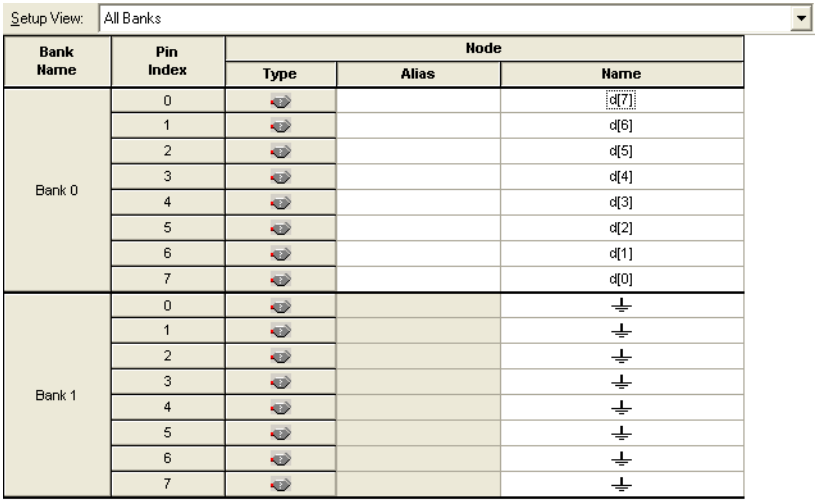
After you have specified the number of banks to use in the Core Parameters settings page, you must assign internal signals for each bank in the Logic Analyzer Interface. Click the **Setup View** arrow and select **Bank *n*** or **ALL Banks** (Figure 13–8).

Figure 13–8. Logic Analyzer Interface Bank Parameters



To view all of your bank connections, click **Setup View** and select **All Banks** (Figure 13–9).

Figure 13–9. Logic Analyzer Interface All Bank Parameters



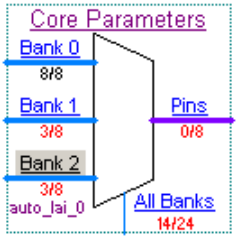
Using the Node Finder

Before making bank assignments, on the View menu, point to Utility Windows, and click **Node Finder**. Find the signals that you want to acquire, then drag and drop the signals from the Node Finder dialog box

into the bank **Setup View**. When adding signals, use **SignalTap II: pre-synthesis** for non-incrementally routed instances and **SignalTap II: post-fitting** for incrementally routed instances.

As you continue to make assignments in the bank Setup View, the schematic of your Logic Analyzer Interface in the Logical View of your Logic Analyzer Interface File begins to reflect your assignments (Figure 13–10).

Figure 13–10. A Logical View of the Logic Analyzer Interface Schematic



Continue making assignments for each bank in the **Setup View** until you have added all of the internal signals for which you wish to acquire data.

You can right-click to switch between the Logic Analyzer Interface schematic and the Logic Analyzer Interface Setup view.

Enabling the Logic Analyzer Interface Before Compiling Your Quartus II Project

Compile your project after you have completed the following steps:

- Configure your Logic Analyzer Interface parameters
- Map the Logic Analyzer Interface pins to available I/O pins
- Map the internal signals to the Logic Analyzer Interface banks

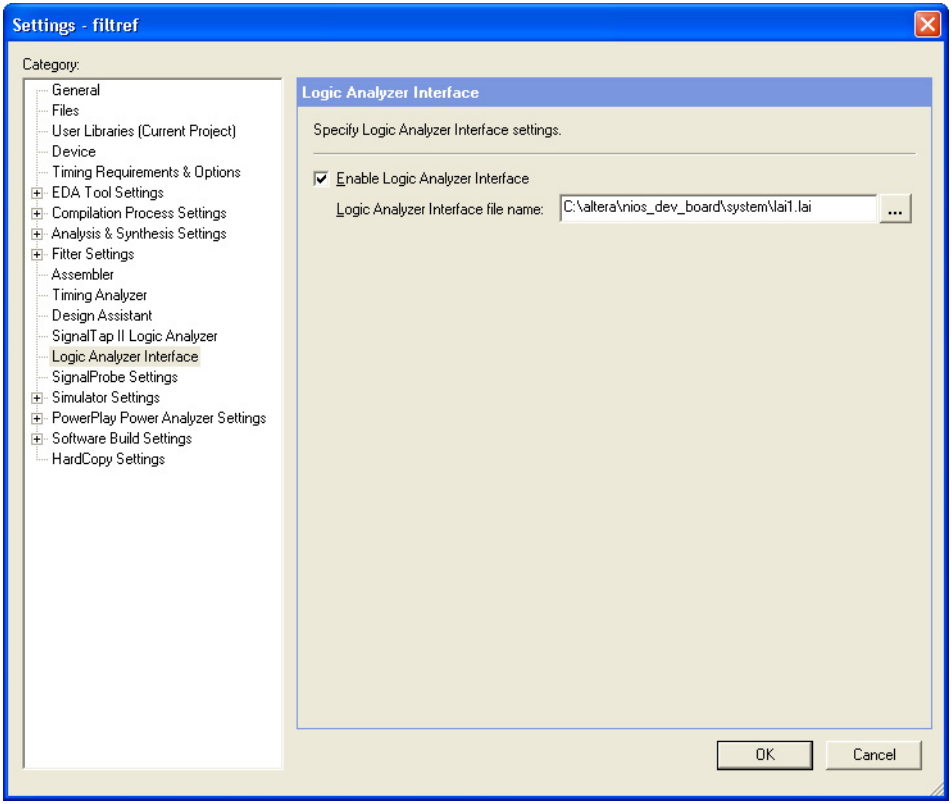
Compiling Your Quartus II Project

Before compilation, you must enable the Logic Analyzer Interface.

1. On the Assignments menu, click **Settings**. The **Settings** dialog box opens. Under Category, click **Logic Analyzer Interface**. The **Logic Analyzer Interface** displays. Turn on **Enable Logic Analyzer Interface.**

2. Click **Logic Analyzer Interface file name** and specify the full path name to your Logic Analyzer Interface File (Figure 13–11).

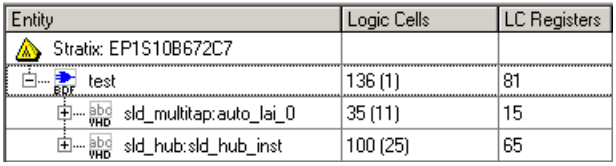
Figure 13–11. Settings Dialog Box—Logic Analyzer Interface Settings



After you have specified the name of your Logic Analyzer Interface File, you must compile your project. To compile your project, on the Processing menu, click **Start Compilation**.

To ensure the Logic Analyzer Interface is properly compiled with your project, expand the entity hierarchy in the Project Navigator. (To display the Project Navigator, on the View menu, point to **Utility Windows**, and click **Project Navigator**.) If the Logic Analyzer Interface compiled with your design, the `sld_hub` and `sld_multitap` entities are shown in the project navigator.

Figure 13–12. Project Navigator

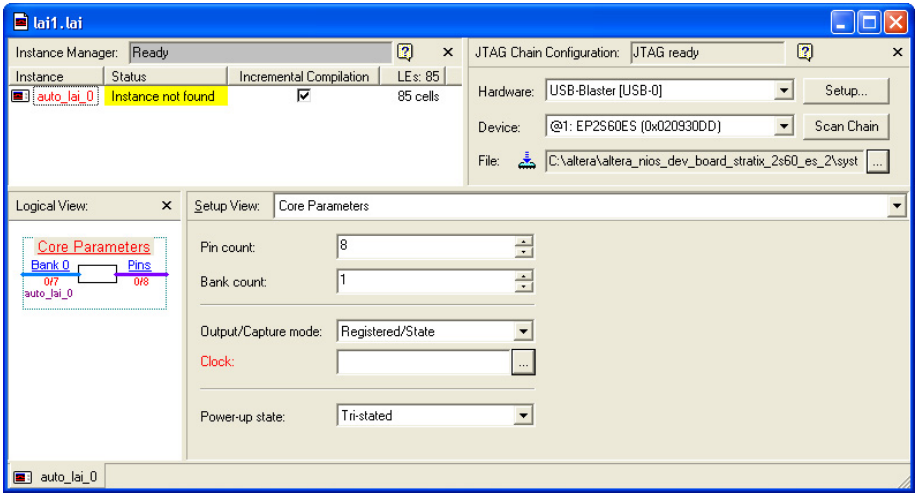


Programming Your FPGA Using the Logic Analyzer Interface

After compilation completes, you must configure your FPGA before using the Logic Analyzer Interface. To configure a device for use with the Logic Analyzer Interface, follow these steps:

1. Open the Logic Analyzer Interface File Editor (Figure 13–13).
2. Under **JTAG Chain Configuration**, click **Hardware** and select your hardware communications device. You may have to click **Settings** to configure your hardware.
3. Click **Device** and select the FPGA device to which you want to download the design (it may be automatically detected). You may have to click **Scan Chain** to configure your device.
4. Click **File** and select the SRAM Object File (**.sof**) that includes the Logic Analyzer Interface File (it may be automatically detected).
5. If desired, turn on **Incremental Compilation**.
6. Save the Logic Analyzer Interface File.
7. Click the **Program Device** icon to program the device.

Figure 13–13. The JTAG Section of the Logic Analyzer Interface File



Using the Logic Analyzer Interface with Multiple Devices

You can use the Logic Analyzer Interface with multiple devices in your JTAG chain. Your JTAG chain can also consist of devices that do not support the Logic Analyzer Interface or non-Altera, JTAG-compliant devices. To use the Logic Analyzer Interface in more than one FPGA, create a Logic Analyzer Interface and configure a Logic Analyzer Interface File for each FPGA that you want to analyze. To perform multi-FPGA analysis, perform the following steps:

1. Open the Quartus II software.
2. Create, configure, and compile a Logic Analyzer Interface File for each design.
3. Open one Logic Analyzer Interface File at a time.

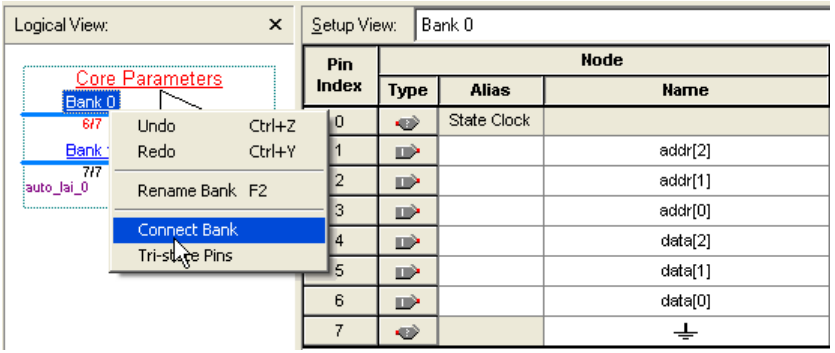
   You do not have to open a Quartus II project to open a Logic Analyzer Interface File.

4. Follow Steps 2 through 6 under "Programming Your FPGA Using the Logic Analyzer Interface" on page 13–13.
5. Click the **Program Device** icon to program the device.
6. Control each Logic Analyzer Interface File independently.

Configuring Banks in the Logic Analyzer Interface File

When you have programmed your FPGA, you can control which bank is mapped to the reserved Logic Analyzer Interface File output pins. To control which bank is mapped, right-click on the bank in the schematic in the logical view and click **Connect Bank**.

Figure 13–14. Configuring Banks



Acquiring Data on Your Logic Analyzer

To acquire data on your logic analyzer, you must establish a connection between your device and the external logic analyzer.

For more information on this process, and for guidelines on how to establish connections between debugging headers and logic analyzers, refer to the documentation for your logic analyzer.

Advanced Features

This section describes the following advanced features:

- Using the Logic Analyzer Interface with Incremental Compilation
- Creating Multiple Logic Analyzer Interface Instances in One FPGA

Using the Logic Analyzer Interface with Incremental Compilation

Using the Logic Analyzer Interface with Incremental Compilation enables you to preserve the synthesis and fitting of your original design and add the Logic Analyzer Interface to your design without recompiling your original source code.

To use the Logic Analyzer Interface with Incremental Compilation, perform the following steps:

1. Start the Quartus II software.

2. Enable Design Partitions. To enable Partitions, perform the following steps:

    a. On the Assignments menu, click, **Design Partitions**.

    b. In the **Incremental Compilation** list, select **Full Incremental Compilation**.

    c. Create Design Partitions for the entities in your design, and set the Netlist Type to **Post-fit**.

    d. On the Processing menu, click **Start Compilation**.

3. Enable Logic Analyzer Interface Incremental Compilation by performing these steps:

    a. In your Logic Analyzer Interface File, under **Instance Manager**, click **Incremental Compilation**.

    When you enable Incremental Compilation, all existing presynthesis signals will be converted into post-fitting signals. Only post-fitting signals can be used with the Logic Analyzer Interface with Incremental Compilation.

    b. Add Post-Fitting nodes to your Logic Analyzer Interface File.

    c. On the Processing menu, click **Start Compilation**.

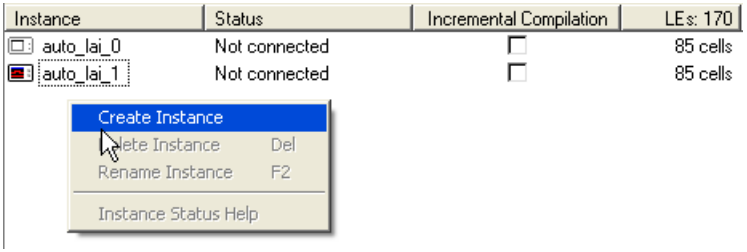
Creating Multiple Logic Analyzer Interface Instances in One FPGA

The Logic Analyzer Interface includes support for multiple interfaces in one FPGA. This feature is particularly useful when you want to build Logic Analyzer Interface configurations that contain different settings. For example, you can build one Logic Analyzer Interface instance to perform Registered/State analysis and build another instance that performs Combinational/Timing analysis on the same set of signals.

Another example would be if you want to perform Registered/State analysis on portions of your design that are in different clock domains.

To create multiple Logic Analyzer Interfaces, on the Edit menu, click **Create Instance**. Alternatively, you can right-click in the Instance Manager window, and click **Create Instance**.

Figure 13–15. Creating Multiple Logic Analyzer Interface Instances in One FPGA



Conclusion

As the FPGA industry continues to make technological advancements, outdated debugging methodologies must be replaced with new technologies that maximize productivity. The Logic Analyzer Interface feature enables you to connect many internal signals within your FPGA to an external logic analyzer with the use of a small number of I/O pins. This new technology in the Quartus II software enables you to use feature-rich external logic analyzers to debug your FPGA design, ultimately enabling you to delver your product in the shortest amount of time.

14. Design Analysis & Engineering Change Management with Chip Editor

QII53010-6.0.0

Introduction

One of the toughest challenges that FPGA designers face is implementing engineering change orders (ECOs) late in the design cycle. When altering functionality late in the design cycle, issues such as preserving functionality and timing while meeting the change request specifications in the shortest amount of time are critical.

With the Quartus® II software's Chip Editor, you can view the internal structure of Altera® devices, examine internal timing, and edit functionality and parameter settings for resources within the device. The Chip Editor also helps you document and manage all of the changes you make in your design.

The Chip Editor works directly on the post place-and-route design database so you can implement design changes in minutes without performing a full compilation. The changes you make are restricted to particular device resources, so the timing performance of the remaining portions of your design are not affected. Design rule checks are performed on all changes to prevent illegal modifications to your design.

This chapter describes how to use the Chip Editor and includes coverage of the following topics:

- Chip Editor
- Design Analysis Using the Chip Editor
- Resource Property Editor
- Change Manager
- Common applications
- Post-Chip Editor commands

Chip Editor

With the Chip Editor, you can view the following architecture-specific information related to your design:

- Device routing resources used by your design: Visually examine how blocks are connected, as well as the signal routing that connects the blocks.
- LE configuration: View how a logic element (LE) is configured within your design. For example, you can view which LE inputs are used, if the LE utilizes the register, the look-up table (LUT), or both, as well as the signal flow through the LE.

- ALM configuration: View how an adaptive logic module (ALM) is configured within your design. For example, you can view which ALM inputs are used, if the ALM utilizes the registers, the upper LUT, the lower LUT, or all of them. You can also view the signal flow through the ALM.
- I/O configuration: View how the device I/O resources are used. For example, you can view which components of the I/O resources are used, if the delay chain settings are enabled, which I/O standards are set, and the signal flow through the I/O.
- PLL configuration: View how a phase-locked loop (PLL) is configured within your design. For example, you can view which control signals of the PLL are used along with the settings for your PLL.
- Timing: View the delay between the inputs and outputs of FPGA elements. For example, you can analyze the timing of `DATAB` input to the `COMBOUT` output.

You can modify the following properties of an Altera device with the Chip Editor:

- LEs and ALMs
- I/O cells
- PLLs
- Connections between elements
- Placement of elements

The Chip Editor supports the following Altera device families:

- Stratix® II
- Stratix II GX
- Stratix
- Stratix GX
- Cyclone™ II
- Cyclone
- MAX® II

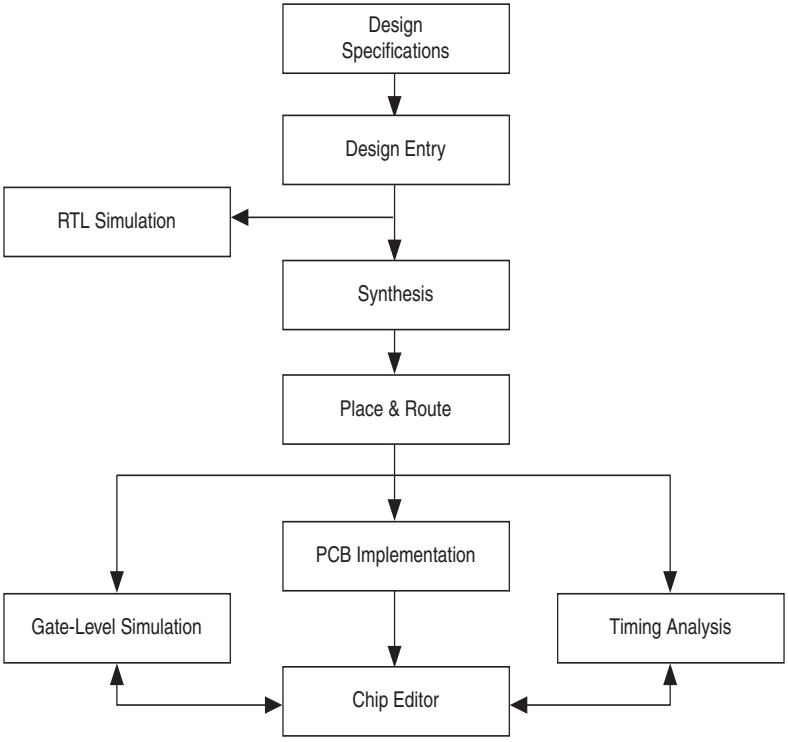
Using the Chip Editor in Your Design Flow

The ideal design flow starts by developing the design specification, creating register transfer level (RTL) code that describes the design specification, verifying that the RTL code performs the correct functionality, and verifying that the fitted design satisfies the design's timing constraints. The flow ends with successfully programming the targeted FPGA.

Unfortunately, similar to most difficult processes, the ideal design flow rarely occurs. Often, you find bugs in the RTL code or the design specifications change midway through the design cycle. The challenge lies in efficiently accommodating these types of design issues. Traditionally, you return to the source code, make the appropriate changes, and then go through the entire design flow again, including synthesis, place-and-route, and verification.

With the Altera Chip Editor, you can shorten the design-cycle time. When changes are made to your design, you do not have to perform a full compilation in the Quartus II software. Instead, you make changes directly to the post place-and-route netlist, generate a new programming file, and test the revised design by performing a gate-level timing simulation and timing analysis without modifying the source code. You can continue to iteratively make changes to your design using the Chip Editor until you correct the problem. Figure 14–1 describes how you can use the Chip Editor in your design flow.

Figure 14–1. Chip Editor Design Flow



Chip Editor Features

The Chip Editor contains many advanced features that enable you to quickly and efficiently make design changes. The Chip Editor's integrated tool set provides the following features:

- Chip Editor Floorplan: enables you to view post-compilation placement, connections, and routing paths; create new logic cells and I/O atoms, and move existing logic cells and I/O atoms while having full view of your design.
- Resource Property Editor: enables you to make changes to the properties and parameters of resources, and modify connectivity between certain types of resources.
- Change Manager: maintains an ongoing record of your post-compilation changes, and assists in ensuring that conflicting changes do not occur; you can also write out a tool command language (**.tcl**) file that allows you to reproduce the changes you made.

The Chip Editor Floorplan allows you to quickly and easily view post-compilation placement and routing information. You can start the Chip Editor Floorplan in any of the following ways:

- On the Tools menu, click **Chip Editor**.
- Use the right-click menu from the Compilation Report
- Use the right-click menu from the RTL source code
- Use the right-click menu from the Timing Closure Floorplan
- Use the right-click menu from the Node Finder
- Use the right-click menu from the Simulation Report
- Use the right-click menu from the RTL Viewer

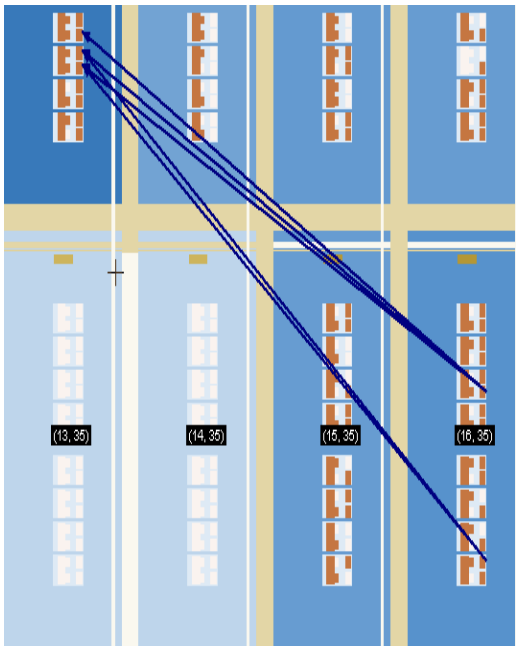
Design Analysis Using the Chip Editor Floorplan

The Chip Editor Floorplan assists you in visually analyzing your design after performing a full design compilation in the Quartus II software. The Chip Editor Floorplan, used in conjunction with traditional Quartus II timing analysis features, provides a powerful method for performing design analysis.

Viewing Critical Paths

The View Critical Paths feature displays routing paths in the Chip Editor, as shown in Figure 14–2. The criticality of a path is determined by its slack and is shown in the timing analysis report. On the View menu, click **Open Critical Path Settings** to view critical paths in the Chip Editor.

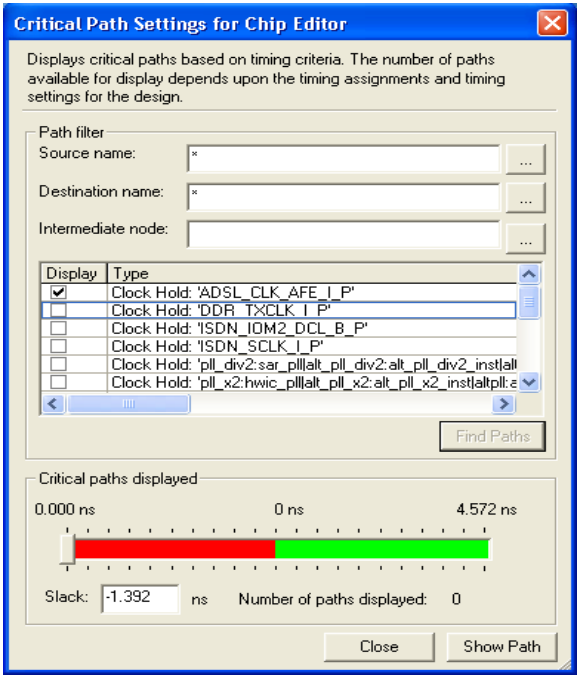
Figure 14–2. Chip Editor with Critical Path Enabled



When viewing critical paths, specify the clock in the design to be viewed. Determine the paths you want displayed by specifying the slack threshold in the slack field. For example, when you specify a slack threshold of -1.392ns in the slack field, six paths with this slack or worse are displayed (Figure 14–3). Therefore, by choosing the slack threshold, you can easily control which critical paths you can view.

Make timing settings and perform a timing analysis for the displayed critical paths in the Chip Editor.

Figure 14–3. Critical Path Settings for Chip Editor



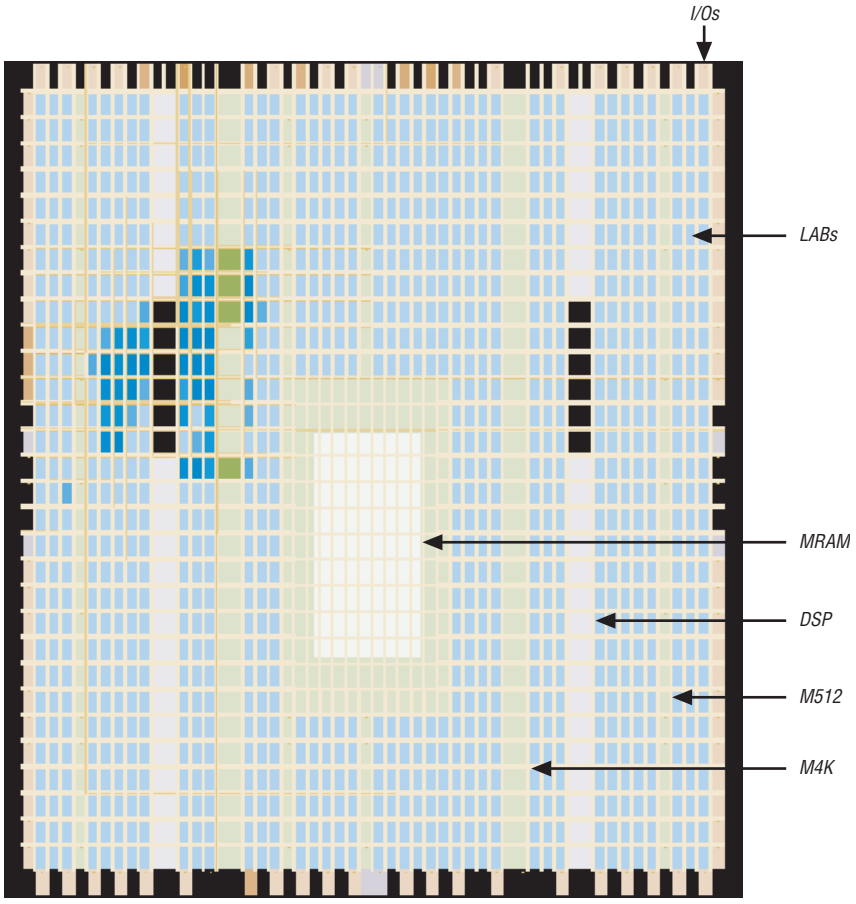
Chip Editor Floorplan Views

The Chip Editor uses a hierarchical zoom viewer that shows various abstraction levels of the targeted Altera device. As you increase the zoom level, the level of abstraction decreases, thus revealing more detail about your design. On the Tools menu, click **Options** to adjust the granularity of the auto-zoom function.

First (Highest) Level View

The first (highest) zoom level provides a high-level view of the entire device floorplan. This view provides a level of detail similar to the Field View in the Quartus II Timing Closure floorplan. You can locate and view the placement of any node in your design. Figure 14–4 shows the Chip Editor's first level view.

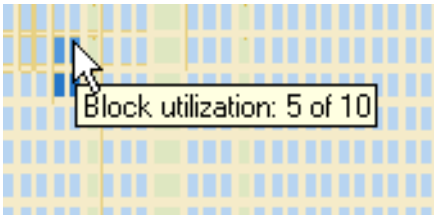
Figure 14–4. Chip Editor's First (Highest) Level View



Each resource is shown in a different color which makes it easier to distinguish between resources. The Chip Editor Floorplan uses a gradient color scheme in which the color becomes darker as the utilization of a resource increases. For example, as more LEs are used in the LAB, the color of the LAB becomes darker.

When you place the mouse pointer over a resource at this level, a tooltip appears that describes, at a high level, the utilization of the resource (Figure 14–5).

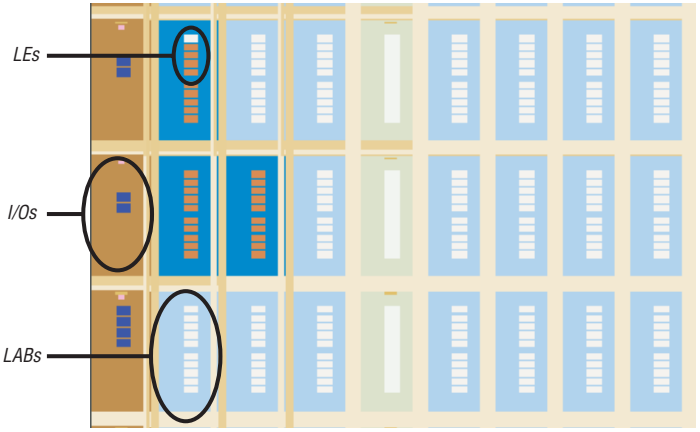
Figure 14–5. Tooltip Message: First Level View



Second Level View

As you zoom in, you see an increase in the level of detail. Figure 14–6 shows the second-level view of the Chip Editor. Floorplan.

Figure 14–6. Chip Editor's Second Level View



At this level you can see the contents of LABs and I/O banks. You also see the routing channels that are used to connect resources.

When you place the mouse pointer over an LE at this level, a tooltip is displayed (Figure 14–7) that shows the name of the LE, the location of the LE, and the number of resources that are used with that LAB. When you place the mouse pointer over an interconnect, the tooltip shows the routing channels that are used by that interconnect.

Figure 14–7. Tooltip Message: Second Level View

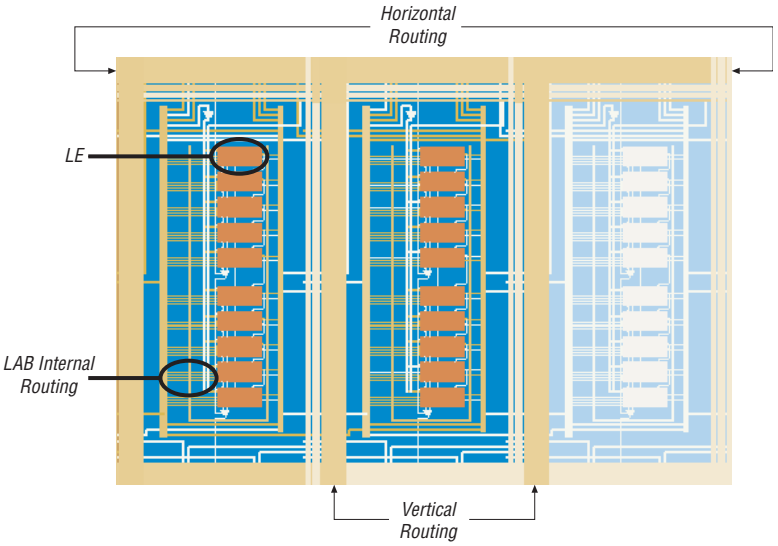
Third Level View

Figure 14–8 shows the level of detail at the third and lowest level. At this level you can see each routing resource that is used within a LAB in the FPGA.

At this level, you can move LEs and I/Os from one physical location to another. You can move a resource by selecting, dragging, and dropping it into the desired location. At this level you also can create new LEs and I/Os. To create a resource, right-click at the location you want to create the resource, click **Create Atom**. To delete a resource, right-click on the resources you want to delete, click **Delete Atom**.

You can only delete a resource after all of its fan-out connections are removed.

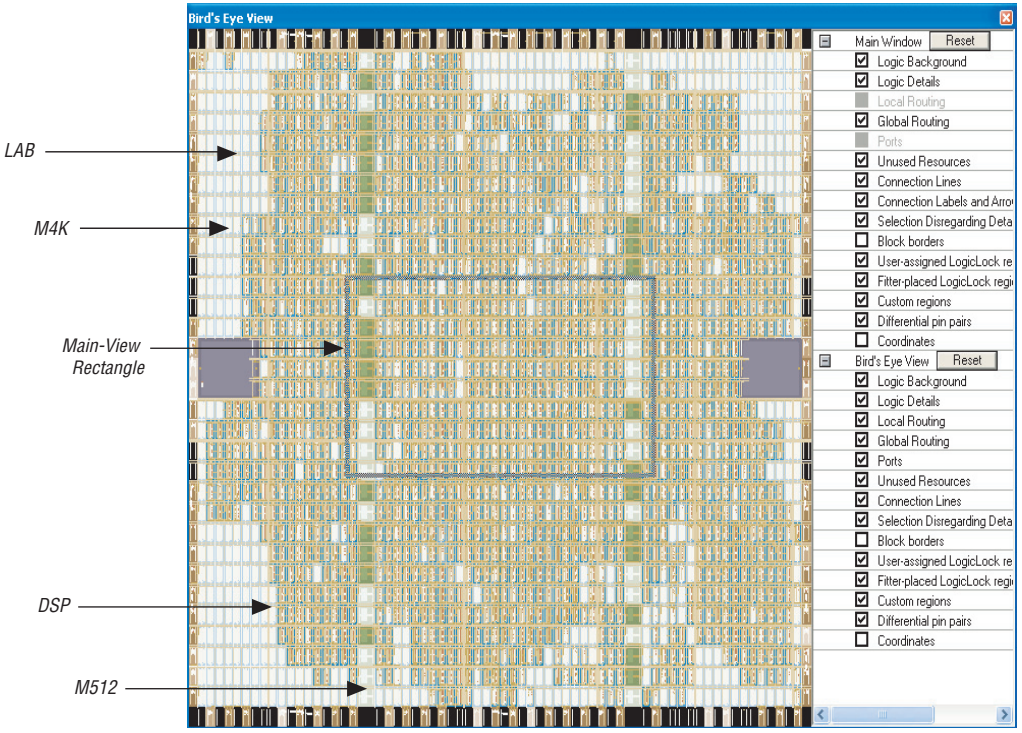
Figure 14–8. Chip Editor's Third Level View



Bird's Eye View

The Bird's Eye View (Figure 14–9) displays a high-level picture of resource usage for the entire chip and provides a fast and efficient way to navigate between areas of interest in the Chip Editor. In addition, it provides controls that allow you to specify which graphic elements are displayed. The specifications can be applied either to the Bird's Eye View or the main Chip Editor window.

Figure 14–9. Bird's Eye View



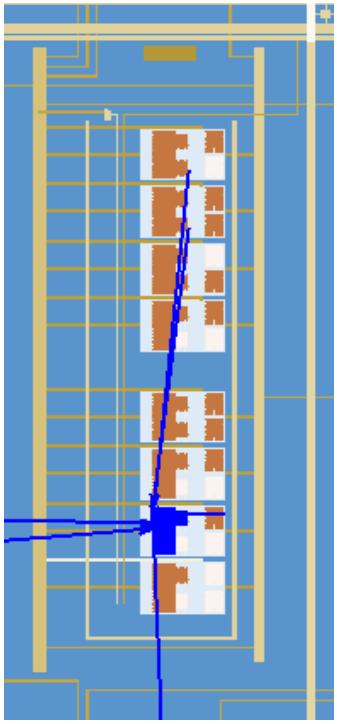
The Bird's Eye View is displayed as a separate window that is linked to the Chip Editor Floorplan. When you select an area of interest in the Bird's Eye View, the Chip Editor Floorplan automatically refreshes to show that region of the device. As you change the size of the main-view rectangle in the Bird's Eye View window, the main Chip Editor Floorplan window also zooms in (or zooms out). You can make the main-view rectangle smaller in the Bird's Eye View to see more detail on the Chip Editor Floorplan window.

The Bird's Eye View is particularly useful when the parts of your design that you are interested in are at opposite ends of the chip and you want to quickly navigate between resource elements without losing your frame of reference.

Generating Fan-in & Fan-Out Connections

This feature enables you to view the atoms that fan-in to or fan-out from the selected atom. To remove the connections displayed, use the **Clear Connections** icon in the **Chip Editor** toolbar. Figure 14–10 shows the fan-in connections for the selected resource.

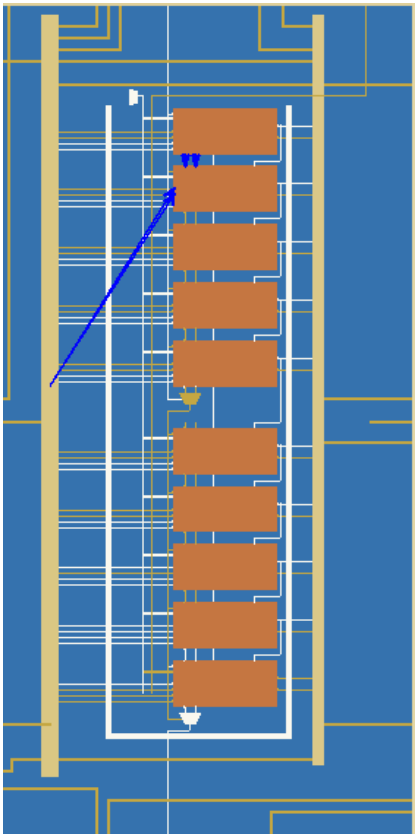
Figure 14–10. Generated Fan-In



Generating Immediate Fan-In & Fan-Out Connections

This feature enables you to view the immediate resource that is the fan-in or fan-out connection for the selected atom. For example, selecting a logic resource and choosing to view the immediate fan-in enables you to see the routing resource that drives the logic resource. You can generate immediate fan-in and fan-outs for all logic resources and routing resources. To remove the connections that are displayed, use the **Clear Connections** icon in the toolbar. Figure 14–11 shows the immediate fan-out connections for the selected resource.

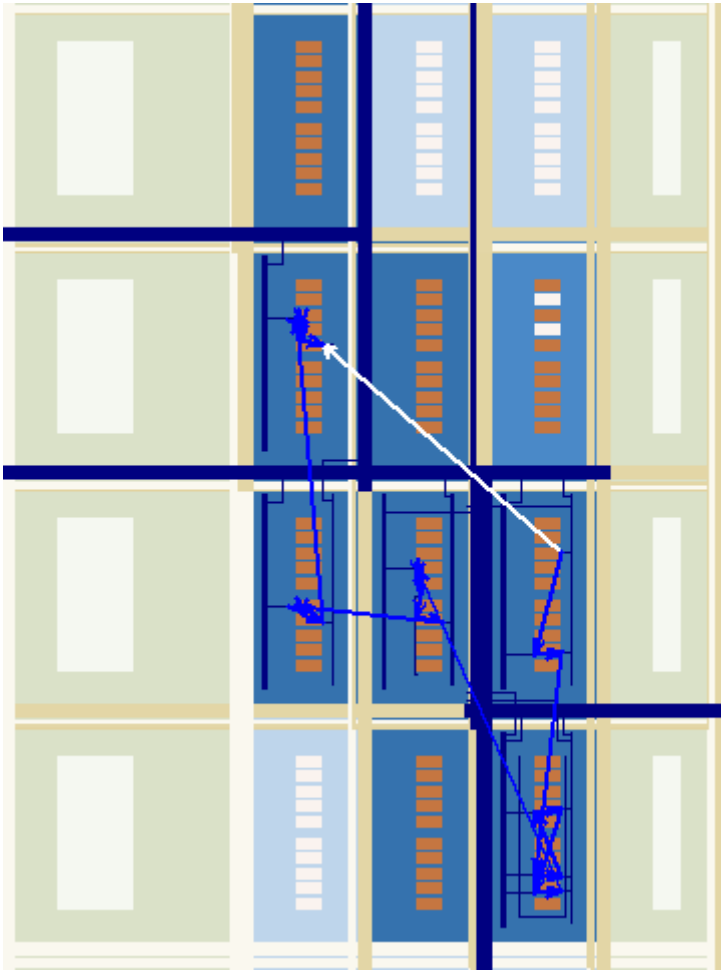
Figure 14–11. Immediate Fan-Out Connection



Highlight Routing

This feature enables you to highlight the routing resources used for a selected path or connection. Figure 14–12 shows the routing resources used between two logic elements.

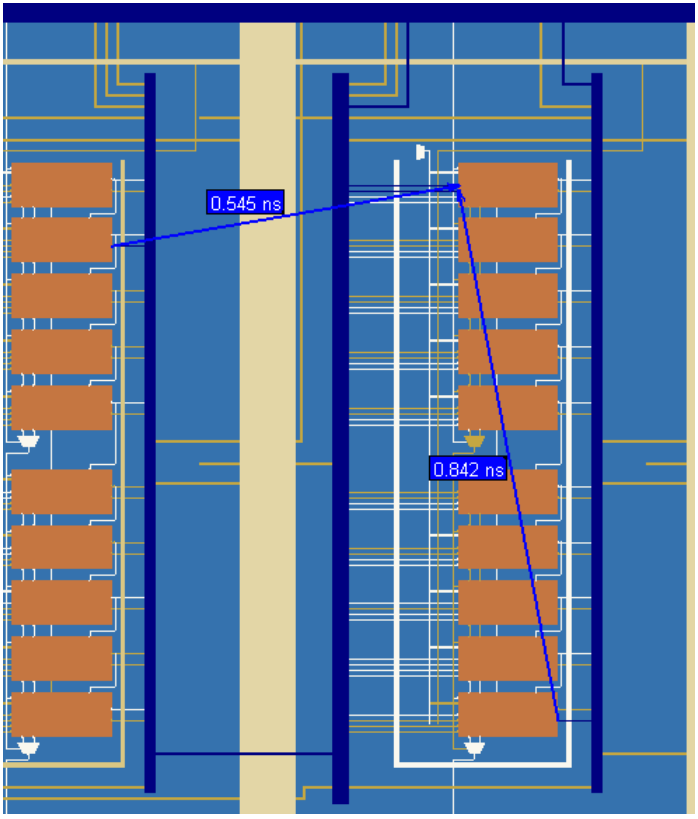
Figure 14–12. Highlight Routing



Show Delays

You can view the timing delays for the highlighted connections when generating connections between elements. For example, you can view the delay between two logic resources or between a logic resource and a routing resource. Figure 14–13 shows the delays between a number of logic elements.

Figure 14–13. Show Delays



Exploring Paths in the Chip Editor

You can use the Chip Editor to explore paths between logic elements. The following example uses the Chip Editor to traverse paths from the Timing Analysis report.

Locate Path from the Timing Analysis Report to the Chip Editor

To locate a path from the Timing Analysis Report to the Chip Editor, perform the following steps:

1. Select the path you want to locate.
2. Right-click on the path in the Timing Analysis Report, right-click **Locate**, then click **Locate in Chip Editor** (Figure 14–14).

The delay that is displayed is the register-to-register delay from the Timing Analysis Report. It doesn't include the skew or micro-parameter calculations.

Figure 14–14. Locate from Timing Analysis Report

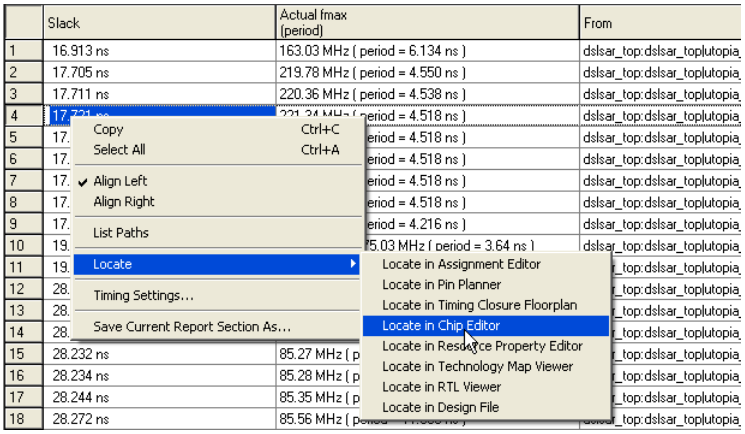
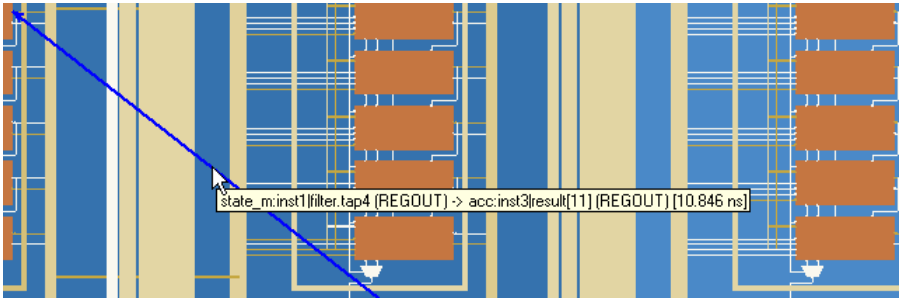


Figure 14–15 shows the path that is displayed in the Chip Editor.

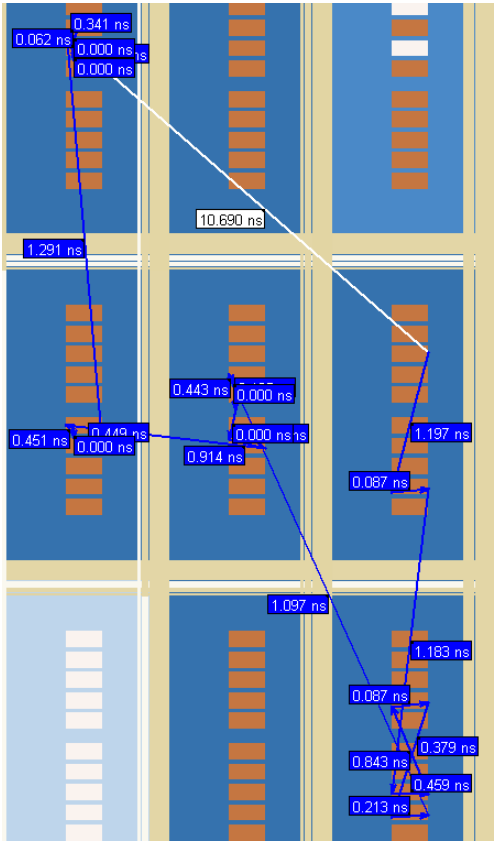
Figure 14–15. Resulting Path



Analyzing Connections for a Path

To determine the connections between items in the Chip Editor, use the **Expand Connections/Paths** icon on the toolbar. To add the timing delays between each connection, use the **Show Delays** icon on the toolbar. Figure 14–16 shows the connections for the selected path that are displayed in the Chip Editor.

Figure 14–16. Path Analysis



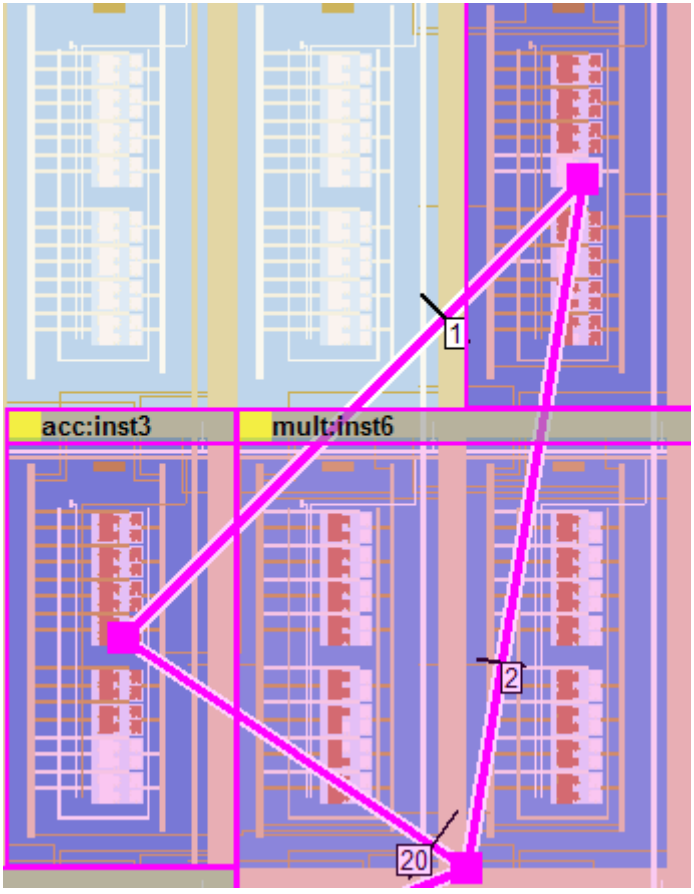
Connection Between LogicLock Regions

Instead of showing multiple connection lines from one LogicLock region to another, you can select the option of viewing connections between LogicLock regions as a single bundled connection (Figure 14–17). To use this option, have the Chip Editor floorplan open, on the View menu, click **Generate inter-region bundles**.

In the **Generate inter-region bundles** dialog box, specify the **Source node to region fanout less than** and the **Bundle width greater than** values.

For more information on the parameters in the **Generate inter-region bundles** dialog box, refer to the Quartus II Help.

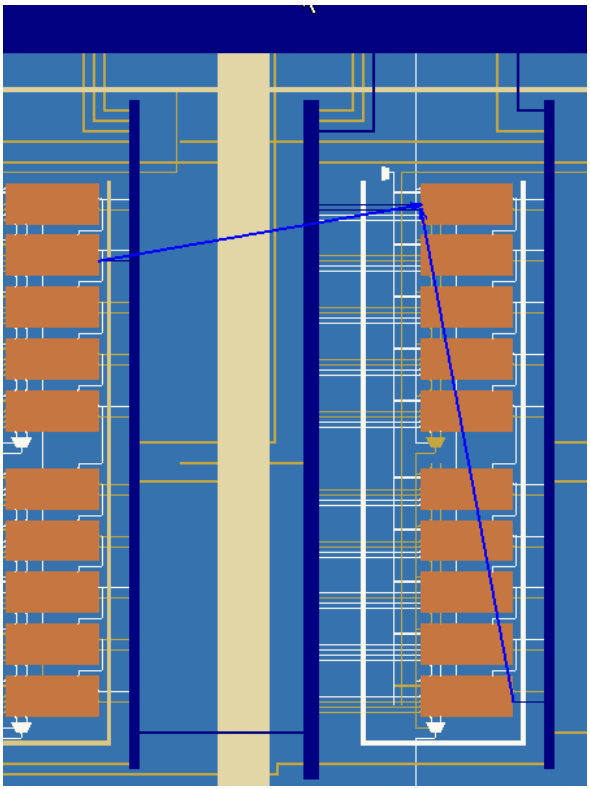
Figure 14–17. Generate Inter-Region Bundles Box



Routing Channels for a Path

To determine the routing channels between connections, click the Highlight Routing icon on the toolbar. Figure 14–18 shows the routing channels used for the selected path in the Chip Editor.

Figure 14–18. Highlight Routing



Resource Property Editor

You can view and edit the following elements with the Resource Property Editor:

- LEs (Stratix, Stratix GX, Cyclone II, Cyclone, MAX II)
- ALMs (Stratix II)
- I/O resources
- PLLs

The Logic Element

An Altera LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a register that is fed by the output of the LUT or by an independent function generated in another LE.

You can use the Resource Property Editor to view and edit any LE in the FPGA. Open the Resource Property Editor for an LE by choosing **Locate in Resource Property Editor** (right-click menu) on an LE from one of the following views:

- Timing Closure
- RTL Viewer
- Node Finder
- Chip Editor

For more information on LE architecture for a particular device family, refer to the device family handbook or data sheet.

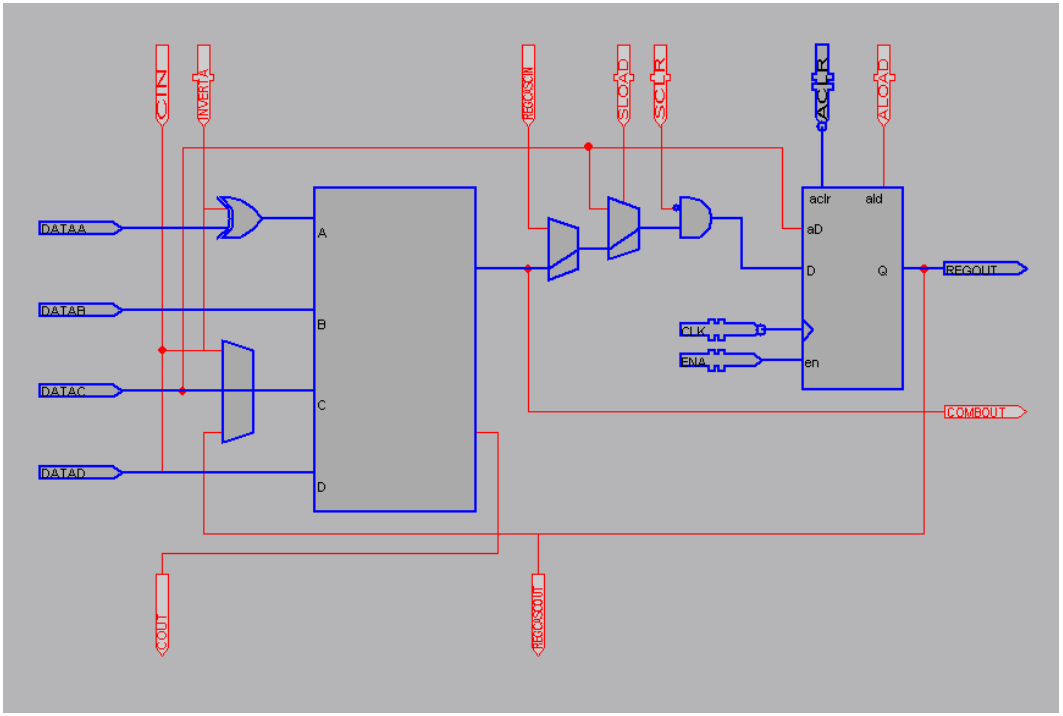
You can use the Resource Property Editor to change the following LE properties:

- Create new LE atoms
- Move existing LE atoms
- Data input to LUT
- LUT mask or LUT equation

Logic Element Schematic View

Figure 14–19 shows how the LE appears in the Resource Property Editor. Figure 14–19 shows an LE that uses the DATAC and DATAD inputs and the COMBOUT output.

Figure 14–19. Stratix LE Architecture *Notes (1), (2)*



Notes to Figure 14–19:

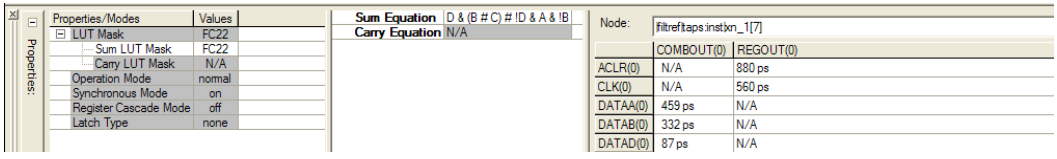
(1) By default, the Quartus II software displays the used resources in blue and the unused in gray. For Figure 14–19, the used resources are in blue and the unused resources are in red.

(2) For more information on the Stratix device's LE Architecture, refer to the *Stratix Device Handbook*.

LE Properties

Figure 14–20 shows the properties that can be viewed for a selected LE in the Resource Property Editor. On the View menu, click **View Properties** to view these properties.

Figure 14–20. LE Properties



Mode of Operation

An LE can operate in either normal or arithmetic mode.

For more information about the modes of operation, refer to volume 1 of the *Stratix Device Handbook*, volume 1 of the *Cyclone Device Handbook*, or the *MAX II Device Handbook*.

When an LE is configured in normal mode, the LUT in the LE can implement a function of four inputs.

When the LE is configured in arithmetic mode, the LUT in the LE is divided into two 3-input LUTs. The first LUT generates the signal that drives the output of the LUT, while the second LUT generates the carry-out signal. The carry-out signal can only drive a carry-in signal of another LE.

Sum & Carry Equation

You can change the logic function implemented by the LUT by changing the SUM & CARRY equation. When the LE is configured in normal mode, you can only change the SUM equation. When the LE is configured in arithmetic mode, you can change both the SUM and the CARRY equation.

The LUT mask is the hexadecimal representation of the LUT equation. When you change the LUT equation, the Quartus II software automatically changes the LUT mask.

When you change the LUT mask, the Quartus II software automatically computes the LUT equation.

Synchronous Mode

When an LE is in synchronous mode, the synchronous load (`sload`) and synchronous clear (`sclr`) signals are used. You can change the LE to synchronous mode by connecting (or disconnecting) the `sload` and `sclr` signals.

You can invert either the `sload` or `sclr` signal feeding into the LE. If the design uses the `sload` signal in an LE, the signal and its inversion state must be the same for all other LEs in the same LAB. For example, if two LEs in a LAB have the `sload` signal connected, both LEs must have the `sload` signal set to the same value. This is also true for the `sclr` signal.

Register Cascade Mode

When register cascade mode is enabled, the cascade-in port feeds the input to the register. The register cascade mode is used most often when the design implements a series of shift registers. You can change the register cascade mode by connecting (or disconnecting) the cascade-in. However, if you create this port, you must ensure that the source port LE is directly above the destination LE.

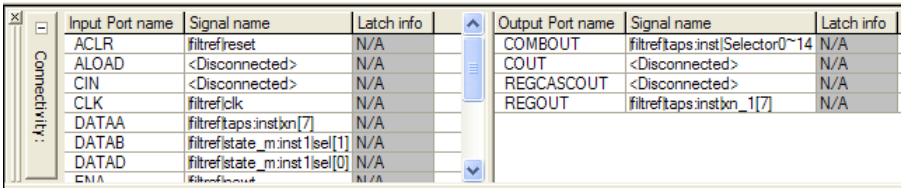
Cell Delay Table

The cell delay table describes the propagation delay from all inputs to all outputs for the selected LE.

LE Connections

On the View menu, click **View Properties** to view the connections that feed in and out of an LE. Figure 14–21 shows the LE connections in the **View Properties** window.

Figure 14–21. View Properties



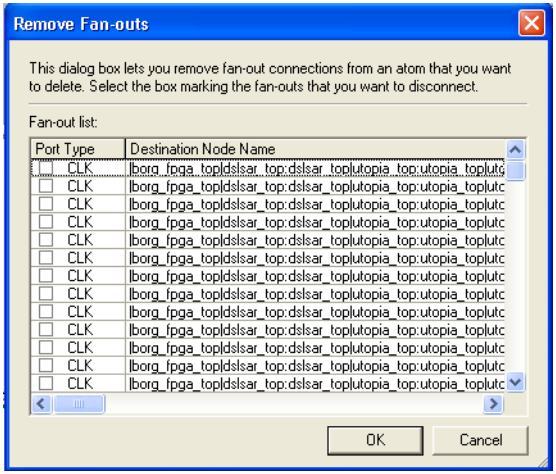
Delete an LE

To delete an LE, perform the following steps:

1. Locate the LE in the Resource Property Editor. Choose Locate from the right-click menu, click **Locate in Resource Property Editor** on an LE.

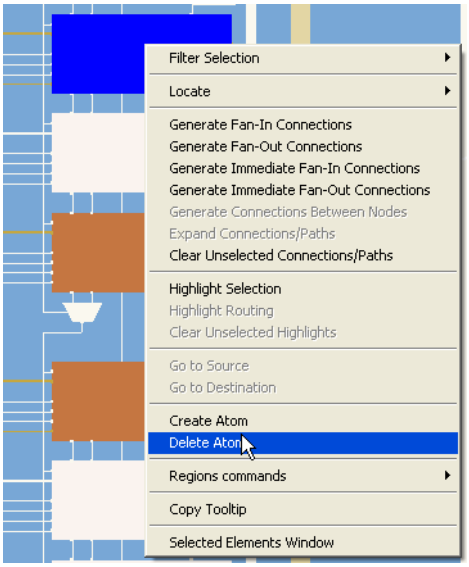
2. Remove Fan-out Connections. After you locate the LE in the Resource Property Editor, delete the fan-out connections. On the right-click menu, choose **Remove**, and click **Fanouts** on all outputs. Figure 14–22 shows the dialog box that appears.

Figure 14–22. Remove Fan-Out Connections



3. Delete an atom after all fan-out connections are removed, reference the atom back in the Chip Editor. Right-click and choose **Delete Atom** (Figure 14–23).

Figure 14–23. Delete Atom

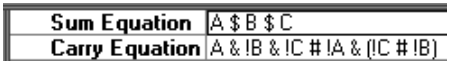


Create a New LE

To create an LE with the Chip Editor, perform the following steps:.

1. On an empty location in the Chip Editor, right-click **Create Atom**.
2. Specify the name of the atom in the **Create Logic Cell Atom** dialog box.
3. After you have created the atom, connect it to other atoms by selecting Edit Connection and clicking Other on an input. In the dialog box that appears, enter the name of the signal that you want to connect to. If you do not know the name of the signal, you can use the Node Finder to find the signal.
4. To modify the functionality of an LE by setting the sum equation. Double-click in the Sum Equation field of the logic cell properties and modify the equation. Figure 14–24 shows the Sum Equation and Carry Equation fields.

Figure 14–24. LUT Equation



The Adaptive Logic Module

The basic building block of logic in the Stratix II architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of LUT-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, each ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can implement any function with up to six inputs and certain seven-input functions. In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers.

You can implement the following types of functions in a single ALM:

- Two independent 4-input functions
- An independent 5-input function and an independent 3-input function
- A 5-input function and a 4-input function, if they share one input
- Two 5-input functions, if they share two inputs
- An independent 6-input functions
- Two 6-input functions, if they share four inputs and share function
- Certain 7-input functions

You can change the following ALM properties:

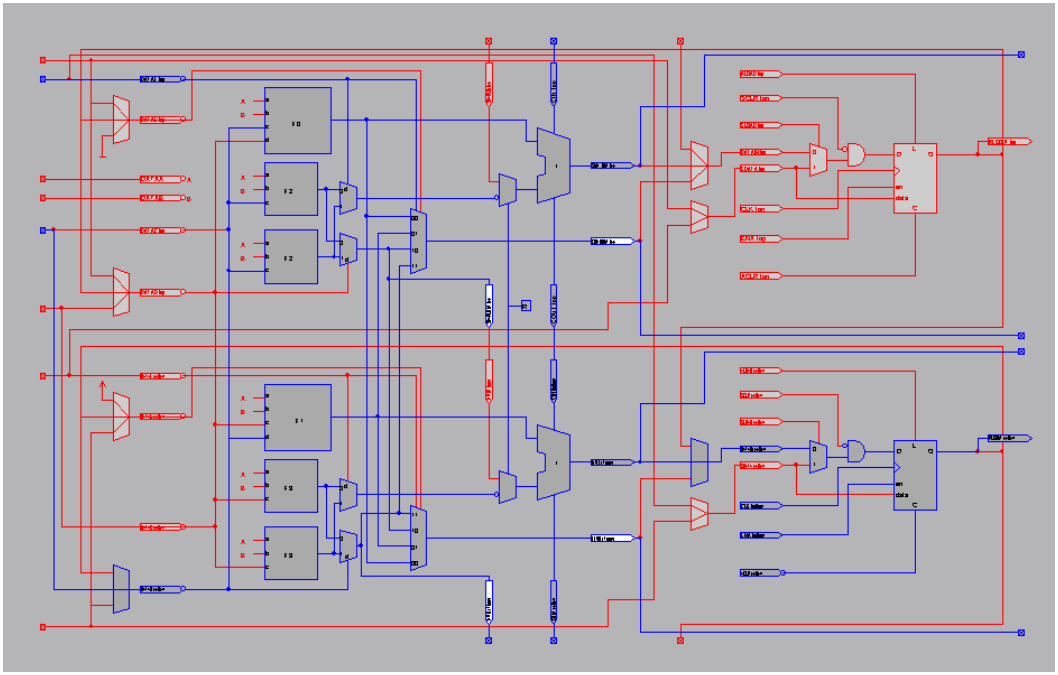
- Create new ALM atoms
- Move existing ALM atoms
- LUT mask or LUT equation

ALM Schematic

You can view and edit any ALM in a Stratix II device with the Resource Property Editor (Figure 14–25). To view a specific ALM in the Resource Property Editor, right-click on the ALM in the Timing Closure Floorplan, RTL Viewer, Node Finder, or Chip Editor. Click **Locate in Resource Property Editor**.

For a detailed description of the ALM, refer to the *Stratix II Device Handbook*.

Figure 14–25. ALM Schematic *Note (1)*



Note to Figure 14–25:

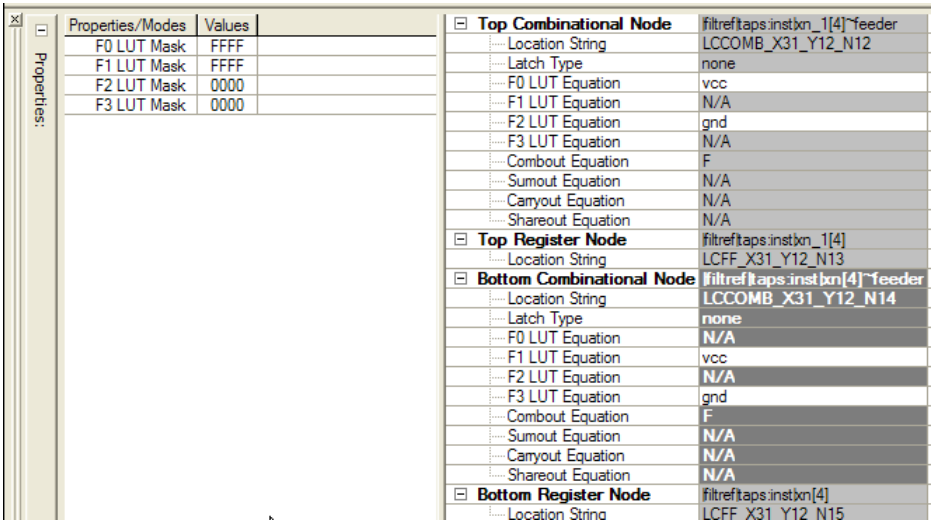
(1) By default, the Quartus II software displays the used resources in blue and the unused in gray. For Figure 14–25, the used resources are in blue and the unused resources are in red.

ALM Properties

The properties displayed for the Stratix II ALM include an equations table that shows the name and location of each of the two combinational nodes and two register nodes in the ALM, the individual LUT equations for each of the combinational nodes and the `combout`, `sumout`, `carryout`, and `shareout` equations for each combinational node.

Figure 14–26 illustrates the properties used by the selected ALM.

Figure 14–26. ALM Properties

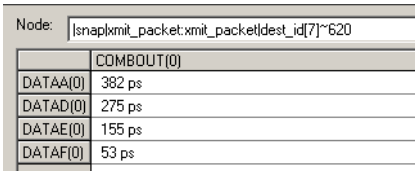


In Figure 14–26, the ALM uses the bottom combinational node. The equation for that node is described in the `combout` equation. To determine which inputs in the ALM are used, examine the equation. In this example, `DATAE` and `DATAF` control the select signals that drive the bottom multiplexer and the `DATAA`, `DATAB` and `DATAC` signals drive the LUTs. The equations for the atom use variables that correspond to the input of the ALM. For example, the `DATAA` input corresponds to the "A" variable in the equation.

ALM Timing Table

Figure 14–27 describes the propagation delay from all inputs to all outputs for the selected ALM.

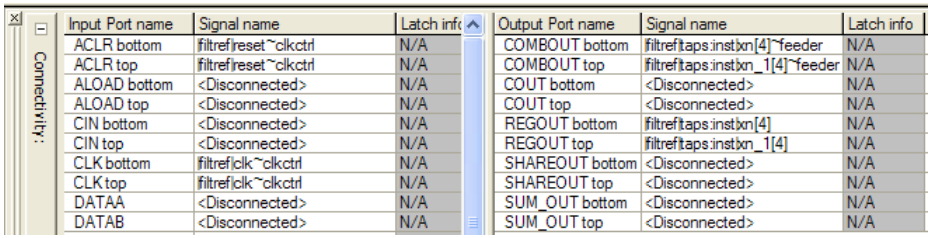
Figure 14–27. ALM Timing



ALM Connections

On the View menu, click **View Properties** to view the connections that feed in and out of an LE (Figure 14–28).

Figure 14–28. ALM Connections



FPGA I/O Elements

Altera FPGAs, with high-performance I/O elements packed with up to six registers, are equipped with support for a number of I/O element standards allowing you to run your design at peak speeds.

For a detailed description of the Stratix II device I/O elements, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

For a detailed description of the Stratix device I/O elements, refer to the *Stratix Architecture* chapter in volume 1 of the *Stratix Device Handbook*.

For a detailed description of the Cyclone II device I/O elements, refer to the *Cyclone II Architecture* chapter in the *Cyclone II Device Handbook*.

For a detailed description of the Cyclone device I/O elements, refer to the *Cyclone Architecture* chapter in volume 1 of the *Cyclone Device Handbook*.

For a detailed description of the MAX II device I/O elements, refer to the *MAX II Architecture* chapter in the *MAX II Device Handbook*.

You can change the following I/O properties:

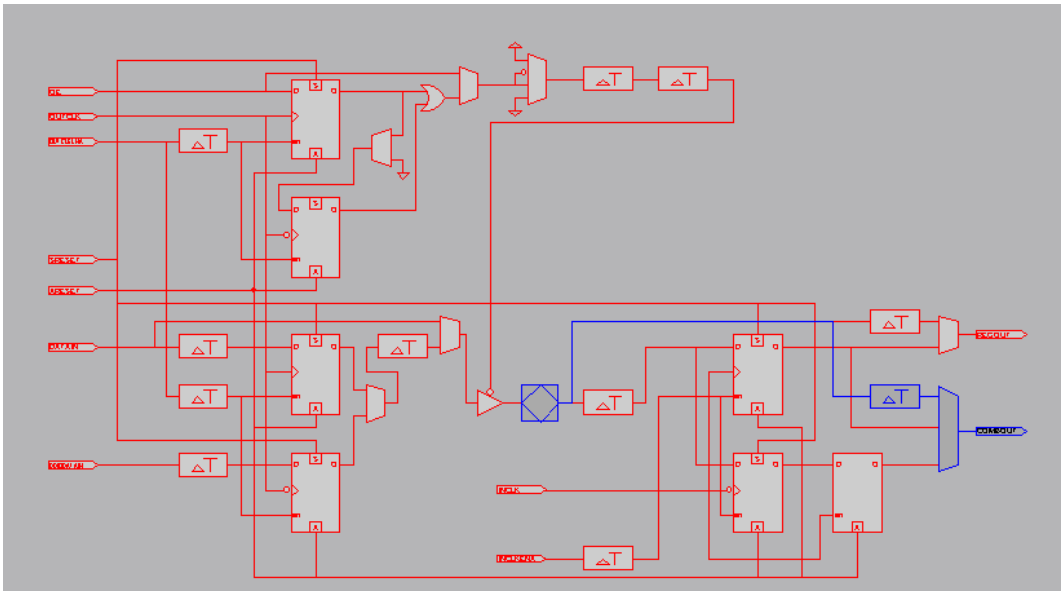
- Create new I/O atom
- Move existing I/O atom
- Delay chain
- Bus hold
- Weak pull up
- Slow slew rate

- I/O standard
- Current strength
- Extend OE disable
- PCI I/O
- Register reset mode
- Register synchronous reset mode
- Register power up
- Register mode

Stratix II, Stratix, & Stratix GX I/O Elements

The I/O elements in Stratix series device families contains a bidirectional I/O buffer, six registers, and a latch for a complete bidirectional single data rate or DDR transfer. Figure 14–29 shows the Stratix and Stratix GX I/O element structure. The I/O element structure contains two input registers (plus a latch), two output registers, and two output enable registers. Figure 14–30 shows the Stratix II I/O element structure.

Figure 14–29. Stratix & Stratix GX Device I/O Element or Structure *Notes (1), (2)*



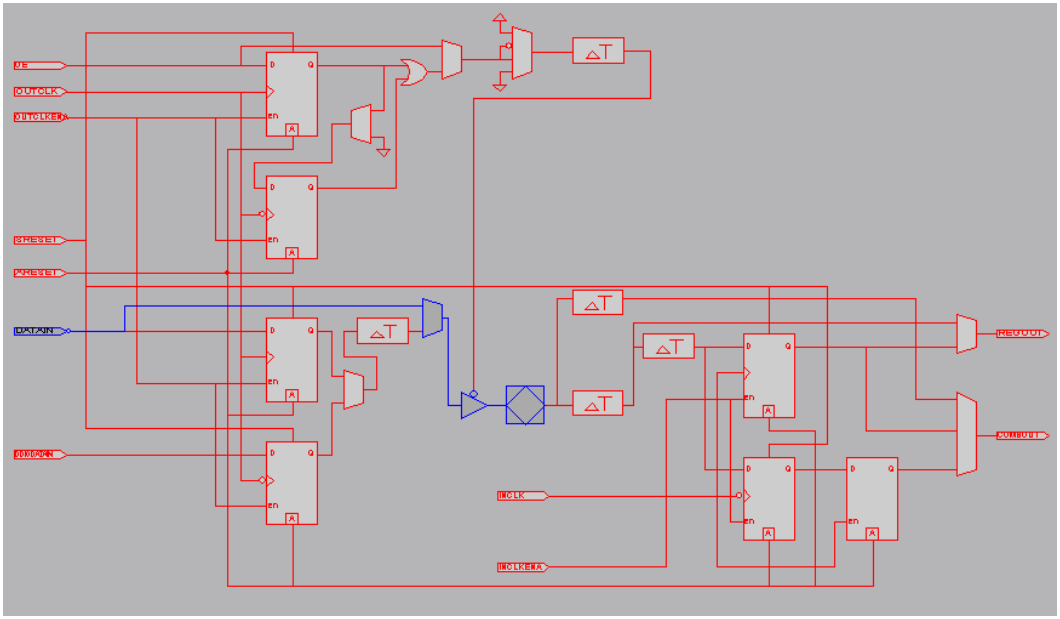
Notes to Figure 14–29:

(1) By default, the Quartus II software displays the used resources in blue and the unused in gray. For Figure 14–29, the used resources are in blue and the unused resources are in red.

(2) For more information on I/O elements in Stratix and Stratix GX devices, refer to the *Stratix Device Handbook* and the *Stratix GX Device Handbook*.

Figure 14–30 shows the Stratix II I/O element structure.

Figure 14–30. Stratix II Device I/O Element or Structure *Notes (1), (2)*



Notes to Figure 14–30:

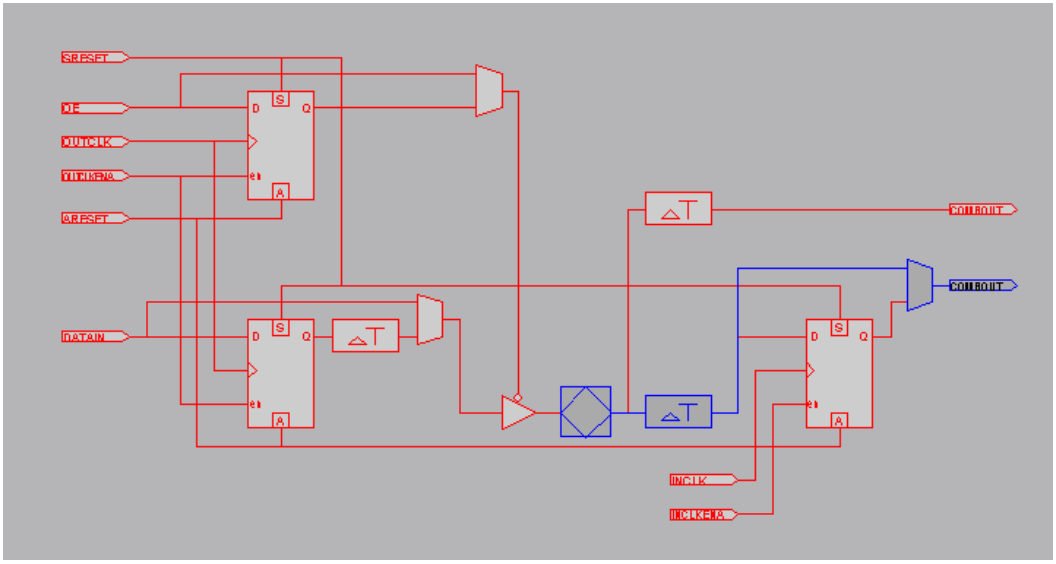
(1) By default, the Quartus II software displays the used resources in blue and the unused in gray. For Figure 14–30, the used resources are in blue and the unused resources are in red.

(2) For more information on I/O elements in Stratix II devices, refer to the *Stratix II Device Handbook*.

Cyclone II & Cyclone I/O Elements

The I/O elements in Cyclone II and Cyclone devices contain a bidirectional I/O buffer and three registers for complete bidirectional single data-rate transfer. Figure 14–31 shows the Cyclone II and Cyclone I/O element structure. The I/O element contains one input register, one output register, and one output enable register.

Figure 14–31. Cyclone II & Cyclone Device I/O Elements or Structure *Notes (1), (2)*



Notes to Figure 14–31:

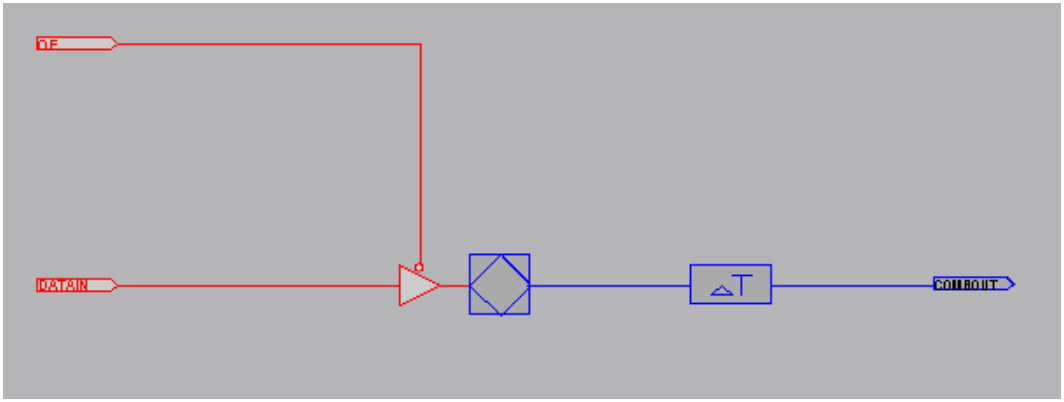
(1) By default, the Quartus II software displays the used resources in blue and the unused in gray. For Figure 14–31, the used resources are in blue and the unused resources are in red.

(2) For more information on I/O elements in Cyclone II and Cyclone devices, refer to the *Cyclone II Device Handbook* and *Cyclone Device Handbook*, respectively.

MAX II I/O Elements

MAX II device I/O elements contain a bidirectional I/O buffer. Figure 14–32 shows the MAX II I/O element structure. Registers from adjacent LABs can drive to or be driven from the I/O element's bidirectional I/O buffers.

Figure 14–32. MAX II Device I/O Elements or Structure *Notes (1), (2)*



Notes for Figure 14–32:

(1) By default, the Quartus II software displays the used resources in blue and the unused in gray. For Figure 14–32, the used resources are in blue and the unused resources are in red.

(2) For more information on I/O elements in MAX II devices, refer to the *MAX II Device Handbook*.

I/O Elements Features in the Resource Property Editor

You use the Resource Property Editor to view, change connectivity, and edit the properties of the I/O elements. You use the Chip Editor to change placement, delete, and create new I/O elements. In addition, all these operations can be performed on Stratix II, Stratix, Stratix GX, Cyclone II, Cyclone, and MAX II devices.

Modifying the PLL Using the Chip Editor

PLLs are used to modify and generate clock signals to meet design requirements. Additionally, PLLs are used for distributing clock signals to different devices in a design, reducing clock skew between devices, improving I/O timing, and generating internal clock signals.

PLL Properties

The Resource Property Editor enables you to modify PLL options, such as phase shift, output clock frequency, and duty cycle. You can also change many of the PLL properties with the Resource Property Editor including the following:

- Input frequency
- M VCO tap
- M initial
- M value
- N value
- M counter delay
- N counter delay
- M2 value
- N2 value
- SS counter
- Charge pump current
- Loop filter resistance
- Loop filter capacitance
- Counter delay
- Counter high
- Counter low
- Counter mode
- Initial
- VCO tap

Adjusting the Duty Cycle

Use the following equation to adjust the duty cycle of individual output clocks:

(1)

High % = Counter High/(Counter High + Counter Low)
Low % = Counter Low/(Counter High + Counter Low)

Adjusting the Phase Shift

Use the following equations to adjust the phase shift of an output clock of a PLL:

(2)

Phase Shift = (Period VCO × 0.125 × Tap VCO) + (Initial VCO × Period VCO)

For a detailed description of the settings, refer to the Quartus II Help. For more information on Stratix device PLLs, refer to the *Stratix Architecture* chapter in volume 1 of the *Stratix Device Handbook*.

For normal node, calculate the phase shift with the following settings:

Tap VCO = Counter Delay - M Tap VCO
Initial VCO = Counter Initial - M Initial
Period VCO = In Clock Period × N / M

For external feedback mode, calculate the phase shift with the following settings:

Tap VCO = Counter Delay - M Tap VCO
Initial VCO = Counter Initial - M Initial
Period VCO = In Clock Period × N / (M + Counter High + Counter Low)

Adjusting the Output Clock Frequency

Use the following equation to adjust the PLL output clock in normal mode:

(3)

$$\text{Output Clock Frequency} = \text{Input Frequency} \cdot \frac{\text{M initial}}{\text{N initial} + \text{Counter High} + \text{Counter Low}}$$

Use the following equation to adjust the PLL output clock in external feedback mode:

(4)

$$\text{OUTCLK} = \text{INCLK} \cdot \frac{\text{M initial} + \text{External Feedback Counter High} + \text{External Feedback Counter Low}}{\text{N initial} + \text{Counter High} + \text{Counter Low}}$$

Adjusting the Spread Spectrum

Use the following equation to adjust the spread spectrum for your PLL:

(5)

$$\%\text{spread} = 1 - \frac{M_2 N_1}{M_1 N_2}$$

Change Manager

The Change Manager maintains a record of every change that you perform with the Resource Property Editor. Each row in the Change Manager represents one change that you made with the Resource Property Editor. The changes are numbered sequentially, such that the larger the number, the more recent the change.

More complex changes are marked in the Change Manager with a "+". You can expand a complex entry in the Change Manager to reveal all the changes that occurred. An example of a complex change is the creation or deletion of an atom.

Table 14–1 summarizes the information shown by the Change Manager.

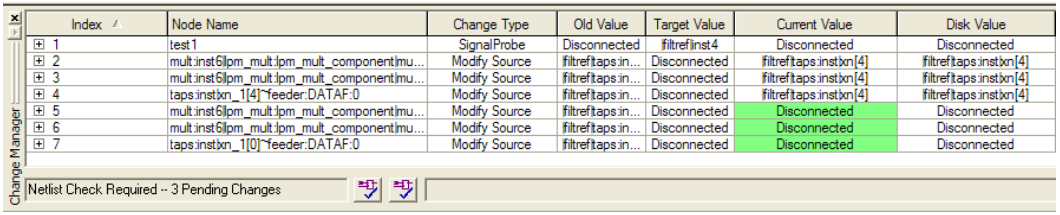
Table 14–1. Change Manager Information

Column Name	Description
Index	Identifies, by a sequential number, change records corresponding to changes made in the Chip Editor or Resource Property Editor. In the case of complex change records, the index column identifies not only the main change, but also any component changes.
Node Name	Uniquely identifies the resource to which a change has been made.
Change Type	Identifies the type of change that has been made to the resource.
Old Value	Lists the value of the resource immediately prior to the change being made.
Target Value	Lists the desired target value (new value) that you have established using the Resource Property Editor, Chip Editor, or SignalProbe.
Current Value	Lists the value of the resource in the netlist that is currently active in memory (as opposed to the value in the netlist saved on disk, which may be different if you have made changes and not yet used the Check and Save All Netlist Changes command). The **Current Value** field can contain one of four possible values: ● current value = old value. Indicates that no change has been applied. ● current value = target value. Indicates that a change has been applied. ● current value = neither old nor target value. Indicates that an invalid change was attempted. ● current value = `Data Not Available` Indicates that you may be using an incomplete data set. This can occur in the following instances: -No netlist exists because the design in use has not been compiled on the current computer. -The node you are trying to change does not exist in the netlist because the source code has been changed. - The node you are trying to change does not exist in the netlist because the node name was originally assigned by the Compiler, and you have subsequently performed a Fitter operation using different optimization parameters, resulting in changed node names.
Disk Value	Lists the current value of the resource on disk.
Comment	Lets you add a comment to a change record in the **Change Manager**. To add a comment to a change record, double-click in the **Comment** field of the record you want to annotate, and type the desired comment.

After you complete all your design modifications, check the integrity of the netlist by right-clicking in the Change Manager and clicking **Check & Save All Netlist Changes**. If the applied changes successfully pass the netlist check, they are written to disk. If the changes do not pass the netlist check, all changes made since the previous successful netlist check are reversed. Figure 14–33 shows the Change Manager.

Colored indicators in the **Current Value** and **Disk Value** columns indicate the present status of the data in those columns. Green in the **Current Value** column indicates that the change has occurred and the value there is the same as the value in memory. Blue in the **Disk Value** column indicates that the change has successfully passed. Choose **Check & Save All Netlist Changes** (right-click menu), and the value in that column is the same as the value on disk.

Figure 14–33. Change Manager Results

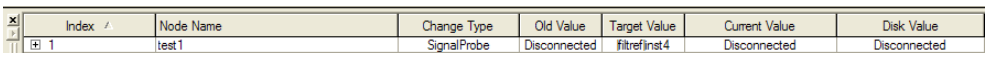


Each line in the Change Manager represents a change record. Simple changes appear as a single line. More complex changes, which require that several actions be performed to achieve the change, appear as a single line marked by a "+". Click on the "+" to show all the component actions performed as part of the change.

Complex Changes in the Change Manager

Certain types of changes that you make in the **Resource Property Editor** or the **Chip Editor** (including creating or deleting atoms and changing connectivity) may appear to be self-contained, but these changes are actually composed of multiple actions. These types of changes are recorded with a "**+**" sign in the **Index** column. Figure 14–34 shows the Change Manager.

Figure 14–34. Change Manager



In the example shown in Figure 14–34, a new atom is created. The change record in the **Change Manager** is a single-line representation of the actual change actions that occurred. You expand the change record to show the component actions that make up the change by clicking the "+" icon (Figure 14–35). When you click the "**+**", it expands the list and becomes "**–**".

Figure 14–35. Change Manager Results

Index	Node Name	Change Type	Old Value	Target Value	Current Value	Disk Value
⊞ 1	test	New Lcell Comb	None	Exists	Exists	None
2	|niosii_mandelbrot_top|mandelbrot_sys:inst|r...	Location Index	LCCOMB_X...	LCCOMB_X...	LCCOMB_X...	LCCOMB_...
3	|niosii_mandelbrot_top|mandelbrot_sys:inst|r...	Location Index	LCCOMB_X...	LCCOMB_X...	LCCOMB_X...	LCCOMB_...
4	|niosii_mandelbrot_top|mandelbrot_sys:inst|r...	Location Index	LCCOMB_X...	LCCOMB_X...	LCCOMB_X...	LCCOMB_...
⊞ 5	|niosii_mandelbrot_top|mandelbrot_sys:inst|r...	Modify Source	|niosii_mand...	Disconnected	Disconnected	Disconnec...

After clicking the "**+**", you can see that creation of an atom consists of three actions:

- The creation of a new logic cell.
- The creation of an output port on the newly created logic cell.
- The assignment of a location index to the newly created logic cell.

You cannot select individual components of a complex change record; if you select any part of a complex change record, the entire complex change record is selected.

For examples of managing changes with the Change Manager, refer to "Example of Managing Changes With the Change Manager" in the Quartus II Help.

Managing SignalProbe Signals

The SignalProbe assignments that you create from the **SignalProbe Pins** dialog box under the Tools menu are recorded in the Change Manager. After you have created a SignalProbe assignment, you can use the Change Manager to quickly disable SignalProbe assignments by selecting **Revert to Last Saved Netlist** from the right- click menu in the Change Manager.

Figure 14–36. Change Manager Results after a SignalProbe Pin is Created

Index	Node Name	Change Type	Old Value	Target Value	Current Value	Disk Value
⊟ 1	test1	SignalProbe	Disconnected	|filtref|inst4	|filtref|inst4	Disconnected
⊞ 1.1	test1	New Output Pin	None	Exists	Exists	None
⊞ 1.2	test1:DATAIN:0	Modify Source	Disconnected	|filtref|inst4	|filtref|inst4	Disconnected

Exporting Changes

You can export all your changes to a tool command language (Tcl) script, a Comma-Separated Value (**.csv)** file, or a Text **(.txt)** file. The Tcl file enables you to write a script that reapplies changes that were erased by compilation. You can also write a script that applies to other Quartus II software projects that you create. The Comma-Separated Value or Text files provide a list of changes in a tabular format. To export changes, perform the following steps:

1. On the right-click menu, choose **Export Changes**.
2. Specify the Tcl file name.
3. Click **OK**.

The resulting Tcl script can also implement similar changes to another Quartus II design.

Common Applications

You can use the Chip Editor functions to help build your system quickly:

- Route an internal signal to an output pin
- Adjust the phase shift of a PLL to meet I/O timing
- Correct a functional flaw in a design

Routing an Internal Signal to an Output Pin

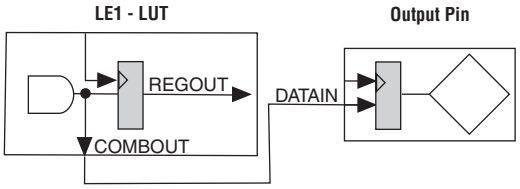
You can use the Chip Editor to route internal signals to unused output pins. This capability allows you to capture signals that are internal to the FPGA with an external logic analyzer.

The process of routing these signals is straightforward and requires very little time, allowing you to spend less time on the setup and more time on debugging.

The following steps describe the process required to route an internal signal to an output pin (Figure 14–37).

1. Create an output pin.

Figure 14–37. Routing an Internal Signal to an Output Pin



2. If a REGOUT or COMBOUT of the source LE does not already exist, create one.

3. Connect the DATAIN of the output pin to the REGOUT or the COMBOUT of the source LE.

4. Optional—Connect a clock to the CLK port of the output pin. Connecting a clock allows you to register the signals before they are driven off-chip.

Adjust the Phase Shift of a PLL to Meet I/O Timing

Using a PLL in your design should help I/O timing. However, if your I/O timing requirements are still unmet, you can adjust the PLL phase shift to try to meet the I/O timing requirements of your design. Shifting the clock backwards gives a better t_{CO} at the expense of the t_{SU}, while shifting it forward gives a better t_{SU} at the expense of t_{CO} and t_{H}.

Use the equations to set the new phase shift value to optimize your I/O timing, shown in "Modifying the PLL Using the Chip Editor" on pages 14–34, to 14–35.

Post-Chip Editor Commands

This section highlights the operations you can perform after making a change in the Chip Editor.

Running the Quartus II Timing Analyzer

After you make a change with the Chip Editor, you should perform timing analysis of your design with the Quartus II Timing Analyzer to ensure that your changes have not adversely affected your design's timing performance.

For example, when you turn on one of the delay chain settings for a specific pin, you change the I/O timing. Therefore, to ensure that all timing requirements are still met, you should perform timing analysis.

Whenever you change your design using the Chip Editor, Altera recommends that you perform a timing simulation on your design with either the Quartus II Simulator or another EDA vendor's simulation tool.

Generating a Netlist for Other EDA Tools

When you use the Chip Editor, it may be necessary to verify the functionality using an Altera-supported simulation tool and/or verify timing using an Altera-supported timing analysis tool. You can run the Netlist Writer to generate a gate-level netlist that allows you to perform simulation or timing analysis in an EDA simulation or timing analysis tool. On the Processing menu, point to **Start**, and click **Start EDA Netlist Writer** to open the Netlist Writer.

Generating a Programming File

After you have performed simulation and timing analysis, and are confident that the changes meet your design requirements, you generate a programming file with the Quartus II Assembler. You use the programming file to implement your design in an Altera device.

Conclusion

As the time-to-market pressure mounts, it is increasingly important to produce a fully functional design in the shortest amount of time. To address this challenge, Altera developed the Quartus II Chip Editor. The Chip Editor allows you to modify the post place-and-route properties of your design. Specifically, you can change certain key properties of the LE, I/O elements, and PLL resources. Most importantly, changes made with the Chip Editor do not require a full recompilation, eliminating the lengthy process of RTL modification, resynthesis, and another place-and-route cycle.

In summary, Chip Editor shortens the verification cycle and brings timing closure to your design in a shorter period of time.

15. In-System Updating of Memory & Constants

QII53012-6.0.0

Introduction

FPGA designs are growing larger in density and are becoming more complex. Designers and verification engineers require more access to the design that is programmed in the device to quickly identify, test, and resolve issues. The in-system updating of memory and constants capability of the Quartus® II software provides read and write access to in-system FPGA memories and constants through the Joint Test Action Group (JTAG) interface, making it easier to test changes to memory contents in the FPGA while the FPGA is functioning in the end system.

This chapter explains how to use the Quartus II In-System Memory Content Editor as part of your FPGA design and verification flow.

Overview

The ability to read and update memories and constants in a programmed device provides more insight into and control over your design. The Quartus II In-System Memory Content Editor gives you access to device memories and constants. When used in conjunction with the SignalTap® II embedded logic analyzer, this feature provides you the visibility required to debug your design in the hardware lab.

For more information on the SignalTap II embedded logic analyzer, refer to the *Design Debugging Using the SignalTap II Embedded Logic Analyzer* chapter in Volume 3 of the *Quartus II Handbook*.

The ability to read data from memories and constants allows you to quickly identify the source of problems. In addition, the write capabilities allow you to bypass functional issues by writing expected data. For example, if a parity bit in your memory is incorrect, you can use the In-System Content Editor to write the correct parity bit values into your RAM, allowing your system to continue functioning. You can also intentionally write incorrect parity bit values into your RAM to check your design's error handling functionality.

Device & Megafunction Support

The following tables list the devices and types of memories and constants that are currently supported by the Quartus II software. Table 15–1 lists the types of memory supported by the MegaWizard® Plug-In Manager and the In-System Memory Content Editor.

Table 15–1. MegaWizard Plug-In Manager Support

Installed Plug-Ins Category	Megafunction Name
Gates	LPM_CONSTANT
Memory Compiler	RAM: 1-PORT, ROM: 1-PORT
Storage	ALTSYNCRAM, LPM_RAM_DQ, LPM_ROM

Table 15–2 lists support for in-system updating of memory and constants for the Stratix® II, Stratix, Cyclone™ II, Cyclone, APEX™ II, APEX 20K, and Mercury™ device families.

Table 15–2. Supported Megafunctions

MegaFunction	Stratix/Stratix II			Cyclone/ Cyclone II	APEX II	APEX 20K	Mercury
	M512 Blocks	M4K Blocks	MegaRAM Blocks				
LPM_CONSTANT	Read/ Write	Read/ Write	Read/ Write	Read/ Write	Read/ Write	Read/ Write	Read/ Write
LPM_ROM	Write	Read/ Write	N/A	Read/ Write	Read/ Write	Write	Read/ Write
LPM_RAM_DQ	N/A	Read/ Write	Read/ Write	Read/ Write	Read/ Write	N/A *(1)*	Read/ Write
ALTSYNCRAM (ROM)	Write	Read/ Write	N/A	Read/ Write	N/A	N/A	N/A
ALTSYNCRAM (Single-Port RAM Mode)	N/A	Read/ Write	Read/ Write	Read/ Write	N/A	N/A	N/A

Note to Table 15–2:

(1) Only write-only mode is applicable for this single-port RAM. In read-only mode, use LPM_ROM instead of LPM_RAM_DQ.

Using In-System Updating of Memory & Constants with Your Design

Using the In-System Updating of Memory and Constants feature requires the following steps:

1. Identify the memories and constants that you want to access.
2. Edit the memories and constants to be run-time modifiable.
3. Perform a full compilation.
4. Program your device.
5. Launch the In-System Memory Content Editor.

Creating In-System Modifiable Memories & Constants

When you specify that a memory or constant is run-time modifiable, the Quartus II software changes the default implementation. A single-port RAM is converted to dual-port RAM, and a constant is implemented in registers instead of look-up tables (LUTs). These changes enable run-time modification without changing the functionality of your design. For a list of run-time modifiable megafunctions, refer to Table 15–1.

To enable your memory or constant to be modifiable, perform the following steps:

1. On the Tools menu, click **MegaWizard Plug-In Manager**.
2. If you are creating a new megafunction, select **Create a new custom megafunction variation**. If you have an existing megafunction, select **Edit an existing custom megafunction variation**.
3. Make the necessary changes to the megafunction based on the characteristics required by your design, turn on **Allow In-System Memory Content Editor to capture and update content independently of the system clock** and type a value in the **Instance ID** text box. These parameters can be found on the last page of the wizard for megafunctions that support in-system updating.

   The Instance ID is a four-character string used to distinquish the megafunction from other in-system memories and constants.

4. Click **Finish**.
5. On the Processing menu, click **Start Compilation**.

If you instantiate a memory or constant megafunction directly using ports and parameters in VHDL or Verilog HDL, add or modify the `lpm_hint` parameter as shown below.

In VHDL code, add the following:

```
lpm_hint => "ENABLE_RUNTIME_MOD = YES,
  INSTANCE_NAME = <instantiation name>";
```

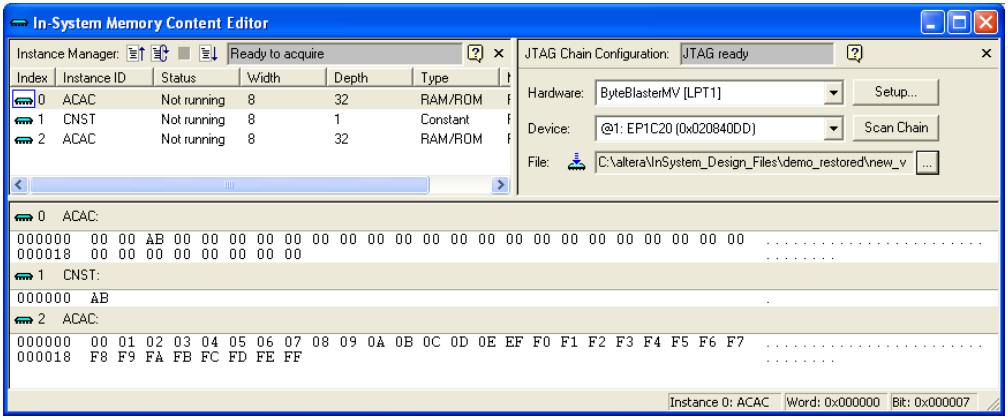
In Verilog HDL code, add the following:

```
defparam <megafunction instance name>.lpm_hint =
  "ENABLE_RUNTIME_MOD = YES,
  INSTANCE_NAME = <instantiation name>";
```

Running the In-System Memory Content Editor

The In-System Memory Content Editor is separated into the Instance Manager, JTAG Chain Configuration, and the Hex Editor (Figure 15–1).

Figure 15–1. In-System Memory Content Editor



The Instance Manager displays all available run-time modifiable memories and constants in your FPGA device. The JTAG Chain Configuration section allows you to program your FPGA and select the Altera® device in the chain to update.

Using the In-System Memory Content Editor does not require that you open a project. The In-System Memory Content Editor retrieves all instances of run-time configurable memories and constants by scanning the JTAG chain and sending a query to the specific device selected in the JTAG Chain Configuration section.

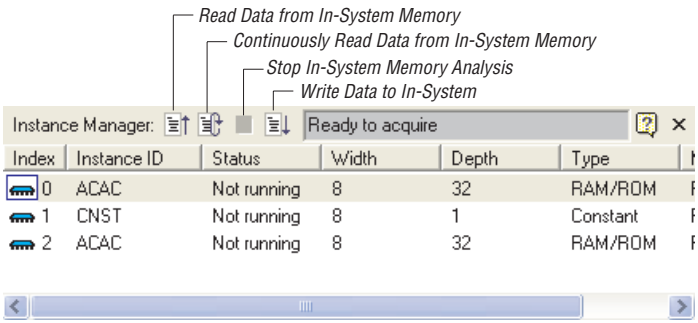
Each In-System Memory Content Editor can access the in-system memories and constants in a single device. If you have more than one device containing in-system configurable memories or constants in a JTAG chain, you can launch multiple In-System Memory Content Editors within the Quartus II software to access the memories and constants in each of the devices.

Instance Manager

Scan the JTAG chain to update the Instance Manager with a list of all run-time modifiable memories and constants in the design. The Instance Manager displays the Index, Instance, Status, Width, Depth, Type, and Mode of each element in the list.

You can read and write to in-system memory using the Instance Manager as shown in Figure 15–2.

Figure 15–2. Instance Manager Controls



The following buttons are provided in the Instance Manger:

- **Read data from In-System Memory**—reads the data from the device independently of the system clock and displays it in the Hex Editor
- **Continuously Read Data from In-System Memory**—Continuously reads the data asynchronously from the device and displays it in the Hex Editor
- **Stop In-System Memory Analysis**—Stops the current read or write operation

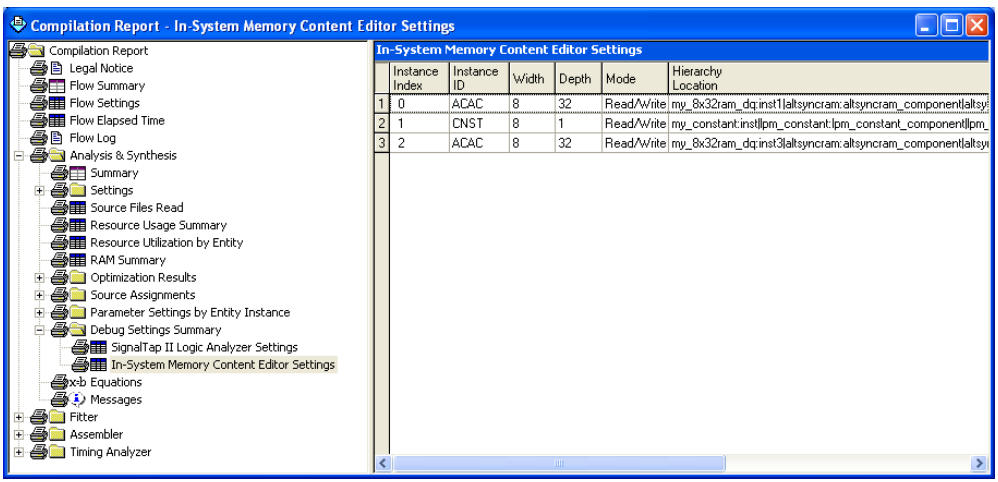
- **Write Data to In-System Memory**—Asynchronously writes data present in the Hex Editor to the device

In addition to the buttons available in the Instance Manager, you can also read and write data by selecting the command from the Processing menu, or the right button pop-up menu in the Instance Manager or Hex Editor.

The status of each instance is also displayed beside each entry in the Instance Manager. The status indicates if the instance is "Not running", "Offloading data" or "Updating Data". The health monitor provides useful information about the status of the editor.

The Quartus II software assigns a different index number to each in-system memory and constant to distinguish between multiple instances of the same memory or constant function. View the **In-System Memory Content Editor Setting** section of the compilation report to match an index with the corresponding instance ID (Figure 15–3).

Figure 15–3. Compilation Report In-System Memory Content Editor Setting Section



Editing Data Displayed in the Hex Editor

You can edit the data read from your in-system memories and constants displayed in the Hex Editor by typing values directly into the editor or by importing memory files.

To modify the data displayed in the Hex Editor, click a location in the editor and type or paste in the new data. The new data appears as blue indicating modified data that has not been written into the FPGA. On the Edit menu, choose Value, and click **Fill with 0's**, **Fill with 1's**, **Fill with Random Values**, or **Custom Fills to** update a block of data by selecting a block of data.

Importing & Exporting Memory Files

Importing and exporting memory files lets you quickly update in-system memories with new memory images and record data for future use and analysis.

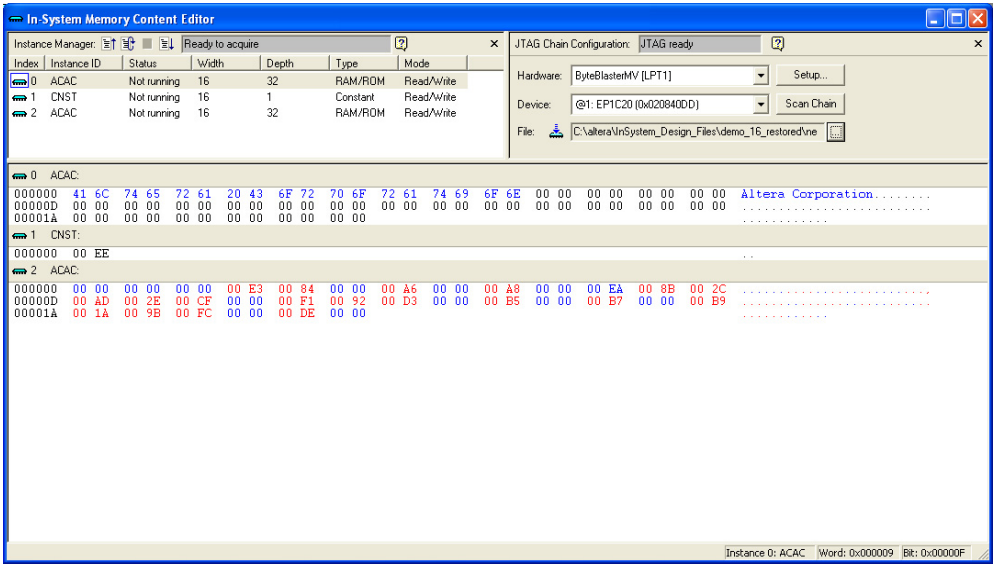
On the Edit menu, click **Import Data from File** to import a memory file, select an in-system memory or constant from the instance manger. You can only import a memory file that is in either a Hexadecimal (Intel-Format) file (**.hex**) or memory initialization file (**.mif**) format.

On the Edit menu, click **Export Data to File** to export data displayed in the Hex Editor to a memory file, to select an in-system memory or constant from the instance manager. You can export data to a HEX, MIF, Verilog Value Change Dump file (**.vcd**), or RAM Initialization file (**.rif**) format.

Viewing Memories & Constants in the Hex Editor

For each instance of an in-system memory or constant, the Hex Editor displays data in hexadecimal representation and ASCII characters (if the word size is a multiple of 8 bits). The arrangement of the hexadecimal numbers depends on the dimensions of the memory. For example, if the word width is 16 bits, the Hex Editor displays data in columns of words that contain columns of bytes (Figure 15–4).

Figure 15–4. Editing 16-Bit Memory Words Using the Hex Editor



Unprintable ASCII characters are represented by a period (.). The color of the data changes as you perform reads and writes. Data displayed in black indicates the data in the Hex Editor was the same as the data read from the device. If the data in the Hex Editor changes color to red, the data previously shown in the Hex Editor was different from the data read from the device.

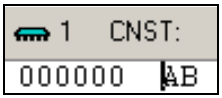
As you analyze the data, you can use the cursor and the status bar to quickly identify the exact location in memory. The status bar is located at the bottom of the In-System Memory Content Editor and displays the selected instance name, word position, and bit offset (Figure 15–5).

Figure 15–5. Status Bar in the In-System Memory & Content Editor

The bit offset is the bit position of the cursor within the word. In the following example, a word is set to be 8-bits wide.

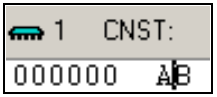
With the cursor in the position shown in Figure 15–6, the word location is 0x0000 and the bit position is 0x0007.

Figure 15–6. Hex Editor Cursor Positioned at Bit 0×0007



With the cursor in the position shown in Figure 15–7, the word location remains 0x0000 but the bit position is 0x0003.

Figure 15–7. Hex Editor Cursor Positioned at Bit 0×0003



Programming the Device Using the In-System Memory Content Editor

If you make changes to your design, you can program the device from within the In-System Memory Content Editor. To program the device, follow these steps:

1. On the Tools menu, click **In-System Memory Content Editor**.
2. In the **JTAG Chain Configuration** panel of the In-System Memory Content Editor, select the SRAM object file (**.sof**) that includes the modifiable memories and constants.
3. Click **Scan Chain**.
4. In the **Device** list, select the device you want to program.
5. Click **Program Device**.

Example: Using the In-System Memory Content Editor with the SignalTap II Embedded Logic Analyzer

The following scenario describes how you can use the In-System Updating of Memory and Constants feature with the SignalTap II embedded logic analyzer to efficiently debug your design in-system. Although both the In-System Content Editor and the SignalTap II embedded logic analyzer use the JTAG communication interface, you are able to use them simultaneously.

After completing your FPGA design, you find that the characteristics of your FIR filter design are not as expected.

1. To locate the source of the problem, you change all your FIR filter coefficients to be in-system modifiable and instantiate the SignalTap II embedded logic analyzer.

2. Using the SignalTap II embedded logic analyzer to tap and trigger on internal design nodes, you find the FIR filter to be functioning outside of the expected cut-off frequency.

3. Using the **In-System Memory Content Editor**, you check the correctness of the FIR filter coefficients. Upon reading each coefficient, you discover that one of the coefficients is incorrect.

4. Since your coefficients are in-system modifiable, you update the coefficients with the correct data using the **In-System Memory Content Editor**.

In this scenario, you are able to quickly locate the source of the problem using both the In-System Memory Content Editor and the SignalTap II embedded logic analyzer. You are also able to verify the functionality of your device by changing the coefficient values before modifying the design source files.

An extension to this example would be to modify the coefficients with the In-System Memory Content Editor to vary the characteristics of the FIR filter (for example, filter attenuation, transition bandwidth, cut-off frequency, and windowing function).

Conclusion

The In-System Updating of Memory and Constants feature provides access into a device for efficient debug in a hardware lab. You can use In-System Memory Updating of Memory and Constants with the SignalTap II embedded logic analyzer to maximize the visibility into an Altera FPGA. By increasing visibility and access to internal logic of the device, you are able to more quickly identify and resolve problems with your design or its implementation.

Section V. Formal Verification

The Quartus® II software easily interfaces with EDA formal design verification tools such as the Cadence Incisive Conformal and Synplicity Synplify software. In addition, the Quartus II software has built-in support for verifying the logical equivalence between the synthesized netlist from Synplicity Synplify and the post-fit Verilog Quartus Mapped (**.vqm**) files using Incisive Conformal software.

This section discusses formal verification, how to set-up the Quartus II software to generate the VQM file and Incisive Conformal script, and how to compare designs using Incisive Conformal software.

This section includes the following chapters:

Revision History

Chapter 12, *In-System Updating of Memory & Constants* was moved to section IV, in volume 3 of the *Quartus II Handbook*.

The table below shows the revision history for Chapters 16 and 17.

Chapter(s)	Date / Version	Changes Made
16	May 2006 v6.0.0	Chapter title changed. Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 14 was previously Chapter 12 in version 5.0.
	May 2005 v5.0.0	• Updates to tables and figures. • New functionality for Quartus II software 5.0.0.
	Dec. 2004 v2.1	• Chapter 13 was formerly Chapter 12. • Updates to tables and figures. • New functionality for Quartus II software 4.2.
	June 2004 v2.0	• Updates to tables, figures. • New functionality for Quartus II software 4.1. • This chapter was formerly chapter 11 in the previous section.
	Feb. 2004 v1.0	Initial release.
17	May 2006 v6.0.0	Minor updates for the Quartus II software version 6.0.0.
	October 2005 v5.1.0	• Updated for the Quartus II software version 5.1. • Chapter 15 was previously Chapter 13 in version 5.0.
	May 2005 v5.0.0	New functionality for Quartus II software 5.0.
	Jan 2005 v1.0	Initial release.

16. Cadence Encounter Conformal Support

QII53011-6.0.0

Introduction

The Quartus® II software provides formal verification support for Altera® designs through interfaces with formal verification EDA tools including the Cadence Encounter Conformal software.

Use the Encounter Conformal software to verify the functional equivalence of a post-synthesis Verilog Quartus Mapping netlist from the Synplicity Synplify Pro software, and a post-fit Verilog Output File from the Quartus II software. You can also use the Encounter Conformal software to verify the functional equivalence of the register transfer level (RTL) source code and post-fit Verilog Output File from the Quartus II software when using Quartus II integrated synthesis. These formal verification flows support designs for the Stratix®, Stratix II, Stratix GX, Stratix II GX, and HardCopy® II, device families.

There are two types of formal verification such as equivalence checking and model checking. This chapter discusses equivalence checking using the Encounter Conformal software.

This chapter discusses the following topics:

- Formal Verification Design Flow
- RTL Coding for Quartus II Integrated Synthesis
- Generating the Verilog Output File & the Encounter Conformal Setup Files
- The Quartus II Software Scripts for Encounter Conformal
- Comparing Designs Using Encounter Conformal
- Debugging Tips
- Known Issues & Limitations
- Tcl Sample Script
- Black Box Models

Equivalence checking uses mathematical techniques to compare the logical equivalence of the two versions of the same design rather than using test vectors to perform simulation. Equivalence checking greatly shortens the verification cycle of the design.

Formal Verification Versus Simulation

Formal verification cannot be considered as a replacement to the vector based simulation. Formal verification only complements the existing vector-based simulation techniques to speed up the verification cycle.

Vector based simulation techniques are used to do the following:

- Check design functionality
- Check timing specifications
- Debug designs

Formal Verification: What You Need to Know

Formal Verification reduces the verification cycle, however, there is an impact on area and performance. The following factors affect the area and performance:

- Hierarchy preservation
- ROM implementation by logic elements (LEs)
- Retiming is disabled

In addition to these factors, formal verification is not supported in the Altera incremental compilation flow. Refer to "Known Issues & Limitations" on page 16–25 before you consider using the formal verification flow in your design methodology.

Formal Verification Design Flow

Altera supports formal verification using the Encounter Conformal software for the following two synthesis tools:

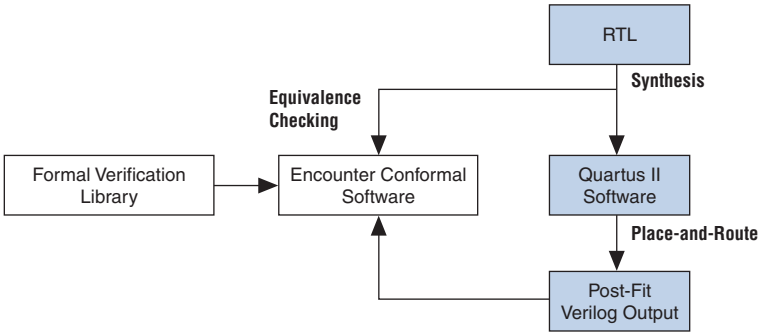
- Quartus II Integrated Synthesis
- Synplify Pro

This section describes the supported design flows for both of these synthesis tools.

Quartus II Integrated Synthesis

The design flow for formal verification using the Quartus II integrated synthesis is shown in Figure 16–1. This flow performs equivalency checking for the RTL source code and the post-fit Verilog Output netlist generated by the Quartus II software.

Figure 16–1. Formal Verification Using Quartus II Integrated Synthesis & the Encounter Conformal Software



EDA Tool Support for Quartus II Integrated Synthesis

The formal verification flow using the Quartus II software and Cadence Encounter Conformal software supports the following software versions and operating systems:

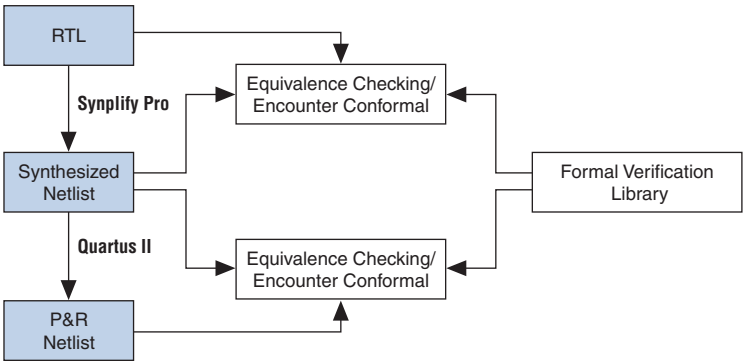
- Quartus II software beginning with version 4.2
- Cadence Encounter Conformal software beginning with 4.3.5.A
- Solaris and Linux operating systems

Synplify Pro

The design flow for formal verification using Synplify Pro Synthesis performs equivalency checking for the post-synthesis netlist from Synplify Pro and the post place-and-route netlist from the Quartus II software. Synplify Pro also supports equivalency checking between RTL and the post synthesis netlist using Encounter Conformal software as shown in the Figure 16–2.

For additional information on performing equivalency checking between RTL and post-synthesis netlist, refer to the Synplify Pro documentation.

Figure 16–2. Formal Verification Flow Using Synplify Pro & the Encounter Conformal Software



EDA Tool Support for Synplify Pro

The formal verification flow using the Quartus II software, the Synplicity Synplify Pro, and the Cadence Encounter Conformal software supports the software versions and operating systems shown in Table 16–1.

Table 16–1. Compatible Software Versions

Software Package	Compatible Versions	Compatible Versions	Compatible Versions
Quartus II Software	Version 4.2	Version 5.0	Version 5.1 or later
Synplify Pro	Version 8.0	Version 8.1	Version 8.4
Encounter Conformal	Version 4.3.5A or greater	Version 5.1.0 or greater	Version 5.1.0 or later

RTL Coding for Quartus II Integrated Synthesis

The Cadence Encounter Conformal software compares the RTL code against the post-fit Verilog Output netlist generated by the Quartus II software. The Encounter Conformal software and the Quartus II integrated synthesis handle the RTL description in slightly different ways. The Quartus II software supports some RTL features that the Encounter Conformal software does not support and vice versa. The style of the RTL code is of particular concern because neither tool supports some constructs, leading to potential formal verification mismatches; for example, state machine extraction, wherein different encoding mechanisms can result in different structures. Therefore, for successful verification, both tools must interpret the RTL code in the same manner.

The following section provides information on recognizing and preventing problems that can arise in the formal verification flow. Altera recommends that you read the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook* for more details on RTL coding styles for the Quartus II Integrated Synthesis.

Some of the coding guidelines apply to both Quartus II Integrated Synthesis and Synplify Pro flow as indicated in each of the guidelines in the following sections.

Synthesis Directives & Attributes

Synthesis directives, also known as pragmas, play an important role in successful verification of RTL against the post-fit Verilog Output netlist from the Quartus II software.

Pragmas and trigger keywords are supported in Quartus II integrated synthesis and Encounter Conformal are also supported in the formal verification flow. The Quartus II integrated synthesis and Encounter Conformal both support the trigger keywords `synthesis` and `synopsys`. When the Quartus II software does not recognize a keyword such as `verplex`, the Encounter Conformal Script file (CTC) disables the keyword. Therefore, it is important to use caution with unsupported pragmas because they can lead to verification mismatches. For example, you can use the Quartus II integrated synthesis to synthesize the RTL code with the synthesis directive `read_comments_as_HDL`.

Verilog HDL Example of Read Comments as HDL

```
// synthesis read_comments_as_HDL on
// my_rom lpm_rom (.address (address),
// .data (data));
// synthesis read_comments_as_HDL off
```

VHDL Example of Read Comments as HDL

```
-- synthesis read_comments_as_HDL on
-- my_rom : entity lpm_rom
-- port map (
-- address => address,
-- data => data, );
-- synthesis read_comments_as_HDL off
```

The Encounter Conformal software does not support the synthesis directive `read_comments_as_HDL`, and the directive has no affect on the Encounter Conformal software.

Table 16–2 lists supported pragmas and trigger keywords for formal verification.

Table 16–2. Supported Pragmas & Trigger Keywords for Formal Verification

Pragmas *(1)*	Trigger Keywords
full_case parallel_case pragma synthesis_off synthesis_on translate_off translate_on	synthesis synopsys

Note to Table 16–2:

(1) Do not use Verilog 2001-style pragma declarations. The Quartus II software and the Encounter Conformal software support this style of pragma in different manners.

Stuck-at Registers

Quartus II integrated synthesis eliminates registers that have their output stuck at a constant value. Quartus II integrated synthesis gives a warning message and adds an entry to the corresponding report panel in the formal verification folder of the Analysis and Synthesis section of the

Compilation Report. If Conformal LEC does not find the same optimizations, it can lead to unmapped points in the golden netlist. The following example illustrates the issue:

```
module stuck_at_example {clk, a,b,c,d,out};
input a,b,c,d,clk;
output out;
reg e,f,g;
    always @(posedge clk) begin
        e <= a & g;// e is stuck at 0
        g <= c & e;// g is stuck at 0
        f <= e | b;
    end
assign out = f & d;
endmodule
```

In this module description, registers `e` and `g` are tied to logic `0`. In this example, the Quartus II software generates the following warning message:

```
Warning: Reduced register "g" with stuck data_in port to stuck value GND
Warning: Reduced register "e" with stuck data_in port to stuck value GND
```

Quartus II integrated synthesis then adds a command to the CTC telling Conformal LEC that a register is stuck at a constant value as shown in the following example:

```
// report floating signals
// Instance-constraints commands for constant-value registers removed
// during compilation
// add instance constraints 0 e -golden
// add instance constraints 0 g -golden
```

The command is commented in the formal verification script, forcing the Encounter Conformal software to treat the register as stuck at a constant value, and potentially hiding a compilation error. You must verify the input to the `e` and `g` registers is constant in the design and uncomment the command to obtain accurate results.

Altera recommends recoding your design to eliminate "stuck-at" registers.

The stuck-at register information in this section also applies to the Synplify Pro flow.

ROM, LPM_DIVIDE & Shift Register Inference

For the purpose of formal verification, the Quartus II integrated synthesis implements both ROM and shift registers in the form of LEs instead of using dedicated on-chip memory resources. Using LEs can be less area-efficient than inferring a megafunction that can be implemented in a RAM block. However, the Quartus II software generates a warning message that indicates that the megafunction was not inferred. Quartus II integrated synthesis also reports a suggested ROM or shift register instantiation that enables you to either use the MegaWizard® Plug-In Manager to create the appropriate megafunction explicitly, or to isolate the corresponding logic in a separate entity that you can set as a black box. If the black-box properties are set on the corresponding megafunction before synthesis, you can verify the megafunction with the Encounter Conformal software.

If the design contains division functionality, then the Quartus II software infers an `lpm_divide` megafunction which is treated as a black box for the purpose of formal verification.

RAM Inference

When the Quartus II software infers the LPM megafunction `altsyncram` from the RTL, the Quartus II software generates the following warning:

```
Created node "<mem_block_name>" as a RAM by generating altsyncram megafunction to
implement register logic with M512 or M4K memory block or M-RAM. Expect to get an error
or a mismatch for this block in the formal verification tool.
```

This warning is generated because the memory block (`altsyncram`) is a new instance in the post-fit Verilog Output netlist that is handled as a black box by the formal verification tool. However, no such instance exists in the original RTL design, resulting in mismatch or error reporting in the formal verification tool.

Latch Inference

A latch is implemented in the Quartus II integrated synthesis using a combinational feedback loop. The Encounter Conformal software infers a latch primitive in the Encounter Conformal library (DLAT) to implement a latch. This results in having a DLAT on the golden side and a combinational loop with a cut point on the revised side, leading to verification mismatches. The Quartus II software issues a warning message whenever a latch is inferred, and the Quartus II software adds an entry to the report panel in the Formal Verification folder of the

Analysis and Synthesis report. Altera recommends that you avoid latches in your design, however, if latches are necessary, Altera recommends using the corresponding `lpm_latch` megafunction.

For more information on the problems related to latches, refer to the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook*.

Combinational Loops

If the design consists of an intended combinational loop, you must define an appropriate cut point for both the RTL and the post-fit Verilog Output netlist. A warning that a combinational loop exists in the design is found in the Formal Verification sub-folder of the Quartus II software Analysis and Synthesis report.

Finite State Machine Coding Styles

When a state machine is inferred by the Encounter Conformal software, it uses sequential encoding as the default encoding when no user-encoding is present. The Quartus II software selects the encoding most suited for the inferred state machine if the State Machine Processing Settings on the Analysis & Synthesis settings page of the Settings dialog box is set to the default value Auto. Therefore, it is important to use the coding style described in the *Recommended HDL Coding Styles* chapter in volume 1 of the *Quartus II Handbook* on RTL when writing finite state Machines (FSMs). This allows the Quartus II integrated synthesis and the Encounter Conformal software to infer a similar state machine for the same RTL code.

Generating the Verilog Output File & the Encounter Conformal Setup Files

The following steps describe how to set up the Quartus II software environment to generate the post-fit Verilog Output netlist and the Encounter Conformal script for use in formal verification. With the exception of step 3, the steps are identical for both of the Synthesis tools:

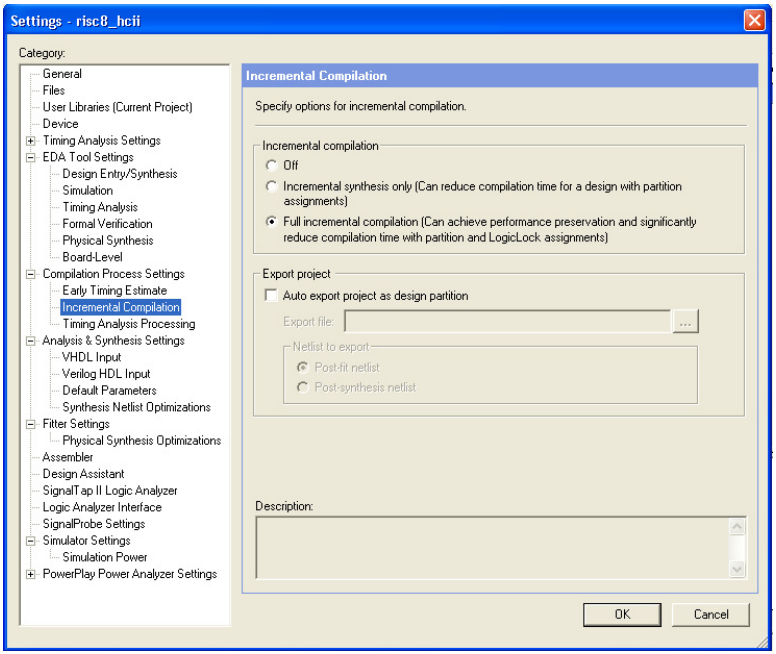
1. Create a new Quartus II project or open an existing project.
2. On the Assignments menu, click **EDA Tool Settings**. The Settings dialog box displays.
3. In the **Category** list, click **EDA Tool Settings**.

   If you are using the Quartus II integrated synthesis, use the following steps:

   a. In the **Category** list, under **EDA Tool Settings**, select **Design Entry/Synthesis**. Select **<*None*>** from the Tool name list.

   b. In the **Category** list, under **EDA Tool Settings**, select **Formal Verification**. Select **Conformal LEC** from the Tool name list (Figure 16–3).

Figure 16–3. Compilation Process Settings



If you are using Synplify Pro, use the following steps:

a. In the **Category** list, under **EDA Tool Settings**, select **Design Entry/Synthesis**. Select **Synplify Pro** from the Tool name list.

b. In the **Category** list, under **EDA Tool Settings**, select **Formal Verification**. Select **Conformal LEC** from the Tool name list.

4. In the **Category** list, select **Compilation Process Settings**. In the **Category** list, under **Compilation Process Settings**, select **Incremental Compilation**.

   In the **Incremental Compilation** page, click **Full Incremental Compilation** to turn on Incremental Compilation.

   or

   Turn on Incremental Compilation by using the following Tcl command:

   ```
   set_global_assignment -name INCREMENTAL_COMPILATION
   FULL_INCREMENTAL_COMPILATION
   ```

   If Incremental Compilation is turned **On** for Formal Verification, then your design should not contain any user created partitions.

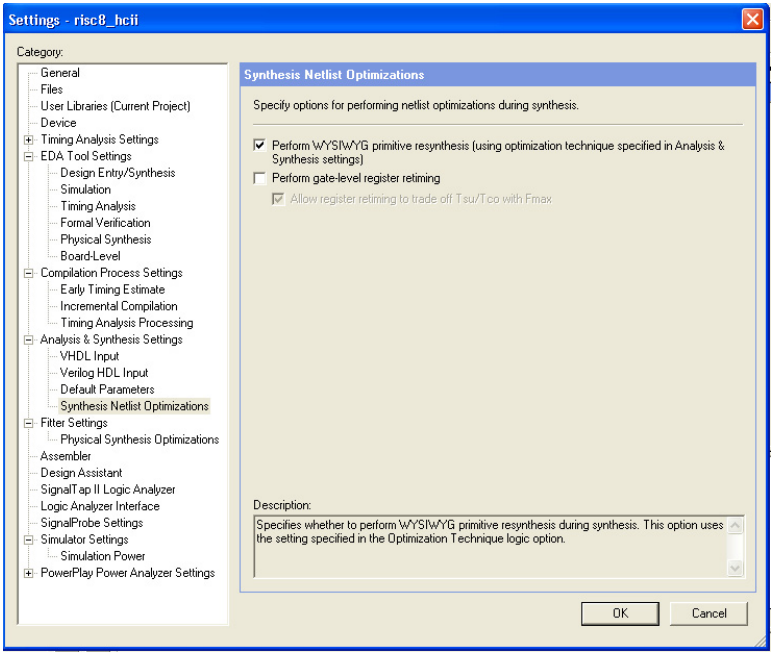
   The Quartus II software allows you to select up to six EDA tools in the EDA tool settings list.

5. In the **Category** list, select **Analysis & Synthesis Settings** to expand the options list, and click **Synthesis Netlist Optimizations**. In the **Synthesis Netlist Optimizations** page, turn off **Perform gate-level register retiming** (Figure 16–4).

   If Perform gate-level register retiming is not turned off, the Encounter Conformal script can display a different set of compare points, making the resulting netlist difficult to compare against the reference netlist file.

Figure 16–4. Synthesis Netlist Optimizations

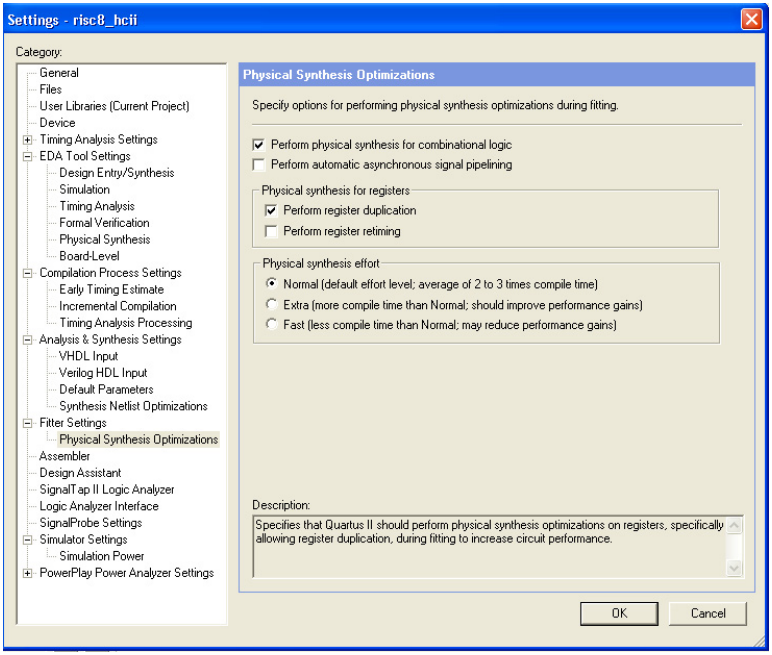


6. In the **Category** list, select **Fitter Settings,** and select **Physical Synthesis Optimizations**. In the **Physical Synthesis Optimizations** page**,** turn on **Perform Register duplication**, and turn off **Perform register retiming** (Figure 16–5).

If the options **Perform gate-level register retiming** (Figure 16–4) and **Perform register retiming** (Figure 16–5) are not turned off, the Encounter Conformal script can display a different set of compare points, making the resulting netlist difficult to compare against the reference netlist file.

For the purpose of Formal Verification, you must turn off the **Perform register retiming** and **Perform gate-level register retiming** options.

Figure 16–5. Fitter Settings



Retiming a design usually results in moving and merging registers along the critical path and is not well supported by the equivalence checking tools. Because equivalence checkers compare the cone of logic terminating at registers, do not move the registers during optimization in the Quartus II software.

7. In the Category list, click **Fitter Settings**, and click **Physical Synthesis Optimizations**. Under **Physical synthesis for registers**, turn on **Perform Register duplication,** and turn off **Perform register retiming** (Figure 16–5).

   The Quartus II software performs register duplication to improve performance. The generated scripts contain information about the duplicated registers that enable successful formal verification flow. Verify the **Perform register duplication** option is turned on (Figure 16–5).

To learn more about register duplication, refer to the *Physical Synthesis for Registers-Register Duplication* section in the *Netlist Optimizations & Physical Synthesis* chapter in volume 2 of the *Quartus II Handbook*.

8. Perform a full compilation of the design. On the Processing menu, click **Start Compilation**, or click the **Start Compilation** icon in the Toolbar.

   If your golden netlist (VQM netlist from Synplify Pro or RTL for the Quartus II integrated synthesis) includes any of the following design entities not having a corresponding formal verification model, the entity is handled as a black box whose boundary interface is preserved. There are three types of black boxes and required user actions depending upon each circumstance. Table 16–3 describes these three types of black boxes and the required user actions in detail.

Table 16–3. Black Boxes & Required User Action

Type of Black Box	Required User Action
Altera library of parameterized modules (LPMs) and megafunctions (refer to Table 16–6 for a complete list).	No action required. The Quartus II software automatically black boxes the list of components and preserves the hierarchy.
Any parametrized entity other than those listed in the Table 16–6.	User must black box the wrapper that instantiates the parametrized entity.
Non parametrized entities which the user wants to black box.	User can black box the entity itself.

You can also set the black-box property on the entities that the formal verification tool does not compare by using Tcl commands or the GUI.

Tcl Command

Use the following Tcl commands to preserve the boundary interface of a black box entity: `dram`.

```
set_instance_assignment -name\ PRESERVE_HIERARCHICAL_BOUNDARY FIRM -to | -entity dram

set_instance_assignment -name EDA_FV_HIERARCHY\ BLACKBOX -to | -entity dram
```

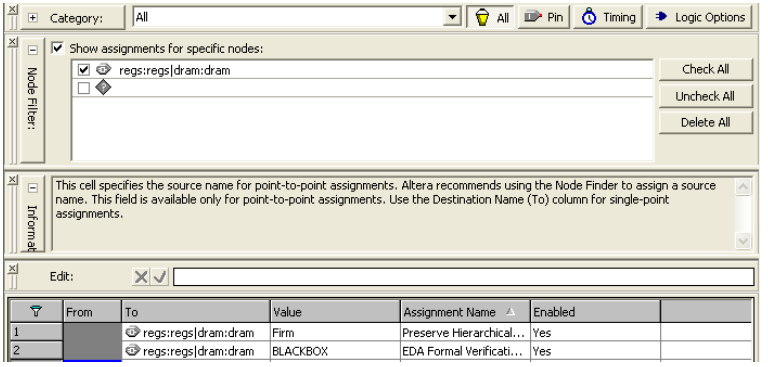
GUI

To preserve the boundary interface of an entity using the GUI, follow these steps:

1. Make an EDA Formal Verification Hierarchy assignment to the entity with the value `BLACKBOX`.

2. Make a Preserve Hierarchical Boundary assignment to the entity with the value `Firm` (Figure 16–6).

Figure 16–6. Setting the Black-Box Property on a Module



The Quartus II Software Compiler-Generated Files & Directories

After successful compilation, the Quartus II software generates a list of files and directories in the <*project_directory*>**fv/conformal/** directory (Table 16–4).

Table 16–4. The Quartus II Software Compiler-Generated Files & Directories (Part 1 of 2)

File or Directory	Name	Details
Verilog Output File	<*proj rev*>**.vo**	The Quartus II software-generated netlist for formal verification.
Script file	<*proj rev*>**.ctc**	The <*proj rev*>**.ctc** file references <*proj rev*>**.clg** and <*proj rev*>**.clr** that read the library files and black-box descriptions. The <*proj rev*>**.ctc** file also references the <*proj rev*>**.cmc** file containing information about the mapped points. *(1)*
	<*proj rev*>**.cmc**	The <*proj rev*>**.cmc** file contains information about the additional points to be mapped in addition to the points selected by the tool.
	<*proj rev*>_trivial**.cmc**	This <*proj rev*>`_trivial`**.cmc** file contains mapping information for all the key points in the design. *(2)*
	<*proj rev*>**.clr**	The <*proj rev*>**.clr** file contains information about the macros and libraries for the revised design.
	<*proj rev*>**.clg**	The <*proj rev*>**.clg** file contains information about the macros and libraries for the golden design.

Table 16–4. The Quartus II Software Compiler-Generated Files & Directories (Part 2 of 2)

File or Directory	Name	Details
blackboxes directory	*<project directory>***/fv/conformal/blackboxes**	This directory contains top-level module descriptions for all the user-defined black-box entities and contains modules with definitions other than Verilog or VHDL, for example, Block Design File (.bdf) in the design directory *<project directory>***/fv/conformal/blackboxes**

Note to Table 16–4:

(1) This file is used with the Encounter Conformal software.

(2) In some cases Encounter Conformal software performs incorrect key point mapping, resulting in formal verification mismatches. To overcome the verification mismatches, Quartus II software writes out <*proj rev*>_trivial**.cmc** file that contains mapping information for all the key points in the design, reading this file during the formal verification setup can result in increased run time. Therefore, the Quartus II software writes out the top-level script file <*proj rev*>**.ctc** with the command to read the <proj rev>_trivial**.cmc** file commented. If the formal verifications results are not acceptable, then the user can uncomment the command and read the <*proj rev*>_trivial**.cmc** file. The command in the <proj rev>**.ctc** file is:

//Trivial mappings with same name registers
//read mapped points SPROJECT/fv/conformal/<proj rev>_trivial.cmc

The script file contains the setup constraints used along with the formal verification tool. The file <*entity*>**.v** in the blackboxes directory contains the module description of entities that are not defined in the formal verification library. The file also contains entities that you specify as black boxes. For example, if there is a reference to a black box for an instance of the `altdpram` megafunction in the design, the blackboxes directory does not contain a module description for the `altdpram` megafunction because it is defined in the **altdpram.v** file of the formal verification library. When a module does not have an RTL description or the description exists only in the formal verification library and you do not want to compare the module using formal verification, then a file containing only the top-level module description with port declaration is written out to the blackboxes directory and read into the Encounter Conformal software.

The Quartus II Software Scripts for Encounter Conformal

The Quartus II software generates scripts to use with the Encounter Conformal Logic Equivalence Check (LEC) software. This section elaborates the details of the Encounter Conformal commands used within the scripts to help you compare the revised netlist with the golden netlist. In most cases, you do not need to add any more Encounter Conformal constraints to verify your netlists. Also a sample script generated by the Quartus II software is provided at the end of the chapter.

The Encounter Conformal Commands within the Quartus II Software-Generated Scripts

The value for the variable `QUARTUS` is the path to the Quartus II software installation directory:

- `setenv QUARTUS <`*Quartus Installation Directory*`>`

The Quartus II software assigns the current working directory of the project to the `PROJECT` variable. Use this variable to change the project directory to the directory where the design files are installed when moving from a UNIX to a Windows environment, or the other way around.

- `setenv PROJECT <`*Quartus Project Directory*`>`

The following command reads both the golden and the revised netlists along with the appropriate library models:

- `read design <`*design files*`>`

You must update the project location when the files are moved from the Windows environment to the UNIX environment.

The post place-and-route netlist from the Quartus II software might contain net and instance names that are slightly different from those of the golden netlist. By using the following command, the Quartus II software defines temporary substitute string patterns enabling the Encounter Conformal software to automatically map key points when the names are not the same:

- `add renaming rule <`*rule*`>`

The Encounter Conformal LEC software employs three name-based methods to map key points to compare the revised netlist with the golden netlist. Scripts set the correct method to get the best results.

- `set mapping method <`*mapping_rule*`>`

The Quartus II software performs several optimizations, including optimizing the registers whose input is driven by a constant. Under these circumstances, for the formal verification software to compare the netlists properly, the command `set flatten model` is used with the option `seq_constant`.

- `set flatten model <flattening_rule>`

When you use the command `report black box`, verify that the following modules are listed as black boxes, along with any of the modules black boxed by the user, in both the golden and revised netlists:

- LPMs and megafunctions without the formal verification models
- Encrypted IP functions
- Entities not implemented in Verilog HDL or VHDL

Use the following command to set the same implementation on multipliers for both the golden and revised netlists:

- `set multiplier implementation <implementation_name>`

If there are any combinational loops or instances of `LPM_LATCH`, the Quartus II software cuts the loop at the same point using the following command on both the golden and revised netlists:

- `add cut point`

The Encounter Conformal software does not always automatically map all the keypoints or can incorrectly map some keypoints. To help the Encounter Conformal software successfully complete the mapping process, the Quartus II software records optimizations performed on the netlist as a series of `add mapped points` in the Encounter Conformal *<file_name>*.**cmc** script.

- `add mapped points <key_points>`

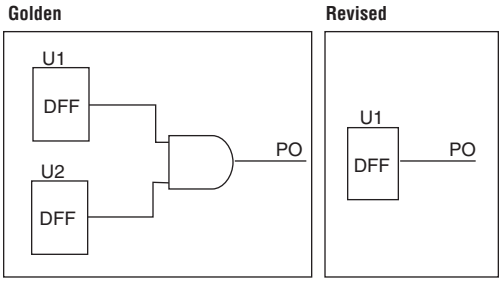
There are situations where the inverter in front of the resistor gets moved after the resistor. In this situation, the following command is used:

- `add mapped points <key_points> -invert`

The following command reads in the mapped point information from the specified file:

- `read mapped points <file_name>.cmc`

Figure 16–7. Instance Equivalence



During the process of optimization, the Quartus II software might merge two registers into one (Figure 16–7). The Quartus II software informs the formal verification tool that the U1 and U2 registers are equivalent to each other using the following command:

- `add instance equivalence` <*instance_pathname ..*> `[-Golden]`

If the register duplication takes place, the following command is used:

- `add instance equivalence` <*instance_pathname ..*> `[-revised]`

The following command is used when the inverter is moved beyond the register along with either register duplication or merging:

- `add instance equivalences` <*instance_pathname*> `[-invert` <*instance_pathname*>`]`

  At times the register output is driven to a constant, either `logic 0` or `logic 1`. The Quartus II software sets the value of the register to a constraint using the `add instance constraint` command. For more information on this command, refer to "Stuck-at Registers" on page 16–6.

- `add instance constraint` <*constraint_value*>

Comparing Designs Using Encounter Conformal

This section discusses using the Encounter Conformal software to compare designs.

Black Boxes in the Encounter Conformal Flow

The Quartus II software compiles the design on a flattened netlist. However, there are some modules in the design that must be treated differently. The following is a list of some of these modules:

- LPMs and megafunctions without formal verification models
- Encrypted IP functions
- Entities not implemented in Verilog HDL or VHDL

To perform equivalence checking between the design consisting of the modules listed above and its revised version, the modules have to be treated as black boxes by the Encounter Conformal software. In order to facilitate the formal verification flow, the Quartus II software reconstructs the hierarchy on the black boxes with a port interface that is identical to the module on the golden side of the design.

Verilog Output netlist files written by the Quartus II software also contain the black-box hierarchy when you make the following assignments for a module:

- An EDA Formal Verification Hierarchy assignment with the value `BLACKBOX`
- A Preserve Hierarchical Boundary assignment with the value `Firm` (Figure 16–6)

If the two assignments listed above are not made for a module, the Quartus II software implements the intended black box module with logic cells. When this happens, the Verilog Output netlist file no longer contains the black-box hierarchy and does not preserve the port interface, resulting in a mismatch within the Encounter Conformal software.

Running the Encounter Conformal Software

To run the Encounter Conformal software, use the GUI or a system command prompt, and use the CTC script generated by the Quartus II software.

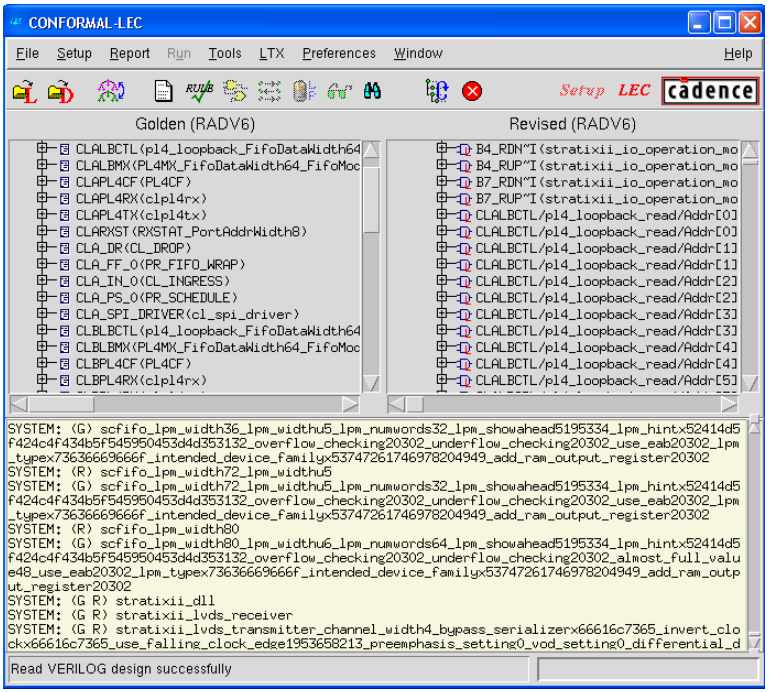
Running the Encounter Conformal Software from the GUI

To run the Encounter Conformal software from the GUI, follow these steps:

1. Open the Encounter Conformal software.
2. On the File menu, click **Do Dofile**.
3. Select the file **<***path to project directory***>/fv/conformal**<*design*>**.ctc**.

The Encounter Conformal software GUI displays the functional comparison netlist results (Figure 16–8). The Golden window displays the original RTL description of the netlist or the post synthesis VQM netlist from Synplify Pro, and the Revised window displays the pos-fit VQ netlist. The message section at the bottom of the window reports the verification results and the number of unmapped and non-equivalent points found in the design.

Figure 16–8. Encounter Conformal Software GUI Display of Functional Comparisons



To investigate the verification results, click the **Mapping Manager** icon in the toolbar, or on the Tools menu, click **Mapping Manager**. The Encounter Conformal software reports the mapped, unmapped, and compared points in the Mapped Points, Unmapped Points, and Compared Points windows, respectively.

For more information on how to diagnose non-equivalent points, refer to the Encounter Conformal software user documentation.

Running the Encounter Conformal Software From a System Command Prompt

To run the Encounter Conformal Software without using the GUI, type the following command at a system command prompt:

```
lec -dofile /<path to project directory>/fv/conformal/<design_name>.ctc -nogui ↵
```

Debugging Tips

Table 16–5 lists debugging tips to overcome Encounter Conformal errors and mismatches.

Table 16–5. Debugging Tips for Encounter Conformal Errors & Mismatches (Part 1 of 3)

Problem	Error	Cause & Solution
While running the Conformal LEC tool, the Read Design command errors out.	Cannot open file <*project_dir*>/pci_master.v	Filenames are case insensitive on the Windows platform, and case sensitive on Unix. If synthesis is run on Windows and the formal verification database is copied to UNIX, make sure the filename in the formal verification script matches the file name in the database.
Encounter Conformal reports pathname not found.	Instance pathname <*design_hierarchy*>/denormal "is not found in Golden/Revised" while reading setup scripts generated by the Quartus II software.	The Quartus II software-generated script contains the net name instead of the instance name. Change the net name to the instance name.
Formal verification using Encounter Conformal reports an undefined design entity in the design.	<*file_name*>:<*line#*> Design unit 'LPM_MULT' is referenced but not defined.	The `lpm_mult` megafunction entity name in design files is in uppercase. Since the formal verification library models for all mega functions are in lowercase, Encounter Conformal cannot find the upper case (LPM_MULT) model in the library. Change the megafunction name in the design file to lowercase.

Table 16–5. Debugging Tips for Encounter Conformal Errors & Mismatches (Part 2 of 3)

Problem	Error	Cause & Solution
Formal verification using Encounter Conformal reports an undefined named port connection.	HRC3.3: Undefined named port connection	Encounter Conformal may report this error while reading the revised netlist because the Verilog Output netlist generated by the Quartus II software contains an additional port in the instantiated black-box module that is not defined in the synthesis or the simulation module. The port is usually a control signal that controls both register and combinational logic inside the black box hierarchy. Add the following command during the setup mode of the design to instruct the Conformal software to ignore the error caused by the additional port: `set rule handling HRC3.3 -warning` *(1)*

Ports are missing from the black box definition in the revised netlist.	Formal verification mismatches	If the output port of a black box is driven by an input port without any logic between the ports, or the logic that existed between the ports is optimized away by the Quartus II software, then the Quartus II software strips off the ports from the black box and replaces the ports with a wire outside of the black box. Black boxes containing logic reduced to a wire in revised netlist results in formal verification mismatches. You must manually verify these mismatches and make sure that functionally there is no difference between the golden and revised netlists.
		For example a black box defined as:
		`module black_box (in,out);`
		`input in;`
		`output out;`
		`endmodule`
		And the actual implementation represented by:
		`module black_box (in,out);`
		`input in;`
		`output out;`
		`assign out = in;`
		`endmodule`
		For these types of black boxes, the Quartus II software replaces the black box with a wire because there is no logic between the port's out and in.

Table 16–5. Debugging Tips for Encounter Conformal Errors & Mismatches (Part 3 of 3)

Problem	Error	Cause & Solution
Formal Verification reports matches on the netlists containing `_unassoc_ports_[]`	When a port on a black box entity drives two or more signals within the black box, the Quartus II software pushes the connections outside of the black box, and creates that many ports on the black box. This problem is associated with only Stratix II and Hardcopy II designs.	The additional ports on the black box are named as `_unassoc_ports_[]` (Figure 16–9). This issue is generally associated with reset and enable signals. Figure 16–9 shows an example where reset pin is split into two ports outside of the black box and the `_unassoc_ports_` is driven by the `clkctrl` block. In such situations, the Verilog Output netlist generated by the Quartus II software has signals driving these black box ports, but golden RTL doesn't contain any signals to drive the `_unassoc_ports_[]` resulting in formal verification mismatch of the black box. The black box module definition generated by the Quartus II software in the directory <*Quartus_project*>**\fv\conformal*_blackboxes** contains these additional `_unassoc_ports_` ports. This black box module is read on both Golden and revised sides of the design, which results in unconnected ports on the golden side and results in formal verification mismatches. Another common occurrence of this issue is in HardCopy II designs. Whenever a port drives large fanout within the black box, the Quartus II software inserts a buffer on the net and moves the logic outside of the black box (Figure 16–10).

Note to Table 16–5:

(1) For a list of formal verification solutions, refer to the formal verification solutions page on the Altera website: **http://answers.altera.com/altera/index.jsp?/Topics/Software/ Verification/Formal%20Verification**

Figure 16–9 shows the creation of `_unassoc_ports_[]` for the reset signal.

Figure 16–9. Creation of _unassoc_ports_[] for the Reset Signal

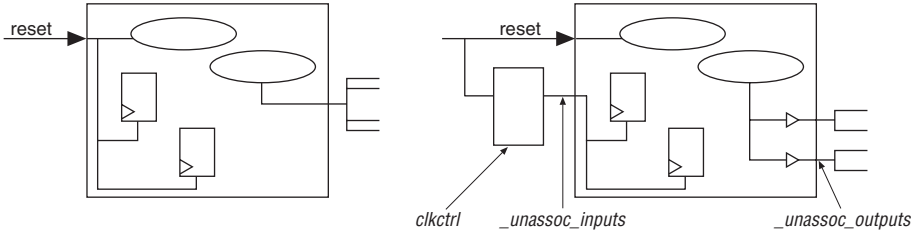
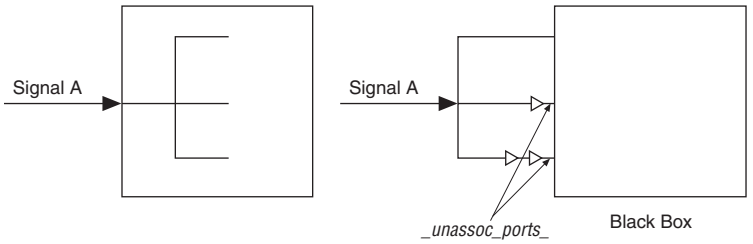


Figure 16–9 shows the creation of `_unassoc_ports_[]` for a signal with large fanout.

Figure 16–10. Creation of _unassoc_ports_[] for a Signal with Large Fanout



Known Issues & Limitations

The following known issues and limitations can occur when using the formal verification flow described in this chapter:

- Unused logic optimized within and around a black box by the Quartus II software can result in a black-box interface different from the interface in the synthesized VQM netlist.
- In designs with combinational feedback loops, the Encounter Conformal software can insert extra cut points in the revised netlist causing unmapped points and ultimately verification mismatches. For more information on how to handle combinational loops, refer to "Combinational Loops" on page 16–9.
- To perform formal verification, certain synthesis optimization options such as register retiming, optimization through black-box hierarchy boundaries, and disabling the ROM and shift register inference are turned off, which can have an impact on the area resource and performance.
- RAM and ROM instantiations/inferences are not verified using formal verification.
- Incremental Compilation for the purpose of formal verification does not support user created design partitions.
- Formal verification does not support clearbox netlist due to unconnected ports on its WYSIWYG instances.
- Formal verification does not support VHDL megafunction variations due to undriven ports on the megafunctions.
- When a black box contains bidirectional ports, the Quartus II software fails to reconstruct the hierarchy. For this reason, the black box is represented by a flat netlist resulting in formal verification mismatches.
- ROMs in the design have to be black boxed before compilation using QIS because the Quartus II software may perform some optimizations on the ROM, resulting in Formal Verification mismatches.

- The MegaWizard-generated megafunction variation file for altpll may not have all of the unused input ports of the altpll connected to default values because the Quartus II software errors out if some inputs are connected in certain modes. However, the Verilog Output file generated for formal verification does connect all the inputs of the altpll with default values. As a result, while running Formal Verification of a design with altpll components, there may be non-equivalent black boxes because the unused inputs are unconnected on the golden side, and driven by a default value on the revised side.
- Conformal may report mismatches or abort comparison of some key points when a DSP megafunction is implemented in LEs by the Quartus II software due to implicit optimizations within the DSP and the complexity of the multiplier logic in terms of LEs.

Conclusion

Formal verification software enables verification of the design during all stages from RTL to placement and routing. Verifying designs takes more time as designs increase in size. Formal verification is a technique that helps reduce the time needed for your design verification cycle.

Black Box Models

The black box models are interface definitions of entities such as primitives, atoms, LPMs, and megafunctions. These models have a parameterized interface, and do not contain any definition of behavior. They are specifically designed and tested to work with the Encounter Conformal software which uses these models along with your design to generate black-boxes for instances of the entity with varying sets of parameters in the design. Table 16–6 describes the supported black box models.

Table 16–6. Supported Black Box Models

Entity Type	Entity Names
Megafunctions	alt3pram, altaccumulate, altfp_mult, altgxb, altsqrt, dcfifo, scfifo, altsyncram, altsqrt
LPMs	lpm_add_sub lpm_divide

Tcl Sample Script

The following script is an example of setup commands generated by the Quartus II software:

```
reset
set system mode setup
set log file risc8.fv.log -replace
set naming rule "%s" -register -golden
set naming rule "%s" -register -revised
set naming rule "%L.%s" "%L[%d].%s" "%s" -instance
// set undefined cell black_box -both
// These are the directives that are not supported by the QIS RTL to gates FV flow
set directive off verplex ambit
set directive off assertion_library black_box clock_hold compile_off compile_on
set directive off dc_script_begin dc_script_end divider enum infer_latch
set directive off mem_rowselect multi_port multiplier operand state_vector template
setenv QUARTUS c:/altera/quartus51
setenv PROJECT <project location>
read design \
    $QUARTUS/eda/fv_lib/vhdl/dummy.vhd \
    -map lpm $QUARTUS/eda/fv_lib/vhdl/lpms \
    -map altera_mf $QUARTUS/eda/fv_lib/vhdl/mfs \
    -map stratix $QUARTUS/eda/fv_lib/vhdl/stratix \
    -vhdl -noelaborate -golden
read design \
    -file $PROJECT/fv/conformal/<proj rev>.clg \
    $PROJECT/<design_name>.vqm \
    -verilog2k -merge none -golden
read design \
    $QUARTUS/eda/fv_lib/vhdl/dummy.vhd \
    -map lpm $QUARTUS/eda/fv_lib/vhdl/lpms \
    -map altera_mf $QUARTUS/eda/fv_lib/vhdl/mfs \
    -map stratix $QUARTUS/eda/fv_lib/vhdl/stratix \
    -vhdl -noelaborate -revised
read design \
    -file $PROJECT/fv/conformal/<proj rev>.clr \
    $PROJECT/fv/conformal/<proj rev>.vo \
    -verilog2k -merge none -revised
add renaming rule r1 "~I\/" "\/" -revised
set multiplier implementation rca -golden
set multiplier implementation rca -revised
set mapping method -name first
set mapping method -unreach
set mapping method -nobbox_name_match
set flatten model -seq_constant
set flatten model -nodff_to_dlat_zero
set flatten model -nodff_to_dlat_feedback
set root module risc8 -golden
set root module risc8 -revised
report messages
report black box
report design data
// report floating signals
add black box altsyncram -module -golden
add black box altsyncram -module -revised
set system mode lec -nomap
read mapped points $PROJECT/fv/conformal/risc8.cmc
map key points
remodel -seq_constant -repeat
add compare points -all
compare
usage
```

17. Synopsys Formality Support

QII53015-6.0.0

Introduction

Formal verification of FPGA designs is gaining momentum as multi-million System-on-a-Chip (SoC) designs are targeted at FPGAs. Use the Formality software to easily verify logic equivalency between the RTL and DC FPGA post-synthesis netlist, and between the DC FPGA post-synthesis netlist and Quartus II post-place-and-route netlist. Beginning with version 4.2, the Quartus® II software interfaces with EDA tools including the Formality and DC FPGA software from Synopsys.

This chapter discusses the following:

- Formal verification
- Formal verification support
- Generating the post-synthesis Verilog file
- Generating the post-place-and-route Verilog HDL (**.vo**) and Formality script
- Known issues and limitations
- Design comparison using the Formality software

Formal Verification

Formal verification uses exhaustive mathematical techniques to verify design functionality. There are two types of formal verification: equivalence checking and model checking. This section discusses equivalence checking.

Equivalence Checking

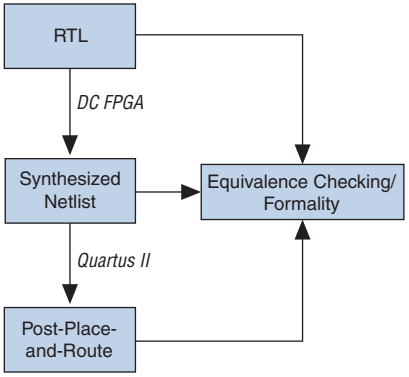
Equivalence checking compares the logical equivalence between the original design and the modified or revised design using mathematical techniques. This method reduces the verification time several-fold compared to the traditional method of performing verification using test vectors. Using a formal verification methodology provides the following key advantages:

- Faster time-to-market
- No test benches or test vectors
- Results in hours compared to days using traditional verification methods

Formal Verification Support

The Quartus II software supports formal verification using the Formality software for the DC FPGA Synthesis tool as shown in Figure 17–1.

Figure 17–1. Equivalence Checking in the FPGA Design Flow



EDA Tools & Device Support

The formal verification flow using the Quartus II software and Synopsys Formality software requires the following software versions:

- Quartus II software, beginning with version 4.2
- Synopsys DC FPGA software, beginning with version W2005.03_EA1
- Synopsys Formality software, beginning with version 2004.12

The formal verification flow, using the Quartus II and Synopsys Formality software, supports Solaris and Linux platforms, and supports Stratix series devices.

Formal Verification Between RTL & Post-Synthesis Netlist

The first step in the FPGA design flow is to synthesize the RTL code using the DC FPGA to generate the synthesized verilog netlist. Equivalence checking using formal verification is performed between the RTL and the synthesized netlist to make sure the synthesis tool has not altered the original functionality of the design.

For more information on how to use the DC FPGA software for synthesizing Altera device designs, refer to the *Synopsys Design Compiler FPGA Support* chapter in volume 1 of the *Quartus II Handbook*.

Generating Post-Synthesis Netlist for Formal Verification

During the synthesis process, the DC FPGA synthesis tool performs operations such as:

- Modifying the net/instance names
- Register duplication
- State machine extraction by different methods

Changes caused by these synthesis operations cause comparison point matching issues and false verification failures. In order to make sure that the Formality software is aware of the design transformations performed during the synthesis, the DC FPGA software writes out a Synopsys setup verification file (**.svf**) to be read into the Formality software. To ensure the SVF constraint file contains all the formal verification setup constraints, you need to set certain commands in the DC FPGA software before compiling the design as detailed in the following section.

DC FPGA Software Settings

The Formality software does not support the **register merging** or **register retiming** synthesis operations, which are off by default, but it is necessary to verify that these settings are turned off during synthesis. Some of the commands necessary to turn off these options and generate a valid Verilog netlist for the formal verification purpose are described in this section.

For more information on creating the Tcl script file to perform synthesis, refer to the *DC FPGA User Guide* or the *Synopsys Design Compiler FPGA Support* chapter in volume 1 of the *Quartus II Handbook*.

To set most of the required synthesis settings to generate a valid formal verification netlist, use the following command:

```
set_fpga_defaults -formality <architecture_name>
```

For example:

```
set_fpga_defaults -formality altera_stratix
```

To view all of the settings performed by this command, add `-verbose` to this command. In addition, you will need to execute the additional commands shown in Table 17–1.

Table 17–1. Commands & Affect of Each Command

Command	Affect
`set verilogout_write_constant_nets true`	Add this command at the beginning of the script to allow unconnected nets to be driven by either power or ground.
`change_names -rule verilog -hierarchy`	This command must be added after the compile command to set the Verilog naming rule to the output netlist for all levels of hierarchy.
`set_verification_friendly_mode -filename \ <top_level>.svf -append -allow_override`	This command helps DC_FPGA to write out a SVF constraint file to be read into the Formality software.
`write -hier -f verilog -o $outputdir/<top_level>.v`	This command writes out a Verilog netlist for Formal Verification.

For a sample DC FPGA script that is ready for compilation, refer to "Tcl Sample Script" on page 17–13.

Post synthesis Verilog netlist for formal verification can be generated by executing the Tcl script either in `fpga_vision` (GUI) or `fpga_shell-t` (command line).

For comparing RTL against post-synthesis netlist using the Formality software, refer to the *DC FPGA Software User Guide*.

Generating the VO File & Formality Script

The following steps describe how to set up the Quartus II software environment to generate the place-and-route, post-place-and-route VO netlist file, and Formality script compatible for formal verification.

1. Create a new Quartus II project or open an existing project.
2. On the Assignments menu, click **Settings**. The **Settings** dialog box is shown.
3. In the Category list, select **Files**. The **Files** page is shown.
4. Highlight the input file by clicking on it, then click **Properties** and select **Verilog Quartus Mapping File**. Click **OK**.

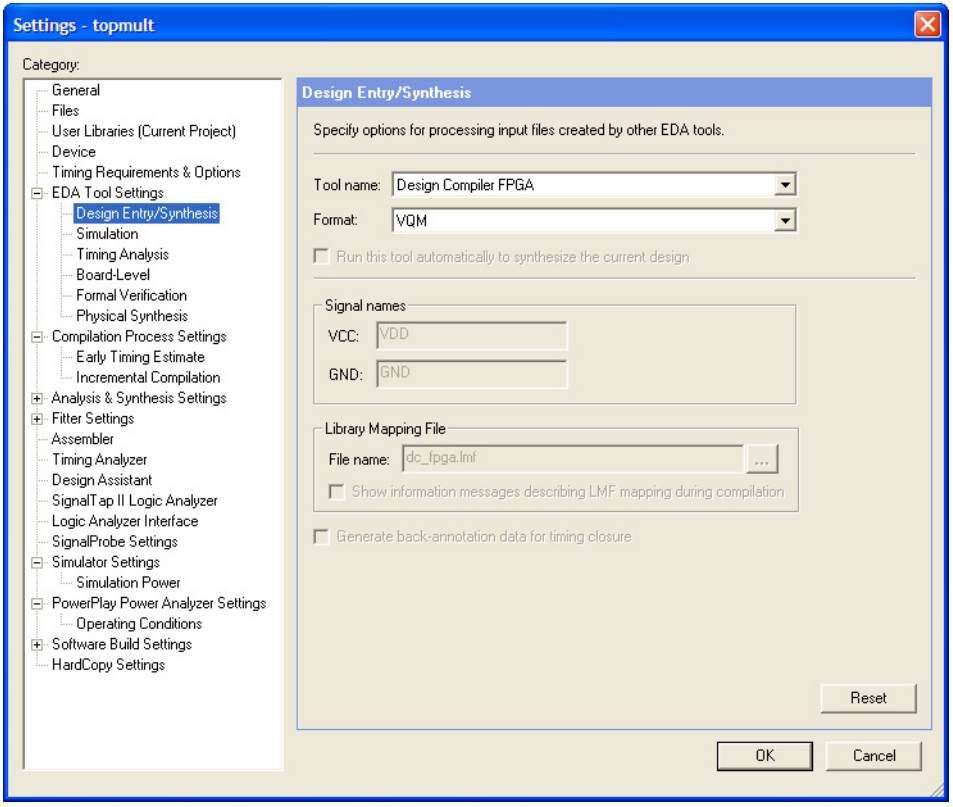
5. In the **Category** list, select **Design entry/synthesis** under **EDA Tool Settings**.

6. In the **Tool name** list, select **Design Compiler FPGA** (Figure 17–2).

These settings can also be performed using the following Tcl commands:

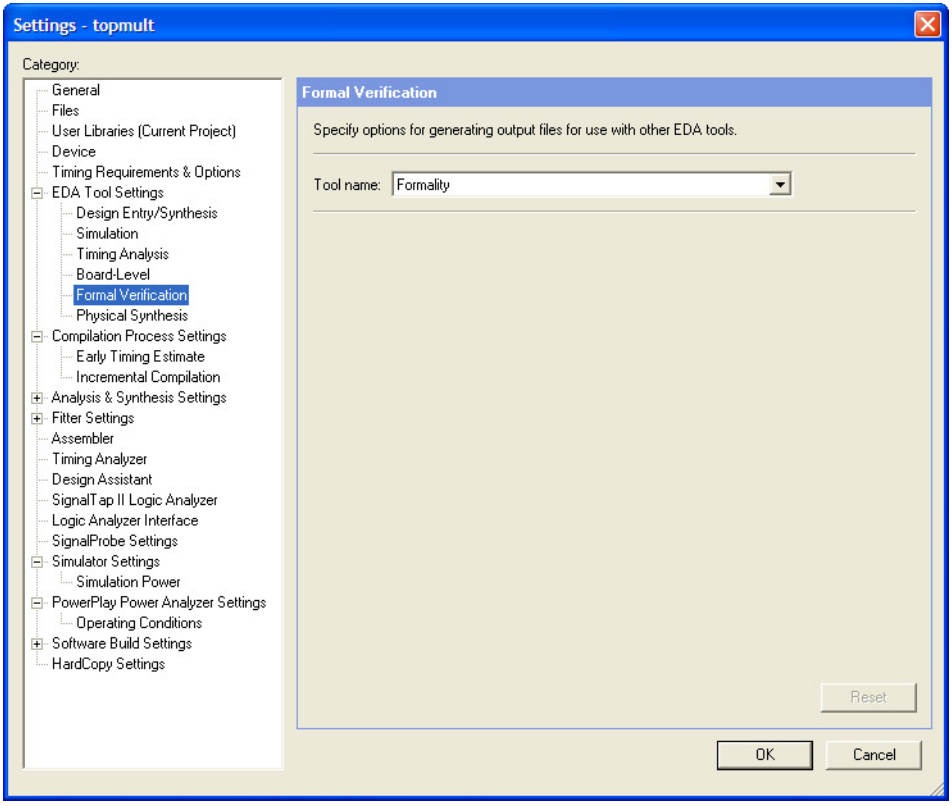
```
set_global_assignment -name VQM_FILE
<verilog_file_from_dc_fpga>

set_global_assignment -name \
EDA_DESIGN_ENTRY_SYNTHESIS_TOOL "Design Compiler FPGA"

set_global_assignment -name EDA_LMF_FILE \
dc_fpga.lmf -section_id eda_design_synthesis
```

Figure 17–2. EDA Tools Selection



7. In the **Category** list, select **Formal verification**. In the **Tool name** list, select **Formality** (Figure 17–3).

Figure 17–3. EDA Tools Selection



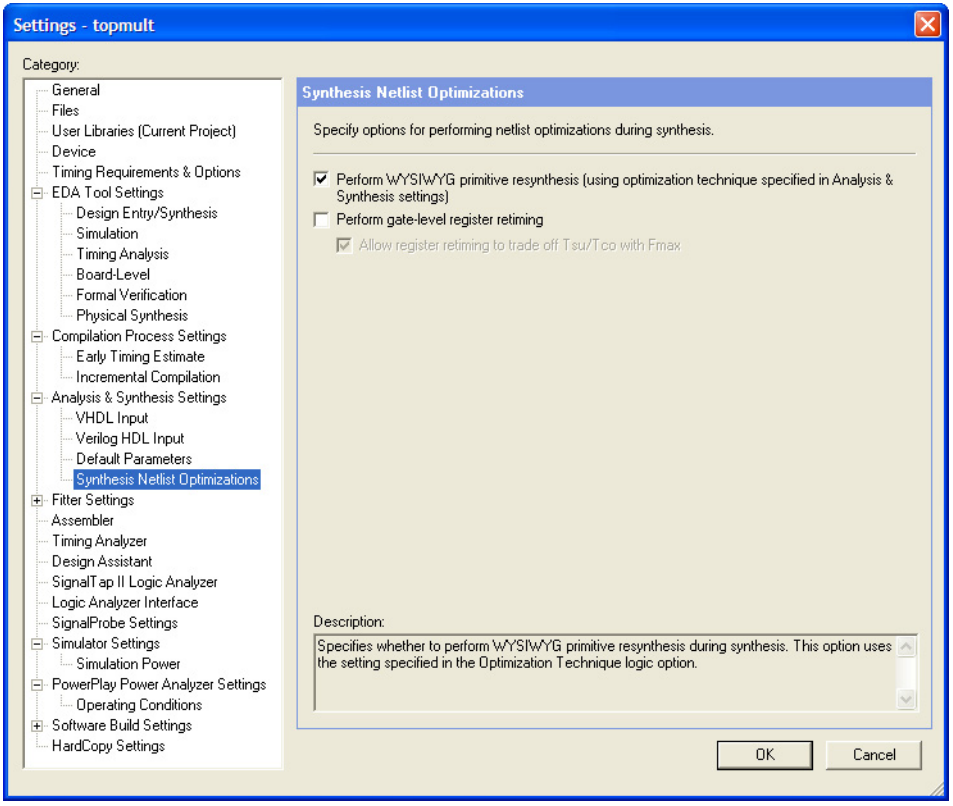
8. Click **OK**.

9. From the Assignments menu, click **Settings**. The **Settings** dialog box is shown.

10. In the **Category** list, click the **+** icon to expand **Analysis & Synthesis Settings** and select **Synthesis Netlist Optimizations**. The **Synthesis Netlist Optimizations** page is shown.

11. Turn off the **Perform gate-level register retiming** option (Figure 17–4).

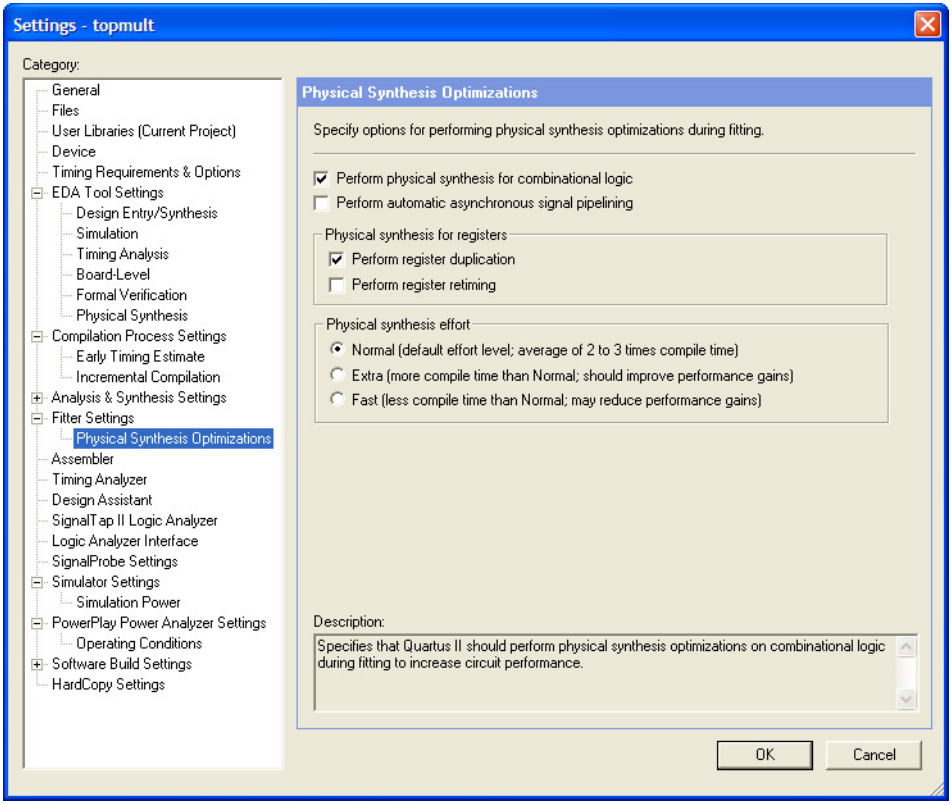
Figure 17–4. Synthesis Netlist Optimizations



12. In the Category list, click the + icon to expand **Fitter Settings** and select **Physical Synthesis Optimizations**. The **Physical Synthesis Optimizations** page is shown.

13. Turn off the **Perform register retiming** option (Figure 17–5).

Figure 17–5. Setting Parameters for Netlist Optimizations



Performing register retiming on a design usually results in moving and merging/duplicating registers along the critical path. Because equivalence checkers compare the cones of logic terminating at registers, you should not move or duplicate the registers during optimization by the Quartus II software. If the options in this section are not selected, the Formality software script could be presented with a different set of compare points, and the resulting netlist is difficult to compare against the reference netlist file.

The Quartus II software, beginning with version 4.2, supports register duplication to improve the timing by duplicating the logic.

To learn more about register duplication, refer to the *Timing Closure Floorplan* chapter in volume 2 of the *Quartus II Handbook*.

14. Perform a full compilation of the design either on the Processing menu by clicking **Start Compilation** or by clicking on the start compilation arrow icon located in the tool bar.

Handling Black Boxes

Every design entity in the golden netlist must have a corresponding formal verification model in order to successfully run formal verification. Design entities in the golden netlist without a corresponding formal verification model are handled as black boxes whose boundary interfaces must be preserved. These design entities appear in the netlist if one of the following situations apply:

- Altera megafunctions including library of parameterized modules (LPM's)

  The black-box property is only applied to LPM modules that do not have a formal verification model.

- Encrypted intellectual property (IP) cores
- Entities that are defined in the design format other than Verilog HDL or VHDL

The Quartus II software has the capability of automatically identifying the black boxes and sets the property Preserve Hierarchical Boundary to Firm to preserve the boundary interfaces of the black boxes which helps the formal verification.

You can also specify the black box property on entities that should be compared by the Formality software. To do this make the following assignments either using Tcl commands or GUI for the entities in question:

Tcl Command

The following two commands preserves the boundary interface of the entity: dram.

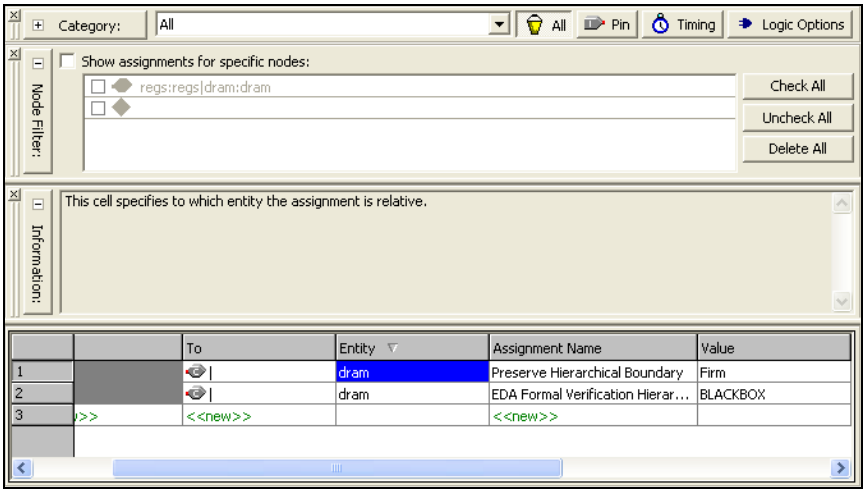
```
set_instance_assignment -name\
PRESERVE_HIERARCHICAL_BOUNDARY FIRM -to | -entity dram
set_instance_assignment -name EDA_FV_HIERARCHY\
BLACKBOX -to | -entity dram
```

GUI

Preserving the boundary interface of an entity using GUI.

- Assign the EDA Formal Verification Hierarchy value as blackbox.
- Assign the Preserve Hierarchical Boundary assignment with a value of Firm to the entity (Figure 17–6).

Figure 17–6. Making a Black Box Assignment to an Entity



The Quartus II software compiler generates the following files and directories:

- VO file: <*design_name*>**.vo.**
- Script file: <*design_name*>**.fms** used with Formality software.
- A black-box directory: black boxes that contains all the user defined black-box entities in the design which is located in the following directory: **/**<*project directory*>**/fv/formality/blackboxes**.

The script file contains the setup constraints used along with the Formality software. The <*entity*>**.v** file in the black-boxes directory contains the module description of only those entities that are not defined in the formal verification library.

For a sample script containing the setup commands generated by the Quartus II software, refer to "Tcl Sample Script" on page 17–13.

Quartus II Scripts for Formality

The Quartus II software generates scripts to use with the Formality software. This section describes the Formality software commands used within the scripts to help customers comparing the implementation and reference netlists. Table 17–2 describes the Formality software commands within Quartus II generated scripts.

Table 17–2. Formality Software Commands within Quartus II Generated Scripts

Command	Affect
`read_verilog` <*design files*>	This command reads both the reference and implementation netlists in addition to the appropriate library models.
`set_compare_rule` <*rule*>	Adds a name matching rule that Formality software applies to a design before creating compare points.
`set signature_analysis_matching` <*value*>	Use this command to specify whether or not to use signature analysis to match previously compared points.
`set_constant` <*value*>	This command allows you to set the logic state of a design object to either 0 or 1.
`set hdlin_altera_generate_naming` <*value*>	This command directs Formality software to apply alter naming conventions for registers.
`Set_user_match` <*mapping_point_name*>	Use this command to create pairs of matched points to compare those that Formality software could not match during its matching process.

Comparing Designs Using the Formality Software

To verify the functional equivalence between post-synthesis and post-place-and-route netlists, use the script file <*file_name*>**.fms** since it contains references to the macros defined in the Altera formal verification library. Some of the macros used are:

- _ALTERA_FAMILY_IS_STRATIX_
- POST_FIT
- FORMALITY
- GATES_TO_GATES

An example on the use of these macros is shown in the **read_verilog** command in the previous section. This script file <*file_name*>**.fms** is executed from either the GUI or using the following command:

```
%formality -file <file_name>.fms
```

For more information about using the Formality software, refer to the *Formality User Guide.*

The Formality software does not support inferred RAMs in RTL while performing RTL-to-Gates verification. Therefore, you should apply the black box property to RAM that is instantiated by the RTL code.

Known Issues & Limitations

This section discusses known issues and limitations of the formal verification flow using the DC FPGA, Quartus II, and Formality software:

1. Formal verification of post synthesis verses post-place-and-route netlist does not support latches because latches are implemented using combinational logic with a feedback loop which poses a problem to the Formality software.

2. If an LPM or an Altera megafunction module is inferred and all the ports of the module are not used, then unused ports should be connected to default values in the post-synthesis Verilog HDL netlist.

3. The Quartus II software may optimize away logic feeding a black box, resulting in mismatches on the blackbox inputs. For example, if certain bits of a RAM output are not being used, then the Quartus II software optimizes away the logic feeding the corresponding data inputs.

Conclusion

Formal verification enables verification of the design during all stages from RTL to place-and-route. As designs become larger, design verification using traditional methods becomes too time consuming. Thus, formal verification easily verifies that any modifications to the netlist in the physical domain have not altered from the Golden netlist. Advanced debugging capabilities within Formality software pinpoints the source of the differences between the Reference and Implementation netlists, enabling the user to easily fix the differences.

Related Links

Altera web site: *Using the Quartus II Software with DC FPGA*
www.altera.com/support/software/nativelink/quartus2/eda_view_using_eda.htm.

Tcl Sample Script

This section provides an example of the DC FPGA software script to perform synthesis and an example formal verification script generated by the Quartus II software.

DC FPGA Synthesis Script

The following example script presents the Altera recommended settings in the DC FPGA software for synthesizing the design for the Stratix architecture. The script also generates the Verilog netlist file for formal verification using the Formality software. These tasks are performed in the following five sections of the script:

- Setting up the library
- Default synthesis settings for Altera Stratix
- Analyzing the design files
- Compiling the design
- Generating the Verilog netlist for formal verification

```
# Setup file for Altera Stratix Devices
# Tcl style setup file but will work for
# original DC shell as well
# Need to define the root location of the
# libraries by changing
# the variable $dcfpga_lib_path
set dcfpga_lib_path "<dcfpga_rootdir>\
/libraries/fpga/altera"
set search_path ". $dcfpga_lib_path
$dcfpga_lib_path/STRATIX $search_path"
set target_library "stratix.db"
set synthetic_library "tmg.sldb altera_mf.sldb\
lpm.sldb"
set link_library "* stratix.db tmg.sldb\
altera_mf.sldb\ lpm.sldb"
set cache_dir_chmod_octal "1777"
set hdlin_enable_vpp "true"
set post_compile_cost_check "false"
set_fpga_defaults -formality altera_stratix
set formality_altera_debug true
set_verification_friendly_mode -filename
<top_level>.svf -append \
-allow_override
set verilogout_no_tri true
set verilogout_write_constant_nets true
set compile_fix_multiple_port_nets true
## Setup design directory for database, temporary files
# and netlist
#</OUTPUTDIR>#
set outputdir <directory_name>
file mkdir $outputdir/WORK
define_design_lib WORK -path $outputdir/WORK
```

```
## Setup the Top-level design name
set top <top_level_module>
##Setup synthesis optimization options
set dcfsm_force_encoding neutral
#<READFILES>#
##Analyze source files
##Elaborate design
elaborate $top
#</ELABORATE>#
##Specify Target device
current_design $top
set_fpga_target_device AUTOFASTEST
## Insert pad during synthesis
set_port_is_pad [get_ports "*"]
#<FPGACONST>#
## Specify clock constraints
#</FPGACONST>#
#<COMPILE>#
##Setup compile options
ungroup -small 500
## Compile design
compile
change_names -rule verilog -hierarchy
#<REPORT>#
##Generate netlist/reports/constraints for PAR
write -hier -f verilog -o $outputdir/$top.v
report_fpga > $outputdir/fpga.rpt
```

Quartus II Software-Generated Formal Verification Script

The following example script shows the sample setup commands generated by Quartus II software:

```
read_verilog -i -vcs \
"+define+_ALTERA_FAMILY_IS_STRATIX_ \
+define+POST_FIT \
+define+FORMALITY -y $QUARTUS/eda/fv_lib/verilog \
+libext+.v -y \
/home/formality/testcases/mult/quartus/fv/ \
formality/blackboxes" \
$PROJECT/fv/formality/mult_ram.vo
set_top mult_ram
set_black_box i:/WORK/altsyncram
report_black_box
set_compare_rule i:/WORK/mult_ram -from "_aI$" -to ""
set_compare_rule r:/WORK/mult_ram -from "\/" -to "_a"
set_compare_rule i:/WORK/mult_ram -from "\/" -to "_a"
match
verify
```

Quartus II Version 6.0 Handbook
Volume 4: SOPC Builder

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QII5v4-6.0

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Chapter 9. Building Memory Subsystems Using SOPC Builder

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Chapter 11. Building Systems with Multiple Clock Domains

Chapter Revision Dates

The chapters in this book, *Quartus II Handbook, Volume 4*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction to SOPC Builder
Revised: *May 2006*
Part number: *QII54001-6.0.0*

Chapter 2. Tour of the SOPC Builder User Interface
Revised: *May 2006*
Part number: *QII54002-6.0.0*

Chapter 3. Avalon Switch Fabric
Revised: *May 2006*
Part number: *QII54003-6.0.0*

Chapter 4. SOPC Builder Components
Revised: *May 2006*
Part number: *QII54004-6.0.0*

Chapter 5. Component Editor
Revised: *May 2006*
Part number: *QII54005-6.0.0*

Chapter 6. Archiving SOPC Builder Projects
Revised: *May 2006*
Part number: *QII54017-6.0.0*

Chapter 7. Board Description Editor
Revised: *May 2006*
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Revised: *May 2006*
Part number: *QII54016-6.0.0*

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Revised: *May 2006*
Part number: *QII54006-6.0.0*

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Revised: *May 2006*
Part number: *QII54007-6.0.0*

Chapter 11. Building Systems with Multiple Clock Domains
Revised: *May 2006*
Part number: *QII54008-6.0.0*

About this Handbook

This handbook provides comprehensive information about the Altera® SOPC Builder tool.

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Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
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Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
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FTP site	ftp.altera.com	ftp.altera.com

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section I. SOPC Builder Features

Section I of this volume introduces the SOPC Builder system integration tool, and describes the main features. Chapters in this section serve to answer the following questions:

- What is SOPC Builder?
- What services does SOPC Builder provide?

This section includes the following chapters:

Revision History

The following table shows the revision history for Chapters 1–8.

Chapter(s)	Date / Version	Changes Made
1	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release.
	February 2005, v1.0	Initial release.
2	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	• Updated for the Quartus II software version 5.1. • Added pipeline for high performance details. • Added endian conversion details.
	May 2005, v5.0.0	No change from previous release.
3	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	Updated for the Quartus II software version 5.1.
	August 2005, v5.0.1	• Added burst transfer management details. • Updated pipeline management details.
	May 2005, v5.0.0	No change from previous release.
	February 2005, v1.0	Initial release.

Chapter(s)	Date / Version	Changes Made
4	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	August 2005, v5.0.1	Corrected reference to figure.
	May 2005, v5.0.0	No change from previous release.
5	May 2006, v6.0.0	No change from previous release.
	December 2005, v5.1.1	• Added section “Naming Signals for Automatic Type and Interface Recognition.” • Added section “Templates for Interfaces to External Logic.” • Clarified operation of the Save command. • Updated all screenshots.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release.
6	May 2006, v6.0.0	Initial release.
7	May 2006, v6.0.0	Chapter 7 was previously chapter 6. No change to content.
	October 2005 v5.1.0	Initial release.
8	May 2006, v6.0.0	Chapter 8 was previously chapter 7. No change to content.
	October 2005 v5.1.0	Initial release.

1. Introduction to SOPC Builder

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Overview

SOPC Builder is a powerful system development tool for creating systems based on processors, peripherals, and memories. SOPC Builder enables you to define and generate a complete system-on-a-programmable-chip (SOPC) in much less time than using traditional, manual integration methods. SOPC Builder is included in the Quartus® II software and is available to all Altera® customers.

Many designers already know SOPC Builder as the tool for creating systems based on the Nios® II processor. However, SOPC Builder is more than a Nios II system builder; it is a general-purpose tool for creating arbitrary SOPC designs that may or may not contain a processor.

SOPC Builder automates the task of integrating hardware components into a larger system. Using traditional system-on-chip (SOC) design methods, you had to manually write top-level HDL files that wire together the pieces of the system. Using SOPC Builder, you specify the system components in a graphical user interface (GUI), and SOPC Builder generates the interconnect logic automatically. SOPC Builder outputs HDL files that define all components of the system, and a top-level HDL design file that connects all the components together. SOPC Builder generates both Verilog HDL and VHDL equally, and does not favor one over the other.

In addition to its role as a hardware generation tool, SOPC Builder also serves as the starting point for system simulation and embedded software creation. SOPC Builder provides features to ease writing software and to accelerate system simulation.

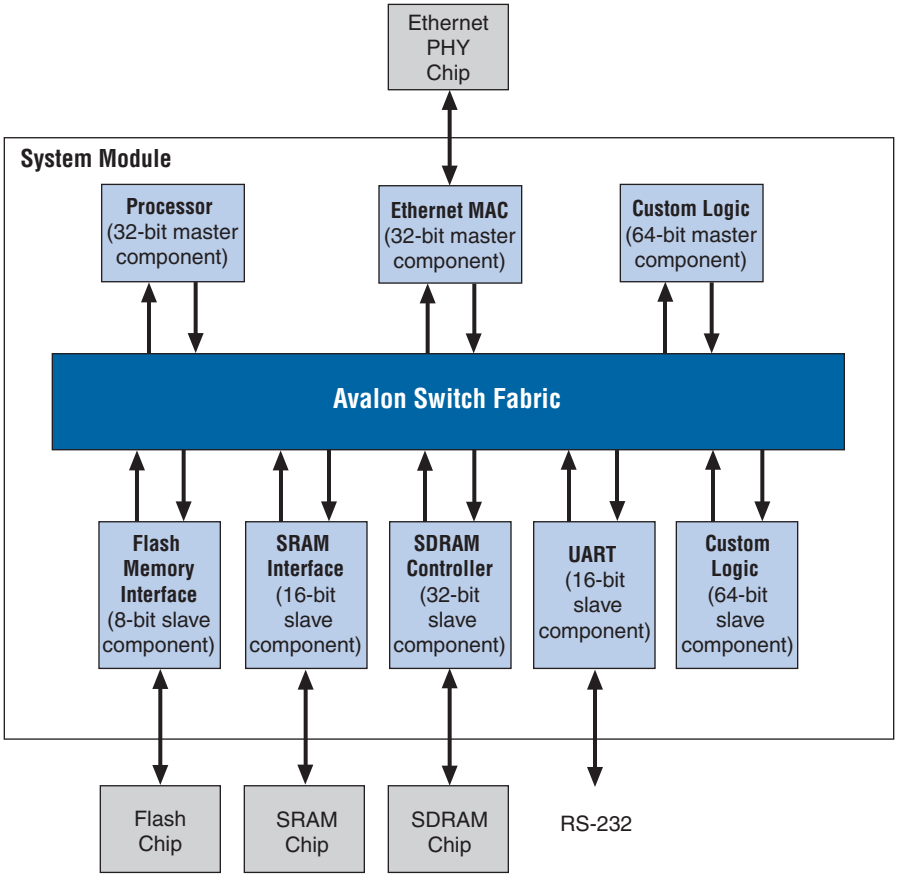
This chapter introduces you to the architectural structure of systems built with SOPC Builder, and describes the primary functions of SOPC Builder.

Architecture of SOPC Builder Systems

This section describes the fundamental architecture of an SOPC Builder system.

An SOPC Builder *component* is a design module that SOPC Builder recognizes and can automatically integrate into a system. SOPC Builder connects multiple components together to create a top-level HDL file called the *system module*. SOPC Builder generates *Avalon® switch fabric* that contains logic to manage the connectivity of all components in the system. Figure 1–1 shows an example of a multi-master system module with Avalon switch fabric connecting the multiple master and slave components.

Figure 1–1. Example of a System Module Generated by SOPC Builder



SOPC Builder Components

SOPC Builder components are the building blocks of the system module. SOPC Builder components use the Avalon interface for the physical connection of components, and you can use SOPC Builder to connect any logical device (either on-chip or off-chip) that has an Avalon interface. The Avalon interface uses an address-mapped read/write protocol that allows master components to read and/or write any slave component.

For details on the Avalon interface, see the *Avalon Interface Specification* at **www.altera.com**.

A component can be a logical device that is entirely contained within the system module, such as the processor component in Figure 1–1 on page 1–2. Alternately, a component can act as an interface to an off-chip device, such as the SRAM interface component in Figure 1–1 on page 1–2. In addition to the Avalon interface, a component can have other signals that connect to logic outside the system module. Non-Avalon signals can provide a special-purpose interface to the system module, such as the Ethernet MAC in Figure 1–1 on page 1–2.

A component can be instantiated more than once per design.

Altera and third-party developers provide ready-to-use SOPC Builder components, such as:

- Microprocessors, such as the Nios II processor
- Microcontroller peripherals
- Timers
- Serial communication interfaces, such as a UART and a serial peripheral interface (SPI)
- General purpose I/O
- Digital signal processing (DSP) functions
- Communications peripherals
- Interfaces to off-chip devices
  - Memory controllers
  - Buses and bridges
  - Application-specific standard products (ASSP)
  - Application-specific integrated circuits (ASIC)
  - Processors

SOPC Builder Ready Components

Altera awards the SOPC Builder Ready certification to intellectual property (IP) designs that have plug–and–play integration with SOPC Builder. These functions may be accompanied by software drivers, low-level routines, or other software design files.

Altera's OpenCore® and OpenCore Plus evaluation programs allow you to "test drive" an SOPC Builder component both in simulation and in hardware before you buy. You can download evaluations of Altera IP functions directly from **www.altera.com/IPMegastore**. For IP functions provided by third-party vendors, contact the vendor directly to obtain an OpenCore evaluation.

Check the Altera web site at **www.altera.com** for up–to–date information about available SOPC Builder Ready components. You can identify SOPC Builder Ready components by the logo shown in Figure 1–2.

Figure 1–2. The SOPC Builder Ready Certification Logo

User-Defined Components

SOPC Builder provides an easy method for you to develop and connect your own components. With the Avalon interface, user-defined logic need only adhere to a simple interface based on address, data, read-enable, and write-enable signals.

You use the following design flow to integrate custom logic into an SOPC Builder system:

1. Define the interface to the user-defined component.
2. If the component logic resides on-chip, write HDL files describing the component in either Verilog HDL or VHDL.
3. Use the SOPC Builder component editor wizard to specify the interface and optionally package your HDL files into an SOPC Builder component.
4. Instantiate your component in the same manner as other SOPC Builder Ready components.

Once you have created an SOPC Builder component, you can reuse the component in other SOPC Builder systems, and share the component with other design teams.

For instructions on developing a custom SOPC Builder component, see the *Developing SOPC Builder Components* chapter in Volume 4 of the *Quartus II Handbook*. For complete detail on the file structure of a component, see the *SOPC Builder Components* chapter in Volume 4 of the *Quartus II Handbook*. For details on the SOPC Builder component editor, see the *Component Editor* chapter in Volume 4 of the *Quartus II Handbook*.

Avalon Switch Fabric

The Avalon switch fabric is the glue that binds SOPC Builder-generated systems together. The Avalon switch fabric is the collection of signals and logic that connects master and slave components, including address decoding, data-path multiplexing, wait-state generation, arbitration, interrupt controller, and data-width matching. SOPC Builder generates the Avalon switch fabric automatically, so that you do not have to manually perform the tedious, error-prone task of connecting hardware modules.

The purpose of SOPC Builder is to abstract away the complexity of interconnect logic, allowing designers to focus on the details of their custom components and the high-level system architecture. Automatically generating the Avalon switch fabric is the keystone to achieving this purpose. Avalon switch fabric in the system module is like air for humans: Its existence is essential, but largely ignored. Because SOPC Builder generates Avalon switch fabric automatically, most users do not interact directly with it or the HDL that describes it.

For further details, see the *Avalon Switch Fabric* chapter in Volume 4 of the *Quartus II Handbook*.

Functions of SOPC Builder

This section describes the fundamental functions of SOPC Builder.

Defining & Generating the System Hardware

The purpose of the SOPC Builder GUI is to allow you to easily define the structure of a hardware system, and then generate the system. The GUI is designed for the tasks of adding components to a system, configuring the components, and specifying how they connect together.

After you add all components and specify all necessary system parameters, SOPC Builder is ready to generate the Avalon switch fabric and output the HDL files that describe the system. During system generation, SOPC Builder outputs the following items:

- An HDL file for the top-level system module and for each component in the system
- A Block Symbol File (**.bsf**) representation of the top-level system module for use in Quartus II Block Diagram Files (**.bdf**)
- (Optional) Software files for embedded software development, such as a memory-map header file and component drivers
- (Optional) Testbench for the system module and ModelSim® simulation project files

After you generate the system module, it can be compiled directly by the Quartus II software, or instantiated in a larger FPGA design.

For more detail on the SOPC Builder GUI for defining and generating systems, see the *Tour of the SOPC Builder User Interface* chapter in Volume 4 of the *Quartus II Handbook*.

Creating a Memory Map for Software Development

For each microprocessor in the system, SOPC Builder optionally generates a header file that defines the address of each slave component. In addition, each slave component can provide software drivers and other software functions and libraries for the processor.

The process for writing software for the system depends heavily on the nature of the processor in the system. For example, Nios II processor systems use Nios II processor-specific software development tools. These tools are separate from SOPC Builder, but they do use the output of SOPC Builder as the foundation for software development.

Creating a Simulation Model & Testbench

You can simulate your custom systems with minimal effort immediately after generating the system with SOPC Builder. During system generation, SOPC Builder optionally outputs a push-button simulation environment that eases the system simulation effort. SOPC Builder generates both a simulation model and a testbench for the entire system. The testbench includes the following functionality:

- Instantiates the system module
- Drives all clocks and resets appropriately
- Optionally instantiates simulation models for off-chip devices

Getting Started

One of the easiest ways to get started using SOPC Builder is to read the *Nios II Hardware Development Tutorial* which guides you step-by-step in building a microprocessor system, including CPU, memory, and peripherals. This tutorial and other SOPC Builder example designs are included in the Nios II Embedded Design Suite (EDS), Evaluation Edition. You can download this design suite for free from the Altera Download Center at **www.altera.com**.

2. Tour of the SOPC Builder User Interface

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This chapter provides reference on how to access the features available in the SOPC Builder graphical user interface (GUI). This chapter will familiarize you with the main features of the SOPC Builder GUI.

Due to evolution and improvement of the software, the figures in this chapter may not match exactly what you see in the software.

Starting SOPC Builder

Each SOPC Builder system is associated with one Quartus® II project. Therefore, to launch SOPC Builder, you must first open a project in the Quartus II software. With a Quartus II project open, you can launch SOPC Builder by choosing **SOPC Builder** (Tools menu) or by clicking the **SOPC Builder** toolbar button. See Figure 2–1.

Figure 2–1. SOPC Builder Toolbar Button

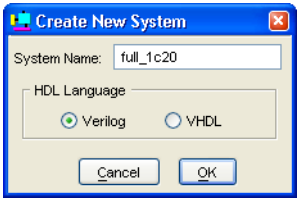
The SOPC Builder toolbar button might not appear by default. To enable it, use the **Customize** window (Tools menu).

Starting a New SOPC Builder System

If an SOPC Builder system does not exist in the current Quartus II project directory, SOPC Builder will display the **Create New System** dialog as shown in Figure 2–2 on page 2–2, and prompt you to specify the following:

- A name for the new SOPC Builder system – This serves as the name of the system module that SOPC Builder will generate.
- Target HDL – This setting determines the output language of the system module.

Figure 2–2. Create New System Dialog



Working with SOPC Builder Systems

SOPC Builder operates on exactly one system at a time, and the system must be associated with a Quartus II project. A Quartus II project may have multiple associated SOPC Builder systems, but typically will have only one (if any).

CAUTION

If you integrate multiple SOPC Builder system modules in one Quartus II project, you must make sure all components are named uniquely across all system modules. Otherwise, filename collision will occur.

In SOPC Builder, you can create a new system by choosing **New System** (File menu). You can switch to a different system by choosing **Open System** (File menu).

SOPC Builder saves files in the same directory as the Quartus II project. Each SOPC Builder system is represented by a file named **<***system module name***>.ptf**, which is a plain-text file describing the structure of the system and other system-specific details. In a purely mechanical sense, the SOPC Builder GUI is a **.ptf** file editor.

Changes you make in the SOPC Builder GUI are saved immediately to the **.ptf** file. When you open a system, SOPC Builder creates a back-up file named **<***system module name***>.ptf.bak**, in case you need to revert changes.

System Contents Tab

SOPC Builder employs a tabbed user interface. Tasks are categorized by function, and related tasks are presented on the same tab.

The **System Contents** tab is displayed when you open SOPC Builder. It is the view of SOPC Builder that you will use most often. You use the **System Contents** tab to do the following:

- Add components to a system
- Configure the components
- Specify connections between components

Figure 2–3 lists the elements of the **System Contents** tab. See Table 2–1 on page 2–4 for details.

Figure 2–3. Elements of the System Contents Tab

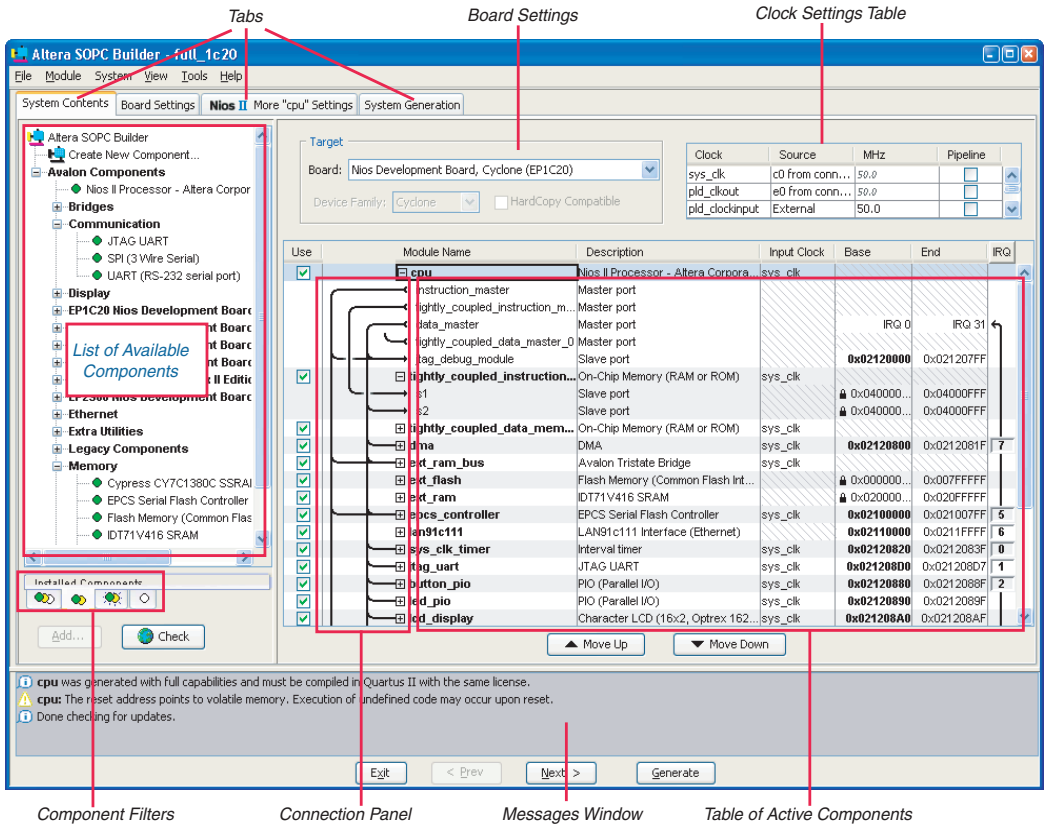


Table 2–1 describes the GUI elements shown in Figure 2–3.

Table 2–1. GUI Elements on the System Generation Tab

GUI Element	Description
Tabs	Categorizes GUI controls, based on task.
List of Available Components	Lists the library of available SOPC Builder components, organized by category. Each component appears with a colored dot next to its name. The colors of the dots have the following meanings: ● Green dot – A full, licensed version of the component is installed. ● Yellow dot – A limited, evaluation version of the component is installed. ● White dot – This component is available from Altera or a partner vendor, but is not installed.
Component Filters	Filters which type of components appear in the list of available components.
Table of Active Components *(1)*	Lists the components instantiated in the current system, and allows you to specify the following: ● Name for each component instance ● Base address for each slave port ● Clock source for each component instance ● Interrupt priority (if any) for each slave port
Connection Panel *(1)*	Represents connections between the components, and allows you to perform the following: ● Specify connections between master ports and slave ports. ● Specify arbitration shares for slave ports that are shared by multiple master ports.
Board Settings	Allows you to specify details regarding the target hardware platform: ● Board - If the target board is known and you have an SOPC Builder board description, you can specify the target board. The board setting provides SOPC Builder with information about the target hardware, such as pin-outs and connections to off-chip devices. ● Device Family - If the target board is not known, you can specify a particular device family, which affects the behavior of certain components. ● HardCopy Compatible - Certain components have limited functionality when targeting Altera HardCopy devices. This option allows you to use only components and settings that are compatible with HardCopy devices.
Clock Settings Table	Allows you to define the clock signals used in the system module. For each clock in the clock settings table, you can specify: ● Name ● Source - Clock signals can be provided from an external source, or can be generated by a component inside the system module. ● Frequency in MHz ● Pipeline for high performance - SOPC Builder can pipeline the Avalon switch fabric for the clock domain, which improves f_{MAX} performance.
Messages Window	Displays information, warning, or error messages related to the current system.

Note for Table 2–1:
(1) Options available in the View menu alter how this element is displayed.

You can connect any master port to any slave port, as long as they use the same interface protocol. If they use different interface protocols, they must communicate through a bridge component, such as the AHB–to–Avalon® bridge provided with SOPC Builder.

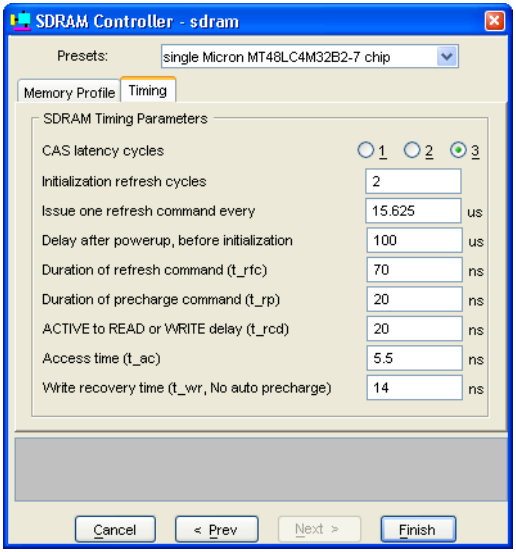
Adding a Component to the System

To add a component to the system, find the component in the list of available components and do one of the following:

- Double-click the component.
- Select the component, then click **Add**.
- Right-click the component and choose **Add New** <*component name*>.

If the component has any parameterized features, a wizard will appear allowing you to configure this instance of the component. Figure 2–4 shows an example of a configuration wizard for the SDRAM controller included with the Quartus II software.

Figure 2–4. SDRAM Controller Configuration Wizard



Like the overall SOPC Builder GUI, component configuration wizards use tabs to categorize GUI features, and have a message window that displays dynamic information about the current configuration of the component.

The parameters and information displayed in the configuration wizard depend on the component. Many wizards provide tool tips that give you information on how to specify each parameter.

You can open component documentation from within SOPC Builder. Right-click the component in the list of available components, and choose one of the document items listed.

Specifying Connections, Base Address, Clock & IRQ

After you add a component, you must configure how it fits within the system.

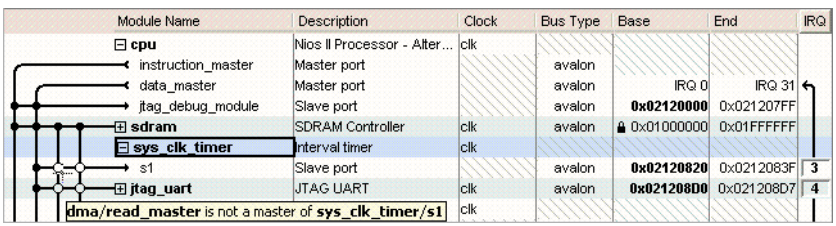
Connection Panel

In the connection panel you specify the master-slave connections between components.

Each SOPC Builder component can have one or more master and slave ports. Each slave port must be connected to a master port.

Hovering the mouse over the connection panel displays the potential connection points between components, represented as dots connecting wires. A filled dot shows that a connection is made; an open dot shows a potential connection point that is not currently connected. Clicking a dot toggles the connection status. See Figure 2–5.

Figure 2–5. Connection Panel



You can connect any master port to any slave port, as long as the ports use the same type of hardware interface. If they use different interfaces, they must communicate through a bridge component, such as the AHB-to-Avalon bridge provided with SOPC Builder.

Table of Active Components

After your component is connected in the connection panel, you use the table of active components to specify the parameters listed in Table 2–2.

Table 2–2. Table of Active Components

Parameter	Description
Name	Name of the instance of the component. SOPC Builder assigns a default name when you add a new component. To change this name, right click the component name and select **Rename**.
Use	Enables/Disables the component in the current system. Turning off the **Use** setting is equivalent to removing the component from the system.
Clock	Clock source for the component. You must choose one of the clocks defined in the clock settings table.
Base *(1)*	Base address where the slave port will appear in the master port's address space. SOPC Builder can automatically choose new base address values to avoid conflicts between all components. You can automatically assign base addresses for all components by choosing **Auto-Assign Base Addresses** (System menu). You can lock the base address on a component so that SOPC Builder will not change it automatically. To lock the base address, right-click the component in the table of active components, and choose **Lock Base Address**.
IRQ *(1)*	Specifies the IRQ value the slave drives to the master, if the slave port can generate interrupts. If you specify **NC** for an IRQ value, SOPC Builder will not connect interrupt signals from slave to master. SOPC Builder can automatically choose new IRQ values to avoid conflicts between all components. To automatically assign IRQs for all components, choose **Auto-Assign IRQs** (System menu).

Note to Table 2–2:
(1) This setting applies to slave ports only.

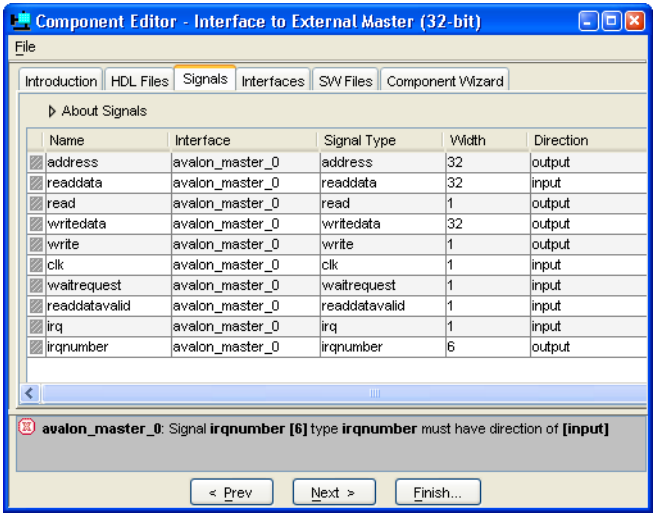
SOPC Builder automatically chooses defaults for these parameters when you add each component, but you must verify that they are appropriate for your system.

Creating User-Defined Components

You can use the SOPC Builder component editor to create a component from user-defined logic. To open the component editor, choose **New Component** (File menu) or select **Create New Component** in the list of available components, and click **Add**.

Figure 2–6 shows an example of the component editor editing a 32-bit master component.

Figure 2–6. SOPC Builder Component Editor



After creating a user-defined component, the process to instantiate the component is the same as for any other component.

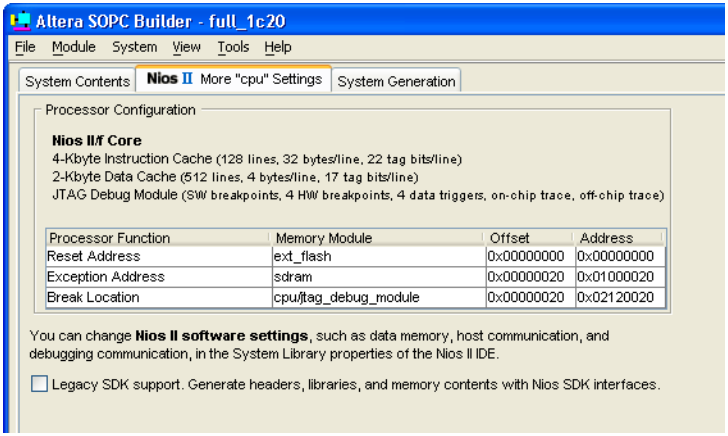
For instructions on developing a custom SOPC Builder component, see the *Developing SOPC Builder Components* chapter in Volume 4 of the *Quartus II Handbook*. For complete detail on the file structure of a component, see the *SOPC Builder Components* chapter in Volume 4 of the *Quartus II Handbook*. For details on the SOPC Builder component editor, see the *Component Editor* chapter in Volume 4 of the *Quartus II Handbook*.

System Dependency Tabs

Certain components must be configured based on system-level factors external to the component. SOPC Builder provides system dependency tabs, which allow further configuration of a component beyond the component's configuration wizard. System dependency tabs are titled **More "**<*Name of component instance*>**" Settings**, and appear next to the **System Contents** tab.

Figure 2–7 shows an example of the system dependency tab for an instance of the Nios® II processor named `cpu`. In this example, the Nios II processor reset and exception addresses depend on memory components in the system but external to the processor, and therefore uses a system dependency tab.

Figure 2–7. System Dependency Tab for a Nios II Processor



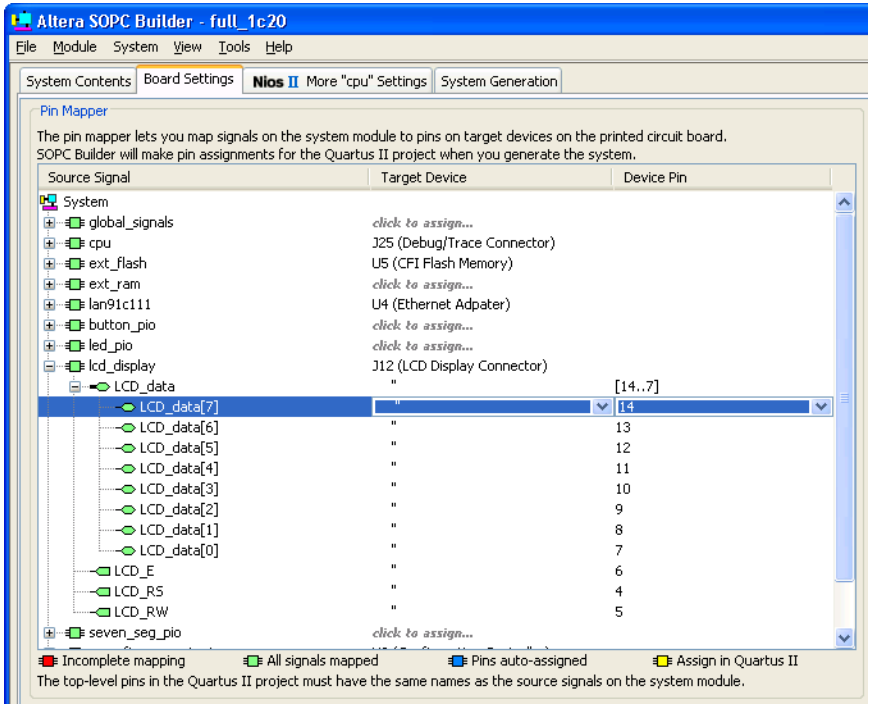
Board Settings Tab

The **Board Settings** tab provides board-specific settings for the target hardware platform. SOPC Builder displays a **Board Settings** tab only if you specify a target board on the **System Contents** tab.

The main feature of the **Board Settings** tab is the SOPC Builder pin mapper. The pin mapper simplifies the process of assigning FPGA pins. You use the pin mapper to map logical connections between system components and devices mounted on the PCB. Based on your pin mapper settings, SOPC Builder applies appropriate pin assignments to your Quartus II project.

In addition to accelerating the process of assigning FPGA pins, the pin mapper provides a level of assurance that you have accounted for the pin assignments required for a target board. Figure 2–8 on page 2–10 shows an example of the pin mapper for a target board.

Figure 2–8. Board Settings Tab

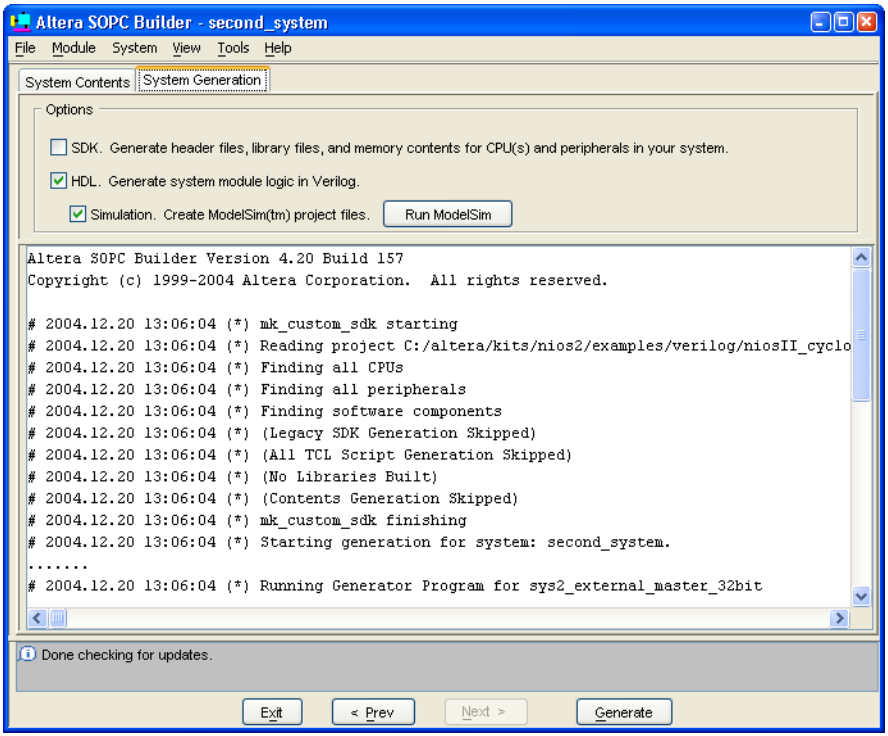


System Generation Tab

This section describes the settings available on the **System Generation** tab, and discusses the various outputs of SOPC Builder. System generation refers to SOPC Builder's process of generating output files that describe your system, based on the parameters you specified in the SOPC Builder GUI.

Figure 2–9 shows an example of the **System Generation** tab.

Figure 2–9. System Generation Page



Some SOPC Builder components, such as the Nios II processor, may modify the available options on this page.

Depending on the options on the **System Generation** tab, SOPC Builder generates the following outputs:

- Hardware design files
- Simulation model, testbench, and ModelSim® project files
- Files for software development

System Generation Tab Options

This section describes each of the options available on the **System Generation** tab.

SDK Option

When the **SDK** option is turned on, during system generation SOPC Builder creates a custom software development kit (SDK) directory in the Quartus II project directory for each CPU in the system. The SDK contains a memory map and software files (drivers, libraries, and utilities) for any system components that provide software support files.

The Nios II processor provides a different software development flow, and therefore does not use the **SDK** option.

SDK files are arranged into the following directories:

- **inc** – This directory contains header files. These files include the definition for the memory map, register declarations for included peripherals, and macros that can be used in creating embedded software applications.
- **lib** – This directory contains software library files. During system generation, processor components can include commands to have SOPC Builder compile the libraries automatically.
- **src** – This directory provides a location for application source code development. Example source code files associated with peripherals may also be copied into this directory during system generation.

Every time you generate or update the system hardware module, you must give the SDK files to the software engineers developing application code.

If you edit the files generated by SOPC Builder, save them with a unique filename to prevent the file from being overwritten in a subsequent system generation.

HDL Option

When the **HDL** option is turned on, during system generation SOPC Builder creates HDL files that describe the system, and stores them in the Quartus II project directory. The HDL files contain the following:

- The top-level system module
- An instance of every component in the system
- The Avalon switch fabric tailored to connect all components in the system
- A simulation model and a simulation testbench, depending on the Simulation option. See "Simulation Option" on page 2–13 for more details.

SOPC Builder outputs the top-level system module file in either Verilog HDL or VHDL, depending on which language you specified when starting SOPC Builder. However, some SOPC Builder components may provide source files in only one language.

Simulation Option

When the **Simulation** option is turned on, during generation SOPC Builder creates a simulation model and a test bench for the system. Simulation-specific files are written to a simulation directory in the Quartus II project directory, separate from the synthesizable HDL files.

The testbench is tailored to the structure of system module. The testbench provides the following functionality:

- Instantiates the system module
- Drives clock and reset inputs with default behaviors
- Instantiates and connects the simulation models provided for any components external to the system module, such as memory models

Individual components may also provide simulation files, which SOPC Builder copies into the simulation directory during system generation.

SOPC Builder generates a ModelSim project directory that includes the following files:

- A ModelSim Project File **(.mpf**) for the current system
- Simulation data files for all memory components that have initialized contents
- A **setup_sim.do** file that contains setup information and aliases customized for simulating the system module
- A **wave_presets.do** file that automatically displays a default set of useful waveforms

You can run the ModelSim software directly from SOPC Builder by clicking **Run ModelSim**. This requires that the ModelSim software be specified in your search path in the **Setup** window (File menu).

Run ModelSim might be disabled by a component in the system. For example, Nios II processor systems provide a different simulation flow, and therefore **Run ModelSim** is unavailable on the **System Generation** tab for Nios II processor systems.

The SOPC Builder output files for simulation are designed to work with the ModelSim simulator. You can use the SOPC Builder-generated simulation model and testbench with other HDL simulators. While the

ModelSim-specific files (**.tcl**, **.do**, **.mpf**, etc.) will not work directly with other simulators, you can inspect these files and use them as a basis for setting up similar capabilities.

Starting System Generation

After you have configured all system parameters and specified the desired generation options on this tab, clicking **Generate** starts the system generation process. **Generate** is available from all tabs in SOPC Builder. It is disabled whenever there are any errors displayed in the messages window.

The middle area of the **System Generation** tab is a progress display, showing a time-stamped list of progress messages that occur during system generation. SOPC Builder executes multiple tools and scripts to generate the system, and the status messages from each step are reported in the progress display.

If system generation completes successfully, SOPC Builder displays a final progress message:

```
# <timestamp> SUCCESS: SYSTEM GENERATION COMPLETED.
```

SOPC Builder saves a log file of the progress messages in the Quartus II project directory.

Other Tools

The Tools menu provides access to a dynamic list of downstream design tools, depending on the components in the system. For example, if the system contains a Nios II processor, Nios II processor-related tools are listed in the Tools menu.

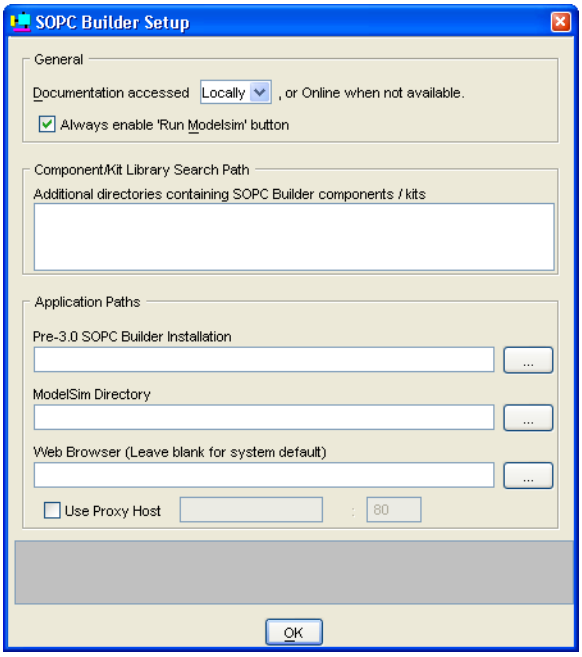
Preferences

The **SOPC Builder Setup** window (File menu) provides global options that affect SOPC Builder's operation, such as:

- Search path for SOPC Builder components
- Install path for ModelSim
- Location of documentation files
- Web browser settings (for accessing component documentation)

The **SOPC Builder Setup** window is shown in Figure 2–10.

Figure 2–10. SOPC Builder Setup Window



3. Avalon Switch Fabric

QII54003-6.0.0

Introduction

Avalon® switch fabric is a high-bandwidth interconnect structure that consumes minimal logic resources and provides greater flexibility than a typical shared system bus. This chapter describes the functions of Avalon switch fabric and the implementation of those functions.

High-Level Description

Avalon switch fabric is the glue that binds together components in a system based on the Avalon interface.

Avalon switch fabric is the collection of interconnect and logic resources that connects Avalon master and slave ports on components in a system. Avalon switch fabric encapsulates the connection details of a system. Avalon switch fabric guarantees that signals travel correctly between master and slave ports, as long as the ports adhere to the rules of the Avalon interface specification. As a result, system designers can think at a higher level and focus on the parts of a system that add value, rather than worry about the interconnect.

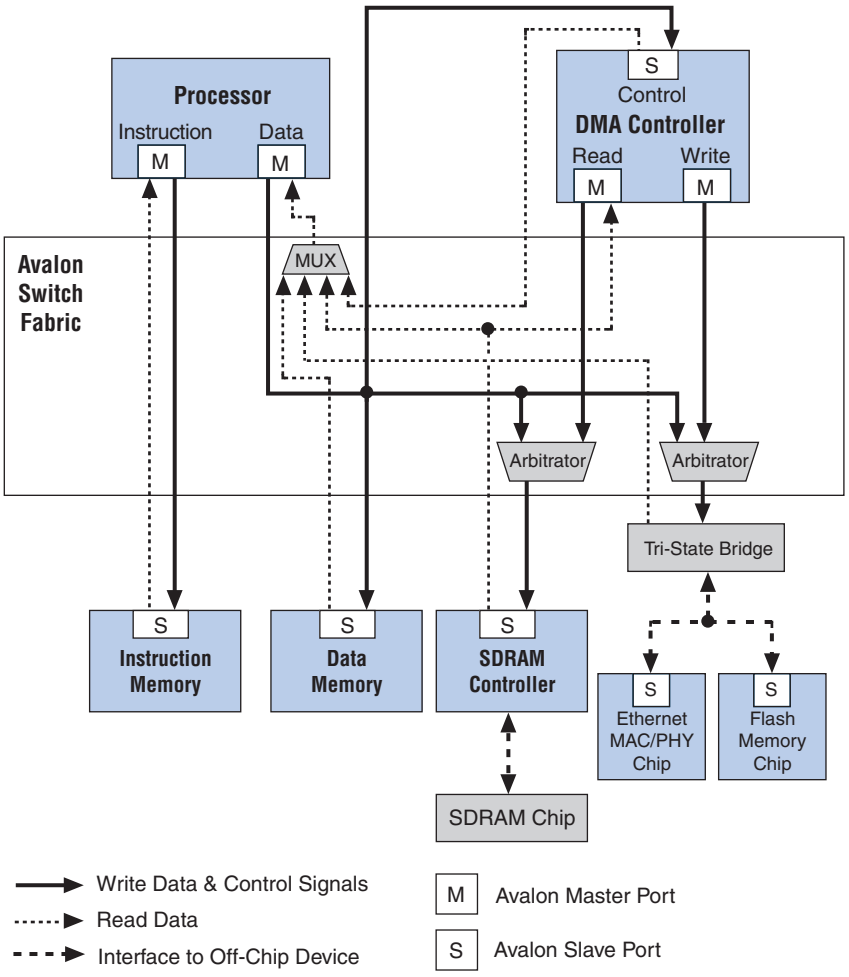
For details on the Avalon interface, refer to the *Avalon Interface Specification* available at **www.altera.com**. For details on how to use SOPC Builder to create Avalon switch fabric, refer to the *Tour of the SOPC Builder User Interface* chapter in volume 4 of the *Quartus II Handbook*.

Avalon switch fabric supports:

- Any number of master and slave components. The master-to-slave relationship can be one-to-one, one-to-many, many-to-one, or many-to-many.
- On-chip components
- Interfaces to off-chip peripherals
- Components of differing data widths
- Big-endian or little-endian components
- Components operating in different clock domains
- Components using multiple Avalon ports

Figure 3–1 shows a simplified diagram of the Avalon switch fabric in an example system with multiple masters.

Figure 3–1. Avalon Switch Fabric Block Diagram – Example System



Some components in Figure 3–1 use multiple Avalon ports. Because an Avalon component can have multiple Avalon ports, you can use Avalon switch fabric to create *super interfaces* that provide more functionality than a single Avalon port. For example, an Avalon slave port can have only one interrupt-request (IRQ) signal. However, by using three Avalon

slave ports together, you can create a component that generates three separate IRQs. In this case, SOPC Builder generates the Avalon switch fabric to connect all ports.

Generating Avalon switch fabric is SOPC Builder's primary purpose. Because SOPC Builder generates Avalon switch fabric automatically, most users do not interact directly with it or the HDL that describes it. You do not need to know anything about the internal workings of Avalon switch fabric to take advantage of the services it provides. On the other hand, a basic understanding of how it works can help you optimize your components and systems. For example, knowledge of the arbitration mechanism can help designers of multi-master systems minimize the impact of arbitration on the system throughput.

Fundamentals of Avalon Switch Fabric Implementation

Avalon switch fabric uses active logic to implement a switched interconnect structure that provides a dedicated path between master and slave ports. Avalon switch fabric consists of synchronous logic and routing resources inside an FPGA.

At each port interface, Avalon switch fabric manages Avalon transfers, responding to signals from the connected component. The signals that appear on the master port and corresponding slave port during a transfer can be very different, depending on how the Avalon switch fabric transports signals between the master-slave pair. In the path between master and slave ports, the Avalon switch fabric can introduce registers for timing synchronization, finite state machines for event sequencing, or nothing at all, depending on the services required by those ports.

Functions of Avalon Switch Fabric

Avalon switch fabric logic provides the following functions:

The behavior of these functions in a specific SOPC Builder system depends on the design of the components in the system and the settings made in the SOPC Builder GUI. The remaining sections of this chapter describe how SOPC Builder implements each function.

Address Decoding

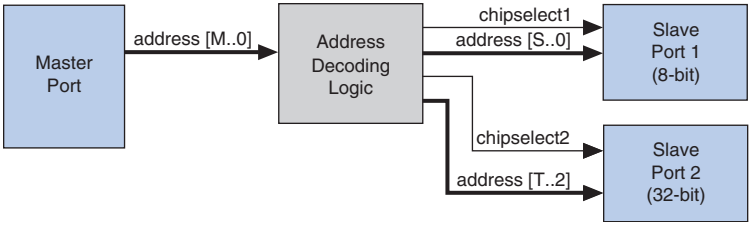
Address decoding logic in the Avalon switch fabric distributes an appropriate address and produces a chipselect signal for each slave port. Address decoding logic simplifies component design in the following ways:

- The Avalon switch fabric selects a slave port whenever it is being addressed by a master. Slave components do not need to decode the address to determine when they are selected.
- Slave port addresses are always properly aligned for the data width of the slave port.
- SOPC Builder automatically generates address decoding logic to implement the memory map specified in the GUI. Therefore, changing the system memory map does not involve manually editing HDL.

Figure 3–2 shows a block diagram of the address-decoding logic for one master and two slave ports. Separate address-decoding logic is generated for every master port in a system.

As shown in Figure 3–2, the address decoding logic handles the difference between the master address width (M) and the individual slave address widths (S & T). It also maps only the necessary master address bits to access words in each slave port's address space.

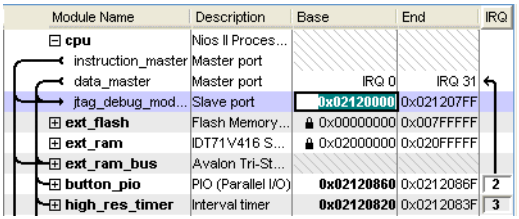
Figure 3–2. Block Diagram of Address Decoding Logic



All figures in this chapter are simplified to show only the particular function being discussed. In a complete system, the Avalon switch fabric might alter the address, data, and control paths beyond what is shown in any one particular figure.

In the SOPC Builder GUI, the user-configurable aspects of address decoding logic are controlled by the **Base** setting in the list of active components on the **System Contents** page, as shown in Figure 3–3.

Figure 3–3. Base Settings in SOPC Builder Control Address Decoding

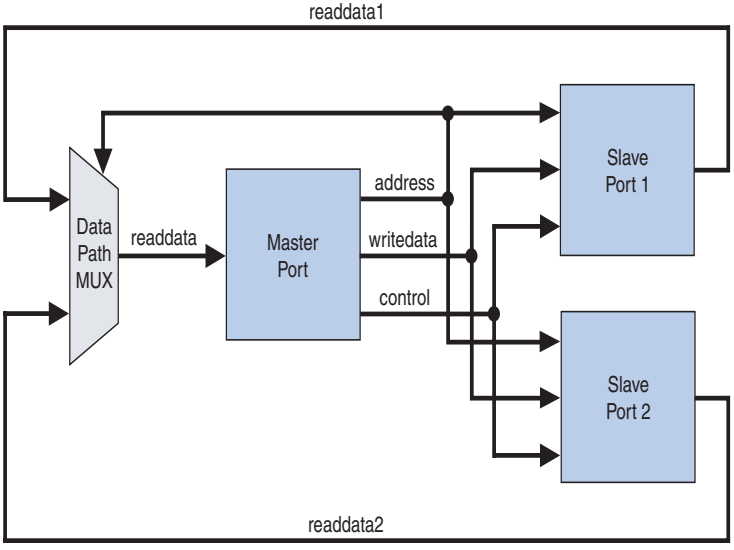


Data-Path Multiplexing

Data-path multiplexing logic in the Avalon switch fabric aggregates read-data signals from multiple slave ports during a read transfer, and presents the signals from only the selected slave back to the master port.

Figure 3–4 shows a block diagram of the data-path multiplexing logic for one master and two slave ports. SOPC Builder generates separate data-path multiplexing logic for every master port in the system.

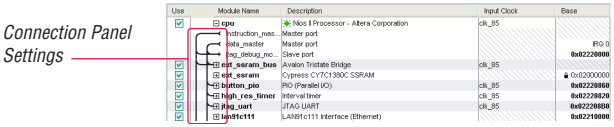
Figure 3–4. Block Diagram of Data-Path Multiplexing Logic



Data-path multiplexing is not necessary in the write-data direction for write transfers. The `writedata` signals are distributed equally to all slave ports, and each slave port ignores `writedata` except for when the address-decoding logic selects that port.

In the SOPC Builder GUI, the generation of data-path multiplexing logic is specified using the connections panel on the **System Contents** page, as shown in Figure 3–5.

Figure 3–5. Connection Panel Settings in SOPC Builder Control Data-Path Multiplexing

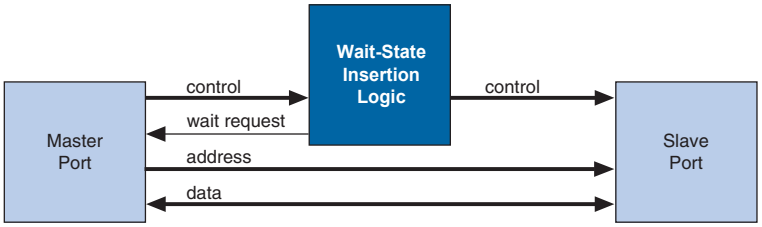


Wait-State Insertion

Wait states extend the duration of a transfer by one or more cycles for the benefit of components with special synchronization needs. Wait-state insertion logic accommodates the timing needs of each slave port, and coordinates the master port to wait until the slave can proceed. Avalon switch fabric inserts wait states into a transfer when the target slave port cannot respond in a single clock cycle. Avalon switch fabric also inserts wait states in cases when slave read-enable and write-enable signals have setup or hold time requirements.

Wait-state insertion logic is a small finite-state machine that translates control signal sequencing between the slave side and the master side. Figure 3–6 shows a block diagram of the wait-state insertion logic between one master and one slave.

Figure 3–6. Block Diagram of Wait-State Insertion Logic



Avalon switch fabric can force a master port to wait for several reasons in addition to the wait state needs of a slave port. For example, arbitration logic in a multi-master system can force a master port to wait until it is granted access to a slave port.

SOPC Builder generates wait-state insertion logic based on the properties of all slave ports in the system.

Pipelining for High Performance

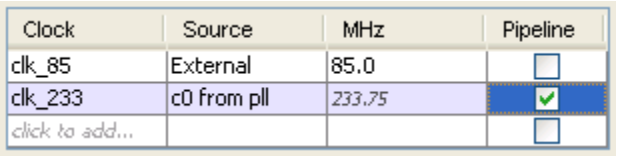
SOPC Builder can pipeline the Avalon switch fabric by inserting stages of registers between master-slave pairs. Adding pipeline registers can increase the f_{MAX} performance of the system and ensure that the critical timing path does not occur inside the Avalon switch fabric.

The pipeline registers introduce one or more clock cycles of latency between master-slave pairs, which creates a trade-off between transfer latency and f_{MAX} performance. The pipeline registers can also increase logic utilization considerably, depending on the complexity of the system. Components that support pipelined Avalon transfers minimize the effects of the pipeline latency. For details on how pipelining for high performance affects pipelined Avalon ports, see section "Pipeline Management" on page 3–8.

Pipeline registers are most likely to improve performance for the case of many master ports sharing a common slave port. For N masters accessing a slave port, the increased latency is on the order of $(\log_2 N + 1)$.

You specify whether or not to add pipelining for high performance with the clock settings table on the **System Contents** tab in SOPC Builder, shown in Figure 3–7. You can pipeline each clock domain separately by turning on its **Pipeline** check box.

Figure 3–7. Turning On Pipelining for High Performance



Pipeline Management

The Avalon interface supports pipelined read transfers. A pipelined Avalon port can start multiple read transfers in succession without waiting for the prior transfers to complete. Pipelined transfers allow master-slave pairs to achieve maximum throughput, even though the slave port may require one or more cycles of latency to return data for each transfer.

SOPC Builder generates Avalon switch fabric with pipeline management logic to take advantage of pipelined components wherever possible, based on the pipeline properties of each master-slave pair in the system. Regardless of the pipeline latency of a target slave port, SOPC Builder guarantees that read data arrives at each master port in the order requested. Because master and slave ports often have mismatched pipeline latency, Avalon switch fabric often contains logic to reconcile the differences. Many cases are possible, as shown in Table 3–1.

Table 3–1. Various Cases of Pipeline Latency in a Master-Slave Pair (Part 1 of 2)

Master Port	Slave Port	Pipeline Management Logic Structure
No Pipeline	No Pipeline	The Avalon switch fabric does not instantiate logic to handle pipeline latency.
No Pipeline	Pipelined with Fixed or Variable Latency	The Avalon switch fabric forces the master port to wait through any slave-side latency cycles. This master-slave pair gains no benefits of pipelining, because the master port is not pipelined and therefore waits for each transfer to complete before beginning a new transfer. However, while the master port is waiting, the slave port can accept transfers from a different master port.
Pipelined	No Pipeline	The Avalon switch fabric carries out the transfer as if neither port were pipelined, forcing the master port to wait until the slave port returns data.

Table 3–1. Various Cases of Pipeline Latency in a Master-Slave Pair (Part 2 of 2)

Master Port	Slave Port	Pipeline Management Logic Structure
Pipelined	Pipelined with Fixed Latency	The Avalon switch fabric coordinates the master port to capture data at the exact clock cycle when data is valid on the slave port. This case enables this master-slave pair to achieve maximum throughput performance.
Pipelined	Pipelined with Variable Latency	This is the simplest pipelined case, in which the slave port asserts a signal when its data is valid, and the master port captures the data. This case enables this master-slave pair to achieve maximum throughput performance.

SOPC Builder generates logic to handle pipeline latency based on the properties of the master and slave ports in the system. When configuring a system in SOPC Builder, there are no GUI settings that directly control the pipeline management logic in the Avalon switch fabric.

Endian Conversion

Starting with version 5.1 of the Quartus II software, SOPC Builder supports big endian master ports. Prior to version 5.1, SOPC Builder treated all components as little endian. With version 5.1 and later, an Avalon-based system can contain both big and little endian components.

The endianness of an Avalon port depends on the component design. Endianness affects the order a master port expects individual bytes to be arranged within a larger word. If all master ports in the system use the same endianness, then all master ports' perception of byte addresses is consistent within the system. In this case there is no further endian-related design consideration required.

Avalon switch fabric provides endian-conversion functionality to allow master ports of differing endianness to share memory. The Avalon endian-conversion logic hides the endian difference of master ports when the following conditions are met:

1. The master ports access a common memory slave port.
2. The data width of the master ports are equal.
3. The master ports read and write the memory using only native-width units of data. For example, a 32-bit master port can read and write only 32-bit units of data.
4. The master ports use a common interpretation of the data type.

As an example, consider a three-chip system comprised of a discrete 32-bit CPU chip, an FPGA containing 32-bit coprocessor logic (an SOPC Builder system), and a shared DDR SDRAM chip. Furthermore, suppose that the CPU is big endian, while the FPGA coprocessor system is little endian. In this case, the CPU and the coprocessor can share data in the SDRAM seamlessly without manually accounting for the endianness of data.

The Avalon switch fabric does not guarantee proper byte arrangement for big-endian master ports when accessing peripheral registers via an Avalon slave port.

Native Address Alignment & Dynamic Bus Sizing

SOPC Builder generates Avalon switch fabric to accommodate master and slave ports with unmatched data widths. Address alignment affects how slave data is aligned in a master port's address space, in the case that the master and slave data widths are different. Address alignment is a property of each slave port, and it may be different for each slave port in a system. A slave port can declare itself to use one of the following:

- Native address alignment
- Dynamic bus sizing

Table 3–2 demonstrates native address alignment and dynamic bus sizing for a 32-bit master port connected to a 16-bit slave port (a 2:1 ratio). In this example, the slave port is mapped to base address 0x0000000 in the master port. In Table 3–2, `OFFSET` refers to the offset into the 16-bit slave port address space.

Table 3–2. 32-Bit Master View of 16-Bit Slave Data

32-bit Master Address	Data with Native Alignment	Data with Dynamic Bus Sizing
`0x00000000` (word 0)	`0x0000:OFFSET[0]`	`0xOFFSET[1]:OFFSET[0]`
`0x00000004` (word 1)	`0x0000:OFFSET[1]`	`0xOFFSET[3]:OFFSET[2]`
`0x00000008` (word 2)	`0x0000:OFFSET[2]`	`0xOFFSET[5]:OFFSET[4]`
`0x0000000C` (word 3)	`0x0000:OFFSET[3]`	`0xOFFSET[7]:OFFSET[6]`
...		
(word *N*)	`0x0000:OFFSET[N]`	`0xOFFSET[2N+1]:OFFSET[2N]`

SOPC Builder generates appropriate address-alignment logic based on the properties of the master and slave ports in the system. When configuring a system in SOPC Builder, there are no GUI settings that directly control the address alignment in the Avalon switch fabric.

Native Address Alignment

Slave ports that access address-mapped registers inside the component generally use native address alignment. The defining properties of native address alignment are:

- Each slave offset (that is, word) maps to exactly one master word, regardless of the data width of the ports.
- One transfer on the master port generates exactly one transfer on the slave port.

In the case of native address alignment, Avalon switch fabric maps all slave data bits to the lower bits of the master data, and fills any remaining upper bits with zero. Avalon switch fabric performs simple wire-mapping in the data path, but nothing else.

Native address alignment is only valid if the master data width is equal to or wider than the slave data width. If an *N*-bit master port is connected to a wider slave with native alignment, then the master port can access only the lower *N* data bits at each offset in the slave.

Dynamic Bus Sizing

Slave ports that access memory devices generally use dynamic bus sizing. Dynamic bus sizing hides the details of interfacing a narrow memory device to a wider master port, and vice versa. When an *N*-bit master port accesses a slave port with dynamic bus sizing, the master port operates exclusively on full *N*-bit words of data, without awareness of the slave data width.

When using dynamic bus sizing, the slave data width must be a power of two.

Dynamic bus sizing provides the following benefits:

- Eliminates the need to create address-alignment hardware manually.
- Reduces design complexity of the master component.
- Enables any master port to access any memory device seamlessly, regardless of the data width.

In the case of dynamic bus sizing, the Avalon switch fabric includes a small finite state machine that reconciles the difference between master and slave data widths. The behavior is different depending on whether the master data width is wider or narrower than the slave.

Wider Master

In the case of a wider master, the dynamic bus-sizing logic accepts a single, wide transfer on the master side, and then performs multiple narrow transfers on the slave side. For a data-width ratio of *N*:1, the dynamic bus-sizing logic generates *N* slave transfers. The master port pays a performance penalty, because it must wait while multiple slave-side transfers complete.

In the case of a read transfer, the Avalon switch fabric merges slave data from multiple read transfers before presenting them to the master port. A read transfer from a wide master port always causes multiple slave-read transfers to sequential addresses in the slave's address space. For example, even if a 32-bit master port needs only one byte from a dynamically-aligned 8-bit memory, a master read transfer generates four slave transfers, and the master port waits until all four transfers complete.

During write transfers, dynamic bus-sizing logic uses the master-side byte-enable signals to generate appropriate slave write transfers. The dynamic bus-sizing logic performs as many slave-side transfers as necessary to write the specified byte lanes to the slave memory.

Narrower Master

In the case of a narrower master, one transfer on the master side generates one transfer on the slave side. In this case, multiple master word addresses map to a single offset in the slave memory space. The dynamic bus-sizing logic maps each master address to a subset of byte lanes in the appropriate slave offset. All bytes of the slave memory are accessible in the master address space. There is no performance penalty when accessing a wider slave port using dynamic bus sizing.

Table 3–3 demonstrates the case of a 32-bit master port accessing a 64-bit slave port with dynamic bus sizing. In the table, offset refers to the offset into the slave port memory space.

Table 3–3. 32-Bit Master View of 64-Bit Slave with Dynamic Bus Sizing

32-bit Address	Data
0x00000000 (word 0)	OFFSET[0]$_{31..0}$
0x00000004 (word 1)	OFFSET[0]$_{63..32}$
0x00000008 (word 2)	OFFSET[1]$_{31..0}$
0x0000000C (word 3)	OFFSET[1]$_{63..32}$

In the case of a read transfer, the dynamic bus-sizing logic multiplexes the appropriate byte lanes of the slave data to the narrow master port. In the case of a write transfer, the dynamic bus-sizing logic uses the slave-side byte-enable signals to write only to the appropriate byte lanes.

Arbitration for Multi-Master Systems

Avalon switch fabric supports systems with multiple master components. In a system with multiple master ports, such as the system pictured in Figure 3–1 on page 3–2, the Avalon switch fabric provides shared access to slave ports using a technique called slave-side arbitration. Slave-side arbitration determines which master port gains access to a specific slave port in the event that multiple master ports attempt to access the same slave port at the same time.

The multi-master architecture used by Avalon switch fabric offers the following benefits:

- Eliminates the need to create arbitration hardware manually.
- Allows multiple master ports to transfer data simultaneously. Unlike traditional host-side arbitration architectures in which each master must wait until it is granted access to the shared bus, multiple Avalon masters can simultaneously perform transfers with independent slaves. Arbitration logic stalls a master port only when multiple master ports attempt to access the same slave port during the same cycle.
- Eliminates unnecessary master-slave connections. The connection between a master port and a slave port exists only if it is specified in the SOPC Builder GUI. If a master port never initiates transfers to a specific slave port, no connection is necessary, and therefore SOPC Builder does not waste logic resources to connect the two ports.
- Provides configurable arbitration settings, and arbitration for each slave port is specified independently. For example, you can grant one master port the most access to a particular slave port, while other master ports have more access to other slave ports.
- Simplifies master component design. The details of arbitration are encapsulated inside the switch fabric. Each Avalon master port connects to the Avalon switch fabric like it is the only master port in the system. As a result, you can reuse a component in single-master and multi-master systems without requiring design changes to the component.

This section discusses the architecture of the Avalon switch fabric generated by SOPC Builder for multi-master systems.

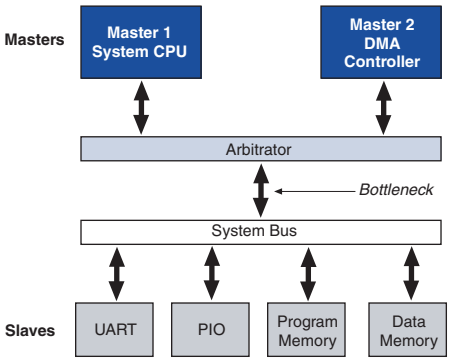
Traditional Shared Bus Architectures

As a frame of reference for the discussion of multiple masters and arbitration, this section describes traditional bus architectures.

In traditional bus architectures, one or more bus masters and bus slaves connect to a shared bus, consisting of wires on a printed circuit board. A single arbitrator controls the bus (that is, the path between bus masters and bus slaves), so that multiple bus masters do not simultaneously drive the bus and cause electrical contention. Each bus master requests control of the bus from the arbitrator, and the arbitrator grants access to a single master at a time. Once a master has control of the bus, the master performs transfers with a bus slave. If multiple masters attempt to access the bus at the same time, the arbitrator allocates the bus resources to a single master based on fixed arbitration rules, forcing all other masters to wait. For example, the priority arbitration scheme—in which the arbitrator always grants control to the master with the highest priority—is used in many existing bus architectures.

Figure 3–8 illustrates the bus architecture for a traditional processor system. Access to the shared system bus becomes the bottleneck for throughput and utilization performance. Only one master has access to the bus at a time, which means that other masters are forced to wait (diminishing throughput), and only one slave can transfer data at a time (diminishing utilization).

Figure 3–8. Bus Architecture in a Traditional Microprocessor System



Slave-Side Arbitration

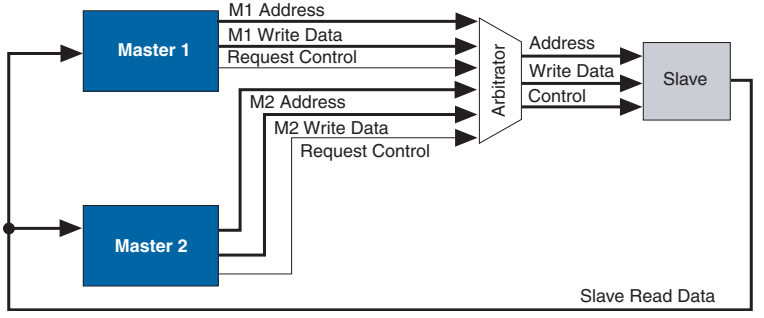
The multi-master architecture used by Avalon switch fabric eliminates the bottleneck for access to a shared bus, because the system does not have shared bus lines. Avalon master-slave pairs are connected by dedicated paths. A master port never waits to access a slave port, unless a different master port attempts to access the same slave port at the same time. As a result, multiple master ports can be active at the same time, simultaneously transferring data with independent slave ports.

A multi-master Avalon system requires arbitration, but only when two masters contend for the same slave port. This arbitration is called slave-side arbitration, because it is implemented at the point where two (or more) master ports connect to a single slave. Master ports contend for individual slave ports, not for a shared bus resource.

For example, Figure 3–1 on page 3–2 demonstrates a system with two master ports (a CPU and a DMA controller) sharing a slave port (an SDRAM controller). Arbitration is performed on the SDRAM slave port; the arbitrator dictates which master port gains access to the slave port if both master ports initiate a transfer with the slave port at the same time.

Figure 3–9 focuses on the two master ports and the shared slave port, and shows additional detail of the data, address, and control paths. The arbitrator logic multiplexes all address, data, and control signals from a master port to a shared slave port.

Figure 3–9. Detailed View of Multi-Master Connections



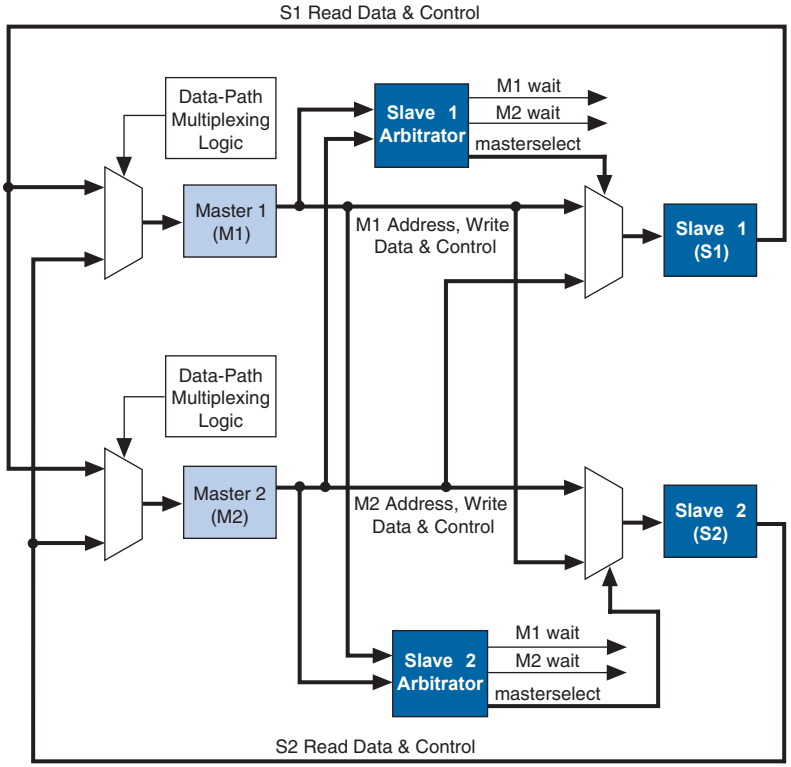
Arbitrator Details

SOPC Builder generates an arbitrator for every slave port connected to multiple master ports, based on arbitration parameters specified in the SOPC Builder GUI. The arbitrator logic performs the following functions for its associated slave port:

- Evaluates the address and control signals from each master port at every clock cycle when a new transfer can begin, and determines which master port, if any, is requesting access to the slave.
- Chooses which master port gains access to the slave next.
- Grants access to the chosen master port (that is, allows it to proceed with the transfer), and forces all other requesting master ports to wait.
- Uses multiplexers to connect address, control, and data paths between the multiple master ports and the slave port. The arbitrator logic guarantees that an appropriate master port (if any) is connected to the slave port.

Figure 3–10 shows the arbitrator logic in an example multi-master system with two master ports, each connected to two slave ports.

Figure 3–10. Block Diagram of Arbitrator Logic



Arbitration Rules

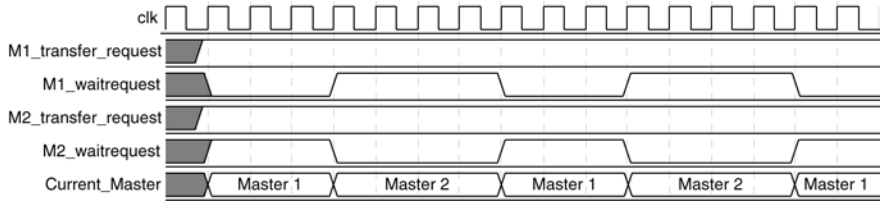
This section describes the rules by which the arbitrator grants access to master ports when they contend.

Fairness-Based Shares

Avalon arbitrator logic uses a fairness-based arbitration scheme. In a fairness-based arbitration scheme, each master port pair has an integer value of transfer *shares* with respect to a slave port. One share represents permission to perform one transfer.

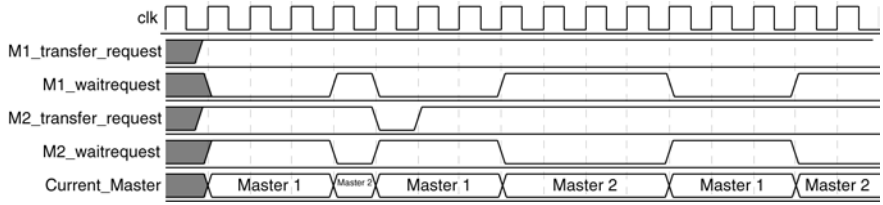
For example, assume that two master ports continuously attempt to perform back-to-back transfers to a slave port. Master 1 is assigned three shares and Master 2 is assigned four shares. In this case, the arbitrator grants Master 1 access for three transfers, then Master 2 for four transfers. This cycle repeats indefinitely. Figure 3–11 demonstrates this case, showing each master port's transfer request output, wait request input (which is driven by the arbitrator logic), and the current master with control of the slave.

Figure 3–11. Arbitration of Continuous Transfer Requests from Two Master Ports



If a master stops requesting transfers before it exhausts its shares, it forfeits all its remaining shares, and the arbitrator grants access to another requesting master. See Figure 3–12. After completing one transfer, Master 2 stops requesting for one clock cycle. As a result, the arbitrator grants access back to Master 1, which gets a replenished supply of shares.

Figure 3–12. Arbitration of Two Masters with a Gap in Transfer Requests



Round-Robin Scheduling

When multiple master ports contend for access to a slave port, the arbitrator grants shares in round-robin order. At every slave transfer, only requesting master ports are included in the round-robin arbitration.

Burst Transfers

Avalon burst transfers grant a master port uninterrupted access to a slave port for a specified number of transfers. The master port specifies the number of transfers when it initiates the burst. Once a burst begins between a master-slave pair, arbitrator logic does not allow any other master port to access the slave port until the burst completes. For further information, see "Burst Management" on page 3–20.

Minimum Share Value

A component design can declare the minimum number of shares in each round-robin cycle, which affects how the arbitrator grants access. For example, if a slave port has a minimum share value of ten, then the arbitrator will grant at least ten shares to any master port when it begins a sequence of transfer requests. The arbitrator might grant more shares, if the master port is assigned more shares in the SOPC Builder GUI.

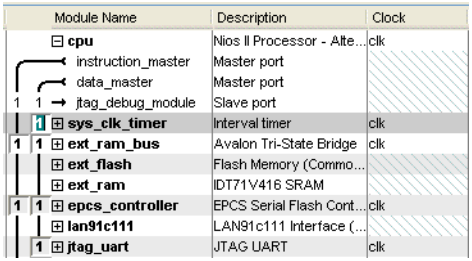
By declaring a minimum share value of *N*, a slave port declares that it is more efficient at handling continuous sequential transfers of length *N*. Accessing the slave port in sequences less than *N* incurs performance penalties that might prevent the slave port from achieving higher performance. By nature, continuous back-to-back master transfers tend to access sequential addresses. However, there is no requirement that the master port perform transfers to sequential addresses.

Burst transfers provide even higher performance for continuous transfers when they are guaranteed to access sequential addresses. The minimum share value does not apply to slave ports that support bursts; the burst length takes precedence over minimum share value. See "Burst Management" on page 3–20 for information.

Setting Arbitration Parameters in the SOPC Builder GUI

You specify the arbitration shares for each master using the connection panel on the **System Contents** tab of the SOPC Builder GUI, as shown in Figure 3–13.

Figure 3–13. Arbitration Settings on the System Contents Tab



The arbitration settings are hidden by default. To view them, on the View menu, click **Show Arbitration**.

Burst Management

Avalon switch fabric provides burst management logic to accommodate the burst capabilities of each port in the system, including ports that do not support burst transfers. Burst management logic is a finite state machine that translates the sequencing of address and control signals between the slave side and the master side.

The maximum burst length for each port is determined by the component design and is independent of other ports in the system. Therefore, a particular master port might be capable of initiating a burst longer than a slave port's maximum supported burst length. In this case, the burst management logic translates the master burst into smaller slave bursts, or into individual slave transfers if the slave port does not support bursts. Until the master port completes the burst, the Avalon arbitrator logic prevents other master ports from accessing the target slave port.

For example, if a master port initiates a burst of 16 transfers to a slave port with maximum burst length of 8, the burst management logic initiates two bursts of length 8 to the slave port. If a master port initiates a burst of 16 transfers to a slave port that does not support bursts, the burst management logic initiates 16 separate transfers to the slave port.

Clock Domain Crossing

SOPC Builder generates clock-domain crossing (CDC) logic that hides the details of interfacing components operating in asynchronous clock domains. The Avalon switch fabric upholds the Avalon protocol with each port independently, and therefore each Avalon port need only be aware of its own clock domain. The Avalon switch fabric logic propagates transfers across clock domain boundaries transparently to the user.

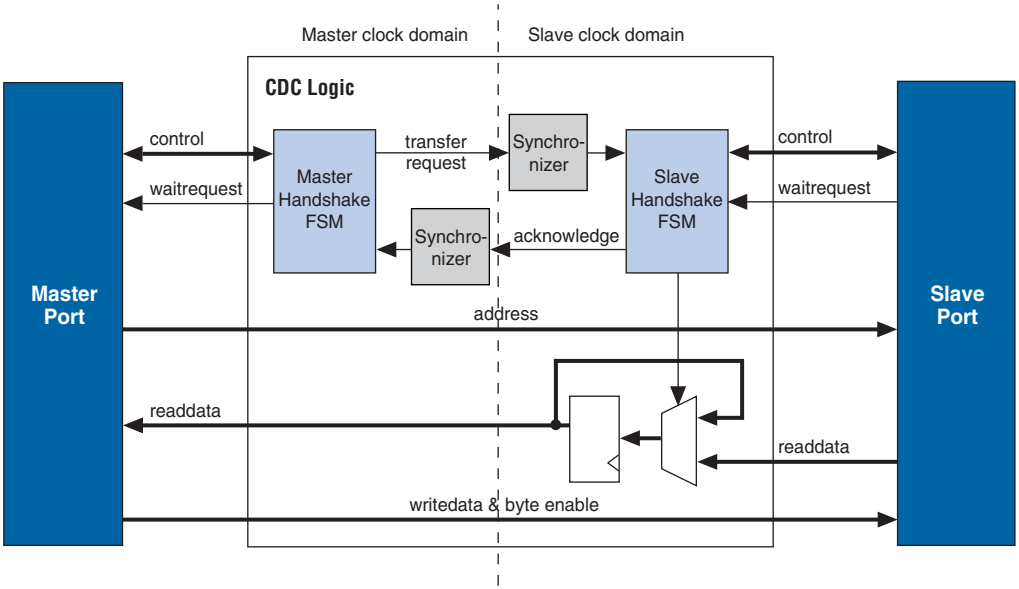
The CDC logic in Avalon switch fabric provides the following benefits that simplify system design efforts:

- Allows component interfaces to operate at a different clock frequency than system logic.
- Eliminates the need to design CDC hardware manually.
- Each Avalon port operates in only one clock domain, which reduces design complexity of components.
- Enables master ports to access any slave port without awareness of the slave clock domain.
- Allows you to focus performance optimization efforts only on components that require fast clock speed.

Description of Clock Domain-Crossing Logic

The CDC logic consists of two finite state machines (FSM), one in each clock domain, which use a simple hand-shaking protocol to propagate transfer control signals (read request, write request, and the master wait-request signals) across the clock boundary. Figure 3–14 shows a block diagram of the clock domain crossing logic between one master and one slave port.

Figure 3–14. Block Diagram of Clock Domain-Crossing Logic



The Synchronizer blocks in Figure 3–14 use multiple stages of flip-flops to eliminate the propagation of metastable events on the control signals that enter the hand-shake FSMs.

The CDC logic works with any clock ratio. Altera® tests the CDC logic extensively on a variety of system architectures, both in simulation and in hardware, to ensure that the logic functions correctly.

The typical sequence of events for a transfer across the CDC logic is described below:

1. Master port asserts address, data, and control signals.
2. The master handshake FSM captures the control signals, and immediately forces the master port to wait.

   The FSM uses only the control signals, not address and data. For example, the master port simply holds the address signal constant until the slave side has safely captured it.

3. Master handshake FSM initiates a transfer request to the slave handshake FSM.

4. The transfer request is synchronized to the slave clock domain.

5. The slave handshake FSM processes the request, performing the requested transfer with the slave port.

6. When the slave transfer completes, the slave handshake FSM sends an acknowledge back to the master handshake FSM.

7. The acknowledge is synchronized back to the master clock domain.

8. The master handshake FSM completes the transaction by releasing the master port from the wait condition.

Transfers proceed as normal on the slave and the master side, without a special protocol to handle crossing clock domains. From the perspective of a slave port, there is nothing different about a transfer initiated by a master port in a different clock domain. From the perspective of a master port, a transfer across clock domains simply takes extra clock cycles. Similar to other transfer delay cases (for example, arbitration delay and/or wait states on the slave side), the Avalon switch fabric simply forces the master port to wait until the transfer terminates. As a result, latency-aware master ports do not benefit from pipelining when performing transfers to a different clock domain.

Location of Clock Domain Crossing Logic

SOPC Builder automatically determines where to insert the CDC logic, based on the system contents and the connections between components. SOPC Builder places CDC logic to maintain the highest transfer rate for all components. SOPC Builder evaluates the need for CDC logic on each slave port independently, and generates CDC logic wherever necessary.

Duration of Transfers Crossing Clock Domains

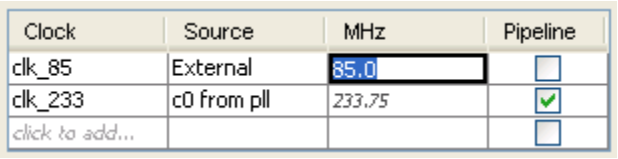
CDC logic extends the duration of master transfers across clock domain boundaries. In the worst case, each transfer is extended by five master clock cycles and five slave clock cycles. The components of this delay are the following:

- Four additional master clock cycles, due to the master-side clock synchronizer
- Four additional slave clock cycles, due to the slave-side clock synchronizer
- One additional clock in each direction, due to potential metastable events as the control signals cross clock domains

Implementing Multiple Clock Domains in the SOPC Builder GUI

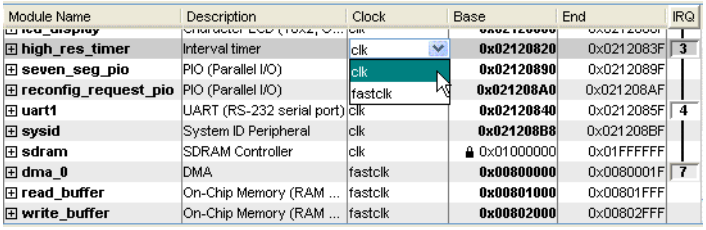
You specify the clock domains used by your system on the **System Contents** tab of the SOPC Builder GUI. You define the input clocks to the system using the clock settings table, shown in Figure 3–15. Clock sources can be driven by external input signals to the system module, or by PLLs inside the system module. Clock domains are differentiated based on the name of the clock. It is possible to create multiple asynchronous clocks with the same frequency.

Figure 3–15. Clock Settings on the System Contents Tab



After you define the system clocks, you specify which clock drives which components using the table of active components, as shown in Figure 3–16.

Figure 3–16. Assigning Clocks to Components



For further details, refer to the *Building Systems with Multiple Clock Domains* chapter in volume 4 of the *Quartus II Handbook*.

Interrupt Controller

In systems with one or more slave ports that generate IRQs, the Avalon switch fabric includes interrupt controller logic. A separate interrupt controller is generated for each master port that accepts interrupts. The interrupt controller aggregates IRQ signals from all slave ports, and maps slave IRQ outputs to user-specified values on the master IRQ inputs.

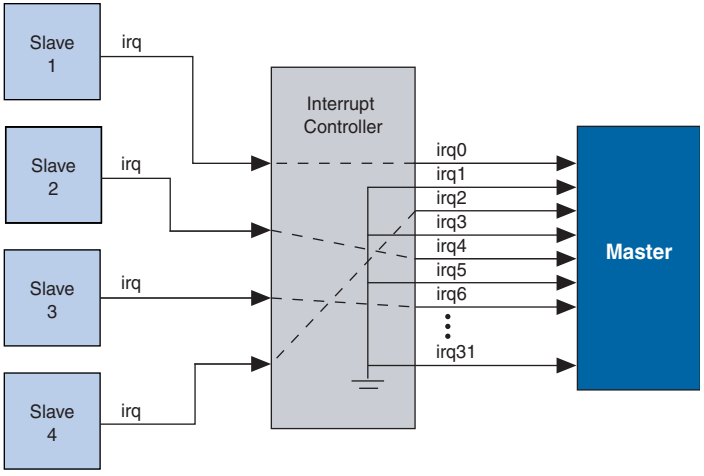
Each slave port optionally produces an IRQ output signal. There are two master signals related to interrupts: `irq` and `irqnumber`. SOPC Builder generates the interrupt controller in one of two configurations, software priority or hardware priority, depending on the interrupt signals present on the master port.

Software Priority

In the software priority configuration, the Avalon switch fabric passes IRQs directly from slave to master port, without making any assumptions about IRQ priority. In the event that multiple slave ports assert their IRQs simultaneously, the master logic (presumably under software control) determines which IRQ has highest priority, then responds appropriately.

Using software priority, the interrupt controller can handle up to 32 slave IRQ inputs. The interrupt controller generates a 32-bit signal `irq[31..0]` to the master port, and simply maps slave IRQ signals to the bits of `irq[31..0]`. Any unassigned bits of `irq[31..0]` are permanently disabled. Figure 3–17 shows an example of the interrupt controller mapping the IRQs on four slave ports to `irq[31..0]` on a master port.

Figure 3–17. IRQ Mapping Using Software Priority

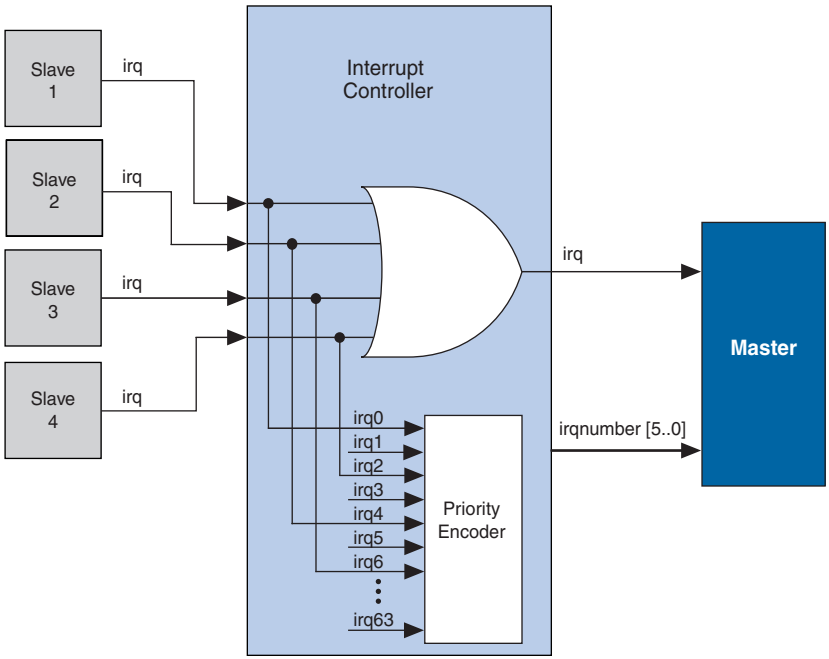


Hardware Priority

In the hardware priority configuration, in the event that multiple slaves assert their IRQs simultaneously, the Avalon switch fabric (i.e. hardware logic) identifies the IRQ of highest priority and passes only that IRQ number to the master port. An IRQ of lesser priority is undetectable until a master port clears all IRQs of higher priority.

Using hardware priority, the interrupt controller can handle up to 64 slave IRQ signals. The interrupt controller generates a 1-bit `irq` signal to the master port, signifying that one or more slave ports have generated an IRQ. The controller also generates a 6-bit `irqnumber` signal, which outputs the encoded value of the highest pending IRQ. See Figure 3–18.

Figure 3–18. IRQ Mapping Using Hardware Priority

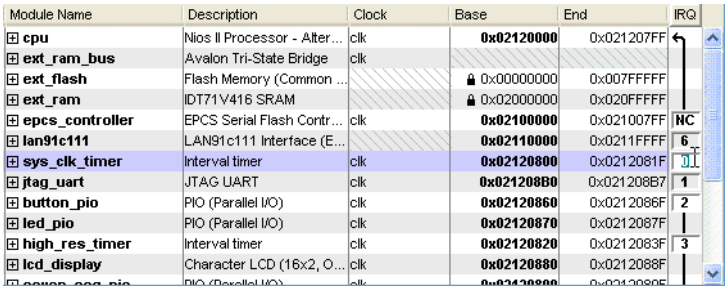


Assigning IRQs in the SOPC Builder GUI

You specify IRQ settings on the **System Contents** tab of the SOPC Builder GUI. After adding all components to the system, you make IRQ settings for all slave ports that can generate IRQs, with respect to each master

port. For each slave port, you can either specify an IRQ number, or specify not to connect the IRQ. Figure 3–19 shows the IRQ settings for multiple slave IRQs that drive the master component named **cpu**.

Figure 3–19. Assigning IRQs in the SOPC Builder GUI



Reset Distribution

The Avalon switch fabric generates and distributes a system-wide reset pulse to all logic in the system module. The switch fabric distributes the reset signal conditioned for each clock domain. The duration of the reset signal is at least one clock period.

The Avalon switch fabric asserts the system-wide reset in the following conditions:

- The global reset input to the system module is asserted.
- A slave port asserts its `resetrequest` signal.
- The FPGA is reconfigured.

All components must enter a well-defined reset state whenever the Avalon switch fabric asserts the system-wide reset. The timing of the reset signal is asynchronous to the operation of transfers.

4. SOPC Builder Components

QII54004-6.0.0

Introduction

This chapter describes in detail what an SOPC Builder component is. SOPC Builder components are individual design blocks that SOPC Builder uses to integrate a larger system module. Each component consists of a structured set of files within a directory.

The files in a component directory serve the following purposes:

- Defines the hardware interface to the component, such as the names and types of I/O signals.
- Declares any parameters that specify the structure of the component logic and the component interface.
- Describes a configuration wizard GUI for configuring the component in SOPC Builder.
- Provides scripts and other information SOPC Builder needs to generate the component HDL and integrate the component into the system module.
- Contains component-related information, such as software drivers, necessary for development steps downstream from SOPC Builder.

For details on creating custom components, see the *Developing SOPC Builder Components* chapter in Volume 4 of the *Quartus II Handbook*. For details on the SOPC Builder component editor, see the *Component Editor* chapter in Volume 4 of the *Quartus II Handbook*.

Sources of Components

There are several sources for components, including the following:

- The Quartus® II software, which includes SOPC Builder, installs a number of components.
- Altera® development kits, such as the Nios® II Development Kit, provide SOPC Builder components as features.
- Third-party developers provide SOPC Builder Ready components, including component directories and documentation on how to use the component.
- You can package your own HDL files into a new, custom component, using the SOPC Builder component editor.

While it is possible to write component files manually, Altera strongly recommends you use the SOPC Builder component editor to create custom components, for reasons of consistency and forward compatibility.

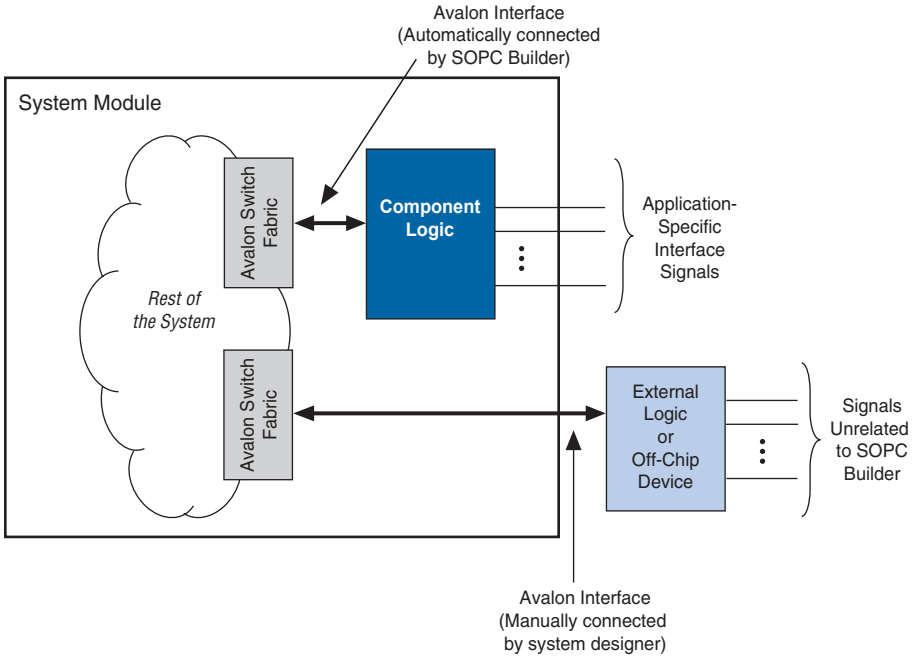
Location of the Component Hardware

There are two types of components, based on where the associated component logic resides:

- Components that include their associated logic inside the system module
- Components that interface to logic outside the system module

Figure 4–1 shows an example of both types of component.

Figure 4–1. Component Logic Inside and Outside the System Module



Components That Include Logic Inside the System Module

In this case, the component files provide a full description of the component hardware. During system generation, SOPC Builder instantiates the component logic inside the system module and automatically wires the component to the rest of the system. Internal to the system module, the component connects to the rest of the system through its Avalon® interface. The component can also have non-Avalon signals that SOPC Builder exposes on the top-level system module.

Components That Interface to Logic Outside the System Module

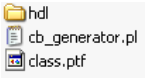
In this case, the component files describe only the interface to logic external to the system module. During system generation, SOPC Builder does not instantiate any logic for this component. Instead, SOPC Builder exposes an Avalon interface for this component on the top-level system module. You must manually wire the interface to external logic, such as a separate HDL module or an off-chip device.

As shown in Figure 4–1, in this case there is no physical embodiment of the SOPC Builder component. Components that interface to external logic describe only the shape of the Avalon interface; they do not include logic inside the system module.

Structure & Contents of a Component Directory

This section describes the files that exist in a component directory. Figure 4–2 shows a typical component directory created by the component editor.

Figure 4–2. Typical Component Directory



At a minimum, a component consists of a directory containing a file named **class.ptf**. Usually there are other files as well. The name of the enclosing directory is ignored. The **class.ptf** file defines everything that SOPC Builder needs to know about the name and location of component files.

As shown in Figure 4–2, the component directory can contain the following items, and other files:

- **class.ptf** file
- **cb_generator.pl** script
- **hdl** directory

class.ptf File

SOPC Builder reads this file to find everything it needs to know about the component. The **class.ptf** file defines the following aspects of a component:

1. The component identity – The component **class.ptf** file defines the following properties that identify a component:

- *Name* – The user-visible name of the component.
- *Class* – The unique identifier that SOPC Builder uses to differentiate components. The class name uses only filename-friendly characters. When you instantiate a component in SOPC Builder, the instantiation name defaults to the class name.
- *Version* – Identifies the version of a component. During system generation, SOPC Builder records the version number of each component in the system module.
- *Group* – Determines in which group the component appears in the list of available components in the SOPC Builder GUI.

2. How the component hardware connects into a system module, including:

   - *Interface to the component* – The **class.ptf** file describes the black box structure of the component, defining the name, type, and direction of each interface signal.
   - *Method to generate a hardware instance of the component* – If the component includes logic inside the system module, the **class.ptf** file specifies a mechanism for SOPC Builder to generate the component hardware. The **class.ptf** file typically specifies a separate executable file to generate the component instance.

3. How the component presents its configurable options to the user – The **class.ptf** file declares the user-configurable parameters, and specifies a GUI for configuring those parameters.

cb_generator.pl File

This file is a Perl script used by SOPC Builder during system generation. Based on parameters you specify in the SOPC Builder GUI, the script generates one or more instances of this component to be instantiated in the top-level system module. The name of the file is not significant. The file name is defined in the **class.ptf** file.

For components generated by the SOPC Builder component editor, this script creates a Verilog or VHDL wrapper that instantiates HDL modules defined by files in the **hdl** directory. During system generation, a typical generator script copies the HDL files to the Quartus II project directory, and renames the files uniquely to match the instance name. The generator script can also define parameters for the top-level HDL module, based on parameters specified in the SOPC Builder GUI.

The generator script for most Altera-provided components dynamically generates HDL for each instance of the component, based on parameters specified in the SOPC Builder GUI. Such components do not include HDL files, because the HDL is generated programmatically.

hdl Directory

This subdirectory contains HDL files that describes the component hardware. This directory is not required to exist, and the name of the directory is not significant. The generator script specifies the exact path to HDL files, if any.

Other Component Files

The component directory can contain other files and subdirectories, depending on the component's design and recommended usage. Typically, such items are not used directly by SOPC Builder, but are necessary for other stages of development. SOPC Builder ignores any files it cannot identify for its own purposes.

Items you might find in a component directory include the following:

- **inc** subdirectory – This directory includes the register map for a peripheral component. The register map is typically declared as a C header file that defines symbols and macros for accessing the component hardware. SOPC Builder does not use this information directly. For Nios II processor systems, the Nios II IDE uses the contents of **inc**.
- **HAL** subdirectory – This directory contains software drivers for a component. SOPC Builder does not use this information directly. For Nios II processor systems, the Nios II IDE uses the contents of **HAL** to generate software for the component.
- **UCOSII** subdirectory – This directory contains software drivers for a component, specific to the MicroC/OS-II real-time operating system (RTOS). SOPC Builder does not use this information directly. For Nios II processor systems, the Nios II IDE uses the contents of **UCOSII** to generate software for the component.
- Files associated with the generator script – The generator script may require data files, Perl libraries, or other files.
- **sdk** subdirectory – This directory contains software and header files to support the legacy software development kit (SDK) flow for the first-generation Nios processor.
- Data files, source code, or other files needed by tools other than SOPC Builder

Component Directory Location

Each time SOPC Builder starts up, it looks for component directories. Any components that it finds are displayed in the list of available components on the SOPC Builder **System Contents** tab.

SOPC Builder searches the following locations for component directories:

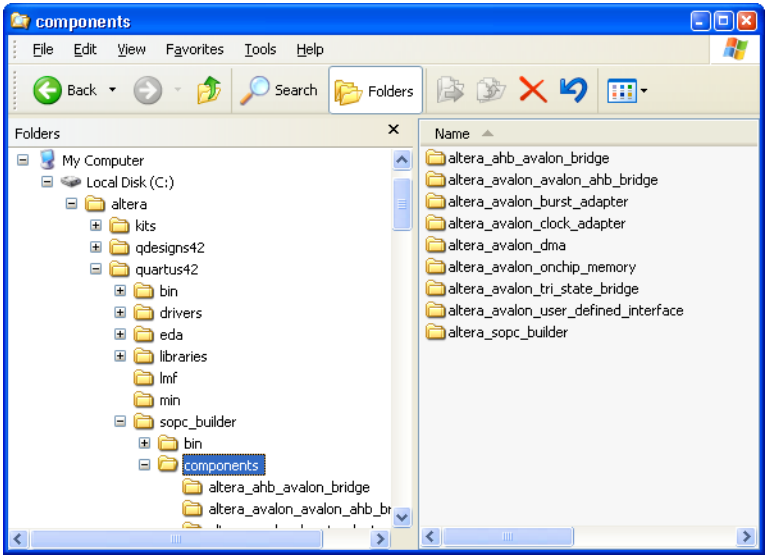
1. The current Quartus II project directory
2. Any directories specified under **Component/Kit Library Search Path** on the SOPC Builder Setup page in the SOPC Builder GUI.
3. **SOPC_BUILDER_PATH**
4. **QUARTUS_ROOTDIR/sopc_builder/**

The following describes the process by which SOPC Builder identifies components:

- **SOPC_BUILDER_PATH** and **QUARTUS_ROOTDIR** are environment variables that are defined during the Quartus II installation process.
- SOPC Builder searches each of these locations for subdirectories in the order shown, and then searches each subdirectory for a **class.ptf** file.
- When SOPC Builder finds a **class.ptf** file, it reads the file, identifies the component, and makes the component available in the SOPC Builder GUI.
- If multiple instances of the same component class exist, SOPC Builder uses the following rules to determine which one to use:
  - The component with the highest version takes precedence.
  - If all component versions are equal, the first component found takes precedence.
- If a directory is recognized as a kit directory (indicated by the presence of a file named **.sopc_builder**), then SOPC Builder further searches in the **components/** subdirectory.

Figure 4–3 shows an example of the directory of components installed with the Quartus II software. Note that not all directories correspond directly to user-visible components.

Figure 4–3. Avalon Component Directories



5. Component Editor

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Introduction

This chapter describes the SOPC Builder component editor. The component editor is a feature of SOPC Builder that lets you create and edit your own SOPC Builder components. You use the component editor GUI to do the following:

- Import hardware description language (HDL) files (if any) that describe the component hardware.
- Specify the hardware interface(s) to the component.
- Package software drivers into the component directory.
- Declare any parameters that alter the component structure or functionality, and define a user interface to let users parameterize instances of the component.

A typical development sequence might include the following steps, not necessarily in this order:

1. Design and test custom hardware in Verilog or VHDL.
2. Build an SOPC Builder system.
3. Use the component editor to package the custom HDL into an SOPC Builder component.
4. Incorporate one or more instances of your custom component into the SOPC Builder system.
5. Test the system including the new component, and make iterative refinements to the HDL.
6. Use component editor to update the component files.

You can also use the component editor to define an Avalon® interface to logic external to the system module. In this case, you do not provide HDL files, and use the component editor only to define the hardware interface.

Component Editor Output

Based on the settings you make using the component editor GUI, the component editor outputs a properly-formed component directory, containing the following items:

- **class.ptf** file – This file identifies the component, defines how the component hardware connects to the overall system, and declares user-configurable parameters.
- **cb_generator.pl** file – This file is a script used by SOPC Builder during system generation to generate instances of the component hardware.
- **hdl** directory – If the component includes logic inside the system module, this directory contains the HDL files.
- Software files – If this component is a processor peripheral, you can associate software files, such as drivers.

Exiting the component editor automatically prompts you to save the component files. On the File menu you can also click **Save** to save the files. Note that "saving" actually creates or copies multiple files, and stores them in their appropriate places in a component directory.

If you later edit the source code, you must update the component. Refer to section "Re-Editing a Component" on page 5–13.

The component editor always saves your new component to a subdirectory in the current Quartus® II project directory. You can relocate the component directory later, if you wish. For example, you could locate the component files in a central location so that other users can instantiate the component in their systems.

The component editor creates components with the following hardware characteristics:

- A component has one or more interfaces. Typically, an *interface* means an Avalon master port or slave port. The component editor lets you build a component with any combination of Avalon master or slave ports.
- Each interface is comprised of one or more signals.
- The component can use a set of global signals that are not associated to a specific Avalon interface.
- The component can include logic inside the system module, or serve as an interface to logic external to the system module.

See the *SOPC Builder Components* chapter in Volume 4 of the *Quartus II Handbook* for details on components. See the *Avalon Interface Specification* for details on the Avalon interface.

Starting the Component Editor

To start the component editor, in the SOPC Builder GUI on the File menu click **New Component**. When the component editor starts, it displays the **Introduction** tab, which provides a simple introduction to using the component editor.

The component editor GUI presents several tabs that group like settings on the same tab. A message window at the bottom of the component editor displays warning and error messages.

Each tab in the component editor GUI provides on-screen information that describes how to use each tab. Click the triangle at the top-left of each tab to view these instructions.

In general, you will proceed through the tabs from left to right as you progress through the component creation process. You can return to an earlier tab at any time.

HDL Files Tab

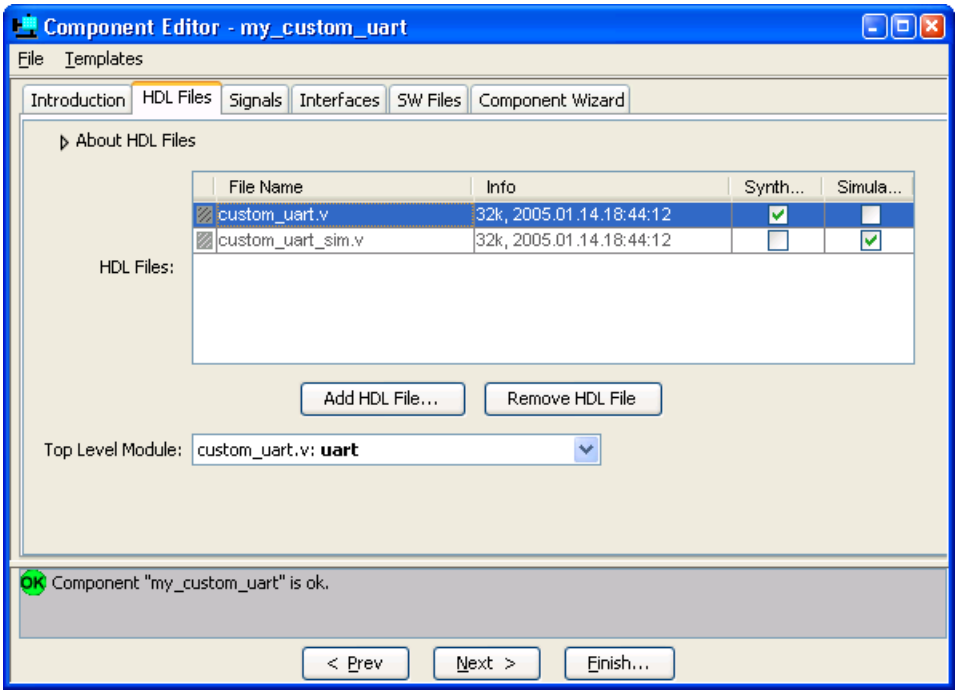
You use the **HDL Files** tab to import existing Verilog or VHDL files that describe the component hardware. When you save the component later, the component editor copies these files into your new component's directory.

If your component is an interface to external logic, then do not specify any files on this tab.

As you add each HDL file, the component editor analyzes the file by invoking the Quartus II Analyzer in the background. If there are errors, a dialog appears on the screen describing the problems. If the file is successfully analyzed, then the component editor identifies any design modules described in the file, and lists them in the **Top Level Module** list. If your HDL contains more than one module, you must select the appropriate top level module in the **Top Level Module** list.

Figure 5–1 shows an example of the **HDL Files** tab.

Figure 5–1. HDL Files Tab



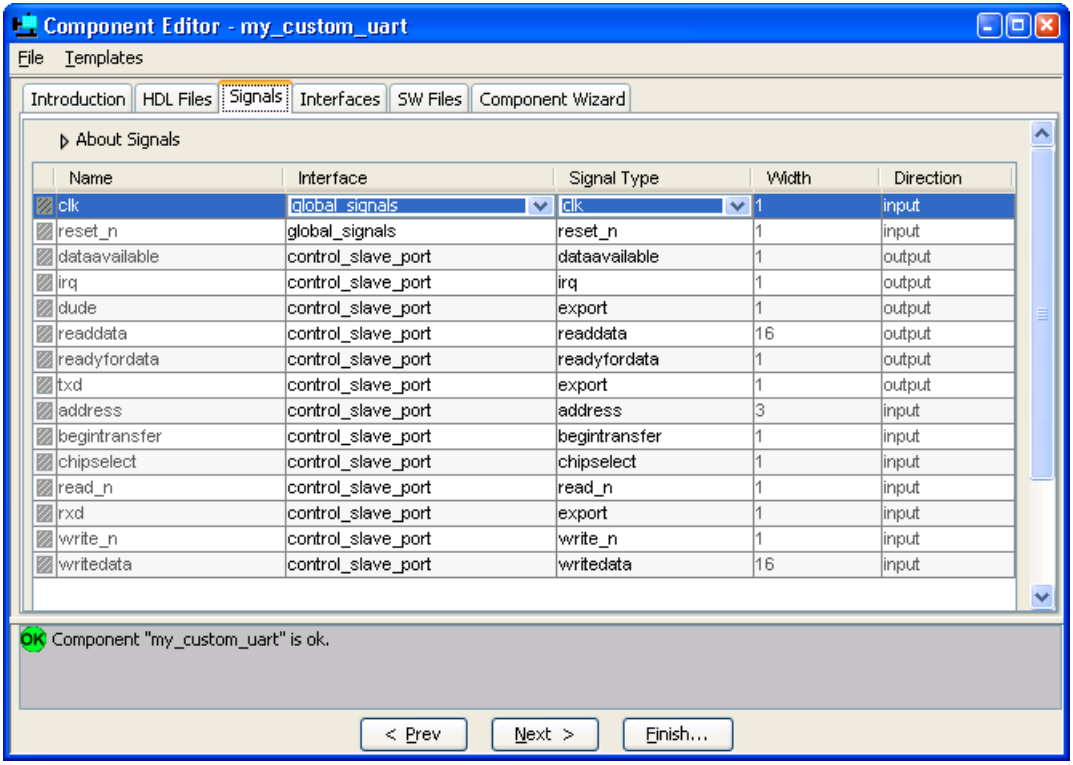
If separate HDL files define the synthesizable hardware and simulation model for the component, use the **Synthesis** and **Simulation** boxes to specify the role for each file.

Signals Tab

You use the **Signals** tab to specify the purpose of each signal in the top level component module. If you specified files on the **HDL Files** tab, then the signals on the top-level module appear on the **Signals** tab. If the component is an interface to external logic, then you must manually add the signals that comprise the interface to the external logic.

Figure 5–2 shows an example of the **Signals** tab.

Figure 5–2. Signals Tab



Each signal must be assigned a signal type. The default type is **export**, which means that SOPC Builder does not connect the signal internally to the system module, and instead exposes the signal on the top-level system module.

You assign each signal to an interface using the **Interface** column. In addition to Avalon port interfaces that you create, every component has a *global interface* for common signals such as `clk` and `reset`, and for exported signals.

Naming Signals for Automatic Type and Interface Recognition

The component editor can automatically recognize signal types and interfaces based on the names of signals in the source HDL file. The component editor recognizes signal names that follow a specific structure. Table 5–1 lists the signal name structures.

Table 5–1. Structure of Automatically Recognized Signal Names

Type of Signal	Name Structure
Avalon signal associated with a specific Avalon interface	<*Interface Type*>_<*Interface Name*>_<*Avalon Signal Type*>[_n]
Export signal associated with a specific Avalon interface	<*Interface Type*>_<*Interface Name*>_export_<*Name*>[_n]
Global clock or reset	gls_clk[_n] or gls_reset[_n]

For any value of *Interface Name* the component editor will automatically create an interface by that name, if necessary, and assign the signal to it. *Avalon Signal Type* must match one of the valid Avalon signal types. You can append `_n` to indicate an active-low signal. Table 5–2 lists the valid values for *Interface Type*.

Table 5–2. Valid Values for <Interface Type>

Value	Meaning
avs	Avalon slave port
avm	Avalon master port
ats	Avalon tristate slave port
gls	Global signals not associated to a specific Avalon port

The following example shows a Verilog HDL module declaration with signal names that infer two Avalon slave ports.

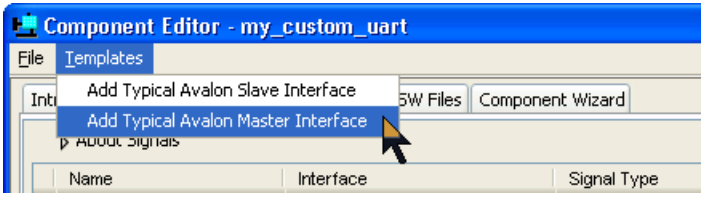
Example: Verilog Module With Automatically Recognized Signal Names

```
module my_multiport_component (
       // Signals for Avalon slave port "s1"
       avs_s1_clk,
       avs_s1_reset_n,
       avs_s1_address,
       avs_s1_read,
       avs_s1_write,
       avs_s1_writedata,
       avs_s1_readdata,
       avs_s1_export_dac_output,

       // Signals for Avalon slave port "s2"
       avs_s2_address,
       avs_s2_read,
       avs_s2_readdata,
       avs_s2_export_dac_output,

       // Global interface siganals
       gls_clk
   );
```

Templates for Interfaces to External Logic

If you are creating an interface to external logic, you can use the **Templates** menu to add a set of signals for a typical Avalon master or slave port. After adding a template, you can add or delete signals to customize the interface to meet your needs. Figures 5–3 shows the **Templates** menu.

Figure 5–3. Templates Menu



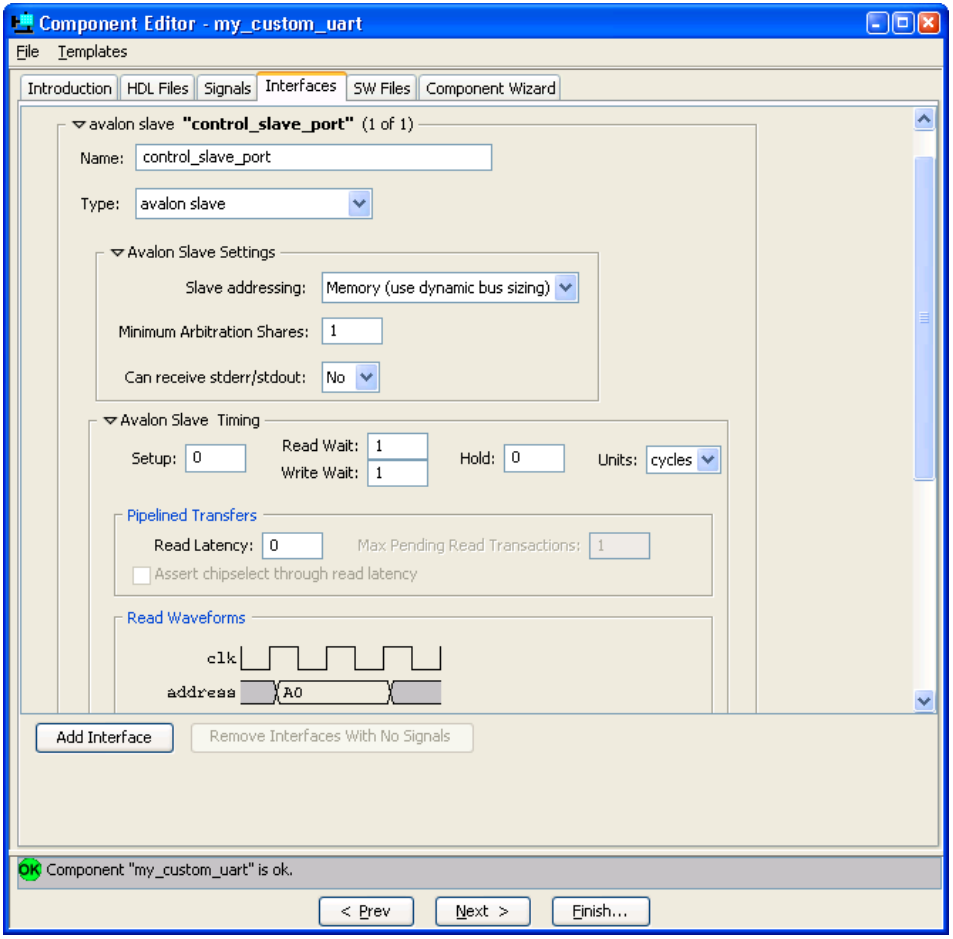
Interfaces Tab

The **Interfaces** tab lets you configure the interfaces on your component, and specify a name for each interface. The interface name identifies the interface, and appears in the SOPC Builder GUI connection panel. The interface name is also used to uniquely identify any signals that are exposed on the top-level system module.

The **Interfaces** tab also lets you configure the type and properties of each interface. For example, an Avalon slave interface has timing parameters which you must set appropriately.

Figure 5–4 shows an example of the **Interfaces** tab.

Figure 5–4. Interfaces Tab



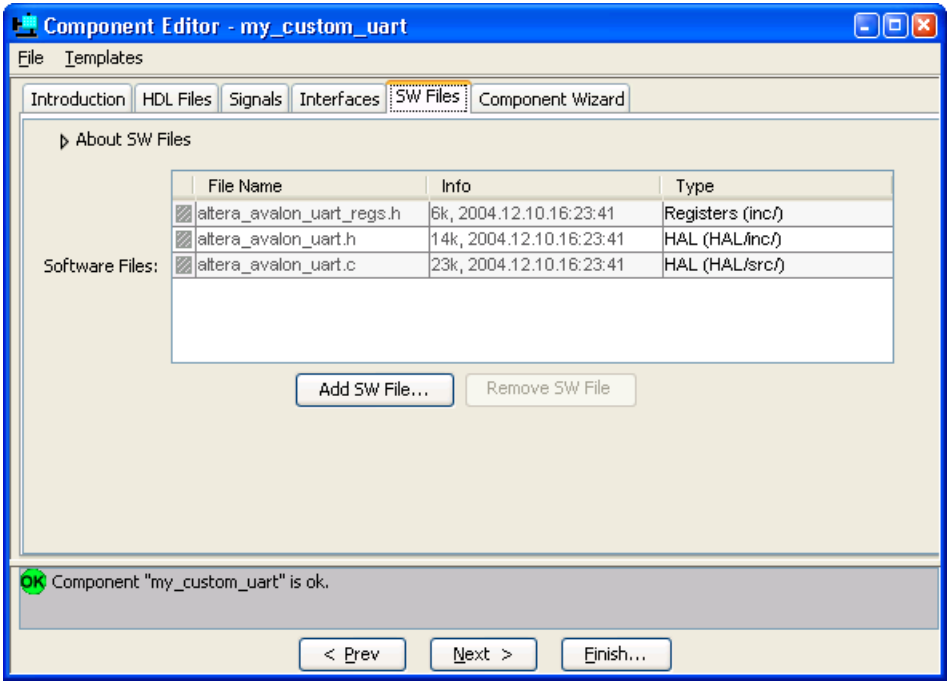
SW Files Tab

The software files tab (**SW Files**) lets you add existing driver software for your new component. When you save the component later, the component editor copies the software files to software subdirectories inside the component directory. The component editor uses the software directory structure specified by the hardware abstraction layer (HAL) for the Nios® II processor.

For information on writing component driver software for the Nios® II processor, including the directory structure, see the *Nios II Software Developer's Handbook*.

Figure 5–5 shows an example of the **SW Files** tab.

Figure 5–5. Software Files (SW Files) Tab

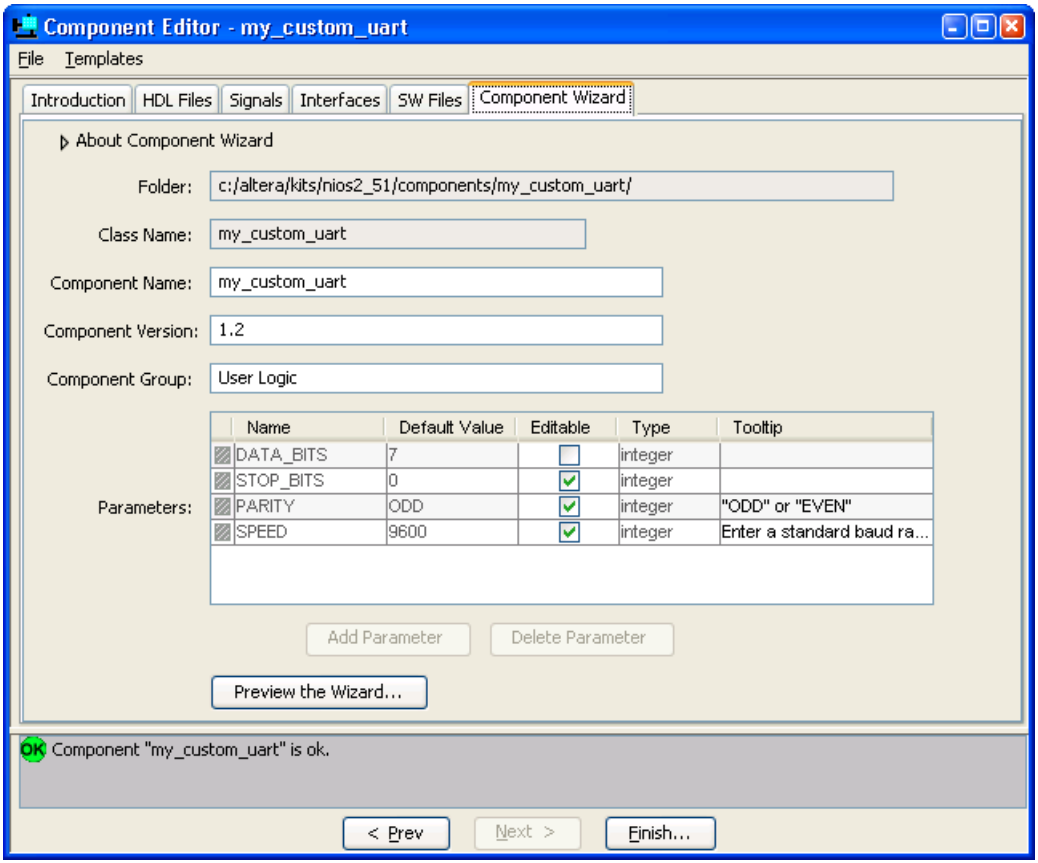


Component Wizard Tab

The **Component Wizard** tab provides settings that affect the presentation of your new component to the user.

Figure 5–6 shows an example of the **Component Wizard** tab.

Figure 5–6. Component Wizard Tab



Identifying Information

You can specify information that identifies the component, such as the component name, version, and group. The component name is the name that appears in the list of available components in the SOPC Builder GUI. The name can include spaces or other special characters.

Based on the component name you specify, the component editor creates a valid class name. The class name determines the component directory name.

You can also specify a component version and a component group. The group setting determines in which group SOPC Builder displays your component in the list of available components. If you enter a previously unused group name, SOPC Builder will display a new group by that name.

Parameters

The **Parameters** table lets you specify the user-configurable parameters for the component.

If the top-level module of the component HDL declares any parameters (*parameters* for Verilog, or *generics* for VHDL) then those parameters appear in the **Parameters** table. These parameters are presented to users when they create or edit an instance of your component.

To provide parameterization for a lower-level submodule, the top-level module must declare the parameter, and pass it down to the appropriate submodule.

Using the **Parameters** table, you can specify whether or not each parameter is user-editable or not. You can also specify a tooltip that is displayed when a user mouses over the parameter name, to help explain its use.

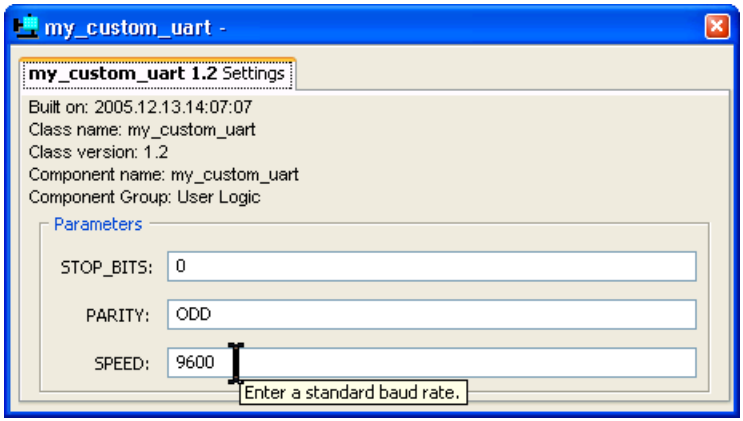
Tooltips can use basic HTML tags, such as `<b>` and `<p>` to format tooltip text. See Figure 5–7.

The following rules apply to HDL parameters exposed via the component GUI:

- Editable parameters cannot contain computed expressions.
- If a parameter *N* defines the width of a signal, the signal width must be of the form *N*-1..0.
- When a VHDL component is used in a Verilog system module, or vice versa, numeric parameters must be 32-bit decimal integers. Passing other numeric parameter types might fail.

Click **Preview the Wizard** at any time to see how the component GUI will look to an end user. Figure 5–7 shows an example of a component wizard preview.

Figure 5–7. Example Component Wizard Preview



Saving a Component

You can save the component by clicking **Finish** on any of the tabs, or by clicking **Save** on the File menu. The component editor saves the component files to the current Quartus® II project directory, in a subdirectory named the same as the component class name specified on the **Component Wizard** tab.

If you later edit the source code, you must update the component. Refer to section "Re-Editing a Component" on page 5–13.

When your component design is final, you can move the component files to a different location.

Re-Editing a Component

After you save a component and exit the component editor, you can re-edit a component at any time from the SOPC Builder GUI. To edit a component, right-click it in the list of available components, and choose **Edit Component**. You cannot edit components that were not created by the component editor, such as Altera®-provided components.

If you alter the source HDL, you need to use the component editor to incorporate the HDL changes into the SOPC Builder component. If you alter the signals on the top-level module, you need to reassign interface signals. If you change the name of a component while editing it, the component editor will save the component files to a new directory.

Existing SOPC Builder systems that use a previous version of the component require further action to reflect the component changes.

To update existing SOPC Builder systems with the new component changes, perform the following steps:

1. Delete any existing instances of the component in the SOPC Builder system, and add the component again.
2. Regenerate the system.

6. Archiving SOPC Builder Projects

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Introduction

The purpose of this chapter is to help you identify the files you need to include when archiving an SOPC Builder system module. With this information, you can archive:

- The SOPC Builder system module
- The associated Nios® II software project, if any
- The associated Nios II system library project, if any

You might need to archive your SOPC Builder system for one of the following reasons:

- To place an SOPC Builder design under source control
- To create a backup
- To bundle a design for transfer to another location

To use this information, you need to decide what source control or archiving tool to use, and you need to know how to use it. This chapter does not provide step-by-step instructions. It does cover the following information:

- How to find and identify the files that must be included in an archived SOPC Builder design.
- Which files must have write permission to allow the design to be generated and the software projects compiled.

Scope

This chapter provides information about archiving SOPC Builder system modules, including their Nios II software applications, if any. If your SOPC Builder system does not contain a Nios II processor, you can disregard information about Nios II software applications.

This chapter does not cover archiving SOPC Builder components, for two reasons:

- SOPC Builder components can be recovered, if necessary, from the original Quartus® II and Nios II installations.
- If your SOPC Builder system was developed with an earlier version of the Quartus II software and Nios II Embedded Development Suite (EDS), when you restore it for use with the current version, you normally use the current, installed components.

If your SOPC Builder system was developed with an earlier version of the Quartus II and Nios II development software, and you restore it for use with the current version, the regenerated system is functionally identical to the original system. However, there might be differences in details such as Quartus II timing, component implementation or HAL implementation. For details of version changes, refer to the release notes for the Quartus II software and the Nios II EDS.

To ensure that you can regenerate your exact original design, maintain a record of the tool and IP version(s) originally used to develop the design. Retain the original installation files or media in a safe place.

The archival process addressed by this chapter is different from Quartus II project archiving. A Quartus II project archive contains the complete Quartus II project, including the SOPC Builder module, but not including any Nios II software. Quartus II adds all HDL files to the archive, including HDL files generated by SOPC Builder, although these files are not strictly necessary.

This chapter is only concerned with archiving the SOPC Builder system, without the generated HDL files, but with all files needed to regenerate them and rebuild the Nios II software (if any).

For more details about archiving Quartus II projects, refer to volume 2 of the *Quartus II Handbook*.

Required Files

This section describes the files required by an SOPC Builder system and its associated Nios II software projects (if any). This is the minimum set of files needed to completely recompile a system, both the FPGA configuration image (.sof) and the executable software (.elf).

If you have Nios II software projects, archive them together with the SOPC Builder system on which they are based. You cannot rebuild a Nios II software project without its associated SOPC Builder system.

SOPC Builder Design Files

The files listed in Table 6–1 are located in the Quartus II project directory.

Table 6–1. Files Required for an SOPC Builder System (Part 1 of 2)

File description	File name	Write permission required? *(1)*
SOPC Builder system description	<sopc_builder_system>.ptf	Yes
All non-generated HDL source files *(2)*	e.g. top_level_schematic.bdf, customlogic.v	No

Table 6–1. Files Required for an SOPC Builder System (Part 2 of 2)		
File description	**File name**	**Write permission required? (1)**
Quartus II project file	<project_name>.qpf	No
Quartus II settings file	<project_name>.qsf	No

Notes to Table 6–1:
(1) For further information about write permissions, see "File Write Permissions" on page 6–4.
(2) Include all HDL source files not generated by SOPC Builder. This includes HDL source files you create or copy from elsewhere. To identify a file generated by SOPC Builder, open the file and look for the Altera® header:
`Legal Notice: (C)2006 Altera Corporation. All rights reserved.`

Nios II Application Software Project Files

The files listed in Table 6–2 are located in the Nios II software project directory.

For more information about Nios II software projects, refer to the *Nios II Software Developer's Handbook*.

Table 6–2. Files Required for a Nios II Application Software Project		
File description	**File name**	**Write permission required? (1)**
All source files	e.g. app.c, header.h, assembly.s, lookuptable.dat	No
Eclipse project file	.project	No
C/C++ Development Toolkit project file	.cdtproject	Yes
C/C++ Development Toolkit option file	.cdtbuild	No
Software configuration file	application.stf	No

Note to Table 6–1:
(1) For further information about write permissions, see "File Write Permissions" on page 6–4.

Nios II System Library Project

The files listed in Table 6–3 are located in the Nios II system library project directory.

For more information about Nios II system libraries, refer to the *Nios II Software Developer's Handbook*.

Table 6–3. Files Required for a Nios II System Library Project

File description	File name	Write permission required? *(1)*
Eclipse project file	.project	Yes
C/C++ Development Toolkit project file	.cdtproject	Yes
C/C++ Development Toolkit option file	.cdtbuild	No
System software configuration file	system.stf	Yes

Note for Table 6–3:
(1) For further information about write permissions, see "File Write Permissions" on page 6–4.

File Write Permissions

You must have write permission for certain files. The tools write to these files as part of the generation and compilation process. If the files are not writable, the toolchain fails.

Many source control tools mark local files read-only by default. In this case, you need to override this behavior. You do not need to check the files out of source control unless you are modifying the SOPC Builder design or Nios II software project.

7. Board Description Editor

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Introduction

This chapter introduces SOPC Builder board descriptions and provides complete reference for the board description editor.

Board Descriptions

SOPC Builder board descriptions contain detail about a printed circuit board (PCB) with a mounted Altera® FPGA. Board descriptions encapsulate low-level details about a board that can be reused by all users of the board. A PCB designer creates a board description so that other designers do not have to be board experts to create SOPC Builder systems for the target board. A board description enables designers to create an SOPC Builder design that works in hardware, even though they might not know how to read a board schematic or make Quartus® II pin assignments.

You can obtain board descriptions from several sources:

1. Altera provides ready-made board descriptions for Altera development boards. If you are targeting an Altera development board, use the board description provided with the board.

2. If you are designing an SOPC Builder system for an existing board, you might receive the board description from the board designer as part of the supporting files for the board.

3. If you are a board designer, you create a board description for your custom boards using the SOPC Builder board description editor.

The figures in this document are based on Altera's Nios Development Board, Cyclone™ II Edition as an example. The development tools for the Nios II processor include several ready-made board descriptions which you can use as reference. You can download an evaluation of the Nios II development tools free at **www.altera.com**.

Uses for Board Descriptions

Board descriptions serve three purposes:

- Provide FPGA pinout details to the SOPC Builder pin mapper.
- Define a system template for the target board. A system template is a ready-made SOPC Builder system for the board, which provides a starting place for future users of the board.
- Provide the Nios II flash programmer with details about flash memory on the board.

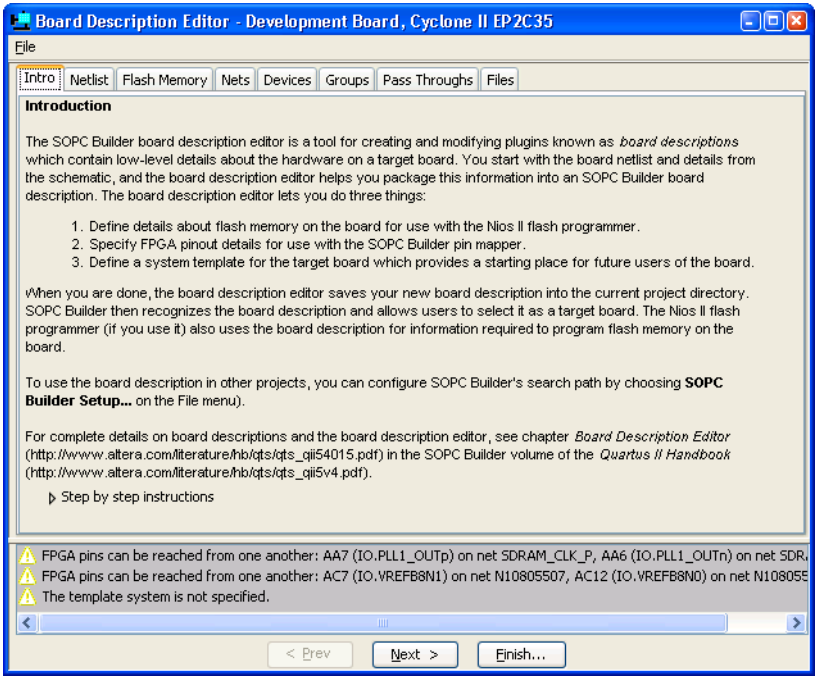
Not all board descriptions serve all three purposes. For example, a board description might contain only information for the Nios II flash programmer. Alternately, it might provide only pinout details and a system template.

For details on the pin mapper, see the chapter *Pin Mapper* in volume 4 of the *Quartus II Handbook*. For details on the Nios II flash programmer, see the *Nios II Flash Programmer User Guide*.

Board Description Editor

The board description editor is a feature of SOPC Builder that provides a graphical user interface (GUI) for creating board descriptions (Figure 7–1). Starting with the PCB netlist and details from the schematic, a PCB designer uses the board description editor to package this information into an SOPC Builder board description.

Figure 7–1. Board Description Editor



The board description editor GUI consists of several tabs and a message window. You do not have to use the tabs in order. The board description editor consists of the following tabs:

- Intro Tab
- Netlist Tab
- Flash Memory Tab
- Nets Tab
- Devices Tab
- Groups Tab
- Pass Throughs Tab
- Files Tab

Each tab in the board description editor GUI provides on-screen instructions that describe the usage of the tab. Click the triangle at the top-left of each tab to view the on-screen instructions.

The remainder of this document provides complete reference for the board description editor.

Creating a Board Description

The process of creating a board description is independent from creating an SOPC Builder system. You can build a new SOPC Builder system with no target board in mind, or you can create a new board description with no particular target system in mind. However, if you want to create an SOPC Builder targeting a particular board, you first must create a board description.

There are two possible flows for using the board description editor:

1. Pins Flow - Creates a board description for use with the SOPC Builder pin mapper.
2. Flash Flow - Creates a board description for use with the Nios II flash programmer.

Depending on how you intend to use the board description, you can use one or both of the flows. The two flows are independent of each other, and can be performed in either order.

Pins Flow

The purpose of the pins flow is to process the PBC netlist for use by the SOPC Builder pin mapper. The end result is a simplified model of the PCB. After finishing the pins flow, you can use your new board description as the target board in SOPC Builder, and you can use the pin mapper to map pins to the PCB.

For further information on the pin mapper, see chapter *Pin Mapper* in volume 4 of the *Quartus II Handbook*.

Steps for the Pins Flow

Below are the typical steps for the pins flow:

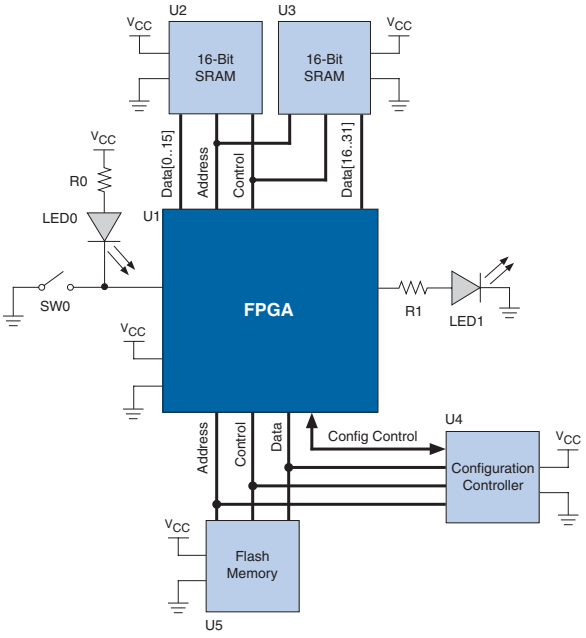
1. Use the **Netlist** tab to select the netlist for the target PCB and specify the target FPGA device.
2. Use the **Devices** and **Nets** tabs to filter devices and nets that are not used by the pin mapper, such as ground and power pins.
3. Use the **Devices** and **Pass Throughs** tabs to define pass-through devices, such as resistors and buffers.
4. Use the **Groups** tab to combine multiple devices into a logical grouping.
5. Use the **Files** tab to name the board description and specify the version.
6. Use the **Files** tab to specify a template system for the PCB.

Creating a PCB Model from the Netlist

The pins flow defines the connections between the FPGA and devices on the PCB. You start with the netlist for the PCB and incrementally add details about the board schematic until the board description editor has an appropriate model of the PCB for the pin mapper.

Figure 7–2 shows a board schematic representing a PCB netlist. Without further information, the pin mapper cannot infer how to connect components in an SOPC Builder system to the devices on the PCB.

Figure 7–2. Board Schematic

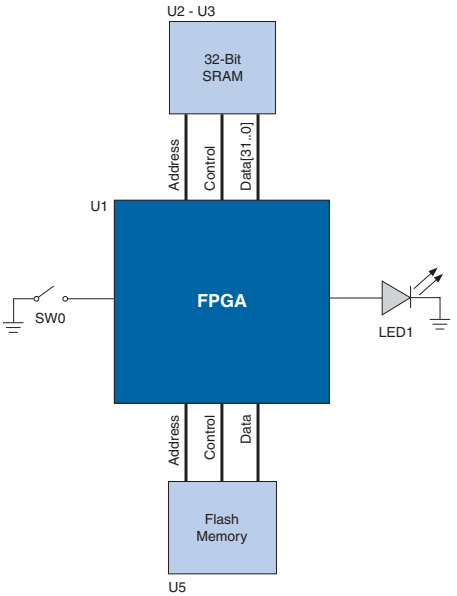


Using Figure 7–2 as an example, you must enter information into the board description editor to overcome the following issues:

- Devices are connected via common GND and VCC nets, but these nets do not carry I/O signals. You must filter these false paths between devices.
- The FPGA drives an LED (LED1), but the net for the FPGA I/O pin connects to a resistor (R1). You must define resistors to be pass-through devices, which are logically transparent devices that I/O signals pass through.
- The SRAM chips (U2, U3) are connected in parallel to be used as a single logical memory. You must define a device group to combine the SRAM chips into a single logical device.
- Certain devices with hard-wired functionality (LED0 and U4) have no relation to the function of the SOPC Builder system in the FPGA. If the SOPC Builder system never needs to connect to a certain device, you can filter the device so that the pin mapper cannot map pins to it.

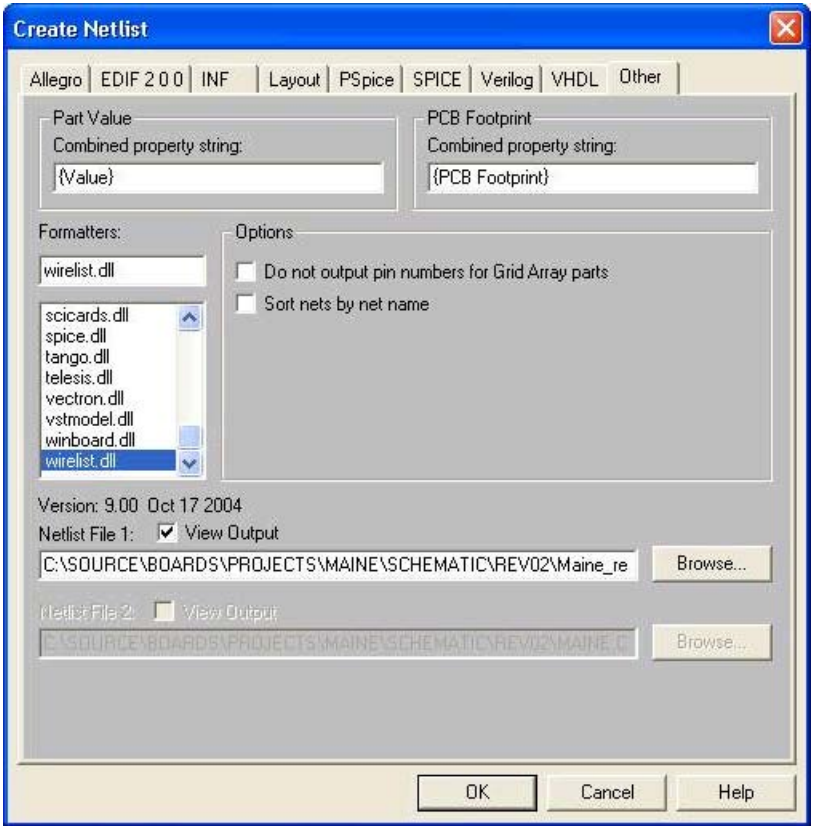
After you provide these details, the pin mapper can model the PCB appropriately, as shown in Figure 7–3.

Figure 7–3. Model of the PCB After Using the Board Description Editor



To begin the pins flow, you need a netlist of the PCB. You must export a netlist in the Wirelist format from your PCB design tool. Figure 7–4 shows an example of the settings in OrCad to create the Wirelist file.

Figure 7–4. Creating a Wirelist File in OrCad



The method you use to produce a Wirelist file differs if you use a different PCB layout tool or a different version of OrCad. If you use OrCad, do not use the Convert view on your symbols, because it causes OrCad to generate incorrect Wirelist files.

Flash Flow

The purpose of the flash flow is to define the flash memory devices on the PCB for use by the Nios II flash programmer. After finishing the flash flow, you can use the Nios II flash programmer to program the flash memory on the PCB.

For further information on using the Nios II flash programmer, see the *Nios II Flash Programmer User Guide*.

The flash flow declares the presence of flash memory on the PCB, and defines ranges in these devices for storing FPGA configuration data. Use the flash flow if SOPC Builder systems for this board will include any of the following components:

- Flash Memory (Common Flash Interface)
- EPCS Serial Flash Controller

Below are the typical steps for the flash flow:

1. Use the **Flash Memory** tab to declare the flash memory devices on the board.

2. Use the **Flash Memory** tab to specify regions of flash memory for FPGA configuration data.

Board Description Editor Output

This section describes the files output by the board description editor, and explains how to share board descriptions with other designers.

Board Description File Structure

Structurally, a board description is a set of files recognized by SOPC Builder and the Nios II IDE. Board descriptions use a file structure similar to SOPC Builder component directories. Based on the settings you make in the GUI, the board description editor outputs a properly formed directory, containing the following items:

- *class.ptf file* - Contains defining information about the board description which allows SOPC Builder and the Nios II IDE to recognize it.
- *netlist folder* - Contains the board netlist, if you provide one.
- *system folder* - Contains the system template for the board, if you provide one.

For details on SOPC Builder component file structure, see the chapter *Components* in volume 4 of the *Quartus II Handbook*.

Using Board Descriptions

After you create a board description, you can share it with other designers. To use a board description, you must store the files in a path where SOPC Builder searches for components. To configure SOPC Builder's search path, on the SOPC Builder File menu click **SOPC Builder Setup**.

Starting the Board Description Editor

You can start the board description editor from the SOPC Builder GUI by doing one of the following:

- On the File menu click **New Board Description** to create a new board description.
- On the File menu click **Edit Board Description** to edit the board description for the currently-selected target board.

When the board description editor starts, it displays the **Intro** tab.

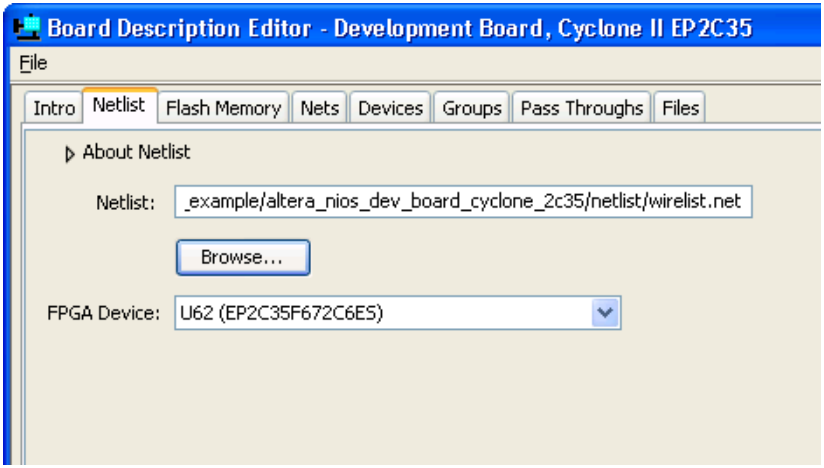
Intro Tab

The **Intro** tab provides a brief description of the board description editor. Figure 7–1 on page 7–3 shows an example of the **Intro** tab.

Netlist Tab

The **Netlist** tab lets you to choose the netlist for the PCB and the target FPGA. Figure 7–5 shows an example of the **Netlist** tab.

Figure 7–5. Netlist Tab



Use the **Netlist** box or the **Browse** button to choose the netlist. The board description editor immediately parses the file for device, pin, and net information.

The netlist must be in the Wirelist format.

After choosing the netlist, you must select which device is the target FPGA in the **Target FPGA** list.

If there are multiple FPGAs on the board that will contain SOPC Builder systems, then you must create multiple board descriptions. Each board description contains pin mapper-related information for one FPGA.

If the netlist contains device names matching the pattern EP1* or EP2* (the first letters of Altera device ordering codes), then the **Target FPGA** list limits your choices to only those devices. Otherwise, it presents all devices in the netlist.

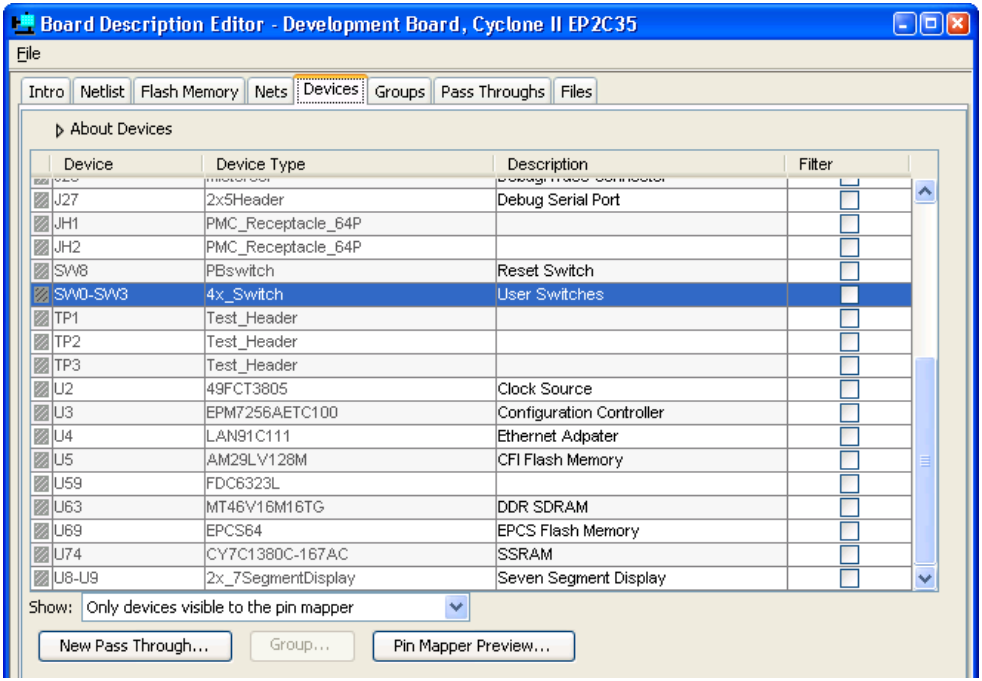
Based on the **Netlist** and **Target FPGA** settings, the board description editor determines possible connections between the FPGA pins and other devices on the PCB.

Devices Tab

The **Devices** tab lets you manage the list of devices that are visible to the pin mapper. Your goal is to manipulate the device list on the **Devices** tab until only devices appropriate for the pin mapper remain. The **Devices** tab is central to the pins flow. For more information, see section "Pins Flow" on page 7–4.

Figure 7–6 shows an example of the **Devices** tab.

Figure 7–6. Devices Tab



Device List

The board description editor populates the device list with the devices found in the netlist. The columns of the device list are described in Table 7–1.

Table 7–1. Device List Columns

Device	Device Type	Description	Filter
The reference designator for each device defined in the netlist file.	Additional device information contained in the netlist file. There is no standard data type or format for **Device Type**. This data is read-only.	Text you type in the **Description** cell appears in the pin mapper, so that future users of the pin mapper easily understand what each device is.	Turning on **Filter** for a device excludes it from the list of devices visible to the pin mapper.

Use the **Show** list to switch between the following modes:

- **All devices** - Lists every device in the netlist.
- **Only devices visible to the pin mapper** - Lists only devices that will be available to the pin mapper after you finish the board description.

All devices listed in the **Only devices visible to the pin mapper** mode will be available as a target device in the pin mapper later.

Filtered Nets, Pass Throughs & Device Groups

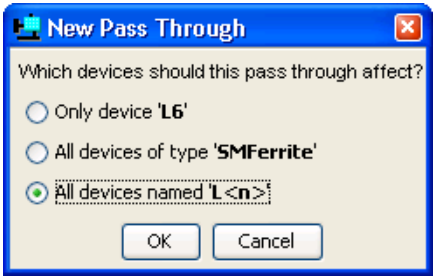
Filtered nets, pass throughs, and device groups modify the way the board description editor displays devices in the device list. You can create new pass throughs and device groups with the **Devices** tab.

The device list changes dynamically based on the settings you make on the **Nets**, **Pass Throughs**, and **Groups** tabs. For further information see the respective sections "Nets Tab", "Pass Throughs Tab", and "Groups Tab".

Creating Pass Throughs

To specify a device as a pass-through device, select it in the device list and click **New Pass Through**. The **New Pass Through** dialog appears, allowing you to choose what type of pass through to create. Figures 7–7 shows an example of creating a pass through for an inductor.

Figure 7–7. Creating a New Pass Through



There are three types of pass throughs:

- *Single device* – Applies only to one specific device, such as a single inductor with reference designator L6.
- *Device type* – Applies to all devices with the same **Device Type**, such as all inductors with **Device Type** "SMFerrite".
- *Reference designator pattern* – Applies to all devices with numbered reference designators sharing a common prefix, such as L*n*, where *n* is any sequence of digits.

After creating a new pass through, you must go to the **Pass Throughs** tab to define the pass through properties.

Creating Device Groups

To specify that multiple devices form a device group, select multiple devices in the device list and click **Group**. To select multiple devices, press and hold the Control key while selecting devices in the list.

After creating a new device group, you must go to the **Groups** tab to name the pins on the device group.

Filtering False Target Devices

Some devices in the netlist file are meaningless to the pin mapper. On the **Devices** tab, you can turn on **Filter** for false target devices to make them invisible to the pin mapper.

Filter the following types of false target devices:

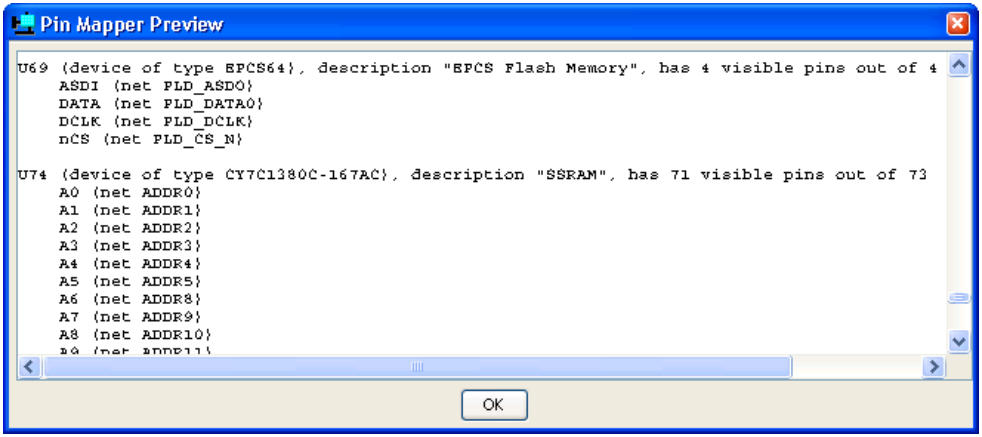
- *Damping capacitors* - Some FPGA pins have a capacitor connected to ground to improve signal integrity. These capacitors are not the intended target for any I/O signal. The board description editor automatically filters any device with reference designator of the form C*n*, where *n* is any sequence of digits.
- *Secondary target devices* - If an FPGA pin connects to two (or more) target devices, you might want to filter the device(s) that do not serve the primary function of the pin. For example, in Figure 7–2 on page 7–6 switch SW0 and LED0 connect to the same FPGA pin. Closing SW0 pulls the FPGA pin low and turns on LED0. In this case, SW0 is the primary function for the FPGA pin, and eliminating LED0 from the pin mapper is a good idea.
- *False paths back to the FPGA* - There might be devices that create false signal paths leading back to the FPGA. For example, termination resistors between differential-pair nets create a loop between FPGA pins that is not a logical signal path.
- *No-stuff devices* - Some devices in the netlist are not stuffed on the PCB during manufacturing. You can filter such devices to disallow pin mapper users from connecting FPGA signals to a target device that does not exist on the board.

If you turn on **Filter** when **Show** is set to **Only devices visible to the pin mapper**, the device immediately disappears from the device list. To see all filtered and unfiltered devices, select **All devices** in the **Show** list.

Previewing Pins Visible to the Pin Mapper

You can click **Pin Mapper Preview** to open the Pin Mapper Preview window which displays the complete list of devices and pins visible to the pin mapper. You are finished with the pins flow when the Pin Mapper Preview window contains exactly the devices and pins you wish to expose to the pin mapper. Figure 7–8 shows an example of the preview listing for a device.

Figure 7–8. Pin Mapper Preview Window



For each device with pins visible to the pin mapper, the preview lists the following:

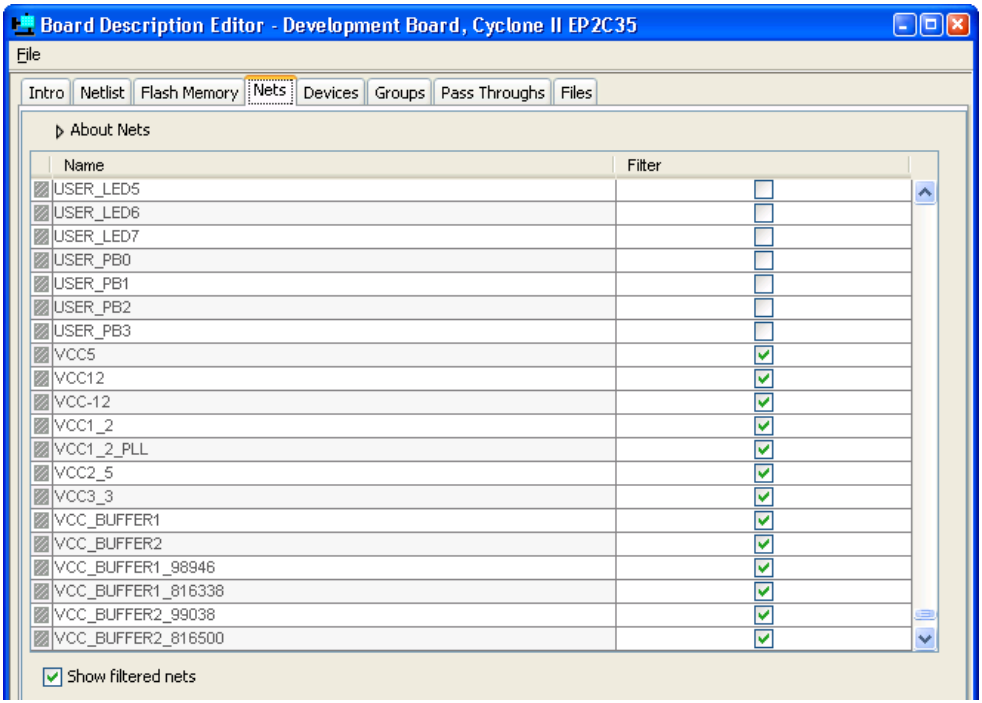
- Reference designator, device type, and description, as shown on the **Devices** tab.
- Total number of pins connected to unfiltered nets, and the number of pins visible to the pin mapper. These numbers provide a useful sanity check. For example, imagine an eight-pin device with one power pin and one ground pin. If power and ground nets are filtered, the total number of unfiltered pins is six. Of the six total pins, perhaps 4 connect to the FPGA.
- The name of each pin visible to the pin mapper, and its corresponding FPGA pin net name.

Nets Tab

The **Nets** tab lets you manage the list of nets that the board description editor considers as signal paths from device-to-device. Typically, multiple devices connect to common power and ground nets, even though not all of these devices have I/O interconnections. Your goal is to filter the netlist to exclude nets that do not carry I/O signals, such as power and ground nets, so that the pin mapper does not detect false signal paths between devices.

Turn on **Filter** for non-I/O nets. Figure 7–9 shows an example with all power supply nets filtered, which prevents the pin mapper from including these nets as signal paths between devices.

Figure 7–9. Nets Tab



The board description editor automatically filters nets matching the pattern GND* or VCC*.

Changes you make on this tab affect the device list on the **Devices** tab. If you filter all nets connecting a device to the FPGA, the **Devices** tab ignores the device.

Pass Throughs Tab

A pass through is a logically transparent device that exists along a signal path but does not alter the signal's logic level, such as a resistor. The **Pass Throughs** tab displays all pass throughs created with the **Devices** tab. After you create a new pass through with the **Devices** tab, you use the **Pass Throughs** tab to define the pin-to-pin paths that are logically transparent. For information on creating pass throughs, see section "Creating Pass Throughs" on page 7–13.

Some FPGA I/O pins drive signals through a pass-through device. Pass throughs are not the signal's final destination. For example, in Figure 7–2 on page 7–6 an FPGA pin connects to R1, but the true signal destination is LED1. You define pass throughs to allow the board description editor to detect the true signal destination beyond the pass through device.

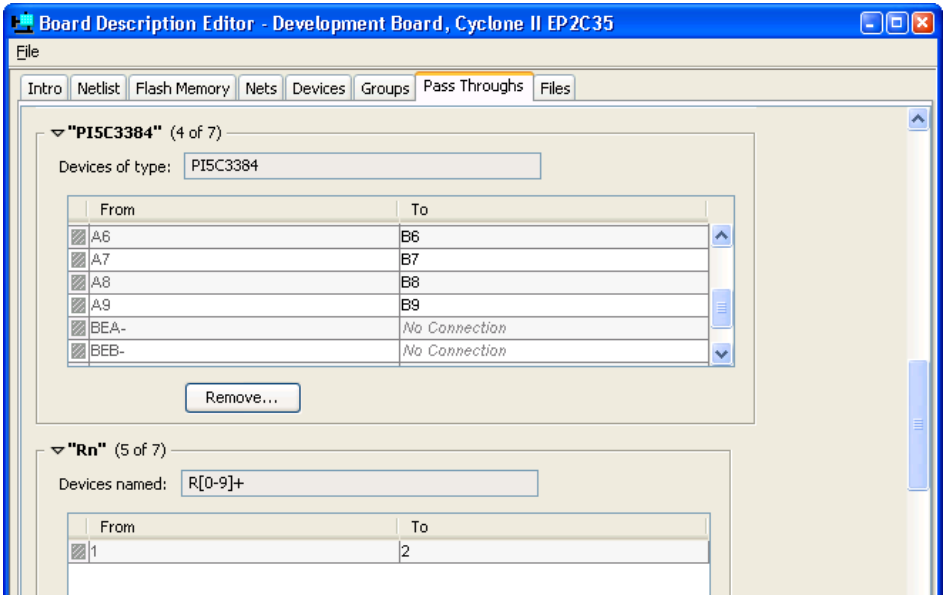
You might have to create pass throughs for the following types of logically transparent devices:

- Resistors in signal paths to limit current flow
- Buffers, level shifters, and power transistors
- Inductors in signal path to improve signal integrity

Figure 7–10 shows an example of the **Pass Throughs** tab with the following pass throughs:

- *For device type PI5C3384* – This pass through affects voltage level-shifters labeled "PI5C3384". Signals pass transparently from pin A*n* to B*n*, where *n* is any digit.
- *For reference designators matching pattern Rn* – This pass through affects all resistors with reference designator R*n*, where *n* is any sequence of digits. Signals pass transparently through the two pins on these resistors.

Figure 7–10. Pass Throughs Tab



For each entry on the **Pass Throughs** tab, you use the table to specify transparent pin-to-pin paths through the device. For each pin in the **From** list, select an appropriate **To** setting. If a pin does not have a logically transparent path through the device, select **No Connection**. **From** and **To** settings only imply transparent paths through the device; they do not imply signal direction.

Changes you make on this tab affect the device list on the **Devices** tab. After you define a pass through for a particular device, the **Devices** tab no longer displays the device. Instead, it displays the device(s) connected to the other side of the pass-through device.

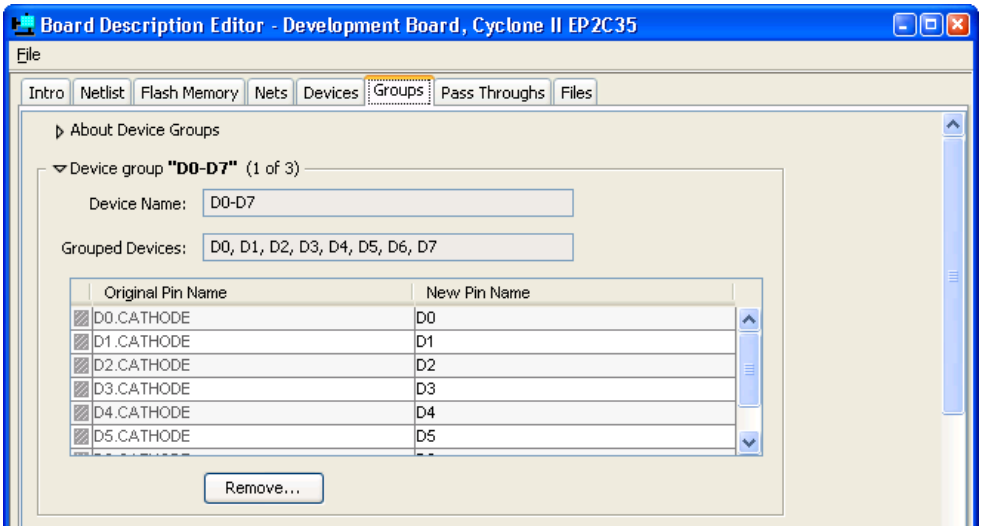
Groups Tab

A device group is comprised of multiple devices that the pin mapper treats as a single device. The **Groups** tab displays all device groups created with the **Devices** tab. After you create a new group with the **Devices** tab, you use the **Groups** tab to name the pins on the group. For information on creating device groups, see section "Creating Device Groups" on page 7–14.

If the PCB is designed for multiple devices to connect to a single SOPC Builder component in the FPGA, creating a device group tends to make the pin mapper easier to use for that component. For example, in Figure 7–2 on page 7–6 grouping the two 16-bit SRAM devices creates a 32-bit SRAM device group.

Figure 7–11 shows the **Groups** tab for the case of eight individual LEDs (D0 to D7) combined to form an 8-bit bank of LEDs.

Figure 7–11. Groups Tab



For each device group on the **Groups** tab, you use the table to specify a new pin name for each pin that existed on the individual devices. For each pin listed in the **Original Pin Name** list, type a descriptive name in **New Pin Name**. This name appears as the pin name in the pin mapper.

The board description editor automatically fills **New Pin Name** cells with default pin names. However, you must manually inspect all new pin names to verify appropriateness.

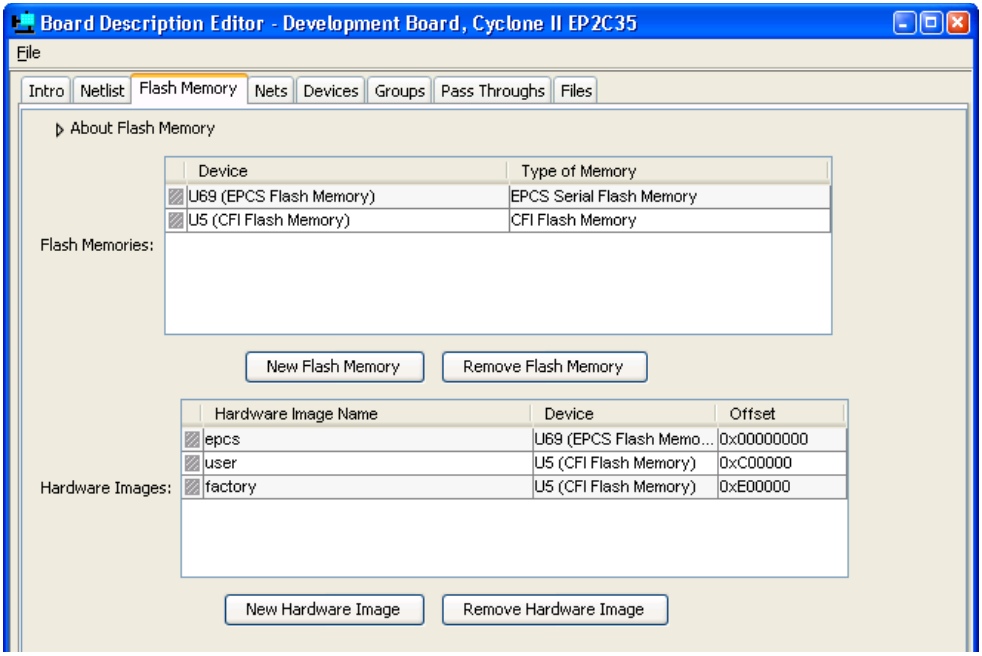
Flash Memory Tab

The **Flash Memory** tab lets you specify details about flash memory on the PCB. This information is used by the Nios II flash programmer. If you do not intend to use the Nios II flash programmer with this board, or if the board does not contain flash memory, then you can ignore this tab. The **Flash Memory** tab is central to the flash flow. For more information, see section "Flash Flow" on page 7–8.

Figure 7–12 shows an example of the **Flash Memory** tab for a PCB with the following flash memories:

- One Altera EPCS serial configuration device containing one hardware image, which is the maximum number of images for an EPCS device.
- One CFI flash memory containing two hardware images. An external configuration controller chip recognizes hardware images at offsets `0xC00000` and `0xE00000` in the flash memory.

Figure 7–12. Flash Memory Tab



You must add a device entry for each flash memory on the PCB that connects to the FPGA. Click **New Flash Memory** to add devices to the **Flash Memories** list. Select **Type of Memory** for each entry in the **Flash Memories** list.

Each flash memory can contain one or more hardware images, which are address ranges allocated for FPGA configuration data. Define all hardware images stored in flash memory on the PCB.

Click **New Hardware Image** to add an entry to the **Hardware Images** list. For each entry, type a descriptive name into the **Hardware Image Name** box. Use the **Device** list to select which flash memory contains the image. Type the offset where the hardware image data starts into the **Offset** cell.

The first location in the flash memory is offset `0x0000`.

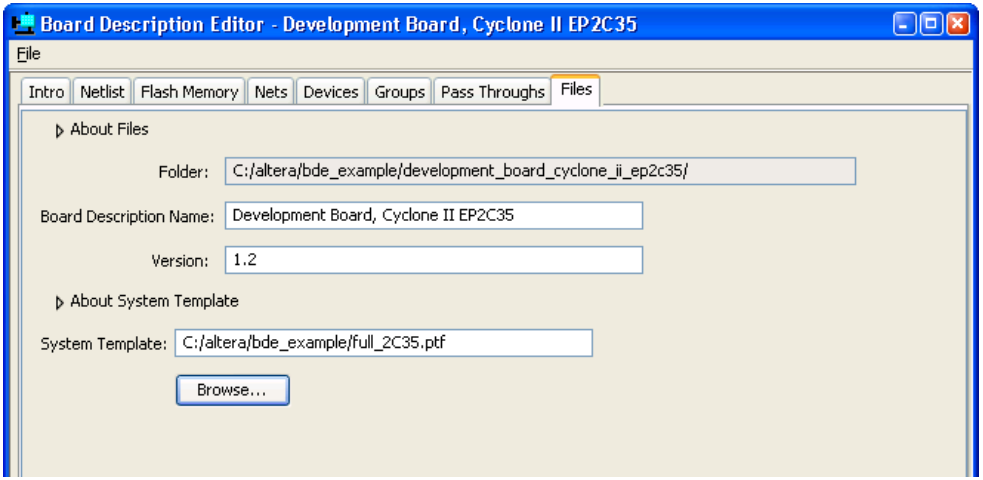
The correct number of hardware images and the offset for each image depend on the following:

- The FPGA configuration controller on the board. In most cases, the configuration controller expects configuration data to exist at specific offsets in flash memory.
- The size of the hardware image data for the target FPGA. The size of the hardware image determines how closely the offsets can be spaced.

Files Tab

The **Files** tab lets you give your new board description a name and version, and specify a system template. Figure 7–13 shows an example of the **Files** tab.

Figure 7–13. Files Tab



Board Description Name and Version

The name you type in the **Board Description Name** box is the name that appears in the SOPC Builder target board list. This name can include spaces or other special characters. The **Folder** box displays the path where the board description editor saves the board description files. **Board Description Name** determines the **Folder** name. If you are creating a new board description, the editor creates a new folder under the Quartus II project path. If you are editing an existing board description, the editor saves the files back to the same folder, unless you change **Board Description Name**.

Similar to the version for SOPC Builder components, **Version** indicates to SOPC Builder which board description is newer, in the event that more than one of the same kind of board description is detected. SOPC Builder displays only the board description with the highest version in the target board list.

System Template

A system template is a ready-made SOPC Builder system for the board, which provides a starting place for future users of the board. The system template should include:

- An SOPC Builder component corresponding to each device connected to the FPGA.
- Complete pin mappings that connect each component to its target device on the PCB.

To specify the system template, type the path to an SOPC Builder system in the **System Template** box, or click **Browse**.

Do not assign a system template the first time you save your board description. First, use the pin mapper with the new board description to map pins for the system template.

To assign a system template correctly, perform the following steps:

1. In SOPC Builder, open or create the SOPC Builder system you plan to use as the system template.
2. Select the new board description as the target board for the system.
3. Use the pin mapper to assign appropriate pin locations for all signals in the system.

4. Return to the **Files** tab in the board description editor, and select the SOPC Builder system with complete pin mappings as the system template.

5. Re-save the board description.

Saving & Exiting the Board Description Editor

You can save the board description by clicking **Finish** on any of the tabs, or by clicking **Save** on the File menu. Exiting the board description editor automatically prompts you to save the files. The board description editor saves files to a board description folder, creating a new folder if necessary.

If you edit and re-save a board description, and you have existing SOPC Builder systems based on a previous version, you must update those systems to recognize the updates to the board description.

To update an existing SOPC Builder system with board description changes, perform the following steps:

1. Open the system with SOPC Builder.

2. Set the target board to **Unspecified Board**.

3. Set the target board back to the updated board description.

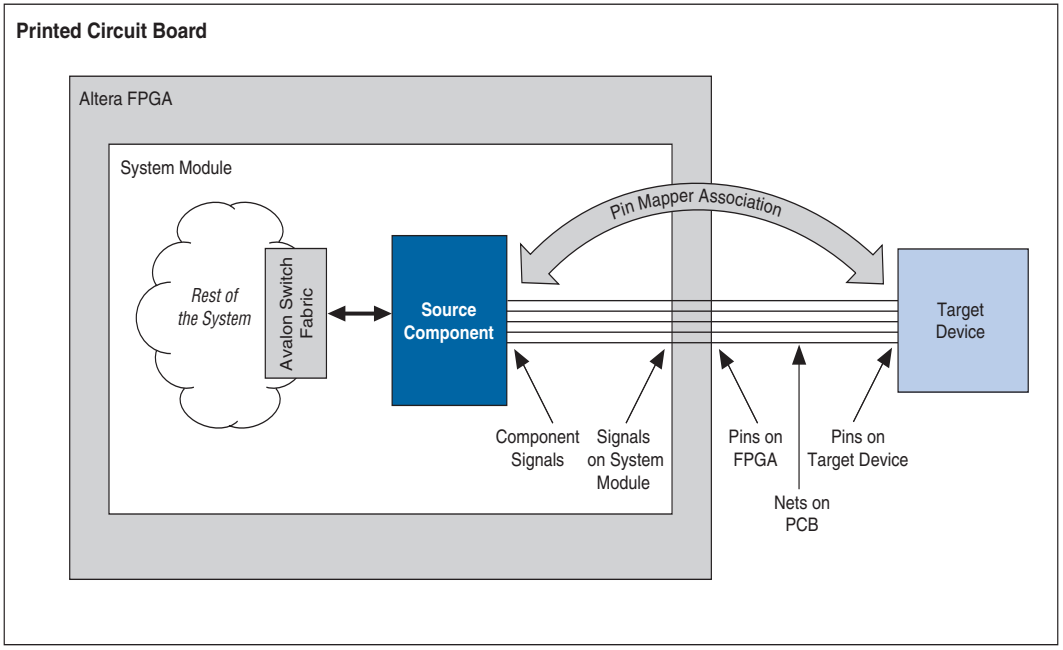
8. Pin Mapper

QII54016-6.0.0

Introduction

The SOPC Builder pin mapper simplifies the process of assigning FPGA pins, allowing you to make device-to-device connections on the printed circuit board (PCB) based on pin function, rather than pin numbers. The pin mapper maps logical connections between SOPC Builder system components and devices mounted on the PCB, as shown in Figures 8–1.

Figure 8–1. Pin Mapper Maps Logical Connections from SOPC Builder Components to Devices on the PCB



The pin mapper accelerates your design time by abstracting details that are tedious and prone to human error, such as:

- Signal names on the SOPC Builder system module
- Pin numbers on the FPGA
- Net names on the PCB

The pin mapper assumes that you know the board you are targeting and that you have an SOPC Builder board description for the target board. Using the board description and information about the components in your SOPC Builder system, the pin mapper GUI lets you map connections from components in the system to device pins on the PCB. To map pins correctly, you must know the function of signals on the source component(s) and pins on the target device(s).

For more information on SOPC Builder board descriptions, refer to the *Board Description Editor* chapter in volume 4 of the *Quartus II Handbook*.

The pin mapper provides a level of assurance that you have accounted for the pin assignments required for a target board. In general, if the Quartus® II project pin assignments do not match the specific board you are using, your design will not function and you could damage the board. The pin mapper helps ensure that you take care of pin assignments for signals on the system module before downloading it to a board.

Design Flow

This section describes the design flow for using the pin mapper, and how the pin mapper affects the Quartus II project.

The following is a typical design flow using the pin mapper:

1. Create an SOPC Builder system targeting a specific board.
2. Instantiate and configure system components on the **System Contents** tab in SOPC Builder.
3. Use the pin mapper to map component signals to devices on the PCB.
4. Generate the system in SOPC Builder. This step automatically applies the pin assignments to the Quartus II project.

When targeting a specific board, you cannot generate the system until you completely map all signals. Alternately, you can leave all signals unmapped, in which case you must assign all pins using the Quartus II Assignment Editor.

5. Integrate the system module into the top-level Quartus II project.
6. Compile the Quartus II project to fit the design in the FPGA using the pin assignments.

The pin mapper is an optional step in the SOPC Builder system design flow. If you choose to use the pin mapper, then SOPC Builder does not allow you to generate the system until you have completely mapped all signals on the system module.

Applying Pin Assignments to the Quartus II Project

During system generation SOPC Builder generates a Tcl script named **<***system module name***>_setup_quartus.tcl** which contains Quartus II commands to assign pin locations for your system module. At the end of system generation, SOPC Builder executes this script to apply the pin assignments to the Quartus II project.

If you edit the SOPC Builder system later, you can alter the pin mapper settings. However, you must regenerate the system in SOPC Builder to update the Tcl script and apply your pin assignments to the Quartus II project.

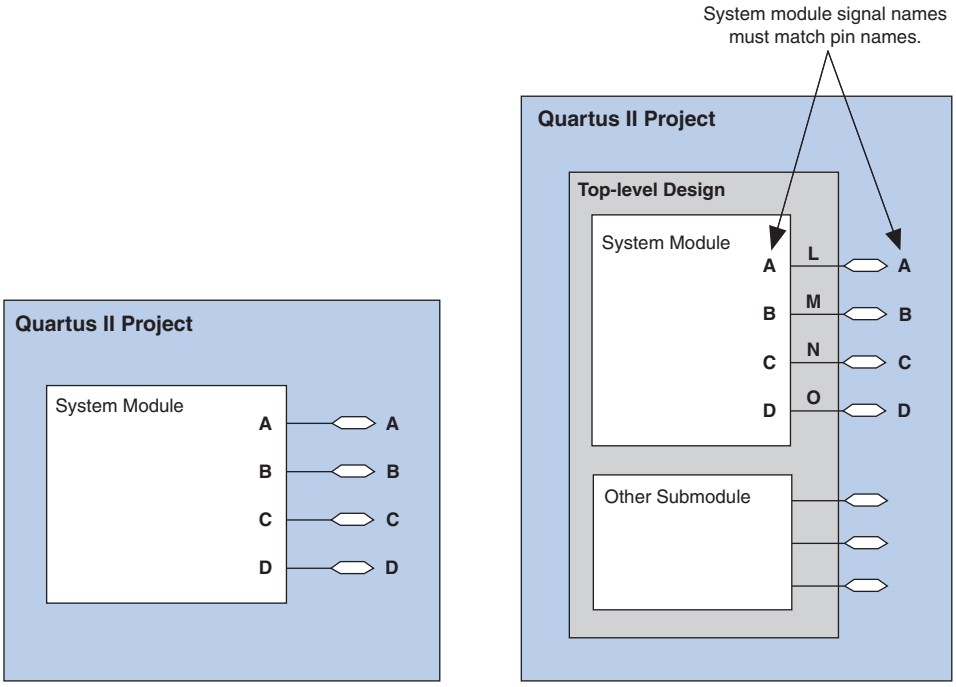
Pin Name Requirements

The **<***system module name***>_setup_quartus.tcl** script makes assignments for pin names matching the names of signals on the system module. Therefore, you must use specific names for pins at the top level of the Quartus II project. For the pin mappings to work, you must name the FPGA pins the same as the signal names on the system module.

For example, imagine a system module with an input vector named `in_port_to_the_button_pio[3..0]`, and suppose that you use the pin mapper to map these signals to four push-button switches on the PCB. The input pins at the top level of the Quartus II project must also be named `in_port_to_the_button_pio[3..0]` for the pin assignments to work.

It does not matter at what level of hierarchy you instantiate the system module in the overall Quartus II project. You can use the system module as the top-level design entity, or you can instantiate the system module inside a lower-level design entity, as shown in Figure 8–2. As long as the top-level pin names match the names of the signals on the system module, the pin mappings will be effective.

Figure 8–2. Pin Mapper and Quartus II Project Hierarchy

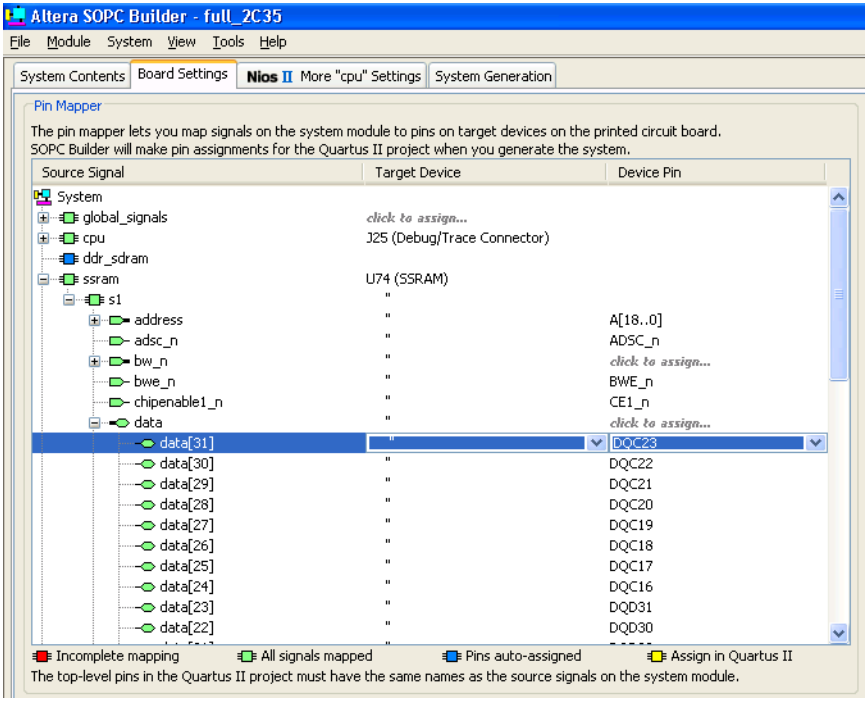


Pin Mapper GUI

The pin mapper GUI is located on the **Board Settings** tab in SOPC Builder, as shown in Figure 8–3.

SOPC Builder displays the **Board Settings** tab only if you specify a target board on the **System Contents** tab. The **Board Settings** tab does not appear when a target board is unspecified, or if the target board description was created prior to version 5.1 of the Quartus II software.

Figure 8–3. Pin Mapper GUI on the Board Settings Tab



The pin mapper interface is a table with three columns. Table 8–1 describes the meaning of each column.

Table 8–1. Columns in the Pin Mapper GUI

Source Signals	Target Device	Target Pin
This column contains the names of signals on the components in the system module. This column groups signals to make the list more manageable.	This column contains the names of the devices on the PCB that connect to the FPGA.	This column contains the names of individual pins on the target device. This column shows only the pins available on the selected target device.

Source Signals Column

You can easily browse through source signals on the system module by expanding and collapsing groups in the **Source Signals** column. The signals are grouped together in the following hierarchical levels:

1. *Component level* – Signals for each component are grouped together. In Figure 8–3 on page 8–5, the **ssram** group contains all signals associated with this instance of the component. Component instances with no external signals do not appear in the pin mapper.

2. *Avalon® port level* – Signals that are associated to a particular Avalon port are grouped together. In Figure 8–3 on page 8–5, the **ssram/s1** group contains all signals associated with slave port **s1**. Some signals are not associated with a particular Avalon port and therefore appear outside of a port-level grouping.

3. *Signal vector level* – Vectored signals are grouped together by a common name. In Figure 8–3 on page 8–5, the **ssram/s1/data** group represents a vector of 32 related data signals.

4. *Individual signal level* – The lowest level of hierarchy is the individual signal level. Each individual signal can connect to one FPGA pin, which connects to one or more pins on a target device. In Figure 8–1 on page 8–1, the **ssram/s1/data/data[31]** row represents an individual signal on the system module.

Target Device Column

The **Target Device** column lets you map signals to a target device. You can easily map individual signals, signal vectors, or an entire component to a target device. For example, to map all signals on a component to a specific device, you can highlight a component-level row and specify the device in the **Target Device** column. Alternately, you can individually map each signal to a particular device.

In Figure 8–3 on page 8–5, the component instance **ssram** is mapped to device **U74**. The **Target Device** column shows that lower levels of hierarchy inherit their device settings from the component level.

Depending on the contents of the board description, the pin mapper might have enough information about certain devices on the PCB to automatically map component signals to appropriate pins on the device. In this case, when you target a whole component to a device, the pin mapper automatically maps signals to pins on the target device.

Target Pin Column

The **Target Pin** column lets you map a signal to a specific pin on a device on the PCB. To specify a target pin for a signal, you first must specify **Target Device**. The **Target Pin** column displays only the pins on the target device.

For example, Figure 8–3 on page 8–5 shows that signal `data[31]` on the component instance **ssram** maps to pin DQC23 on device U74.

Vector Signals

You can map a vector signal to a group of pins by clicking the **Target Pin** cell for a vector signal. For a vector signal the **Target Pin** dropdown list displays all groupings of pins on the target device that could logically map to the vector signal.

Differential Signals

To map a signal to pins using a differential I/O standard such as LVDS, you need to map the positive pin only. The Quartus II software will automatically assign the negative pin.

You must set the I/O standard using the Assignment Editor in the Quartus II software.

Signals with Multiple Destinations

Some FPGA I/O pin nets connect to multiple devices on the PCB. As a result, a signal routed to that I/O pin connects to multiple devices. In this case, using the pin mapper to map a signal to any one of the target device pins is equivalent to mapping the signal to all of connected target pins.

Assign in Quartus II

The **Target Pin** column provides the **Assign in Quartus II** setting to make the pin mapper ignore a particular pin. When you set a signal to **Assign in Quartus II**, the pin mapper does not create a Quartus II pin assignment for that signal.

The **Assign in Quartus II** setting is useful for the following cases:

- You want to manually assign the pin using the Quartus II Assignment Editor.
- If a particular signal connects to logic inside the FPGA rather than to I/O pins, the signal does not need a pin assignment.

Pin Mappings Status

The pin mapper displays the current status of signal mappings. When you place the mouse over a row in the pin mapper, a tooltip displays the FPGA pin assignment that will result from the current pin mapping.

In addition, the colors of symbols in the **Source Signals** column change to indicate status. Table 8–2 on page 8–8 shows the color coding for signal mapping status.

Table 8–2. Color Coding for Signal Status

Color	Meaning	Example Cases
Red	Incomplete mapping	An individual signal is not yet mapped, or a group of signals contains one or more signals that are not yet mapped
Green	All signals mapped	The element is mapped, or the element is set to **Assign in Quartus II**.
Blue	Pins auto-assigned – This component provides its own pin assignments which cannot be overridden by the pin mapper.	The Altera DDR/DDR2 SDRAM MegaCore provides specific pin assignments which must be used with the core.
Yellow	Assign in the Quartus II software – The pin mapper cannot assign pins for this component, and therefore you must manually assign pins using the Quartus II Assignment Editor.	The pin mapper does not support components created before Quartus II version 5.0.

Section II. Building Systems with SOPC Builder

Section II of this volume provides instructions on how to use SOPC Builder to achieve specific goals. Chapters in this section serve to answer the question, "How do I use SOPC Builder?" Many chapters in this handbook provide design examples that you can download free from **www.altera.com**. Design file hyperlinks are located with individual chapters linked from the Altera web site.

This section includes the following chapters:

- Chapter 9, Building Memory Subsystems Using SOPC Builder
- Chapter 10, Developing Components for SOPC Builder
- Chapter 11, Building Systems with Multiple Clock Domains

Revision History

The following table shows the revision history for Chapters 9 through 11.

Chapter(s)	Date / Version	Changes Made
9	May 2006, v6.0.0	Chapter 9 was previously chapter 8. No change to content.
	October 2005, v5.1.0	Chapter 8 was previously chapter 6. No change to content.
	May 2005, v5.0.0	Initial release.
10	May 2006, v6.0.0	Chapter 10 was previously chapter 9. No change to content.
	October, 2005 v5.1.0	Chapter 9 was previously chapter 7. No change to content.
	August 2005, v5.0.1	Corrected Table 7-5.
	May 2005, v5.0.0	No change from previous release.
	February 2005, v1.0	Initial release.
11	May 2006, v6.0.0	Chapter 11 was previously chapter 10. No change to content.
	October 2005, v5.1.0	Chapter 10 was previously chapter 8. No change to content.
	May 2005, v5.0.0	No change from previous release.
	February 2005, v1.0	Initial release.

9. Building Memory Subsystems Using SOPC Builder

QII54006-6.0.0

Introduction

Most systems generated with SOPC Builder require memory. For example, embedded processor systems require memory for software code, while digital signal processing (DSP) systems require memory for data buffers. Many systems use multiple types of memories. For example, a processor-based DSP system can use off-chip SDRAM to store software code, and on-chip RAM for fast access to data buffers. You can use SOPC Builder to integrate almost any type of memory into your system.

This chapter describes the process for building a memory subsystem as part of a larger system created with SOPC Builder. This chapter focuses on the kinds of memory most commonly used in SOPC Builder systems:

- On-chip RAM and ROM
- EPCS serial configuration devices
- SDRAM
- Off-chip RAM and ROM, such as SRAM and common flash interface (CFI) flash memory

This chapter assumes that you are familiar with the following:

- Creating FPGA designs and making pin assignments with the Quartus® II software. For details, see the *Introduction to Quartus II Manual*.
- Building simple systems with SOPC Builder. For details, see the *Introduction to SOPC Builder* and *Tour of the SOPC Builder User Interface chapters* in volume 4 of the *Quartus II Handbook*.
- SOPC Builder components. For details, see the *SOPC Builder Components* chapter in volume 4 of the *Quartus II Handbook*.
- Basic concepts of the Avalon® interface. You do not need extensive knowledge of the Avalon interface, such as transfer types or signal timing. However, to create your own custom memory subsystem with external memories, you need to understand the Avalon interface. For details, see the *Avalon Switch Fabric* chapter in volume 4 of the *Quartus II Handbook* and the *Avalon Interface Specification*.

Example Design

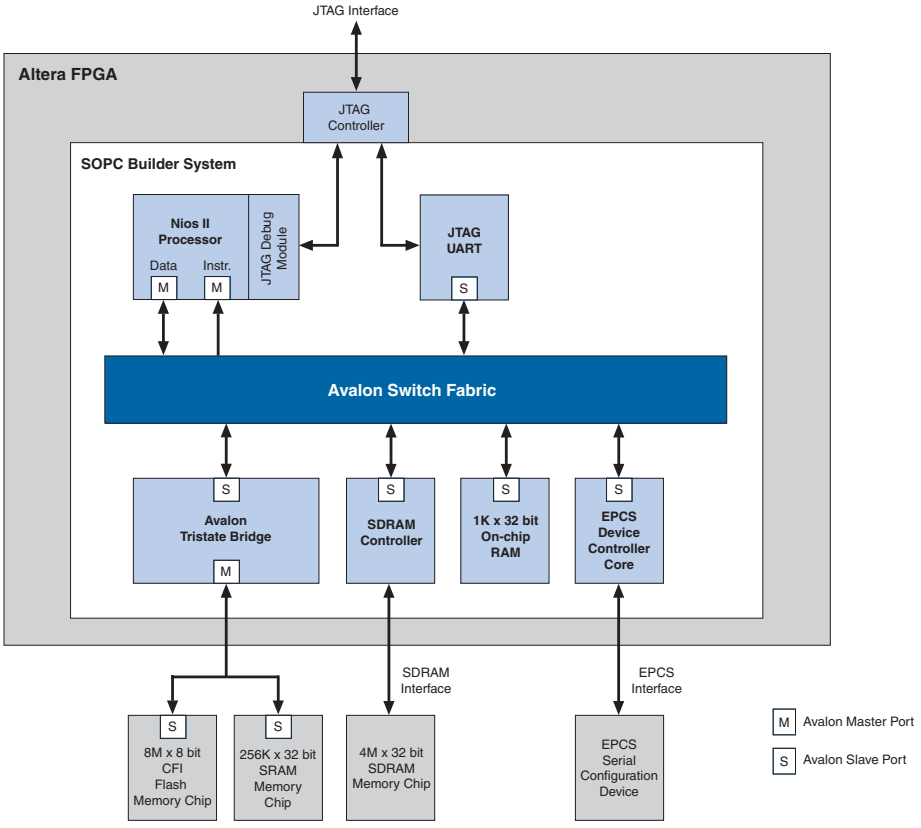
This chapter demonstrates the process for building a system that contains one of each type memory as shown in Figure 9–1. Each section of the chapter builds on previous sections, culminating in a complete system.

By following the example design through this chapter, you will learn how to create a complete memory subsystem for your own custom system. The memory components in the example design are independent. For a custom system, you can instantiate exactly the memories you need, and skip the memories you don't need. Furthermore, you can create multiple instantiations of the same type of memory, limited only by on-chip memory resources or FPGA pins to interface with off-chip memory devices.

Example Design Structure

Figure 9–1 shows a block diagram of the example system.

Figure 9–1. Example Design Block Diagram



In Figure 9–1, all blocks shown below the Avalon switch fabric comprise the memory subsystem. For demonstration purposes, this system uses a Nios® II processor core to master the memory devices, and a JTAG UART core to communicate with the processor. However, the memory subsystem could be connected to any master component, either on-chip or off-chip.

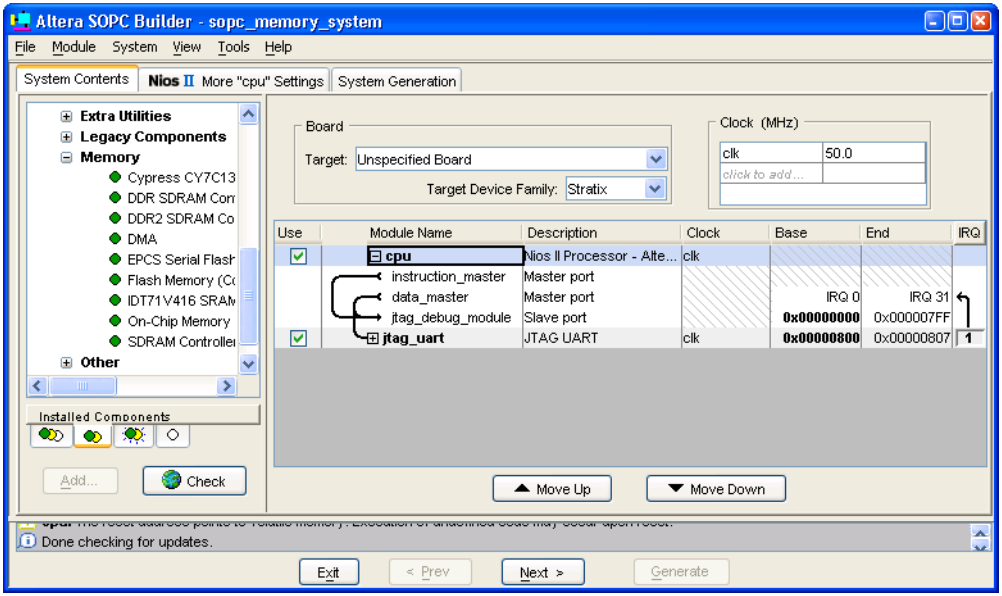
Example Design Starting Point

The following elements comprise the example design:

- A Quartus II project named **quartus2_project**.A block diagram file (BDF) named **toplevel_design**. **toplevel_design** is the top-level design file for **quartus2_project**. **toplevel_design** instantiates the SOPC Builder system module, as well as other pins and modules required to complete the design.
- An SOPC Builder system named **sopc_memory_system**. **sopc_memory_system** is a subdesign of **toplevel_design**. **sopc_memory_system** instantiates the memory components and other SOPC Builder components required for a functioning system module.

The starting point for this chapter assumes that **quartus2_project** already exists, that **sopc_memory_system** has been started in SOPC Builder, and that the Nios II core and the JTAG UART core are already instantiated. This example design uses the default settings for the Nios II/s core and the JTAG UART core; these settings do not affect the rest of the memory subsystem. Figure 9–2 shows the starting point in SOPC Builder.

Figure 9–2. Starting Point for the Example Design



All sections in this chapter build on this starting point.

Hardware & Software Requirements

To build a memory subsystem similar to the example design in this chapter, you need the following:

- Quartus II Software version 5.0 or higher –Both Quartus II Web Edition and the fully licensed version support this design flow.
- Nios II Embedded Design Suite (EDS) version 5.0 or higher –Both the evaluation edition and the fully licensed version support this design flow. The Nios II EDS provides the SOPC Builder memory components described in this chapter. It also provides several complete example designs which demonstrate a variety of memory components instantiated in working systems.

The Quartus II Web Edition software and the Nios II EDS, Evaluation Edition are available free for download from the Altera® website. Visit **www.altera.com/download**.

This chapter does not go as far as downloading and verifying a working system in hardware. Therefore, there are no hardware requirements for the completion of this chapter. However, the example memory subsystem has been tested in hardware.

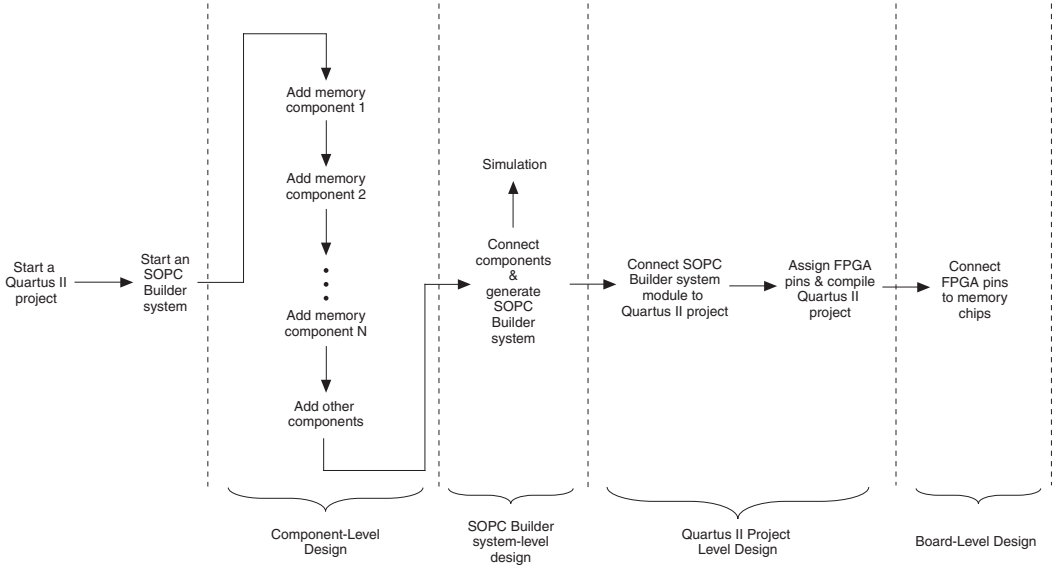
Design Flow

This section describes the design flow for building memory subsystems with SOPC Builder.

The design flow for building a memory subsystem is similar to other SOPC Builder designs. After starting a Quartus II project and an SOPC Builder system, there are five steps to completing the system, as shown in Figure 9–3:

1. Component-level design in SOPC Builder
2. SOPC Builder system-level design
3. Simulation
4. Quartus II project-level design
5. Board-level design

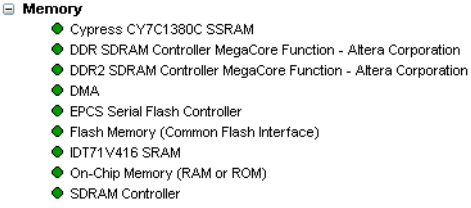
Figure 9–3. Design Flow



Component-Level Design in SOPC Builder

In this step, you specify which memory components to use, and you configure each component to meet the needs of the system. All memory components are available from the **Memory** category in the SOPC Builder list of available components, shown in Figure 9–4.

Figure 9–4. List of Available Memory Components in SOPC Builder



SOPC Builder System-Level Design

In this step, you connect components together and configure the SOPC Builder system as a whole. Similar to the process for adding non-memory SOPC Builder components, you use the SOPC Builder System Contents tab to do the following:

- Rename the component instance (optional).
- Connect the memory component to master ports in the system. Each memory component must be connected to at least one master port.
- Assign a base address.
- Assign a clock domain. A memory component can operate on the same or different clock domain as the master port(s) that access it.

Simulation

In this step, you verify the functionality of the SOPC Builder system module. For systems with memories, this step depends on simulation models for each of the memory components, in addition to the system testbench generated by SOPC Builder. See "Simulation Considerations" on page 9–7.

Quartus II Project-Level Design

In this step, you integrate the SOPC Builder system module with the rest of the Quartus II project. This step includes wiring the system module to FPGA pins, and wiring the system module to other design blocks (such as other HDL modules) in the Quartus II project.

In the example design in this chapter, the SOPC Builder system module comprises the entire FPGA design. There are no other design blocks in the Quartus II project.

Board-Level Design

In this step, you connect the physical FPGA pins to memory devices on the board. If the SOPC Builder system interfaces with off-chip memory devices, then you must make board-level design choices.

Simulation Considerations

SOPC Builder can automatically generate a testbench for register transfer level (RTL) simulation of the system. This testbench instantiates the system module and can also instantiate memory models for external memory components. The testbench is plain-text hardware description

language (HDL), located at the bottom of the top-level system module HDL design file. To explore the contents of the auto-generated testbench, open the top-level HDL file, and search on keyword `test_bench`.

Generic Memory Models

The memory components described in this chapter, except for the SRAM, provide generic simulation models. Therefore, it is very easy to simulate an SOPC Builder system with memory components immediately after generating the system.

The generic memory models store memory initialization files, such as Data [file name extension] (**.dat**) and Hexadecimal (**.hex**) files, in a directory named *<Quartus II project directory>/<SOPC Builder system name>*_**sim**. When generating a new system, SOPC Builder creates empty initialization files. You can manually edit these files to provide custom memory initialization contents for simulation.

For Nios II processor users, the Nios II integrated development environment (IDE) generates initialization contents automatically.

Vendor-Specific Memory Models

You can also manually connect vendor-specific memory models to the system module. In this case, you must manually edit the testbench and connect the vendor memory model. You might also need to edit the vendor memory model slightly for time delays. The SOPC Builder testbench assumes zero delay.

There are special sections of the system module design file that you can edit safely. You must edit only these sections, because SOPC Builder overwrites the rest of the system module every time you generate the system. These sections are marked by the following text:

Verilog HDL

```
// <ALTERA_NOTE> CODE INSERTED BETWEEN HERE
//  add your signals and additional architecture here
// AND HERE WILL BE PRESERVED </ALTERA_NOTE>
```

VHDL

```
-- <ALTERA_NOTE> CODE INSERTED BETWEEN HERE
--add your component and signal declaration here
-- AND HERE WILL BE PRESERVED </ALTERA_NOTE>
```

On-Chip RAM & ROM

Altera FPGAs include on-chip memory blocks, that can be used as RAM or ROM in SOPC Builder systems. On-chip memory has the following benefits for SOPC Builder systems:

- On-chip memory has fast access time, compared to off-chip memory.
- SOPC Builder automatically instantiates on-chip memory inside the system module, so you do not have to make any manual connections.
- Certain memory blocks can have initialized contents when the FPGA powers up. This feature is useful, for example, for storing data constants or processor boot code.

FPGAs have limited on-chip memory resources, which limits the maximum practical size of an on-chip memory to approximately one megabyte in the largest FPGA family.

Component-Level Design for On-Chip Memory

In SOPC Builder you instantiate on-chip memory by adding an **On-chip Memory (RAM or ROM)** component. The configuration wizard for the **On-chip Memory (RAM or ROM)** component has the following options: **Memory Type**, **Size**, and **Read Latency**.

Memory Type

The **Memory Type** options define the structure of the on-chip memory.

- **RAM (writeable)** – This setting creates a readable and writeable memory.
- **ROM (read only)** – This setting creates a read-only memory.
- **Dual-Port Access** – Turning on this setting creates a memory component with two slave ports, which allows two master ports to access the memory simultaneously.
- **Block Type** – This setting forces the Quartus II software to use a specific type of memory block when fitting the on-chip memory in the FPGA. The following choices are available:
  - **Automatic** – This setting allows the Quartus II software to choose the most appropriate memory resource.
  - **M512** – This setting forces the Quartus II software to use M512 blocks.
  - **M4K** – This setting forces the Quartus II software to use M4K blocks.
  - **M-RAM** – This setting forces the Quartus II software to use M-RAM blocks. The 64 Kbit M-RAM blocks are appropriate for larger RAM data buffers. However, M-RAM blocks do not allow pre-initialized contents at power up.

Size

The **Size** options define the size and width of the memory.

- **Memory Width** – This setting determines the data width of the memory. The available choices are 8, 16, 32, 64, or 128 bits. Assign **Memory Width** to match the width of the master port that accesses this memory the most frequently or has the most critical timing requirements.
- **Total Memory Size** – This setting determines the total size of the on-chip memory block. The total memory size must be less than the available memory in the target FPGA.

Read Latency

On-chip memory components use synchronous, pipelined Avalon slave ports. Pipelined access improves f_{MAX} performance, but also adds latency cycles when reading the memory. The **Read Latency** option allows you to specify the number of read latency cycles required to access data. If the **Dual-Port Access** setting is turned on, you can specify a different read latency for each slave port.

SOPC Builder System-Level Design for On-Chip Memory

There are not many SOPC Builder system-level design considerations for on-chip memories. See "SOPC Builder System-Level Design" on page 9–7.

When generating a new system, SOPC Builder creates a blank initialization file in the Quartus II project directory for each on-chip memory that can power up with initialized contents. The name of this file is <*Name of memory component*>**.hex**.

Simulation for On-Chip Memory

At system generation time, SOPC Builder generates a simulation model for the on-chip memory. This model is embedded inside the system module, and there are no user-configurable options for the simulation testbench.

You can provide memory initialization contents for simulation in the file <*Quartus II project directory*>/<*SOPC Builder system name*>**_sim/**<*Memory component name*>**.dat**.

Quartus II Project-Level Design for On-Chip Memory

The on-chip memory is embedded inside the SOPC Builder system module, and therefore there are no signals to connect to the Quartus II project.

To provide memory initialization contents, you must fill in the file <*Name of memory component*>**.hex.** The Quartus II software recognizes this file during design compilation and incorporates the contents into the configuration files for the FPGA.

For Nios II processor users, the Nios II integrated development environment (IDE) generates memory initialization file automatically.

Board-Level Design for On-Chip Memory

The on-chip memory is embedded inside the SOPC Builder system module, and therefore there is nothing to connect at the board level.

Example Design with On-Chip Memory

This section demonstrates adding a 4 Kbyte on-chip RAM to the example design. This memory uses a single slave port with read latency of one cycle.

Figure 9–5 shows the **On-Chip Memory (RAM or ROM)** configuration wizard settings for the example design.

Figure 9–5. On-Chip Memory (RAM or ROM) Configuration Wizard

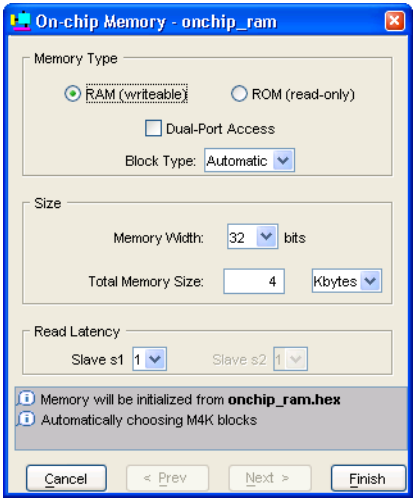
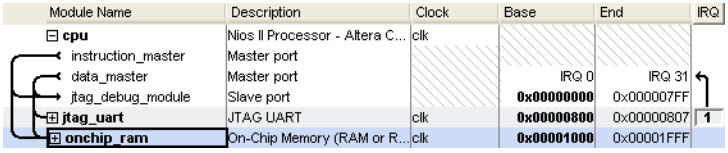


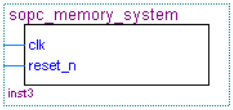
Figure 9–6 shows the SOPC Builder system after adding an instance of the on-chip memory component, renaming it to `onchip_ram`, and assigning it a base address.

Figure 9–6. SOPC Builder System with On-Chip Memory



For demonstration purposes, Figure 9–7 shows the result of generating the system module at this stage. (In a normal design flow, you generate the system only after adding all system components.)

Figure 9–7. System Module with On-Chip Memory



Because the on-chip memory is contained entirely within the system module, **sopc_memory_system** has no I/O signals associated with **onchip_ram**. Therefore, you do not need to make any Quartus II project connections or assignments for the on-chip RAM, and there are no board-level considerations.

EPCS Serial Configuration Device

Many systems use an Altera EPCS serial configuration device to configure the FPGA. Altera provides the EPCS device controller core, which allows SOPC Builder systems to access the memory contents of the EPCS device. This feature provides flexible design options:

- The FPGA design can reprogram its own configuration memory, providing a mechanism for in-field upgrades.
- The FPGA design can use leftover space in the EPCS as nonvolatile storage.

Physically the EPCS device is a serial flash memory device, which has slow access time. Altera provides software drivers to control the EPCS core for the Nios II processor only. Therefore, EPCS controller core features are available only to SOPC Builder systems that include a Nios II processor.

For further details on the features and usage of the EPCS device controller core, see the *EPCS Device Controller Core with Avalon Interface* chapter in volume 5 of the *Quartus II Handbook*.

Component-Level Design for an EPCS Device

In SOPC Builder you instantiate an EPCS controller core by adding an **EPCS Serial Flash Controller** component. There is only one setting for this component: **Reference Designator**. When targeting a board that declares a reference designator for the EPCS device, the **Reference Designator** setting is fixed.

SOPC Builder uses reference designators to specify a unique identifier for flash memory devices on the board. This convention is a requirement of the Nios II EDS, specifically the Nios II Flash Programmer utility.

For details, see the *Nios II Flash Programmer User Guide*.

SOPC Builder System-Level Design for an EPCS Device

There are not many SOPC Builder system-level design considerations for EPCS devices:

- Assign a base address.
- Set the IRQ connection to **NC** (disconnected). The EPCS controller hardware is capable of generating an IRQ. However, the Nios II driver software does not use this IRQ, and therefore you can leave the IRQ signal disconnected.

There can only be one EPCS controller core per FPGA, and the instance of the core is always named `epcs_controller`.

Simulation for an EPCS Device

The EPCS controller core provides a limited simulation model:

- Functional simulation does not include the FPGA configuration process, and therefore the EPCS controller does not model the configuration features.
- The simulation model does not support read and write operations to the flash region of the EPCS device.
- A Nios II processor can boot from the EPCS device in simulation. However, the boot loader code is different during simulation. The EPCS controller boot loader code assumes that all other memory simulation models are pre-initialized, and therefore the boot load process is unnecessary. During simulation, the boot loader simply forces the Nios II processor to jump to start, skipping the boot load process.

Verification in hardware is the best way to test features related to the EPCS device.

Quartus II Project-Level Design for an EPCS Device

The Quartus II software automatically connects the EPCS controller core in the SOPC Builder system to the dedicated configuration pins on the FPGA. This connection is invisible to the user. Therefore there are no EPCS-related signals to connect in the Quartus II project.

Board-Level Design for an EPCS Device

You must connect the EPCS device to the FPGA as described in the Altera *Configuration Handbook*. No other connections are necessary.

Example Design with an EPCS Device

This section demonstrates adding an EPCS device controller core to the example design.

Figure 9–8 shows the **EPCS Serial Flash Controller** configuration wizard settings for the example design. In this example, the target board declares a reference designator U59 for the EPCS device on the board.

Figure 9–8. EPCS Serial Flash Controller Configuration Wizard

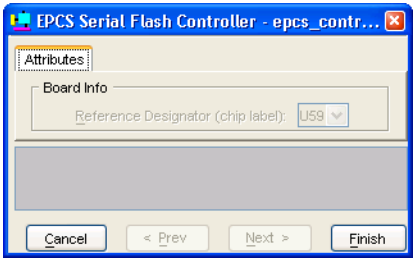
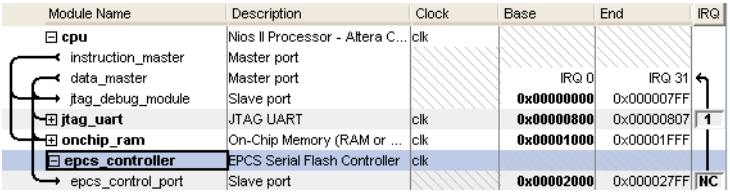


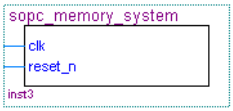
Figure 9–9 shows the SOPC Builder system after adding an instance of the EPCS controller core and assigning it a base address.

Figure 9–9. SOPC Builder System with EPCS Device



For demonstration purposes only, Figure 9–10 shows the result of generating the system module at this stage.

Figure 9–10. System Module with EPCS Device



Because the Quartus II software automatically connects the EPCS controller core to the FPGA pins, the system module has no I/O signals associated with **epcs_controller**. Therefore, you do not need to make any Quartus II project connections or assignments for the EPCS controller core.

This chapter does not cover the details of configuration using the EPCS device. For further information, see Altera's *Configuration Handbook*.

SDRAM

Altera provides a free SDRAM controller core, which lets you use inexpensive SDRAM as bulk RAM in your FPGA designs. The SDRAM controller core is necessary, because Avalon signals cannot describe the complex interface on an SDRAM device. The SDRAM controller acts as a bridge between the Avalon switch fabric and the pins on an SDRAM device. The SDRAM controller can operate in excess of 100 MHz.

For further details on the features and usage of the SDRAM controller core, see the *SDRAM Controller Core with Avalon Interface* chapter in volume 5 of the *Quartus II Handbook*.

Component-Level Design for SDRAM

The choice of SDRAM device(s) and the configuration of the device(s) on the board heavily influence the component-level design for the SDRAM controller. Typically, the component-level design task involves parameterizing the SDRAM controller core to match the SDRAM device(s) on the board. You must specify the structure (address width, data width, number of devices, number of banks, etc.) and the timing specifications of the device(s) on the board.

For complete details on configuration options for the SDRAM controller core, see the *SDRAM Controller Core with Avalon Interface* chapter in volume 5 of the *Quartus II Handbook*.

SOPC Builder System-Level Design for SDRAM

In SOPC Builder on the System Contents tab, the SDRAM controller looks like any other memory component. Similar to on-chip memory, there are not many SOPC Builder system-level design considerations for SDRAM. See "SOPC Builder System-Level Design" on page 9–7.

Simulation for SDRAM

At system generation time, SOPC Builder can generate a generic SDRAM simulation model and include the model in the system testbench. To use the generic SDRAM simulation model, you must turn on a setting in the

SDRAM controller configuration wizard. You can provide memory initialization contents for simulation in the file <*Quartus II project directory*>/<*SOPC Builder system name*>**_sim/**<*Memory component name*>**.dat.**

Alternately, you can provide a specific vendor memory model for the SDRAM. In this case, you must manually wire up the vendor memory model in the system testbench.

For further details, see "Simulation Considerations" on page 9–7 and "Hardware Simulation Considerations" in the chapter *SDRAM Controller Core with Avalon Interface* in volume 5 of the *Quartus II Handbook*.

Quartus II Project-Level Design for SDRAM

SOPC Builder generates a system module with top-level I/O signals associated with the SDRAM controller. In the Quartus II project, you must connect these I/O signals to FPGA pins, which connect to the SDRAM device on the board. In addition, you might have to accommodate clock skew issues.

Connecting & Assigning the SDRAM-Related Pins

After generating the system with SOPC Builder, you can find the names and directions of the I/O signals in the top-level HDL file for the SOPC Builder system module. The file has the name <*Quartus II project directory*>/<*SOPC Builder system name*>**.v** or <*Quartus II project directory*>/<*SOPC Builder system name*>**.vhd**. You must connect these signals in the top-level Quartus II design file.

You must assign a pin location for each I/O signal in the top-level Quartus II design to match the target board. Depending on the performance requirements for the design, you might have to assign FPGA pins carefully to achieve performance.

Accommodating Clock Skew

As SDRAM frequency increases, so does the possibility that you must accommodate skew between the SDRAM clock and I/O signals. This issue affects all synchronous memory devices, including SDRAM. To accommodate clock skew, you can instantiate an `altpll` megafunction in the top-level Quartus II design to create a phase-locked loop (PLL) clock output. You use a phase-shifted PLL output to drive the SDRAM clock and overcome clock-skew issues. The exact settings for the `altpll` depend on your target hardware; you must experiment to tune the phase shift to match the board.

For details, see the *altpll Megafunction User Guide*.

Board-Level Design for SDRAM

Memory requirements largely dictate the board-level configuration of the SDRAM device(s). The SDRAM controller core can accommodate various configurations of SDRAM on the board, including multiple banks and multiple devices.

For further details, see the "Example Configurations" section in the *SDRAM Controller Core with Avalon Interface* chapter in volume 5 of the *Quartus II Handbook*.

Example Design with SDRAM

This section demonstrates adding a 16 Mbyte SDRAM device to the example design. This SDRAM is a single device with 32-bit data. Figure 9–11 shows the **SDRAM Controller** configuration wizard settings for the example design.

Figure 9–11. SDRAM Controller Configuration Wizard

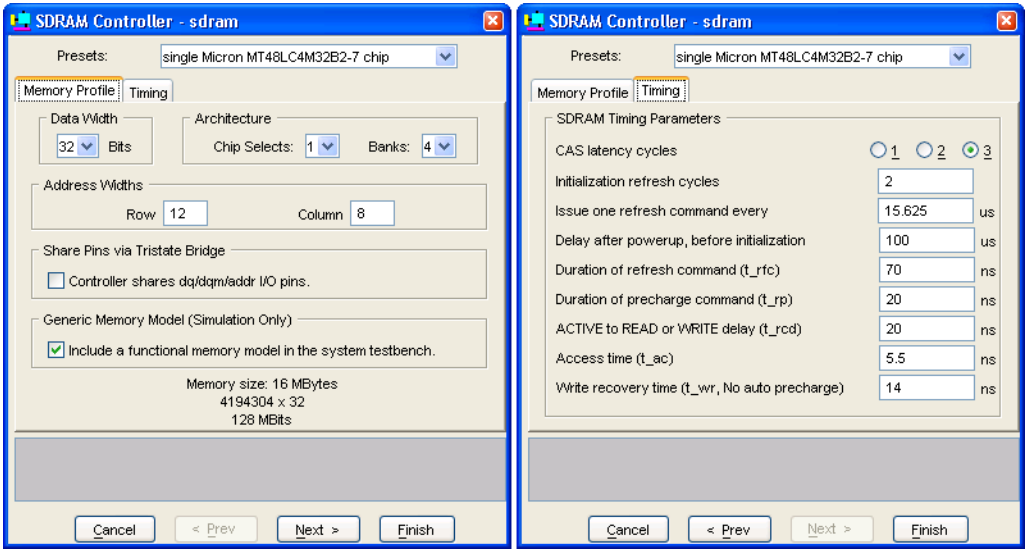
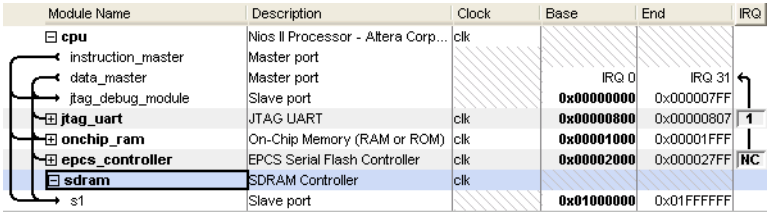


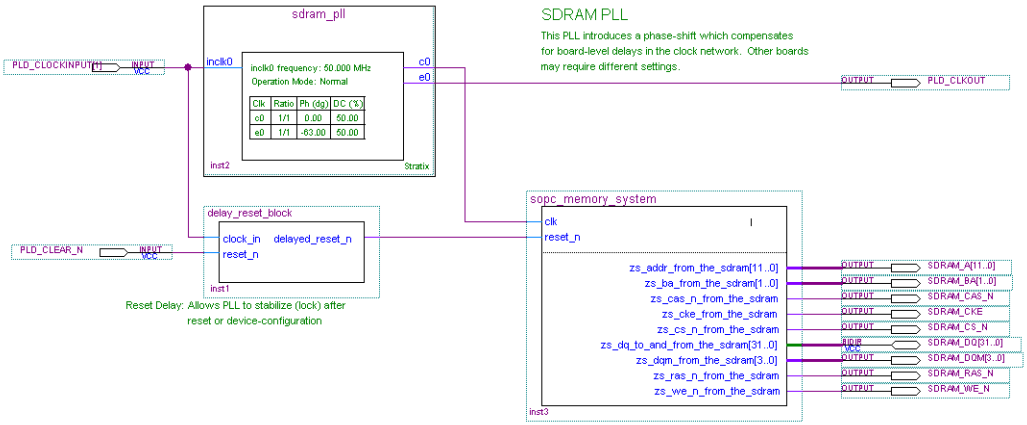
Figure 9–12 shows the SOPC Builder system after adding an instance of the SDRAM controller, renaming it to **sdram**, and assigning it a base address.

Figure 9–12. SOPC Builder System with SDRAM



For demonstration purposes, Figure 9–13 shows the result of generating the system module at this stage, and connecting it in **toplevel_design.bdf**.

Figure 9–13. toplevel_design.bdf with SDRAM



After generating the system, the top-level system module file **sopc_memory_system.v** contains the list of SDRAM-related I/O signals which must be connected to FPGA pins:

```
output   [ 11: 0] zs_addr_from_the_sdram;
output   [  1: 0] zs_ba_from_the_sdram;
output            zs_cas_n_from_the_sdram;
output            zs_cke_from_the_sdram;
output            zs_cs_n_from_the_sdram;
inout    [ 31: 0] zs_dq_to_and_from_the_sdram;
output   [  3: 0] zs_dqm_from_the_sdram;
output            zs_ras_n_from_the_sdram;
output            zs_we_n_from_the_sdram;
```

As shown in Figure 9–13, **toplevel_design.bdf** uses an instance of `sdram_pll` to phase shift the SDRAM clock by -63 degrees. **toplevel_design.bdf** also uses a subdesign `delay_reset_block` to insert a delay on the `reset_n` signal for the system module. This delay is necessary to allow the PLL output to stabilize before the SOPC Builder system begins operating.

Figure 9–14 shows pin assignments in the Quartus II assignment editor for some of the SDRAM pins. The correct pin assignments depend on the target board.

Figure 9–14. Pin Assignments for SDRAM

	To	Location	I/O Bank	I/O Standard	General Function	Special Function	Reserved
188	SDRAM_A[0]	PIN_AE4	7	LVTTL	Column I/O		
189	SDRAM_A[10]	PIN_Y11	7	LVTTL	Column I/O		
190	SDRAM_A[11]	PIN_AB7	7	LVTTL	Column I/O		
191	SDRAM_A[1]	PIN_W12	7	LVTTL	Column I/O	PGM0	
192	SDRAM_A[2]	PIN_AC11	7	LVTTL	Column I/O	nRS	
193	SDRAM_A[3]	PIN_W10	7	LVTTL	Column I/O	RUnLU	
194	SDRAM_A[4]	PIN_AA11	7	LVTTL	Column I/O	PGM1	
195	SDRAM_A[5]	PIN_AC10	7	LVTTL	Column I/O	RDN7	
196	SDRAM_A[6]	PIN_AB11	7	LVTTL	Column I/O	RUP7	
197	SDRAM_A[7]	PIN_AC8	7	LVTTL	Column I/O	FCLK5	
198	SDRAM_A[8]	PIN_AB10	7	LVTTL	Column I/O	FCLK4	
199	SDRAM_A[9]	PIN_V11	7	LVTTL	Column I/O		
200	SDRAM_BA[0]	PIN_AG19	8	LVTTL	Column I/O	DQ6B4	
201	SDRAM_BA[1]	PIN_AF19	8	LVTTL	Column I/O	DQ6B5	
202	SDRAM_CAS_N	PIN_AD18	8	LVTTL	Column I/O	DQ6B2	
203	SDRAM_CKE	PIN_AE18	8	LVTTL	Column I/O	DQ6B1	
204	SDRAM_CS_N	PIN_AG18	8	LVTTL	Column I/O	DQ6B0	
205	SDRAM_DQM[0]	PIN_AE14	7	LVTTL	Column I/O	CLK6n	
206	SDRAM_DQM[1]	PIN_Y13	7	LVTTL	Column I/O	CLK7n	
207	SDRAM_DQM[2]	PIN_AE7	7	LVTTL	Column I/O	DQS1B	
208	SDRAM_DQM[3]	PIN_AG10	7	LVTTL	Column I/O	DQS3B	

Off-Chip SRAM & Flash Memory

SOPC Builder systems can directly access many off-chip RAM and ROM devices, without a controller core to drive the off-chip memory. Avalon signals can exactly describe the interfaces on many standard memories, such as SRAM and flash memory. In this case, I/O signals on the SOPC Builder system module can connect directly to the memory device.

While off-chip memory usually has slower access time than on-chip memory, off-chip memory provides the following benefits:

- Off-chip memory is less expensive than on-chip memory resources.
- The size of off-chip memory is bounded only by the 32-bit Avalon address space.
- Off-chip ROM, such as flash memory, can be used for bulk storage of nonvolatile data.
- Multiple off-chip RAM and ROM memories can share address and data pins to conserve FPGA I/O resources.

Adding off-chip memories to an SOPC Builder system also requires the **Avalon Tristate Bridge** component.

This section describes the process of adding off-chip flash memory and SRAM to an SOPC Builder system.

Component-Level Design for SRAM & Flash Memory

There are several ways to instantiate an interface to an off-chip memory device:

- For common flash interface (CFI) flash memory devices, add the **Flash Memory (Common Flash Interface)** component in SOPC Builder.
- For Altera development boards, Altera provides SOPC Builder components that interface to the specific devices on each development board. For example, the Nios II EDS includes the components **Cypress CY7C1380C SSRAM** and **IDT71V416 SRAM**, which appear on Nios development boards.

These components make it easy for you to create memory systems targeting Altera development boards. However, these components target only the specific memory device on the board; they do not work for different devices.

- For general memory devices, RAM or ROM, you can create a custom interface to the device with the SOPC Builder component editor. Using the component editor, you define the I/O pins on the memory device and the timing requirements of the pins.

In all cases, you must also instantiate the **AvalonTristateBridge** component as well. Multiple off-chip memories can connect to a single tristate bridge.

Avalon Tristate Bridge

A tristate bridge connects off-chip devices to on-chip Avalon switch fabric. The tristate bridge creates I/O signals on the SOPC Builder system module, which you must connect to FPGA pins in the top-level Quartus II project. These pins represent the Avalon switch fabric to off-chip devices.

The tristate bridge creates address and data pins which can be shared by multiple off-chip devices. This feature lets you conserve FPGA pins when connecting the FPGA to multiple devices with mutually exclusive access.

You must use a tristate bridge in either of the following cases:

- The off-chip device has bidirectional data pins.
- Multiple off-chip devices share the address and/or data buses.

In SOPC Builder, you instantiate a tristate bridge by instantiating the **AvalonTristateBridge** component. The Avalon Tristate Bridge configuration wizard has a single option: To register incoming (to the FPGA) signals or not.

- **Registered** – This setting adds registers to all FPGA input pins associated with the tristate bridge (outputs from the memory device).
- **Not Registered** – This setting does not add registers between the memory device output pins and the Avalon switch fabric.

The Avalon tristate bridge automatically adds registers to output signals from the tristate bridge to off-chip devices.

Registering the input and output signals shortens the register-to-register delay from the memory device to the FPGA, resulting in higher system f_{MAX} performance. However, in each direction, the registers add one additional cycle of latency for Avalon master ports accessing memory connected to the tristate bridge. The registers do not affect the timing of the transfers from the perspective of the memory device.

For details on the Avalon tristate interface, refer to the *Avalon Interface Specification*.

Flash Memory

In SOPC Builder, you instantiate an interface to CFI flash memory by adding a **Flash Memory (Common Flash Interface)** component. If the flash memory is not CFI compliant, you must create a custom interface to the device with the SOPC Builder component editor.

The choice of flash device(s) and the configuration of the device(s) on the board heavily influence the component-level design for the flash memory configuration wizard. Typically, the component-level design task involves parameterizing the flash memory interface to match the device(s) on the board. Using the Flash Memory (Common Flash Interface) configuration wizard, you must specify the structure (address width and data width) and the timing specifications of the device(s) on the board.

For details on features and usage, refer to chapter *Common Flash Interface Controller Core with Avalon Interface* in volume 5 of the *Quartus II Handbook*.

For an example of instantiating the Flash Memory (Common Flash Interface) component in an SOPC Builder system, see "Example Design with SRAM & Flash Memory" on page 9–26.

SRAM

To instantiate an interface to off-chip RAM, you perform the following steps:

1. Create a new component with the SOPC Builder component editor that defines the interface.
2. Instantiate the new interface component in the SOPC Builder system.

The choice of RAM device(s) and the configuration of the device(s) on the board determine how you create the interface component. The component-level design task involves entering parameters into the component editor to match the device(s) on the board.

For details on using the component editor, refer to the *Component Editor* chapter in volume 4 of the *Quartus II Handbook*.

SOPC Builder System-Level Design for SRAM & Flash Memory

In SOPC Builder on the System Contents tab, the Avalon tristate bridge has two ports:

- Avalon slave port – This port faces the on-chip logic in the SOPC Builder system. You connect this slave port to on-chip master ports in the system.
- Avalon tristate master port – This port faces the off-chip memory devices. You connect this master port to the Avalon tristate slave ports on the interface components for off-chip memories.

You assign a clock to the Avalon tristate bridge which determines the Avalon clock cycle time for off-chip devices connected to the tristate bridge.

You must assign base addresses to each off-chip memory. The Avalon tristate bridge does not have an address; it passes unmodified addresses from on-chip master ports to off-chip slave ports.

Simulation for SRAM & Flash Memory

The SOPC Builder output for simulation depends on the type of memory component(s) in the system:

- **Flash Memory (Common Flash Interface)** component – This component provides a generic simulation model. You can provide memory initialization contents for simulation in the file *<Quartus II project directory>/<SOPC Builder system name>*_**sim/***<Flash memory component name>*.**dat**.
- Custom memory interface created with the component editor – In this case, you must manually connect the vendor simulation model to the system testbench. SOPC Builder does not automatically connect simulation models for custom memory components to the system module.
- Altera-provided interfaces to memory devices – Altera provides simulation models for these interface components. You can provide memory initialization contents for simulation in the file *<Quartus II project directory>/<SOPC Builder system name>*_**sim/***<Memory component name>*.**dat**. Alternately, you can provide a specific vendor simulation model for the memory. In this case, you must manually wire up the vendor memory model in the system testbench.

For further details, see "Simulation Considerations" on page 9–7.

Quartus II Project-Level Design for SRAM & Flash Memory

SOPC Builder generates a system module with top-level I/O signals associated with the tristate bridge and the memory interface components. In the Quartus II project, you must connect the I/O signals to FPGA pins, which connect to the memory device(s) on the board.

After generating the system with SOPC Builder, you can find the names and directions of the I/O signals in the top-level HDL file for the SOPC Builder system module. The file has the name <*Quartus II project directory*>/<*SOPC Builder system name*>**.v** or <*Quartus II project directory*>/<*SOPC Builder system name*>**.vhd**. You must connect these signals in the top-level Quartus II design file.

You must assign a pin location for each I/O signal in the top-level Quartus II design to match the target board. Depending on the performance requirements for the design, you might have to assign FPGA pins carefully to achieve performance.

SOPC Builder inserts synthesis directives in the top-level system module HDL to assist the Quartus II fitter with signals that interface with off-chip devices. An example is below:

```
reg [ 22: 0] tri_state_bridge_address /* synthesis
ALTERA_ATTRIBUTE =  "FAST_OUTPUT_REGISTER=ON" */;
```

Board-Level Design for SRAM & Flash Memory

Memory requirements largely dictate the board-level configuration of the SRAM & flash memory device(s). You can lay out memory devices in any configuration, as long as the resulting interface can be described with Avalon signals.

Special consideration is required when connecting the Avalon `address` signal to the address pins on the memory devices.

The system module presents the smallest number of address lines required to access the largest off-chip memory, which is usually less than 32 address bits. Not all memory devices connect to all address lines.

Aligning the Least-Significant Address Bits

The Avalon tristate `address` signal always presents a byte address. Each address location in many memory devices contains more than one byte of data. In this case, the memory device must ignore one or more of the least-significant Avalon `address` lines. For example, a 16-bit memory device must ignore Avalon `address[0]` (which is a byte address), and connect Avalon `address[1]` to the least-significant address line.

Table 9–1 shows the relationship between Avalon address lines and off-chip address pins for all possible Avalon data widths.

Table 9–1. Connecting the Least-Significant Avalon Address Line

Avalon address Line	Address Line on Memory Device				
	8-bit Memory	16-bit Memory	32-bit Memory	64-bit Memory	128-bit Memory
address[0]	A0	No connect	No connect	No connect	No connect
address[1]	A1	A0	No connect	No connect	No connect
address[2]	A2	A1	A0	No connect	No connect
address[3]	A3	A2	A1	A0	No connect
address[4]	A4	A3	A2	A1	A0
address[5]	A5	A4	A3	A2	A1
address[6]	A6	A5	A4	A3	A2
address[7]	A7	A6	A5	A4	A3
address[8]	A8	A7	A6	A5	A4
address[9]	A9	A8	A7	A6	A5
address[10]	A10	A9	A8	A7	A6
...	...	...	...	...	...

Aligning the Most-Significant Address Bits

The Avalon address signal contains enough address lines for the largest memory on the tristate bridge. Smaller off-chip memories might not use all of the most-significant address lines.

For example, a memory device with 2^{10} locations uses 10 address bits, while a memory with 2^{20} locations uses 20 address bits. If both these devices share the same tristate bridge, then the smaller memory ignores the ten most-significant Avalon address lines.

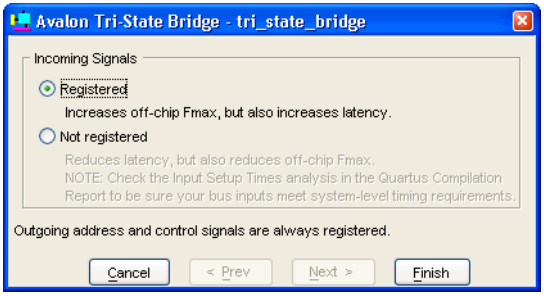
Example Design with SRAM & Flash Memory

This section demonstrates adding a 1 Mbyte SRAM and an 8Mbyte flash memory to the example design. These memory devices connect to the Avalon switch fabric through an Avalon tristate bridge.

Adding the Avalon Tristate Bridge

Figure 9–15 shows the **Avalon Tristate Bridge** configuration wizard for the example design. The example design uses registered inputs and outputs to maximize system f_{MAX}, which increases the read latency by two for both the SRAM and flash memory.

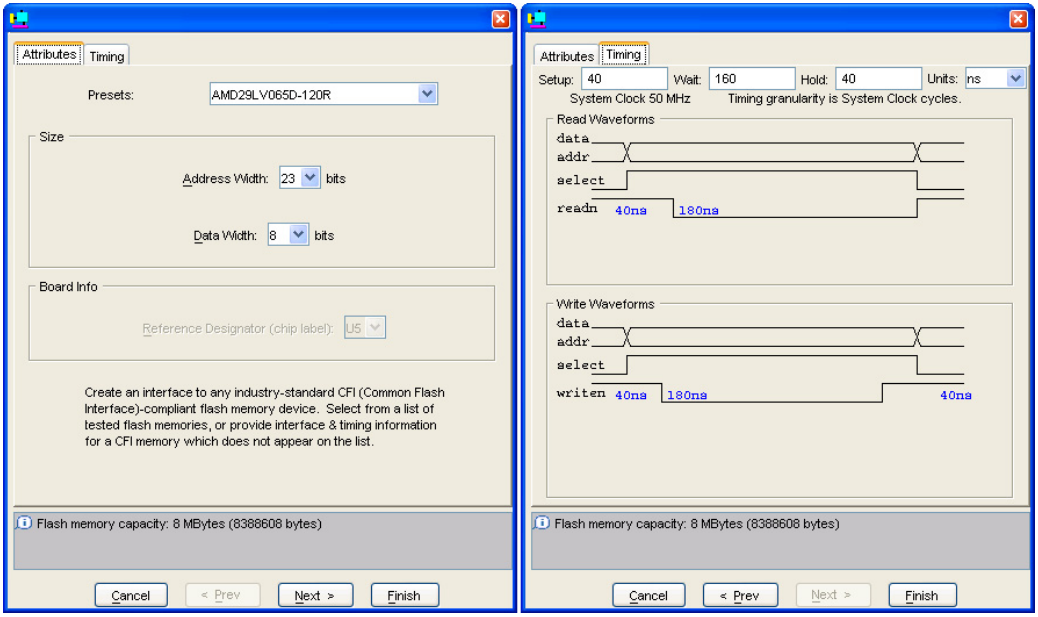
Figure 9–15. Avalon Tristate Bridge Configuration Wizard



Adding the Flash Memory Interface

The flash memory is 8M x 8-bit, which requires 23 address bits and 8 data bits. Figure 9–16 shows the **Flash Memory (Common Flash Interface)** configuration wizard settings for the example design. In this example, the target board declares a reference designator U5 for the flash device on the board.

Figure 9–16. Flash Memory Configuration Wizard



Adding the SRAM Interface

The SRAM device is 256K x 32-bit, which requires 18 address bits and 32 data bits. The example design uses a custom memory interface created with the SOPC Builder component editor. Figure 9–17 – Figure 9–21 shows the settings required on the various component editor tabs to implement an interface to this SRAM.

Figure 9–17. SRAM Interface Component Editor HDL Files Tab

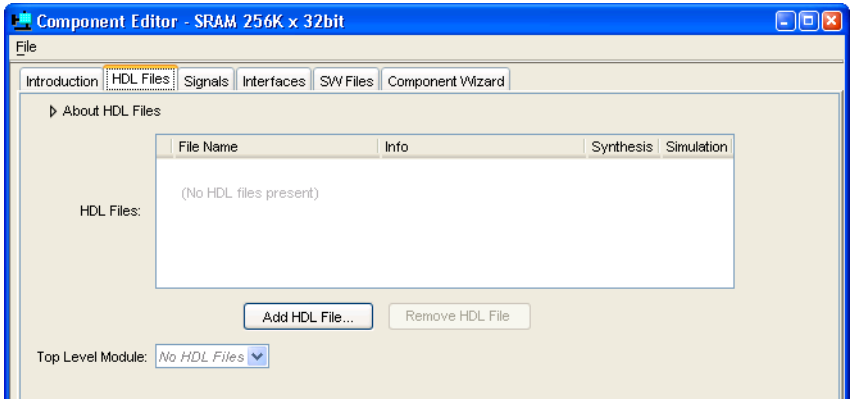


Figure 9–18. SRAM Interface Component Editor Signals Tab

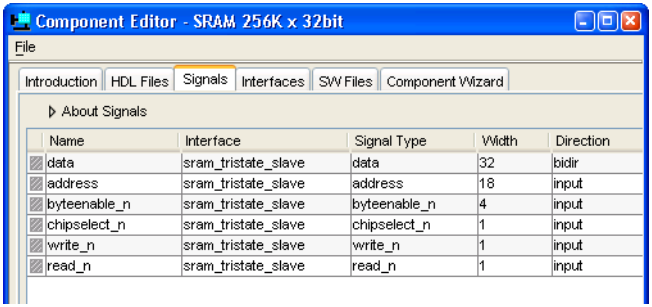


Figure 9–19. SRAM Interface Component Editor Interfaces Tab

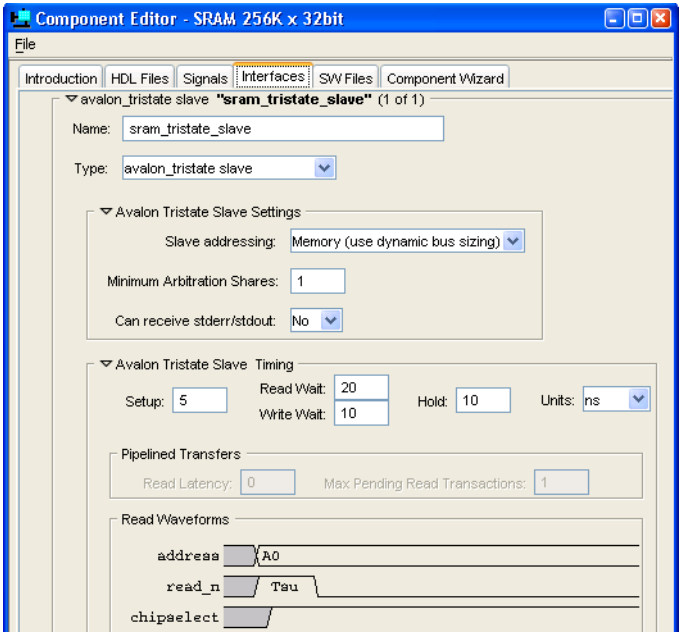
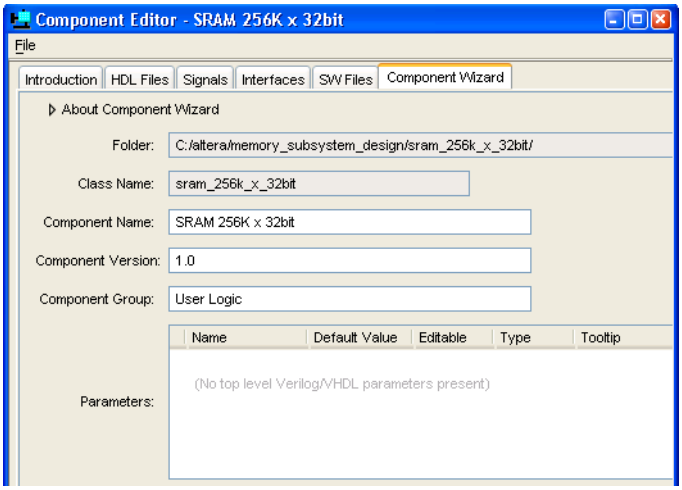


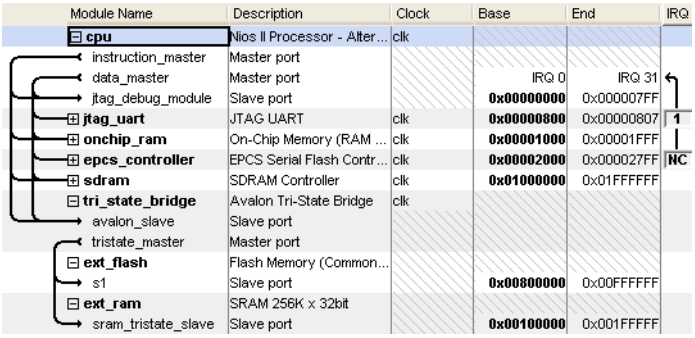
Figure 9–20. SRAM Interface Component Editor Component Wizard Tab



SOPC Builder System Contents Tab

Figure 9–21 shows the SOPC Builder system after adding the tristate bridge and memory interface components, and configuring them appropriately on the **System Contents** tab. Figure 9–21 represents the complete example design in SOPC Builder.

Figure 9–21. SOPC Builder System with SRAM & Flash Memory



After generating the system, the top-level system module file **sopc_memory_system.v** contains the list of I/O signals for SRAM and flash memory which must be connected to FPGA pins:

```
output            chipselect_n_to_the_ext_ram;
output            read_n_to_the_ext_ram;
output            select_n_to_the_ext_flash;
output   [ 22: 0] tri_state_bridge_address;
output   [  3: 0] tri_state_bridge_byteenablen;
inout    [ 31: 0] tri_state_bridge_data;
output            tri_state_bridge_readn;
output            write_n_to_the_ext_flash;
output            write_n_to_the_ext_ram;
```

The Avalon tristate bridge signals which can be shared are named after the instance of the tristate bridge component, such as `tri_state_bridge_data[31:0]`.

Connecting & Assigning Pins in the Quartus II Project

Figure 9–22 shows the result of generating the system module for the complete example design, and connecting it in **toplevel_design.bdf**.

Figure 9–22. toplevel_design.bdf with SRAM & Flash Memory

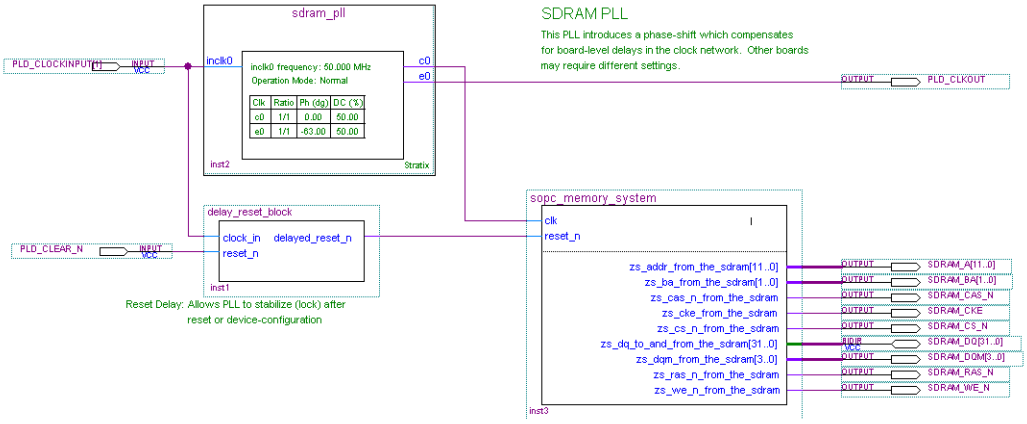


Figure 9–23 shows the pin assignments in the Quartus II assignment editor for some of the SRAM and flash memory pins. The correct pin assignments depend on the target board.

Figure 9–23. Pin Assignments for SRAM & Flash Memory

	To	Location	I/O Bank	I/O Standard	General Function	Special Function	Reser
243	SRAM_BE_N[0]	PIN_M18	3	LVTTL	Column I/O		
244	SRAM_BE_N[1]	PIN_F17	3	LVTTL	Column I/O		
245	SRAM_BE_N[2]	PIN_J18	3	LVTTL	Column I/O	RUP3	
246	SRAM_BE_N[3]	PIN_L17	3	LVTTL	Column I/O	CLK15n	
247	SRAM_CS_N	PIN_B24	3	LVTTL	Column I/O	DQ9T4	
248	SRAM_OE_N	PIN_B26	3	LVTTL	Column I/O	DQ9T7	
249	SRAM_WE_N	PIN_C24	3	LVTTL	Column I/O	DQS9T	

Connecting FPGA Pins to Devices on the Board

Table 9–2 shows the mapping between the Avalon address lines and the address pins on the SRAM and flash memory devices.

Table 9–2. FPGA Connections to SRAM & Flash Memory (Part 1 of 2)

Avalon Address Line	Flash Address (8M x 8-bit Data)	SRAM Address (256K x 32-bit data)
tri_state_bridge_address[0]	A0	No connect
tri_state_bridge_address[1]	A1	No connect
tri_state_bridge_address[2]	A2	A0

Table 9–2. FPGA Connections to SRAM & Flash Memory (Part 2 of 2)

Avalon Address Line	Flash Address (8M x 8-bit Data)	SRAM Address (256K x 32-bit data)
tri_state_bridge_address[3]	A3	A1
tri_state_bridge_address[4]	A4	A2
tri_state_bridge_address[5]	A5	A3
tri_state_bridge_address[6]	A6	A4
tri_state_bridge_address[7]	A7	A5
tri_state_bridge_address[8]	A8	A6
tri_state_bridge_address[9]	A9	A7
tri_state_bridge_address[10]	A10	A8
tri_state_bridge_address[11]	A11	A9
tri_state_bridge_address[12]	A12	A10
tri_state_bridge_address[13]	A13	A11
tri_state_bridge_address[14]	A14	A12
tri_state_bridge_address[15]	A15	A13
tri_state_bridge_address[16]	A16	A14
tri_state_bridge_address[17]	A17	A15
tri_state_bridge_address[18]	A18	A16
tri_state_bridge_address[19]	A19	A17
tri_state_bridge_address[20]	A20	No connect
tri_state_bridge_address[21]	A21	No connect
tri_state_bridge_address[22]	A22	No connect

10. Developing Components for SOPC Builder

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Introduction

This chapter describes the design flow to develop a custom SOPC Builder component. This chapter provides tutorial steps that guide you through the process of creating a custom component, integrating it into a system, and downloading it to hardware.

This chapter is divided into the following sections:

- *Component Development Flow* (see page 10–3).
- *Design Example: Pulse-Width Modulator (PWM) Slave* (see page 10–8). This design example demonstrates developing a component with a single Avalon® slave interface. In this section, you will start with a ready-made HDL design, package it into a SOPC Builder component, and then instantiate it in a system. If you have a development board, you can download the design to hardware and see the PWM work.
- *Sharing Components* (see page 10–28). This section shows you how to relocate component files to use them in other systems, or share them with other designers.

SOPC Builder Components & the Component Editor

SOPC Builder provides a component editor that lets you create and edit your own SOPC Builder components. By following the procedures described in this document, you will learn to use the component editor and turn any custom logic module into an SOPC Builder component.

Once your custom logic is packaged as component, you can instantiate it in an SOPC Builder system in the same manner as commercially available SOPC Builder Ready components. You can share your component with other designers to encourage design reuse.

Typically, a component is comprised of the following:

- Hardware files: HDL modules that describe the component hardware
- Software files: A C-language header file that defines the component register map, and driver software that allows programs to control the component
- Component description file (**class.ptf**): This file defines the structure of the component, and provides SOPC Builder the information it needs to integrate the component into a system. The component

editor generates this file automatically based on the hardware & software files you provide, and the parameters you specify in the component editor GUI.

After you create the hardware and software files that describe the component, you use the component editor to package those file into an SOPC Builder component. You can also use the component editor later to re-edit the component, if you ever update the hardware or software files.

Assumptions About the Reader

This chapter assumes that you are familiar with the following:

- Building systems with SOPC Builder. For details, see the *Introduction to SOPC Builder* and *Tour of the SOPC Builder User Interface* chapters in volume 4 of the *Quartus II Handbook*.
- SOPC Builder components. For details, see the *SOPC Builder Components* chapter in volume 4 of the *Quartus II Handbook*.
- Basic concepts of the Avalon interface. You do not need extensive knowledge of the Avalon interface, such as transfer types or signal timing, to use the design example(s) provided with this chapter. However, to create your own custom components, you need a fuller understanding of the Avalon interface. For details, see the *Avalon Interface Specification*.

Hardware & Software Requirements

To use the design example(s) in this chapter, you must have the following:

- Design files for the example design – A hyperlink to the design files appears next to this chapter on the SOPC Builder literature page. Visit **www.altera.com/sopcbuilder**.
- Quartus® II Software version 4.2 or higher – Both Quartus II Web Edition and the fully licensed version will work with the example design.
- Nios® II Embedded Design Suite (EDS) version 1.1 or higher – Both the evaluation edition and the fully licensed version will work with the example design.
- Nios development board and an Altera® USB-Blaster™ download cable (Optional) – You can use any of the following Nios development boards:
  - Stratix® II Edition
  - Stratix Edition
  - Stratix Professional Edition
  - Cyclone™ Edition

If you do not have a development board, you can follow the hardware development steps, but you will not be able to download the complete system to a working board.

You can download the Quartus II Web Edition software and the Nios II EDS, Evaluation Edition for free from the Altera Download Center at **www.altera.com**.

Before you begin, you must install the Quartus® II software and Nios II development tools.

Component Development Flow

This section provides an overview of the development process for SOPC Builder components, covering both the hardware and software aspects. This section focuses on the design flow for components with a single Avalon slave interface. However, these steps are easily extrapolated to components with a master port, or multiple master and slave ports.

Typical Design Steps

A typical development sequence for a slave component includes the following steps, not necessarily in this order:

1. Specify the hardware functionality.
2. If a microprocessor will be used to control the component, specify the application program interface (API) to access and control the hardware.
3. Based on the hardware and software requirements, define an Avalon interface that provides:
    a. Appropriate control mechanisms
    b. Adequate throughput performance
4. Write HDL that describes the hardware in either Verilog or VHDL.
5. Test the component hardware alone to verify correct operation.
6. Write a C header file that defines the hardware-level register map for software.
7. Use the component editor to package the initial hardware and software files into a component.

8. Instantiate the component into a simple SOPC Builder system module.

9. Test register-level accesses to the component using a microprocessor, such as the Nios II processor. You can perform verification in hardware, or on an HDL simulator such as ModelSim®.

10. If a microprocessor will be used to control the component, write driver software.

11. Iteratively improve the component design, based on in-system behavior of the component:

    a. Make hardware improvements and adjustments.

    b. Make software improvements and adjustments.

    c. Incorporate hardware and software changes into the component using the component editor.

12. Build a complete SOPC Builder system incorporating one or more instances of the component.

13. Perform system-level verification. Make further iterative improvements, if necessary.

14. Finalize the component and distribute it for design reuse.

The design process for a master component is similar, except for software development aspects.

Hardware Design

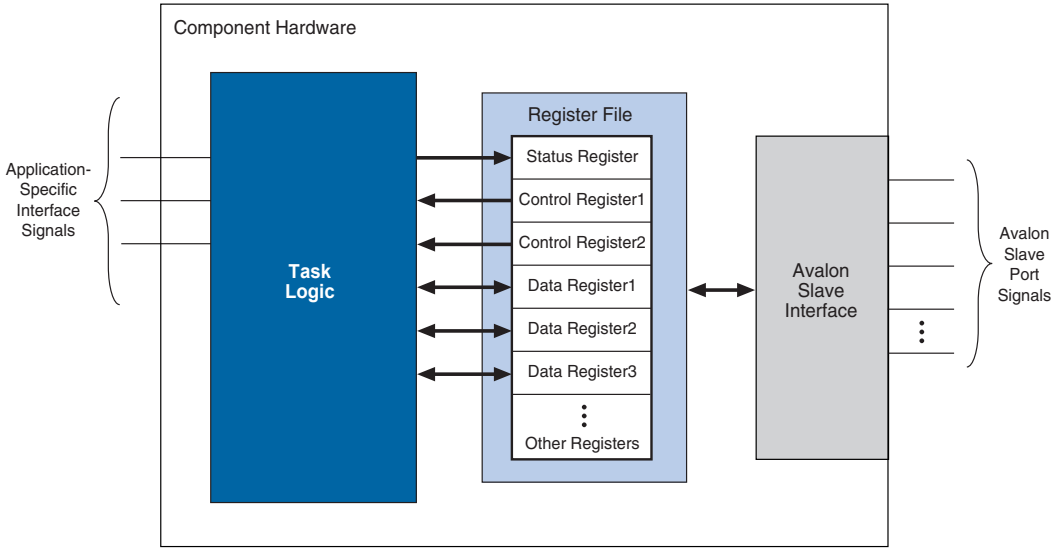
As with any logic design process, the development of SOPC Builder component hardware begins after the specification phase. Coding the HDL is an iterative process, as you write and verify the HDL logic against the specification.

The architecture of a typical component consists of the following functional blocks:

- *Task Logic* - The task logic implements the component's fundamental function. The task logic is design dependent.
- *Register File* - The register file provides a path for communicating signals from inside the task logic to the outside world, and vice versa. The register file maps internal nodes to addressable offsets that can be read or written by the Avalon interface.
- *Avalon Interface* - The Avalon interface provides a standard Avalon front-end to the register file. The interface uses any Avalon signal types necessary to access the register file and support the transfer types required by the task logic. The following factors affect the Avalon interface:
  - How wide is the data to be transferred?
  - What is the throughput requirement for the data transfers?
  - Is this interface primarily for control or for data? That is, do transfers tend to be sporadic, or come in continuous bursts?
  - Is the hardware relatively fast or slow compared to other components that will be in a system?

Figure 10–1 shows a block diagram of a typical component with one Avalon slave port.

Figure 10–1. Typical Component with One Avalon Slave Port



Software Design

If your intent is for a microprocessor to control your component, then you must provide software files that define the software view of the component. At a minimum, you must define the register map for each slave port that is accessible to a processor. The component editor lets you package a C header file with the component to define the software view of the hardware.

Typically, the header file declares macros to read and write each register in the component, relative to a symbolic base address assigned to the component. The following example shows an excerpt from the register map for an Altera-provided UART component for the Nios II processor.

Example: Register Map for a Component

```
#include <io.h>
#define IOADDR_ALTERA_AVALON_TIMER_STATUS(base)         __IO_CALC_ADDRESS_NATIVE(base, 0)
#define IORD_ALTERA_AVALON_TIMER_STATUS(base)           IORD(base, 0)
#define IOWR_ALTERA_AVALON_TIMER_STATUS(base, data)     IOWR(base, 0, data)

#define ALTERA_AVALON_TIMER_STATUS_TO_MSK               (0x1)
#define ALTERA_AVALON_TIMER_STATUS_TO_OFST              (0)
#define ALTERA_AVALON_TIMER_STATUS_RUN_MSK              (0x2)
#define ALTERA_AVALON_TIMER_STATUS_RUN_OFST             (1)

#define IOADDR_ALTERA_AVALON_TIMER_CONTROL(base)        __IO_CALC_ADDRESS_NATIVE(base, 1)
#define IORD_ALTERA_AVALON_TIMER_CONTROL(base)          IORD(base, 1)
#define IOWR_ALTERA_AVALON_TIMER_CONTROL(base, data)    IOWR(base, 1, data)

#define ALTERA_AVALON_TIMER_CONTROL_ITO_MSK             (0x1)
#define ALTERA_AVALON_TIMER_CONTROL_ITO_OFST            (0)
#define ALTERA_AVALON_TIMER_CONTROL_CONT_MSK            (0x2)
#define ALTERA_AVALON_TIMER_CONTROL_CONT_OFST           (1)
#define ALTERA_AVALON_TIMER_CONTROL_START_MSK           (0x4)
#define ALTERA_AVALON_TIMER_CONTROL_START_OFST          (2)
#define ALTERA_AVALON_TIMER_CONTROL_STOP_MSK            (0x8)
#define ALTERA_AVALON_TIMER_CONTROL_STOP_OFST           (3)
```

Software drivers abstract hardware details of the component so that software can access the component at a high level. The driver functions provide the software an API to access the hardware. The software requirements vary according to the needs of the component. The most common types of routines initialize the hardware, read data, and write data.

Driver software is dependent on the target processor. The component editor lets you easily package software drivers for the hardware abstraction layer (HAL) used by the Nios II processor development tools. To provide drivers for other processors, you must accommodate the needs of the development tools for the target processor.

For details on writing drivers for the Nios II HAL, see the *Nios II Software Developer's Handbook*. It is instructive to look at the software files provided for other ready-made components. The Nios II EDS provides many components you can use as reference. See <*Nios II EDS install path*>**/components/**.

Verifying the Component

You can verify the component in incremental stages, as you complete more and more of the design. Typically, you first verify the hardware logic as a unit (which might comprise multiple smaller stages of verification), and later you verify the component in a system.

Unit Verification

To test the task logic block alone, you use your preferred verification method(s), such as behavioral or register transfer level (RTL) simulation tools. Similarly, you can verify all component logic, including the register file and the Avalon interface(s), using your preferred verification tools.

After you package the HDL files into a component using the component editor, the Nios II EDS offers an easy-to-use method to simulate read and write transactions to the component. Using the Nios II processor's robust simulation environment, you can write C code for the Nios II processor that initiates read and write transfers to your component. The results can be verified either on the ModelSim simulator or on hardware, such as a Nios development board.

See *AN351: Simulating Nios II Embedded Processor Designs* for more information.

System-Level Verification

After you package the HDL files into a component using the component editor, you can instantiate the component in a system, and verify the functionality of the overall system module.

SOPC Builder provides support for system-level verification for RTL simulators such as ModelSim. While SOPC Builder produces a testbench for system-level verification, the capability of the simulation environment is largely dependent on the components included in the system.

During the verification phase, including a Nios II processor in the system can be useful to get the benefits of the Nios II simulation environment. Even if your component has no relationship to the Nios II processor, the auto-generated ModelSim simulation environment provides an easy-to-use base that you can build upon to verify other logic in the system.

Design Example: Pulse-Width Modulator Slave

This section uses a pulse-width modulator (PWM) design example to demonstrate the steps to create a component and instantiate it in a system. This component has a single Avalon slave port.

In this section, you will perform the following steps:

1. Install the design files.
2. Review the example design specifications.
3. Package the design files into an SOPC Builder component.
4. Instantiate the component in hardware.
5. Compile the hardware design in the Quartus II software, and download the design to a target board.
6. Exercise the hardware using Nios II software.

Install the Design Files

Before you proceed, you must install the Nios II development tools and download the PWM example design from the Altera web site. The hardware design used in this chapter is based on the **standard** hardware example design included with the Nios II EDS.

Do not use spaces in any directory path names when installing the design files. If the path contains spaces, SOPC Builder might not be able to access the files.

Perform the following steps to setup the design environment:

1. Unzip the contents of the PWM zip file to a directory on your computer. This document will refer to this directory as the <*PWM design files*> directory.

2. On your host computer file system, locate the following directory:

   *<Nios II EDS install path>***/examples/***<verilog or vhdl>***/***<board version>***/standard**

   Each development board has a VHDL and Verilog version of the design. You can use either one. Table 10–1 shows the names of the directories for the available Nios development boards.

Table 10–1. Design File Directories

Nios Development Board	Tutorial Directory
Stratix II Edition	niosII_stratixII_2s60_es
Stratix Edition	niosII_stratix_1s10 or niosII_stratix_1s10_es
Stratix Professional Edition	niosII_stratix_1s40
Cyclone Edition	niosII_cyclone_1c20

   For demonstration purposes, the figures in this chapter show the case of the Verilog design on the Nios Development Board, Cyclone Edition.

3. Copy the **standard** directory to a new location. By copying the design files, you avoid corrupting the original design. This document will refer to the newly-created directory as the ***<Quartus II project>*** directory.

Review the Example Design Specifications

This section discusses the design specifications for the provided PWM example design, giving details on each of the following topics:

- PWM Design Files
- Functional Specification
- PWM Task Logic
- Register File
- Avalon Interface
- Software API

In a typical design flow, it is the designer's responsibility to specify the behavior of the component.

PWM Design Files

Table 10–2 lists the contents provided in the <*PWM design files*> directory.

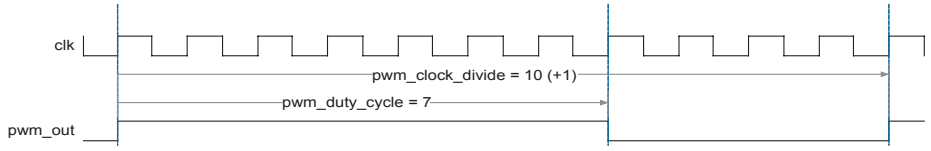
Table 10–2. PWM Design Files Directory

File Name	Description
/pwm_hw	Contains HDL files describing the component hardware.
pwm_task_logic.v	Contains the core of the PWM functionality.
pwm_register_file.v	Contains logic for reading and writing PWM registers.
pwm_avalon_interface.v	Instantiates task logic and register file, and provides an Avalon slave interface. This file contains the top-level module.
/pwm_sw	Contains C files describing the software interface to the component.
/inc	Contains header files defining low-level hardware interface.
avalon_slave_pwm_regs.h	Defines macros to access registers in the PWM component.
/HAL	Contains HAL driver files for the Nios II processor.
/inc	Contains HAL driver include files.
altera_avalon_pwm_routines.h	Declares function prototypes for accessing the PWM.
/src	Contains HAL driver source code files.
altera_avalon_pwm_routines.c	Defines functions for accessing the PWM.
/test_software	Contains an example program to test the component hardware & software.
hello_altera_avalon_pwm.c	`main()` initializes the PWM hardware, and uses the PWM to blink an LED.

Functional Specification

A PWM component outputs a square wave with modulated duty cycle. A basic pulse-width waveform is shown in Figure 10–2.

Figure 10–2. Basic Pulse-Width Modulation Waveform



The PWM component is specified and created as follows:

- The task logic operates synchronously to a single clock.
- The task logic uses 32-bit counters to provide a suitable range of PWM periods and duty cycles.
- A host processor is responsible for setting the PWM period value and duty-cycle value. This requirement implies the need for a read/write interface to control logic.
- Register elements are defined to hold the PWM period value and duty-cycle value.
- The host processor can halt the PWM output by using an enable control bit.

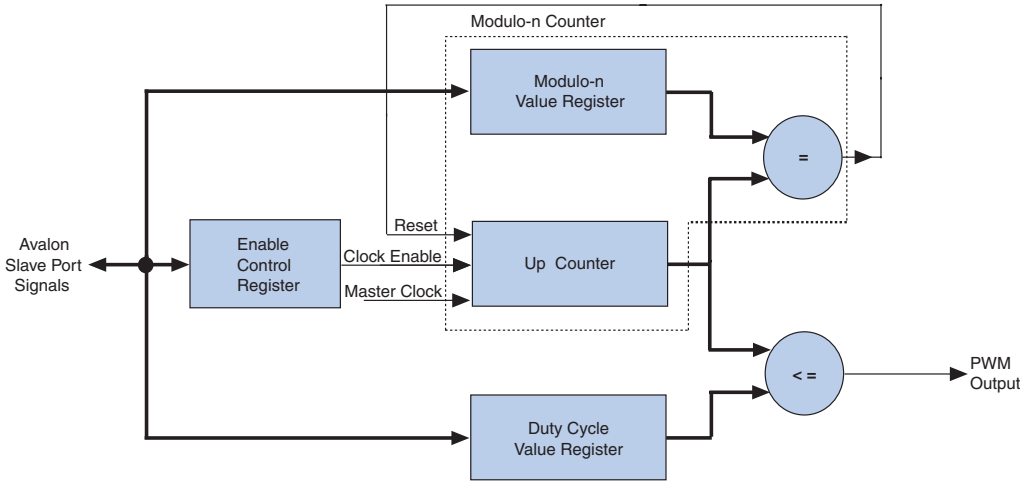
PWM Task Logic

The PWM task logic has the following characteristics:

- The PWM task logic consists of an input clock (`clk`), an output signal (`pwm_out`), an enable bit, a 32-bit modulo-n counter, and a 32-bit comparator circuit.
- `clk` drives the 32-bit modulo-n counter to establish the period of the `pwm_out` signal.
- The comparator compares the current value of the modulo-n counter to the duty-cycle value and determines the output of `pwm_out`.
- When the current count value is less than or equal to the duty-cycle value, `pwm_out` drives logic value 0; otherwise, it drives logic value 1.

The task-logic structure is shown in Figure 10–3.

Figure 10–3. PWM Task Logic Structure



Register File

The register file provides access to the enable bit, the modulo-n value and the duty cycle value, shown in Figure 10–3. The design maps each register to a unique offset in the Avalon slave port address space.

Each register has read and write access, which means that software can read back values previously written into the registers. This is an arbitrary design choice that provides software convenience at the expense of hardware resources. You could equally design the registers to be write-only, which would conserve on-chip logic resources, but make it impossible for software to read back the register values.

The register file and offset mapping is shown in Table 10–3. To support three registers, two bits of address encoding are necessary. This gives rise to the fourth register which is reserved.

Table 10–3. Register File & Address Mapping

Register Name	Offset	Access	Description
`clock_divide`	00	Read / Write	The number of clock cycles counted during one cycle of the PWM output.
`duty_cycle`	01	Read / Write	The number of clock cycles in which the PWM output will be low.
`enable`	10	Read / Write	Enables/disables the PWM output. Setting bit `0` to `1` enables the PWM.
Reserved	11	-	

To read or write the registers requires only one clock cycle, which affects the wait-states for the Avalon interface.

Avalon Interface

The Avalon interface for the PWM component requires a single slave port using a small set of Avalon signals to handle simple read and write transfers to the registers. The component's Avalon slave port has the following characteristics:

- It is synchronous to the Avalon slave port clock.
- It is readable and writeable.
- It has zero wait states for reading and writing, because the registers are able to respond to transfers within one clock cycle.
- It has no setup or hold restrictions for reading and writing.
- Read latency is not required, because all transfers can complete in one clock cycle. Read latency would not improve performance.
- It uses native address alignment, because the slave port is connected to registers rather than a memory device.

Table 10–4 lists the Avalon signals types required to implement these transfer properties. The table also lists the names of each signal as defined in the HDL design file.

Table 10–4. PWM Signal Names & Avalon Signal Types

Signal Name in HDL	Avalon Signal Type	Bit-Width	Direction	Notes
clk	clk	1	input	Clock that synchronizes data transfers and task logic
resetn	reset_n	1	input	Reset signal; active low.
avalon_chip_select	chipselect	1	input	Chip-select signal
address	address	2	input	2-bit address; only three encodings are used.
write	write	1	input	Write enable signal
write_data	writedata	32	input	32-bit write-data value
read	read	1	input	Read enable signal
read_data	readdata	32	output	32-bit read-data value

For details on the behavior of Avalon signals and Avalon transfers, see the *Avalon Interface Specification*.

Software API

The PWM example design provides both a header file that defines the register map, and driver software for the Nios II processor. See Table 10–2 on page 10–10 for a description of the individual files. The driver functions are listed in Table 10–5.

Table 10–5. PWM Driver Functions (1)

Function	Prototype Description
altera_avalon_pwm_init();	Initializes the PWM hardware
altera_avalon_pwm_enable();	Activates the PWM output
altera_avalon_pwm_disable();	Deactivates the PWM output
altera_avalon_pwm_change_duty_cycle();	Changes the PWM duty cycle

Note for Table 10–5:
(1) Each function takes a parameter that specifies the base address of a specific instance of the PWM component.

Package the Design Files into an SOPC Builder Component

In this section, you will use the SOPC Builder component editor to package the design files into an SOPC Builder component. You will perform the following operations:

1. Open the Quartus II project and start the component editor.
2. Configure the settings on each tab of the component editor.
3. Save the Component.

Open the Quartus II Project & Start the Component Editor

To open SOPC Builder from the Quartus II software, you must have a Quartus II project open. Perform the following steps:

1. Start the Quartus II software.
2. Open the project **standard.qpf** in the **<*Quartus II project*>** directory.
3. On the Tools menu, click **SOPC Builder**. The SOPC Builder GUI appears, displaying a ready-made example design containing a Nios II processor and several components in the table of active components.
4. On the File menu, click **New Component**. The component editor GUI appears, displaying the **Introduction** tab.

HDL Files Tab

In this section you will associate the HDL files with the component using the **HDL Files** tab. Perform the following steps:

1. Click the **HDL Files** tab.

Each tab in the component editor GUI provides on-screen information that describes how to use each tab. Click the triangle at the top-left of each tab to view these instructions.

2. Click **Add HDL File**.
3. Browse to the <*PWM design files*>**/pwm_hw** directory. There are three Verilog HDL (**.v**) files in this directory.

4. Select all three HDL files in this directory and click **Open**. Use the control key to select multiple files.

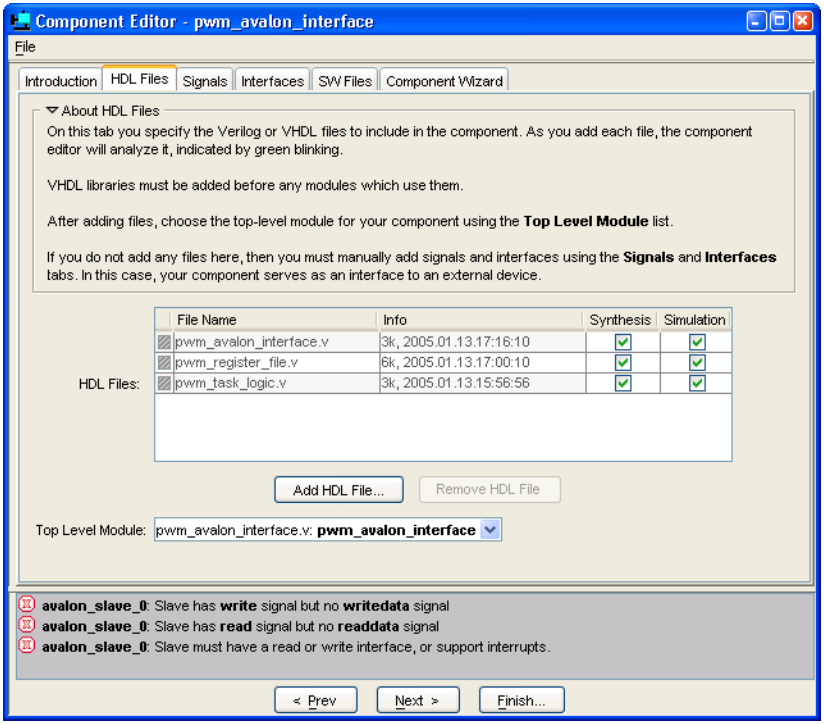
   You will return to the **HDL Files** tab. The component editor immediately analyzes each file to read I/O signal and parameter information from the file.

5. Ensure that both the **Simulation** and **Synthesis** boxes are turned on for all files. This indicates that each file is appropriate for both simulation and synthesis design flows.

6. Select **pwm_avalon_interfave.v: pwm_avalon_interface** in the **Top Level Module** list to specify the top-level module.

At this point, the component editor GUI displays error messages. Ignore these messages for now, because you will fix them in later steps. Figure 10–4 shows the state of the **HDL Files** tab.

Figure 10–4. HDL Files Tab



Signals Tab

For every I/O signal present on the top-level HDL module, you must map the signal name to a valid Avalon signal type using the **Signals** tab. The component editor automatically fills in signal details that it finds in the top-level HDL source file. If a signal is named the same as a recognized Avalon signal type (such as `write` or `address`), then the component editor automatically assigns the signal's type. If the component editor cannot determine the signal type, it assigns it to type **export.**

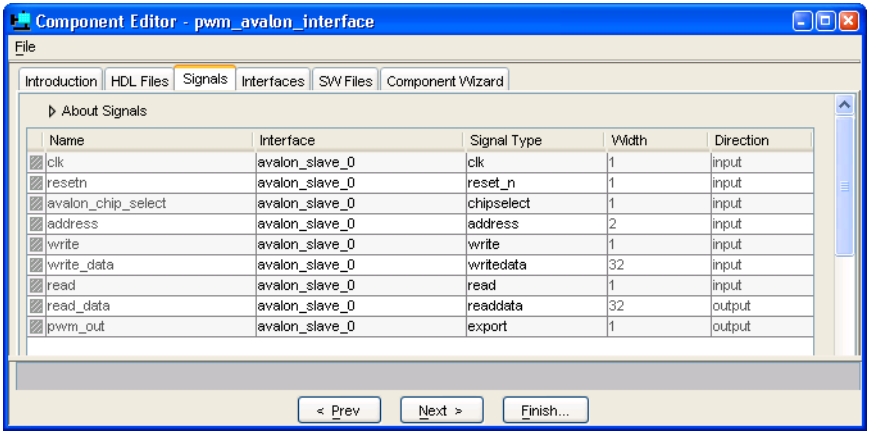
Perform the following steps to define the component I/O signals:

1. Click the **Signals** tab. All of the I/O signals in the top level HDL module **pwm_avalon_interface** appear automatically.

2. Assign the **Signal Type** settings for all signals, as show in Figure 10–5. To change a value, click the **Signal Type** cell to display a drop-down list, and select a new signal type from the list.

After you correctly assign each signal name to a signal type, the error messages should disappear.

Figure 10–5. Assigning Signal Names to Signal Types



You assign type **export** to the signal `pwm_out`, because it is not an Avalon signal. It is intended to be an output of the SOPC Builder system.

Interfaces Tab

The **Interfaces** tab lets you configure the properties of all Avalon interfaces on the component. In this case there is only one Avalon interface, as specified in the section "Avalon Interface" on page 10–13. Perform the following steps to configure the Avalon slave port:

1. Click the **Interfaces** tab. The component editor displays a default Avalon slave port that it created automatically, based on the top-level I/O signals in the component design.

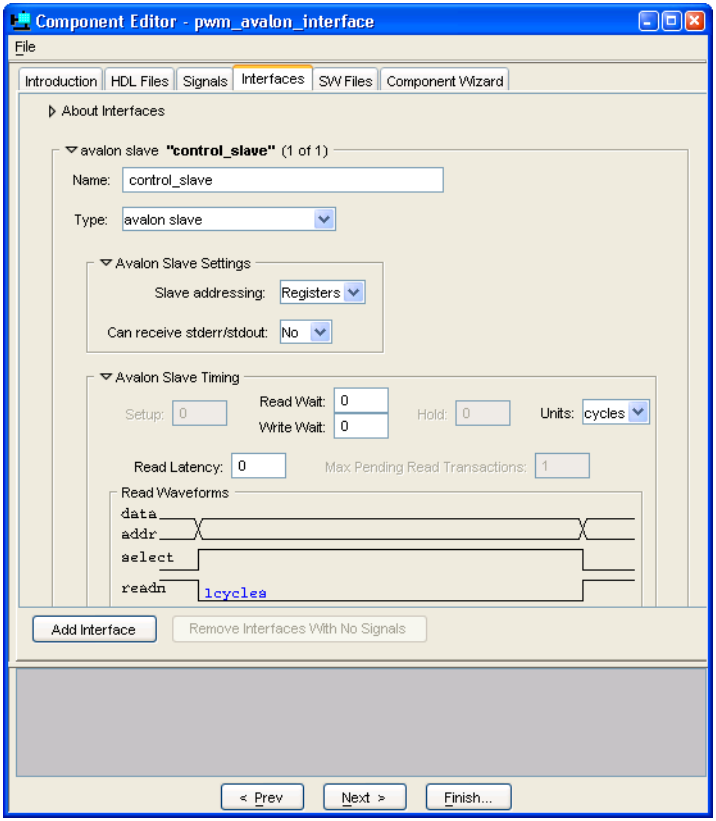
2. Type `control_slave` in the **Name** field to rename the slave port. This name appears in the SOPC Builder GUI when you instantiate the component in SOPC Builder.

3. Change the settings for the **control_slave** interface as listed in Table 10–6 below. Figure 10–6 on page 10–19 shows the **Interfaces** tab with the correct settings.

Table 10–6. Control Slave Interface Settings

Setting	Value	Description
Slave addressing	Registers	This setting is appropriate for slave ports used to access address-mapped registers
Read Wait	0	This setting means that the slave port responds to read requests in a single clock cycle (that is, it does not need read waitstates.)
Write Wait	0	This setting means that the slave port captures write requests in a single clock cycle (that is, it does not need write waitstates.)

Figure 10–6. Configuring the Interface Properties



Software Files (SW Files) Tab

The **SW Files** tab lets you associate software files with the component, and specify their usage. This component example design provides both a header file that defines the registers and driver software for the Nios II processor. For a description of each file, see Table 10–2 on page 10–10.

Perform the following steps to import the software files into the component:

1. Click the **SW Files** tab.
2. Click **Add SW File**. The Open dialog appears.
3. Browse to the directory <*PWM design files*>**/pwm_sw/inc**.

4. Select the file **altera_avalon_pwm_regs.h** and click **Open**.

5. Click the **Type** cell for **altera_avalon_pwm_regs.h** to change the file type. A drop-down list appears.

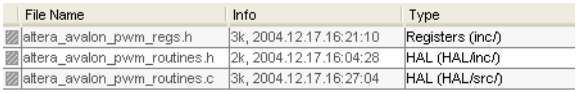
6. Select **type Registers (inc/)**.

7. Repeat steps 2 to 6 to add the file **<***PWM design files***>/pwm_sw/HAL/inc/altera_avalon_pwm_routines.h** and set its type to **HAL (HAL/inc/)**.

8. Repeat steps 2 to 6 to add the file **<***PWM design files***>/pwm_sw/HAL/src/altera_avalon_pwm_routines.c** and set its type to **HAL (HAL/src/)**.

Figure 10–7 shows the SW Files tab with the correct settings.

Figure 10–7. Software Files (SW Files) Tab



Component Wizard Tab

This tab lets you control how SOPC Builder presents the component to a user. Perform the following steps to configure the user presentation of the component:

1. Click the **Component Wizard** tab.

2. For this example, do not change the default settings for **Component Name**, **Component Version**, and **Component Group**.

   These settings affect how SOPC Builder identifies the component and displays it in the list of available components. The component editor creates a default name for the component, based on the name of the top-level design module.

3. Under **Parameters**, in the **Tooltip** cell for the parameter **clock_divide_reg_init**, type the following:

```
Initial PWM Period After Reset
```

4. In the **Tooltip** cell for **clock_cycle_reg_init**, type:

```
Initial Duty Cycle After Reset
```

5. Click **Preview the Wizard** to preview how the component wizard will appear when instantiated from within SOPC Builder.

6. Close the preview window when you are done.

Save the Component

Perform the following steps to save the component and exit the component editor:

1. Click **Finish**. A dialog appears describing the files that will be created for the component.

2. Click **Yes** to save the files. The component editor saves the files to a subdirectory under **<*Quartus II project*>**. The component editor closes, and you return to the main SOPC Builder GUI.

3. Locate the new component **pwm_avalon_interface** in the list of available components under the **User Logic** group.

You are ready to instantiate the component into an SOPC Builder system.

Instantiate the Component in Hardware

At this point, the new component is ready to instantiate in an SOPC Builder system. The usage of a component is design dependent, based on the needs of the system. The remaining steps for this design example show one possible way to instantiate and test the component. However, there is an unlimited number of ways this component can be used in a system.

In this section you will add the new PWM component to a system, recompile the hardware design, and configure the FPGA. This section includes the following steps:

1. Add a PWM component to the SOPC Builder system and regenerate the system.

2. Modify the Quartus II design to connect the PWM output to an FPGA pin.

3. Compile the Quartus II design and configure the FPGA with the new hardware image.

Add a PWM Component to the SOPC Builder System

Perform the following steps to setup SOPC Builder's component search path:

1. In the SOPC Builder GUI, on the File menu, click **SOPC Builder Setup**.
2. Under **Component/Kit Library Search Path**, enter the path to the ***<Quartus II project>*** directory. If there are pre-existing paths, use "+" to separate the path names.
3. Click **OK**.

The steps above make the component's software files visible to the Nios II IDE in later steps. These steps are necessary for the Quartus II software v4.2 and the Nios II IDE v1.1. Future releases will eliminate the need for these steps.

Perform the following steps to add a PWM component to the SOPC Builder system:

1. On the SOPC Builder **System Contents** tab, select the new component **pwm_avalon_interface** under the **User Logic** group in the list of available components, and click **Add**. The configuration wizard for the PWM component appears.

   If you want to, you can modify the parameters in the configuration GUI. The parameters affect the reset state of the PWM control registers, but have no affect on the outcome of the steps in this chapter.
2. Click **Finish**. You return to the SOPC Builder **System Contents** tab, and the component **pwm_avalon_interface_0** appears in the table of active components.
3. Right-click **pwm_avalon_interface_0** and choose **Rename**.
4. Type `z_pwm_0` for the component name and press **Enter**. (This name is unusual, but it minimizes effort later when you update the Quartus II design in section "Modify the Quartus II Design to Use the PWM Output" on page 10–23.

You must name the component exactly as directed, or else later steps in this chapter will fail.

5. Click **Generate** to start generating the system.

6. After system generation completes successfully, exit SOPC Builder and return to the Quartus II software.

Modify the Quartus II Design to Use the PWM Output

At this point, you have created an SOPC Builder system that uses the PWM component. Now you must update the Quartus II project to use the PWM output.

The file **standard.bdf** is the top-level Block Design File (BDF) for the Quartus II project. The BDF contains a symbol for the SOPC Builder system module, named **std_<*FPGA*>**, where **<*FPGA*>** refers to the FPGA on the target development board.

In the previous steps you added a PWM component which produces an additional output from the system module. Now you need to update the symbol for the system module, and connect the PWM output to an FPGA pin.

To complete this section, you must be familiar with the Quartus II Block Editor.

1. In the Quartus II software, open the file **standard.bdf**.

2. Right-click the symbol **std_<*FPGA*>** in the BDF and choose **Update Symbol or Block**. The Update Symbol or Block dialog appears.

3. Select **Selected Symbol(s) or Block(s)**.

4. Click **OK** to close the dialog. The symbol **std_<*FPGA*>** in the BDF is updated, and it now has an additional output port named **pwm_out_from_the_z_pwm_0**.

   SOPC Builder creates unique names for all I/O ports on the system module, by combining the signal name in the component design file with the instance name of the component in the system module.

5. Delete the symbol for pins `LEDG[7..0]` which are connected to port `out_port_from_the_led_pio[7..0]` on the system module.

   These pins connect to LEDs on the development board. This example design uses one of the LEDs to display the output of the PWM.

6. Create a new output pin named `LEDG[0]`.

7. Connect the new pin `LEDG[0]` to `pwm_out_from_the_z_pwm_0` on **std_<*FPGA*>**.

The hardware design is now ready to compile.

Compile the Hardware Design & Download to the Target Board

Perform the following steps to compile the hardware design and download it to the target board.

1. On the File menu, click **Save** to save changes to the BDF.

2. On the Processing menu, click **Start Compilation** to start compiling the hardware design. The compilation begins.

If you performed all prior steps correctly, the Quartus II compilation will finish successfully after several minutes, and generate a new FPGA configuration file for the project.

You can only perform the remaining steps in this chapter if you have a development board.

Perform the following steps to download the hardware design to the board:

1. Connect your host computer to the development board using an Altera download cable, such as the USB Blaster, and apply power to the board.

2. On the Tools menu, click **Programmer** to open the Quartus II Programmer.

3. Use the Programmer window to download the following FPGA configuration file to the board: **<*Quartus II project*>/standard.sof**.

At this point, you have completed all the steps to create a hardware design and download it to hardware.

Exercise the Hardware Using Nios II Software

The PWM example design is based on the Nios II processor. You must execute software on the Nios II processor to exercise the PWM hardware. The example design files provide a C test program that pulses an LED by

gradually modulating the PWM duty cycle. This test program accesses the hardware both by using the register map declarations directly, and by calling the driver functions.

In this section you will perform the following steps:

1. Start the Nios II IDE and create a new Nios II IDE project.
2. Build and run the C test program.
3. View the results.

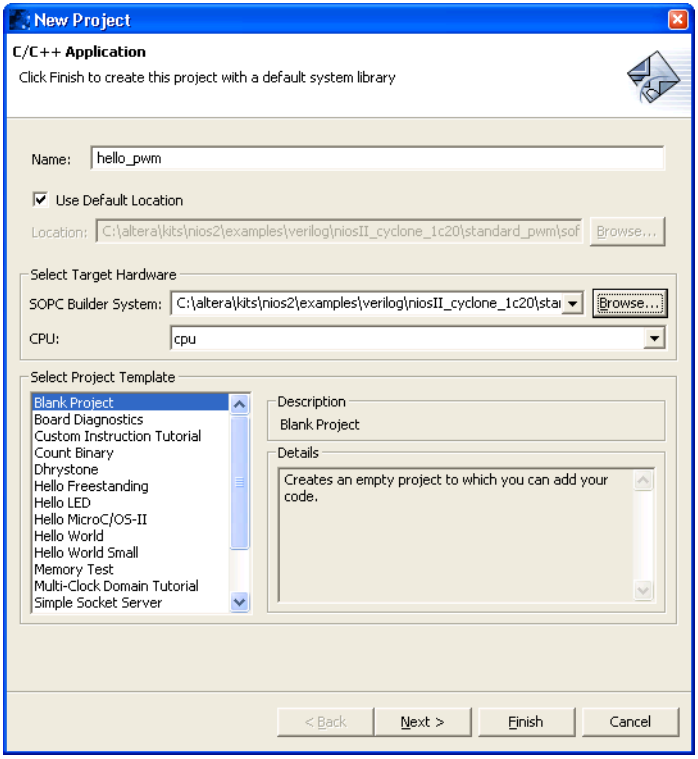
To complete this section, you must have performed all prior steps, and successfully configured the target board with the hardware design.

Start the Nios II IDE & Create a New IDE Project

Perform the following steps to start the Nios II IDE and create a new IDE project:

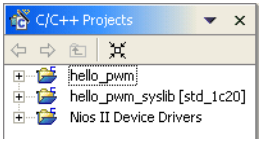
1. Start the Nios II IDE.
2. On the File menu, click **New > C/C++ Application** to start a new project. The first page of the **New Project** wizard appears.
3. Under **Select Project Template**, select **Blank Project**.
4. In the **Name** field, type `hello_pwm`.
5. Ensure that **Use Default Location** is turned on.
6. Click **Browse** under **Select Target Hardware**. The **Select Target Hardware** dialog box appears.
7. Browse to the **<*Quartus II project*>** directory.
8. Select the file **std_<*FPGA*>.ptf**.
9. Click **Open** to return to the New Project wizard. The **SOPC Builder System** and the **CPU** fields are now specified, as shown in Figure 10–8 on page 10–26.
10. Click **Finish**.

Figure 10–8. New Project Wizard



After the IDE successfully creates the new project, the C/C++ Projects view will contain two new projects, **hello_pwm** and **hello_pwm_syslib**, in addition to **Nios II Device Drivers**, as shown in Figure 10–9.

Figure 10–9. New Projects in the C/C++ Projects View



Compile the Software Project & Run on the Target Board

In this section you will compile the C test program provided with the PWM design files, and then download it to the target board.

First, perform the following steps to associate the C source file with the new C/C++ project.

1. In your computer's file system, copy the file <*PWM design files*>**/pwm_sw/test_software/hello_altera_avalon_pwm.c** to the directory **<*Quartus II project*>/software/hello_pwm/**.

2. In the Nios II IDE C/C++ Projects view, right-click **hello_pwm** and choose **Refresh**. This forces the IDE to recognize the new file in the project directory.

The project is now ready to compile and run. Perform the following steps:

1. Right-click **hello_pwm** and choose **Build Project** to compile the program. The first time you build the project, it can take a few minutes for the compilation to finish.

2. After compilation completes, select **hello_pwm** in the C/C++ Projects view.

3. On the Run menu, click **Run**. The Run dialog appears.

4. Under **Configurations** select **Nios II Hardware**, and click **New**. A new run/debug configuration named **hello_pwm Nios II HW configuration** appears.

5. If the **Run** button (in the bottom right of the Run dialog) is deactivated, perform the following steps:

    a. Click the **Target Connection** tab.

    b. Click **Refresh** next to the **JTAG cable** list.

    c. From the **JTAG cable** list, select the download cable you want to use.

    d. Click **Refresh** next to the **JTAG device** list.

6. Click **Run**.

7. View the results:

   a. The **Console** view in the IDE displays messages similar to the following:

```
Hello from the PWM test program.
The starting values in the PWM registers are:
Period = 0
Duty cycle = 0
Notice the pulsing LED on the development board.
```

   b. LED0 on the development board repeatedly pulses on and off.

Congratulations! You have finished all steps for the PWM design example.

Sharing Components

When you create a component using the component editor, SOPC Builder automatically saves the component in the current Quartus II project directory. To promote design reuse, you can use the component in different projects, and you can share your component with other designers.

Perform the following steps to share a component:

1. In your computer's file system, move the component directory to a central location, outside any particular Quartus II project's directory. For example, you could create a directory **c:\my_component_library** to store your custom components.

   The directory path name cannot contain spaces. If the path contains spaces, SOPC Builder might not be able to access the files.

2. In SOPC Builder, on the File menu, click **SOPC Builder Setup**. The **SOPC Builder Setup** dialog appears, which lets you specify where SOPC Builder searches for component files.

3. Under **Component/Kit Library Search Path**, add the path to the enclosing directory of the component directory. For example, for a component directory **c:\my_component_library\pwm_avalon_interface**, add the path **c:\my_component_library**. If there are pre-existing paths, use "+" to separate the path names.

4. Click **OK**.

11. Building Systems with Multiple Clock Domains

QII54008-6.0.0

Introduction

This chapter guides you through the process of using SOPC Builder to create a system with multiple clock domains. You will start with a ready-made design that uses a single clock domain, and modify the design to use two clocks.

Example Design Overview

The design in this chapter mimics the common scenario of a system with separate control and data paths. Typically, the control path is slow, because the controller itself is relatively slow, and it is used only in short bursts to set up data transfers. On the other hand, the data path is fast so that, after the controller initiates a transfer, data moves as quickly as possible from source to destination.

Figure 11–1 on page 11–2 shows a simplified block diagram of the system structure. In this design, a Nios® II processor acts as the controller operating at 50 MHz. A DMA controller operating at 100 MHz manages the data path, and reads and writes data buffers that also operate at 100 MHz. The figure focuses on the multi-clock nature of the system, and shows the connections between master and slave ports.

Figure 11–1. Simplified Block Diagram of the Example Design

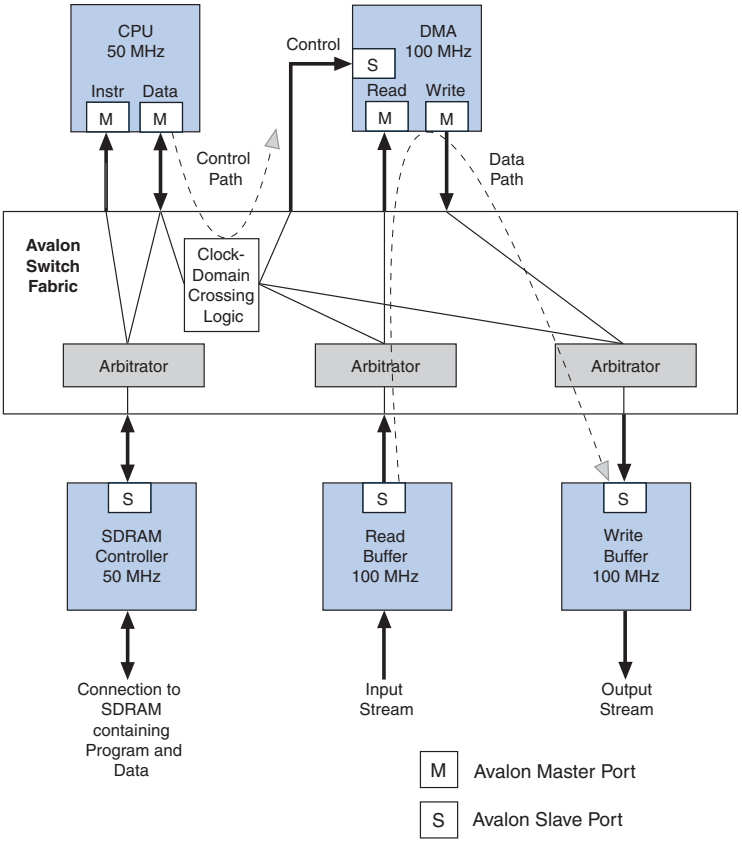


Figure 11–1 does not show example design features that are not directly related to the issue of multiple clocks, such as a JTAG UART communication peripheral and timer peripheral used by the Nios II processor.

Hardware & Software Requirements

To use the design example(s) in this chapter, you must have the following:

- Design files for the example design – A hyperlink to the design files is located with this chapter on the SOPC Builder literature page. Visit **www.altera.com/sopcbuilder**.

- Quartus® II Software version 4.2 or higher – Both Quartus II Web Edition and the fully licensed version will work with the example design.
- Nios II Embedded Design Suite (EDS) version 1.1 or higher – Both the evaluation edition and the fully licensed version will work with the example design.
- Nios development board and an Altera® USB-Blaster™ download cable (Optional) – You can use any of the following Nios development boards:

  - Stratix® II Edition
  - Stratix Edition
  - Stratix Professional Edition
  - Cyclone™ Edition

  If you do not have a development board, you can follow the hardware development steps, but you will not be able to download the complete system to a working board.

You can download the Quartus II Web Edition software and the Nios II EDS Evaluation Edition for free from the Altera Download Center at **www.altera.com**.

Before you begin, you must install the Quartus II software and Nios II EDS.

Creating the Multi-Clock Hardware System

In this section, you will start with an example hardware design provided with the Nios II EDS and create a multi-clock system. You will perform the following steps:

1. Copy the hardware design files to a new directory
2. Modify the design in SOPC Builder to create a multi-clock hardware system
3. Update the Quartus II design to use the new clock domain
4. Compile the hardware design in the Quartus II software, and download the hardware design to a target board

Copy the Hardware Design Files to a New Directory

The hardware design used in this chapter is based on the **standard** hardware example design included with the Nios II EDS. Copy the design files by performing the following steps:

1. In your host computer file system, locate the following directory:

   *<Nios II EDS install path>***examples**\<*verilog or vhdl*>\<*board version*>**standard**

   Each development board has a VHDL and Verilog version of the design. You can use either one. Table 11–1 shows the names of the directories for the available Nios development boards.

Table 11–1. Design File Directories

Nios Development Board	Tutorial Directory
Stratix II Edition	niosII_stratixII_2s60_es
Stratix Edition	niosII_stratix_1s10 or niosII_stratix_1s10_es
Stratix Professional Edition	niosII_stratix_1s40
Cyclone Edition	niosII_cyclone_1c20

   For demonstration purposes, the figures in this chapter show the case of the Verilog design on the Nios Development Board, Cyclone Edition.

2. Copy the **standard** directory to a new location. This document will refer to the newly-created directory as <*hardware files directory*>.

Modify the Design in SOPC Builder

This section walks you through the process of implementing a multi-clock system in SOPC Builder. In this section you will do the following:

1. Open the system in SOPC Builder.
2. Add a DMA controller and two 4 Kbyte on-chip memory components.
3. Connect DMA master ports to memory slave ports.
4. Make clock domain assignments.
5. Regenerate the system.

Open the System in SOPC Builder

To open the system in SOPC Builder, perform the following steps:

1. Start the Quartus II software.
2. Choose **Open Project** (File menu).
3. Browse to <*hardware files directory*>.
4. Select **standard.qpf** and click **Open**.
5. Choose **SOPC Builder** (Tools menu) to start SOPC Builder.

The SOPC Builder window appears, displaying the contents of the system, which you will use as a starting point for your design.

Add DMA Controller & Memory Components

Perform the following steps to add the DMA controller and memory components to the system:

1. In the SOPC Builder list of available components, select **DMA** in the **Other** group, and click **Add**. The DMA configuration wizard displays.
2. In the DMA configuration wizard, click **Finish** to accept the default settings. You return to the SOPC Builder **System Contents** tab which displays the new DMA component, named **dma_0**.

   Errors are displayed in the SOPC Builder messages window. You can ignore these messages for now, because you will fix the errors in later steps.
3. In the list of available components, select **On-Chip Memory (RAM or ROM)** in the **Memory** group, and click **Add**. The On-Chip Memory configuration wizard appears.
4. In the On-Chip Memory configuration wizard, click **Finish** to accept the default settings. You return to the SOPC Builder **System Contents** tab, which displays the new memory component.
5. Right-click the new memory component and choose **Rename**.
6. Type `read_buffer`↵ to rename the component.
7. Repeat steps 3 and 4 to add another On-Chip Memory component to the system.

8. Right-click the new memory component and choose **Rename**.

9. Type `write_buffer`↵ to rename the component.

You must name the DMA and memory components exactly as specified above (**dma_0, read_buffer**, and **write_buffer**). If you name the components differently, later steps will fail.

Connect DMA Master Ports to Memory Slave Ports

Now that you have added the DMA controller and the memory components to the system, you must connect their master and slave ports appropriately. Perform the following steps:

1. Hover the mouse pointer over the connections panel in the SOPC Builder **System Contents** tab to display the potential master port connections for the DMA. See Figure 11–2.

2. Connect the DMA read master port (**dma_0/read_master**) to the **read_buffer** memory.

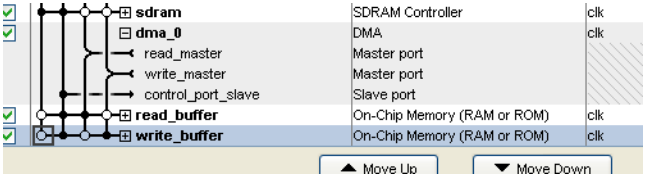
3. Connect the DMA write master port (**dma_0/write_master**) to the **write_buffer** memory.

4. Disconnect the Nios II processor instruction master (**cpu/instruction_master**) from both the on-chip memories' slave ports. For this example design, the processor does not use these memories to fetch instructions.

5. Verify that the Nios II processor data master (**cpu/data_master**) is connected to the DMA slave port (**dma/control_port_slave**).

Figure 11–2 shows the state of the connections panel after all components have been correctly connected.

Figure 11–2. Correct Connections Between Master & Slave Ports



After the DMA controller is connected properly to the on-chip memories, the error messages disappear from the SOPC Builder messages window.

Make Clock Domain Assignments

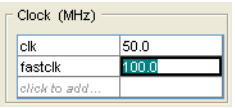
In this section you will specify a 100 MHz clock input, and assign the DMA and memory components to the new clock domain. Then you will generate the system. Perform the following steps:

1. On the **System Contents** tab under **Clock MHz**, click the cell labeled **click to add** to enter a new clock entry.

2. Type **fastclk** for the name of the new clock, as shown in Figure 11–3.

3. Type **100** for the speed of `fastclk`, as shown in Figure 11–3.

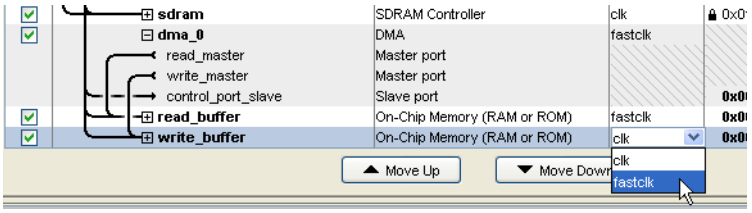
Figure 11–3. Clock Settings



4. In the **Clock** list for the DMA component, select **fastclk** to assign the 100 MHz clock to the DMA component, as shown in Figure 11–4.

5. Repeat step 4 for the **read_buffer** and **write_buffer** components, as shown in Figure 11–4.

Figure 11–4. Assigning a Different Clock to the DMA & Memory Components



6. Click **Generate** to start generating the system.

7. After system generation completes successfully, exit SOPC Builder and return to the Quartus II software.

Update the Quartus II Design

At this point, you have created an SOPC Builder system that uses multiple clock domains. In this section you will do the following:

1. Update the system module symbol.
2. Update PLL settings to generate a 100 MHz clock.
3. Connect the 100 MHz clock to the system module.
4. Compile the Design and download it to the board.

To complete this section, you must be familiar with the Quartus II Block Editor.

Update the System Module Symbol

The file **standard.bdf** is the top-level Block Diagram File (BDF) for the Quartus II project. The BDF contains a symbol for the SOPC Builder system module, named **std_<*FPGA*>**, where **<*FPGA*>** refers to the FPGA on the target development board.

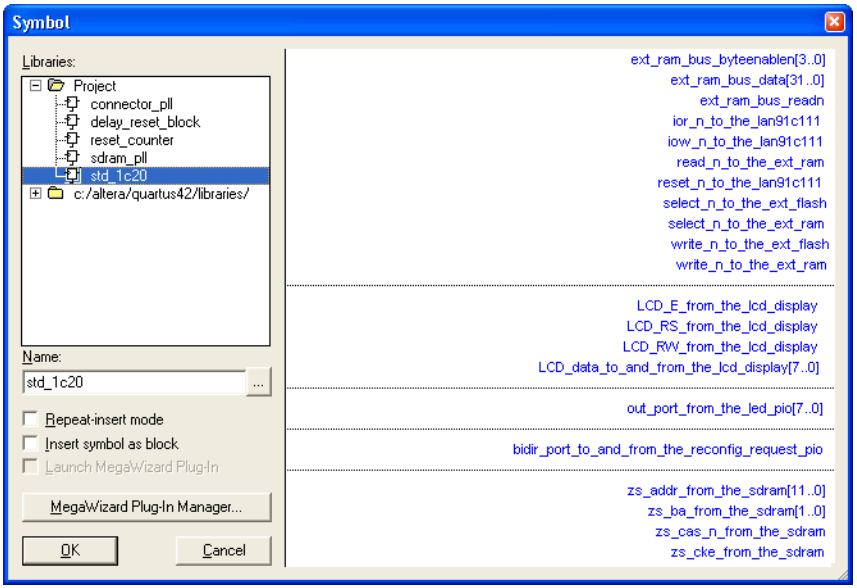
The SOPC Builder system module requires an additional clock input for the 100 MHz clock domain, and therefore you need to update the symbol for the system module. To remove the old symbol and insert an updated symbol, perform the steps below.

In the following steps you will disconnect and then reconnect all connections to the system module, including connections to FPGA pins. You must make these connections exactly, or else the design will not work in hardware, potentially damaging the development board. If possible, print the BDF as a reference to help you reconnect pins to the system module later.

1. In the BDF, select the symbol **std_<*FPGA*>** and delete it.
2. Click-and-drag to select all of the pins that previously connected to the right-hand-side of the symbol.
3. Press the right-arrow key ten times to move the pins to the right, creating space for the new symbol.
4. Double click in the space where the symbol used to be to insert a new symbol. The **Symbol** window appears.
5. Expand the **Project** folder under **Libraries**.

6. Select the **std_<*FPGA*>** symbol, and click OK. See Figure 11–5.

Figure 11–5. Selecting & Inserting the New Symbol



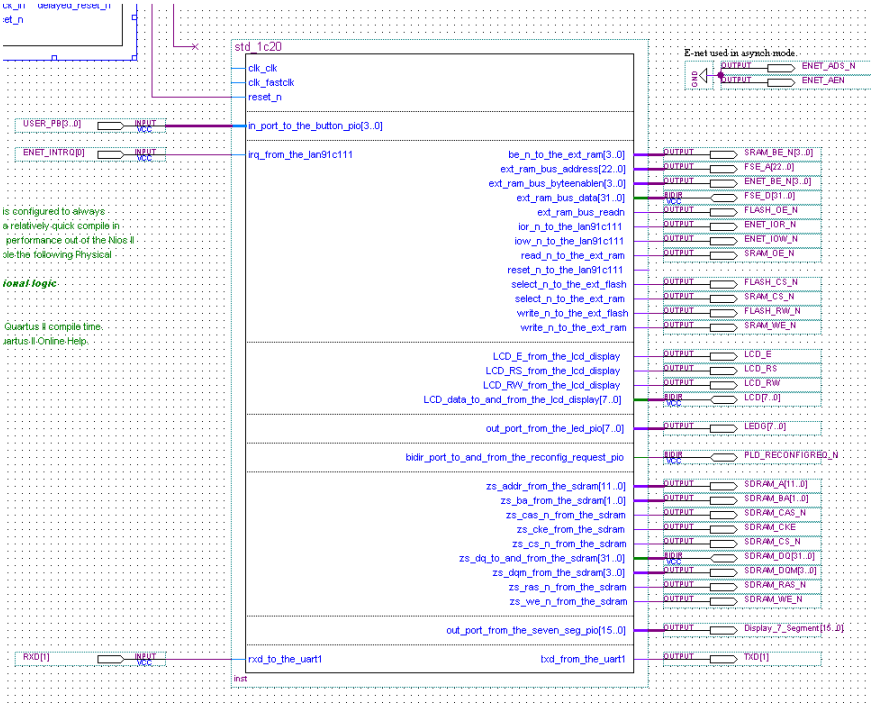
7. Move the mouse to position the symbol between the pin symbols, then click the left mouse button to place the symbol.

8. Look at the symbol, and notice the new clock input, **clk_fastclk**, and the old clock input, which is now named **clk_clk**.

9. Reconnect all previous connections to the **std_<*FPGA*>** symbol, except for the clock inputs **clk_clk** and **clk_fastclk**. You will connect the clock inputs in later steps.

Figure 11–6 shows the new symbol reconnected to all signals except for the clocks.

Figure 11–6. Updated Symbol Without Clock Connections



Update PLL Settings to Generate a 100 MHz Clock

Perform the following steps to modify the PLL instance in the BDF to generate a 100 MHz clock:

1. Locate the symbol **sdram_pll** in the BDF.

2. Right-click the symbol and select **MegaWizard® Plug-in Manager** to configure the PLL settings. The MegaWizard Plug-In Manager for the ALTCLKLOCK function displays.

   At this point, the Quartus II software might display a benign warning: `Delay shifts (time delay elements) are no longer supported in the Stratix PLLs`. If you see this message, click **OK**.

3. Click **Next** until you reach page 6 of 15 of the wizard flow, shown in Figure 11–7.

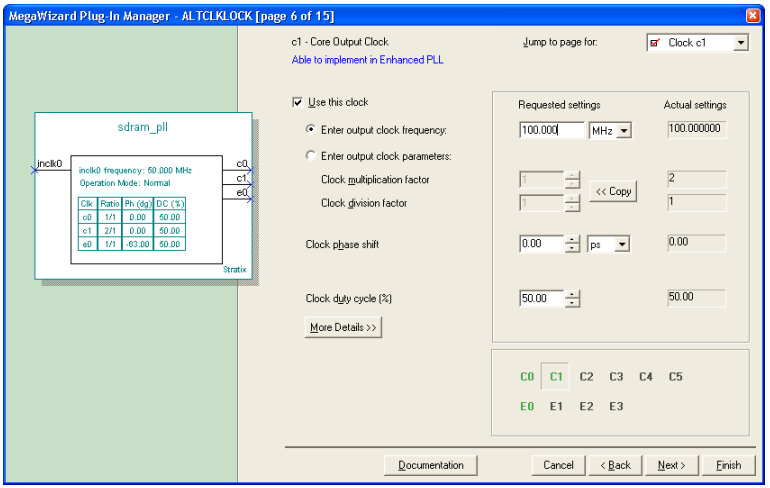
4. Click **Use this clock**.

5. Select **Enter output clock frequency**.

6. Under **Requested settings,** type `100` and select **MHz**.

Figure 11–7 shows the **ALTCLKLOCK** MegaWizard Plug-In Manager with the correct settings.

Figure 11–7. ALTCLKLOCK Settings to Generate a 100MHz Clock



7. Click **Finish** to jump to the final stage (page 15 of 15) of the wizard flow.

8. Click **Finish** again to return to the Quartus II software.

9. Right-click the **sdram_pll** symbol and choose **Update Symbol or Block**. The Update Symbol or Block dialog appears.

10. Click **OK** to update the selected instance of the symbol.

The PLL is now configured correctly to generate a 100 MHz output clock.

For further information on using the PLLs in Altera devices, see the handbook for the target device family.

Connect the 100 MHz Clock to the System Module

You now must connect the clock signals to the SOPC Builder system module. The easiest way to accomplish this is to symbolically link the PLL outputs to the system module inputs using conduit aliases. This section will guide you through the process of making one connection, and leave the remaining connections to you as an exercise.

To connect the 100 MHz clock signal from the PLL to the system module, perform the following steps:

1. Move the mouse pointer over node **c1** on **sdram_pll** until the pointer changes to a cross-hairs.
2. Click and drag right to add a conduit (i.e. a connection line) to node **c1**.
3. Click on the conduit line to select it.
4. Type `dmaclk` and press Enter.
5. Move the mouse pointer over node **clk_fastclk** on **std_<FPGA>** until the pointer changes to a cross-hairs.
6. Click and drag left to add a conduit to node **clk_fastclk**.
7. Click on the conduit line to select it.
8. Type `dmaclk` and press **Enter**.

The two nodes are now linked symbolically (by the name `dmaclk`) via a conduit alias.

Follow the instructions below to complete the remaining clock connections. Depending on which Nios development board you are targeting, the remaining PLL connections to the PLL(s) are slightly different. This section gives instructions to accommodate all Nios development boards.

Be sure to use the instructions that apply to your board, or else the design will fail in hardware.

For the Nios Development Board, Stratix II Edition, Stratix Professional Edition, and Stratix Edition, connect the PLL according to Table 11–2.

Table 11–2. PLL Connections

Node on sdram_pll	Connects to
c0	`clk_clk` on **std_<*FPGA*>**
c1	`clk_fastclk` on **std_<*FPGA*>**
e0	`PLD_CLKOUT` pin

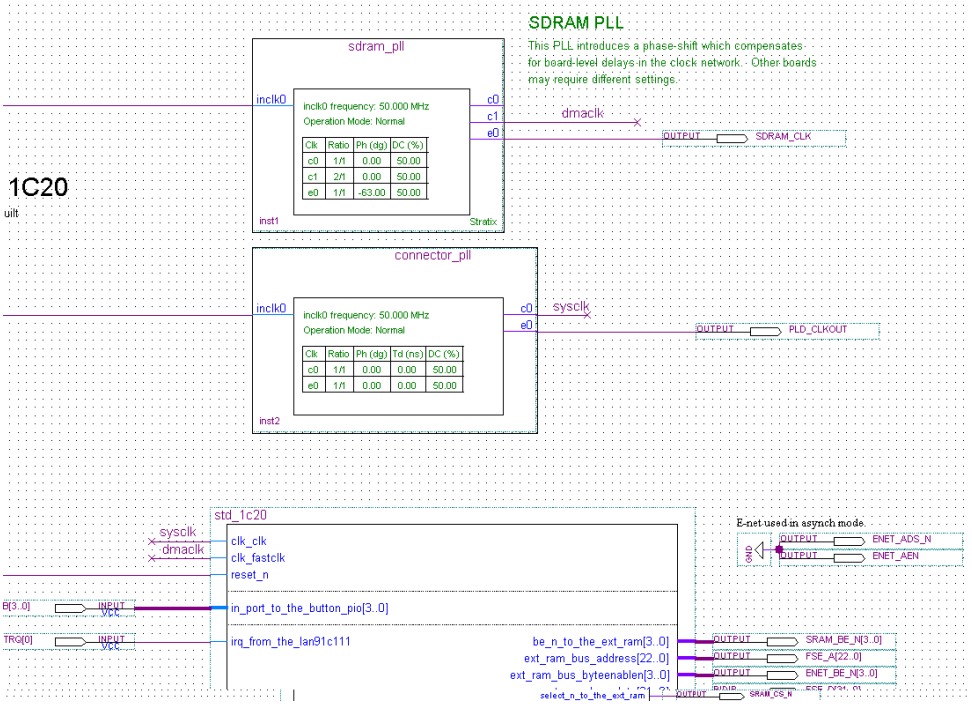
The BDF for the Nios Development Board, Cyclone Edition contains a second PLL symbol named **connector_pll** in addition to **sdram_pll**. Connect both PLLs according to Table 11–3.

Table 11–3. PLL Connections for the Nios Development Board, Cyclone Edition

Node	Connects to
c0 on **sdram_pll**	Nothing
c1 on **sdram_pll**	`clk_fastclk` on **std_<*FPGA*>**
e0 on **sdram_pll**	`SDRAM_CLK` pin
c0 on **connector_pll**	`clk_clk` on **std_<*FPGA*>**
e0 on **connector_pll**	`PLD_CLKOUT` pin

Figure 11–8 shows an example of the BDF for the Nios Development Board, Cyclone Edition with all connections completed using conduit aliases.

Figure 11–8. Symbolic Conduit Aliases Connecting PLL(s) to System Module



Compile the Design & Download to the Board

To compile the design and download it to the target board, perform the following steps:

1. Chose **Save** (File menu) to save changes to the BDF.

2. Choose **Start Compilation** (Processing menu) to start compiling the hardware design. The compilation begins.

If you performed all prior steps correctly, the Quartus II compilation will finish successfully after several minutes, and generate a new FPGA configuration file for the project.

You can only perform the remaining steps in this chapter if you have a development board.

To download the hardware design to the board, perform the following steps:

1. Connect your host computer to the development board via an Altera download cable, such as the USB Blaster.
2. Choose **Programmer** (Tools menu) to open the Quartus II Programmer.
3. Use the Programmer window to download the following FPGA configuration file to the board: **<*Hardware files directory*>\standard.sof**.

You have completed all the steps to create a multi-clock hardware design and download it to hardware. This design is based on the Nios II processor, and therefore you will have to run a software program on the processor to exercise the hardware.

Running Software to Exercise the Multi-Clock Hardware

In this section, you will run a program on the Nios II processor to exercise the multi-clock domain hardware. This program sets up and initiates a DMA transfer using the Nios II processor, and measures the time for the DMA transfer to complete.

There is nothing special about this program that makes it specific to multi-clock domain systems. Because the Avalon switch fabric abstracts the details of clock domain crossing, the Nios II processor benefits from the fast performance of the DMA controller without needing to be aware of the system clock domain properties.

You will perform the following steps:

1. Install the example software design files.
2. Create a new Nios II IDE project using the software files.
3. Build and run the program.
4. Analyze the results.

To complete this section, you must have performed all prior steps, and successfully configured the target board with your multi-clock hardware design.

Install the Example Software Design Files

In this section, you will install the example software design files on your computer. You can download the example design files from the Altera web site. Before you proceed installing the files, download the file **multi_clock.zip** associated with the URL for this chapter.

The file **multi_clock.zip** contains the following C-language source files:

- **dma_xfer.c** — Contains `main()`.
- **init.c**, **init.h** — Contain initialization routines to set up memory buffers, and initialize the timer.
- **settings_check.h** — Provides basic error checking to verify that the hardware contains the necessary DMA and memory components.

The file **multi_clock.zip** contains example software files packaged as a Nios II IDE software template. Perform the following steps to install the files:

1. Extract the contents of **multi_clock.zip** into a new directory called **multi_clock**.

2. Move the **multi_clock** directory under the following directory: **<***Nios II EDS install path***>\examples\software**

The files are packaged as a Nios II IDE template only to minimize the number of steps required for you to run the software. Using a template is not a necessary part of writing software for multi-clock domain systems. Using the template automatically provides the following functionality in the Nios II IDE, which you otherwise would have to perform manually:

1. Imports source files into a new project directory.

2. Sets up the system library settings.

3. Sets up the project settings.

Create a New Nios II IDE Project

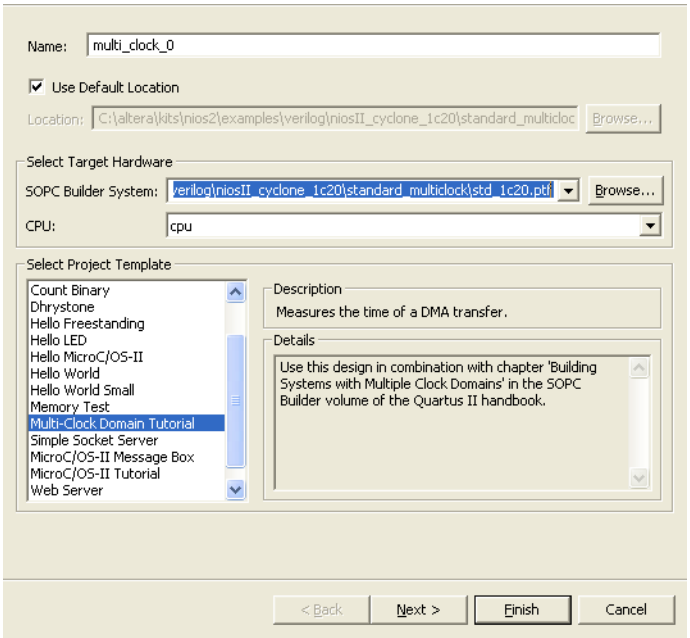
To create a new Nios II IDE project using the provided example files, perform the following steps:

1. Start the Nios II IDE.

2. Choose **New > C/C++ Application** (File menu) to start a new project. The first page of the **New Project** wizard appears.

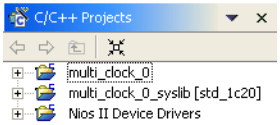
3. Under **Select Project Template**, select **Multi-Clock Domain Tutorial**.
4. Ensure that **Use Default Location** is turned on.
5. Click **Browse** under **Select Target Hardware**. The **Select Target Hardware** dialog box appears.
6. Browse to the <*hardware files directory*> directory where you created the hardware design earlier.
7. Select the file **std_<***FPGA***> .ptf**.
8. Click **Open** to return to the **New Project** wizard. The **SOPC Builder System** field is now specified and the **CPU** field now contains the name of the CPU in the system, as shown in Figure 11–9.
9. Click **Finish**.

Figure 11–9. New Project Wizard Filled in with Correct Settings



After the IDE successfully creates the new project, the **C/C++ Projects** view contains two new projects, **multi_clock_0** and **multi_clock_0_syslib**, in addition to **Nios II Device Drivers**, as shown in Figure 11–10.

Figure 11–10. New Projects Displayed in the C/C++ Projects View



Build & Run the Program

In this section, you will build the software in the Nios II IDE and run it on a development board. In short, the program does the following:

- Initializes the read and write memory buffers, filling the read memory buffer with random values.
- Performs timer initialization to accurately measure how long a DMA transaction will take.
- Sets up a DMA transaction to copy the contents of the read buffer to the write buffer.
- Starts the timer, initiates the DMA transaction, and waits for the DMA to generate an interrupt.
- Stops the timer when the DMA transaction finishes.
- Verifies that the write buffer contents are correct.
- Reports the duration of the DMA transaction.

To build and run the program, perform the following steps:

1. In the Nios II IDE C/C++ Projects view, select the **multi_clock_0** project.

2. Choose **Run As** > **Nios II Hardware** (Run menu) to build the program, download it to the board, and run it. The IDE automatically builds the program before attempting to run it. The build process can take several minutes. After the build completes, the IDE will download the program to the target board and run it.

3. View the results in the **Console** view.

The **Console** view will display results similar to the following:

```
nios2-terminal: starting in terminal mode (Control-C
exits)

Hello from Nios II!
Starting DMA transfer...

Starting a DMA transfer of 4096 bytes of data.
DMA transfer completed.
It took 34.3600006104 useconds to complete the
transfer.
Comparing send and receive buffer data...
Data Matches.

Program completed successfully.
```

See the Nios II IDE online help for more information on building and downloading projects.

In this example, the DMA achieved approximately 120 MBytes per second (4096 bytes / 34.36 usec). The source (read) and destination (write) buffer memories have zero wait states, and therefore can perform a maximum of one transfer per clock cycle. For successive 32-bit transfers at 100 MHz, the theoretical maximum DMA transfer performance is 400 MBytes per second. The 34.36 usec time includes the following processor overhead, which accounts for the difference between 400 and 120:

- Time spent in the DMA driver setting up the DMA transfer.
- Time spent in the interrupt handler after the DMA flags that it has completed the transfer.
- Time spent entering the DMA callback function to capture the finish time.

Conclusion

Congratulations! You have completed all tutorial steps in this chapter to create a multi-clock domain system with SOPC Builder and exercise the system in hardware.

Quartus II Version 6.0 Handbook

Volume 5: Altera Embedded Peripherals

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QII5V5-6.0

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Chapter 14. PLL Core with Avalon Interface

Chapter 15. Performance Counter Core with Avalon Interface

Chapter Revision Dates

The chapters in this book, *Quartus II Handbook, Volume 5*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. SDRAM Controller Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51005-6.0.0*

Chapter 2. Common Flash Interface Controller Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51013-6.0.0*

Chapter 3. EPCS Device Controller Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51012-6.0.0*

Chapter 4. DMA Controller Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51006-6.0.0*

Chapter 5. JTAG UART Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51009-6.0.0*

Chapter 6. UART Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51010-6.0.0*

Chapter 7. SPI Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51011-6.0.0*

Chapter 8. Optrex 16207 LCD Controller Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51019-6.0.0*

Chapter 9. Mutex Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51020-6.0.0*

Chapter 10. Mailbox Core with Avalon Interface
Revised: *May 2006*
Part number: *NII53001-6.0.0*

Chapter 11. PIO Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51007-6.0.0*

Chapter 12. Timer Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51008-6.0.0*

Chapter 13. System ID Core with Avalon Interface
Revised: *May 2006*
Part number: *NII51014-6.0.0*

Chapter 14. PLL Core with Avalon Interface
Revised: *May 2006*
Part number: *NII53002-6.0.0*

Chapter 15. Performance Counter Core with Avalon Interface
Revised: *May 2006*
Part number: *QII55001-6.0.0*

About This Handbook

Introduction

This volume describes intellectual property (IP) cores provided by Altera® for embedded systems design. These cores are installed with the Quartus II software, and you can use them free of charge in Altera devices. Each core is SOPC Builder ready and can be instantiated in any SOPC Builder system. Most cores provide software driver support for the Altera Nios® II processor, and work seemlessly in Nios II systems.

Each chapter provides complete reference for a core, including the following information:

- Hardware structure
- Features and interface(s) to the core
- Available options when instantiating the core in SOPC Builder
- Hardware simulation considerations, if any
- Software programming model, including a description of the registers and driver functions.
- Device & tools support

How to Contact Altera

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Information Type	USA & Canada	All Other Locations
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	(800) 800-EPLD (3753) (7:00 a.m. to 5:00 p.m. Pacific Time)	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
Non-technical customer service	(800) 767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	ftp.altera.com	ftp.altera.com

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section I. Memory Peripherals

This section describes memory components and interfaces provided by Altera®. These components provide access to on-chip or off-chip memory for SOPC Builder systems.

See *About This Handbook* for further details.

This section includes the following chapters:

- Chapter 1, SDRAM Controller Core with Avalon Interface
- Chapter 2, Common Flash Interface Controller Core with Avalon Interface
- Chapter 3, EPCS Device Controller Core with Avalon Interface
- Chapter 4, DMA Controller Core with Avalon Interface

Revision History

The following table shows the revision history for Chapters 1– 4.

Chapter(s)	Date / Version	Changes Made
1	May 2006, v6.0.0	Chapter title changed, but no change in content from previous release.
	December 2005, v5.1.1	Updated Figure 1-1. Updated sections “Off-Chip SDRAM Interface” and “Board Layout & Pinout Considerations.” Added section “Clock, PLL & Timing Considerations.”
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.

Chapter(s)	Date / Version	Changes Made
2	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	December 2004, v1.2	Added Cyclone II support.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.
3	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.
4	May 2006, v6.0.0	Chapter title changed, but no change in content from previous release.
	December 2005, v5.1.1	Changed Avalon “streaming” terminology to “flow control” based on a change to the *Avalon Interface Specification*
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	December 2004, v1.2	• Updated description of the `GO` bit. • Updated descriptions of `ioctl()` macros in table 6-2.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.

1. SDRAM Controller Core with Avalon Interface

NII51005-6.0.0

Core Overview

The SDRAM controller with Avalon® interface provides an Avalon interface to off-chip SDRAM. The SDRAM controller allows designers to create custom systems in an Altera® FPGA that connect easily to SDRAM chips. The SDRAM controller supports standard SDRAM as described in the PC100 specification.

SDRAM is commonly used in cost-sensitive applications requiring large amounts of volatile memory. While SDRAM is relatively inexpensive, control logic is required to perform refresh operations, open-row management, and other delays and command sequences. The SDRAM controller connects to one or more SDRAM chips, and handles all SDRAM protocol requirements. Internal to the FPGA, the core presents an Avalon slave port that appears as linear memory (i.e., flat address space) to Avalon master peripherals.

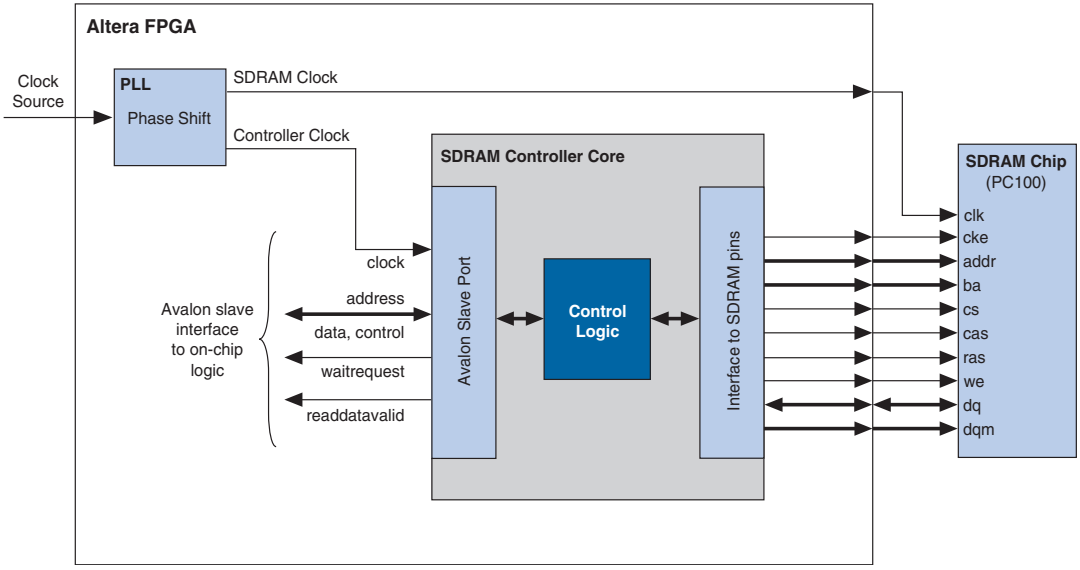
The core can access SDRAM subsystems with various data widths (8, 16, 32, or 64 bits), various memory sizes, and multiple chip selects. The Avalon interface is latency-aware, allowing read transfers to be pipelined. The core can optionally share its address and data buses with other off-chip Avalon tristate devices. This feature is valuable in systems that have limited I/O pins, yet must connect to multiple memory chips in addition to SDRAM.

The SDRAM controller with Avalon Interface is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

Functional Description

Figure 1–1 shows a block diagram of the SDRAM controller core connected to an external SDRAM chip.

Figure 1–1. SDRAM Controller with Avalon Interface Block Diagram



The following sections describe the components of the SDRAM controller core in detail. All options are specified at system generation time, and cannot be changed at run-time.

Avalon Interface

The Avalon slave port is the user-visible part of the SDRAM controller core. The slave port presents a flat, contiguous memory space as large as the SDRAM chip(s). When accessing the slave port, the details of the PC100 SDRAM protocol are entirely transparent. The Avalon interface behaves as a simple memory interface. There are no memory-mapped configuration registers.

The Avalon slave port supports peripheral-controlled wait-states for read and write transfers. The slave port stalls the transfer until it can present valid data. The slave port also supports read transfers with variable latency, enabling high-bandwidth, pipelined read transfers. When a master peripheral reads sequential addresses from the slave port, the first data returns after an initial period of latency. Subsequent reads can produce new data every clock cycle. However, data is not guaranteed to return every clock cycle, because the SDRAM controller must pause periodically to refresh the SDRAM.

See the *Avalon Interface Specification* for details on Avalon transfer types.

Off-Chip SDRAM Interface

The interface to the external SDRAM chip presents the signals defined by the PC100 standard. These signals must be connected externally to the SDRAM chip(s) via I/O pins on the Altera FPGA.

Signal Timing & Electrical Characteristics

The timing and sequencing of signals depends on the configuration of the core. The hardware designer configures the core to match the SDRAM chip chosen for the system. See "Instantiating the Core in SOPC Builder" on page 1–6 for details. The electrical characteristics of the FPGA pins depend on both the target device family and the assignments made in the Quartus® II software. Some FPGA families support a wider range of electrical standards, and therefore are capable of interfacing with a greater variety of SDRAM chips. For details, see the handbook for the target FPGA family.

Synchronizing Clock and Data Signals

The clock for the SDRAM chip (hereafter "SDRAM clock") must be driven at the same frequency as the clock for Avalon interface on the SDRAM controller (hereafter "controller clock"). Like all synchronous design, you must ensure that address, data and control signals at the SDRAM pins are stable when a clock edge arrives. As shown in Figure 1–1, you can use an on-chip phase-locked loop (PLL) to alleviate clock skew between the SDRAM controller core and the SDRAM chip. At lower clock speeds, the PLL might not be necessary. At higher clock rates, a PLL becomes necessary to ensure that the SDRAM clock toggles only when signals are stable on the pins. The PLL block is not part of the SDRAM controller core. If a PLL is necessary, you must instantiate it manually. You can instantiate the PLL Core with Avalon Interface, which is an SOPC Builder component, or instantiate an altpll megafunction outside the SOPC Builder system module.

If you use a PLL, you must tune the PLL to introduce a clock phase shift so that SDRAM clock edges arrive after synchronous signals have stabilized. See "Clock, PLL & Timing Considerations" on page 1–13 for details.

For more information on instantiating a PLL in your SOPC Builder system, refer to the *PLL Core with Avalon Interface* chapter of the *Quartus II Handbook, Volume 5: Embedded Peripherals*. The Nios® II development tools provide example hardware designs that use the SDRAM controller core in conjunction with a PLL, which you can use as a reference for your custom designs. The Nios II development tools are available free for download from **www.altera.com**.

Clock Enable (CKE) Not Supported

The SDRAM controller does not support clock-disable modes. The SDRAM controller permanently asserts the CKE signal on the SDRAM.

Sharing Pins with Other Avalon Tristate Devices

If an Avalon tristate bridge is present in the SOPC Builder system, the SDRAM controller core can share pins with the existing tristate bridge. In this case, the core's `addr`, `dq` (data) and `dqm` (byte-enable) pins are shared with other devices connected to the Avalon tristate bridge. This feature conserves I/O pins, which is valuable in systems that have multiple external memory chips (e.g., flash, SRAM, in addition to SDRAM), but too few pins to dedicate to the SDRAM chip. See "Performance Considerations" for details on how pin sharing affects performance.

Board Layout & Pinout Considerations

When making decisions about the board layout and FPGA pinout, try to minimize the skew between the SDRAM signals. For example, when assigning the FPGA pinout, group the SDRAM signals, including the SDRAM clock output, physically close together. Also, you can use the Fast Input Register and Fast Output Register logic options in the Quartus II software, which place registers for the SDRAM signals in the I/O cells. Signals driven from registers in I/O cells have similar timing characteristics, such as t_{CO}, t_{SU}, and t_{H}.

Performance Considerations

Under optimal conditions, the SDRAM controller core's bandwidth approaches one word per clock cycle. However, because of the overhead associated with refreshing the SDRAM, it is impossible to reach one word per clock cycle. Other factors affect the core's performance, as described below.

Open Row Management

SDRAM chips are arranged as multiple banks of memory, wherein each bank is capable of independent open-row address management. The SDRAM controller core takes advantage of open-row management for a single bank. Continuous reads or writes within the same row and bank will operate at rates approaching one word per clock. Applications that frequently access different destination banks will require extra management cycles for row closings and openings.

Sharing Data & Address Pins

When the controller shares pins with other tristate devices, average access time usually increases while bandwidth decreases. When access to the tristate bridge is granted to other devices, the SDRAM requires row open and close overhead cycles. Furthermore, the SDRAM controller has to wait several clock cycles before it is granted access again.

To maximize bandwidth, the SDRAM controller automatically maintains control of the tristate bridge as long as back-to-back read or write transactions continue within the same row and bank.

Note that this behavior may degrade the average access time for other devices sharing the Avalon tristate bridge.

The SDRAM controller closes an open row whenever there is a break in back-to-back transactions, or whenever a refresh transaction is required. As a result:

- The controller cannot permanently block access to other devices sharing the tristate bridge.
- The controller is guaranteed not to violate the SDRAM's row open time limit.

Hardware Design & Target FPGA

The target FPGA affects the maximum achievable clock frequency of a hardware design. Certain device families achieve higher f_{MAX} performance than other families. Furthermore, within a device family faster speed grades achieve higher performance. The SDRAM controller core can achieve 100 MHz in Altera's high-performance device families, such as Stratix® brand FPGAs. However, the core might not achieve 100 MHz performance in all Altera FPGA families.

The f_{MAX} performance also depends on the SOPC Builder system design. The SDRAM controller clock might also drive other logic in the system module, which could affect the maximum achievable frequency. For the

SDRAM controller core to achieve f_{MAX} performance of 100 MHz, all components driven by the same clock must be designed for a 100 MHz clock rate, and timing analysis in the Quartus II software must verify that the overall hardware design is capable of 100 MHz operation.

Device & Tools Support

The SDRAM Controller with Avalon Interface core supports all Altera FPGA families. Different FPGA families support different I/O standards, which may affect the ability of the core to interface to certain SDRAM chips. For details on supported I/O types, see the handbook for the target FPGA family.

Instantiating the Core in SOPC Builder

Designers use the configuration wizard for the SDRAM controller in SOPC Builder to specify hardware features and simulation features. The SDRAM controller configuration wizard has two tabs: **Memory Profile** and **Timing**. This section describes the options available on each tab.

The **Presets** list offers several pre-defined SDRAM configurations as a convenience. If the SDRAM subsystem on the target board matches one of the preset configurations, then the SDRAM controller core can be configured easily by selecting the appropriate preset value. The following preset configurations are defined:

- Micron MT8LSDT1664HG module
- Four SDR100 8 MByte x 16 chips
- Single Micron MT48LC2M32B2-7 chip
- Single Micron MT48LC4M32B2-7 chip
- Single NEC D4564163-A80 chip (64 MByte x 16)
- Single Alliance AS4LC1M16S1-10 chip
- Single Alliance AS4LC2M8S0-10 chip

Selecting a preset configuration automatically changes values on the **Memory Profile** and **Timing** tabs to match the specific configuration. Altering a configuration setting on any tab changes the **Preset** value to **custom**.

Memory Profile Tab

The **Memory Profile** tab allows designers to specify the structure of the SDRAM subsystem, such as address and data bus widths, the number of chip select signals, and the number of banks. Table 1–1 lists the settings available on the **Memory Profile** tab.

Table 1–1. Memory Profile Tab Settings

Settings		Allowed Values	Default Values	Description
Data Width		8, 16, 32, 64	32	SDRAM data bus width. This value determines the width of the `dq` bus (data) and the `dqm` bus (byte-enable).
Architecture Settings	Chip Selects	1, 2, 4, 8	1	Number of independent chip selects in the SDRAM subsystem. By using multiple chip selects, the SDRAM controller can combine multiple SDRAM chips into one memory subsystem.
	Banks	2, 4	4	Number of SDRAM banks. This value determines the width of the `ba` bus (bank address) that connects to the SDRAM. The correct value is provided in the data sheet for the target SDRAM.
Address Width Settings	Row	11, 12, 13, 14	12	Number of row address bits. This value determines the width of the `addr` bus. The Row and Column values depend on the geometry of the chosen SDRAM. For example, an SDRAM organized as 4096 (2^{12}) rows by 512 columns has a Row value of 12.
	Column	>= 8, and less than Row value	8	Number of column address bits. For example, the SDRAM organized as 4096 rows by 512 (2^{9}) columns has a Column value of 9.
Controller shares dq/dqm/addr I/O pins		Yes, No	No	When set to No, all pins are dedicated to the SDRAM chip. When set to Yes, the `addr`, `dq`, and `dqm` pins can be shared with a tristate bridge in the system. In this case, SOPC Builder presents a new configuration tab that allows the user to associate the SDRAM controller pins with a specific tristate bridge.
Include a functional memory model in the system testbench		Yes, No	Yes	When this option is turned on, SOPC Builder creates a functional simulation model for the SDRAM chip. This default memory model accelerates the process of creating and verifying systems that use the SDRAM controller. See "Hardware Simulation Considerations" on page 1–9.

Based on the settings entered on the **Memory Profile** tab, the wizard displays the expected memory capacity of the SDRAM subsystem in units of megabytes, megabits, and number of addressable words. It is useful to compare these expected values to the actual size of the chosen SDRAM to verify that the settings are correct.

Timing Tab

The **Timing** tab allows designers to enter the timing specifications of the SDRAM chip(s) used. The correct values are provided in the manufacturer's data sheet for the target SDRAM. Table 1–2 lists the settings available on the **Timing** tab.

Table 1–2. Timing Tab Settings

Settings	Allowed Values	Default Values	Description
CAS latency	1, 2, 3	3	Latency (in clock cycles) from a read command to data out.
Initialization refresh cycles	1 - 8	2	This value specifies how many refresh cycles the SDRAM controller will perform as part of the initialization sequence after reset.
Issue one refresh command every	–	15.625 µs	This value specifies how often the SDRAM controller refreshes the SDRAM. A typical SDRAM requires 4,096 refresh commands every 64 ms, which can be met by issuing one refresh command every 64 ms / 4,096 = 15.625 µs.
Delay after power up, before initialization	–	100 µs	The delay from stable clock and power to SDRAM initialization.
Duration of refresh command (t_rfc)	–	70 ns	Auto Refresh period.
Duration of precharge command (t_rp)	–	20 ns	Precharge command period.
ACTIVE to READ or WRITE delay (t_rcd)	–	20 ns	ACTIVE to READ or WRITE delay.
Access time (t_ac)	–	17 ns	Access time from clock edge. This value may depend on CAS latency.
Write recovery time (t_wr, No auto precharge)	–	14 ns	Write recovery if explicit precharge commands are issued. This SDRAM controller always issues explicit precharge commands.

Regardless of the exact timing values input by the user, the actual timing achieved for each parameter will be integer multiples of the Avalon clock. For the **Issue one refresh command every** parameter, the actual timing will be the greatest number of clock cycles that does not exceed the target

value. For all other parameters, the actual timing is the smallest number of clock ticks that provides a value greater than or equal to the target value.

Hardware Simulation Considerations

This section discusses considerations for simulating systems with SDRAM. There are three major components required for simulation:

- The simulation model for the SDRAM controller
- The simulation model for the SDRAM chip(s), also called the memory model
- A simulation testbench that wires the memory model to the SDRAM controller pins.

Some or all of these components are generated by SOPC Builder at system generation time.

SDRAM Controller Simulation Model

The SDRAM controller design files generated by SOPC Builder are suitable for both synthesis and simulation. Some simulation features are implemented in the HDL using "translate on/off" synthesis directives that make certain sections of HDL code invisible to the synthesis tool.

The simulation features are implemented primarily for easy simulation of Nios and Nios II processor systems using the ModelSim simulator. There is nothing ModelSim-specific about the SDRAM controller simulation model. However, minor changes may be required to make the model work with other simulators.

If you change the simulation directives to create a custom simulation flow, be aware that SOPC Builder overwrites existing files during system generation. Take precaution so that your changes are not overwritten.

Refer to *AN 351: Simulating Nios II Processor Designs* for a demonstration of simulation of the SDRAM controller in the context of Nios II embedded processor systems.

SDRAM Memory Model

There are two options for simulating a memory model of the SDRAM chip(s), as described below.

Using the Generic Memory Model

If the **Include a functional memory model the system testbench** option is enabled at system generation, then SOPC Builder generates an HDL simulation model for the SDRAM memory. In the auto-generated system testbench, SOPC Builder automatically wires this memory model to the SDRAM controller pins.

Using the automatic memory model and testbench accelerates the process of creating and verifying systems that use the SDRAM controller. However, the memory model is a generic functional model that does not reflect the true timing or functionality of real SDRAM chips. The generic model is always structured as a single, monolithic block of memory. For example, even for a system that combines two SDRAM chips, the generic memory model is implemented as a single entity.

Using the SDRAM Manufacturer's Memory Model

If the **Include a functional memory model the system testbench** option is not enabled, the designer is responsible for obtaining a memory model from the SDRAM manufacturer, and manually wiring the model to the SDRAM controller pins in the system test bench.

Example Configurations

The following examples show how to connect the SDRAM controller outputs to an SDRAM chip or chips. The bus labeled ctl is an aggregate of the remaining signals, such as `cas_n`, `ras_n`, `cke` and `we_n`.

Figure 1–2 shows a single 128-Mbit SDRAM chip with 32-bit data. Address, data and control signals are wired directly from the controller to the chip. The result is a 128-Mbit (16-Mbyte) memory space.

Figure 1–2. Single 128-Mbit SDRAM Chip with 32-Bit Data

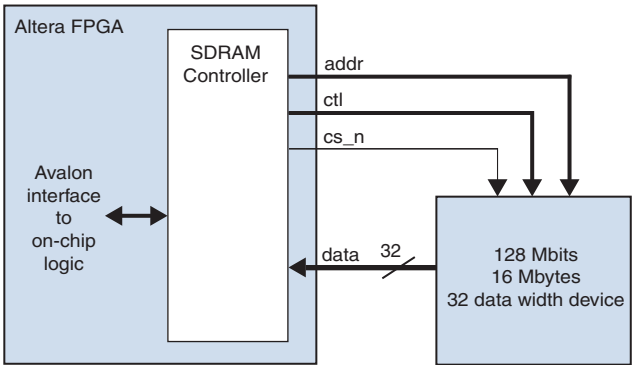


Figure 1–3 shows two 64-Mbit SDRAM chips, each with 16-bit data. Address and control signals wire in parallel to both chips. Note that chipselect (cs_n) is shared by the chips. Each chip provides half of the 32-bit data bus. The result is a logical 128-Mbit (16-Mbyte) 32-bit data memory.

Figure 1–3. Two 64-MBit SDRAM Chips Each with 16-Bit Data

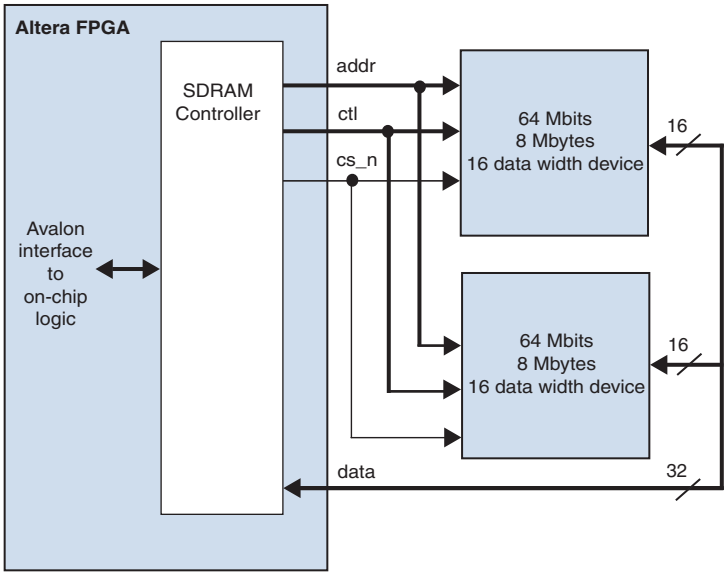
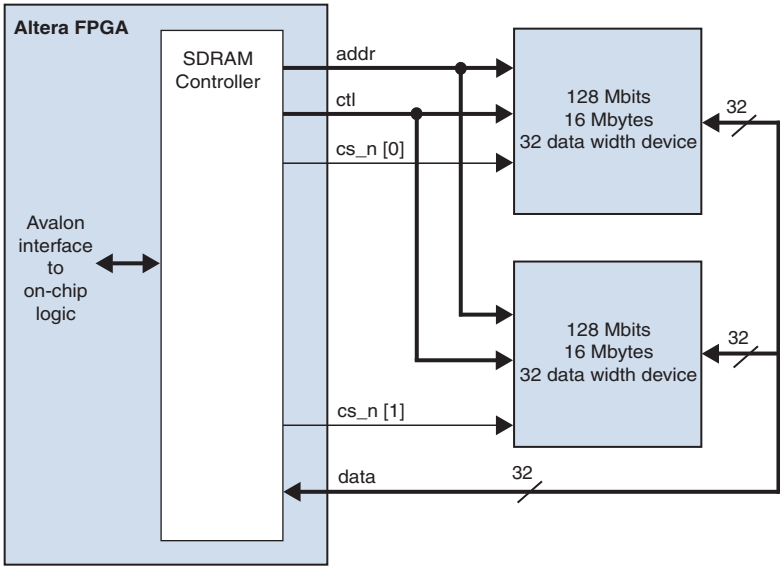


Figure 1–4 shows two 128-Mbit SDRAM chips, each with 32-bit data. Control, address and data signals wire in parallel to the two chips. The chipselect bus (`cs_n[1:0]`) determines which chip is selected. The result is a logical 256-Mbit 32-bit wide memory.

Figure 1–4. Two 128-Mbit SDRAM Chips Each with 32-Bit Data



Software Programming Model

The SDRAM controller behaves like simple memory when accessed via the Avalon interface. There are no software-configurable settings, and there are no memory-mapped registers. No software driver routines are required for a processor to access the SDRAM controller.

Clock, PLL & Timing Considerations

This section describes issues related to synchronizing signals from the SDRAM controller core with the clock that drives the SDRAM chip. During SDRAM transactions, the address, data, and control signals are valid at the SDRAM pins for a window of time, during which the SDRAM clock must toggle to capture the correct values. At slower clock frequencies, the clock naturally falls within the valid window. At higher frequencies, you must compensate the SDRAM clock to align with the valid window.

Either by calculation or by analyzing the SDRAM pins with an oscilloscope you can observe when the valid window occurs. Then you can use a PLL to adjust the phase of the SDRAM clock so that edges occur in the middle of the valid window. Tuning the PLL can require trial-and-error effort to align the phase shift to the properties of your target board.

For details on the PLL circuitry in your target device, refer to the appropriate device family handbook. For details on configuring the PLLs in Altera FPGAs, refer to the *altpll Megafunction User Guide*.

Factors Affecting SDRAM Timing

The location and duration of the window depends on several factors:

- Timing parameters of the FPGA and SDRAM I/O pins — I/O timing parameters vary based on device family and speed grade.
- Pin location on the FPGA — FPGA I/O pins connected to row routing have different timing than pins connected to column routing.
- Logic options used during the Quartus II compilation — Logic options, such as Fast Input Register and Fast Output Register, affect the design fit. The location of logic and registers inside the FPGA affects the propagation delays of signals to the I/O pins.
- SDRAM CAS latency

As a result, the valid window timing is different for different combination of FPGA and SDRAM devices. Furthermore, the window depends on the Quartus II fitting results and pin assignments.

Symptoms of an Untuned PLL

Detecting when the PLL is not tuned correctly can be difficult. Data transfers to or from the SDRAM might not fail universally. For example, individual transfers to the SDRAM controller might succeed, whereas burst transfers fail. For processor-based systems, if software can perform read or write data to SDRAM, but cannot run when the code is located in SDRAM, then the PLL is probably tuned incorrectly.

Estimating the Valid Signal Window

This section describes how to estimate the location and duration of the valid signal window using timing parameters provided in the SDRAM datasheet and the Quartus II compilation report. After finding the window, you can tune the PLL so that SDRAM clock edges occur exactly in the middle of the window.

Calculating the window is a two-step process. First you find how much the SDRAM clock can lag the controller clock, and then how much it can lead. After finding the maximum lag and lead values, you calculate the midpoint between them.

These calculations provide an estimation only. The following delays can also affect proper PLL tuning, but are not accounted for by these calculations.

- Signal skew due to delays on the printed circuit board — These calculations assume zero skew.
- Delay from the PLL clock output nodes to destinations — These calculations assume that the delay from the PLL SDRAM-clock output-node to the pin is the same as the delay from the PLL controller-clock output-node to the clock inputs in the SDRAM controller. If these clock delays are significantly different, you must account for this phase shift in your window calculations.

Figure 1–5 shows how to calculate the maximum amount that the SDRAM clock can lag the controller clock, and Figure 1–6 shows how to calculate the maximum lead. Lag is a negative time shift, relative to the controller clock, and lead is a positive time shift. The SDRAM clock can lag the controller clock by the lesser of the maximum lag for a read cycle or a write cycle. In other words, *Maximum Lag* = minimum(*Read Lag*, *Write Lag*). Similarly, the SDRAM clock can lead by the lesser of the maximum lead for a read cycle or a write cycle. In other words, *Maximum Lead* = minimum(*Read Lead*, *Write Lead*).

Figure 1–5. Calculating the Maximum SDRAM Clock Lag

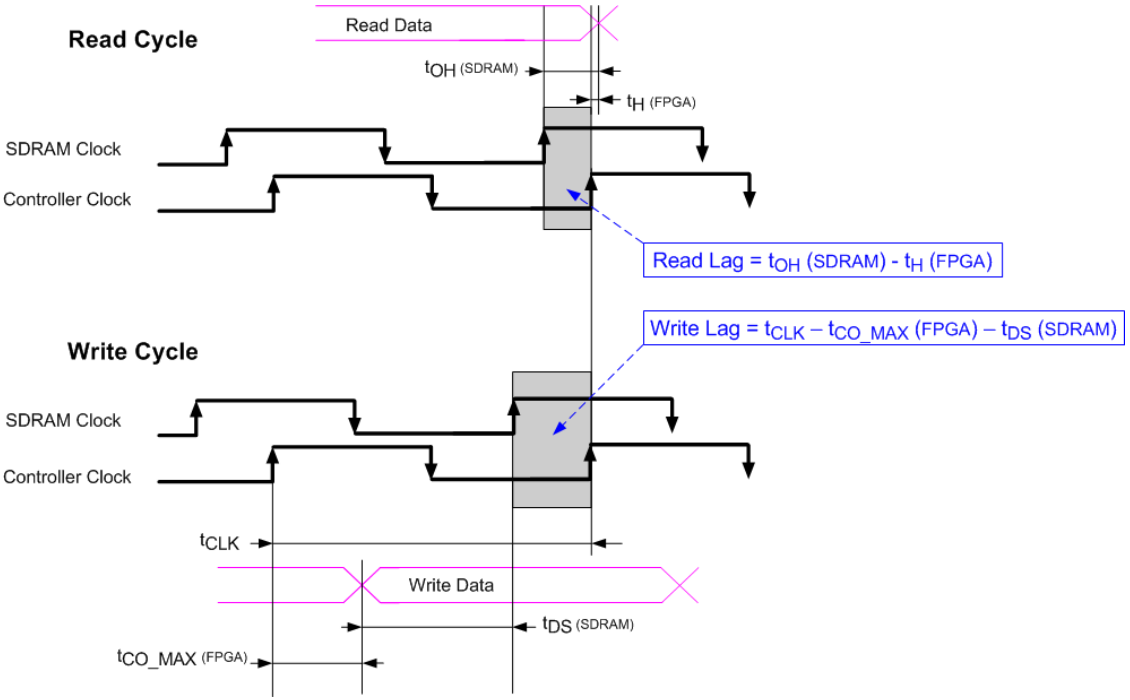
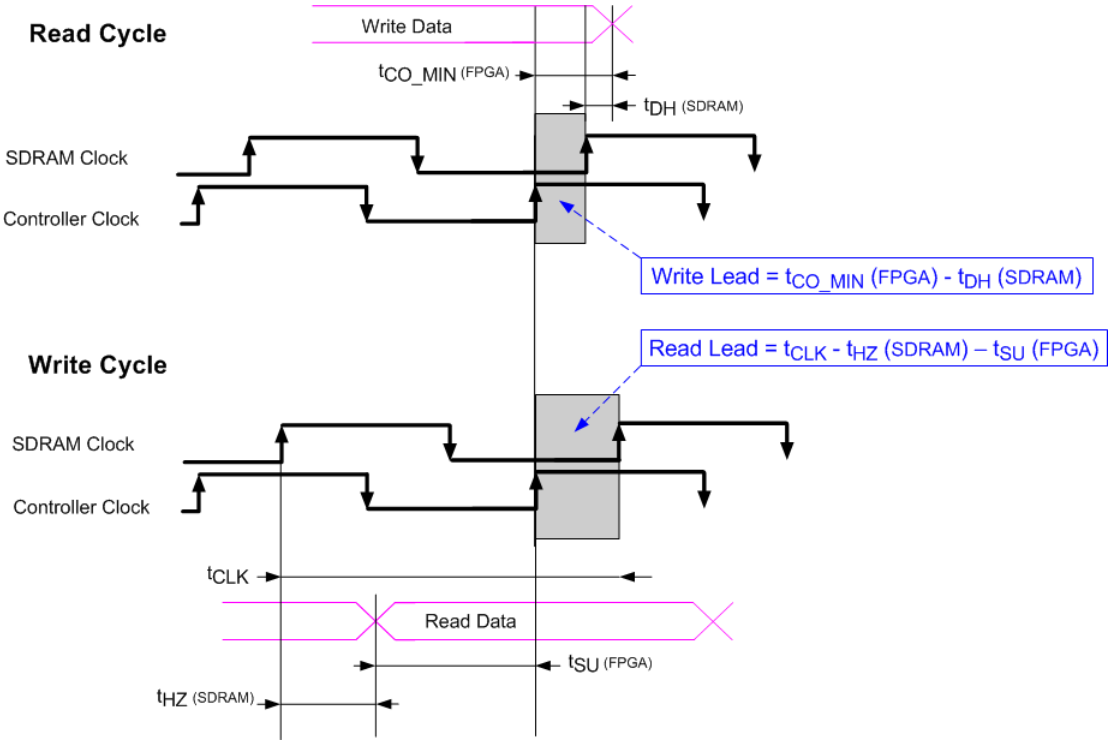


Figure 1–6. Calculating the Maximum SDRAM Clock Lead



Example Calculation

This section demonstrates an example of calculating the signal window for a Micron® MT48LC4M32B2-7 SDRAM chip and an FPGA design targeting an Altera Stratix II EP2S60F672C5 FPGA. This example uses a CAS latency (CL) of 3 cycles, and a clock frequency of 50 MHz. All SDRAM signals on the FPGA are registered in I/O cells, enabled with the Fast Input Register and Fast Output Register logic options in the Quartus II software.

Table 1–3 shows the relevant timing parameters excerpted from the MT48LC4M32B2 device datasheet.

Table 1–3. Timing Parameters for Micron MT48LC4M32B2 SDRAM Device

Parameter		Symbol	Value (ns) in -7 Speed Grade	
			Min.	Max.
Access time from CLK (pos. edge)	CL = 3	$t_{AC(3)}$		5.5
	CL = 2	$t_{AC(2)}$		8
	CL = 1	$t_{AC(1)}$		17
Address hold time		t_{AH}	1	
Address setup time		t_{AS}	2	
CLK high-level width		t_{CH}	2.75	
CLK low-level width		t_{CL}	2.75	
Clock cycle time	CL = 3	$t_{CK(3)}$	7	
	CL = 2	$t_{CK(2)}$	10	
	CL = 1	$t_{CK(1)}$	20	
CKE hold time		t_{CKH}	1	
CKE setup time		t_{CKS}	2	
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	1	
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	2	
Data-in hold time		t_{DH}	1	
Data-in setup time		t_{DS}	2	
Data-out high-impedance time	CL = 3	$t_{HZ(3)}$		5.5
	CL = 2	$t_{HZ(2)}$		8
	CL = 1	$t_{HZ(1)}$		17
Data-out low-impedance time		t_{LZ}	1	
Data-out hold time		t_{OH}	2.5	

Table 1–4 shows the relevant FPGA timing information, obtained from the Timing Analyzer section of the Quartus II Compilation Report. The values in Table 1–4 are the maximum or minimum values among all FPGA pins related to the SDRAM. The variance in timing between the SDRAM pins on the FPGA is small (less than 100 ps) because the registers for these signals are placed in the I/O cell.

Table 1–4. FPGA I/O Timing Parameters

Parameter	Symbol	Value (ns)
Clock period	t_{CLK}	20
Minimum clock-to-output time	t_{CO_MIN}	2.399
Maximum clock-to-output time	t_{CO_MAX}	2.477
Maximum hold time after clock	t_{H_MAX}	-5.607
Maximum setup time before clock	t_{SU_MAX}	5.936

You must compile the design in the Quartus II software to obtain the I/O timing information for the FPGA design. Although Altera device family datasheets contain generic I/O timing information for each device, the Quartus II Compilation Report provides the most precise timing information for your specific design.

The timing values found in the compilation report can change, depending on fitting, pin location, and other Quartus II logic settings. When you recompile the design in the Quartus II software, verify that the I/O timing has not changed significantly.

With the values from Table 1–3 and Table 1–4 you can perform the calculations from Figures 1–5 and Figures 1–6, as shown below.

The SDRAM clock can lag the controller clock by the lesser of *Read Lag* or *Write Lag*:

$$\textit{Read Lag} = t_{OH}(\text{SDRAM}) - t_{H\_MAX}(\text{FPGA})$$

$$= 2.5\text{ ns} - (-5.607\text{ ns}) = 8.107\text{ ns}$$

or

$$\textit{Write Lag} = t_{CLK} - t_{CO\_MAX}(\text{FPGA}) - t_{DS}(\text{SDRAM})$$

$$= 20\text{ ns} - 2.477\text{ ns} - 2\text{ ns} = 15.523\text{ ns}$$

The SDRAM clock can lead the controller clock by the lesser of *Read Lead* or *Write Lead*:

Read Lead = t_{CO_MIN}(FPGA) - t_{DH}(SDRAM)

= 2.399 ns - 1.0 ns = 1.399 ns

or

Write Lead = t_{CLK} - $t_{HZ(3)}$(SDRAM) - t_{SU_MAX}(FPGA)

= 20 ns - 5.5 ns - 5.936 ns = 8.564 ns

Therefore, for this example you can shift the phase of the SDRAM clock from -8.107 ns to 1.399 ns relative to the controller clock. Choosing a phase shift in the middle of this window results in the value (-8.107 + 1.399)/2 = -3.35 ns.

2. Common Flash Interface Controller Core with Avalon Interface

NII51013-6.0.0

Core Overview

The common flash interface controller core with Avalon® interface ("the CFI controller") allows you to easily connect SOPC Builder systems to external flash memory that complies with the Common Flash Interface (CFI) specification. The CFI controller is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

For the Nios® II processor, Altera provides hardware abstraction layer (HAL) driver routines for the CFI controller. The drivers provide universal access routines for CFI-compliant flash memories. Therefore, you do not need to write any additional code to program CFI-compliant flash devices. The HAL driver routines take advantage of the HAL generic device model for flash memory, which allows you to access the flash memory using the familiar HAL application programming interface (API) and/or the ANSI C standard library functions for file I/O. For details on how to read and write flash using the HAL API, refer to the *Nios II Software Developer's Handbook*.

The Nios II Embedded Design Suite (EDS) provides a flash programmer utility based on the Nios II processor and the CFI controller. The flash programmer utility can be used to program any CFI-compliant flash memory connected to an Altera® FPGA. For details, refer to the *Nios II Flash Programmer User Guide*.

Further information on the Common Flash Interface specification is available at **www.intel.com/design/flash/swb/cfi.htm**. As an example of a flash device supported by the CFI controller, see the data sheet for the AMD Am29LV065D-120R, available at **www.amd.com**.

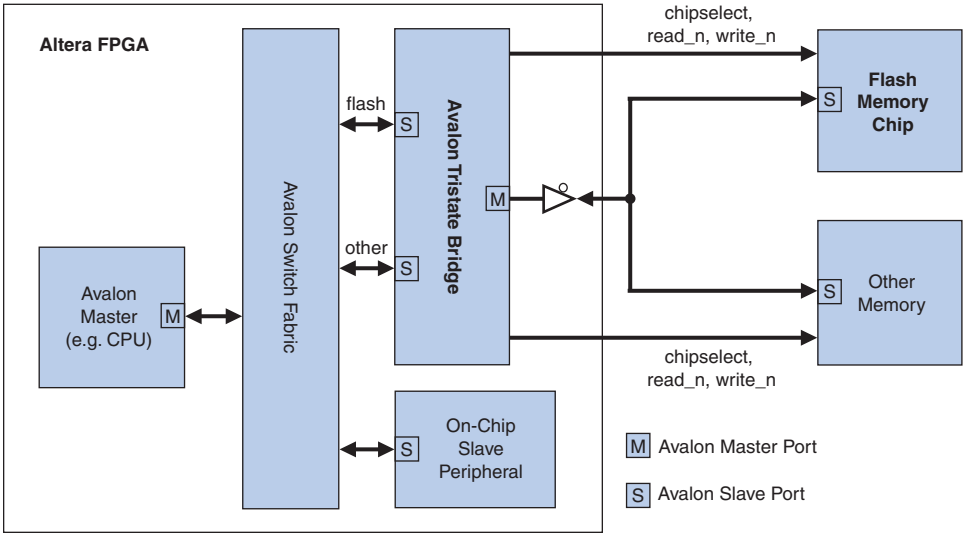
The common flash interface controller core supersedes previous Altera flash cores distributed with SOPC Builder or Nios development kits. All flash chips associated with these previous cores comply with the CFI specification, and therefore are supported by the CFI controller.

Functional Description

Figure 2–1 shows a block diagram of the CFI controller in a typical system configuration. As shown in Figure 2–1, the Avalon interface for flash devices is connected through an Avalon tristate bridge. The Avalon tristate bridge creates an off-chip memory bus that allows the flash chip to share address and data pins with other memory chips. It provides separate chipselect, read, and write pins to each chip connected to the memory bus. The CFI controller hardware is minimal: It is simply an

Avalon tristate slave port configured with waitstates, setup, and hold time appropriate for the target flash chip. This slave port is capable of Avalon tristate slave read and write transfers.

Figure 2–1. An SOPC Builder System Integrating a CFI controller



Avalon master ports can perform read transfers directly from the CFI controller's Avalon port. See "Software Programming Model" on page 2–4 for more detail on writing/erasing flash memory.

Device & Tools Support

The CFI controller supports the Stratix®, Stratix II, Cyclone™, and Cyclone II device families. The CFI controller provides drivers for the Nios II HAL system library. No software support is provided for the first-generation Nios processor.

Instantiating the Core in SOPC Builder

Hardware designers use the CFI controller's SOPC Builder configuration wizard to specify the core features. The following sections describe the available options in the configuration wizard.

Attributes Tab

The options on this tab control the basic hardware configuration of the CFI controller.

Presets Settings

The **Presets** setting is a drop-down menu of flash chips that have already been characterized for use with the CFI controller. After you select one of the chips in the **Presets** menu, the wizard updates all settings on both tabs (except for the Board Info setting) to work with the specified flash chip.

If the flash chip on your target board does not appear in the **Presets** list, you must configure the other settings manually.

Size Settings

The size setting specifies the size of the flash device. There are two settings:

- **Address Width**—The width of the flash chip's address bus.
- **Data Width—**The width of the flash chip's data bus

The size settings cause SOPC Builder to allocate the correct amount of address space for this device. SOPC Builder will automatically generate dynamic bus sizing logic that appropriately connects the flash chip to Avalon master ports of different data widths. See the *Avalon Interface Specification* for details about dynamic bus sizing.

Board Info

The **Board Info** setting is used by the flash programmer utility provided in the Nios II EDS. This setting maps a CFI controller to a known chip in a target system board component for the SOPC Builder system.

The **Reference Designator (chip label)** setting is a drop-down menu that maps the current flash component to a reference designator on the target board. This drop-down menu is only enabled if there are multiple flash chips on the target board. If all flash chips on the board are represented by other instances of the CFI controller, SOPC Builder displays an error.

For details, see the *Nios II Flash Programmer User Guide*.

Timing Tab

The options on this tab specify the timing requirements for read and write transfers with the flash device. The settings available on the Timing page are:

- **Setup**—After asserting `chipselect`, the time required before asserting the `read` or `write` signals.
- **Wait**—The time required for the `read` or `write` signals to be asserted for each transfer.
- **Hold**—After deasserting the `write` signal, the time required before deasserting the `chipselect` signal.
- **Units**—The timing units used for the **Setup**, **Wait**, and **Hold** values. Possible values include ns, us, ms, and clock cycles.

For more information about signal timing for the Avalon interface, see the *Avalon Interface Specification*.

Software Programming Model

This section describes the software programming model for the CFI controller. In general, any Avalon master in the system can read the flash chip directly as a memory device. For Nios II processor users, Altera provides HAL system library drivers that enable you to erase and write the flash memory using the HAL API functions.

HAL System Library Support

The Altera-provided driver implements a HAL flash device driver that integrates into the HAL system library for Nios II systems. Programs call the familiar HAL API functions to program CFI-compliant flash memory. You do not need to know anything about the details of the underlying drivers.

The HAL API for programming flash, including C code examples, is described in detail in the *Nios II Software Developer's Handbook*. The Nios II EDS also provides a reference design called Flash Tests that demonstrates erasing, writing, and reading flash memory.

Limitations

Currently, the Altera-provided drivers for the CFI controller support only AMD and Intel flash chips.

Software Files

The CFI controller provides the following software files. These files define the low-level access to the hardware, and provide the routines for the HAL flash device driver. Application developers should not modify these files.

- **altera_avalon_cfi_flash.h, altera_avalon_cfi_flash.c**—The header and source code for the functions and variables required to integrate the driver into the HAL system library.
- **altera_avalon_cfi_flash_funcs.h**, **altera_avalon_cfi_flash_table.c**—The header and source code for functions concerned with accessing the CFI table.
- **altera_avalon_cfi_flash_amd_funcs.h**, **altera_avalon_cfi_flash_amd.c**—The header and source code for programming AMD CFI-compliant flash chips.
- **altera_avalon_cfi_flash_intel_funcs.h**, **altera_avalon_cfi_flash_intel.c**—The header and source code for programming Intel CFI-compliant flash chips.

3. EPCS Device Controller Core with Avalon Interface

NII51012-6.0.0

Core Overview

The EPCS device controller core with Avalon® interface ("the EPCS controller") allows Nios® II systems to access an Altera® EPCS serial configuration device. Altera provides drivers that integrate into the Nios II hardware abstraction layer (HAL) system library, allowing you to read and write the EPCS device using the familiar HAL application program interface (API) for flash devices.

Using the EPCS controller, Nios II systems can:

- Store program code in the EPCS device. The EPCS controller provides a boot-loader feature that allows Nios II systems to store the main program code in an EPCS device.
- Store nonvolatile program data, such as a serial number, a NIC number, and other persistent data.
- Manage the FPGA configuration data. For example, a network-enabled embedded system can receive new FPGA configuration data over a network, and use the EPCS controller to program the new data into an EPCS serial configuration device.

The EPCS controller is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system. The flash programmer utility in the Nios II IDE allows you to manage and program data contents into the EPCS device.

For information on the EPCS serial configuration device family, see the *Serial Configuration Devices (EPCS1 & EPCS4) Data Sheet*. For details on using the Nios II HAL API to read and write flash memory, see the *Nios II Software Developer's Handbook*. For details on managing and programming the EPCS memory contents, see the *Nios II Flash Programmer User Guide*.

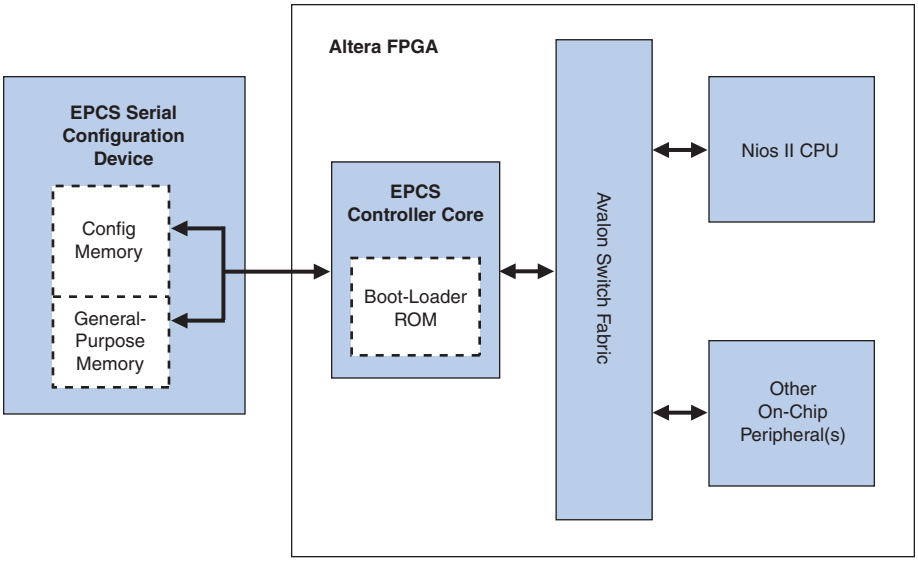
For Nios II processor users, the EPCS controller core supersedes the Active Serial Memory Interface (ASMI) device. New designs should use the EPCS controller instead of the ASMI core.

Functional Description

Figure 3–1 shows a block diagram of the EPCS controller in a typical system configuration. As shown in Figure 3–1, the EPCS device's memory can be thought of as two separate regions:

- *FPGA configuration memory*—FPGA configuration data is stored in this region.
- *General-purpose memory*—If the FPGA configuration data does not fill up the entire EPCS device, any left-over space can be used for general-purpose data and system startup code.

Figure 3–1. Nios II System Integrating an EPCS Controller



By virtue of the HAL generic device model for flash devices, accessing the EPCS device using the HAL API is the same as accessing any flash memory. The EPCS device has a special-purpose hardware interface, so Nios II programs must read and write the EPCS memory using the provided HAL flash drivers.

The EPCS controller core contains a 1 Kbyte on-chip memory for storing a boot-loader program. The Nios II processor can be configured to boot from the EPCS controller. In this case, after reset the CPU first executes code from the boot-loader ROM, which copies data from the EPCS general-purpose memory region into a RAM. Then, program control transfers to the RAM. The Nios II IDE provides facilities to compile a

program for storage in the EPCS device, and create a programming file to program into the EPCS device. See the *Nios II Flash Programmer User Guide*.

The Altera EPCS configuration device connects to the FPGA through dedicated pins on the FPGA, not through general-purpose I/O pins. Therefore, the EPCS controller core does not create any I/O ports on the top-level SOPC Builder system module. If the EPCS device and the FPGA are wired together on a board for configuration using the EPCS device (i.e. active serial configuration mode), no further connection is necessary between the EPCS controller and the EPCS device. When you compile the SOPC Builder system in the Quartus II software, the EPCS controller core signals are automatically routed to the device pins for the EPCS device.

If you program the EPCS device using the Quartus® II Programmer, all previous content is erased. To program the EPCS device with a combination of FPGA configuration data and Nios II program data, use the Nios II IDE flash programmer utility.

Avalon Slave Interface & Registers

The EPCS controller core has a single Avalon slave interface that provides access to both boot-loader code and registers that control the core. As shown in Table 3–1 on page 3–4, the first 256 words are dedicated to the boot-loader code, and the next 7 words are control and data registers. A Nios II CPU can read 256 instruction words starting from the EPCS controller's base address as flat memory space, which enables the CPU to reset into the EPCS controller's address space.

Table 3–1. EPCS Controller Register Map

Offset	Register Name	R/W	Bit Description
			31…0
0x000	Boot ROM Memory	R	Boot Loader Code
...			
0x0FF			
0x100	Read Data	R	*(1)*
0x101	Write Data	W	*(1)*
0x102	Status	R/W	*(1)*
0x103	Control	R/W	*(1)*
0x104	Reserved	-	*(1)*
0x105	Slave Enable	R/W	*(1)*
0x106	End of Packet	R/W	*(1)*

Note to Table 3–1:

(1) Altera does not publish the usage of the control and data registers. To access the EPCS device, you must use the HAL drivers provided by Altera.

Device & Tools Support

The EPCS controller supports all Altera FPGA families that support the EPCS configuration device, such as the Cyclone™ device family. The EPCS controller must be connected to a Nios II processor. The core provides drivers for HAL-based Nios II systems, and the precompiled boot loader code compatible with the Nios II processor. No software support is provided for any other processor, including the first-generation Nios.

Instantiating the Core in SOPC Builder

Hardware designers use the EPCS controller's SOPC Builder configuration wizard to specify the core features. There is only one available option in the configuration wizard.

- **Reference Designator**—This setting is a drop-down menu that allows you to select a reference designator on the current SOPC Builder target board component, which associates the current EPCS controller to the reference designator for an EPCS device on the board. If no matching reference designator is found for the target board (i.e., the board component does not declare an EPCS device),

then an EPCS controller cannot be added to the system. The reference designator is used by the Nios II IDE flash programmer. For details see the *Nios II Flash Programmer User Guide*.

Only one EPCS controller can be instantiated in each FPGA design.

Software Programming Model

This section describes the software programming model for the EPCS controller. Altera provides HAL system library drivers that enable you to erase and write the EPCS memory using the HAL API functions. Altera does not publish the usage of the cores registers. Therefore, you must use the HAL drivers provided by Altera to access the EPCS device.

HAL System Library Support

The Altera-provided driver implements a HAL flash device driver that integrates into the HAL system library for Nios II systems. Programs call the familiar HAL API functions to program the EPCS memory. You do not need to know anything about the details of the underlying drivers to use them.

The HAL API for programming flash, including C-code examples, is described in detail in the *Nios II Software Developer's Handbook*. For details on managing and programming the EPCS device contents, see the *Nios II Flash Programmer User Guide*.

Software Files

The EPCS controller provides the following software files. These files provide low-level access to the hardware and drivers that integrate into the Nios II HAL system library. Application developers should not modify these files.

- **altera_avalon_epcs_flash_controller.h**, **altera_avalon_epcs_flash_controller.c**—Header and source files that define the drivers required for integration into the HAL system library.
- **epcs_commands.h**, **epcs_commands.c**—Header and source files that directly control the EPCS device hardware to read and write the device. These files also rely on the Altera SPI core drivers.

4. DMA Controller Core with Avalon Interface

NII51006-6.0.0

Core Overview

The Direct Memory Access (DMA) controller with Avalon® interface ("the DMA controller") performs bulk data transfers, reading data from a source address range and writing the data to a different address range. An Avalon master peripheral, such as a CPU, can offload memory transfer tasks to the DMA controller. While the DMA controller performs memory transfers, the master is free to perform other tasks in parallel.

The DMA controller transfers data as efficiently as possible, reading and writing data at the maximum pace allowed by the source or destination. The DMA controller is capable of performing Avalon transfers with flow control, enabling it to automatically transfer data to or from a slow peripheral with flow control (e.g., a universal asynchronous receiver/transmitter [UART]), at the maximum pace allowed by the peripheral.

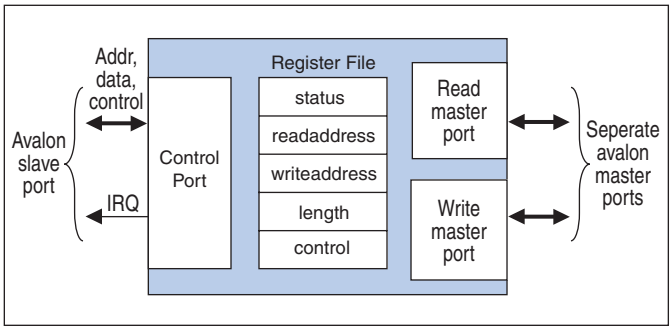
The DMA controller is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system. For the Nios® II processor, device drivers are provided in the HAL system library. See "Software Programming Model" on page 4–5 for details of HAL support.

Functional Description

The DMA controller is used to perform direct memory-access data transfers from a source address-space to a destination address-space. The source and destination may be either an Avalon slave peripheral (i.e., a constant address) or an address range in memory. The DMA controller can be used in conjunction with peripherals with flow control, which allows data transactions of fixed or variable length. The DMA controller can signal an interrupt request (IRQ) when a DMA transaction completes. This document defines a transaction as a sequence of one or more Avalon transfers initiated by the DMA controller core.

The DMA controller has two Avalon master ports—a master read port and a master write port—and one Avalon slave port for controlling the DMA as shown in Figure 4–1.

Figure 4–1. DMA Controller Block Diagram



A typical DMA transaction proceeds as follows:

1. A CPU prepares the DMA controller for a transaction by writing to the control port.

2. The CPU enables the DMA controller. The DMA controller then begins transferring data without additional intervention from the CPU. The DMA's master read port reads data from the read address, which may be a memory or a peripheral. The master write port writes the data to the destination address, which can also be a memory or peripheral. A shallow FIFO buffers data between the read and write ports.

3. The DMA transaction ends when a specified number of bytes are transferred (i.e., a fixed-length transaction), or an end-of-packet signal is asserted by either the sender or receiver (i.e., a variable-length transaction). At the end of the transaction, the DMA controller generates an interrupt request (IRQ) if it was configured by the CPU to do so.

4. During or after the transaction, the CPU can determine if a transaction is in progress, or if the transaction ended (and how) by examining the DMA controller's status register.

Setting Up DMA Transactions

An Avalon master peripheral sets up and initiates DMA transactions by writing to registers via the control port. The master peripheral configures the following options:

- Read (source) address location
- Write (destination) address location

- Size of the individual transfers: Byte (8-bit), halfword (16-bit), word (32-bit), doubleword (64-bit) or quadword (128-bit)
- Enable interrupt upon end of transaction
- Enable source or destination to end the DMA transaction with end-of-packet signal
- Specify whether source and destination are memory or peripheral

The master peripheral then sets a bit in the `control` register to initiate the DMA transaction.

The Master Read & Write Ports

The DMA controller reads data from the source address through the master read port, and then writes to the destination address through the master write port. There is a shallow FIFO buffer between the master read and write ports. The default depth is 2, which makes the write action depend on the data-available status of the FIFO, rather than on the status of the master read port.

Both the read and write master ports are capable of performing Avalon transfers with flow control, which allows the slave peripheral to control the flow of data and terminate the DMA transaction.

For details on flow control in Avalon data transfers and Avalon peripherals, see the *Avalon Interface Specification*.

Address Incrementing

When accessing memory, the read (or write) address increments by 1, 2, 4, 8 or 16 after each access, depending on the width of the data. On the other hand, a typical peripheral device (such as UART) has fixed register locations. In this case, the read/write address is held constant throughout the DMA transaction.

The rules for address incrementing are, in order of priority:

- If the `control` register's `RCON` (or `WCON`) bit is set, the read (or write) increment value is 0.
- Otherwise, the read and write increment values are set according to the transfer size specified in the control register, as shown in Table 4–1.

Table 4–1. Address Increment Values

Transfer Width	Increment
byte	1
halfword	2
word	4
doubleword	8
quadword	16

Instantiating the Core in SOPC Builder

Designers use the DMA controller's SOPC Builder configuration wizard to specify hardware options for the target system. Instantiating the DMA controller in SOPC Builder creates one slave port and two master ports. The designer must specify which slave peripherals can be accessed by the read and write master ports. Likewise, the designer must specify which other master peripheral(s) can access the DMA control port and initiate DMA transactions. The DMA controller does not export any signals to the top level of the system module.

The configurable hardware features are described below.

DMA Parameters (Basic)

The following sections describe the basic parameters.

Width of the DMA Length Register

This option sets the minimum width of the DMA's transaction length register. The acceptable range is 1 to 32. The `length` register determines the maximum number of transfers possible in a single DMA transaction.

By default, the length register is wide enough to span any of the slave peripherals mastered by the read or write ports. Overriding the length register may be necessary if the DMA master port (read or write) masters only data peripherals, such as a UART. In this case, the address span of each slave is small, but a larger number of transfers may be desired per DMA transaction.

Construct FIFO from Registers vs. Construct FIFO from Memory Blocks

This option controls the implementation of the FIFO buffer between the master read and write ports. When **Construct FIFO from Registers** is selected (the default), the FIFO is implemented using one register per storage bit. This has a strong impact on logic utilization when the DMA controller's data width is large (see "Advanced Options" on page 4–5). When **Construct FIFO from Memory Blocks** is selected, the FIFO is implemented using embedded memory blocks available in the FPGA.

Advanced Options

This section describes the advanced options.

Allowed Transactions

The designer can choose the transfer data width(s) supported by the DMA controller hardware. The following data-width options can be enabled or disabled:

- Byte
- Halfword (two bytes)
- Word (four bytes)
- Doubleword (eight bytes)
- Quadword (sixteen bytes)

Disabling unnecessary transfer widths reduces the amount of on-chip logic resources consumed by the DMA controller core. For example, if a system has both 16-bit and 32-bit memories, but the DMA controller will only transfer data to the 16-bit memory, then 32-bit transfers could be disabled to conserve logic resources.

Software Programming Model

This section describes the programming model for the DMA controller, including the register map and software declarations to access the hardware. For Nios II processor users, Altera provides HAL system library drivers that enable you to access the DMA controller core using the HAL API for DMA devices.

HAL System Library Support

The Altera-provided driver implements a HAL DMA device driver that integrates into the HAL system library for Nios II systems. HAL users should access the DMA controller via the familiar HAL API, rather than accessing the registers directly.

If your program uses the HAL device driver to access the DMA controller, accessing the device registers directly will interfere with the correct behavior of the driver.

The HAL DMA driver provides both ends of the DMA process; the driver registers itself as both a receive channel (alt_dma_rxchan) and a transmit channel (alt_dma_txchan). The *Nios II Software Developer's Handbook* provides complete details of the HAL system library and the usage of DMA devices.

ioctl() Operations

`ioctl()` operation requests are defined for both the receive and transmit channels, which allows you to control the hardware-dependent aspects of the DMA controller. Two `ioctl()` functions are defined for the receiver driver and the transmitter driver: `alt_dma_rxchan_ioctl()` and `alt_dma_txchan_ioctl()`. Table 4–2 lists the available operations. These are valid for both the transmit and receive channels.

Table 4–2. Operations for alt_dma_rxchan_ioctl() & alt_dma_txchan_ioctl()

Request	Meaning
`ALT_DMA_SET_MODE_8`	Transfers data in units of 8 bits. The value of "arg" is ignored.
`ALT_DMA_SET_MODE_16`	Transfers data in units of 16 bits. The value of "arg" is ignored.
`ALT_DMA_SET_MODE_32`	Transfers data in units of 32 bits. The value of "arg" is ignored.
`ALT_DMA_SET_MODE_64`	Transfers data in units of 64 bits. The value of "arg" is ignored.
`ALT_DMA_SET_MODE_128`	Transfers data in units of 128 bits. The value of "arg" is ignored.
`ALT_DMA_RX_ONLY_ON` *(1)*	Sets a DMA receiver into streaming mode. In this case, data is read continuously from a single location. The "arg" parameter specifies the address to read from.
`ALT_DMA_RX_ONLY_OFF` *(1)*	Turns off streaming mode for a receive channel. The value of "arg" is ignored.
`ALT_DMA_TX_ONLY_ON` *(1)*	Sets a DMA transmitter into streaming mode. In this case, data is written continuously to a single location. The "arg" parameter specifies the address to write to.
`ALT_DMA_TX_ONLY_OFF` *(1)*	Turns off streaming mode for a transmit channel. The value of "arg" is ignored.

Note to Table 4–2:

(1) These macro names changed in version 1.1 of the Nios II Embedded Design Suite (EDS). The old names (`ALT_DMA_TX_STREAM_ON`, `ALT_DMA_TX_STREAM_OFF`, `ALT_DMA_RX_STREAM_ON`, and `ALT_DMA_RX_STREAM_OFF`) are still valid, but new designs should use the new names.

Limitations

Currently the Altera-provided drivers do not support 64-bit and 128-bit DMA transactions.

This function is not thread safe. If you want to access the DMA controller from more than one thread then you should use a semaphore or mutex to ensure that only one thread is executing within this function at any time.

Software Files

The DMA controller is accompanied by the following software files. These files define the low-level interface to the hardware. Application developers should not modify these files.

- **altera_avalon_dma_regs.h**—This file defines the core's register map, providing symbolic constants to access the low-level hardware. The symbols in this file are used only by device driver functions.
- **altera_avalon_dma.h**, **altera_avalon_dma.c**—These files implement the DMA controller's device driver for the HAL system library.

Register Map

Programmers using the HAL API never access the DMA controller hardware directly via its registers. In general, the register map is only useful to programmers writing a device driver.

The Altera-provided HAL device driver accesses the device registers directly. If you are writing a device driver, and the HAL driver is active for the same device, your driver will conflict and fail to operate.

Table 4–3 shows the register map for the DMA controller. Device drivers control and communicate with the hardware through five memory-mapped 32-bit registers.

Table 4–3. DMA Controller Register Map

Offset	Register Name	Read/Write	31. . .11	10	9	8	7	6	5	4	3	2	1	0
0	status *(1)*	RW	*(2)*							LEN	WEOP	REOP	BUSY	DONE
1	readaddress	RW	Read master start address											
2	writeaddress	RW	Write master start address											
3	length	RW	DMA transaction length (in bytes)											
4		-	Reserved *(3)*											
5		-	Reserved *(3)*											
6	control	RW	*(2)*	*(4)*	*(5)*	WCON	RCON	LEEN	WEEN	REEN	I_EN	GO	WORD	HW	BYTE
7		-	Reserved *(3)*											

Notes:
(1) Writing zero to the status register clears the LEN, WEOP, REOP, and DONE bits.
(2) These bits are reserved. Read values are undefined. Write zero.
(3) This register is reserved. Read values are undefined. The result of a write is undefined.
(4) QUADWORD.
(5) DOUBLEWORD.

status Register

The status register consists of individual bits that indicate conditions inside the DMA controller. The status register can be read at any time. Reading the status register does not change its value.

The status register bits are shown in Table 4–4.

Table 4–4. status Register Bits (Part 1 of 2)

Bit Number	Bit Name	Read/Write/Clear	Description
0	DONE	R/C	A DMA transaction is completed. The DONE bit is set to 1 when an end of packet condition is detected or the specified transaction length is completed. Write zero to the status register to clear the DONE bit.
1	BUSY	R	The BUSY bit is 1 when a DMA transaction is in progress.

Table 4–4. status Register Bits (Part 2 of 2)

Bit Number	Bit Name	Read/Write/Clear	Description
2	REOP	R	The REOP bit is 1 when a transaction is completed due to an end-of-packet event on the read side.
3	WEOP	R	The WEOP bit is 1 when a transaction is completed due to an end of packet event on the write side.
4	LEN	R	The LEN bit is set to 1 when the length register decrements to zero.

readaddress Register

The `readaddress` register specifies the first location to be read in a DMA transaction. The `readaddress` register width is determined at system generation time. It is wide enough to address the full range of all slave ports mastered by the read port.

writeaddress Register

The `writeaddress` register specifies the first location to be written in a DMA transaction. The `writeaddress` register width is determined at system generation time. It is wide enough to address the full range of all slave ports mastered by the write port.

length Register

The `length` register specifies the number of bytes to be transferred from the read port to the write port. The `length` register is specified in bytes. For example, the value must be a multiple of 4 for word transfers, and a multiple of 2 for halfword transfers.

The `length` register is decremented as each data value is written by the write master port. When `length` reaches 0 the `LEN` bit is set. The `length` register does not decrement below 0.

The length register width is determined at system generation time. It is at least wide enough to span any of the slave ports mastered by the read or write master ports, and it can be made wider if necessary.

control Register

The control register is composed of individual bits that control the DMA's internal operation. The control register's value can be read at any time. The control register bits determine which, if any, conditions of the DMA transaction result in the end of a transaction and an interrupt request.

The control register bits are shown in Table 4–5.

Table 4–5. control Register Bits

Bit Number	Bit Name	Read/Write/Clear	Description
0	BYTE	RW	Specifies byte transfers.
1	HW	RW	Specifies halfword (16-bit) transfers.
2	WORD	RW	Specifies word (32-bit) transfers.
3	GO	RW	Enables DMA transaction. When the GO bit is set to 0, the DMA is prevented from executing transfers. When the GO bit is set to 1 and the length register is non-zero, transfers occur.
4	I_EN	RW	Enables interrupt requests (IRQ). When the I_EN bit is 1, the DMA controller generates an IRQ when the status register's DONE bit is set to 1. IRQs are disabled when the I_EN bit is 0.
5	REEN	RW	Ends transaction on read-side end-of-packet. When the REEN bit is set to 1, a slave port with flow control on the read side may end the DMA transaction by asserting its end-of-packet signal.
6	WEEN	RW	Ends transaction on write-side end-of-packet. When the WEEN bit is set to 1, a slave port with flow control on the write side may end the DMA transaction by asserting its end-of-packet signal.
7	LEEN	RW	Ends transaction when the `length` register reaches zero. When the LEEN bit is 1, the DMA transaction ends when the `length` register reaches 0. When this bit is 0, `length` reaching 0 does not cause a transaction to end. In this case, the DMA transaction must be terminated by an end-of-packet signal from either the read or write master port.
8	RCON	RW	Reads from a constant address. When RCON is 0, the read address increments after every data transfer. This is the mechanism for the DMA controller to read a range of memory addresses. When RCON is 1, the read address does not increment. This is the mechanism for the DMA controller to read from a peripheral at a constant memory address. For details, see "Address Incrementing" on page 4–3.
9	WCON	RW	Writes to a constant address. Similar to the RCON bit, when WCON is 0 the write address increments after every data transfer; when WCON is 1 the write address does not increment. For details, see "Address Incrementing" on page 4–3.
10	DOUBLEWORD	RW	Specifies doubleword transfers.
11	QUADWORD	RW	Specifies quadword transfers.

The data width of DMA transactions is specified by the BYTE, HW, WORD, DOUBLEWORD, and QUADWORD bits. Only one of these bits can be set at a time. If more than one of the bits is set, the DMA controller behavior is undefined. The width of the transfer is determined by the narrower of the two slaves read and written. For example, a DMA transaction that reads from a 16-bit flash memory and writes to a 32-bit on-chip memory requires a halfword transfer. In this case, HW must be set to 1, and BYTE, WORD, DOUBLEWORD, and QUADWORD must be set to 0.

To successfully perform transactions of a specific width, that width must be enabled in hardware using the **Allowed Transaction** hardware option. For example, the DMA controller behavior is undefined if quadword transfers are disabled in hardware, but the QUADWORD bit is set during a DMA transaction.

Interrupt Behavior

The DMA controller has a single IRQ output that is asserted when the `status` register's DONE bit equals 1 and the control register's I_EN bit equals 1.

Writing the `status` register clears the DONE bit and acknowledges the IRQ. A master peripheral can read the `status` register and determine how the DMA transaction finished by checking the LEN, REOP, and WEOP bits.

Section II. Communication Peripherals

This section describes communication peripherals provided by Altera®. These components provide communication interfaces for SOPC Builder systems.

See *About This Handbook* for further details.

This section includes the following chapters:

- Chapter 5, JTAG UART Core with Avalon Interface
- Chapter 6, UART Core with Avalon Interface
- Chapter 7, SPI Core with Avalon Interface

Revision History

The table below shows the revision history for Chapters 5–7.

Chapter(s)	Date / Version	Changes Made
5	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	December 2004, v1.2	Added Cyclone II support.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.
6	May 2006, v6.0.0	No change from previous release.
	December 2005, v5.1.1	Changed Avalon “streaming” terminology to “flow control” based on a change to the *Avalon Interface Specification.*
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	September 2004, v1.1	Updates for Nios II 1.01 release.
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Chapter(s)	Date / Version	Changes Made
7	May 2006, v6.0.0	No change from previous release.
	December 2005, v5.1.1	Changed Avalon ""streaming" terminology to "flow control" based on a change to the *Avalon Interface Specification*.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.

5. JTAG UART Core with Avalon Interface

NII51009-6.0.0

Core Overview

The JTAG universal asynchronous receiver/transmitter (UART) core with Avalon® interface implements a method to communicate serial character streams between a host PC and an SOPC Builder system on an Altera® FPGA. In many designs, the JTAG UART core eliminates the need for a separate RS-232 serial connection to a host PC for character I/O. The core provides a simple register-mapped Avalon interface that hides the complexities of the JTAG interface from embedded software programmers. Master peripherals (such as a Nios® II processor) communicate with the core by reading and writing control and data registers.

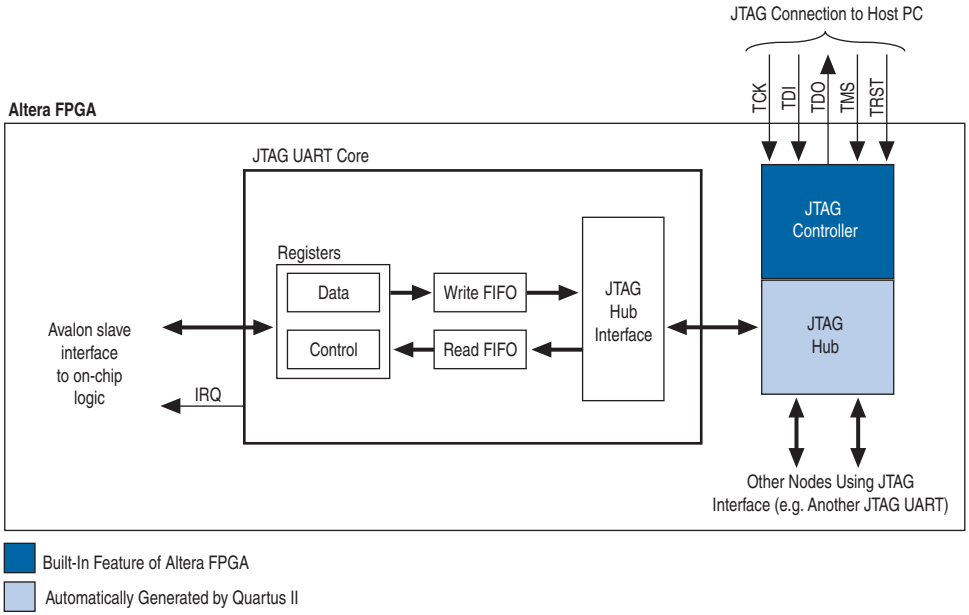
The JTAG UART core uses the JTAG circuitry built in to Altera FPGAs, and provides host access via the JTAG pins on the FPGA. The host PC can connect to the FPGA via any Altera JTAG download cable, such as the USB-Blaster™ cable. Software support for the JTAG UART core is provided by Altera. For the Nios II processor, device drivers are provided in the HAL system library, allowing software to access the core using the ANSI C Standard Library **stdio.h** routines. For the host PC, Altera provides JTAG terminal software that manages the connection to the target, decodes the JTAG data stream, and displays characters on screen.

The JTAG UART core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

Functional Description

Figure 5–1 shows a block diagram of the JTAG UART core and its connection to the JTAG circuitry inside an Altera FPGA. The following sections describe the components of the core.

Figure 5–1. JTAG UART Core Block Diagram



Avalon Slave Interface & Registers

The JTAG UART core provides an Avalon slave interface to the JTAG circuitry on an Altera FPGA. The user-visible interface to the JTAG UART core consists of two 32-bit registers, `data` and `control`, that are accessed through an Avalon slave port. An Avalon master, such as a Nios II processor, accesses the registers to control the core and transfer data over the JTAG connection. The core operates on 8-bit units of data at a time; eight bits of the `data` register serve as a one-character payload.

The JTAG UART core provides an active-high interrupt output that can request an interrupt when read data is available, or when the write FIFO is ready for data. For further details see "Interrupt Behavior" on page 5–13.

Read & Write FIFOs

The JTAG UART core provides bidirectional FIFOs to improve bandwidth over the JTAG connection. The FIFO depth is parameterizable to accommodate the available on-chip memory. The FIFOs can be constructed out of memory blocks or registers, allowing designers to trade off logic resources for memory resources, if necessary.

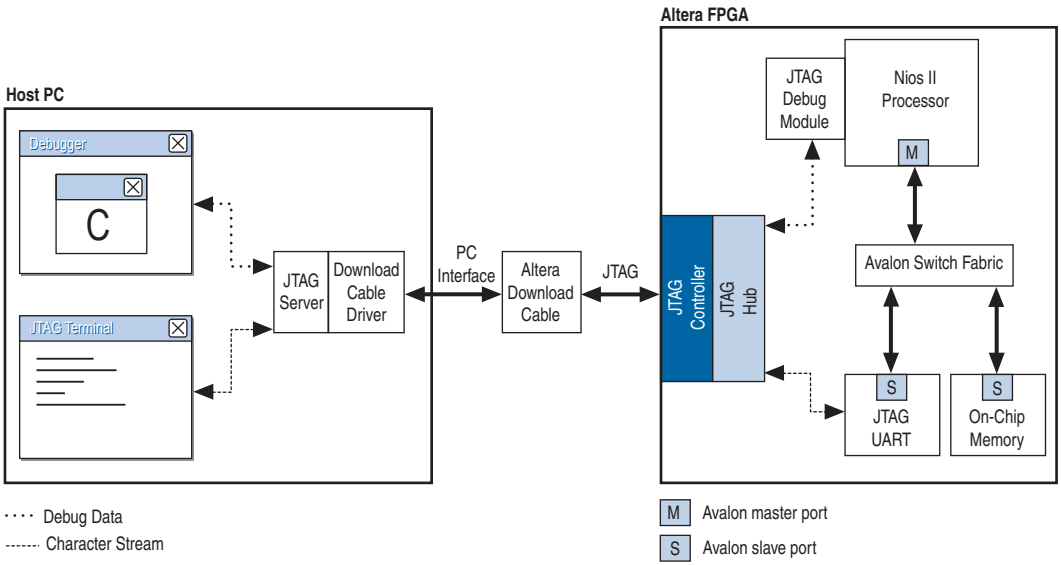
JTAG Interface

Altera FPGAs contain built-in JTAG control circuitry that interfaces the device's JTAG pins to logic inside the device. The JTAG controller can connect to user-defined circuits called "nodes" implemented in the FPGA. Because there may be several nodes that need to communicate via the JTAG interface, a JTAG hub (i.e., a multiplexer) becomes necessary. During logic synthesis and fitting, the Quartus® II software automatically generates the JTAG hub logic. No manual design effort is required to connect the JTAG circuitry inside the device; it is presented here only for clarity.

Host-Target Connection

Figure 5–2 shows the connection between a host PC and an SOPC Builder-generated system containing a JTAG UART core.

Figure 5–2. Example System Using the JTAG UART Core



The JTAG controller on the FPGA and the download cable driver on the host PC implement a simple data-link layer between host and target. All JTAG nodes inside the FPGA are multiplexed through the single JTAG connection. JTAG server software on the host PC controls and decodes the JTAG data stream, and maintains distinct connections with nodes inside the FPGA.

The example system in Figure 5–2 contains one JTAG UART core and a Nios II processor. Both agents communicate to the host PC over a single Altera download cable. Thanks to the JTAG server software, each host application has an independent connection to the target. Altera provides the JTAG server drivers and host software required to communicate with the JTAG UART core.

Systems with multiple JTAG UART cores are possible, and all cores communicate via the same JTAG interface. Only one processor should communicate with each JTAG UART core to maintain coherent data streams.

Device Support & Tools

The JTAG UART core supports the Stratix®, Stratix II, Cyclone™ and Cyclone II device families. The JTAG UART core is supported by the Nios II hardware abstraction layer (HAL) system library. No software support is provided for the first-generation Nios processor.

To view the character stream on the host PC, the JTAG UART core must be used in conjunction with the JTAG terminal software provided by Altera. Nios II processor users access the JTAG UART via the Nios II IDE or the **nios2-terminal** command-line utility.

For further details, refer to the *Nios II Software Developer's Handbook* or the Nios II IDE online help

Instantiating the Core in SOPC Builder

Designers use the JTAG UART core's SOPC Builder configuration wizard to specify the core features. The following sections describe the available options in the configuration wizard.

Configuration Tab

The options on this tab control the hardware configuration of the JTAG UART core. The default settings are pre-configured to behave optimally with the Altera-provided device drivers and JTAG terminal software. Most designers should not change the default values, except for the **Construct using registers instead of memory blocks** option.

Write FIFO Settings

The write FIFO buffers data flowing from the Avalon interface to the host. The following settings are available:

- **Depth**—The write FIFO depth can be set from 8 to 32,768 bytes. Only powers of two are allowable. Larger values consume more on-chip memory resources. A depth of 64 is generally optimal for performance, and larger values are rarely necessary.

- **IRQ Threshold**—The write IRQ threshold governs how the core asserts its IRQ in response to the FIFO emptying. As the JTAG circuitry empties data from the write FIFO, the core asserts its IRQ when the number of characters remaining in the FIFO reaches this threshold value. For maximum bandwidth efficiency, a processor should service the interrupt by writing more data and preventing the write FIFO from emptying completely. A value of 8 is typically optimal. See "Interrupt Behavior" on page 5–13 for further details.

- **Construct using registers instead of memory blocks**—Turning on this option causes the FIFO to be constructed out of on-chip logic resources. This option is useful when memory resources are limited. Each byte consumes roughly 11 logic elements (LEs), so a FIFO depth of 8 (bytes) consumes roughly 88 LEs.

Read FIFO Settings

The read FIFO buffers data flowing from the host to the Avalon interface. Settings are available to control the depth of the FIFO and the generation of interrupts.

- **Depth**—The read FIFO depth can be set from 8 to 32,768 bytes. Only powers of two are acceptable. Larger values consume more on-chip memory resources. A depth of 64 is generally optimal for performance, and larger values are rarely necessary.

- **IRQ Threshold—**The IRQ threshold governs how the core asserts its IRQ in response to the FIFO filling up. As the JTAG circuitry fills up the read FIFO, the core asserts its IRQ when the amount of space remaining in the FIFO reaches this threshold value. For maximum bandwidth efficiency, a processor should service the interrupt by reading data and preventing the read FIFO from filling up completely. A value of 8 is typically optimal. See "Interrupt Behavior" on page 5–13 for further details.

- **Construct using registers instead of memory blocks**—Turning on this option causes the FIFO to be constructed out of logic resources. This option is useful when memory resources are limited. Each byte consumes roughly 11 LEs, so a FIFO depth of 8 (bytes) consumes roughly 88 LEs.

Simulation Settings

At system generation time when SOPC Builder generates the logic for the JTAG UART core, a simulation model is also constructed. The simulation model offers features to simplify simulation of systems using the JTAG UART core. Changes to the simulation settings do not affect the behavior of the core in hardware; the settings affect only functional simulation.

Simulated Input Character Stream

You can enter a character stream that will be simulated entering the read FIFO upon simulated system reset. The configuration wizard accepts an arbitrary character string, which is later incorporated into the test bench. After reset, this character string is pre-initialized in the read FIFO, giving the appearance that an external JTAG terminal program is sending a character stream to the JTAG UART core.

Prepare Interactive Windows

At system generation time, the JTAG UART core generator can create ModelSim macros to open interactive windows during simulation. These windows allow the user to send and receive ASCII characters via a console, giving the appearance of a terminal session with the system executing in hardware. The following options are available.

- **Do not generate ModelSim aliases for interactive windows**—This option does not create any ModelSim macros for character I/O.
- **Create ModelSim alias to open a window showing output as ASCII text**—This option creates a ModelSim macro to open a console window that displays output from the write FIFO. Values written to the write FIFO via the Avalon interface are displayed in the console as ASCII characters.
- **Create ModelSim alias to open an interactive stimulus/response window**—This option creates a ModelSim macro to open a console window that allows input and output interaction with the core. Values written to the write FIFO via the Avalon interface are displayed in the console as ASCII characters. Characters typed into

the console are fed into the read FIFO, and can be read via the Avalon interface. When this option is enabled, the simulated character input stream option is ignored.

Hardware Simulation Considerations

The simulation features were created for easy simulation of Nios II processor systems when using the ModelSim simulator. The simulation model is implemented in the JTAG UART core's top-level HDL file. The synthesizable HDL and the simulation HDL are implemented in the same file. Some simulation features are implemented using "translate on/off" synthesis directives that make certain sections of HDL code visible only to the synthesis tool.

Refer to *AN 351: Simulating Nios II Processor Designs* for complete details of simulating the JTAG UART core in Nios II systems.

Other simulators can be used, but will require user effort to create a custom simulation process. Designers can use the auto-generated ModelSim scripts as reference to create similar functionality for other simulators.

Do not edit the simulation directives if you are using Altera's recommended simulation procedures. If you change the simulation directives to create a custom simulation flow, be aware that SOPC Builder overwrites existing files during system generation. Take precaution so that your changes are not overwritten.

Software Programming Model

The following sections describe the software programming model for the JTAG UART core, including the register map and software declarations to access the hardware. For Nios II processor users, Altera provides HAL system library drivers that enable you to access the JTAG UART using the ANSI C standard library functions, such as `printf()` and `getchar()`.

HAL System Library Support

The Altera-provided driver implements a HAL character-mode device driver that integrates into the HAL system library for Nios II systems. HAL users should access the JTAG UART via the familiar HAL API and the ANSI C standard library, rather than accessing the JTAG UART registers. `ioctl()` requests are defined that allow HAL users to control the hardware-dependent aspects of the JTAG UART.

If your program uses the Altera-provided HAL device driver to access the JTAG UART hardware, accessing the device registers directly will interfere with the correct behavior of the driver.

For Nios II processor users, the HAL system library API provides complete access to the JTAG UART core's features. Nios II programs treat the JTAG UART core as a character mode device, and send and receive data using the ANSI C standard library functions, such as `getchar()` and `printf()`.

"Printing Characters to a JTAG UART Core as stdout" demonstrates the simplest possible usage, printing a message to stdout using `printf()`. In this example, the SOPC Builder system contains a JTAG UART core, and the HAL system library has been configured to use this JTAG UART device for stdout.

Printing Characters to a JTAG UART Core as stdout

```
#include <stdio.h>
int main ()
{
  printf("Hello world.\n");
  return 0;
}
```

"Transmitting Characters to a JTAG UART Core" on page 5–9 demonstrates reading characters from and sending messages to a JTAG UART core using the C standard library. In this example, the SOPC Builder system contains a JTAG UART core named `jtag_uart` that is not necessarily configured as the stdout device. In this case, the program treats the device like any other node in the HAL file system.

Transmitting Characters to a JTAG UART Core

```
/* A simple program that recognizes the characters 't' and 'v' */
#include <stdio.h>
#include <string.h>
int main ()
{
  char* msg = "Detected the character 't'.\n";
  FILE* fp;
  char prompt = 0;

  fp = fopen ("/dev/jtag_uart", "r+"); //Open file for reading and writing
  if (fp)
  {
    while (prompt != 'v')
    {  // Loop until we receive a 'v'.
      prompt = getc(fp);  // Get a character from the JTAG UART.
      if (prompt == 't')
      {  // Print a message if character is 't'.
        fwrite (msg, strlen (msg), 1, fp);
      }

      if (ferror(fp))// Check if an error occurred with the file pointer
        clearerr(fp);// If so, clear it.
    }

    fprintf(fp, "Closing the JTAG UART file handle.\n");
    fclose (fp);
  }

  return 0;
}
```

In this example, the `ferror(fp)` is used to check if an error occurred on the JTAG UART connection, such as a disconnected JTAG connection. In this case, the driver detects that the JTAG connection is disconnected, reports an error (`EIO`), and discards data for subsequent transactions. If this error ever occurs, the C library latches the value until you explicitly clear it with the `clearerr()` function.

The *Nios II Software Developer's Handbook* provides complete details of the HAL system library. The Nios II Embedded Design Suite (EDS) provides a number of software example designs that use the JTAG UART core.

Driver Options: Fast vs. Small Implementations

To accommodate the requirements of different types of systems, the JTAG UART driver provides two variants: A fast version and a small version. The fast behavior will be used by default. Both the fast and small drivers fully support the C standard library functions and the HAL API.

The fast driver is an interrupt-driven implementation, which allows the processor to perform other tasks when the device is not ready to send or receive data. Because the JTAG UART data rate is slow compared to the processor, the fast driver can provide a large performance benefit for systems that could be performing other tasks in the interim. In addition, the fast version of the Altera Avalon JTAG UART monitors the connection to the host. The driver discards characters if there is no host connected, or if the host is not running an application that handles the I/O stream.

The small driver is a polled implementation that waits for the JTAG UART hardware before sending and receiving each character. The performance of the small driver is poor if you are sending large amounts of data. The small version assumes that the host is always connected, and will never discard characters. Therefore, the small driver will hang the system if the JTAG UART hardware is ever disconnected from the host while the program is sending or receiving data. There are two ways to enable the small footprint driver:

- Enable the small footprint setting for the HAL system library project. This option affects device drivers for all devices in the system as well.
- Specify the preprocessor option `-DALTERA_AVALON_JTAG_UART_SMALL`. You can use this option if you want the small, polled implementation of the JTAG UART driver, but you do not want to affect the drivers for other devices.

ioctl() Operations

The fast version of the JTAG UART driver supports the `ioctl()` function to allow HAL-based programs to request device-specific operations. Specifically, you can use the `ioctl()` operations to control the timeout period, and to detect whether or not a host is connected. The fast driver defines the `ioctl()` operations shown in Table 5–1.

Table 5–1. JTAG UART ioctl() Operations for the Fast Driver Only

Request	Meaning
TIOCSTIMEOUT	Set the timeout (in seconds) after which the driver will decide that the host is not connected. A timeout of 0 makes the target assume that the host is always connected. The `ioctl` arg parameter passed in must be a pointer to an integer.
TIOCGCONNECTED	Sets the integer arg parameter to a value that indicates whether the host is connected and acting as a terminal (1), or not connected (0). The `ioctl` arg parameter passed in must be a pointer to an integer.

Refer to the *Nios II Software Developer's Handbook* for details on the `ioctl()` function.

Software Files

The JTAG UART core is accompanied by the following software files. These files define the low-level interface to the hardware, and provide the HAL drivers. Application developers should not modify these files.

- **altera_avalon_jtag_uart_regs.h**—This file defines the core's register map, providing symbolic constants to access the low-level hardware. The symbols in this file are used only by device driver functions.
- **altera_avalon_jtag_uart.h**, **altera_avalon_jtag_uart.c**—These files implement the HAL system library device driver.

Accessing the JTAG UART Core via a Host PC

Host software is necessary for a PC to access the JTAG UART core. The Nios II IDE supports the JTAG UART core, and displays character I/O in a console window. Altera also provides a command-line utility called **nios2-terminal** that opens a terminal session with the JTAG UART core.

For further details, refer to the *Nios II Software Developer's Handbook* and the Nios II IDE online help.

Register Map

Programmers using the HAL API never access the JTAG UART core directly via its registers. In general, the register map is only useful to programmers writing a device driver for the core.

The Altera-provided HAL device driver accesses the device registers directly. If you are writing a device driver, and the HAL driver is active for the same device, your driver will conflict and fail to operate.

Table 5–2 shows the register map for the JTAG UART core. Device drivers control and communicate with the core through the two 32-bit memory-mapped registers.

Table 5–2. JTAG UART Core Register Map

Offset	Register Name	R/W	Bit Description													
			31	…	16	15	14	…	11	10	9	8	7	…	2	1	0
0	data	RW	RAVAIL			RVALID	*(1)*						DATA				
1	control	RW	WSPACE			*(1)*				AC	WI	RI	*(1)*			WE	RE

Note to Table 5–2:
(1) Reserved. Read values are undefined. Write zero.

Data Register

Embedded software accesses the read and write FIFOs via the `data` register. Table 5–3 describes the function of each bit.

Table 5–3. data Register Bits

Bit Number	Bit/Field Name	Read/Write/Clear	Description
0 .. 7	DATA	R/W	The value to transfer to/from the JTAG core. When writing, the DATA field is a character to be written to the write FIFO. When reading, the DATA field is a character read from the read FIFO.
15	RVALID	R	Indicates whether the DATA field is valid. If RVALID=1, then the DATA field is valid, else DATA is undefined.
16 .. 32	RAVAIL	R	The number of characters remaining in the read FIFO (after this read).

A read from the `data` register returns the first character from the FIFO (if one is available) in the DATA field. Reading also returns information about the number of characters remaining in the FIFO in the RAVAIL field. A write to the `data` register stores the value of the DATA field in the write FIFO. If the write FIFO is full, then the character is lost.

Control Register

Embedded software controls the JTAG UART core's interrupt generation and reads status information via the `control` register. Table 5–4 describes the function of each bit.

Table 5–4. control Register Bits

Bit Number	Bit/Field Name	Read/Write/Clear	Description
0	RE	R/W	Interrupt-enable bit for read interrupts
1	WE	R/W	Interrupt-enable bit for write interrupts
8	RI	R	Indicates that the read interrupt is pending
9	WI	R	Indicates that the write interrupt is pending
10	AC	R/C	Indicates that there has been JTAG activity since the bit was cleared. Writing 1 to AC clears it to 0.
16 .. 32	WSPACE	R	The number of spaces available in the write FIFO.

A read from the `control` register returns the status of the read and write FIFOs. Writes to the register can be used to enable/disable interrupts, or clear the AC bit.

The RE and WE bits enable interrupts for the read and write FIFOs, respectively. The WI and RI bits indicate the status of the interrupt sources, qualified by the values of the interrupt enable bits (WE and RE). Embedded software can examine RI and WI to determine what condition generated the IRQ. See "Interrupt Behavior" on page 5–13 for further details.

The AC bit indicates that an application on the host PC has polled the JTAG UART core via the JTAG interface. Once set, the AC bit remains set until it is explicitly cleared via the Avalon interface. Writing 1 to AC clears it. Embedded software can examine the AC bit to determine if a connection exists to a host PC. If no connection exists, the software may choose to ignore the JTAG data stream. When the host PC has no data to transfer, it can choose to poll the JTAG UART core as infrequently as once per second. Delays caused by other host software using the JTAG download cable could cause delays of up to 10 seconds between polls.

Interrupt Behavior

The JTAG UART core generates an interrupt when either of the individual interrupt conditions are pending and enabled.

Interrupt behavior is of concern to device driver programmers concerned with the bandwidth performance to the host PC. Example designs and the JTAG terminal program provided with Nios II Embedded Design Suite (EDS) are pre-configured with optimal interrupt behavior.

The JTAG UART core has two kinds of interrupts: write interrupts and read interrupts. The WE and RE bits in the `control` register enable/disable the interrupts.

The core can assert a write interrupt whenever the write FIFO is nearly empty. The "nearly empty" threshold, *write_threshold*, is specified at system generation time and cannot be changed by embedded software. The write interrupt condition is set whenever there are *write_threshold* or fewer characters in the write FIFO. It is cleared by writing characters to fill the write FIFO beyond the *write_threshold*. Embedded software should only enable write interrupts after filling the write FIFO. If it has no characters remaining to send, embedded software should disable the write interrupt.

The core can assert a read interrupt whenever the read FIFO is nearly full. The "nearly full" threshold value, *read_threshold*, is specified at system generation time and cannot be changed by embedded software. The read interrupt condition is set whenever the read FIFO has *read_threshold* or fewer spaces remaining. The read interrupt condition is also set if there is at least one character in the read FIFO and no more characters are expected. The read interrupt is cleared by reading characters from the read FIFO.

For optimum performance, the interrupt thresholds should match the interrupt response time of the embedded software. For example, with a 10-MHz JTAG clock, a new character will be provided (or consumed) by the host PC every 1µs. With a threshold of 8, the interrupt response time must be less than 8µs. If the interrupt response time is too long, then performance will suffer. If it is too short, then interrupts will occur too frequently.

For Nios II processor systems, read and write thresholds of 8 are an appropriate default.

6. UART Core with Avalon Interface

NII51010-6.0.0

Core Overview

The universal asynchronous receiver/transmitter core with Avalon® interface ("the UART core") implements a method to communicate serial character streams between an embedded system on an Altera® FPGA and an external device. The core implements the RS-232 protocol timing, and provides adjustable baud rate, parity, stop and data bits, and optional RTS/CTS flow control signals. The feature set is configurable, allowing designers to implement just the necessary functionality for a given system.

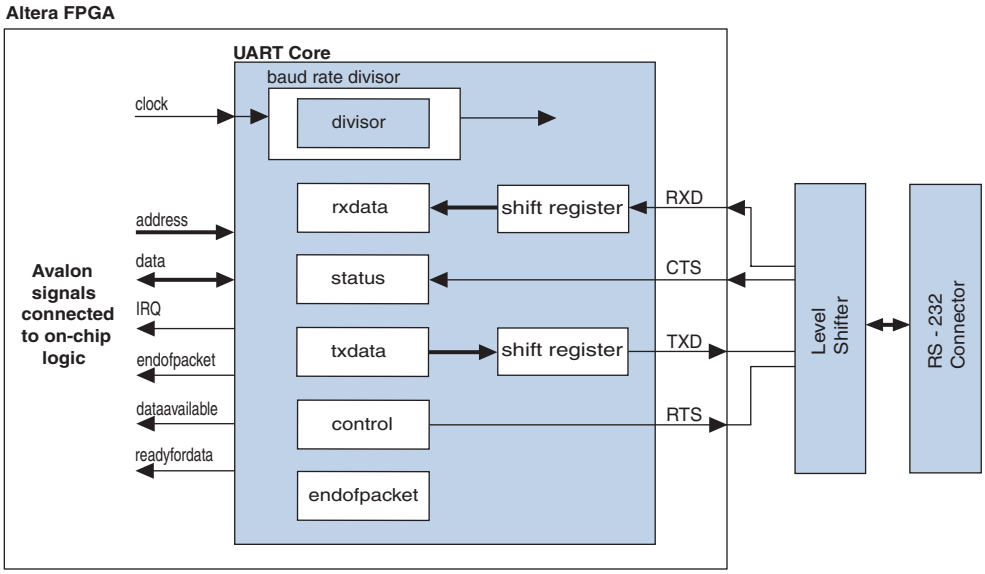
The core provides a simple register-mapped Avalon slave interface that allows Avalon master peripherals (such as a Nios® II processor) to communicate with the core simply by reading and writing control and data registers.

The UART core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

Functional Description

Figure 6–1 shows a block diagram of the UART core.

Figure 6–1. Block Diagram of the UART Core in a Typical System



The core has two user-visible parts:

- The register file, which is accessed via the Avalon slave port
- The RS-232 signals, `RXD`, `TXD`, `CTS`, and `RTS`

Avalon Slave Interface & Registers

The UART core provides an Avalon slave interface to the internal register file. The user interface to the UART core consists of six 16-bit registers: `control`, `status`, `rxdata`, `txdata`, `divisor`, and `endofpacket`. A master peripheral, such as a Nios II processor, accesses the registers to control the core and transfer data over the serial connection.

The UART core provides an active-high interrupt request (IRQ) output that can request an interrupt when new data has been received, or when the core is ready to transmit another character. For further details see "Interrupt Behavior" on page 6–20.

The Avalon slave port is capable of transfers with flow control. The UART core can be used in conjunction with a direct memory access (DMA) peripheral with Avalon flow control to automate continuous data transfers between, for example, the UART core and memory.

See the *Timer Core with Avalon Interface* chapter for details. See the *Avalon Interface Specification* for details of the Avalon interface.

RS-232 Interface

The UART core implements RS-232 asynchronous transmit and receive logic. The UART core sends and receives serial data via the `TXD` and `RXD` ports. The I/O buffers on most Altera FPGA families do not comply with RS-232 voltage levels, and may be damaged if driven directly by signals from an RS-232 connector. To comply with RS-232 voltage signaling specifications, an external level-shifting buffer is required (e.g., Maxim MAX3237) between the FPGA I/O pins and the external RS-232 connector.

The UART core uses a logic 0 for mark, and a logic 1 for space. An inverter inside the FPGA can be used to reverse the polarity of any of the RS-232 signals, if necessary.

Transmitter Logic

The UART transmitter consists of a 7-, 8-, or 9-bit `txdata` holding register and a corresponding 7-, 8-, or 9-bit transmit shift register. Avalon master peripherals write the `txdata` holding register via the Avalon slave port. The transmit shift register is automatically loaded from the `txdata` register when a serial transmit shift operation is not currently in progress. The transmit shift register directly feeds the `TXD` output. Data is shifted out to `TXD` least-significant bit (LSB) first.

These two registers provide double buffering. A master peripheral can write a new value into the `txdata` register while the previously written character is being shifted out. The master peripheral can monitor the transmitter's status by reading the `status` register's transmitter ready (trdy), transmitter shift register empty (tmt), and transmitter overrun error (toe) bits.

The transmitter logic automatically inserts the correct number of start, stop, and parity bits in the serial `TXD` data stream as required by the RS-232 specification.

Receiver Logic

The UART receiver consists of a 7-, 8-, or 9-bit receiver-shift register and a corresponding 7-, 8-, or 9-bit `rxdata` holding register. Avalon master peripherals read the `rxdata` holding register via the Avalon slave port. The `rxdata` holding register is loaded from the receiver shift register automatically every time a new character is fully received.

These two registers provide double buffering. The `rxdata` register can hold a previously received character while the subsequent character is being shifted into the receiver shift register.

A master peripheral can monitor the receiver's status by reading the `status` register's read-ready (rrdy), receiver-overrun error (roe), break detect (brk), parity error (pe), and framing error (fe) bits. The receiver logic automatically detects the correct number of start, stop, and parity bits in the serial RXD stream as required by the RS-232 specification. The receiver logic checks for four exceptional conditions in the received data (frame error, parity error, receive overrun error, and break), and sets corresponding status register bits (fe, pe, roe, or brk).

Baud Rate Generation

The UART core's internal baud clock is derived from the Avalon clock input. The internal baud clock is generated by a clock divider. The divisor value can come from one of the following sources:

- A constant value specified at system generation time
- The 16-bit value stored in the `divisor` register

The `divisor` register is an optional hardware feature. If it is disabled at system generation time, the divisor value is fixed, and the baud rate cannot be altered.

Device Support & Tools

The UART core can target all Altera FPGAs, including Stratix™ and Cyclone™ device families.

Instantiating the Core in SOPC Builder

Instantiating the UART in hardware creates at least two I/O ports for each UART core: An `RXD` input, and a `TXD` output. Optionally, the hardware may include flow control signals, the `CTS` input and RTS output.

The hardware feature set is configured via the UART core's SOPC Builder configuration wizard. The following sections describe the available options.

Configuration Settings

This section describes the configuration settings.

Baud Rate Options

The UART core can implement any of the standard baud rates for RS-232 connections. The baud rate can be configured in one of two ways:

- **Fixed rate**—The baud rate is fixed at system generation time and cannot be changed via the Avalon slave port.
- **Variable rate**—The baud rate can vary, based on a clock divisor value held in the `divisor` register. A master peripheral changes the baud rate by writing new values to the `divisor` register.

The baud rate is calculated based on the clock frequency provided by the Avalon interface. Changing the system clock frequency in hardware without re-generating the UART core hardware will result in incorrect signaling.

Baud Rate (bps) Setting
The **Baud Rate** setting determines the default baud rate after reset. The **Baud Rate** option offers standard preset values (e.g., 9600, 57600, 115200 bps), or you can manually enter any baud rate.

The baud rate value is used to calculate an appropriate clock divisor value to implement the desired baud rate. Baud rate and divisor values are related as follows:

$$divisor = int((clock\ frequency)/(baud\ rate) + 0.5)$$

$$baud\ rate = (clock\ frequency)/(divisor + 1)$$

Baud Rate Can Be Changed By Software Setting
When this setting is on, the hardware includes a 16-bit `divisor` register at address offset 4. The `divisor` register is writeable, so the baud rate can be changed by writing a new value to this register.

When this setting is off, the UART hardware does not include a `divisor` register. The UART hardware implements a constant (unchangeable) baud divisor, and the value cannot be changed after system generation. In this case, writing to address offset 4 has no effect, and reading from address offset 4 produces an undefined result.

Data Bits, Stop Bits, Parity

The UART core's parity, data bits and stop bits are configurable. These settings are fixed at system generation time; they cannot be altered via the register file. The following settings are available.

Data Bits Setting
See Table 6–1.

Table 6–1. Data Bits Setting

Setting	Allowed Values	Description
Data Bits	7, 8, 9	This setting determines the widths of the `txdata`, `rxdata`, and `endofpacket` registers.
Stop Bits	1, 2	This setting determines whether the core transmits 1 or 2 stop bits with every character. The core always terminates a receive transaction at the first stop bit, and ignores all subsequent stop bits, regardless of the Stop Bits setting.
Parity	None, Even, Odd	This setting determines whether the UART transmits characters with parity checking, and whether it expects received characters to have parity checking. See below for further details.

Parity Setting
When **Parity** is set to **None**, the transmit logic sends data without including a parity bit, and the receive logic presumes the incoming data does not include a parity bit. When parity is None, the status register's pe (parity error) bit is not implemented; it always reads 0.

When **Parity** is set to **Odd** or **Even**, the transmit logic computes and inserts the required parity bit into the outgoing `TXD` bitstream, and the receive logic checks the parity bit in the incoming `RXD` bitstream. If the receiver finds data with incorrect parity, the status register's pe is set to 1. When parity is Even, the parity bit is 1 if the character has an even number of 1 bits; otherwise the parity bit is 0. Similarly, when parity is Odd, the parity bit is 1 if the character has an odd number of 1 bits.

Flow Control

The following flow control option is available.

Include CTS/RTS pins & control register bits
When this setting is on, the UART hardware includes:

- CTS_N (logic negative `CTS`) input port
- RTS_N (logic negative `RTS`) output port
- CTS bit in the `status` register

- DCTS bit in the `status` register
- RTS bit in the `control` register
- IDCTS bit in the `control` register

Based on these hardware facilities, an Avalon master peripheral can detect `CTS` and transmit RTS flow control signals. The `CTS` input and RTS output ports are tied directly to bits in the `status` and `control` registers, and have no direct effect on any other part of the core.

When the **Include CTS/RTS pins and control register bits** setting is off, the core does not include the hardware listed above. The control/status bits CTS, DCTS, IDCTS, and RTS are not implemented; they always read as 0.

Avalon Transfers With Flow Control (DMA)

The UART core's Avalon interface optionally implements Avalon transfers with flow control. This allows an Avalon master peripheral to write data only when the UART core is ready to accept another character, and to read data only when the core has data available. The UART core can also optionally include the end-of-packet register.

Include end-of-packet register
When this setting is on, the UART core includes:

- A 7-, 8-, or 9-bit `endofpacket` register at address-offset 5. The data width is determined by the **Data Bits** setting.
- eop bit in the status register
- ieop bit in the control register
- `endofpacket` signal in the Avalon interface to support data transfers with flow control to/from other master peripherals in the system

End-of-packet (EOP) detection allows the UART core to terminate a data transaction with a Avalon master with flow control. EOP detection can be used with a DMA controller, for example, to implement a UART that automatically writes received characters to memory until a specified character is encountered in the incoming `RXD` stream. The terminating (end of packet) character's value is determined by the `endofpacket` register.

When the end-of-packet register is disabled, the UART core does not include the resources listed above. Writing to the `endofpacket` register has no effect, and reading produces an undefined value.

Simulation Settings

When the UART core's logic is generated, a simulation model is also constructed. The simulation model offers features to simplify and accelerate simulation of systems that use the UART core. Changes to the simulation settings do not affect the behavior of the UART core in hardware; the settings affect only functional simulation.

For examples of how to use the following settings to simulate Nios II systems, refer to *AN 351: Simulating Nios II Embedded Processor Designs*.

Simulated RXD-Input Character Stream

You can enter a character stream that will be simulated entering the RXD port upon simulated system reset. The UART core's configuration wizard accepts an arbitrary character string, which is later incorporated into the UART simulation model. After reset in reset, the string is input into the RXD port character-by-character as the core is able to accept new data.

Prepare Interactive Windows

At system generation time, the UART core generator can create ModelSim macros that facilitate interaction with the UART model during simulation. The following options are available:

Create ModelSim Alias to open streaming output window
A ModelSim macro is created to open a window that displays all output from the TXD port.

Create ModelSim Alias to open interactive stimulus window
A ModelSim macro is created to open a window that accepts stimulus for the RXD port. The window sends any characters typed in the window to the RXD port.

Simulated Transmitter Baud Rate

RS-232 transmission rates are often slower than any other process in the system, and it is seldom useful to simulate the functional model at the true baud rate. For example, at 115,200 bps, it typically takes thousands of clock cycles to transfer a single character. The UART simulation model has the ability to run with a constant clock divisor of 2. This allows the simulated UART to transfer bits at half the system clock speed, or roughly one character per 20 clock cycles. You can choose one of the following options for the simulated transmitter baud rate:

- **accelerated (use divisor = 2)**—TXD emits one bit per 2 clock cycles in simulation.

- **actual (use true baud divisor)**—`TXD` transmits at the actual baud rate, as determined by the `divisor` register.

Hardware Simulation Considerations

The simulation features were created for easy simulation of Nios, Nios II or Excalibur™ processor systems when using the ModelSim simulator. The documentation for each processor documents the suggested usage of these features. Other usages may be possible, but will require additional user effort to create a custom simulation process.

The simulation model is implemented in the UART core's top-level HDL file; the synthesizable HDL and the simulation HDL are implemented in the same file. The simulation features are implemented using `translate on` and `translate off` synthesis directives that make certain sections of HDL code visible only to the synthesis tool.

Do not edit the simulation directives if you are using Altera's recommended simulation procedures. If you do change the simulation directives for your custom simulation flow, be aware that SOPC Builder overwrites existing files during system generation. Take precaution so that your changes are not overwritten.

For details on simulating the UART core in Nios II processor systems see *AN 351: Simulating Nios II Processor Designs*. For details on simulating the UART core in Nios embedded processor systems see *AN 189: Simulating Nios Embedded Processor Designs*.

Software Programming Model

The following sections describe the software programming model for the UART core, including the register map and software declarations to access the hardware. For Nios II processor users, Altera provides hardware abstraction layer (HAL) system library drivers that enable you to access the UART core using the ANSI C standard library functions, such as `printf()` and `getchar()`.

HAL System Library Support

The Altera-provided driver implements a HAL character-mode device driver that integrates into the HAL system library for Nios II systems. HAL users should access the UART via the familiar HAL API and the ANSI C standard library, rather than accessing the UART registers. `ioctl()` requests are defined that allow HAL users to control the hardware-dependent aspects of the UART.

If your program uses the HAL device driver to access the UART hardware, accessing the device registers directly will interfere with the correct behavior of the driver.

For Nios II processor users, the HAL system library API provides complete access to the UART core's features. Nios II programs treat the UART core as a character mode device, and send and receive data using the ANSI C standard library functions.

The driver supports the CTS/RTS control signals when they are enabled in SOPC Builder. See "Driver Options: Fast vs. Small Implementations" on page 6–11.

The following code demonstrates the simplest possible usage, printing a message to stdout using `printf()`. In this example, the SOPC Builder system contains a UART core, and the HAL system library has been configured to use this device for stdout.

Example: Printing Characters to a UART Core as stdout

```
#include <stdio.h>
int main ()
{
  printf("Hello world.\n");
  return 0;
}
```

The following code demonstrates reading characters from and sending messages to a UART device using the C standard library. In this example, the SOPC Builder system contains a UART core named `uart1` that is not necessarily configured as the stdout device. In this case, the program treats the device like any other node in the HAL file system.

Example: Sending & Receiving Characters

```
/* A simple program that recognizes the characters 't' and 'v' */
#include <stdio.h>
#include <string.h>
int main ()
{
  char* msg = "Detected the character 't'.\n";
  FILE* fp;
  char prompt = 0;

  fp = fopen ("/dev/uart1", "r+"); //Open file for reading and writing
  if (fp)
  {
    while (prompt != 'v')
    {  // Loop until we receive a 'v'.
      prompt = getc(fp);  // Get a character from the UART.
      if (prompt == 't')
      {  // Print a message if character is 't'.
        fwrite (msg, strlen (msg), 1, fp);
      }
```

```
    }

    fprintf(fp, "Closing the UART file.\n");
    fclose (fp);
  }

  return 0;
}
```

The *Nios II Software Developer's Handbook* provides complete details of the HAL system library.

Driver Options: Fast vs. Small Implementations

To accommodate the requirements of different types of systems, the UART driver provides two variants: A fast version and a small version. The fast behavior will be used by default. Both the fast and small drivers fully support the C standard library functions and the HAL API.

The fast driver is an interrupt-driven implementation, which allows the processor to perform other tasks when the device is not ready to send or receive data. Because the UART data rate is slow compared to the processor, the fast driver can provide a large performance benefit for systems that could be performing other tasks in the interim.

The small driver is a polled implementation that waits for the UART hardware before sending and receiving each character. There are two ways to enable the small footprint driver:

- Enable the small footprint setting for the HAL system library project. This option affects device drivers for all devices in the system as well.
- Specify the preprocessor option `-DALTERA_AVALON_UART_SMALL`. You can use this option if you want the small, polled implementation of the UART driver, but you do not want to affect the drivers for other devices.

See the help system in the Nios II IDE for details on how to set HAL properties and preprocessor options.

If the CTS/RTS flow control signals are enabled in hardware, the fast driver automatically uses them. The small driver always ignores them.

ioctl() Operations

The UART driver supports the `ioctl()` function to allow HAL-based programs to request device-specific operations. Table 6–2 defines operation requests that the UART driver supports.

Table 6–2. UART ioctl() Operations

Request	Meaning
`TIOCEXCL`	Locks the device for exclusive access. Further calls to `open()` for this device will fail until either this file descriptor is closed, or the lock is released using the TIOCNXCL `ioctl` request. For this request to succeed there can be no other existing file descriptors for this device. The `ioctl` "arg" parameter is ignored.
`TIOCNXCL`	Releases a previous exclusive access lock. See the comments above for details. The `ioctl` "arg" parameter is ignored.

Additional operation requests are also optionally available for the fast driver only, as shown in Table 6–3. To enable these operations in your program, you must set the preprocessor option `-DALTERA_AVALON_UART_USE_IOCTL`.

Table 6–3. Optional UART ioctl() Operations for the Fast Driver Only

Request	Meaning
`TIOCMGET`	Returns the current configuration of the device by filling in the contents of the input termios (1) structure. A pointer to this structure is supplied as the value of the `ioctl` "opt" parameter.
`TIOCMSET`	Sets the configuration of the device according to the values contained in the input termios structure (1). A pointer to this structure is supplied as the value of the `ioctl` "arg" parameter.

Note to Table 6–3:

(1) The termios structure is defined by the Newlib C standard library. You can find the definition in the file *<Nios II EDS install path>***/components/altera_hal/HAL/inc/sys/termios.h**.

Refer to the *Nios II Software Developer's Handbook* for details on the `ioctl()` function.

Limitations

The HAL driver for the UART core does not support the endofpacket register. See "Register Map" on page 6–13 for details.

Software Files

The UART core is accompanied by the following software files. These files define the low-level interface to the hardware, and provide the HAL drivers. Application developers should not modify these files.

- **altera_avalon_uart_regs.h**—This file defines the core's register map, providing symbolic constants to access the low-level hardware. The symbols in this file are used only by device driver functions.
- **altera_avalon_uart.h**, **altera_avalon_uart.c**—These files implement the UART core device driver for the HAL system library.

Legacy SDK Routines

The UART core is also supported by the legacy SDK routines for the first-generation Nios processor. For details on these routines, refer to the UART documentation that accompanied the first-generation Nios processor. For details on upgrading programs based on the legacy SDK to the HAL system library API, refer to *AN 350: Upgrading Nios Processor Systems to the Nios II Processor*.

Register Map

Programmers using the HAL API or the legacy SDK for the first-generation Nios processor never access the UART core directly via its registers. In general, the register map is only useful to programmers writing a device driver for the core.

The Altera-provided HAL device driver accesses the device registers directly. If you are writing a device driver, and the HAL driver is active for the same device, your driver will conflict and fail to operate.

Table 6–4 shows the register map for the UART core. Device drivers control and communicate with the core through the memory-mapped registers.

Table 6–4. UART Core Register Map

Offset	Register Name	R/W	Description/Register Bits													
			15 . . .13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	rxdata	RO	*(1)*					*(2)*	*(2)*	Receive Data						
1	txdata	WO	*(1)*					*(2)*	*(2)*	Transmit Data						
2	status *(3)*	RW	*(1)*	eop	cts	dcts	(1)	e	rrdy	trdy	tmt	toe	roe	brk	fe	pe
3	control	RW	*(1)*	ieop	rts	idcts	trbk	ie	irrdy	itrdy	itmt	itoe	iroe	ibrk	ife	ipe
4	divisor *(4)*	RW	Baud Rate Divisor													
5	endofpacket *(4)*	RW	*(1)*					*(2)*	*(2)*	End-of-Packet Value						

Notes to Table 6–4:

(1) These bits are reserved. Reading returns an undefined value. Write zero.

(2) These bits may or may not exist, depending on the **Data Width** hardware option. If they do not exist, they read zero, and writing has no effect.

(3) Writing zero to the status register clears the dcts, e, toe, roe, brk, fe, and pe bits.

(4) This register may or may not exist, depending on hardware configuration options. If it does not exist, reading returns an undefined value and writing has no effect.

Some registers and bits are optional. These registers and bits exists in hardware only if it was enabled at system generation time. Optional registers and bits are noted below.

rxdata Register

The `rxdata` register holds data received via the `RXD` input. When a new character is fully received via the `RXD` input, it is transferred into the `rxdata` register, and the `status` register's rrdy bit is set to 1. The `status` register's rrdy bit is set to 0 when the `rxdata` register is read. If a character is transferred into the `rxdata` register while the rrdy bit is already set (i.e., the previous character was not retrieved), a receiver-overrun error occurs and the `status` register's roe bit is set to 1. New characters are always transferred into the `rxdata` register, regardless of whether the previous character was read. Writing data to the `rxdata` register has no effect.

txdata Register

Avalon master peripherals write characters to be transmitted into the `txdata` register. Characters should not be written to `txdata` until the transmitter is ready for a new character, as indicated by the TRDY bit in the `status` register. The TRDY bit is set to 0 when a character is written into the `txdata` register. The TRDY bit is set to 1 when the character is transferred from the `txdata` register into the transmitter shift register. If a character is written to the `txdata` register when TRDY is 0, the result is undefined. Reading the `txdata` register returns an undefined value.

For example, assume the transmitter logic is idle and an Avalon master peripheral writes a first character into the `txdata` register. The TRDY bit is set to 0, then set to 1 when the character is transferred into the transmitter shift register. The master can then write a second character into the `txdata` register, and the TRDY bit is set to 0 again. However, this time the shift register is still busy shifting out the first character to the `TXD` output. The TRDY bit is not set to 1 until the first character is fully shifted out and the second character is automatically transferred into the transmitter shift register.

status Register

The `status` register consists of individual bits that indicate particular conditions inside the UART core. Each status bit is associated with a corresponding interrupt-enable bit in the `control` register. The `status` register can be read at any time. Reading does not change the value of any of the bits. Writing zero to the `status` register clears the DCTS, E, TOE, ROE, BRK, FE, and PE bits.

The status register bits are shown in Table 6–5.

Table 6–5. status Register Bits (Part 1 of 3)

Bit	Bit Name	Read/ Write/ Clear	Description
0 *(1)*	PE	RC	Parity error. A parity error occurs when the received parity bit has an unexpected (incorrect) logic level. The PE bit is set to 1 when the core receives a character with an incorrect parity bit. The PE bit stays set to 1 until it is explicitly cleared by a write to the status register. When the PE bit is set, reading from the rxdata register produces an undefined value. If the **Parity** hardware option is not enabled, no parity checking is performed and the PE bit always reads 0. See "Data Bits, Stop Bits, Parity" on page 6–6.
1	FE	RC	Framing error. A framing error occurs when the receiver fails to detect a correct stop bit. The FE bit is set to 1 when the core receives a character with an incorrect stop bit. The FE bit stays set to 1 until it is explicitly cleared by a write to the status register. When the FE bit is set, reading from the rxdata register produces an undefined value.
2	BRK	RC	Break detect. The receiver logic detects a break when the RXD pin is held low (logic 0) continuously for longer than a full-character time (data bits, plus start, stop, and parity bits). When a break is detected, the BRK bit is set to 1. The BRK bit stays set to 1 until it is explicitly cleared by a write to the status register.
3	ROE	RC	Receive overrun error. A receive-overrun error occurs when a newly received character is transferred into the rxdata holding register before the previous character is read (i.e., while the RRDY bit is 1). In this case, the ROE bit is set to 1, and the previous contents of rxdata are overwritten with the new character. The ROE bit stays set to 1 until it is explicitly cleared by a write to the status register.
4	TOE	RC	Transmit overrun error. A transmit-overrun error occurs when a new character is written to the txdata holding register before the previous character is transferred into the shift register (i.e., while the TRDY bit is 0). In this case the TOE bit is set to 1. The TOE bit stays set to 1 until it is explicitly cleared by a write to the status register.
5	TMT	R	Transmit empty. The TMT bit indicates the transmitter shift register's current state. When the shift register is in the process of shifting a character out the TXD pin, TMT is set to 0. When the shift register is idle (i.e., a character is not being transmitted) the TMT bit is 1. An Avalon master peripheral can determine if a transmission is completed (and received at the other end of a serial link) by checking the TMT bit.

Table 6–5. status Register Bits (Part 2 of 3)

Bit	Bit Name	Read/ Write/ Clear	Description
6	TRDY	R	Transmit ready. The TRDY bit indicates the `txdata` holding register's current state. When the `txdata` register is empty, it is ready for a new character, and trdy is 1. When the `txdata` register is full, TRDY is 0. An Avalon master peripheral must wait for TRDY to be 1 before writing new data to `txdata`.
7	RRDY	R	Receive character ready. The RRDY bit indicates the `rxdata` holding register's current state. When the `rxdata` register is empty, it is not ready to be read and rrdy is 0. When a newly received value is transferred into the `rxdata` register, RRDY is set to 1. Reading the `rxdata` register clears the RRDY bit to 0. An Avalon master peripheral must wait for RRDY to equal 1 before reading the `rxdata` register.
8	E	RC	Exception. The E bit indicates that an exception condition occurred. The E bit is a logical-OR of the TOE, ROE, BRK, FE, and PE bits. The e bit and its corresponding interrupt-enable bit (IE) bit in the `control` register provide a convenient method to enable/disable IRQs for all error conditions. The E bit is set to 0 by a write operation to the status register.
10 *(1)*	DCTS	RC	Change in clear to send (CTS) signal. The DCTS bit is set to 1 whenever a logic-level transition is detected on the CTS_N input port (sampled synchronously to the Avalon clock). This bit is set by both falling and rising transitions on CTS_N. The DCTS bit stays set to 1 until it is explicitly cleared by a write to the `status` register. If the **Flow Control** hardware option is not enabled, the DCTS bit always reads 0. See "Flow Control" on page 6–6.
11 *(1)*	CTS	R	Clear-to-send (CTS) signal. The CTS bit reflects the CTS_N input's instantaneous state (sampled synchronously to the Avalon clock). Because the CTS_N input is logic negative, the CTS bit is 1 when a 0 logic-level is applied to the CTS_N input. The CTS_N input has no effect on the transmit or receive processes. The only visible effect of the CTS_N input is the state of the CTS and DCTS bits, and an IRQ that can be generated when the control register's idcts bit is enabled. If the **Flow Control** hardware option is not enabled, the CTS bit always reads 0. See "Flow Control" on page 6–6.

Table 6–5. status Register Bits (Part 3 of 3)

Bit	Bit Name	Read/ Write/ Clear	Description
12 *(1)*	EOP	R	End of packet encountered. The EOP bit is set to 1 by one of the following events: • An EOP character is written to `txdata` • An EOP character is read from `rxdata` The EOP character is determined by the contents of the `endofpacket` register. The EOP bit stays set to 1 until it is explicitly cleared by a write to the `status` register. If the **Include End-of-Packet Register** hardware option is not enabled, the EOP bit always reads 0. See "Avalon Transfers With Flow Control (DMA)" on page 6–7.

Note to Table 6–5:
(1) This bit is optional and may not exist in hardware.

control Register

The `control` register consists of individual bits, each controlling an aspect of the UART core's operation. The value in the `control` register can be read at any time.

Each bit in the `control` register enables an IRQ for a corresponding bit in the `status` register. When both a status bit and its corresponding interrupt-enable bit are 1, the core generates an IRQ. For example, the pe bit is bit 0 of the `status` register, and the ipe bit is bit 0 of the `control` register. An interrupt request is generated when both pe and ipe equal 1.

The control register bits are shown in Table 6–6.

Table 6–6. control Register Bits (Part 1 of 2)

Bit	Bit Name	Read/ Write	Description
0	IPE	RW	Enable interrupt for a parity error.
1	IFE	RW	Enable interrupt for a framing error.
2	IBRK	RW	Enable interrupt for a break detect.
3	IROE	RW	Enable interrupt for a receiver overrun error.
4	ITOE	RW	Enable interrupt for a transmitter overrun error.
5	ITMT	RW	Enable interrupt for a transmitter shift register empty.

Table 6–6. control Register Bits (Part 2 of 2)

Bit	Bit Name	Read/ Write	Description
6	ITRDY	RW	Enable interrupt for a transmission ready.
7	IRRDY	RW	Enable interrupt for a read ready.
8	IE	RW	Enable interrupt for an exception.
9	TRBK	RW	Transmit break. The TRBK bit allows an Avalon master peripheral to transmit a break character over the `TXD` output. The `TXD` signal is forced to 0 when the TRBK bit is set to 1. The TRBK bit overrides any logic level that the transmitter logic would otherwise drive on the `TXD` output. The TRBK bit interferes with any transmission in process. The Avalon master peripheral must set the TRBK bit back to 0 after an appropriate break period elapses.
10	IDCTS	RW	Enable interrupt for a change in CTS signal.
11 *(1)*	RTS	RW	Request to send (RTS) signal. The RTS bit directly feeds the RTS_N output. An Avalon master peripheral can write the RTS bit at any time. The value of the RTS bit only affects the RTS_N output; it has no effect on the transmitter or receiver logic. Because the RTS_N output is logic negative, when the RTS bit is 1, a low logic-level (0) is driven on the RTS_N output. If the **Flow Control** hardware option is not enabled, the RTS bit always reads 0, and writing has no effect. See "Flow Control" on page 6–6.
12	IEOP	RW	Enable interrupt for end-of-packet condition.

Note to Table 6–6:
(1) This bit is optional and may not exist in hardware.

divisor Register (Optional)

The value in the `divisor` register is used to generate the baud rate clock. The effective baud rate is determined by the formula:

Baud Rate = (Clock frequency) / (divisor + 1)

The `divisor` register is an optional hardware feature. If the **Baud Rate Can Be Changed By Software** hardware option is not enabled, then the `divisor` register does not exist. In this case, writing `divisor` has no effect, and reading `divisor` returns an undefined value. For more information see "Baud Rate Options" on page 6–5.

endofpacket Register (Optional)

The value in the `endofpacket` register determines the end-of-packet character for variable-length DMA transactions. After reset, the default value is zero, which is the ASCII null character (\0). For more information, see Table 6–5 on page 6–16 for the description for the eop bit.

The endofpacket register is an optional hardware feature. If the **Include end-of-packet register** hardware option is not enabled, then the endofpacket register does not exist. In this case, writing endofpacket has no effect, and reading returns an undefined value.

Interrupt Behavior

The UART core outputs a single IRQ signal to the Avalon interface, which can connect to any master peripheral in the system, such as a Nios II processor. The master peripheral must read the status register to determine the cause of the interrupt.

Every interrupt condition has an associated bit in the status register and an interrupt-enable bit in the control register. When any of the interrupt conditions occur, the associated status bit is set to 1 and remains set until it is explicitly acknowledged. The IRQ output is asserted when any of the status bits are set while the corresponding interrupt-enable bit is 1. A master peripheral can acknowledge the IRQ by clearing the status register.

At reset, all interrupt-enable bits are set to 0; therefore, the core cannot assert an IRQ until a master peripheral sets one or more of the interrupt-enable bits to 1.

All possible interrupt conditions are listed with their associated status and control (interrupt-enable) bits in Table 6–5 on page 6–16 and Table 6–6 on page 6–18. Details of each interrupt condition are provided in the status bit descriptions.

7. SPI Core with Avalon Interface

NII51011-6.0.0

Core Overview

SPI is an industry-standard serial protocol commonly used in embedded systems to connect microprocessors to a variety of off-chip sensor, conversion, memory, and control devices. The SPI core with Avalon® interface implements the SPI protocol and provides an Avalon interface on the back end.

The SPI core can implement either the master or slave protocol. When configured as a master, the SPI core can control up to 16 independent SPI slaves. The width of the receive and transmit registers are configurable between 1 and 16 bits. Longer transfer lengths (e.g., 24-bit transfers) can be supported with software routines. The SPI core provides an interrupt output that can flag an interrupt whenever a transfer completes.

The SPI core is SOPC Builder ready and integrates easily into any SOPC Builder-generated system.

Functional Description

The SPI core communicates using two data lines, a control line, and a synchronization clock:

- Master Out Slave In (`mosi`)—Output data from the master to the inputs of the slaves
- Master In Slave Out (`miso`)—Output data from a slave to the input of the master
- Serial Clock (`sclk`)—Clock driven by the master to slaves, used to synchronize the data bits
- Slave Select (`ss_n`)— Select signal (active low) driven by the master to individual slaves, used to select the target slave

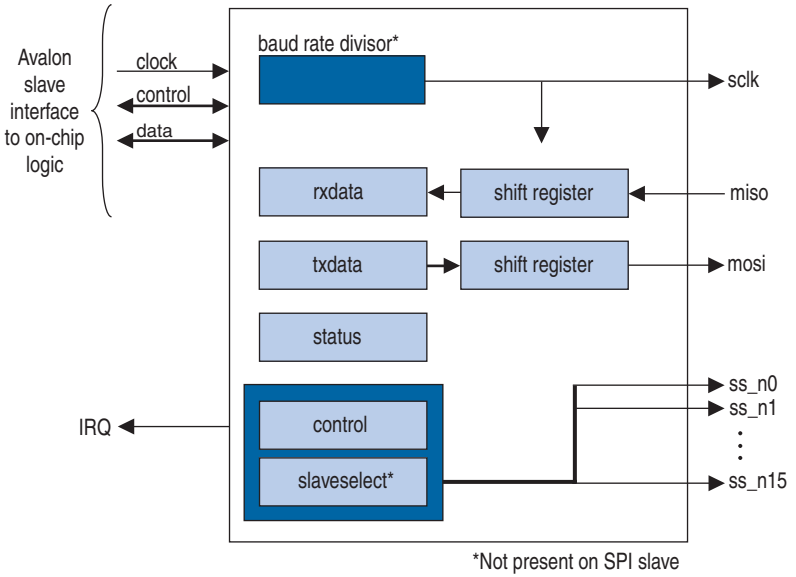
The SPI core has the following user-visible features:

- A memory-mapped register space comprised of five registers: `rxdata`, `txdata`, `status`, `control`, and `slaveselect`
- Four SPI interface ports: `sclk`, `ss_n`, `mosi`, and `miso`

The registers provide an interface to the SPI core and are visible via the Avalon slave port. The `sclk`, `ss_n`, `mosi`, and `miso` ports provide the hardware interface to other SPI devices. The behavior of `sclk`, `ss_n`, `mosi`, and `miso` depends on whether the SPI core is configured as a master or slave.

Figure 7–1 shows a block diagram of the SPI core in master mode.

Figure 7–1. SPI Core Block Diagram

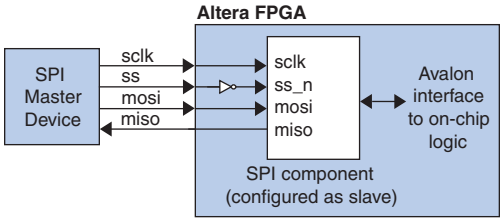


The SPI core logic is synchronous to the clock input provided by the Avalon interface. When configured as a master, the core divides the Avalon clock to generate the SCLK output. When configured as a slave, the core's receive logic is synchronized to SCLK input. The core's Avalon interface is capable of Avalon transfers with flow control. The SPI core can be used in conjunction with a DMA controller with flow control to automate continuous data transfers between, for example, the SPI core and memory. See the *Timer Core with Avalon Interface* chapter for details.

Example Configurations

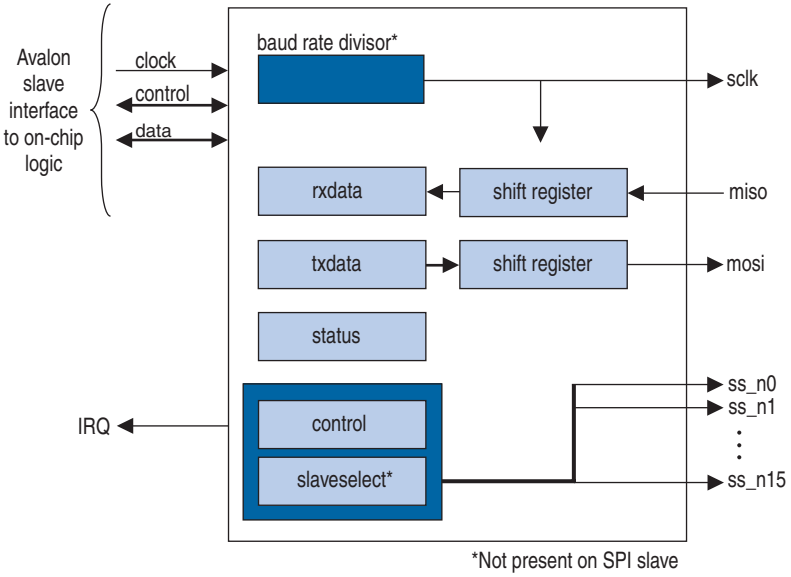
Two possible configurations are shown below. In Figure 7–2, the SPI core provides a slave interface to an off-chip SPI master.

Figure 7–2. SPI Core Configured as a Slave



In Figure 7–3 the SPI core provides a master interface driving multiple off-chip slave devices. Each slave device in Figure 7–3 must tristate its `miso` output whenever its select signal is not asserted.

Figure 7–3. SPI Core Configured as a Master



The `ss_n` signal is active-low. However, any signal can be inverted inside the FPGA, allowing the slave-select signals to be either active high or active low.

Transmitter Logic

The SPI core transmitter logic consists of a transmit holding register (`txdata`) and transmit shift register, each *n* bits wide. The register width *n* is specified at system generation time, and can be any integer value from 1 to 16. After a master peripheral writes a value to the `txdata` register, the value is copied to the shift register and then transmitted when the next operation starts.

The shift register and the `txdata` register provide double buffering during data transmission. A new value can be written into the `txdata` register while the previous data is being shifted out of the shift register. The transmitter logic automatically transfers the `txdata` register to the shift register whenever a serial shift operation is not currently in process.

In master mode, the transmit shift register directly feeds the `mosi` output. In slave mode, the transmit shift register directly feeds the `miso` output. Data shifts out least-significant bit (LSB) first or most-significant bit (MSB) first, depending on the configuration of the SPI core.

Receiver Logic

The SPI core receive logic consists of a receive holding register (`rxdata`) and receive shift register, each *n* bits wide. The register width *n* is specified at system generation time, and can be any integer value from 1 to 16. A master peripheral reads received data from the `rxdata` register after the shift register has captured a full *n*-bit value of data.

The shift register and the `rxdata` register provide double buffering during data receiving. The `rxdata` register can hold a previously received data value while subsequent new data is shifting into the shift register. The receiver logic automatically transfers the shift register content to the `rxdata` register when a serial shift operation completes.

In master mode, the shift register is fed directly by the `miso` input. In slave mode, the shift register is fed directly by the `mosi` input. The receiver logic expects input data to arrive least-significant bit (LSB) first or most-significant bit (MSB) first, depending on the configuration of the SPI core.

Master & Slave Modes

At system generation time, the designer configures the SPI core in either master mode or slave mode. The mode cannot be switched at runtime.

Master Mode Operation

In master mode, the SPI ports behave as shown in Table 7–1.

Table 7–1. Master Mode Port Configurations

Name	Direction	Description
mosi	output	Data output to slave(s)
miso	input	Data input from slave(s)
sclk	output	Synchronization clock to all slaves
ss_n*M*	output	Slave select signal to slave *M*, where M is a number between 0 and 15.

Only an SPI master can initiate an operation between master and slave. In master mode, an intelligent host (e.g., a microprocessor) configures the SPI core using the control and slaveselect registers, and then writes data to the txdata buffer to initiate a transaction. A master peripheral can monitor the status of the transaction by reading the status register. A master peripheral can enable interrupts to notify the host whenever new data is received (i.e., a transfer has completed), or whenever the transmit buffer is ready for new data.

The SPI protocol is full duplex, so every transaction both sends and receives data at the same time. The master transmits a new data bit on the mosi output and the slave drives a new data bit on the miso input for each active edge of sclk. The SPI core divides the Avalon system clock using a clock divider to generate the sclk signal.

When the SPI core is configured to interface with multiple slaves, the core has one ss_n signal for each slave, up to a maximum of sixteen slaves. During a transfer, the master asserts ss_n to each slave specified in the slaveselect register. Note that there can be no more than one slave transmitting data during any particular transfer, or else there will be a conflict on the miso input. The number of slave devices is specified at system generation time.

Slave Mode Operation

In slave mode, the SPI ports behave as shown in Table 7–2.

Table 7–2. Slave Mode Port Configurations

Name	Direction	Description
mosi	input	Data input from the master
miso	output	Data output to the master
sclk	input	Synchronization clock
ss_n	input	Select signal

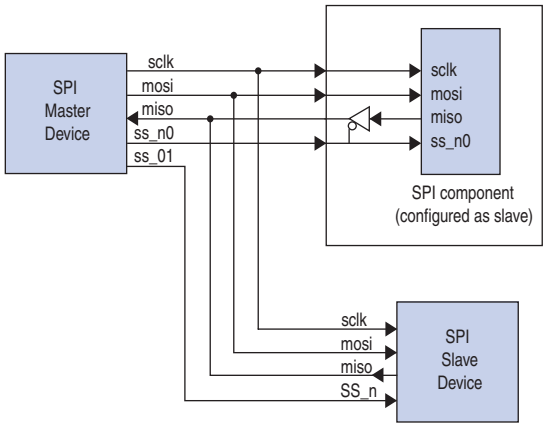
In slave mode, the SPI core simply waits for the master to initiate transactions. Before a transaction begins, the slave logic is continuously polling the ss_n input. When the master asserts ss_n (drives it low), the slave logic immediately begins sending the transmit shift register contents to the miso output. The slave logic also captures data on the mosi input, and fills the receive shift register simultaneously. Thus, a read and write transaction are carried out simultaneously.

An intelligent host (e.g., a microprocessor) writes data to the txdata registers, so that it will be transmitted the next time the master initiates an operation. A master peripheral reads received data from the rxdata register. A master peripheral can enable interrupts to notify the host whenever new data is received, or whenever the transmit buffer is ready for new data.

Multi-Slave Environments

When ss_n is not asserted, typical SPI cores set their miso output pins to high impedance. The Altera®-provided SPI slave core drives an undefined high or low value on its miso output when not selected. Special consideration is necessary to avoid signal contention on the miso output, if the SPI core in slave mode will be connected to an off-chip SPI master device with multiple slaves. In this case, the ss_n input should be used to control a tristate buffer on the miso signal. Figure 7–4 shows an example of the SPI core in slave mode in an environment with two slaves.

Figure 7–4. SPI Core in a Multi-Slave Environment



Avalon Interface

The SPI core's Avalon interface consists of a single Avalon slave port. In addition to fundamental slave read and write transfers, the SPI core supports Avalon read and write transfers with flow control.

Instantiating the SPI Core in SOPC Builder

The hardware feature set is configured via the SPI core's SOPC Builder configuration wizard. The following sections describe the available options.

Master/Slave Settings

The designer can select either master mode or slave mode to determine the role of the SPI core. When master mode is selected, the following options are available: **Generate Select Signals**; **SPI Clock Rate**; and **Specify Delay**.

Generate Select Signals

This setting specifies how many slaves the SPI master will connect to. The acceptable range is 1 to 16. The SPI master core presents a unique `ss_n` signal for each slave.

SPI Clock (sclk) Rate

This setting determines the rate of the sclk signal that synchronizes data between master and slaves. The target clock rate can be specified in units of Hz, kHz or MHz. The SPI master core uses the Avalon system clock and a clock divisor to generate sclk.

The actual frequency of sclk may not exactly match the desired target clock rate. The achievable clock values are:

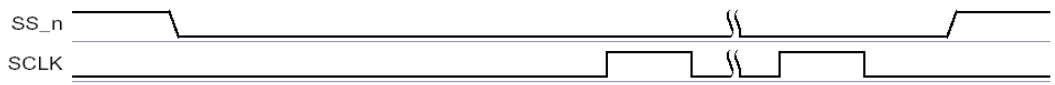
<*Avalon system clock frequency*> / [2, 4, 6, 8, ...]

The actual frequency achieved will not be greater than the specified target value. For example, if the system clock frequency is 50 MHz and the target value is 25 MHz, then the clock divisor is 2 and the actual sclk frequency achieves exactly 25 MHz. However, if the target frequency is 24 MHz, then the clock divisor is 4 and the actual sclk frequency becomes 12.5 MHz.

Specify Delay

Turning on this option causes the SPI master to add a time delay between asserting the ss_n signal and shifting the first bit of data. This delay is required by certain SPI slave devices. If the delay option is turned on, the designer must also specify the delay time in units of ns, us or ms. An example is shown in Figure 7–5.

Figure 7–5. Time Delay Between Asserting ss_n & Toggling sclk



The delay generation logic uses a granularity of half the period of sclk. The actual delay achieved is the desired target delay rounded up to the nearest multiple of half the sclk period, as shown in the following equations:

p = ½ * <*period of sclk*>

actual delay = ceiling(<*desired delay*> / p) * p

Data Register Settings

The data register settings affect the size and behavior of the data registers in the SPI core. There are two data register settings:

- *Width*—This setting specifies the width of `rxdata`, `txdata`, and the receive and transmit shift registers. Acceptable values are from 1 to 16.
- *Shift direction*—This setting determines the direction that data shifts (MSB first or LSB first) into and out of the shift registers.

Timing Settings

The timing settings affect the timing relationship between the `ss_n`, `sclk`, `mosi` and `miso` signals. In this discussion the `mosi` and `miso` signals are referred to generically as "data". There are two timing settings:

- *Clock polarity*—This setting can be 0 or 1. When clock polarity is set to 0, the idle state for `sclk` is low. When clock polarity is set to 1, the idle state for `sclk` is high.
- *Clock phase*—This setting can be 0 or 1. When clock phase is 0, data is latched on the leading edge of `sclk`, and data changes on trailing edge. When clock phase is 1, data is latched on the trailing edge of `sclk`, and data changes on the leading edge.

Figures 7–6 through 7–9 demonstrate the behavior of signals in all possible cases of clock polarity and clock phase.

Figure 7–6. Clock Polarity = 0, Clock Phase = 0

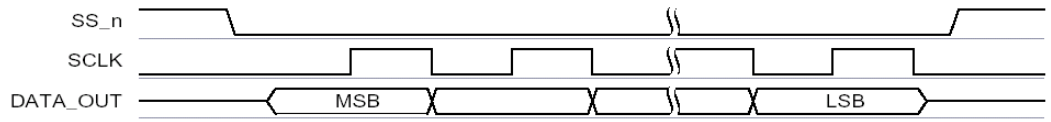


Figure 7–7. Clock Polarity = 0, Clock Phase = 1

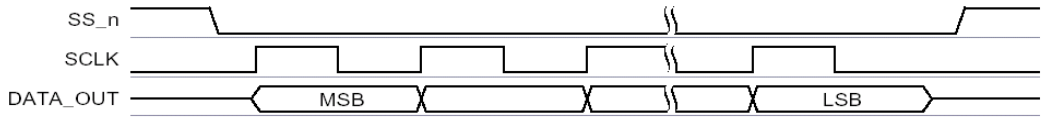


Figure 7–8. Clock Polarity = 1, Clock Phase = 0

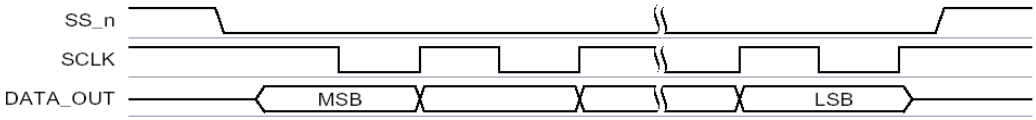
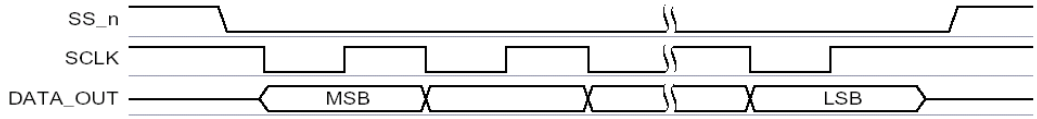


Figure 7–9. Clock Polarity = 1, Clock Phase = 1



Device & Tools Support

The SPI core can target all Altera FPGAs.

Software Programming Model

The following sections describe the software programming model for the SPI core, including the register map and software constructs used to access the hardware. For Nios® II processor users, Altera provides the HAL system library header file that defines the SPI core registers. The SPI core does not match the generic device model categories supported by the HAL, so it cannot be accessed via the HAL API or the ANSI C standard library. Altera provides a routine to access the SPI hardware that is specific to the SPI core.

Hardware Access Routines

Altera provides one access routine, `alt_avalon_spi_command()`, that provides general-purpose access to an SPI core configured as a master.

alt_avalon_spi_command()

Prototype:

```
int alt_avalon_spi_command(alt_u32 base, alt_u32 slave,
                           alt_u32 write_length,
                           const alt_u8* wdata,
                           alt_u32 read_length,
                           alt_u8* read_data,
                           alt_u32 flags)
```

Thread-safe: No.

Available from ISR: No.

Include: **<altera_avalon_spi.h>**

Description: `alt_avalon_spi_command()` is used to perform a control sequence on the SPI bus. This routine is designed for SPI masters of 8-bit data width or less. Currently, it does not support SPI hardware with data-width greater than 8 bits. A single call to this function writes a data buffer of arbitrary length out the MOSI port, and then reads back an arbitrary amount of data from the MISO port. The function performs the following actions:

(1) Asserts the slave select output for the specified slave. The first slave select output is numbered 0, the next is 1, etc.
(2) Transmits `write_length` bytes of data from `wdata` through the SPI interface, discarding the incoming data on MISO.
(3) Reads `read_length` bytes of data, storing the data into the buffer pointed to by `read_data`. MOSI is set to zero during the read transaction.
(4) Deasserts the slave select output, unless the flags field contains the value `ALT_AVALON_SPI_COMMAND_MERGE`. If you want to transmit from scattered buffers then you can call the function multiple times, specifying the merge flag on all the accesses except the last.

This function is not thread safe. If you want to access the SPI bus from more than one thread, then you should use a semaphore or mutex to ensure that only one thread is executing within this function at any time.

Returns: The number of bytes stored in the `read_data` buffer.

Software Files

The SPI core is accompanied by the following software files. These files provide a low-level interface to the hardware.

- **altera_avalon_spi.h**—This file defines the core's register map, providing symbolic constants to access the low-level hardware.
- **altera_avalon_spi.c**—This file implements low-level routines to access the hardware.

Legacy SDK Routines

The SPI core is also supported by the legacy SDK routines for the first-generation Nios processor. For details on these routines, refer to the SPI documentation that accompanied the first-generation Nios processor. For details on upgrading programs based on the legacy SDK to the HAL system library API, refer to *AN 350: Upgrading Nios Processor Systems to the Nios II Processor*.

Register Map

An Avalon master peripheral controls and communicates with the SPI core via the six 16-bit registers, shown in Table 7–3. The table assumes an *n*-bit data width for `rxdata` and `txdata`.

Table 7–3. Register Map for SPI Master Device

Internal Address	Register Name	15…11	10	9	8	7	6	5	4	3	2	1	0
0	`rxdata` *(1)*	RXDATA (n-1..0)											
1	`txdata` *(1)*	TXDATA (n-1..0)											
2	`status` *(2)*				E	RRDY	TRDY	TMT	TOE	ROE			
3	`control`		sso *(3)*		IE	IRRDY	ITRDY		ITOE	IROE			
4	Reserved												
5	`slaveselect` *(3)*	Slave Select Mask											

Notes to Table 7–3:

(1) Bits 15 to *n* are undefined when *n* is less than 16.

(2) A write operation to the `status` register clears the `roe`, `toe` and `e` bits.

(3) Present only in master mode.

Reading undefined bits returns an undefined value. Writing to undefined bits has no effect.

rxdata Register

A master peripheral reads received data from the `rxdata` register. When the receive shift register receives a full *n* bits of data, the `status` register's `rrdy` bit is set to 1 and the data is transferred into the `rxdata` register. Reading the `rxdata` register clears the `rrdy` bit. Writing to the `rxdata` register has no effect.

New data is always transferred into the `rxdata` register, whether or not the previous data was retrieved. If `rrdy` is 1 when data is transferred into the `rxdata` register (i.e., the previous data was not retrieved), a receive-overrun error occurs and the `status` register's `roe` bit is set to 1. In this case, the contents of `rxdata` are undefined.

txdata Register

A master peripheral writes data to be transmitted into the `txdata` register. When the `status` register's `trdy` bit is 1, it indicates that the `txdata` register is ready for new data. The `trdy` bit is set to 0 whenever the `txdata` register is written. The `trdy` bit is set to 1 after data is transferred from the `txdata` register into the transmitter shift register, which readies the `txdata` holding register to receive new data.

A master peripheral should not write to the `txdata` register until the transmitter is ready for new data. If `trdy` is 0 and a master peripheral writes new data to the `txdata` register, a transmit-overrun error occurs and the `status` register's `toe` bit is set to 1. In this case, the new data is ignored, and the content of `txdata` remains unchanged.

As an example, assume that the SPI core is idle (i.e., the `txdata` register and transmit shift register are empty), when a CPU writes a data value into the `txdata` holding register. The `trdy` bit is set to 0 momentarily, but after the data in `txdata` is transferred into the transmitter shift register, `trdy` returns to 1. The CPU writes a second data value into the `txdata` register, and again the `trdy` bit is set to 0. This time the shift register is still busy transferring the original data value, so the `trdy` bit remains at 0 until the shift operation completes. When the operation completes, the second data value is transferred into the transmitter shift register and the `trdy` bit is again set to 1.

status Register

The `status` register consists of bits that indicate status conditions in the SPI core. Each bit is associated with a corresponding interrupt-enable bit in the `control` register, as discussed in "control Register" on page 7–14.

A master peripheral can read status at any time without changing the value of any bits. Writing status does clear the roe, toe and e bits. Table 7–4 describes the individual bits of the status register.

Table 7–4. status Register Bits

#	Name	Description
3	ROE	**Receive-overrun error** The ROE bit is set to 1 if new data is received while the rxdata register is full (that is, while the RRDY bit is 1). In this case, the new data overwrites the old. Writing to the status register clears the ROE bit to 0.
4	TOE	**Transmitter-overrun error** The TOE bit is set to 1 if new data is written to the txdata register while it is still full (that is, while the TRDY bit is 0). In this case, the new data is ignored. Writing to the status register clears the TOE bit to 0.
5	TMT	**Transmitter shift-register empty** The TMT bit is set to 0 when a transaction is in progress and set to 1 when the shift register is empty.
6	TRDY	**Transmitter ready** The TRDY bit is set to 1 when the txdata register is empty.
7	RRDY	**Receiver ready** The RRDY bit is set to 1 when the rxdata register is full.
8	E	**Error** The E bit is the logical OR of the TOE and ROE bits. This is a convenience for the programmer to detect error conditions. Writing to the status register clears the E bit to 0.

control Register

The control register consists of data bits to control the SPI core's operation. A master peripheral can read control at any time without changing the value of any bits.

Most bits (IROE, ITOE, ITRDY, IRRDY, and IE) in the control register control interrupts for status conditions represented in the status register. For example, bit 1 of status is ROE (receiver-overrun error), and bit 1 of control is IROE, which enables interrupts for the ROE condition. The SPI core asserts an interrupt request when the corresponding bits in status and control are both 1.

The control register bits are shown in Table 7–5.

Table 7–5. control Register Bits

#	Name	Description
3	IROE	Setting IROE to 1 enables interrupts for receive-overrun errors.
4	ITOE	Setting ITOE to 1 enables interrupts for transmitter-overrun errors.
6	ITRDY	Setting ITRDY to 1 enables interrupts for the transmitter ready condition.
7	IRRDY	Setting IRRDY to 1 enables interrupts for the receiver ready condition.
8	IE	Setting IE to 1 enables interrupts for any error condition.
10	SSO	Setting SSO to 1 forces the SPI core to drive its `ss_n` outputs, regardless of whether a serial shift operation is in progress or not. The `slaveselect` register controls which `ss_n` outputs are asserted. `sso` can be used to transmit or receive data of arbitrary size (i.e., greater than 16 bits).

After reset, all bits of the control register are set to 0. All interrupts are disabled and no `ss_n` signals are asserted after reset.

slaveselect Register

The `slaveselect` register is a bit mask for the `ss_n` signals driven by an SPI master. During a serial shift operation, the SPI master selects only the slave device(s) specified in the `slaveselect` register.

The `slaveselect` register is only present when the SPI core is configured in master mode. There is one bit in `slaveselect` for each `ss_n` output, as specified by the designer at system generation time. For example, to enable communication with slave device 3, set bit 3 of `slaveselect` to 1.

A master peripheral can set multiple bits of `slaveselect` simultaneously, causing the SPI master to simultaneously select multiple slave devices as it performs a transaction. For example, to enable communication with slave devices 1, 5, and 6, set bits 1, 5, and 6 of `slaveselect`. However, consideration is necessary to avoid signal contention between multiple slaves on their `miso` outputs.

Upon reset, bit 0 is set to 1, and all other bits are cleared to 0. Thus, after a device reset, slave device 0 is automatically selected.

Section III. Display Peripherals

This section describes display interface peripherals provided by Altera®. These components provide interfaces to visual display devices for SOPC Builder systems.

See *About This Handbook* for further details.

This section includes the following chapter:

Revision History

The table below shows the revision history for Chapter 8.

Chapter(s)	Date / Version	Changes Made
8	May 2006, v6.0.0	Chapter title changed, but no change in content from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	September 2004, v1.0	First publication.

8. Optrex 16207 LCD Controller Core with Avalon Interface

NII51019-6.0.0

Core Overview

The Optrex 16207 LCD Controller Core with Avalon® Interface ("the LCD controller") provides the hardware interface and software driver required for a Nios® II processor to display characters on an Optrex 16207 (or equivalent) 16x2-character LCD panel. Device drivers are provided in the HAL system library for the Nios II processor. Nios II programs access the LCD controller as a character mode device using ANSI C standard-library routines, such as `printf()`. The LCD controller is SOPC Builder-ready, and integrates easily into any SOPC Builder-generated system.

The Nios II Embedded Design Suite (EDS) includes an Optrex LCD module and provide several ready-made example designs that display text on the Optrex 16207 via the LCD controller. For details on the Optrex 16207 LCD module, see the manufacturer's *Dot Matrix Character LCD Module User's Manual* available at **http://www.optrex.com**.

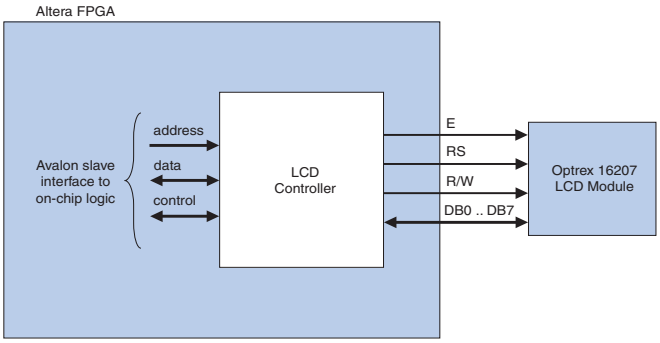
Functional Description

The LCD controller hardware consists of two user-visible components:

1. Eleven signals that connect to pins on the Optrex 16207 LCD panel – These signals are defined in the Optrex 16207 data sheet.
   - `E` – Enable (output)
   - `RS` – Register Select (output)
   - `R/W` – Read or Write (output)
   - `DB0` through `DB7` – Data Bus (bidirectional)
2. An Avalon slave interface that provides access to 4 registers – The HAL device drivers make it unnecessary for users to access the registers directly. Therefore, Altera does not provide details on the register usage. For further details, see "Software Programming Model" on page 8–2.

Figure 8–1 shows a block diagram of the LCD controller core.

Figure 8–1. LCD Controller Block Diagram



Device & Tools Support

The LCD controller hardware supports all Altera FPGA families. The LCD controller drivers support the Nios II processor. The drivers do not support the first-generation Nios processor.

Instantiating the Core in SOPC Builder

In SOPC Builder, the LCD controller component has the name Character LCD (16x2, Optrex 16207). The LCD controller does not have any user-configurable settings. The only choice to make in SOPC Builder is whether or not to add an LCD controller to the system. For each LCD controller included in the system, the top-level system module includes the 11 signals that connect to the LCD module.

Software Programming Model

This section describes the software programming model for the LCD controller.

HAL System Library Support

Altera provides HAL system library drivers for the Nios II processor that enable you to access the LCD controller using the ANSI C standard library functions. The Altera-provided drivers integrate into the HAL system library for Nios II systems. The LCD driver is a standard character-mode device, as described in the *Nios II Software Developer's Handbook*. Therefore, using `printf()` is the easiest was to write characters to the display.

The LCD driver requires that the HAL system library include the system clock driver.

Displaying Characters on the LCD

The driver implements VT100 terminal-like behavior on a miniature scale for the 16x2 screen. Characters written to the LCD controller are stored to an 80-column x 2-row buffer maintained by the driver. As characters are written, the cursor position is updated. Visible characters move the cursor position to the right. Any visible characters written to the right of the buffer are discarded. The line feed character (\n) moves the cursor down one line and to the left-most column.

The buffer is scrolled up as soon as a printable character is written onto the line below the bottom of the buffer. Rows do not scroll as soon as the cursor moves down to allow the maximum useful information in the buffer to be displayed.

If the visible characters in the buffer will fit on the display, then all characters are displayed. If the buffer is wider than the display, then the display scrolls horizontally to display all the characters. Different lines scroll at different speeds, depending on the number of characters in each line of the buffer.

The LCD driver understands a small subset of ANSI and VT100 escape sequences which can be used to control the cursor position, and clear the display as shown in Table 8–1.

Table 8–1. Escape Sequence Supported by the LCD Controller

Sequence	Meaning
BS (\b)	Moves the cursor to the left by one character.
CR (\r)	Moves the cursor to the start of the current line.
LF (\n)	Moves the cursor to the start of the line and move it down one line.
ESC((\x1B)	Starts a VT100 control sequence.
ESC [<y> ; <x> H	Moves the cursor to the y, x position specified – positions are counted from the top left which is 1;1.
ESC [K	Clears from current cursor position to end of line.
ESC [2 J	Clears the whole screen.

The LCD controller is an output-only device. Therefore, attempts to read from it will return immediately indicating that no characters have been received.

The LCD controller drivers are not included in the system library when the **Reduced device drivers** option is enabled for the system library. If you want to use the LCD controller while using small drivers for other devices, then add the preprocessor option `-DALT_USE_LCD_16207` to the preprocessor options.

Software Files

The LCD controller is accompanied by the following software files. These files define the low-level interface to the hardware and provide the HAL drivers. Application developers should not modify these files.

- **altera_avalon_lcd_16207_regs.h** — This file defines the core's register map, providing symbolic constants to access the low-level hardware.
- **altera_avalon_lcd_16207.h, altera_avalon_lcd_16207.c** — These files implement the LCD controller device drivers for the HAL system library.

Register Map

The HAL device drivers make it unnecessary for you to access the registers directly. Therefore, Altera does not publish details on the register map. For more information, the **altera_avalon_lcd_16207_regs.h** file describes the register map, and the *Dot Matrix Character LCD Module User's Manual* from Optrex describes the register usage.

Interrupt Behavior

The LCD controller does not generate interrupts. However, the LCD driver's text scrolling feature relies on the HAL system clock driver, which uses interrupts for timing purposes.

Section IV. Multiprocessor Coordination Peripherals

This section describes multiprocessor coordination peripherals provided by Altera® for SOPC Builder systems. These components provide reliable mechanisms for multiple Nios® II processors to communicate with each other, and coordinate operations.

See *About This Handbook* for further details.

This section includes the following chapters:

- Chapter 9, Mutex Core with Avalon Interface
- Chapter 10, Mailbox Core with Avalon Interface

Revision History

The table below shows the revision history for Chapters 9–10.

Chapter(s)	Date / Version	Changes Made
9	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	December 2004, v1.0	First publication.
10	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	First publication.

9. Mutex Core with Avalon Interface

NII51020-6.0.0

Core Overview

Multiprocessor environments can use the mutex core with Avalon® interface (the mutex core) to coordinate accesses to a shared resource. The mutex core provides a protocol to ensure mutually exclusive ownership of a shared resource.

The mutex core provides a hardware-based atomic test-and-set operation, allowing software in a multiprocessor environment to determine which processor owns the mutex. The mutex core can be used in conjunction with shared memory to implement additional interprocessor coordination features, such as mailboxes and software mutexes.

The mutex core is designed for use in Avalon-based processor systems, such as a Nios® II processor system. Altera provides device drivers for the Nios II processor to enable use of the hardware mutex.

The mutex core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

Functional Description

The mutex core has a simple Avalon slave interface that provides access to two memory-mapped, 32-bit registers. Table 9–1 shows the registers.

Table 9–1. Mutex Core Register Map

Offset	Register Name	R/W	Bit Description		
			31 … 16	15 … 1	0
0	mutex	RW	OWNER	VALUE	
1	reset	RW	–	–	RESET

The mutex core has the following basic behavior. This description assumes there are multiple processors accessing a single mutex core, and each processor has a unique identifier (ID).

- When the VALUE field is 0x0000, the mutex is available (i.e, unlocked). Otherwise, the mutex is unavailable (i.e., locked).
- The mutex register is always readable. A processor (or any Avalon master peripheral) can read the mutex register to determine its current state.

- The mutex register is writeable only under specific conditions. A write operation changes the mutex register only if one or both of the following conditions is true:
  - The VALUE field of the mutex register is zero.
  - The OWNER field of the mutex register matches the OWNER field in the data to be written.
- A processor attempts to acquire the mutex by writing its ID to the OWNER field, and writing a non-zero value to VALUE. The processor then checks if the acquisition succeeded by verifying the OWNER field.
- After system reset, the RESET bit in the reset register is high. Writing a one to this bit clears it.

Device & Tools Support

The mutex core supports all Altera device families supported by SOPC Builder, and provides device drivers for the Nios II hardware abstraction layer (HAL) system library.

Instantiating the Core in SOPC Builder

Hardware designers use the mutex core's SOPC Builder configuration wizard to specify the core's hardware features. The configuration wizard provides the following settings:

- **Initial Value**—the initial contents of the VALUE field after reset. If the **Initial Value** setting is non-zero, you must also specify **Initial Owner**.
- **Initial Owner**—the initial contents of the OWNER field after reset. When **Initial Owner** is specified, this owner must release the mutex before it can be acquired by another owner.

Software Programming Model

The following sections describe the software programming model for the mutex core, such as the software constructs used to access the hardware. For Nios II processor users, Altera provides routines to access the mutex core hardware. These functions are specific to the mutex core and directly manipulate low-level hardware. The mutex core cannot be accessed via the HAL API or the ANSI C standard library. In Nios II processor systems, a processor locks the mutex by writing the value of its cpuid control register to the OWNER field of the mutex register.

Software Files

Altera provides the following software files accompanying the mutex core:

- **altera_avalon_mutex_regs.h**—this file defines the core's register map, providing symbolic constants to access the low-level hardware.

- **altera_avalon_mutex.h—**this file defines data structures and functions to access the mutex core hardware.
- **altera_avalon_mutex.c**—this file contains the implementations of the functions to access the mutex core

Hardware Mutex

This section describes the low-level software constructs for manipulating the mutex core hardware.

The file **altera_avalon_mutex.h** declares a structure `alt_mutex_dev` that represents an instance of a mutex device. It also declares functions for accessing the mutex hardware structure, listed in Table 9–2.

Table 9–2. Hardware Mutex Functions

Function Name	Description
`altera_avalon_mutex_open()`	Claims a handle to a mutex, enabling all the other functions to access the mutex core.
`altera_avalon_mutex_trylock()`	Tries to lock the mutex. Returns immediately if it fails to lock the mutex.
`altera_avalon_mutex_lock()`	Locks the mutex. Will not return until it has successfully claimed the mutex.
`altera_avalon_mutex_unlock()`	Unlocks the mutex.
`altera_avalon_mutex_is_mine()`	Determines if this CPU owns the mutex.
`altera_avalon_mutex_first_lock()`	Tests whether the mutex has been released since reset.

These routines coordinate access to the software mutex structure using a hardware mutex core. For a complete description of each function, see section "Mutex API" on page 9–5.

The following code demonstrates opening a mutex device handle and locking a mutex:

Example: Opening and locking a mutex

```
#include <altera_avalon_mutex.h>

/* get the mutex device handle */
alt_mutex_dev* mutex = altera_avalon_mutex_open( "/dev/mutex" );

/* acquire the mutex, setting the value to one */
altera_avalon_mutex_lock( mutex, 1 );

/*
 * Access a shared resource here.
 */

/* release the lock */
altera_avalon_mutex_unlock( mutex );
```

Mutex API

This section describes the application programming interface (API) for the mutex core.

altera_avalon_mutex_is_mine()

Prototype:	`int altera_avalon_mutex_is_mine(alt_mutex_dev* dev)`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mutex.h**>
Parameters:	`dev`—the mutex device to test.
Returns:	Returns non zero if the mutex is owned by this CPU.
Description:	`altera_avalon_mutex_is_mine()` determines if this CPU owns the mutex.

altera_avalon_mutex_first_lock()

Prototype:	`int altera_avalon_mutex_first_lock(alt_mutex_dev* dev)`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mutex.h**>
Parameters:	`dev`—the mutex device to test.
Returns:	Returns 1 if this mutex has not been released since reset, otherwise returns 0.
Description:	`altera_avalon_mutex_first_lock()` determines whether this mutex has been released since reset.

altera_avalon_mutex_lock()

Prototype:	`void altera_avalon_mutex_lock(alt_mutex_dev* dev, alt_u32 value)`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mutex.h**>
Parameters:	`dev`—the mutex device to acquire. `value`—the new value to write to the mutex.
Returns:	–
Description:	`altera_avalon_mutex_lock()` is a blocking routine that acquires a hardware mutex, and at the same time, loads the mutex with the `value` parameter.

altera_avalon_mutex_open()

Prototype:	`alt_mutex_dev* alt_hardware_mutex_open(const char* name)`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mutex.h**>
Parameters:	`name`—the name of the mutex device to open.
Returns:	A pointer to the mutex device structure associated with the supplied name, or NULL if no corresponding mutex device structure was found.
Description:	`altera_avalon_mutex_open()` retrieves a pointer to a hardware mutex device structure.

altera_avalon_mutex_trylock()

Prototype:	`int altera_avalon_mutex_trylock(alt_mutex_dev* dev, alt_u32 value)`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mutex.h**>
Parameters:	`dev`—the mutex device to lock. `value`—the new value to write to the mutex.
Returns:	Zero if the mutex was successfully locked, or non zero if the mutex was not locked.
Description:	`altera_avalon_mutex_trylock()` tries once to lock the hardware mutex, and returns immediately.

altera_avalon_mutex_unlock()

Prototype:	`void altera_avalon_mutex_unlock(alt_mutex_dev* dev)`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mutex.h**>
Parameters:	`dev`—the mutex device to unlock.
Returns:	-
Description:	`altera_avalon_mutex_unlock()` releases a hardware mutex device. Upon release, the value stored in the mutex is set to zero. If the caller does not hold the mutex, the behavior of this function is undefined.

10. Mailbox Core with Avalon Interface

NII53001-6.0.0

Core Overview

Multiprocessor environments can use the mailbox core with Avalon® interface (the mailbox core) to send messages between processors.

The mailbox core contains mutexes to ensure that only one processor modifies the mailbox contents at a time. The mailbox core must be used in conjunction with a separate shared memory which is used for storing the actual messages.

The mailbox core is designed for use in Avalon-based processor systems, such as a Nios® II processor system. Altera® provides device drivers for the Nios II processor. The mailbox core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

Functional Description

The mailbox core has a simple Avalon slave interface that provides access to four memory-mapped, 32-bit registers. Table 10–1 shows the registers.

Table 10–1. Mutex Core Register Map

Offset	Register Name	R/W	Bit Description		
			31 … 16	15 … 1	0
0	mutex0	RW	OWNER	VALUE	
1	reset0	RW	–	–	RESET
2	mutex1	RW	OWNER	VALUE	
3	reset1	RW	–	–	RESET

The mailbox component contains two mutexes: One to ensure unique write access to shared memory and one to ensure unique read access from shared memory. The mailbox core is used in conjunction with a separate memory in the system which is shared among multiple processors.

Mailbox functionality using the mutexes and memory is implemented entirely in software. Refer to "Software Programming Model" on page 10–3 for details of how to use the mailbox core in software.

For a detailed description of the mutex hardware operation, see the *Mutex Core with Avalon Interface* chapter.

Device & Tools Support

The mailbox core supports all Altera device families supported by SOPC Builder, and provides device drivers for the Nios II hardware abstraction layer (HAL) system library.

Instantiating the Core in SOPC Builder

Hardware designers instantiate and configure the mailbox core in an SOPC Builder system using the following process.

1. Decide which processors will share the mailbox.
2. On the SOPC Builder **System Contents** tab, instantiate a memory component to serve as the mailbox buffer. Any RAM can be used as the mailbox buffer. The mailbox buffer can share space in an existing memory, such as program memory; it does not require a dedicated memory.
3. On the SOPC Builder **System Contents** tab, instantiate the mailbox component. The mailbox configuration wizard presents no configurable settings.
4. Make connections on the SOPC Builder **System Contents** tab.
    a. Connect each processor's data bus master port to the mailbox slave port.
    b. Connect each processor's data bus master port to the shared mailbox memory.
5. Configure the mailbox core with the **More** <*mailbox name*> **Settings** tab. This tab is available in the SOPC Builder graphical user interface (GUI) whenever a mailbox component exists in the system.

The **More** <*mailbox name*> **Settings** tab provides the following options:

- **Memory module** - Specifies which memory to use for the mailbox buffer. If the **Memory module** list does not contain the desired shared memory, the memory is not connected in the system correctly. Refer to Step 4 on page page 10–2.
- **Shared Mailbox Memory Offset** - Specifies an offset into the memory. The mailbox message buffer starts at this offset.
- **Mailbox Size (bytes)** - Specifies the number of bytes to use for the mailbox message buffer. The Nios II driver software provided by Altera uses eight bytes of overhead to implement the mailbox functionality. For a mailbox capable of passing only one message at a time, **Mailbox Size (bytes)** must be at least 12 bytes.

Software Programming Model

The following sections describe the software programming model for the mailbox core, such as the software constructs used to access the hardware. For Nios II processor users, Altera provides routines to access the mailbox core hardware. These functions are specific to the mailbox core and directly manipulate low-level hardware.

The mailbox software programming model has the following characteristics and assumes there are multiple processors accessing a single mailbox core and a shared memory:

- Each mailbox message is one 32-bit word.
- There is a predefined address range in shared memory dedicated to storing messages. The size of this address range imposes a maximum limit on the number of messages pending.
- The mailbox software implements a message FIFO between processors. Only one processor can write to the mailbox at a time, and only one processor can read from the mailbox at a time, ensuring message integrity.
- The software on both the sending and receiving processors must agree on a protocol for interpreting mailbox messages. Typically processors treat the message as a pointer to a structure in shared memory.
- The sending processor can post messages in succession, up to the limit imposed by the size of the message address range.
- When messages exist in the mailbox, the receiving processor can read messages. The receiving processor can block until a message appears, or it can poll the mailbox for new messages.
- Reading the message removes the message from the mailbox.

Software Files

Altera provides the following software files accompanying the mailbox core hardware:

- **altera_avalon_mailbox_regs.h** – Defines the core's register map, providing symbolic constants to access the low-level hardware.
- **altera_avalon_mailbox.h** – Defines data structures and functions to access the mailbox core hardware.
- **altera_avalon_mailbox.c** – Contains the implementations of the functions to access the mailbox core.

Programming with the Mailbox Core

This section describes the software constructs for manipulating the mailbox core hardware.

The file **altera_avalon_mailbox.h** declares a structure `alt_mailbox_dev` that represents an instance of a mailbox device. It also declares functions for accessing the mailbox hardware structure, listed in Table 10–2. For a complete description of each function, see section "Mailbox API" on page 10–6.

Table 10–2. Mailbox API Functions

Function Name	Description
`altera_avalon_mailbox_close()`	Closes the handle to a mailbox.
`altera_avalon_mailbox_get()`	Returns a message if one is present, but does not block waiting for a message.
`altera_avalon_mailbox_open()`	Claims a handle to a mailbox, enabling all the other functions to access the mailbox core.
`altera_avalon_mailbox_pend()`	Blocks waiting for a message to be in the mailbox.
`altera_avalon_mailbox_post()`	Posts a message to the mailbox.

The following code demonstrates writing to and reading from a mailbox. For this example, assume that the hardware system has two processors communicating via mailboxes. The system includes two mailbox cores, which provide two-way communication between the processors.

Example: Writing to and reading from a mailbox

```
#include <stdio.h>
#include "altera_avalon_mailbox.h"

int main()
{
  alt_u32 message = 0;
  alt_mailbox_dev* send_dev, recv_dev;
  /* Open the two mailboxes between this processor and another */
  send_dev = altera_avalon_mailbox_open("/dev/mailbox_0");
  recv_dev = altera_avalon_mailbox_open("/dev/mailbox_1");

  while(1)
  {
    /* Send a message to the other processor */
    altera_avalon_mailbox_post(send_dev, message);

    /* Wait for the other processor to send a message back */
    message = altera_avalon_mailbox_pend(recv_dev);

  }

  return 0;
}
```

Mailbox API

This section describes the application programming interface (API) for the mailbox core.

altera_avalon_mailbox_close()

Prototype:	`void altera_avalon_mailbox_close (alt_mailbox_dev* dev);`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mailbox.h**>
Parameters:	`dev`—the mailbox to close.
Returns:	–
Description:	`altera_avalon_mailbox_close()` closes the mailbox.

altera_avalon_mailbox_get()

Prototype:	`alt_u32 altera_avalon_mailbox_get (alt_mailbox_dev* dev, int* err);`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mailbox.h**>
Parameters:	`dev`—the mailbox handle, `err`—pointer to an error code that is returned.
Returns:	Returns a message if one is available in the mailbox, otherwise returns 0. The value pointed to by `err` is 0 if the message was read correctly, or `EWOULDBLOCK` if there is no message to read.
Description:	`altera_avalon_mutex_get()` returns a message if one is present, but does not block waiting for a message.

altera_avalon_mailbox_open()

Prototype:	`alt_mailbox_dev* altera_avalon_mailbox_open (const char* name);`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mailbox.h**>
Parameters:	`name`—the name of the mailbox device to open.
Returns:	Returns a handle to the mailbox, or NULL if this mailbox does not exist.
Description:	`altera_avalon_mailbox_open()` opens a mailbox.

altera_avalon_mailbox_pend()

Prototype:	`alt_u32 altera_avalon_mailbox_pend (alt_mailbox_dev* dev);`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mailbox.h**>
Parameters:	`dev`—the mailbox device to read a message from.
Returns:	Returns the message.
Description:	`altera_avalon_mailbox_pend()` is a blocking routine that waits for a message to appear in the mailbox and then reads it.

altera_avalon_mailbox_post()

Prototype:	`int altera_avalon_mailbox_post (alt_mailbox_dev* dev, alt_u32 msg);`
Thread-safe:	Yes.
Available from ISR:	No.
Include:	<**altera_avalon_mailbox.h**>
Parameters:	`dev`—the mailbox device to post a message to `msg`—the value to post.
Returns:	Returns 0 on success, or `EWOULDBLOCK` if the mailbox is full.
Description:	`altera_avalon_mailbox_post()` posts a message to the mailbox.

Section V. Other Peripherals

This section describes peripherals provided by Altera® for SOPC Builder systems. The components described in this chapter do not fit the categories described in other sections of this handbook.

See *About This Handbook* for further details.

This section includes the following chapters:

- Chapter 11, PIO Core with Avalon Interface
- Chapter 12, Timer Core with Avalon Interface
- Chapter 13, System ID Core with Avalon Interface
- Chapter 14, PLL Core with Avalon Interface
- Chapter 15, Performance Counter Core with Avalon Interface

Revision History

The table below shows the revision history for Chapters 11–15.

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11	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.
12	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.
13	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	No change from previous release.
	May 2005, v5.0.0	No change from previous release. Previously in the Nios II Processor Reference Handbook.
	September 2004, v1.1	Updates for Nios II 1.01 release.
	May 2004, v1.0	First publication.

Chapter(s)	Date / Version	Changes Made
14	May 2006, v6.0.0	No change from previous release.
	October 2005, v5.1.0	First publication.
15	May 2006, v6.0.0	No change from previous release.
	December 2005, v5.1.0	First publication.

11. PIO Core with Avalon Interface

NII51007-6.0.0

Core Overview

The parallel input/output (PIO) core provides a memory-mapped interface between an Avalon® slave port and general-purpose I/O ports. The I/O ports connect either to on-chip user logic, or to I/O pins that connect to devices external to the FPGA.

The PIO core provides easy I/O access to user logic or external devices in situations where a "bit banging" approach is sufficient. Some example uses are:

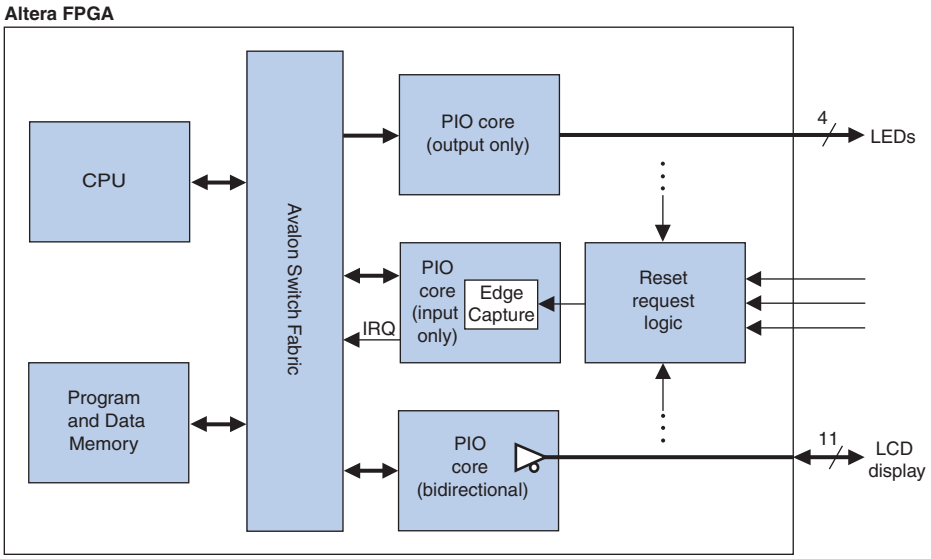
- Controlling LEDs
- Acquiring data from switches
- Controlling display devices
- Configuring and communicating with off-chip devices, such as application-specific standard products (ASSP)

The PIO core interrupt request (IRQ) output can assert an interrupt based on input signals. The PIO core is SOPC Builder ready and integrates easily into any SOPC Builder-generated system.

Functional Description

Each PIO core can provide up to 32 I/O ports. An intelligent host such as a microprocessor controls the PIO ports by reading and writing the register-mapped Avalon interface. Under control of the host, the PIO core captures data on its inputs and drives data to its outputs. When the PIO ports are connected directly to I/O pins, the host can tristate the pins by writing control registers in the PIO core. Figure 11–1 shows an example of a processor-based system that uses multiple PIO cores to blink LEDs, capture edges from on-chip reset-request control logic, and control an off-chip LCD display.

Figure 11–1. An Example System Using Multiple PIO Cores



When integrated into an SOPC Builder-generated system, the PIO core has two user-visible features:

- A memory-mapped register space with four registers: `data`, `direction`, `interruptmask`, and `edgecapture`.
- 1 to 32 I/O ports.

The I/O ports can be connected to logic inside the FPGA, or to device pins that connect to off-chip devices. The registers provide an interface to the I/O ports via the Avalon interface. See Table 11–2 on page 11–7 for a description of the registers. Some registers are not necessary in certain hardware configurations, in which case the unnecessary registers do not exist. Reading a non-existent register returns an undefined value, and writing a non-existent register has no effect.

Data Input & Output

The PIO core I/O ports can connect to either on-chip or off-chip logic. The core can be configured with inputs only, outputs only, or both inputs and outputs. If the core will be used to control bidirectional I/O pins on the device, the core provides a bidirectional mode with tristate control.

The hardware logic is separate for reading and writing the data register. Reading the data register returns the value present on the input ports (if present). Writing data affects the value driven to the output ports (if present). These ports are independent; reading the data register does not return previously-written data.

Edge Capture

The PIO core can be configured to capture edges on its input ports. It can capture low-to-high transitions, high-to-low transitions, or both. Whenever an input detects an edge, the condition is indicated in the `edgecapture` register. The type of edges to detect is specified at system generation time, and cannot be changed via the registers.

IRQ Generation

The PIO core can be configured to generate an IRQ on certain input conditions. The IRQ conditions can be either:

- *Level-sensitive*—The PIO core hardware can detect a high level. A `NOT` gate can be inserted external to the core to provide negative sensitivity.
- *Edge-sensitive*—The core's edge capture configuration determines which type of edge causes an IRQ

Interrupts are individually maskable for each input port. The interrupt mask determines which input port can generate interrupts.

Example Configurations

Figure 11–2 shows a block diagram of the PIO core configured with input and output ports, as well as support for IRQs.

Figure 11–2. PIO Core with Input & Output Ports & with IRQ Support

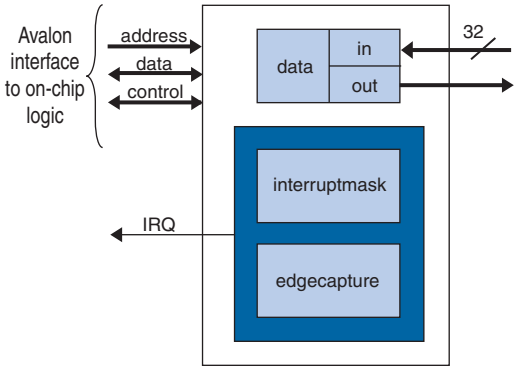
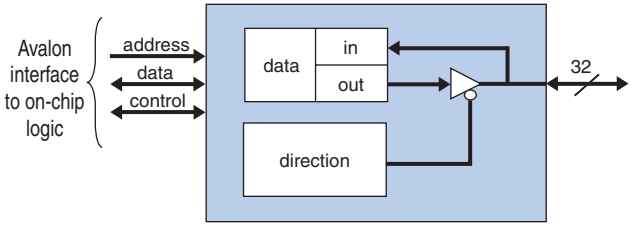


Figure 11–3 shows a block diagram of the PIO core configured in bidirectional mode, without support for IRQs.

Figure 11–3. PIO Core with Bidirectional Ports



Avalon Interface

The PIO core's Avalon interface consists of a single Avalon slave port. The slave port is capable of fundamental Avalon read and write transfers. The Avalon slave port provides an IRQ output so that the core can assert interrupts.

Instantiating the PIO Core in SOPC Builder

The hardware feature set is configured via the PIO core's SOPC Builder configuration wizard. The following sections describe the available options.

The configuration wizard has two tabs, **Basic Settings** and **Input Options**.

Basic Settings

The **Basic Settings** tab allows the designer to specify the width and direction of the I/O ports.

- The **Width** setting can be any integer value between 1 and 32. For a value of *n*, the I/O ports become *n*-bits wide.
- The **Direction** setting has four options, as shown in Table 11–1.

Table 11–1. Direction Settings

Setting	Description
Bidirectional (tristate) ports	In this mode, each PIO bit shares one device pin for driving and capturing data. The direction of each pin is individually selectable. To tristate an FPGA I/O pin, set the direction to input.
Input ports only	In this mode the PIO ports can capture input only.
Output ports only	In this mode the PIO ports can drive output only.
Both input and output ports	In this mode, the input and output ports buses are separate, unidirectional buses of *n* bits wide.

Input Options

The **Input Options** tab allows the designer to specify edge-capture and IRQ generation settings. The **Input Options** tab is not available when **Output ports only** is selected on the **Basic Settings** tab.

Edge Capture Register

When the **Synchronously capture** option is turned on, the PIO core contains the edge capture register, `edgecapture`. The user must further specify what type of edge(s) to detect:

- **Rising Edge**
- **Falling Edge**
- **Either Edge**

The edge capture register allows the core to detect and (optionally) generate an interrupt when an edge of the specified type occurs on an input port.

When the **Synchronously capture** option is turned off, the `edgecapture` register does not exist.

Interrupt

When the **Generate IRQ** option is turned on, the PIO core is able to assert an IRQ output when a specified event occurs on input ports. The user must further specify the cause of an IRQ event:

- **Level**—The core generates an IRQ whenever a specific input is high and interrupts are enabled for that input in the `interruptmask` register.
- **Edge**—The core generates an IRQ whenever a specific bit in the edge capture register is high and interrupts are enabled for that bit in the `interruptmask` register.

When the **Generate IRQ** option is turned off, the `interruptmask` register does not exist.

Device & Tools Support

The PIO core supports all Altera® FPGA families.

Software Programming Model

This section describes the software programming model for the PIO core, including the register map and software constructs used to access the hardware. For Nios® II processor users, Altera provides the HAL system library header file that defines the PIO core registers. The PIO core does not match the generic device model categories supported by the HAL, so it cannot be accessed via the HAL API or the ANSI C standard library.

The Nios II Embedded Design Suite (EDS) provides several example designs that demonstrate usage of the PIO core. In particular, the **count_binary.c** example uses the PIO core to drive LEDs, and detect button presses using PIO edge-detect interrupts.

Software Files

The PIO core is accompanied by one software file, **altera_avalon_pio_regs.h**. This file defines the core's register map, providing symbolic constants to access the low-level hardware.

Legacy SDK Routines

The PIO core is supported by the legacy SDK routines for the first-generation Nios processor. For details on these routines, refer to the PIO documentation that accompanied the first-generation Nios processor. For details on upgrading programs based on the legacy SDK to the HAL system library API, refer to *AN 350: Upgrading Nios Processor Systems to the Nios II Processor*.

Register Map

An Avalon master peripheral, such as a CPU, controls and communicates with the PIO core via the four 32-bit registers, shown in Table 11–2. The table assumes that the PIO core's I/O ports are configured to a width of *n* bits.

Table 11–2. Register Map for the PIO Core

Offset	Register Name		R/W	(n-1)	...	2	1	0
0	`data`	read access	R	Data value currently on PIO inputs				
		write access	W	New value to drive on PIO outputs				
1	`direction` *(1)*		R/W	Individual direction control for each I/O port. A value of 0 sets the direction to input; 1 sets the direction to output.				
2	`interruptmask` *(1)*		R/W	IRQ enable/disable for each input port. Setting a bit to 1 enables interrupts for the corresponding port.				
3	`edgecapture` *(1)*, *(2)*		R/W	Edge detection for each input port.				

Notes to Table 11–2:

(1) This register may not exist, depending on the hardware configuration. If a register is not present, reading the register returns an undefined value, and writing the register has no effect.

(2) Writing any value to `edgecapture` clears all bits to 0.

data Register

Reading from `data` returns the value present at the input ports. If the PIO core hardware is configured in output-only mode, reading from `data` returns an undefined value.

Writing to `data` stores the value to a register that drives the output ports. If the PIO core hardware is configured in input-only mode, writing to `data` has no effect. If the PIO core hardware is in bidirectional mode, the registered value appears on an output port only when the corresponding bit in the `direction` register is set to 1 (output).

direction Register

The `direction` register controls the data direction for each PIO port, assuming the port is bidirectional. When bit *n* in `direction` is set to 1, port *n* drives out the value in the corresponding bit of the `data` register.

The `direction` register only exists when the PIO core hardware is configured in bidirectional mode. The mode (input, output, or bidirectional) is specified at system generation time, and cannot be changed at runtime. In input-only or output-only mode, the `direction` register does not exist. In this case, reading `direction` returns an undefined value, writing `direction` has no effect.

After reset, all bits of direction are 0, so that all bidirectional I/O ports are configured as inputs. If those PIO ports are connected to device pins, the pins are held in a high-impedance state.

interruptmask Register

Setting a bit in the `interruptmask` register to 1 enables interrupts for the corresponding PIO input port. Interrupt behavior depends on the hardware configuration of the PIO core. See "Interrupt Behavior" on page 11–9.

The `interruptmask` register only exists when the hardware is configured to generate IRQs. If the core cannot generate IRQs, reading `interruptmask` returns an undefined value, and writing to `interruptmask` has no effect.

After reset, all bits of `interruptmask` are zero, so that interrupts are disabled for all PIO ports.

edgecapture Register

Bit *n* in the `edgecapture` register is set to 1 whenever an edge is detected on input port *n*. An Avalon master peripheral can read the `edgecapture` register to determine if an edge has occurred on any of the PIO input ports. Writing any value to `edgecapture` clears all bits in the register.

The type of edge(s) to detect is fixed in hardware at system generation time. The `edgecapture` register only exists when the hardware is configured to capture edges. If the core is not configured to capture edges, reading from `edgecapture` returns an undefined value, and writing to `edgecapture` has no effect.

Interrupt Behavior

The PIO core outputs a single interrupt-request (IRQ) signal that can connect to any master peripheral in the system. The master can read either the `data` register or the `edgecapture` register to determine which input port caused the interrupt.

When the hardware is configured for level-sensitive interrupts, the IRQ is asserted whenever corresponding bits in the `data` and `interruptmask` registers are 1. When the hardware is configured for edge-sensitive interrupts, the IRQ is asserted whenever corresponding bits in the `edgecapture` and `interruptmask` registers are 1. The IRQ remains asserted until explicitly acknowledged by disabling the appropriate bit(s) in `interruptmask`, or by writing to `edgecapture`.

Software Files

The PIO core is accompanied by the following software file. This file provide low-level access to the hardware. Application developers should not modify the file.

- **altera_avalon_pio_regs.h**—This file defines the core's register map, providing symbolic constants to access the low-level hardware. The symbols in this file are used by device driver functions.

12. Timer Core with Avalon Interface

NII51008-6.0.0

Core Overview

The timer core with Avalon® interface core is a 32-bit interval timer for Avalon-based processor systems, such as a Nios® II processor system. The timer provides the following features:

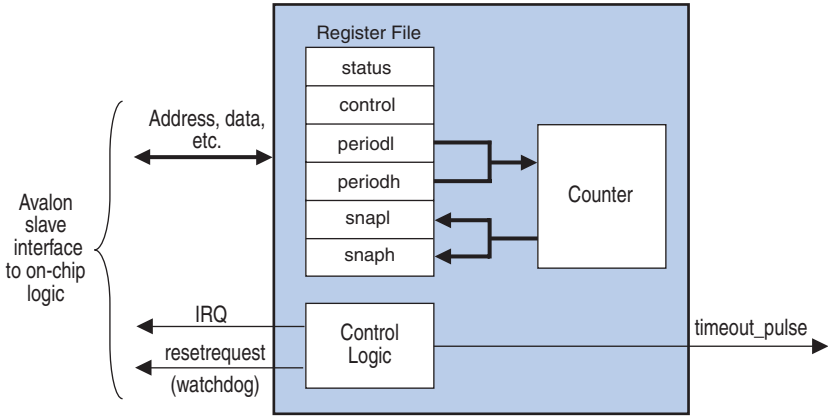
- Controls to start, stop, and reset the timer
- Two count modes: count down once and continuous count-down
- Count-down period register
- Maskable interrupt request (IRQ) upon reaching zero
- Optional watchdog timer feature that resets the system if timer ever reaches zero
- Optional periodic pulse generator feature that outputs a pulse when timer reaches zero
- Compatible with 32-bit and 16-bit processors

Device drivers are provided in the HAL system library for the Nios II processor. The timer core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

Functional Description

Figure 12–1 shows a block diagram of the timer core.

Figure 12–1. Timer Core Block Diagram



The timer core has two user-visible features:

- The Avalon interface that provides access to six 16-bit registers
- An optional pulse output that can be used as a periodic pulse generator

All registers are 16-bits wide, making the timer compatible with both 16-bit and 32-bit processors. Certain registers only exist in hardware for a given configuration. For example, if the timer is configured with a fixed period, the period registers do not exist in hardware.

The basic behavior of the timer is described below:

- An Avalon master peripheral, such as a Nios II processor, writes the timer core's `control` register to:
  - Start and stop the timer
  - Enable/disable the IRQ
  - Specify count-down once or continuous count-down mode
- A processor reads the `status` register for information about current timer activity.
- A processor can specify the timer period by writing a value to the period registers, `periodl` and `periodh`.
- An internal counter counts down to zero, and whenever it reaches zero, it is immediately reloaded from the period registers.
- A processor can read the current counter value by first writing to either `snapl` or `snaph` to request a coherent snapshot of the counter, and then reading `snapl` and `snaph` for the full 32-bit value.
- When the count reaches zero:
  - If IRQs are enabled, an IRQ is generated
  - The (optional) pulse-generator output is asserted for one clock period
  - The (optional) watchdog output resets the system

Avalon Slave Interface

The timer core implements a simple Avalon slave interface to provide access to the register file. The Avalon slave port uses the `resetrequest` signal to implement watchdog timer behavior. This signal is a non-maskable reset signal, and it drives the reset input of all Avalon peripherals in the SOPC Builder system. When the `resetrequest` signal is asserted, it forces any processor connected to the system to reboot. See "Configuring the Timer as a Watchdog Timer" on page 12–4 for further details.

Device & Tools Support

The timer core supports all Altera® FPGA families.

Instantiating the Core in SOPC Builder

Designers use the timer's SOPC Builder configuration wizard to specify the hardware features. This section describes the options available in the configuration wizard.

Timeout Period

The **Timeout Period** setting determines the initial value of the `periodl` and `periodh` registers. When the **Writeable period** setting is enabled, a processor can change the value of the period by writing `periodl` and `periodh`. When the **Writeable period** setting (see below) is turned off, the period is fixed and cannot be updated at runtime.

The **Timeout Period** setting can be specified in units of **usec**, **msec**, **sec**, or **clocks** (number of clock cycles). The actual period achieved depends on the system clock. If the period is specified in usec, msec or sec, the true period will be the smallest number of clock cycles that is greater than or equal to the specified **Timeout Period**.

Hardware Options

The following options affect the hardware structure of the timer core. As a convenience, the **Preset Configurations** list offers several pre-defined hardware configurations, such as:

- **Simple periodic interrupt**—This configuration is useful for systems that require only a periodic IRQ generator. The period is fixed and the timer cannot be stopped, but the IRQ can be disabled.
- **Full-featured**—This configuration is useful for embedded processor systems that require a timer with variable period that can be started and stopped under processor control.
- **Watchdog**—This configuration is useful for systems that require watchdog timer to reset the system in the event that the system has stopped responding. See "Configuring the Timer as a Watchdog Timer" on page 12–4.

Register Options

Table 12–1 shows the settings that affect the timer core's registers.

Table 12–1. Register Options

Option	Description
Writeable period	When this option is enabled, a master peripheral can change the count-down period by writing `periodl` and `periodh`. When disabled, the count-down period is fixed at the specified **Timeout Period**, and the `periodl` and `periodh` registers do not exist in hardware.
Readable snapshot	When this option is enabled, a master peripheral can read a snapshot of the current count-down. When disabled, the status of the counter is detectable only via other indicators, such as the `status` register or the IRQ signal. In this case, the `snapl` and `snaph` registers do not exist in hardware, and reading these registers produces an undefined value.
Start/Stop control bits	When this option is enabled, a master peripheral can start and stop the timer by writing the START and STOP bits in the `control` register. When disabled, the timer runs continuously. When the **System reset on timeout (watchdog)** option is enabled, the START bit is also present, regardless of the **Start/Stop control bits** option.

Output Signal Options

Table 12–2 shows the settings that affect the timer core's output signals.

Table 12–2. Output Signal Options

Option	Description
Timeout pulse (1 clock wide)	When this option is enabled, the timer core outputs a signal `timeout_pulse`. This signal pulses high for one clock cycle whenever the timer reaches zero. When disabled, the `timeout_pulse` signal does not exist.
System reset on timeout (watchdog)	When this option is enabled, the timer core's Avalon slave port includes the `resetrequest` signal. This signal pulses high for one clock cycle (causing a system-wide reset) whenever the timer reaches zero. When this option is enabled, the internal timer is stopped at reset. Explicitly writing the START bit of the `control` register starts the timer. When this option is disabled, the `resetrequest` signal does not exist. See "Configuring the Timer as a Watchdog Timer" on page 12–4.

Configuring the Timer as a Watchdog Timer

To configure the timer for use as a watchdog, in the configuration wizard select **Watchdog** in the **Preset Configurations** list, or choose the following settings:

- Set the **Timeout Period** to the desired "watchdog" period.
- Turn **off** the **Writeable period** option.
- Turn **off** the **Readable snapshot** option.

- Turn **off** the **Start/Stop control bits** option.
- Turn **off** the **Timeout pulse** option.
- Turn **on** the **System reset on timeout (watchdog)** option.

A watchdog timer wakes up (i.e., comes out of reset) stopped. A processor later starts the timer by writing a 1 to the `control` register's START bit. Once started, the timer can never be stopped. If the internal counter ever reaches zero, the watchdog timer resets the system by generating a pulse on its `resetrequest` output. To prevent the system from resetting, the processor must periodically reset the timer's count-down value by writing either the `periodl` or `periodh` registers (the written value is ignored). If the processor fails to access the timer because, for example, software stopped executing normally, then the watchdog timer resets the system and returns the system to a defined state.

Software Programming Model

The following sections describe the software programming model for the timer core, including the register map and software declarations to access the hardware. For Nios II processor users, Altera provides hardware abstraction layer (HAL) system library drivers that enable you to access the timer core using the HAL application programming interface (API) functions.

HAL System Library Support

The Altera-provided drivers integrate into the HAL system library for Nios II systems. When possible, HAL users should access the timer via the HAL API, rather than accessing the timer registers.

Altera provides a driver for both the HAL timer device models: system clock timer, and timestamp timer.

System Clock Driver

When configured as the system clock, the timer runs continuously in periodic mode, using the default period set in SOPC builder. The system clock services are then run as a part of the interrupt service routine for this timer. The driver is interrupt-driven, and therefore must have its interrupt signal connected in the system hardware.

The Nios II integrated development environment (IDE) allows you to specify system library properties that determine which timer device will be used as the system clock timer.

Timestamp Driver

The timer core may be used as a timestamp device if it meets the following conditions:

- The timer has a writeable `snapshot` register, as configured in SOPC Builder.
- The timer is not selected as the system clock.

The Nios II IDE allows you to specify system library properties that determine which timer device will be used as the timestamp timer.

If the timer hardware is not configured with writeable `period` registers, then calls to the `alt_timestamp_start()` API function will not reset the timestamp counter. All other HAL API calls will perform as expected.

See the *Nios II Software Developer's Handbook* for details on using the system clock and timestamp features that use these drivers. The Nios II Embedded Design Suite (EDS) also provides several example designs that use the timer core.

Limitations

The HAL driver for the timer core does not support the watchdog reset feature of the timer core.

Software Files

The timer core is accompanied by the following software files. These files define the low-level interface to the hardware, and provide the HAL drivers. Application developers should not modify these files.

- **altera_avalon_timer_regs.h—**This file defines the core's register map, providing symbolic constants to access the low-level hardware.
- **altera_avalon_timer.h**, **altera_avalon_timer_sc.c, altera_avalon_timer_ts.c, altera_avalon_timer_vars.c—**These files implement the timer device drivers for the HAL system library.

Register Map

A programmer should never have to directly access the timer via its registers if using the standard features provided in the HAL system library for the Nios II processor. In general, the register map is only useful to programmers writing a device driver.

CAUTION

The Altera-provided HAL device driver accesses the device registers directly. If you are writing a device driver, and the HAL driver is active for the same device, your driver will conflict and fail to operate correctly.

Table 12–3 shows the register map for the timer.

Table 12–3. Register Map

Offset	Name	R/W	Description of Bits						
			15	…	4	3	2	1	0
0	status	RW	*(1)*					RUN	TO
1	control	RW	*(1)*			STOP	START	CONT	ITO
2	periodl	RW	Timeout Period – 1 (bits 15..0)						
3	periodh	RW	Timeout Period – 1 (bits 31..16)						
4	snapl	RW	Counter Snapshot (bits 15..0)						
5	snaph	RW	Counter Snapshot (31..16)						

Note to Table 12–3:
(1) Reserved. Read values are undefined. Write zero.

status Register

The `status` register has two defined bits, as shown in Table 12–4.

Table 12–4. status Register Bits

Bit	Name	Read/ Write/ Clear	Description
0	TO	RC	The TO (timeout) bit is set to 1 when the internal counter reaches zero. Once set by a timeout event, the TO bit stays set until explicitly cleared by a master peripheral. Write zero to the `status` register to clear the TO bit.
1	RUN	R	The RUN bit reads as 1 when the internal counter is running; otherwise this bit reads as 0. The RUN bit is not changed by a write operation to the `status` register.

control Register

The `control` register has four defined bits, as shown in Table 12–5.

Table 12–5. control Register Bits

Bit	Name	Read/ Write/ Clear	Description
0	ITO	RW	If the ITO bit is 1, the timer core generates an IRQ when the `status` register's TO bit is 1. When the ITO bit is 0, the timer does not generate IRQs.
1	CONT	RW	The CONT (continuous) bit determines how the internal counter behaves when it reaches zero. If the CONT bit is 1, the counter runs continuously until it is stopped by the STOP bit. If CONT is 0, the counter stops after it reaches zero. When the counter reaches zero, it reloads with the 32-bit value stored in the `periodl` and `periodh` registers, regardless of the CONT bit.
2	START (1)	W	Writing a 1 to the START bit starts the internal counter running (counting down). The START bit is an event bit that enables the counter when a write operation is performed. If the timer is stopped, writing a 1 to the START bit causes the timer to restart counting from the number currently held in its counter. If the timer is already running, writing a 1 to START has no effect. Writing 0 to the START bit has no effect.
3	STOP *(1)*	W	Writing a 1 to the STOP bit stops the internal counter. The STOP bit is an event bit that causes the counter to stop when a write operation is performed. If the timer is already stopped, writing a 1 to STOP has no effect. Writing a 0 to the stop bit has no effect. Writing 0 to the STOP bit has no effect. If the timer hardware is configured with the **Start/Stop control bits** option turned off, writing the STOP bit has no effect.

Note:
(1) Writing 1 to both START and STOP bits simultaneously produces an undefined result.

periodl & periodh Registers

The `periodl` and `periodh` registers together store the timeout period value. `periodl` holds the least-significant 16 bits, and `periodh` holds the most-significant 16 bits. The internal counter is loaded with the 32-bit value stored in `periodh` and `periodl` whenever one of the following occurs:

- A write operation to either the `periodh` or `periodl` register
- The internal counter reaches 0

The timer's actual period is one cycle greater than the value stored in `periodh` and `periodl`, because the counter assumes the value zero (0x00000000) for one clock cycle.

Writing to either periodh or periodl stops the internal counter, except when the hardware is configured with the **Start/Stop control bits** option turned off. If the **Start/Stop control bits** option is turned off, writing either register does not stop the counter. When the hardware is configured with the **Writeable period** option disabled, writing to either periodh or periodl causes the counter to reset to the fixed **Timeout Period** specified at system generation time.

snapl & snaph Registers

A master peripheral may request a coherent snapshot of the current 32-bit internal counter by performing a write operation (write-data ignored) to either the snapl or snaph registers. When a write occurs, the value of the counter is copied to snapl and snaph. snapl holds the least-significant 16 bits of the snapshot and snaph holds the most-significant 16 bits. The snapshot occurs whether or not the counter is running. Requesting a snapshot does not change the internal counter's operation.

Interrupt Behavior

The timer core generates an IRQ whenever the internal counter reaches zero and the ITO bit of the control register is set to 1. Acknowledge the IRQ in one of two ways:

- Clear the TO bit of the status register
- Disable interrupts by clearing the ITO bit of the control register

13. System ID Core with Avalon Interface

NII51014-6.0.0

Core Overview

The system ID core is a simple read-only device that provides SOPC Builder systems with a unique identifier. Nios® II processor systems use the system ID core to verify that an executable program was compiled targeting the actual hardware image configured in the target FPGA. If the expected ID in the executable does not match the system ID core in the FPGA, it is possible that the software will not execute correctly.

Functional Description

The system ID core provides a read-only Avalon® slave interface. There are two registers, as shown in Table 13–1.

Table 13–1. System ID Core Register Map

Offset	Register Name	R/W	Bit Description
			31...0
0	id	R	SOPC Builder System ID *(1)*
1	timestamp	R	SOPC Builder Generation Time *(1)*

Note to Table 13–1:
(1) Return value is constant.

The value of each register is determined at system generation time, and always returns a constant value. The meaning of the values is:

- id— A unique 32-bit value that is based on the contents of the SOPC Builder system. The id is similar to a check-sum value; SOPC Builder systems with different components and/or different configuration options produce different id values.
- timestamp—A unique 32-bit value that is based on the system generation time. The value is equivalent to the number of seconds after Jan. 1, 1970.

There are two basic ways to use the system ID core:

- Verify the system ID before downloading new software to a system. This method is used by software development tools, such as the Nios II integrated development environment (IDE). There is little point in downloading a program to a target hardware system, if the

program is compiled for different hardware. Therefore, the Nios II IDE checks that the system ID core in hardware matches the expected system ID of the software before downloading a program to run or debug.

- Check system ID after reset. If a program is running on hardware other than the expected SOPC Builder system, then the program may fail to function altogether. If the program does not crash, it can behave erroneously in subtle ways that are difficult to debug. To protect against this case, a program can compare the expected system ID against the system ID core, and report an error if they do not match.

Device & Tools Support

The system ID core supports all device families supported by SOPC Builder. The system ID core provides a device driver for the Nios II hardware abstraction layer (HAL) system library. No software support is provided for any other processor, including the first-generation Nios processor.

Instantiating the Core in SOPC Builder

The System ID core has no user-settable features. The `id` and `timestamp` register values are determined at system generation time based on the configuration of the SOPC Builder system and the current time. You can add only one system ID core to an SOPC Builder system, and its name is always `sysid`.

After system generation, you can examine the values stored in the `id` and `timestamp` registers by opening the System ID configuration wizard. Hovering over the component in SOPC Builder also displays a tool-tip showing the values.

Software Programming Model

This section describes the software programming model for the system ID core. For Nios II processor users, Altera provides the HAL system library header file that defines the system ID core registers. Altera provides one access routine, `alt_avalon_sysid_test()`, that returns a value indicating whether the system ID expected by software matches the system ID core.

alt_avalon_sysid_test()

Prototype:	`alt_32 alt_avalon_sysid_test(void)`
Thread-safe:	No.
Available from ISR:	Yes.
Include:	**<altera_avalon_sysid.h>**
Description:	Returns 0 if the values stored in the hardware registers match the values expected by software. Returns 1 if the hardware timestamp is greater than the software timestamp. Returns -1 if the software timestamp is greater than the hardware timestamp.

Software Files

The System ID core comes with the following software files. These files provide low-level access to the hardware. Application developers should not modify these files.

- **alt_avalon_sysid_regs.h**—Defines the interface to the hardware registers.
- **alt_avalon_sysid.c, alt_avalon_sysid.h**—Header and source files defining the hardware access functions.

14. PLL Core with Avalon Interface

NII53002-6.0.0

Core Overview

The Avalon® phase locked loop (PLL) core provides a means of accessing the dedicated on-chip PLL circuitry in Altera's Stratix® and Cyclone™ series FPGAs. The PLL core is a component wrapper around the Altera® altpll Megafunction. The PLL core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

The core takes an SOPC Builder system clock as its input and generates PLL output clocks locked to that reference clock.

The PLL core supports the following features:

- All PLL features provided by Altera's altpll Megafunction. The exact feature set depends on the device family.
- Access to status and control signals via Avalon registers or top-level signals on the SOPC Builder system module.

The PLL output clocks are made available in two ways:

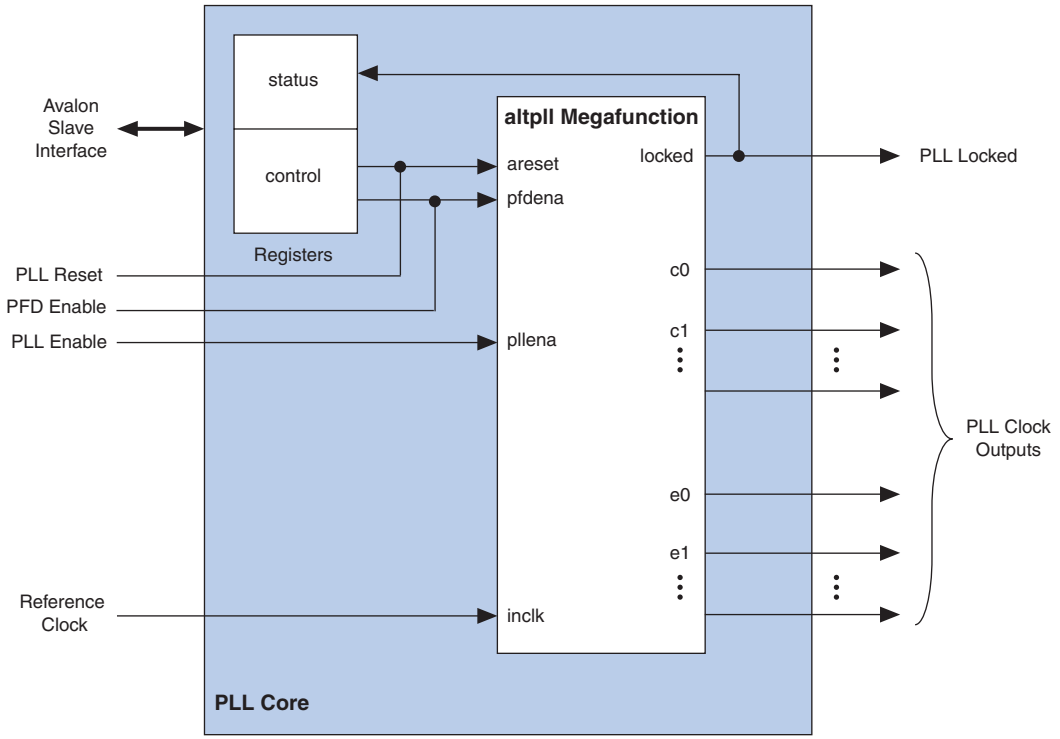
- As sources to system-wide clocks in your SOPC Builder system.
- As output signals on your SOPC Builder system module.

For details on the altpll Megafunction, see the *altpll Megafunction User Guide*.

Functional Description

Figure 14–1 shows a block diagram of the PLL core and its connection to the PLL circuitry inside an Altera FPGA. The following sections describe the components of the core.

Figure 14–1. PLL Core Block Diagram



altpll Megafunction

The PLL core consists of an altpll Megafunction instantiation and an Avalon slave interface. This interface can optionally provide access to status and control registers within the core. The altpll Megafunction takes an SOPC Builder system clock as its reference, and generates one or more phase-locked output clocks.

Clock Outputs

Depending on the target device family, the altpll Megafunction can produce two types of output clock:

- internal (c) – clock outputs that can drive logic either inside or outside the SOPC Builder system module. Internal clock outputs can also be mapped to top-level FPGA pins. Internal clock outputs are available on all device families.
- external (e) – clock outputs that can only drive dedicated FPGA pins. They can not be used as on-chip clock sources. External clock outputs are not available on all device families.

To determine the exact number and type of output clocks available on your target device, see the *altpll Megafunction User Guide*.

PLL Status and Control Signals

Depending on how altpll is parameterized, there can be a variable number of status and control signals. You can choose to export certain status and control signals to the top-level SOPC Builder system module. Alternatively, Avalon registers can provide access to the signals. Any status or control signals which are not mapped to registers are exported to the top-level module.

For details, see "Instantiating the Core in SOPC Builder".

System Reset Considerations

At FPGA configuration, the PLL core resets automatically. PLL-specific reset circuitry guarantees that the PLL locks before releasing reset for the overall SOPC Builder system module.

Resetting the PLL resets the entire SOPC Builder system module.

Device & Tools Support

The PLL core is supported by the Quartus II software version 5.1 and later. The core supports any Altera FPGA family supported by the altpll Megafunction.

For details see the *altpll Megafunction User Guide*.

Instantiating the Core in SOPC Builder

This section describes the options available in the SOPC Builder Avalon PLL configuration wizard.

The PLL core contains an instantiation of the altpll Megafunction. The configuration wizard for the PLL core allows you to configure the altpll, and specify connections to selected altpll status and control signals. The PLL core appears in the **Other** category in the SOPC Builder list of available components.

The following sections describe the settings available in the configuration wizard.

PLL Settings Tab

The **PLL Settings** tab contains a button that launches Altera's altpll Megawizard. Use the Megawizard to parameterize the altpll. The set of available parameters depends on the target device family.

For details on using the altpll Megawizard see the *altpll Megafunction User Guide*.

You cannot click **Finish** in the Avalon PLL wizard, nor configure the PLL interface, until you parameterize the altpll.

Interface Tab

The **Interface** tab configures the access modes for the optional advanced PLL status and control signals.

For each advanced signal present on the altpll, you can select one of the following access modes:

- **Export** - Exports the signal to the top level of the SOPC builder system module.
- **Register** - Maps the signal to a bit in a status or control register.

The advanced signals are optional. If you choose not to create any of them in the altpll Megawizard, the PLL's default behavior will be as shown in Table 14–1.

You can specify the access mode for the advanced signals shown in Table 14–1. altpll core signals which are not displayed in this table are automatically exported to the top level of the SOPC Builder system module.

Table 14–1. altpll Advanced Signals

altpll Name	Input / Output	Avalon PLL Wizard Name	Default Behavior	Description
areset	input	PLL Reset Input	The PLL is reset only at device configuration.	This signal resets the entire SOPC Builder system module, and restores the PLL to its initial settings.
pllena	input	PLL Enable Input	The PLL is enabled.	This signal enables the PLL. pllena is always exported.
pfdena	input	PFD Enable Input	The phase-frequency detector is enabled.	This signal enables the phase-frequency detector in the PLL, allowing it to lock on to changes in the clock reference.
locked	output	PLL Locked Output	-	This signal is asserted when the PLL is locked to the input clock.

Asserting areset resets the entire SOPC Builder system module, not just the PLL.

Finish

Click **Finish** to insert the PLL into the SOPC Builder system. The PLL clock output(s) appear in the clock settings table on the SOPC Builder **System Contents** tab.

If the PLL has external output clocks, they appear in the clock settings table like other clocks; however, you cannot use them to drive components within the SOPC Builder system.

For details on using external output clocks, see the *altpll Megafunction User Guide*.

SOPC Builder automatically connects the PLL's reference clock input to the first available clock in the clock settings table.

If there is more than one SOPC Builder system clock available, verify that the PLL is connected to the appropriate reference clock.

Hardware Simulation Considerations

The HDL files generated by SOPC Builder for the PLL core are suitable for both synthesis and simulation. The PLL core supports the standard SOPC Builder simulation flow, so there are no special considerations for hardware simulation.

Register Definitions & Bit List

Table 14–2 shows the register map for the PLL core. Device drivers can control and communicate with the core through two 16-bit memory-mapped registers, `status` and `control`.

Note that the status and control bits shown below are present only if they have been created in the altpll Megawizard, and set to **Register** on the **Interface** tab in the PLL wizard.

Table 14–2. PLL Core Register Map

Offset	Register Name	R/W	Bit Description				
			15	…	2	1	0
0	`status`	R/O	*(1)*				LOCKED
1	`control`	R/W	*(1)*			PFDENA	ARESET

Note to Table 14–2:
(1) Reserved. Read values are undefined. When writing, set reserved bits to zero.

Status Register

Embedded software can access the PLL status via the `status` register. Writing to `status` has no effect. Table 14–3 describes the function of each bit.

Table 14–3. Status Register Bits

Bit Number	Bit Name	Value after reset	Description
0	LOCKED	1	Connects to the `locked` signal on the altpll. The LOCKED bit is high when valid clocks are present on the output of the PLL
1 .. 15		-	Reserved. Read values are undefined.

Control Register

Embedded software can control the PLL via the `control` register. Software can also read back the status of control bits. Table 14–4 describes the function of each bit.

Table 14–4. Control Register Bits

Bit Number	Bit Name	Value after reset	Description
0	ARESET	0	Connects to the `areset` signal on the altpll. Writing a 1 to this bit asserts the `areset` signal for one clock cycle.
1	PFDENA	1	Connects to the `pfdena` signal on the altpll.
2 .. 15		-	Reserved. Read values are undefined. When writing, set reserved bits to zero.

15. Performance Counter Core with Avalon Interface

QIII55001-6.0.0

Core Overview

The performance counter core enables relatively unobtrusive, real-time profiling of software programs. With the performance counter, you can accurately measure execution time taken by multiple sections of code. You need only add a single instruction at the beginning and end of each section to be measured.

The main benefit of using the performance counter core is the accuracy of the profiling results. Alternatives include the following approaches:

- GNU profiler, `gprof`—`gprof` provides broad low-precision timing information about the entire software system. It uses a substantial amount of RAM, and degrades the real-time performance. For many embedded applications, `gprof` distorts real-time behavior too much to be useful.
- Interval timer peripheral—The interval timer is less intrusive than `gprof`. It can provide good results for narrowly targeted sections of code. However, the granularity of the results is milliseconds, which is too coarse for many embedded applications.

The performance counter core is unobtrusive, requiring only a single instruction to start and stop profiling, and no RAM. It is appropriate for high-precision measurements of narrowly targeted sections of code.

See *AN 391: Profiling Nios® II Systems*, for further discussion of all three profiling methods.

The performance counter core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system. The core is designed for use in Avalon®-based processor systems, such as a Nios II processor system. Altera® provides device drivers to enable the Nios II processor to use the performance counters.

Functional Description

The performance counter core is a set of counters which track clock cycles, timing multiple sections of your software. You can start and stop these counters in your software, individually or as a group. You can read cycle counts from hardware registers.

The core contains two counters for every section:

- Time: A 64-bit clock cycle counter.
- Events: A 32-bit event counter.

Section Counters

Each 64-bit time counter records the aggregate number of clock cycles spent in a section of code. The 32-bit event counter records the number of times the section executes.

The performance counter core can have up to seven section counters.

Global Counter

The global counter controls all section counters. The section counters are enabled only when the global counter is running.

The 64-bit global clock cycle counter tracks the aggregate time for which the counters were enabled. The 32-bit global event counter tracks the number of global events, that is, the number of times the performance counter core has been enabled.

Register Map

The performance counter core has a simple Avalon slave interface that provides access to memory-mapped registers. Reading from the registers retrieves the current times and event counts. Writing to the registers starts, stops and resets the counters. Table 15–1 shows the registers in detail.

Table 15–1. Performance Counter Core Register Map

Offset	Register Name	Bit Description		
		Read	Write	
		31 … 0	31 …	0
0	T[0]$_{lo}$	global clock cycle counter [31: 0]	*(1)*	0 = STOP 1 = RESET
1	T[0]$_{hi}$	global clock cycle counter [63:32]	*(1)*	0 = START
2	Ev[0]	global event counter	*(1)*	*(1)*
3	–	*(1)*	*(1)*	*(1)*
4	T[1]$_{lo}$	section 1 clock cycle counter [31: 0]	*(1)*	0 = STOP
5	T[1]$_{hi}$	section 1 clock cycle counter [63:32]	*(1)*	0 = START
6	Ev[1]	section 1 event counter	*(1)*	*(1)*
7	–	*(1)*	*(1)*	*(1)*
8	T[2]$_{lo}$	section 2 clock cycle counter [31: 0]	*(1)*	0 = STOP
9	T[2]$_{hi}$	section 2 clock cycle counter [63:32]	*(1)*	0 = START
10	Ev[2]	section 2 event counter	*(1)*	*(1)*
11	–	*(1)*	*(1)*	*(1)*
. . .	. . .	. . .	. . .	. . .
4*n* + 0	T[n]$_{lo}$	section *n* clock cycle counter [31: 0]	*(1)*	0 = STOP
4*n* + 1	T[n]$_{hi}$	section *n* clock cycle counter [63:32]	*(1)*	0 = START
4*n* + 2	Ev[n]	section *n* event counter	*(1)*	*(1)*
4*n* + 3	–	*(1)*	*(1)*	*(1)*

Note to Table 15–1:
(1) Reserved. Read values are undefined. When writing, set reserved bits to zero.

System Reset Considerations

After system reset, the performance counter core is stopped and disabled, and all counters contain zero.

Device & Tools Support

The performance counter core supports all Altera device families supported by SOPC Builder, and provides device drivers for the Nios II hardware abstraction layer (HAL) system library.

Instantiating the Core in SOPC Builder

To specify the core's hardware features, use the performance counter core's SOPC Builder configuration wizard.

Define Counters

Choose the number of section counters you want to generate by selecting from the "**Number of simultaneously-measured sections"** list. The performance counter core may have up to seven sections. If you require more that seven sections, you can instantiate multiple performance counter cores.

Multiple Clock Domain Considerations

If your SOPC Builder system uses multiple clocks, place the performance counter core in the same clock domain as the CPU. Otherwise, it is not possible to convert cycle counts to seconds correctly.

Hardware Simulation Considerations

You can use this core in simulation with no special considerations.

Software Programming Model

The following sections describe the software programming model for the performance counter core.

Software Files

Altera provides the following software files for Nios II systems. These files define the low-level access to the hardware and provide control and reporting functions. Do not modify these files.

- **altera_avalon_performance_counter.h, altera_avalon_performance_counter.c** —The header and source code for the functions and macros needed to control the performance counter core and retrieve raw results.
- **perf_print_formatted_report.c**—The source code for simple profile reporting.

Using the Performance Counter

In a Nios II system, you can control the performance counter core with a set of highly efficient C macros, and extract the results with C functions.

API Summary

The Nios II application program interface (API) for the performance counter core consists of functions, macros and constants.

Functions and macros

Table 15–2 lists macros and functions for accessing the performance counter hardware structure.

Table 15–2. Performance Counter Macros and Functions

Name	Summary
`PERF_RESET()`	Stops and disables all counters, resetting them to 0.
`PERF_START_MEASURING()`	Starts the global counter and enables section counters.
`PERF_STOP_MEASURING()`	Stops the global counter and disables section counters.
`PERF_BEGIN()`	Starts timing a code section.
`PERF_END()`	Stops timing a code section.
`perf_print_formatted_report()`	Sends a formatted summary of the profiling results to stdout.
`perf_get_total_time()`	Returns the aggregate global profiling time in clock cycles.
`perf_get_section_time()`	Returns the aggregate time for one section in clock cycles.
`perf_get_num_starts()`	Returns the number of counter events.
`alt_get_cpu_freq()`	Returns the CPU frequency in Hz.

For a complete description of each macro and function, see "Performance Counter API" on page 15–7.

Hardware constants

You can get the performance counter hardware parameters from constants defined in **system.h**. The constant names are based on the performance counter instance name, specified on the **System Contents** tab in SOPC Builder. Table 15–3 lists the hardware constants.

Table 15–3. Performance counter constants	
Name *(1)*	**Meaning**
PERFORMANCE_COUNTER_BASE	Base address of core
PERFORMANCE_COUNTER_SPAN	Number of hardware registers
PERFORMANCE_COUNTER_HOW_MANY_SECTIONS	Number of section counters

Note to Table 15–3:
(1) Example based on instance name "performance_counter"

Startup

Before using the performance counter core, invoke `PERF_RESET` to stop, disable and zero all counters.

Global Counter Usage

Use the global counter to enable and disable the entire performance counter core. For example, you might choose to leave profiling disabled until your software has completed its initialization.

Section Counter Usage

To measure a section in your code, surround it with the macros `PERF_BEGIN()` and `PERF_END()`. These macros consist of a single write to the performance counter core.

You can simultaneously measure as many code sections as you like, up to the number specified in SOPC Builder. See "Define Counters" on page 15–4 for details. You can start and stop counters individually, or as a group.

Typically, you assign one counter to each section of code you intend to profile. However, in some situation you may wish to group several sections of code in a single section counter. As an example, to measure general interrupt overhead, you can measure all interrupt service routines (ISRs) with one counter.

To avoid confusion, assign a mnemonic symbol for each section number.

For an example, see the performance checksum design files accompanying *AN 391: Profiling Nios II Systems*. These files may be found on the Altera Nios II literature page at www.altera.com/literature/lit-nio2.jsp.

Viewing Counter Values

Library routines allow you to retrieve and analyze the results. Use `perf_print_formatted_report()` to list the results to stdout. For example:

```
perf_print_formatted_report(
    (void *)PERFORMANCE_COUNTER_BASE,  // Peripheral's HW base address
    alt_get_cpu_freq(),                // defined in "system.h"
    3,                                 // How many sections to print
    "1st checksum_test",               // Display-names of sections
    "pc_overhead",
    "ts_overhead");
```

The preceding example creates a table similar to this:

```
--Performance Counter Report--
Total Time: 2.07711 seconds (103855534 clock-cycles)
+-----------------+--------+-----------+---------------+-----------+
| Section         |      % | Time (sec)| Time (clocks) |Occurrences|
+-----------------+--------+-----------+---------------+-----------+
|1st checksum_test|     50 |   1.03800 |      51899750 |         1 |
+-----------------+--------+-----------+---------------+-----------+
| pc_overhead     |1.73e-05|   0.00000 |            18 |         1 |
+-----------------+--------+-----------+---------------+-----------+
| ts_overhead     |4.24e-05|   0.00000 |            44 |         1 |
+-----------------+--------+-----------+---------------+-----------+
```

For full documentation of `perf_print_formatted_report()`, see "Performance Counter API" on page 15–7.

Interrupt Behavior

The performance counter core does not generate interrupts.

You can start and stop performance counters, and read raw performance results, in an interrupt service routine (ISR). Do not call function `perf_print_formatted_report()` from an ISR.

If a interrupt occurs during the measurement of a section of code, the time taken by the CPU to process the interrupt and return to the section is added to the measurement time. The same applies to context switches in a multithreaded environment. Your software must take appropriate measures to avoid or handle these situations.

Performance Counter API

This section describes the application programming interface (API) for the performance counter core.

For Nios II processor users, Altera provides routines to access the performance counter core hardware. These functions are specific to the performance counter core and directly manipulate low level hardware. The performance counter core cannot be accessed via the HAL API or the ANSI C standard library.

PERF_RESET()

Prototype:	`PERF_RESET(p)`
Thread-safe:	Yes
Available from ISR:	Yes
Include:	**<altera_avalon_performance_counter.h>**
Parameters:	`p`—performance counter core base address
Returns:	—
Description:	Macro `PERF_RESET()` stops and disables all counters, resetting them to 0.

PERF_START_MEASURING()

Prototype:	`PERF_START_MEASURING(p)`
Thread-safe:	Yes
Available from ISR:	Yes
Include:	**<altera_avalon_performance_counter.h>**
Parameters:	`p`—performance counter core base address
Returns:	—
Description:	Macro `PERF_START_MEASURING()` starts the global counter, enabling the performance counter core. The behavior of individual section counters is controlled by `PERF_BEGIN()` and `PERF_END()`. `PERF_START_MEASURING()` defines the start of a global event, and increments the global event counter. This macro is a single write to the performance counter core.

PERF_STOP_MEASURING()

Prototype:	`PERF_STOP_MEASURING(p)`
Thread-safe:	Yes
Available from ISR:	Yes
Include:	**<altera_avalon_performance_counter.h>**
Parameters:	`p`—performance counter core base address
Returns:	—
Description:	Macro `PERF_STOP_MEASURING()` stops the global counter, disabling the performance counter core. This macro is a single write to the performance counter core.

PERF_BEGIN()

Prototype:	`PERF_BEGIN(p,n)`
Thread-safe:	Yes
Available from ISR:	Yes
Include:	**<altera_avalon_performance_counter.h>**
Parameters:	`p`—performance counter core base address `n`—counter section number. Section counter numbers start at 1. Do not refer to counter 0 in this macro.
Returns:	—
Description:	Macro `PERF_BEGIN()` starts the timer for a code section, defining the beginning of a section event, and incrementing the section event counter. If you subsequently use PERF_STOP_MEASURING() and PERF_START_MEASURING() to disable and re-enable the core, the section counter will resume. This macro is a single write to the performance counter core.

PERF_END()

Prototype:	`PERF_END(p,n)`
Thread-safe:	Yes
Available from ISR:	Yes
Include:	**<altera_avalon_performance_counter.h>**
Parameters:	`p`—performance counter core base address `n`—counter section number. Section counter numbers start at 1. Do not refer to counter 0 in this macro.
Returns:	—
Description:	Macro `PERF_END()` stops timing a code section. The section counter does not run, regardless whether the core is enabled or not. This macro is a single write to the performance counter core.

perf_print_formatted_report()

Prototype:

```
int perf_print_formatted_report (
    void* perf_base,
    alt_u32 clock_freq_hertz,
    int num_sections, ...)
```

Thread-safe: No

Available from ISR: No

Include: **<altera_avalon_performance_counter.h>**

Parameters:

`perf_base`—performance counter core base address
`clock_freq_hertz`—clock frequency
`num_sections`—The number of section counters to display. This must not exceed *<instance_name>*_HOW_MANY_SECTIONS.

Returns: 0

Description:

Function `perf_print_formatted_report()` reads the profiling results from the performance counter core, and prints a formatted summary table This function disables all counters. However, for predictable results in a multithreaded or interrupt environment, invoke `PERF_STOP_MEASURING()` when you reach the end of the code to be measured, rather than relying on `perf_print_formatted_report()`.

perf_get_total_time()

Prototype:	`alt_u64 perf_get_total_time(void* hw_base_address)`
Thread-safe:	No
Available from ISR:	Yes
Include:	**<altera_avalon_performance_counter.h>**
Parameters:	`hw_base_address`—base address of performance counter core
Returns:	Aggregate global time in clock cycles
Description:	Function `perf_get_total_time()` reads the raw global time. This is the aggregate time, in clock cycles, that the performance counter core has been enabled. This function has the side effect of stopping the counters.

perf_get_section_time()

Prototype:	`alt_u64 perf_get_section_time (void* hw_base_address, int which_section)`
Thread-safe:	No
Available from ISR:	Yes
Include:	**<altera_avalon_performance_counter.h>**
Parameters:	`hw_base_address`—performance counter core base address which_section—counter section number
Returns:	Aggregate section time in clock cycles
Description:	Function `perf_get_section_time()` reads the raw time for a given section. This is the time, in clock cycles, that the section has been running. This function has the side effect of stopping the counters.

perf_get_num_starts()

Prototype:
```
alt_u32 perf_get_num_starts
    (void* hw_base_address, int which_section)
```

Thread-safe: Yes

Available from ISR: Yes

Include: **<altera_avalon_performance_counter.h>**

Parameters:
`hw_base_address`—performance counter core base address
`which_section`—counter section number

Returns: Number of counter events

Description: Function `perf_get_num_starts()` retrieves the number of counter events (or times a counter has been started). If which_section = 0, it retrieves the number of global events (times the performance counter core has been enabled). This function does not stop the counters.

alt_get_cpu_freq()

Prototype:	`alt_u32 alt_get_cpu_freq()`
Thread-safe:	Yes.
Available from ISR:	Yes.
Include:	**<altera_avalon_performance_counter.h>**
Parameters:	
Returns:	CPU frequency in Hz
Description:	Function `alt_get_cpu_freq()` returns the CPU frequency in Hz.