A Universal Device Model for Nanoelectronic Circuit Simulation

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***Abstract*—As nanoelectronics approaches the maturity needed for circuit level integration we will need modeling approaches that can capture non-classical behaviors in a compact manner. We propose a universal device model (UDM) that addresses the challenge of correctly balancing accuracy, complexity, and flexibility. The UDM qualitatively represents fundamental classical and quantum phenomena such that nanoelectronic circuit design and simulation become possible. We discuss the motivation behind this modeling approach as well as the underlying details of the model. Furthermore, we present circuit examples of the model in action.**

I. Introduction

The push to scale electronics to nanometer dimensions is bringing new device phenomena to the forefront. Experiment and theory show nanoscale devices may exhibit non-classical characteristics due to electron energy discreteness, electron tunneling, and Coulomb blockade effects. Although some of these phenomena may be considered parasitic in conventional devices, it is possible that nanoelectronic circuits and systems may achieve greater performance through the utilization of such non-classical behavior. Modeling the behavior of nanoscale devices in a manner that allows complex circuits to be simulated in a reasonable amount of time will require new approaches to device modeling. Furthermore, with the field of nanoelectronics being in such an infant stage, there have been many new devices proposals. The ability to quickly and easily create robust device models will aid device designers and circuit designers in evaluating the applicability of new devices. Based on the fundamental classical and quantum phenomena in such devices, we propose a generic universal device model (UDM) that captures the device behavior such that circuit simulation and design become possible at the nanoscale level.

Our concept for the UDM involves using empirical equations to describe each fundamental quantum and classical effect that may be relevant to an electronic device. Since the aim of this model is to promote the design and simulation of circuits containing nanoscale devices, the fundamental effects are represented in terms of their current vs. voltage (I-V) characteristics. The fundamental properties currently included in the model are resistance, thermionic emission (diode-like behavior), resonant tunneling, and Coulomb blockade effects. The superposition of these fundamental properties in the correct proportions yields the overall device behavior. Each empirical equation in the UDM uses a set of parameters that can vary the contribution of the fundamental effect, thus allowing the model to mimic almost any device.

The remainder of this paper is divided into five sections that show the development and structural details of the model. Section II describes the motivation for a universal device model, while section III describes the underlying equations and how they are combined to form models for nanoelectronic devices. The design methodologies used for the development of a model employing the UDM are discussed in section IV. The paper concludes with a section that contains some circuit examples in order to demonstrate the UDM in action.

II. Model Motivation and Background

The field of nanoelectronics has primarily focused on device science and engineering. But, recent work suggests that the field is ready to undertake the challenge of integrating numerous devices into functional circuits. Solid-state nanoscale integrated circuits have been demonstrated by many and are in the process of maturing [1], while molecular nanoelectronics are at the verge of integration [2], [3], [4].

The ability to cope with the complexity of many nanoscale devices will require a similar circuit level abstraction as used in conventional VLSI design. Many efforts are underway for developing solid-state nanoscale compact models [5], [6]. On the other hand, the majority of the higher-level work in molecular nanoelectronics has for the most part skipped the circuit level and focused on architectures [7], [8], [?], [9]. Thus, modeling molecular devices at the level of abstraction needed for circuit design requires a jumpstart to fill the gap between the device level work and the architectural proposals.

The conventional method for modeling devices for use in circuit simulation, such as MOSFETs, incrementally builds on a well established model framework. However, newly designed nanoscale devices do not have this legacy and need to be modeled from ground up. Furthermore, many of these devices exhibit non-classical characteristics due to electron energy discreteness, electron tunneling, and Coulomb blockade. These behaviors are not accounted for in conventional compact device models. With the fundamental physics governing these devices less understood, it may be difficult to develop compact physics-

based models for all the devices that require evaluation at the circuit level.

Two important choices for SPICE-level simulation include the underlying modeling approach and the method of implementing the model. We classify underlying modeling approaches into physics-based models, component-based models, and empirical models. In terms of implementation, models can either be interpreted, i.e. subcircuits, or compiled, i.e. added to the simulator source code. While interpreted models provide a "quick and dirty" implementation option, a compiled model allows for faster simulation and can take advantage of advanced convergence algorithms [5]. Previous work on non-classical device models for SPICE simulation includes models for Resonant-Tunneling Diodes (RTDs) [5], [10] and Single-Electron Transistors (SETs) [6]. The two RTD models mentioned above exhibit the two ends of the spectrum for modeling and implementation approaches. Bhattacharya and Mazumder [5] have developed a physics-based RTD using the compact RTD equations presented in [11]. This compiled model was added to the open source Berkeley SPICE simulator. The advantages of the model in [5] include fast and robust simulation, since it is compiled with the simulator and contains underlying equations based on physical parameters. However, the down sides include a difficult implementation and reduced model flexibility. On the other hand, Yan and Deer [10] present an empirical interpreted model added to PSPICE. While this model provides an easy implementation, which increases flexibility, it incurs increased simulation time because it must be interpreted. Furthermore, the empirical nature of the model losses any connection to the underlying physical structure of the device.

While the previous modeling solutions for nanoelectronics have demonstrated the many options in device modeling, the variety of emerging nanoscale devices without compact physical models calls for a robust modeling methodology capable of developing models in an automated fashion. Our solution is a universal device model (UDM) that qualitatively represents the fundamental phenomena and captures device behavior. The UDM balances the accuracy, complexity, and flexibility so that circuit simulation and design become possible at the fast changing pace of nanoelectronics. The UDM uses empirical equations to intuitively describe each fundamental quantum effect and classical effect. The combination of these basis functions yields the overall device behavior. Fig. 1 shows a schematic of the UDM. Conceptually, the UDM can be considered a hybrid component-based and empirical modeling approach. Our present embodiment of the UDM is composed of parallel capacitance, resistance, thermionic emission, negative differential resistance, and Coulomb blockade components. In this paper we consider only DC solutions for two-terminal devices. We include the capacitance in Fig. 1 to model dynamic device behavior. Extending the UDM concept to other solutions and multi-terminal devices is currently being pursued.

The two principal components in circuit simulation tools are the underlying simulation engine and the models of the devices being simulated. Our device modeling methodology involves incorporating the UDM into the highly developed framework of existing circuit simulators. We are currently targeting SPICE simulators and analog hardware description language (analog

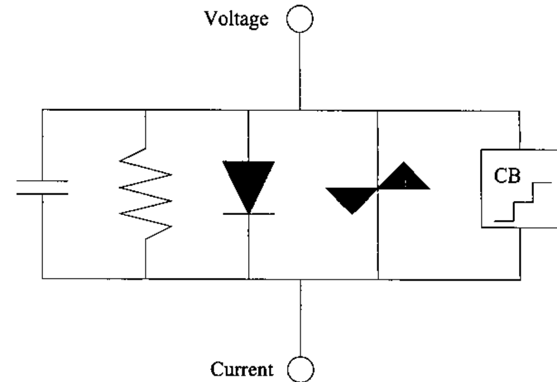

Fig. 1. The overall behavior of the two-terminal UDM consists of parameterized contributions of a variety fundamental effects. The fundamental components of the model presented in this paper are: capacitance, resistance, themionic emission, negatice differential resistance, and Coulomb blockade

HDL) simulators. SPICE simulation is the industrial standard for accurately simulating complex circuits. However, adding new and robust models to SPICE is somewhat tedious and requires modifying the internal source code of the simulator and recompiling. This process must be repeated for each new device when using the traditional SPICE device modeling approach. However, we can greatly reduce the effort of adding new models to SPICE with the UDM. After adding the UDM to the source code of a simulator once, we can robustly model a wide variety of devices by changing the parameters governing the individual fundamental effects. While SPICE simulators have traditionally carried the bulk of the simulation duties at the circuit level, analog HDL simulators are emerging as highly proficient tools for prototyping devices and simulation of complex devices. The results we report in this paper use a version of the UDM implemented in Verilog-A. Simulations were performed with the Spectre simulator from Cadence, which allows cosimulation of SPICE models and analog HDLs.

III. MODEL STRUCTURE

Since the purpose of the UDM is to provide device models that allow fast and accurate simulation of circuits containing *any* nanoelectronic device, the model has been set up in an empirical manner that masks the underlying physics. The I-V characteristics are essentially all that must be known to calibrate the empirical basis equations. Furthermore, empirical equations tend to be less tedious than their physics-based counterparts making them ideal for use in circuit simulation. This section presents the underlying UDM equations. While the equations are not necessarily derived from physics, they intuitively represent each phenomenon, provide low computational overhead, and also have good convergence properties. We use four basis functions, each representing a separate physical phenomenon, to construct the overall DC model. An additional resistor in series with the four parallel effects may also be beneficial.

A. Classical Device Effects

The first two of these effects, ohmic resistance and thermionic emission, are well understood due to their roles in classical devices, specifically resistors and diodes. Because they are

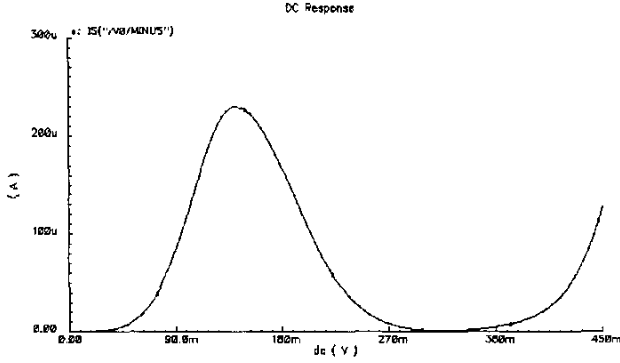

Fig. 2. A generic I-V characteristic of a resonant tunneling diode contains a positive differential resistance region followed by a negative differential resistance region.

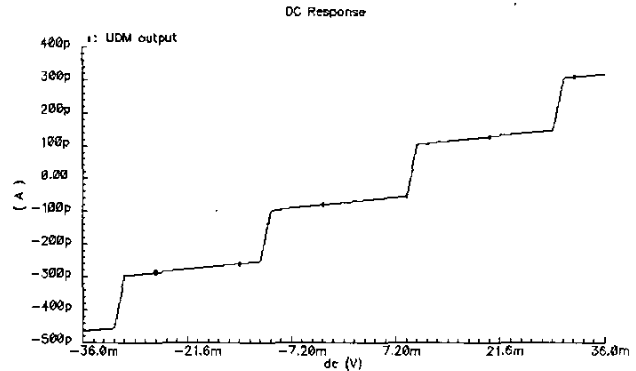

Fig. 3. An I-V characteristic exhibiting a Coulomb blockade typically has step-like features.

well known, little explanation is given here about these effects. Equation (1) is the current contribution from ohmic resistance, $I_R(V)$, while equation (2) represents the thermionic emission (diode-like behavior) portion of the current, $I_D(V)$.

$$I_R(V) = V/R \tag{1}$$

$$I_D(V) = I_s \cdot \left\{ \exp\left(\frac{V}{NV_T}\right) - 1 \right\} \tag{2}$$

The only parameter needed for equation (1) is R, which is the resistance for the model. Since the thermal voltage $V_T = kT/q$ is a constant related to the temperature, only two parameters are needed for equation (2), the saturation current I_s, and the emission coefficient N.

B. Tunneling Current

To determine an accurate model for the tunneling current, two regions of the I-V curve must be considered. As can be seen in Fig. 2, the tunneling current has a "mountain" and "valley" characteristic with a positive differential resistance (PDR region) followed by a negative differential resistance (NDR region). The overall tunneling current, $I_T(V)$, is given by equation (3), where $I_T(V)$ is composed of the PDR current, $I_{TP}(V)$, from equation (4), and the NDR current, $I_{TN}(V)$, from equation (5), which were first presented in [10]. These components contain an extra multiplier term, M, that serves as a connection between $I_{TP}(V)$ and $I_{TN}(V)$ [10].

$$I_T(V) = I_{TP}(V) + I_{TN}(V) \tag{3}$$

$$\begin{aligned} I_{TP}(V) = I_p \exp\left\{\frac{-(V-V_p)^2}{2\sigma_p^2}\right\} \\ \cdot \exp\left\{\left[1-\frac{V}{V_p}\right]\exp\left[M\left(V-V_p\right)\right]\right\} \end{aligned} \tag{4}$$

$$\begin{aligned} I_{TN}(V) = \left\{I_p' \exp\left[\frac{-(V-V_p)^2}{2\sigma_n^2}\right] - I_{TP}(V)\right\} \\ \cdot \exp\left\{\left[\frac{V}{V_p}-1\right]\exp\left[M\left(V_p-V\right)\right]\right\} \end{aligned} \tag{5}$$

It can be seen in the equation (5) that $I_{TN}(V)$ is based on a gaussian profile. We have found that circuits consisting of resonant tunneling diodes (RTDs) modeled with this gaussian converge better than RTD models employing an exponential substitute. The ability for a model to converge well is an essential property in circuit simulation leads to our choice of the gaussian function for $I_{TN}(V)$. It has been shown, however, that if the NDR region is extended then the exponential function may be preferable [10]. An exponential function for the NDR component of the tunneling current is given in equation (6).

$$\begin{aligned} I_{TN-E}(V) = \left\{I_p \exp\left[\frac{-(V-V_p)}{2\sigma_n}\right] - I_{TP}(V)\right\} \\ \cdot \exp\left\{\left[\frac{V}{V_p}-1\right]\exp\left[M\left(V_p-V\right)\right]\right\} \end{aligned} \tag{6}$$

When developing a model that includes tunneling using the UDM there are five parameters that must be considered. Two of the parameters are the peak current I_p and the peak voltage V_p, which specify the point at which the PDR region transitions to the NDR region. The width of the gaussian can be specified by using the parameters σ_p and σ_n. The final parameter M is associated with the step-like function that connects $I_{TP}(V)$ and $I_{TN}(V)$ and must be chosen as large as possible (usually $M > 10000$) to make the function approach the ideal case.

C. Coulomb Blockade Effects

The final contributing factor to a device modeled with the UDM is based on single electron charging effects. An example I-V curve for a device dominated by Coulomb blockade effects is shown in Fig. 3. The UDM takes into account the Coulomb blockade effects by adding a simple step function given by equation (7).

$$I_{CB}(V) = \frac{I_{STEP} \cdot \exp\left[C\left(V - V_{STEP}\right)\right]}{\exp\left(I_{STEP}\right) + \exp\left[C\left(V - V_{STEP}\right)\right]} \tag{7}$$

This function starts at a plateau current then rises to a "peak" current where the curve saturates after passing through a "peak" voltage (the term peak refers to a peak in the conductance vs. voltage curve). By combining this step function with the diode function and possibly the resistor function, the I-V characteristic for a device based on the Coulomb blockade can be developed.

When considering the step function by itself there are four parameters that must be taken into account. The main two pa-

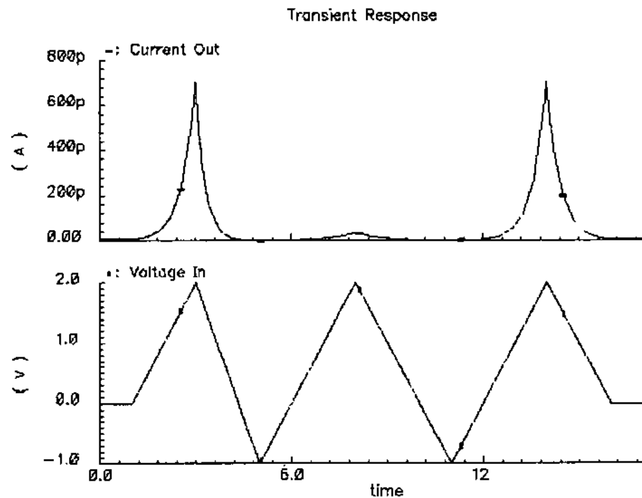

Fig. 5. The UDM can model devices having hysteresis curves using a set of parameters to describe each behavior.

rameters are the saturation current I_{STEP} and the peak conductance voltage V_{STEP}. The other parameter, C, is necessary for defining the slope of the rise from zero current to the saturation value. The parameter C is usually chosen to be quite large ($C > 5000$). One way to think of C is as the maximum conductance around the step. This model also makes use of a fourth parameter called N_{STEP} which is the number of steps that exist in the I-V curve. Multiple steps are not always seen in Coulomb blockade devices, but, for example, could exist in the case of a single electron transistor (SET) where the resistances of the tunnel junctions are different [12].

D. The Complete Model

With the various parts of the UDM defined, the current can be obtained from the parallel combination of all contributing phenomena. In addition to the parameters of each individual function, weights are assigned to each phenomenon to control the magnitude of the contribution. The current equation including all of the contributing factors and their respective weights is given by equation (8).

$$I_{UDM}(V) = \alpha_R I_R(V) + \alpha_D I_D(V) + \alpha_T I_T(V) + \alpha_{CB} I_{CB}(V) \quad (8)$$

The UDM presented in this paper is designed to model nearly any two-terminal device by selecting the correct parameter settings. Table I summarizes the UDM parameters. Included in the table are three parameters classified under 'Negative Voltage' because they govern the behavior of the I-V curve for negative voltages.

E. Hysteresis Modeling

In addition to non-classical behavior, the ability to model hysteresis will be needed for many nanoelectronic devices. Hysteresis in terms of nanoscale devices typically refers to a device's ability to switch between stable behaviors. These devices may ultimately provide the means for memory and programmable logic [4], [13]. Modeling hysteresis using the UDM

Contributions	
α_R	Resistor
α_D	Diode
α_T	Tunneling
α_{CB}	Coulomb Blockade
Negative Voltage	
TQ	Reflect in third quadrant
$Mirror$	Mirror the positive values
$Flip$	Flip the entire curve
Resistor	
R	Resistance
Diode	
I_s	Saturation current
N	Emission coefficient
Tunneling	
V_p	Peak voltage
I_p	Peak current
σ_p	Width parameter
σ_n	Width parameter
G	Gauss or exponential
M	Step rise
Coulomb Blockade	
V_{STEP}	Peak conductance voltage
I_{STEP}	Saturation current
N_{STEP}	Number of steps
C	Slope of the step

TABLE I
SUMMARY OF THE UDM PARAMETERS.

requires a data set for each I-V characteristic as well as a toggle definition. A toggle definition is an action that causes the behavior to switch between stable points, e.g., an applied bias. When modeling a bistable device, the UDM will reference one parameter set and then switch to a second parameter set when the toggle condition occurs. Fig. 5 shows a simulation of the UDM modeling a bistable device. The voltage across the device is on the lower graph and the output current is on the upper graph. We created one parameter set with a larger turn-on current, which is approximately the closed switch state of the rotaxane device in [4]. A second parameter set models the open switch state. Note that we slighly amplified the current for the closed state so that it is visually apparent that the UDM can model two different curves. We also use arbitrary time units due to the lack of transient data. We define a toggle definition of -0.7 volts as presented in [4]. In Fig. 5, the device begins in closed state and is toggled to the open state when the voltage across the device is -0.7 volts. The next voltage sweep produces an output current defined by the second parameter set, i.e. the open state. The second crossing of the toggle voltage reverts the I-V curve to the closed state. Although is was suggested that the rotaxane devices are only one-time programmable [4], we defined this model as reconfigurable for demonstration purposes.

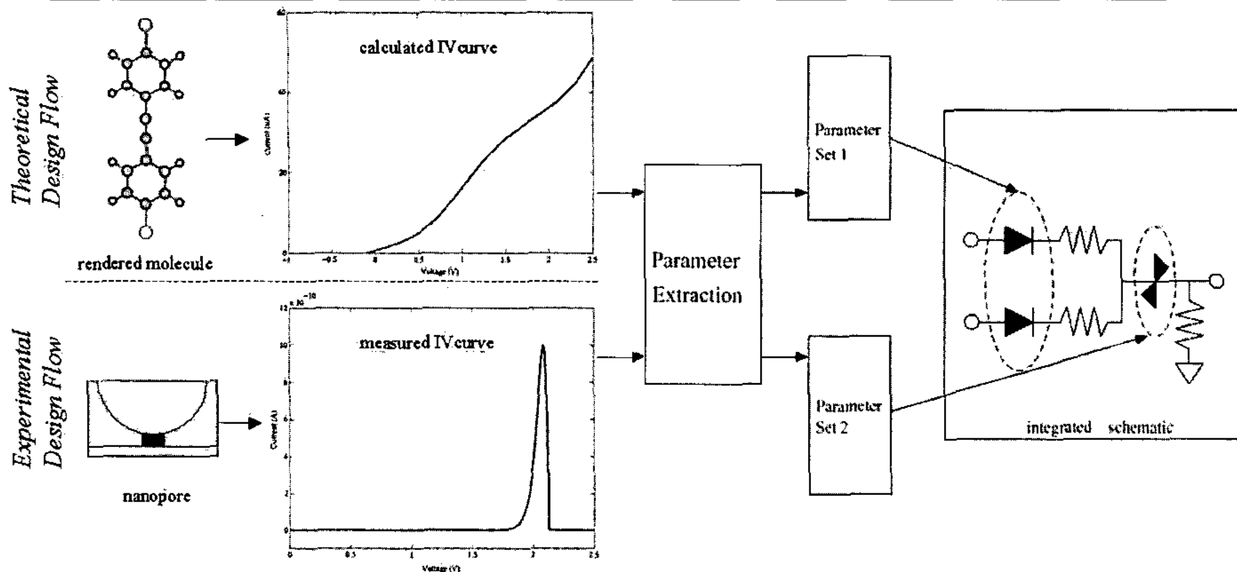

Fig. 4. Circuits containing multiple device types can be designed with the UDM. The UDM is blind to the method of device characterization. The devices can be characterized either theoretically or experimentally, providing the behavior of the devices are presented in IV curve data sets.

IV. Design Methodologies

One goal of the UDM is to provide a method for rapidly using a device with characterized behavior in circuit simulation without investing time in coding a device model or modifying a simulator. New devices are typically characterized either theoretically or experimentally. The input required for generating the UDM parameters is a file containing a set of current and voltage data points, i.e. points along the I-V curve. The data file is fed to a UDM parameter extraction tool. The UDM parameter extraction tool uses a genetic algorithm to match the UDM parameters to the input I-V curve. The extracted parameters are used during simulation to customize the UDM to the desired device. The UDM is blind to the method of obtaining the input set of I-V points. It can thus be used to model devices characterized either theoretically or experimentally, providing the I-V curve is described by a set of data points.

Fig. 4 shows the device design flows using the UDM for both of these approaches. The upper portion of Fig. 4 shows the theoretical design flow, where as the lower portion of the figure depicts the experimental design flow. The I-V curve in Fig. 4 from the theoretical design flow was obtained by using Purdue's Huckel-IV simulator [14], while the I-V shown in the experimental design flow was recreated from the molecular RTD in [15]. The key aspect is that the interface to the UDM parameter extraction tool is an I-V curve. The right portion of the figure illustrates that a schematic can contain different devices modeled by the UDM and that the source of the devices is blind to the UDM. The schematic shown in Fig. 4 is a design for an XOR gate [16]. We use this gate simply to illustrate the UDM design flows; however, the particular device characteristics in the figure do not yield a functional gate. We will show functional circuits employing UDM in the next section.

V. Circuit Examples

A good example of the UDM as it would be used in circuit simulation is a latch consisting of two resonant tunneling diodes (RTDs) as shown in Fig. 6a [1], [17]. In the circuit, one RTD works as the load device, while the other drives it, based on the bias voltage CLK. Due to the positive differential resistance (PDR) and negative differential resistance (NDR) regions of the RTDs, the circuit effectively has three stable points. Varying the bias voltage CLK and the input current causes the circuit to settle on either the high or low stable states. The process in which the RTD pair evolves toward one of these two states is known as the monostable-bistable transition (MBT). A detailed description of how this device works can be found in [1].

The RTD latch was simulated using the UDM in order to verify the capabilities of the model. These simulations were done using Cadence's Spectre with the UDM implemented in Verilog-A (an analog HDL). Verilog-A has been used mainly because it allows a behavioral description of a device to be included quickly and easily. The convergence properties of Spectre and Verilog-A are also attractive in comparison to other simulators. As can be seen in Fig. 6b, the circuit will latch the input voltage after the bias is pulsed low. Since the circuit is driven by the input current, the resistance at the input had to be chosen carefully to obtain the desired results. Another useful property of the RTD latch can be seen when cascading three latches as in Fig. 6c. These cascaded latches show that the circuit will settle closer to the stable points after each level of the cascade. Fig. 6d shows the output waveform of a cascaded RTD latch that demonstrates gain.

The RTD latch simulated using the UDM behaved as expected demonstrating that the model worked correctly. This example shows the UDM behaves well for both tunneling and diode-like devices but more work needs to be done to verify the other properties included in the model. Single electron devices and circuits which utilize phenomena such as the Coulomb

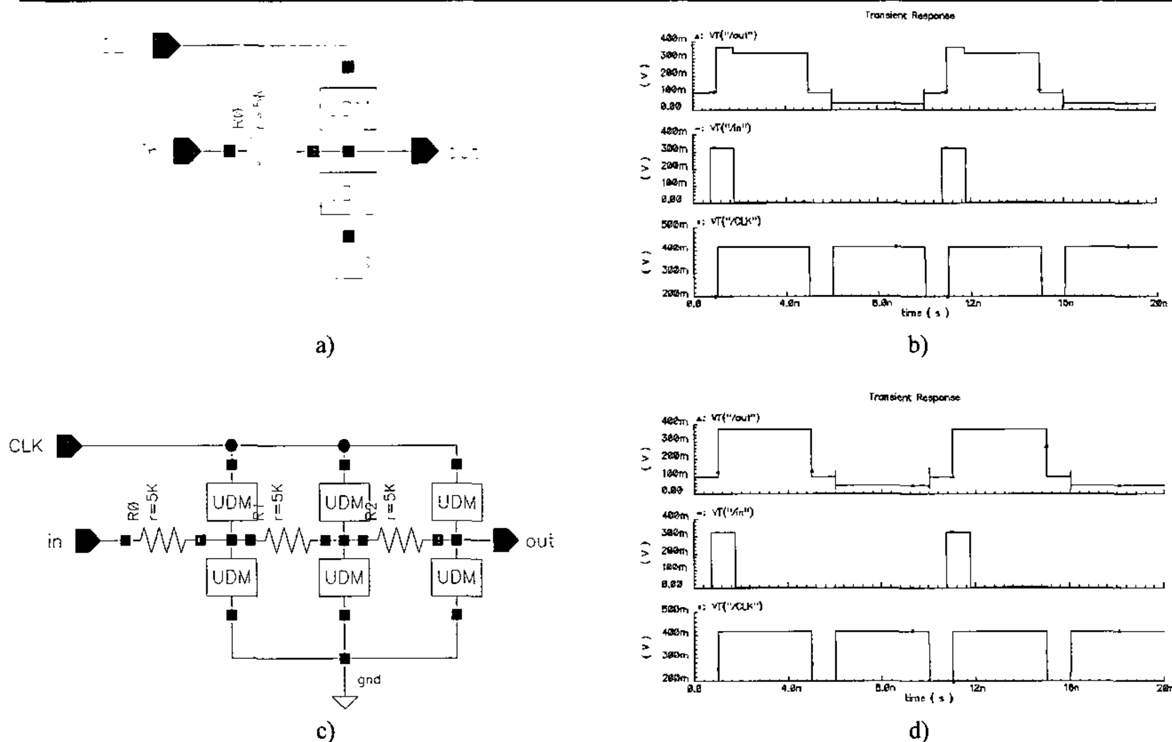

Fig. 6. RTD latch circuits demostrating the UDM in action: a) single RTD latch showing how two RTDs can be used to sample a signal, b) the input signal *in* is captured once the bias voltage CLK drops low and remains until CLK goes low again, c) cascading multiple RTD latches provides the ability for gain, d) gain can be seen in as the output of the circuit comes closer to the high and low stable points of the RTD.

blockade need to be simulated as well.

VI. Conclusion

We have presented an approach for generating a SPICE level or analog-HDL model for nearly any type of device behavior. We believe such a modeling approach will be necessary for simulating the many new and emerging nanoscale devices in quick and robost fashion. Our universal device model (UDM) addresses the challenge of correctly balancing accuracy, complexity, and flexibility. We have presented the underlying UDM equations that qualitatively represent fundamental classical and quantum phenomena. In addition, we have demonstrated the UDM's ability to model hysteretic devices and have given circuit examples that show the UDM in action.

VII. Acknowledgments

This work was supported in part by a University of Virginia FEST grant and by an NSF NIRT award. Thanks to Dr. James Ellenbogen from the MITRE Corporation for inspiring discussions.

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