SESSION 26: Evening Panel Discussion

Nanoelectronics – Now or Never?

Tuesday, December 14, 8:00 p.m.
Continental Ballroom 6-9

Moderator: Mark Lundstrom, Purdue University

Traditional 'top-down' microelectronics has become nanoelectronics with device dimensions comparable to those being explored in the new field of 'bottom-up' nano- and molecular electronics. We use the terms, top-down and bottom-up, in a very general sense. Top-down refers to a way of thinking and building that begins at the macro (continuum) scale and pushes to the nanoscale. Bottom-up refers to a way of thinking and building that begins at the atomistic level and builds up to the nanoscale. The top-down approach has already delivered silicon MOSFETs with channel lengths of ~ 5nm, but scaling down device dimensions with commensurate increase in device and system performance is increasingly challenging. Bottom-up technology has demonstrated molecular switches, nanotube and nanowire FET's, NDR and single electron devices, and ultra-dense memory prototypes. Is bottom-up nanotechnology ready to address the industry's challenges, or is it still long-term research with essentially unpredictable outcomes? This panel will debate the question of what the intersection of top-down and bottom-up electronics will mean to semiconductor technology of the future.

A panel of experts will provide their perspectives and engage the audience in a debate on the likely role of unconventional nano- and molecular electronics in future electronic systems. Specific questions to be addressed include:

- How far will the top-down approach take us and what will ultimately limit it?
- Has device scaling slowed or stopped?
- Is nanoelectronics here? Has silicon microelectronics become silicon nanoelectronics?
- How does/can bottom-up nanoelectronics address the challenges of CMOS scaling?
- What new information processing paradigms will bottom-up nanoelectronics enable?
- How can bottom-up nanoelectronics complement and extend Si CMOS?
- What can bottom-up nanoelectronics do that Si CMOS can't?
- What have been the major successes (scientific and technological) of three decades of research in nano- and molecular electronics? What are the Grand Challenges now?
- The nanotechnology field has often been accused of suffering from an excess of hype. Is this so? If so, why? Is there something real here?
- What is or should be the goal of research in bottom-up nanoelectronics?

Panel Members:

Joerg Appenzeller
IBM

Robert Chau
Intel

Andre DeHon
Caltech

Jim Heath
Caltech

Mark Horowitz
Stanford

Charles Lieber
Harvard

Jim Meindl
Georgia Tech

Mark Reed
Yale

Jim Tour
Rice University

Victor Zhirnov
SRC