Recent Advances in Nanotechnology: Key Issues & Potential Problem Areas

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Abstract: Recent developments in nanosciences and nanotechnology have created tremendous enthusiasm among researchers and scientists across the globe. The rapidly increasing interest among various engineering disciplines toward research and development needs of nano-domain have spurred the growth in areas such as nanoelectronics, biotechnology & health delivery system and commerce in general. In this paper, a state-of-the-art encompassing the recent developments and the key problems in nanomanufacturing that relate to the domain are presented. Furthermore, contribution in this field from the researchers in different parts of the world are included and compared to monitor the present progress.

With the down sizing of present silicon IC technology, validity of Moore's law has become seemingly limited. However, it is strongly believed that the novel materials will provide the answer for further scaling of device density and performance. For example, most recent attention has been paid on carbon nanotubes, which can be used in nanosize electronic devices. It is still a question whether nanotube based technology will actually contribute to the existing CMOS technology or it is a totally new device architecture from CMOS technology. Besides, it is unclear whether this material will meet scalability, durability and existing performance. Modelling and simulation is a vital element for gaining insight to the behaviour of these materials and also to the characterization process. A part of this paper will be devoted to fully analyze the current trends in nanoelectronics based on nanostructured materials other than silicon.

I. INTRODUCTION

This paper is aimed at presenting current status, recent advances and challenges ahead in the field of Nanotechnology.

In June of 2001 Intel's semiconductor & microelectronics research team projected that by 2007 the company will have 45nm technology (45nm transistor on microprocessor chip) in full production. In late 2002, Intel revised its projection upward with a promise of delivering 45nm transistor by 2005 and projected that 30nm transistor for microprocessor production by 2007 instead. This accelerated development in semiconductor industry signals that some solution to the currently perceived end to Moore's Law might be insight and might become a reality sooner than anticipated. It also seems to indicate that radically different technologies and processes might be close to realization, and therefore, Moore's Law as applied to semiconductor industry can be applied endlessly at least for a foreseeable period. Whatever one might infer from the recent development Intel has been in nanometer range in its manufacturing operation for about last five years. As we march forward deeper into the nanotechnology era, it is critically important for us to look into the issues of manufacturing for nano-scale devices. According to Professor Yoshio Nishi, Director of Stanford Nano-Fabrication Center, Integrated circuits technology is the prime example which, to some extent, is almost in the domain of "nano-scale manufacturing". To look back at what we have experienced in the past in order to bring a variety of technologies up to what we see today would be meaningful exercise to understand the magnitude of challenges from creation of ideas through manufacturability demonstration via proof of concept[2].

To those who have high stakes in silicon-based technologies any significant change in the means and resources would be extremely expensive purely from short-term cost standpoint. Such a development would result in disruption across the major segment of world economy. In our daily lives a great deal is dependent on goods and services that are primarily derived from silicon-based technologies today. Therefore, it would be important to analyze what are some of the new technologies, processes and resources that might play an important role with some plausible answers to 'why' and 'how', and possibly some idea of 'when'.

II. RECENT DEVELOPMENTS

In the domain of sub-micron to nanometer range for large-scale fabrication an accelerated pace in momentum has been observed in the recent years. Yet several daunting challenges lie ahead. Although semiconductor industry has already been in nano domain for sometime now but further progress with significant levels miniaturization is becoming expensive as well as technologically demanding. As

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much as fabrication at this scale is posing serious problems inspection and rework is not possible. We know from the era of industrial revolution that measurement, compliance and assurance to consistently achieve a desired quality standard would not have been realized without adequate developments in metrology. Therefore, nanoscale manufacturing would not be possible without sub-nanoscale measurement capability with high precision and repeatability without loss of fidelity and reliability. One research group at MIT under the leadership of Professor Henry Smith is working on filling this void. This group is utilizing a variety of laser interference techniques and feedback systems to achieve fiducial grids with nanometer-level accuracy and long-range spatial-phase coherence. These grids, in turn, are employed in fabrication and metrological tools for producing nanostructures with nanoaccuracy. Often scientists conceptualize and model new development from natural processes. But here is an anomaly. Although living systems employ nanostructures and appear to ignore the issue of nanoaccuracy, this turns out not to be the case, and in artificial nanostructures the history of the industrial revolution, with respect to metrology, is almost certainly to be repeated.

As semiconductor industry moves further in nano domain for large scale manufacturing one important indicator that will continue to be used is number of transistors and like devices packed in 1 cm^2 area. In the recent years the latest Intel processors are jammed with 4 million such devices. In the near future this number is projected to rise upto a billion. These processor chips are already packed in multiple layers with increasingly larger number of electronic devices. Between two device layers, another layer of silicon dioxide is deposited to provide an insulating layer and to protect them from high electric fields. In order to pack higher number of electronic devices microscaling of these devices would be necessary. Several problems arise when attempting to microscale electronic devices. For example, the smaller the transistor, the thinner would be its silicon dioxide insulating layer becomes. As a result, electrons on a transistor's gate can leak through or "tunnel" into the silicon substrate below, thus affecting the transistor's performance. To overcome this problem newer materials with higher dielectric constant need to be developed and used in the fabrication of future microscale electronic devices. In addition, as a result of shrinking the size of interconnections, unwanted motion of component material can occur in the interconnects that are typically aluminum wires, that join the chip's various electronic elements. This is known as *electromigration*, or current-induced diffusion. With the increasing density of circuit elements, other novel materials and techniques are being investigated to solve electromigration problems.

By combining elements from groups III and V, custom-made electronic materials can be produced for various microelectronic devices. One approach to building these devices is *heteroepitaxy*. By layering thin films of different materials on a crystalline substrate, heteroepitaxy can provide a multilayer superlattice, a periodic array of alternate layers made of two semiconductors. The techniques used to grow heteroepitaxial films include: liquid-phase epitaxy, where cooling of a heated solution of desired elements occurs on a substrate; chemical vapor deposition, which exposes the substrate to heated gaseous elements or compounds; and molecular beam epitaxy, which targets heated molecule beams or atoms at a substrate in an ultrahigh vacuum.

Researchers are not restricted to naturally occurring III-V compounds. Although a material's structure and properties determine its performance level and behavior, structural configurations can be changed through closely controlled processing methods[3]. Crystal growing techniques, such as molecular beam epitaxy (MBE), can combine the desired properties of many chosen elements. MBE techniques have been referred to as "spray painting with atoms" by Bell Laboratories, where it was invented. Molecular beam epitaxy can build custom-made semiconductor crystals by depositing different semiconductor compounds in evenly deposited and alternating atomic layers, or films. Beams of a chosen material's atoms or molecules are emitted from heated effusion cells, or crucibles. These beams are aimed at a single-crystal substrate on a temperature-controlled substrate holder in an ultrahigh vacuum chamber. The resulting epitaxy is oriented or controlled growth, with each successive layer resembling the lattice orientation of the layer beneath it. Finished films are uniformly flat to within one atom in depth. Professor Mildred S. Dresselhaus's group at MIT is engaged in engineering & characterizing different types of carbon nanotubes (CNT) with properties ranging from the ones typically found among semiconductors to those observed among conductors.

III. CHALLENGES AHEAD

Several researching groups in the nanoscale manufacturing are working on an entirely different approach realizing the limitations of conventional fabrication processes especially for sub-20nm critical dimension for process control[2]. At lower gate lengths of 20 and 15nm, the transistor - a building block and basic unit of any semiconductor device today - still maintains excellent device characteristics and follow traditional scaling with respect to gate delay and energy delay, although off-state leakage and gate leakage increase substantially limiting the performance and its basic function. In order to

circumvent these problems the research community is exploring processes in life sciences. One of these is the recent discovery of active microelectronic arrays. Active microelectronic arrays have been developed for applications in genomic research and DNA diagnostics. These active devices combine the best attributes of both DNA array and "lab on a chip" technologies. These microarray devices are able to create reconfigurable electric field transport geometries on the array surface, which allows charged reagent and analytic molecules (DNA, RNA, oligonucleotide probes, amplicons antibodies, proteins, enzymes, and even cells), to be moved to or from any of the microscopic test sites on the device surface. These same microelectronic array devices may also have potential use for nanofabrication applications, including the directed self-assembly of molecular, nanoscale and microscale components into more complex structures, and for creating higher-order mechanisms. Electric field assisted self-assembly using active microelectronic arrays is being investigated as a "Pick and Place Heterogeneous Integration" process for fabrication of two and three dimensional devices and structures within defined perimeters of larger silicon or semiconductor structures. This technology has the inherent hierarchical logic of allowing one to control the organization, assembly and communication of structures and components from the molecular scale ---> to the nanoscale ---> to microscale systems. Living systems have macromolecular structures called enzymes, which have highly efficient chemomechanical dynamic properties. These enzyme molecules are true "nanomachines" and the very engines of life. Enzyme molecules, for which many of the 3-D structures are completely known, have chemomechanical properties that allow them to rapidly synthesize and/or degrade an almost limitless number of complex molecules. Many are able to efficiently convert chemical energy into mechanical energy and translational motion. More recently, ATP synthase and other such enzymes have been modified and used as nanomotors. In principle, the functioning of such an enzyme molecule should be well within the general understanding of today's scientists and engineers. Nevertheless, there are no examples of any "synthetic macromolecules" with the properties of an ATP synthase. The explanation for this seeming dichotomy may be that we have not really applied the same level of effort to this area of molecular engineering, as has been applied to many other areas. The acceleration of efforts to create nanostructures with higher-order chemomechanical properties should be a key objective of the nanotechnology initiative.

Stanley Jurga & group at MIT [2] is engaged in an NSF funded research on functional three-dimensional (3D) nanostructures in a silicon-based device. Functional 3D nanostructures are of interest in numerous technological domains. The 3rd dimension promises to extend microprocessors and memories beyond "the end of Moore's law," *i.e.* when feature sizes of planar electronics reach their minimum practical limit. In applications other than electronics, the need to conquer the 3rd dimension is even more urgent. Examples include optical elements that integrate sensing and processing for defense or commercial applications, miniature reactors for chemical and biochemical analysis, drug delivery by miniaturized microfluidic implants, micromechanical and nanomechanical energy storage elements, and environmental monitoring and industrial quality control applications. However, 3D fabrication is not well understood and developed. Our CMSE seed grant research is aimed at a specific method for 3D fabrication and assembly, which we refer to as "membrane folding." and a case study in three-dimensional diffractive optical elements.

For a 3D technology to be successful and widely applicable to the world of solid-state electronics, MEMS, and nanomanufacturing, it must satisfy the functional requirement of sufficient connectivity between the micro and nano devices that compose the system (i.e. the transistors and capacitors of a microchip). Additionally, a winning technology must avoid competing against the momentum of an existing industry with established tool-sets and large capital investments; a new 3D technology must be easily integrated and compatible with current methods of fabrication that remain planar in nature (i.e. photolithography, etching and deposition are all 2D).

Researchers at MIT adopt a two step process designed to satisfy the following functional requirements: (a) integration of dimensional scales from the nano to the micro and beyond; (b) maximum utilization of existing fabrication tools; and (c) flexibility in achieving a large number of possible 3D configurations with minimum cost and maximum repeatability and yield. That meets the connectivity constraint, provides an additional means for actuation, and allows for the seamless integration of existing 2D fabrication methods as well as new advances in the state of the art photolithography and nanopatterning. In the first step, all devices are fabricated on a planar substrate just as they are in today's semiconductor industry. In the second step, is an assembly technique in which the planar substrate is folded into a 3D structure or quasi-3D. Designated compliant zones act as hinges between stiffer regions that contain micro and nano devices. By virtue of compliant circuitry that spans the hinge areas, full 2D connectivity is preserved across the entire length after folding. This is important for electronics as well as communication in MEMS sensors and actuators and integrated nano devices[2]. An additional source of connectivity may also be achieved in the vertical, 3rd direction if by designing vertical connections to be formed when the

planar folds are designed to contact each other at reach predetermined locations during folding.

Most connectivity remains within the plane and through the compliant hinges, while sparse connections permeate the vertical direction. The architecture achieved through various folding techniques is unique to the micro and nano realm because it creates a framework for building devices and structures that were previously impossible to imagine or too expensive to fabricate with other methods. For example, at present, this study aims to build 3D diffractive-optical elements (3D-DOEs) as a case study in the technology development for folded-membrane devices. 3D-DOEs promise better performance in terms of efficiency and angular selectivity than traditional 2D diffractive-optical elements. Spacing multiple diffractive gratings or fresnel zone plates (perhaps as many as 50) vertically above one another establishes a matched filter with very high efficiency. Although such a 3-D structure could be fabricated one layer at a time, the folded-membrane approach should be far more cost effective. Also, the folded membrane approach may enable tuning of the diffractive optical systems, for example, by electrically varying the spacing of the stack.

In their preliminary work, we have demonstrated a single 180-degree fold in a silicon-based device with magnetic-actuation-effecting induced folding. The gold hinges are plastically deformed so that the folded membrane remains near 180 degrees. Electron beam evaporated gold was chosen for the compliant hinges due to its high ductility and comparatively small spring back angle. The hinges also complete a current loop around the perimeter of the membrane. By placing the device in a magnetic field and controlling the magnitude of current in this loop, a Lorentz force is generated that rotates the flap about its hinges. The Lorentz force is highly controllable and thus allows extensive experimental characterization of the mechanics of folding in our device. In the future, we will also explore other means of actuation such as stress and chemically-induced folding. Some of these alternatives are more attractive than the magnetic method from the point of view of alignment and flexibility in 3D assembly schemes. is an ideal means of actuation for the first round of prototypes because it is a highly controllable force that allows for good experimental analysis of the mechanics of folding.

The first 3D diffractive device is constructed in its unfolded state attached to the substrate. Electrostatic combdrives tune the period of the binary grating, which changes the angle of the diffracted orders. The fresnel Fresnel zone plate (essentially a diffractive lens) will be folded over and aligned to the grating as a demonstration of compound diffractive optics in 3D.

Future work will focus on the final alignment and latching of the folds in addition to new actuation methods for folding that could be categorized as templated-self-assembly. Work in implementing multiple folds and studying their behavior of multiple folds is also underway. These steps are the early formative building blocks for establishing a multi-use platform. 3D assembly through folding lends itself to broader goals such as combining discrete devices of varied functionality (optics, electronics, microfluidics, etc) into one cohesive, self-contained system capable of multiple tasks such as advanced sensing and response.

IV. CONCLUSION

We have attempted to take a snapshot of research activities and recent developments in the field of nanotechnology. It could not be complete by any means although we intended to report all significant ones here. We know we ran out of space here to include recent developments from the group at Delft University of Technology, Delft, Netherlands.

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