Silicon Technology Directions in the Nanoelectronics Era

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Abstract

For decades the scalability of MOS technology has fostered continual improvements in almost every dimension of electronic products. However at ~130nm, VLSI has neared a variety of limits threatening compromises, and the industry has returned to a state more like the 1970s where new directions in materials, processes and devices are being intensively evaluated. However the complexity of the challenge today is many orders of magnitude higher – e.g. controlling atomic thickness over billions of components – while economic pressures, both on R&D as well as time to yield, are driving a new industry landscape. This presentation explores key technology challenges and reviews main industry directions – many times across traditional R&D boundaries – that will enable the pervasive growth in application content promised by the nanoelectronics era.

Industry Landscape

With the onset of volume 90nm CMOS, nanoelectronics production has unequivocally begun, following in the footsteps of over 40 years of constant improvement IC performance, power, size and cost. And although some rates of improvement have slowed, the most important factor – cost per function (bit, gate, etc.) – continues to encourage products to be designed in new technologies. And with more electronics content being driven by global consumer applications, cost is a more important driver than ever before.

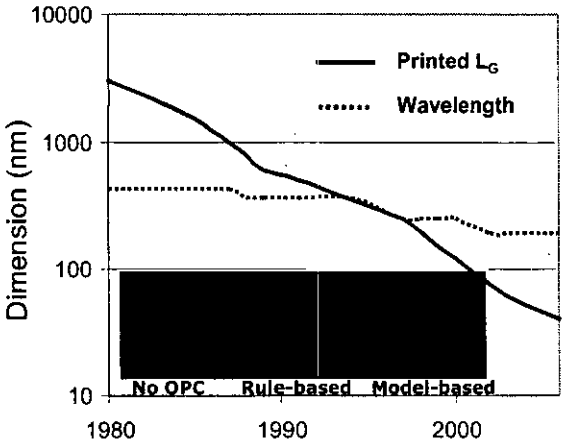

Figure 1: Optical lithography wavelength and final gate length as a function of year.

Because scaling cannot continue to drive exponential improvements in every product dimension forever, new technologies require compromises and circuit workarounds. The so-called "red brick wall" – where by industry consensus[1] no solution is yet known to meet a target device specification – is getting closer to the present. Process solutions are being investigated at a rapid pace with increased efforts on new materials and integration schemes. The expanded scope of R&D together with the continued need for higher precision escalates process R&D cost. And product design costs continue to increase due to the complexity of higher levels of integration compounded by the need to include the impact of manufacturability more directly. All of these issues have led to new modes of R&D collaboration – joint development between suppliers-customers, alliances between peers, and connections between heretofore non-interacting segments (e.g. EDA and equipment).

Nanopatterning Technology

Optical lithography has continued to extend well beyond expectations, producing features smaller than the wavelength λ of exposure radiation since mid 1990s (0.18um). Because near term evolution of λ beyond 193nm appears impractical, industry focus has been on improving the numerical aperture NA of the optical systems and process improvements (lower k_1) as described by the Rayliegh equation: $CD = k_1 \cdot \lambda/NA$. Immersion lithography has allowed further improvement of NA by reducing reflections at the exit of the lens. Key process improvements include reticle enhancement technologies (OPC/RET) and enhanced process integration schemes (multilayer films, advanced etch).

It is expected that immersion lithography with reticle and process enhancements should extend the roadmap to at least 32nm. As in the past, there is no clearly leading contender beyond optics with EUVL, projection beam, direct/maskless beam and now imprint lithography all as possible candiates.

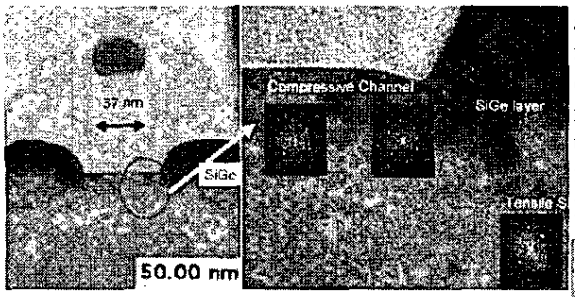

Figure 2: Sub 37nm PMOSFET with selective SiGe source/drains[4] to realize 35% improvement in I_{on}.

Nanoscale Transistors

Transistor scaling has reached a power crisis as the nanoelectronics era has been entered. The fact that threshold voltages cannot be reduced indefinitely and oxide leakage and reliability would limit SiO_2 has been known for some time. In fact, SiO_2 based gate dielectrics have been extended well past what many thought possible – to at least the 65nm node using plasma nitride treatments to minimize leakage and dopant diffusion.

High-k gate dielectrics have made significant progress, with two primary candidates – HfO_2 for high performance and HfSiON for low power – both showing excellent capacitor behavior. Used with polysilicon alone however, transistors with these materials to date have shown lower channel mobilities. Together with eliminating poly depletion capacitances, this has led to intensive R&D to develop metal gates along with the high-k dielectrics[3]. Metal gates have their own challenges, including the need to achieve dual workfunctions and process integration. It currently seems likely that high-k gate dielectrics will be introduced in some 45nm nodes, primarily with metal gates but perhaps even with polysilicon for some mobile applications.

Strain engineering has arisen as a significant innovation, allowing transistors to recoup performance improvements thought lost to voltage scaling. Stress can be induced to improve both NMOS and PMOS using deposited films (etch stops, PMD) or in the substrate through epitaxy or isolation fill. Simulations show that stress from multiple sources can be additive, suggesting that I_{on} improvements required for as many as two technology nodes can be achieved using strain inducing techniques. It appears that the combination of new gate materials and stress engineering should extend the life of the planar MOSFET to at least the 32nm technology node.

Interconnect

Interconnect scaling presents limited possibilities, owing to the lack of materials electrically better than Cu and air. In fact, unlike gate length, the rate of progress in lowering dielectric constants has slowed between each ITRS update. It is even a challenge to keep Cu resistivity from increasing at smaller geometries owing to grain boundary and line edge roughness effects. And no practical discontinuity (e.g. optical or wireless) has yet been found for on-chip distribution.

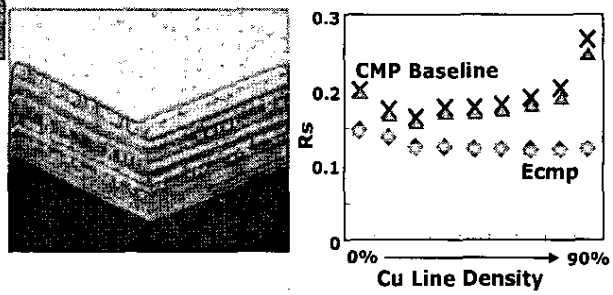

Figure 3: (a) Multilevel metal interconnect using Black Diamond™ low-k dielectric; (b) improved metal planarity using Ecmp.

Therefore development of interconnects for sub 130nm has focused on getting as close to a perfect air/copper as possible – e.g. continuing to improve low k while maintaining mechanical integrity for packaging, maintaining Cu resistivity and miminizing parasitic effects (added higher k dielectric layers, higher resistivity metal barriers) that introduce higher effective RC. Other key technology drivers include manufacturing control to mitigate design challenges and limiting or even reducing process cost/level to allow more interconnect levels to circumvent RC bottlenecks.

A good example of new process innovation for scaled interconnects is the recently developed Ecmp process[5] which by combines electro-, chemical and mechanical polishing to enable use of more fragile, lower-k films while improving uniformity and lowering process cost through less expensive consumables.

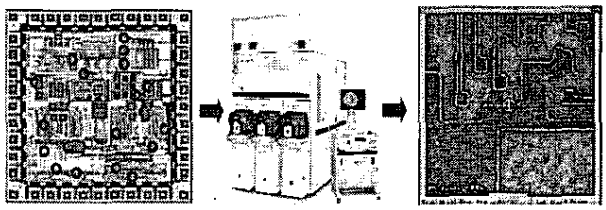

Figure 4: OPC Check™ connects critical areas in the design database directly to SEM inspection to dramatically accelerate OPC/RET validation.

Design and Manufacturability

The increasing cost of design in new technology nodes is exacerbated by design for manufacturability (DFM) issues – e.g. arising from the impact of feature fidelity and reproducibility rather than just random defect driven yield[6]. This has led to supplementary

design tools, extended design rules and added iterations to get products to adequate yield. It should not be surprising that the fairly simple rule based design approach would inevitably be challenged.

Because the health of the industry depends on rapid ROI of fab and design investments, DFM is a top priority for the entire R&D chain. From a tool/process perspective, emphasis is given to developing processes like Ecmp that are inherently better controlled. Integrated metrology is more broadly employed to monitor process conditions and resulting structures, increasingly fed back to use in automated adaptive process control. And metrology and inspection tools can being linked to design databases to give more rapid learning, e.g. for more quickly optimizing OPC.

Conclusions

The nanoelectronics era holds the promise of expanding the IC revolution towards more content, more mobility and greater global penetration. To be realized, timely innovations are essential, requiring new processes, materials and design techniques together with new levels of collaboration throughout the industry.

References

[1] International Technology Roadmap for Semiconductors, 2004.
[2] See SPIE Proc. Intl Symp. on Microlithography, Feb. 2005.
[3] J. K. Schaeffer et.al., IEDM Tech. Dig., Dec. 2004.
[4] P. R. Chidambaram et.al., Proc. VLSI Tech. Symp., Jun. 2004.
[5] "Flat, cheap, and under control," IEEE Spectrum, Jan 2005.
[6] See Proc. Intl. Symp. on Quality Electronic Design, Mar. 2005.