12.5 Digital Logic Using Molecular Electronics

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This reconfigurable architecture is based on chemically assembled electronic nanotechnology (CAEN). CAEN is a promising alternative to CMOS that takes advantage of chemical synthesis techniques to combine molecular-scale circuit elements (such as resistors, diodes, and reconfigurable switches) using directed self-assembly. A serious drawback to CAEN is the inability (in the near-term) to include three-terminal devices (e.g., transistors) in circuits. A molecular latch, based on molecular resonant tunneling diodes (RTDs) [6], provides the most important benefits of the lithographically fabricated transistor: voltage restoration, fan-out, tolerance to manufacturing variability, and I/O isolation.

To make CAEN circuits economically viable they must be manufactured through thermodynamic self-assembly and self-alignment. For example, devices will be incorporated into the circuit out of topological necessity, i.e., devices are included only at the intersection of two wires coated with the appropriate molecular device. Because self-assembly is an imprecise, thermodynamically controlled process, it can no longer be expected to produce working devices in specified locations with high reliability. This implies that the devices must be testable and that defects must be tolerated. Moreover, self-assembly can produce only a limited range of circuit complexity while remaining manageable. Thus the manufacturing process must be decoupled from the production of the final circuit. Any deterministic aperiodic circuit must be created through configuration after the device is fabricated.

A plausible hybrid architecture combines molecular self-assembly and lithographically-produced aperiodic structure. At the nanoscale, all subprocesses are self-directed; only at the micron scale are deterministic operations allowed. Functionalized wires are aligned into parallel rafts using flow techniques. These rafts are then combined into 2-D grids. Active devices are created, without the requirement of precise alignment, wherever two appropriately functionalized wires intersect. The rafts are then aligned with a lithographically produced CMOS die which provides support circuitry. Note that this manufacturing technique rules out 3-terminal devices.

Figure 12.5.1 shows a schematic of a proposed nanoblock that can be constructed using the above techniques. The MLA is a 2-D grid of reconfigurable diodes that can be configured into circuits based on diode/resistor threshold logic [2]. Figure 12.5.2 shows how a nanoblock can be configured into an AND gate. The reconfigurable nature of the circuit also allows defects to be tolerated [3].

The architecture described above satisfies the key constraints of nanoscale technology. It requires no deterministic manufacturing steps at the nanoscale, it uses only two-terminal nanoscale devices, and it is reconfigurable. To build an operational circuit, however, requires signal restoration between nanoscale wire grids. Figure 12.5.3 shows a molecular scale latch that provides signal restoration through the interaction of a pair of molecular RTDs. This latch is constructed using a nanowire that includes the RTD molecules within the wire. Such inline wires are constructed and characterized [5]. Simulations are based on NDR molecules characterized in [1].

While RTD latch technology is exploited in constructing a GaAsFET logic family [4], in CAEN the RTD latches are used for a different purpose: they are used primarily for signal restoration. All computation is performed by diode-resistor logic and the latch restores the signal for a later stage. Work in the 1960s with tunnel diodes and threshold logic was hampered for two reasons. The first, high inter-device manufacturing variability, is solved due to the characteristics of the molecular RTDs (they have a much higher peak-to-valley ratio). The second was a lack of I/O-isolation.

To provide I/O isolation, additional devices are incorporated into the latch, and Vdd is clocked as shown in Figure 12.5.4. The molecular-scale diode is added to prevent current from a downstream latch from flowing to set an upstream latch. The resistor immediately following the RTD-pair forces enough current into RTD_{drive} to allow it to switch high, while allowing enough current into the next latch to determine its value. The resistor to ground allows a latch to go low when the downstream circuit is high. The value of this resistor must be large to prevent current loss that would cause latch-setting failure. However, the resistor should also be as small as possible to minimize latch reset time.

Finally, a clocking scheme for the pull-up voltage is introduced, as shown in Figure 12.5.4 b. The pull-up voltage is temporarily brought to ground during the setting of the preceding latch. This removes the forward influence and allows the latches to be set properly.

Several simple circuits using the above latch configuration are simulated using SPICE, including the delay circuit in Figure 12.5.5 and the AND, OR, and XOR circuits shown in Figure 12.5.6. Circuits with more logic levels are also successfully simulated. The latch appears to be stable against the expected variability brought about by manufacture. Because of the relatively low current required to switch states, one molecular latch can drive several other latches, i.e., latches can have moderate fan-out. In combination with the clocking scheme described above, the latch also provides the necessary I/O isolation to ensure scalability of these circuits.

Some caveats are necessary, however. While not intrinsically slow, the RTD devices discovered thus far are extremely resistive, thus, the RC constant for circuits incorporating them is large (on the order of hundreds of nanoseconds). Also, the relative sizes of the various resistors must be controlled during manufacture to ensure that they are properly matched. Lastly, the use of a clocked pull-up voltage may result in increased power consumption.

Acknowledgments:
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References:
[1] J. Chen, M. Reed, "Molecular wires, switches and memories," Molecular Electronics, Dec. 2000.
[2] C. P. Collier et al., "Electronically configurable molecular-based logic gates," Science, 285:391–3, 1999.
[3] S. C. Goldstein, M. Budiu, "Nanofabrics: Spatial computing using molecular electronics," Int'l Symp. on Computer Architecture, June 2001.
[4] R. H. Mathews et al., "A new RTD-FET logic family," Proc. of IEEE, 87(4):596, 1999.
[5] T. Mayer et al., "Molecular electronic building blocks: Functional metal nanowires," ACS, Aug. 2001.
[6] M. Reed et al., "The Design and Measurement of Molecular Electronic Switches and Memories," ISSCC Digest of Technical Papers, pp. 114–6, Feb. 2001.

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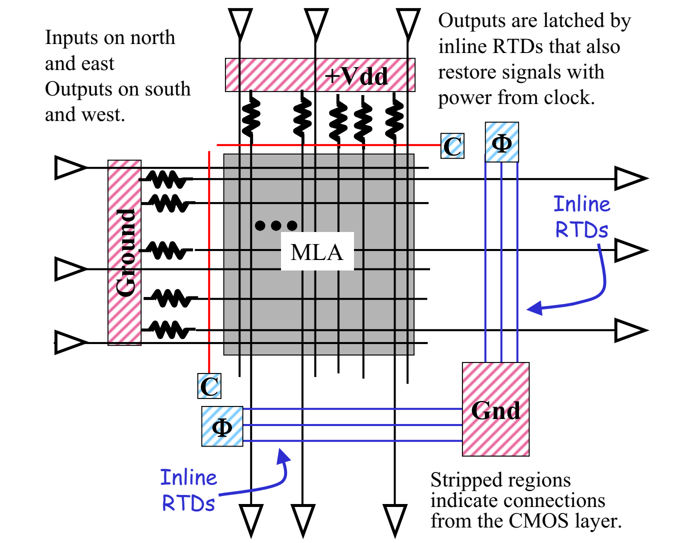

Figure 12.5.1: A schematic of a nanoblock.

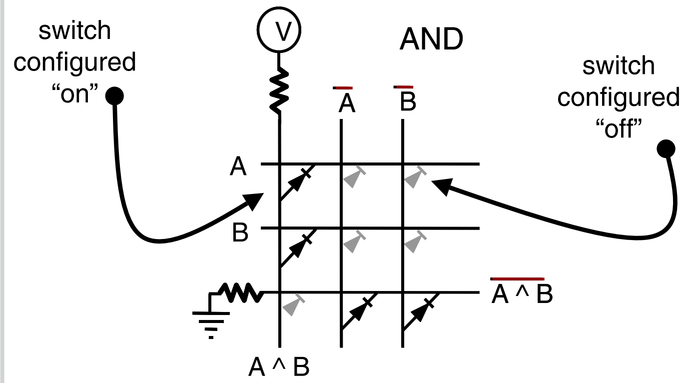

Figure 12.5.2: A two-input AND gate implemented in a reconfigurable CAEN grid.

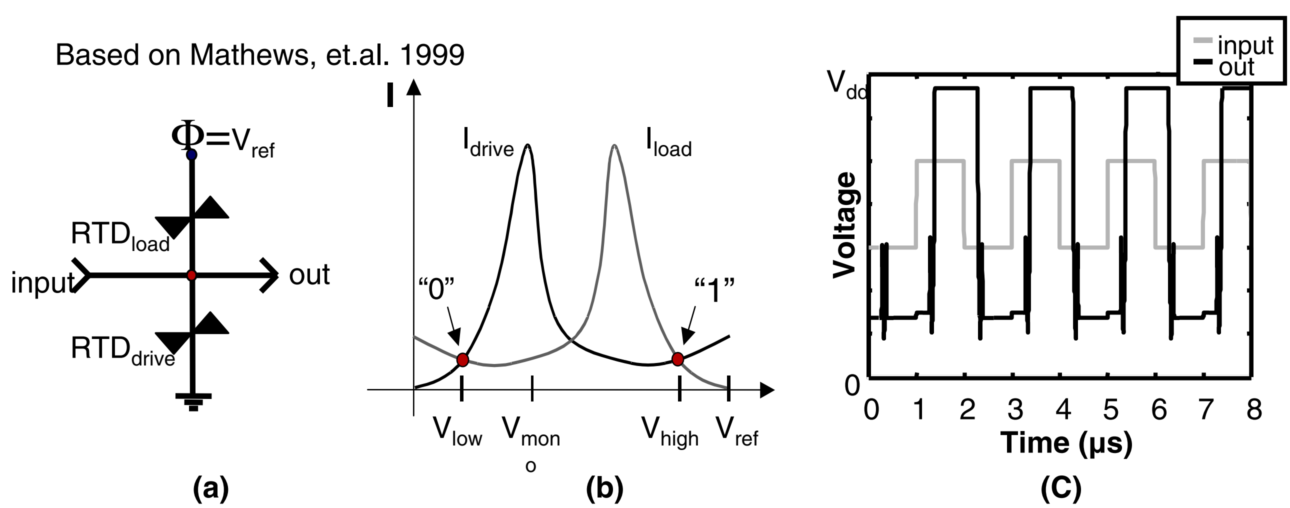

Figure 12.5.3: (a) Simple molecular latch circuit. (b) Load-line diagram. (c) Simulation results showing latching and voltage restoration.

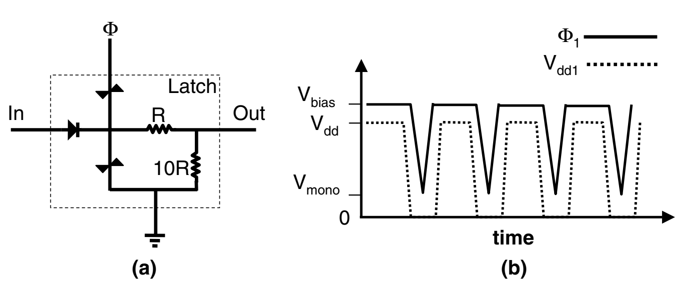

Figure 12.5.4: (a) The complete molecular latch and (b) the clocking methodology.

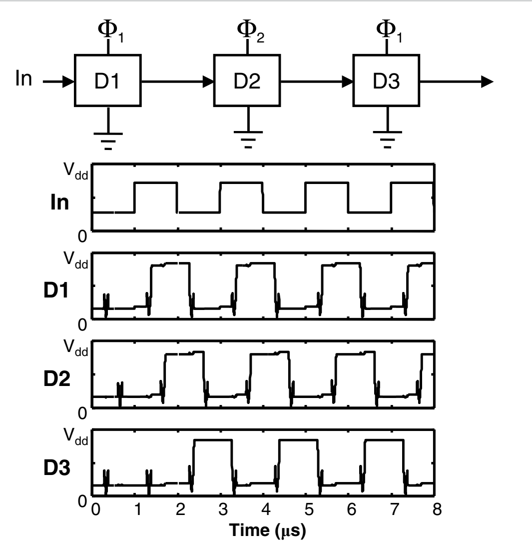

Figure 12.5.5: Simple 3-stage delay circuit using the molecular latch from Figure 12.5.4.

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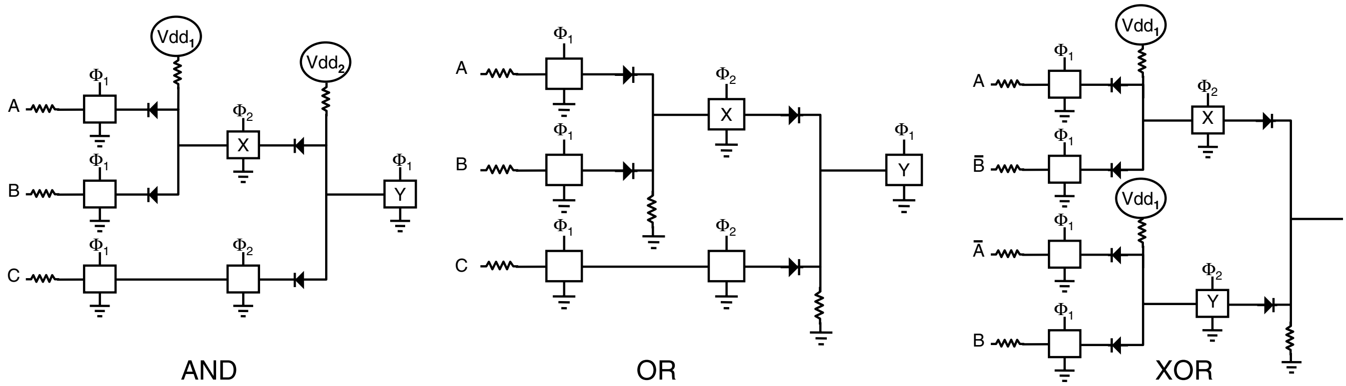

Figure 12.5.6: AND, OR, and XOR circuits using diode-resistor logic and intermediate molecular latches.

