Computational Paradigm for Nanoelectronics: Self Assembled Quantum Dot Cellular Neural Networks *

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Abstract

We review recent work on a unique locally interconnected neuromorphic architecture that can be implemented with chemically self assembled arrays of nanowires acting as circuit nodes. The nanowires have non-monotonic and non-linear current voltage characteristics (e.g. a negative differential resistance) that provide the functionality needed for complex circuit functions. This self assembled network, which, in its most rudimentary form, can be "grown" in a beaker using traditional electrochemistry, is theoretically capable of performing Boolean logic operations, complex image processing tasks, and associative memory functions. Here, we describe relevant features of the network and present some recent results. In particular, we present experimental results showing that the transport non-linearities of the nanowires can be modulated with infrared radiation. This makes it naturally amenable to optical inputs which eliminates the need for electrical input connections and contacts, thereby allowing extremely high device density. It also makes it eminently suitable for image processing tasks. Furthermore, critical features of the systems are synergistic with biologically inspired networks. We have experimentally extracted the relevant circuit parameters using a prototype self assembled structure, and used them in simulations to demonstrate functionality of the network for several applications.

1 Introduction

The workhorse of modern electronic circuits has been the celebrated "transistor" discovered by Bardeen, Brattain and Shockley more than half a century ago. The transistor is an amazing entity. It continues to perform well with surprising tenacity even as its dimensions are shrunk to sizes where the active device region consists of only a few tens of atoms [1]. However making nanoelectronic circuits with scaled down conventional transistors, with feature sizes smaller than 10 nm, is usually beset with numerous difficulties. Among them are irreproducibility of devices, astronomical fabrication costs, complex scaling issues and a daunting interconnection problem. There are no obvious ways to avoid these roadblocks, except to strive against them with mounting costs. Although it is unlikely that semiconductor based electronics will ever witness a radical paradigm shift and discard the time-tested transistor based circuits to embrace something new and unproven – no matter how challenging transistor based circuits get to be – it is possible that non-traditional "transistorless" circuits may find some small, niche applications where they outperform conventional transistor-based circuits. In this respect, they may have a role similar to organic electronics which competes favorably with semiconductor electronics in some niche areas such as light emitting diodes (LEDs) [2, 3]. In fact, some industries predict that organic LEDs (which are considerably cheaper than semiconductor LEDs) may capture 50% of the display market by 2025. Similarly, transistorless circuit architectures may some day carve out a niche area in nanoelectronics.

Non-traditional (transistorless) circuits may flourish where device attributes such as "gain" and "isolation between input and output" (which are typically found only in 3-terminal devices) are not critical. Boolean logic circuits, for example, require these attributes and therefore are best implemented with conventional transistors. The five inviolable requirements for classical Boolean logic devices are listed in ref. [4] and are reiterated here with some elucidation: (i) The output signal of the logic device must be a *deterministic* prescribed (Boolean logic) function of the inputs; (ii) signals must be quantized to two binary levels with sufficiently large separation between the levels.

This requires a non-linear device characteristic; (iii) signal restoration at logic nodes is necessary for fault tolerance, which requires that the logic device have a voltage gain (if voltage is used to encode logic levels); (iv) device unidirectionality is required which ensures that logic signal flows unidirectionally from the input to the output and not the other way around. This will guarantee that the output will be a single-valued function of the input(s). The unidirectionality needs to be innate and not forced by extraneous influences such as the input itself. If we rely on the input to ensure unidirectionality, then we cannot change the input till the final output signal has been produced at the output terminal. In this case, the circuit is not a pipelined architecture and therefore is very slow. Unidirectionality can be imposed either in space, or in time [5]. For spatial unidirectionality, there must be "isolation" between the input and output of the logic device. For temporal unidirectionality, clocking of successive devices will be required (e.g. in charge coupled device arrays and most bucket-brigade circuits); and finally (v) the output of one stage will be able to drive the inputs of many succeeding stages, i.e. the fan-out should be significantly larger than unity. This requires some current gain in the logic device. Taken together with requirement (iii), this implies that the logic device must have an overall power gain[1].

A transistor can meet all of these requirements and therefore has been the workhorse for Boolean logic circuits (particularly combinational circuits, as opposed to sequential circuits)[2]. Transistorless circuits, on the other hand, may have preferred applications in massively parallel but non-logic paradigms such as neural networks [7], cellular automata [8] and cellular neural networks (CNN) [9]. They may be particularly useful for collective

[1]It is sometimes not realized that typically both voltage and current gains are required. A step-up transformer has a voltage gain at the expense of current attenuation, and is therefore not an acceptable logic device.

[2]The only well known exception to this is Rapid Single Flux Quantum Logic (RSFQL) [6] operating at nearly 100 GHz clock speed. It uses Josephson junctions rather than transistors. In spite of its speed, it does not contend well against conventional semiconductor transistor based circuits because there is no room temperature superconductor (as yet) and the materials technology for superconductors is far behind that of semiconductors

computational models where the computational activity is elicited from the co-operative functioning of many devices acting in unison. Such circuits are inherently fault tolerant; they tolerate stochastic variations across the chip. This is extremely attractive for nanoelectronic circuits since ultrasmall devices often show significant variability in their characteristics. For example, a 20 nm gate-length nanotransistor may have only 20 or so dopants in the channel (even for very heavy doping), so that a variation of even a single dopant atom results in a significant threshold shift[3]. It is very difficult (and therefore very costly) to ensure acceptable device reproducibility on a chip containing nanodevices. Therefore, the intelligent alternative is to adopt circuit paradigms that do not require strict device reproducibility, namely collective computational models. In collective computation, no single device is critical for circuit operation. It is the collective activity that matters. Therefore, the circuits can work even if a significant fraction of the devices fail. Finally, device gain and isolation are not mandatory for non-logic circuits, so that it is possible to do away with the transistor and replace it with something much simpler and less expensive, for example, a 2-terminal nanowire.

There are quite a few proposals around for transistorless circuit paradigms in nanoelectronics. A small fraction of them may be promising. We have found that certain important criteria must be satisfied by "good" transistorless nanoelectronic circuits paradigms, and those that remain faithful to these criteria are likely to succeed. These criteria are listed below:

1. The circuit should be based on collective computational models in order to tolerate device-to-device variations which are unavoidable with present or near-term technology.

2. The circuit paradigm should not require gain and/or isolation in individual devices. These requirements are difficult to meet without transistors. Therefore, Boolean

[3]It is possible to use an undoped channel and rely on carriers from the source and drain contacts to turn the device on, but then a single *unintentional* dopant atom in the channel can still cause a significant threshold shift

logic paradigms (particularly combinational circuits) are not appropriate.

3. It is advisable to adopt locally interconnected architectures rather than random wired architectures. The former has only short range connections and each device is connected to a few near neighbors. This avoids two problems. First, it ameliorates the routing problem because remote devices on a chip do not have to communicate by meandering/multilevel interconnect lines, and second, no device needs to drive many others. The current drive capability of all nanodevices is low since they contain few charge carriers. This limits the fan out severely. One device therefore cannot drive very many successive stages and consequently, non-local architectures such as random wired neural networks (as opposed to cellular neural networks), are not suitable.

4. The fabrication/synthesis route should be simple and relatively inexpensive. Paradigms that are inspired by high-throughput and inexpensive technologies for nanosynthesis, such as "self-assembly", are more promising than those requiring exorbitantly expensive complicated fine-line lithography for pattern delineation.

1.1 A Nanoelectronic Neuromorphic Architecture

A number of transistorless circuit ideas have appeared in the literature over the last decade. Chief among them is a cellular neural network idea using nearest-neighbor linked metallic nanoparticles interfaced with non-ohmic nanowires [10, 11, 12]. A quantum dot based cellular neural network idea [13] was inspired by [10, 11, 12]. These ideas are predicated on collective computational models (although they could be configured to perform some logic operations, if needed) [11]. The appeal of [10, 11, 12] is that it is based on a very simple system that can synthesized with simple chemical self assembly methods. The architecture is also extremely powerful and can perform associative memory functions and specific image processing tasks such as edge detection-enhancement and vertical/horizontal line detection with ultrafast speed [14, 15]. Overall, it is a revolutionary new idea that epitomizes a true "bottom up" approach in designing circuits

where a very simple system is first self-assembled and then its circuit functionalities are elicited.

In its simplest form, the architecture proposed in [10, 11, 12] consists of a two-dimensional array of vertically standing nanowires, each capped with a metallic contact. The nanowire conduction characteristic exhibits a non-monotonic non-linearity, such as a negative differential resistance (NDR). The metallic caps are connected to their nearest neighbors by linear resistive and capacitive links. The circuit diagram for this system is shown in Fig. 1. Here q_{ij} denotes the metallic caps which are nanodots themselves, J_{ij} represent the inter-dot currents carried by the inter-dot resistive/capacitive connections, and J_{si} is the vertical current through the nanowire (metallic dot to the substrate) which exhibits an NDR characteristic. Some of the metallic dots can also be connected to the outside world via lithographically defined contacts for external current biasing which is denoted by I_{ij} in Fig. 1.

In the past, this architecture was studied theoretically in a number of publications [10], [11], [12] that illustrated its applications in various computational and signal processing tasks. More recently, a simple prototype was chemically self assembled and circuit parameters were experimentally measured [15]. We then used these "measured parameters" to simulate the circuit operation. Also, for the first time, these simulations were performed at the circuit-system level for large dynamical systems. We showed that the quantum dot network can perform two specific operations that are useful image processing tasks. They are: (i) edge detection enhancement and (ii) horizontal/vertical line detection. In addition, it was shown that the same circuit-system level model with NDR characteristic forms a reaction-diffusion dynamics and allows generation and propagation of trigger waves across the device area [16].

The outline of the paper is as follows. Section 2 describes self-assembly of the quantum dot network that conforms to the system in Fig. 1. This section also presents measured circuit parameters, namely interdot resistance, interdot and dot-to-substrate capacitance and NDR characteristic of the nanowire. We also present data showing that the NDR characteristic of the nanowire can be *modulated* externally, by means of

an infrared excitation. The extraction of circuit model parameters and the notion of "superdot" comprising a suitable cluster of the metallic dots (in the context of optical image processing), is presented. In Section 3, the quantum dot nanostructure is introduced at circuit-system level. In Section 4, several system capabilities are demonstrated via simulated results, based on the extracted parameters. Section 5 concludes the paper.

2 Self Assembly of a 2D Quantum Dot Array

The network in Fig. 1 has two main components: (i) a 2D periodic array of metallic islands (nanodots), each interfaced with a nanowire resistor displaying a negative differential resistance, and (ii) a resistive/capacitive coupling between nearest neighbor islands. This network can be self assembled electrochemically. We start with a n^+ silicon substrate and evaporate a thin layer (20 nm) of titanium on it. Next, we evaporate 1-2 μm thick layer of aluminum in several steps. The titanium layer improves the adhesion of aluminum to the silicon substrate. Then, we anodize the aluminum in 15% sulfuric or 3% oxalic acid at room temperature to convert it to a porous alumina film containing a *nearly periodic* regimented array of nanopores. An AFM micrograph of such pores can be seen in [17]. The pore diameter is 8 nm if the anodization is carried out in sulfuric acid and 50 nm if the anodization is carried out in oxalic acid. Lower pore diameters, down to 3 nm, can be obtained by carrying out the anodization at 270 K. When all of the aluminum is anodized into a porous alumina layer, the anodizing current begins to change rapidly, at which point the anodization is terminated. After this, we soak the sample in phosphoric acid to remove the alumina barrier layer that lies between the porous film and the silicon substrate. During this soaking process, a dc current is passed between the silicon substrate and a platinum electrode. When the barrier layer is completely removed, this current increases rapidly and saturates. Next, we sequentially electrodeposit a semiconductor (e.g. CdS or ZnSe) and a metal (e.g Cu) selectively within the pores. CdS is electrodeposited by immersing the alumina film (along with the substrate) in an electrolyte consisting of a non-aqueous solution of dimethylsulfox-

ide comprising 50 mMolar cadmium perchlorate, 10 mMolar lithium perchlorate and 10 mMolar sulphur powder. In the case of ZnSe deposition, cadmium perchlorate is replaced by zinc perchlorate and sulfur powder with selenium powder. Electrodeposition is carried out at 100°C with an ac signal of 20 V at 250 Hz. During the negative half of the ac cycle, the Cd^{++} or Zn^{++} ions in the solution are reduced to zero-valent Cd or Zn and are deposited selectively in the pores which offer the least impedance path for the electric current to flow. During the positive cycle, the zero-valent metals are not re-oxidized into the ions since alumina is a valve metal oxide. The high temperature of the solution then allows Cd or Zn in the pores to react with S or Se in the solution to produce CdS or ZnSe. The deposition is made to last a few minutes so that the length of the CdS or ZnSe nanowires within the pores is a few microns. These nanowires are cylindrical with a nominal length of a few microns and a nominal diameter of either 10 nm or 50 nm. To deposit Cu, we soak the structure in an aqueous solution of $CuSO_4$ and carry out the electrodeposition at 20 V rms, 250 Hz. The Cu^{++} ion is converted to zero-valent Cu and is electrodeposited selectively within the pores on top of CdS or ZnSe. The resulting structure is shown in Fig. 2.

The Cu dots are then partially exposed by controlled etching of the alumina in phosphoric acid. The steps are shown in Fig. 2. Neighboring dots are electrically isolated by the intervening alumina layer which is a semi-insulator. In the case of sulfuric acid anodization, the thickness of the isolation layer is about 10 nm and in the case of oxalic acid anodization, the thickness is about 20 nm. Once complete, the structure is a self-assembled experimental realization of the system shown in Fig. 1.

2.1 Measurements of Circuit Parameters

Interdot resistance : In the past, the resistance of the alumina layer separating neighboring pores was measured by delineating two contact pads, spaced 100 μm apart, on the surface of a 1 μm thick porous alumina film produced by anodization of aluminum in sulfuric acid. The pores were filled with a semiconductor. The resistance measured

between the pads, which were 1 mm wide, was about 80 MΩ [18]. In this experiment, the effective width of the alumina between the pads was approximately one-half of the distance between the pads, namely 50 μm. Therefore, the resistivity of the alumina is 80 MΩ×1mm×1μm/50μm = 160 KΩ-cm. The conduction through the alumina was found to be ohmic [18] (probably conduction takes place through impurity bands in the alumina), so that the alumina resistivity can be assumed to be a constant. Therefore, when the alumina layer thickness between neighboring pores is 10 nm and the pore diameter is 10 nm (sulfuric acid anodization), the inter-dot resistance will be of the order of 1.6 GΩ. If the anodization is carried out in oxalic acid instead of sulfuric acid, the alumina barrier between neighboring pores is 20 nm wide and the pore diameter is 50 nm. In that case, the interdot resistance is 640 MΩ. These parameters can change somewhat depending on the anodization conditions.

NDR characteristics : When metals or semiconductors are electrodeposited within pores, they tend to break up in small crystalline grains. Each grain is a few nm in diameter [19]. Neighboring grains are separated by amorphous regions which are also a few nm thick. The amorphous regions are much more resistive than the crystalline regions, so that an amorphous-crystalline-amorphous combination acts like an effective double barrier resonant tunneling diode. A series of these diodes will result in a "pass-bands" of energies separated by "stop-bands". As a result, we expect the current voltage characteristic to exhibit a weak negative differential resistance. We have observed a weak negative differential resistance (with peak-to-valley ratio of 1.5:1 at room temperature) in vertical conduction through CdS nanowires electrodeposited within 50-nm pores produced by anodization in oxalic acid. Two current voltage characteristics showing negative differential resistance were shown in ref. [15]. They were measured at room temperature. In the first sample, we probed about 100 nanowires in parallel [20]. The peak-to-valley ratio was 1.5:1 and the peak current was 1.5 nA for the 100-wire ensemble. Therefore, the peak current per wire is 15 pA. In the second sample, about 10 nanowires were probed in parallel and *multiple* negative differential resistance peaks

were found at room temperature. Multiple NDR peaks can be found when several pass bands and stop bands are spaced closely in energy.

Dot capacitances : In the past, we have observed room-temperature single electron charging (Coulomb blockade) effects in these systems [20]. From those measurements, we estimate that the dot-to-substrate capacitance (i.e. the capacitance of the CdS nanowire) is of the order of 0.5 aF in sulfuric acid anodized templates. This value agrees nicely with what we would have calculated if we viewed the CdS wire as a parallel plate capacitor. The wire has the shape of a cylinder of diameter 10 nm and height 1 μm. The relative dielectric constant of bulk CdS is 5.4 [21]. Therefore, the "parallel-plate" capacitance of the mesa is 0.1 aF which is close to what we measure. We have also observed Coulomb blockade in the oxalic acid anodized structures. There, the Coulomb blockade picture is somewhat more complicated since the semiconductor within the pores breaks up into small crystalline grains separated by amorphous regions. Consequently, they form a series of capacitors (or tunnel junctions). In fact, we have observed Coulomb staircase in oxalic acid anodized systems [20] because they comprise multiple capacitors in series. Based on the observed Coulomb staircase, we found that the effective dot-to-substrate capacitance in oxalic acid anodized templates is actually 5 times *smaller* than what it is in sulfuric acid anodized templates, even though the pore area in oxlic anodized templates is 25 times larger. This apparently anomalous result can be explained by the fact that in the case of oxalic acid templates, the dot-to-substrate capacitance is a *series* combination of many capacitors which reduces the effective capacitance between the dot and the substrate.

2.2 The "Superdot" Representation of Dot Clusters

A solution for interfacing of large nanostructure arrays with external input can be the *programming of dot states with light*, which will represent the input information. This is an extremely attractive approach and very advantageous since making *electrical* input connections to each dot in a densely packed array is a formidable task. In Fig. 3(c),

we show the measured NDR characteristics of ~ 100 nanowires in parallel, in the dark and under near-infrared illumination. The measurement results show that it is indeed possible to change the NDR characteristic of the nanowires (both the peak position and the peak height), when they are exposed to near-infrared light (wavelength 2-6 μm). This significant result promises a very effective interfacing method which is especially suitable for image processing tasks. In accordance with this possibility, we present the superdot concept for coupled dot clusters. The pitch of the 2D quantum dot array (dot diameter plus inter-dot separation) in oxalic acid anodized templates is about 70-80 nm. Since the edge of a pixel in an image should be perhaps approximately the wavelength of light (we will assume light of wavelength 5500 nm for near infrared excitation), therefore the edge of a pixel is $5500/70 \approx 80$ times larger than the pitch of the quantum dot array. Therefore, approximately $80 \times 80 = 6400$ dots will represent a pixel. Thus, we assume that a dot cluster of about 6400 dots can be approximated as an equivalent "superdot" which will act as a single node interacting with the light wave. Hence, its dynamical behavior can be modeled by treating it as a single dot if the circuit parameter values are modified accordingly. This means that the superdot-to-substrate capacitance is 6400 times the single dot capacitance, i.e. $6400 \times 0.5 = 3.2$ fF, the inter-superdot resistance is 80 times smaller than the inter-dot resistance (since the edge of the superdot contains 80 single dots), i.e. $640/80 = 8$ MΩ, and the peak current for a superdot is 6400×15 pA≈ 0.1 μA. The peak-to-valley ratio can be improved by annealing the structures at some optimum temperature to promote uniform grain growth. We consider a possible ratio of at least 10:1. One parameter that we have not been able to measure is the inter-dot capacitance. Therefore, we will estimate it assuming a parallel plate geometry for simplicity. The relative dielectric constant of alumina is roughly 4; therefore, the interdot capacitance is 5 aF if the anodization is carried out in oxalic acid. Here, we have assumed that the quantum dot is 50 nm wide for oxalic acid anodization and it is 50 nm thick (to electrodeposit 50 nm of metals within the pores takes only a few seconds of electrodeposition). Based on this, the inter-*superdot* capacitance is 4 fF for oxalic acid anodization. The circuit parameters for the superdot are given in Table I.

We also use these "order of magnitude" estimates in the numerical simulations.

3 Quantum Dot Network

The self-assembled structure of the quantum dot array constitutes a parallel processing network. Consider the 2D array structure of quantum dots shown in Fig. 1. The back of the substrate is grounded. A charge balance equation (or Kirchoff's current law equation) for each single dot can be written as

$$C_{si}\dot{v}_i = I_{Bi}(t) - J_{si}(v_i) + \sum_{j \neq i} J_{ij}(v_i - v_j) \tag{1}$$

where $I_{Bi}(t)$ is the bias current for dot i, v_i is the dot voltage and $\dot{v}_i$ denotes its time derivative. C_{si} is the dot-to-substrate capacitance and J_{ij} is the current sinking into the i-th dot from neighboring dots which may be a linear or non-linear function of dot potentials. The vertical current J_{si} through the semiconductor wire underlying the dot is modeled by a piecewise linear approximation as shown in Fig. 4 which replicates NDR characteristic. In this model v_P and I_P are the peak voltage and current, v_V and I_V are the valley voltage and current, and G_{PR} models the second positive conductance region respectively. The NDR region resistance is defined through the values of v_P, I_P, v_V and I_V. In addition, a linear capacitive-resistive coupling model for J_{ij} is employed between neighboring dots.

Due to the linear coupling model, equation (1) also holds for a cluster of dots (superdot) under same biasing conditions and initial states [15]. Therefore, a cluster of m dots can also be approximated as a single node with a re-scaling of the dot circuit model parameters as

$$mC_{si} \rightarrow C_{si};\ mI_{Bi}(t) \rightarrow I_{Bi}(t);\ mJ_{si}(v_i) \rightarrow J_{si}(v_i) \tag{2}$$

which gives the circuit representation of a superdot. Since the coupling is linear, the summation of external coupling can be expressed by assigning equivalent coupling conductances between the superdots. Therefore, (1) can also be used for the superdot dynamic state with scaled circuit parameters.

A parallel network which exhibits 4-neighborhood coupling with rectangular mesh connectivity is considered as a coupled superdot array. The related circuit models, the superdot pair coupling and the corresponding network are also shown in Fig. 4. If one applies this model to a 2D array then the current equation for each of them can be expressed as

$$\begin{aligned}&(C_{si} + \sum_{j \neq i} C_{ij})\dot{v}_i = \\ &I_{Bi}(t) - J_{si}(v_i) + \sum_{j \neq i} [G_{ij}(v_j - v_i) + C_{ij}\dot{v}_j]\end{aligned} \tag{3}$$

Note that the all the parameters in (3) now refer to the superdot (or dot clusters). The state equation (3) has remarkable similarities with the cell dynamics defined in the CNN theory [22]. However, the quantum dot network model has a more specific CNN structure [16]. The network does not exhibit a separation between state and output variables. Therefore, the state of the system can be considered as the output itself. Furthermore, the differential ($\dot{v}_j$) coupling of the neighboring dot states also affect the individual dot state v_i because of the capacitive coupling element C_{ij}. In fact, (3) can be arranged in matrix form as

$$[\dot{v}]_{k\times 1} = [A]_{k\times k}[v]_{k\times 1} + [C]^{-1}_{k\times k}[I_B(t) - J_s(v)]_{k\times 1} \tag{4}$$

Here, k denotes the number of state variables and $k = N \times M$ for a 2D array of $N \times M$ dots. Equation (4) represents a tightly coupled nonlinear system which exhibits cooperative behavior [23]. In general, the system matrices $[A]$ and $[C]^{-1}$ may have significant non-diagonal entries mainly due to contributions of C_{ij}, resulting in non-local dependency among the state variables. This implies that in general, the system of equations in (4) has to be solved.

Using the NDR model parameters in Fig. 4, the steady-state analysis of (3) gives trivial equilibrium voltages for the dot states as

$$V_{Low} = \frac{I_B}{G_D}; \quad V_{High} = \frac{I_B - I_V}{G_{PR}} + v_V \tag{5}$$

The superdots change state cooperatively, in the direction of neighbor superdot states as to either low or high states. The expressions given for V_{Low} or V_{High} hold for the

dot states within the regions where all the dots have the same final states. However, for arbitrary initial conditions and network configuration, these equilibrium states do not represent the only possible steady-states. Note also that the bias current applied to superdots is always necessary for the desired bistable system operation.

An important result that follows from the network model in (4) is a spatiotemporal phenomenon, namely a state wave propagation across the nanoarray [16]. The NDR current response and constant bias current results in a reaction-diffusion dynamics in (4). As a consequence, the network is capable of propagating trigger waves as state changes of superdots in the array. The stationary or propagating patterns in reaction-diffusion systems are well known. Such systems are frequently identified in modeling of spatiotemporal phenomena in biological and chemical processes (for a related survey, see [25] for example). In accordance, it is remarkable that the self assembled network dynamics coincide with the activator part of Fitzhugh-Nagumo model for neuroelectric activity [26]. The realization of a complete Fitzhugh-Nagumo model on the other hand, requires an additional network layer with modified functionality and a 2-layer coupling.

Since the state and the output is the same for the network, one natural way to make use of the system dynamics is via the programming of the initial state conditions. The significance of NDR characteristics changing with light interaction becomes more clear at this stage. The dot voltage steady states are governed by the characteristics of the NDR curve. This curve can be shifted vertically in the phase space by adjusting the coupling contributions and bias current [16]. In addition, it is also possible to change stable states in the phase space, if one can directly modify the NDR response. Therefore in principle, the initial superdot states of the network can be programmed via light interaction, which modifies this response as the measurements indicate. This approach may solve an important part of the connectivity issue in interfacing, which is common to all parallel processing networks. Furthermore, it is extremely convenient for image processing tasks.

4 Simulations

In parallel with the superdot concept and its initial state programming, we demonstrate the capabilities of quantum dot network via circuit-system level simulations. These capabilities include: (i) edge-detection,(ii) line detection and (iii) wave propagation. A dedicated simulator is used in the simulation of 2D superdot arrays. The measured and estimated model parameters in Table I are considered for each superdot in these simulations. For different examples, we slightly modify the interdot resistances from the value given in Table I (8 MΩ) in order to obtain various responses. These modifications are small and the final values remain within the same order of magnitude as those experimentally measured.

In the examples below, we assume the capacitances and NDR response as identical for each superdot in the array. The values of substrate and coupling capacitances are $C_{si} = 3.2$ fF and $C_{ij} = 4$ fF (see Table I). The NDR is represented by a piecewise linear model (see Fig. 4) and the parameters used are $v_P = 0.7$ V, $v_V = 0.78$ V, $I_P = 0.1$ μA, $I_V = 0.01$ μA and $G_{PR} = G_D = 1.43 \times 10^{-7}$ S based on measured data reported in [15]. The dynamical system defined by (4) is then simulated for different network configurations, namely for different coupling strength and bias current. For image processing examples, a number of gray scale input images are provided to the system. The intensity information of each pixel is mapped as the initial superdot voltage, hence each superdot represents a pixel. The range of the pixel states in terms of voltage is scaled according to V_{Low} and V_{High} values, as obtained from (5) by substituting the related parameter values.

(i) Edge detection-enhancement. This example demonstrates an image processing capability of the self assembled network as a result of cooperative response from superdots. The coupling conductances are $G_{ij} = 0.125$ μS (8 MΩ), which are assumed identical for all superdots.

The pixel intensities of a *150* $\times$ *150* pixel ($k = 22500$) gray scale input image are mapped to the network voltage states. The common bias current value used is $I_B = 60$

nA. Using this value in (5), the corresponding equilibrium states become $V_{Low} = 0.42$ V and $V_{High} = 1.13$ V. The image mapping is performed as linear from 0 V (black) to $V_{High} = 1.13$ V (white) and represents the initial condition of the superdot voltage states at $t = 0$ as shown in Fig. 5. The system is left to evolve for a total duration of 100 nanoseconds and the dynamical change in the dot voltages are examined. The top-right image Fig. 5 shows the system state at $t = 20$ nsec, and bottom-left is the superdot voltage state when $t = 50$ nsec. It is observed that the initial state rapidly evolves to the final state. When the top-left image in Fig. 5 is input to the dot array, the steady state system output is reached around $t = 100$ nsec for these parameters, and the result is very similar to an edge detection-enhancement process, in accordance with the cooperative dynamics. As can be expected, the steady-state result is essentially *independent* of the input image size.

(ii) Horizontal-vertical line detection. The second example we demonstrate is the horizontal and vertical line detection capability. This feature can be extracted if one assumes a relative difference between the horizontal and vertical coupling conductance (G_{ij}) values, i.e. $G_H \neq G_V$ [15]. In practice, this condition can be realized by damaging horizontal or vertical rows of alumina between the dots with a scanning ion beam. For the purpose of simulation, another 150×150 pixel image is chosen. In the horizontal detection phase, the conductance values are arranged as $G_H/G_V \approx 20$ where $G_H = 0.1$ μS (10 MΩ). Therefore the coupling in the horizontal direction is stronger. For a vertical line detection, the relation is simply reversed and one has $G_V/G_H \approx 20$ with $G_V = 0.1$ μS. Hence, the vertical coupling is enhanced. Identical input images are introduced to these two different system configurations as the initial superdot states. The capacitance values and NDR model parameters are kept the same as in Table I. The common bias current used is $I_B = 50$ nA. The corresponding equilibrium states of the system then become $V_{Low} = 0.35$ V and $V_{High} = 1.06$ V. The input image intensity is again linearly mapped to the system initial states within this voltage range. The snapshots from the system dynamics are presented for both horizontal and vertical configurations in Fig. 6. The results show that if the coupling conductance is improved

in the horizontal direction, the system performs a horizontal line detection task. A parallel argument holds for the vertical line detection. Note that for this particular input image, the horizontal detection result is more distinctive due to the image features. In addition, the network preserves the main edge enhancement characteristic along with line detection.

(iii) Wave propagation. If configured as an excitable media, the same network is capable of propagating trigger waves of state changes. A state of excitable media can be obtained for a bias current level which is close to the peak current of the NDR response. This choice relocates the superdot low equilibrium states closer to saddle node transition in the phase space [16]. Furthermore, the coupling of the superdots is enhanced to allow triggering propagations. In the excitable configuration, the superdot states still remain low, but they are capable of changing state with a local and temporary excitation. Once started, the state changes across the network continue even if the source of excitation is removed, as a triggering wave of high state transitions. For this example, a 4-neighborhood array with size 50×50 is simulated. The bias current is $I_B = 90$ nA, which is close to the peak current and the all coupling conductances are adjusted to $G = 0.5$ μS. Other parameter values remain the same. Then two superdot nodes in upper and lower edges are temporarily forced to change state using an excitation current pulse of 0.1 μA. Figure 7 shows the corresponding response from the start of voltage state changes as propagating high states in time, again visualized as pixel intensities. These changes are from $V_{Low} = 0.63\ V$ to $V_{High} = 1.34\ V$. This result indicates that within the range of measured parameters, it is indeed possible to obtain wave propagation across the nanoarray surface.

5 Conclusions

The circuit-system level simulation results which employ measured parameter values indicate significance of the proposed nanostructure array as a parallel processing media. It was shown that the network model constitutes a specific cellular neural network.

Considering the concept of light wave interaction with superdots and related initial state programming, we demonstrated that the quantum dot network performs a number of important processing tasks. The applications depend on configurations of the coupling strength and the superdot biasing conditions. The basic configuration of the network model allows an edge detection-enhancement capability. This behavior can be modified to a line detection response, if one enhances the strength of superdot coupling in favor of a spatial direction, for example as modification of vertical or horizontal coupling strength. This may be achieved in practice by damaging the alumina along specific rows with a scanning ion beam to increase/decrease the resistance along those rows. The same network can also be brought to an excitable media state where it can propagate trigger waves, using enhanced current biasing and coupling. This result is related to the reaction-diffusion dynamical form present within the state equations. The measured NDR response of the nanowire clusters and the bias current play the key role in establishing this particular characteristic by providing bistable and excitable voltage states of the superdots.

Finally related to the spatiotemporal capability, the resemblance of the quantum dot network model to Fitzhugh-Nagumo neuron model is intriguing. The current network structure exhibits a part of the neurobiological model and further study is required for nanoscale architectures that can implement complete neuron models. However, the results are promising. Novel nanoscale architectures can be available in the near future, which mimic neurobiological systems with unprecedented capacity.

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switching in self assembled nanowires", *Appl. Phys. Lett.*, vol. 79, no. 26, pp. 4423-4425, 2001.

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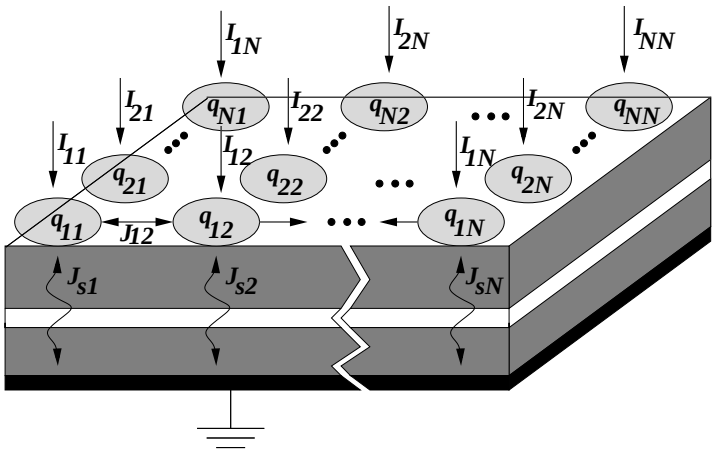
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I_{2N}
I_{NN}
I_{21}
I_{22}
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I_{11}
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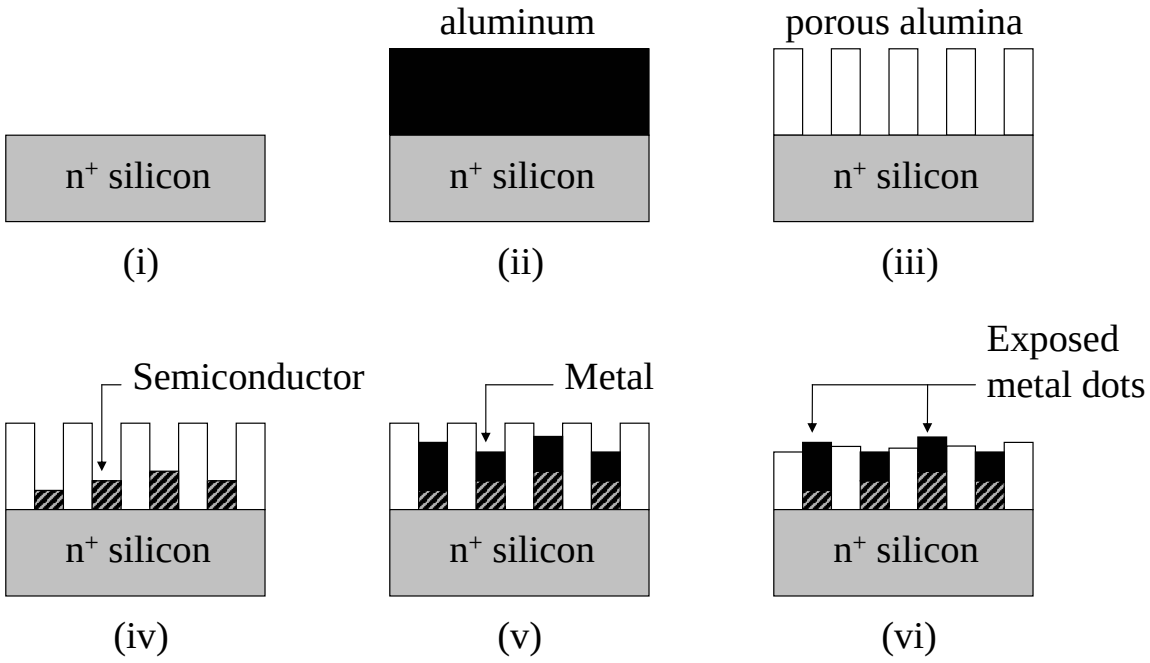

aluminum
porous alumina
n+ silicon
n+ silicon
n+ silicon
(i)
(ii)
(iii)
Semiconductor
Metal
Exposed
metal dots
n+ silicon
n+ silicon
n+ silicon
(iv)
(v)
(vi)

Figure 2:

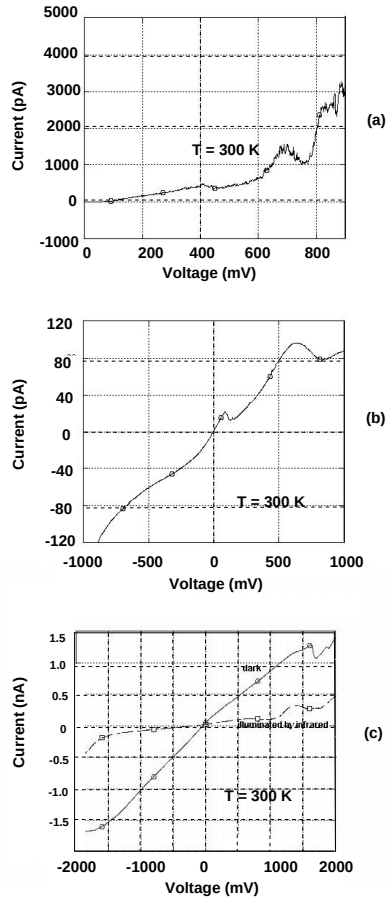

5000
4000
3000
2000
1000
0
-1000
Current (pA)
T = 300 K
0
200
400
600
800
Voltage (mV)
(a)
120
80
40
0
-40
-80
-120
Current (pA)
T = 300 K
-1000
-500
0
500
1000
Voltage (mV)
(b)
1.5
1.0
0.5
0
-0.5
-1.0
-1.5
Current (nA)
dark
illuminated by infrared
T = 300 K
-2000
-1000
0
1000
2000
Voltage (mV)
(c)

Figure 3:

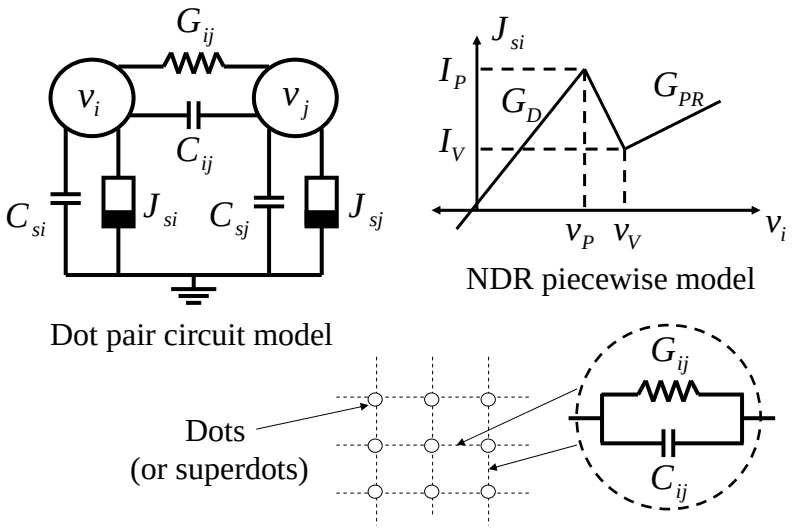
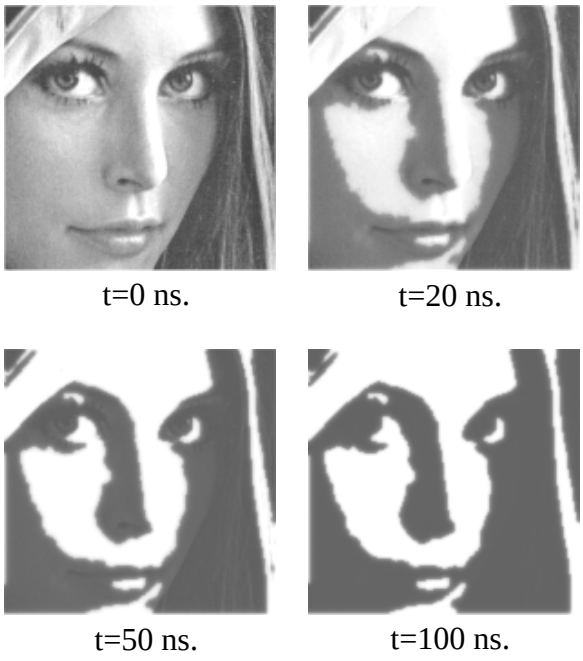

G_{ij}
v_i
v_j
C_{ij}
C_{si}
J_{si}
C_{sj}
J_{sj}
Dot pair circuit model
J_{si}
I_P
G_D
G_{PR}
I_V
v_P
v_V
v_i
NDR piecewise model
Dots
(or superdots)
G_{ij}
C_{ij}
Network Connectivity (Top view)

Figure 4:



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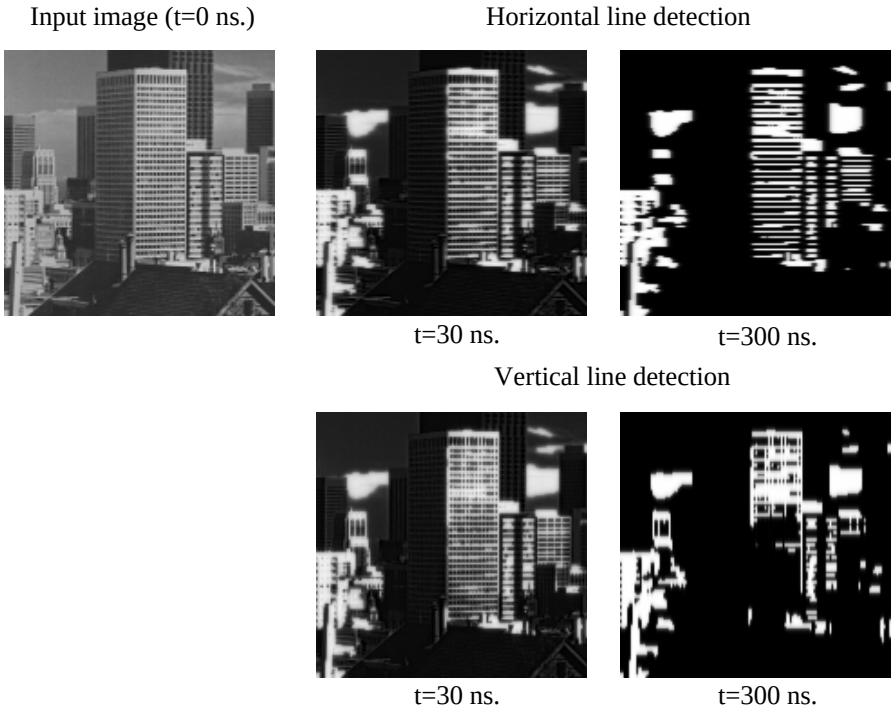
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t=300 ns.
Vertical line detection
t=30 ns.
t=300 ns.

Figure 6:

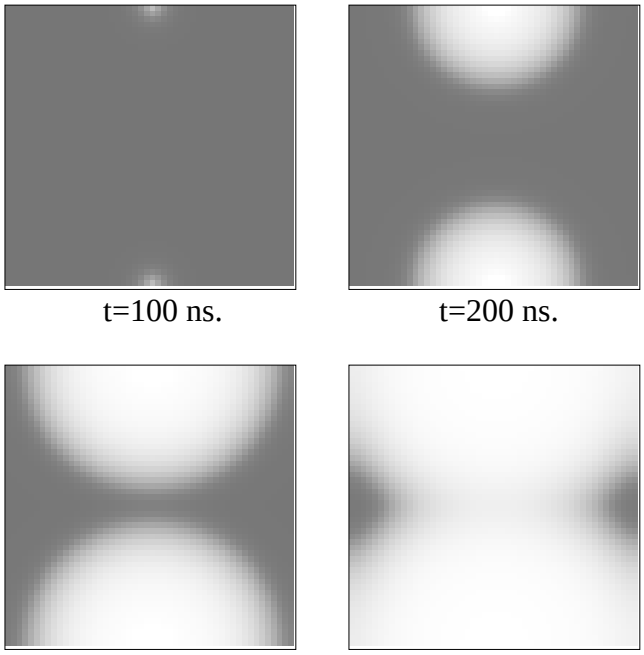

Figure 7:

Table 1:

Circuit parameter	Value
Superdot-to-substrate capacitance	3.2 fF
Inter-superdot capacitance	4 fF
Inter-superdot resistance	8 MΩ
Peak current in a superdot	0.1 μA
Valley current in a superdot	0.01 μA