Collective Computational Activity in Self-Assembled Arrays of Quantum Dots: A Novel Neuromorphic Architecture for Nanoelectronics

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Abstract—**We describe a new class of nanoelectronic circuits which exploits the charging behavior in resistively/capacitively linked arrays of nanometer-sized metallic islands (quantum dots), self-assembled on a resonant tunneling diode, to perform neuromorphic computation. These circuits produce associative memory effects and realize the additive short-term memory (STM) or content addressable memory (CAM) models of neural networks without requiring either large-area/high-power operational amplifiers, or massive interconnectivity between devices. Both these requirements had seriously hindered the application of neural networks in the past. Additionally, the circuits can solve NP-complete optimization problems (such as the traveling salesman problem) using single electron charge dynamics, exhibit rudimentary image-processing capability, and operate at room temperature unlike most quantum devices. Two-dimensional (2D) processors, with a 100 $\times$ 100 pixel capacity, can be fabricated in an area of 10^{-8} cm^2 leading to unprecedented functional density. Possible routes to synthesizing these circuits, employing self-assembly, are also discussed.**

I. Introduction

It is widely believed in the solid state device community that conventional strategies for integrating devices on a chip will be impractical for nanoelectronic devices because of their small size ($\sim$100 nm), low power handling capacity and low gain. Accordingly, many new proposals have been advanced, articulating primarily, visions of future architectures for nanoelectronic circuits [1]–[10]. Some of these proposals, which contemplate building Boolean logic circuits using Coulomb interaction between bistable charge polarizations in quantum dots are flawed [5]. They have overlooked the fact that bistability is a necessary, but not a sufficient condition for implementing Boolean logic circuits. Individual logic devices must also have *isolation* between the input and output (as in a conventional transistor) so that the input drives the output and not the reverse. Coulomb interaction between two identical charge polarizations is *reciprocal* so that it is impossible to distinguish the "input" polarization from the "output" polarization (i.e., there is no isolation between the input and output). In other words, the output influences the input just as much as the input influences the output! Consequently, logic signal cannot propagate *unidirectionally* from the input to the output, or from one stage to the next, leading to total failure [6], [7], [11]. The failure occurs because the input cannot uniquely (and predictably) determine the output. This problem is pathological in many proposed schemes of nanoelectronic architecture. Other proposals, which advocate the use of *cellular automata* architectures with local connectivity [1], also have shortcomings; they offer no mechanism for loading the initial program into the cellular array of quantum devices [11]. As a result, they are also of questionable efficacy. Recently, a scheme, based on the precise phase-locking of single electron tunneling oscillations in capacitively coupled nanojunctions to realize the parametron computing model of von-Neumann and Goto, has been proposed [10]; but it seems to lack fault-tolerance. Finally, some recent proposals for dissipationless computing [4], although quite intriguing, can hardly be considered practical since they have no error-correcting capability. Added to all this is the fact that most of these schemes make unreasonable demands on materials and fabrication technology that cannot be met in the near future.

In [6], [8], and [9], we proposed a radically different scheme for nanoelectronic architecture that suffers from none of the drawbacks just discussed. It has a number of unusual features. First, we realized that any proposal, which requires extreme fabrication tolerance whereby billions of nanoelectronic devices must be fabricated on a wafer with nominally identical behavior, is unrealistic. There will always be *stochasticity* in a large-scale system (e.g., a complex computer or signal-processing chip) and it may be wiser to exploit this stochasticity to realize useful functions rather than strive against it. This is precisely what we do. Second, we insist on *room temperature* operation since cryogenic operation is impractical. Finally, we restrict attention to niche applications where the collective (and sometimes stochastic) activity of a large number of nanostructure devices, working in unison, gives rise to useful computational activity.

The architecture that we implement is inspired by standard models of neural networks. It is massively parallel and inherently fault-tolerant. Moreover, it has significant fabrication tolerance (a 100% variation in the size of an individual device is quite tolerable) and a great deal of noise immunity. The

Manuscript received April 29, 1996. This work was supported in part by the U.S. Army Research Office under Grants DAAH04-95-1-0586 and DAAL03-G-0144, and by the U.S. National Science Foundation under Grant ECS 9 308 814.

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Publisher Item Identifier S 0018-9383(96)07213-9.

relative insensitivity to size variation accrues from the fact that the size determines the capacitance of an individual device. A 100% variation in the size of an individual device will result in a similar variation in the capacitance and this does not affect the performance of the circuit as a whole very much because of the "collective" nature of the computation. Here the collective activities of all devices acting cooperatively matter, rather than the characteristic of a single device. The switching speed of every device is $\sim$1 ps and the power delay product can approach the fundamental thermodynamic limit of $kT\ ln\ 2$ [12] which is less than 10^{-20} Joules. Needless to say, all of these are very desirable features.

This paper is organized as follows. In the next section, we describe a prototype nanoelectronic network fashioned from a 2D array of metallic islands self-assembled on the surface of a double barrier resonant tunneling diode structure. This very simple system produces associative memory effects, realizes the short-term additive memory (STM) or content addressable memory (CAM) model of neural networks, performs 2D image processing and solves NP-complete combinatorial optimization problems. Examples of all this are provided in Section III. In Section IV, we discuss possible techniques for fabricating the network. Finally, in Section V, we provide the conclusions.

II. A Self Assembled Array of Metallic Islands on a Resonant Tunneling Diode: A Neuromorphic Circuit

In the past, many proposals for nanoelectronic circuits advanced ideas that could not be implemented in practice using technology that is either presently available or is likely to be available in the near future. In contrast, the basic array of circuit nodes in our proposed system can be fabricated with relative ease. The primary technology required to produce our circuits is a technology to create a 2D periodic array of nanometer-sized metallic islands (with nearest neighbor interconnections) on a substrate whose current-voltage characteristic has a *nonmonotonic* nonlinearity. Individual islands can have a diameter between 10 and 100 nm depending on the application. Such a structure is shown in Fig. 1(a). The nearest-neighbor interconnects are implemented by organic molecular wires or some other suitable means. This is an established technology and the details of the fabrication will be given in Section IV. The substrate can be a resonant tunneling diode (RTD) whose conduction characteristic has the required nonmonotonic nonlinearity [13]. All our circuits utilize this basic structure. We assume that the molecular wires or other interconnections between the metallic islands can produce a variety of different network mechanisms (e.g., phase-coherent, or ohmic, or nonlinear, or single-electron, or rectifying transport, etc.) which lead to a rich plethora of circuit functions. Some of these possible network mechanisms are depicted in Fig. 1(b)–(d).

Electrically coupled arrays of nanometer scale metallic islands, comparable to that depicted in Fig. 1(a), have been fabricated in the past using self-assembly [14]. There is experimental evidence that one can establish inter-island conductive and capacitive links between the nanometer sized metallic islands with organic molecular wires [14]. Single electron charging effects and nonlinear transport have been demonstrated in these systems at room temperature [15]. Furthermore, self-assembled buckytubes may also realize the interconnects [16], [17]. Additionally, there is experimental evidence that phase-coherent links may prevail between metallic spheres which have been embedded in a porous dielectric matrix [18]. Therefore, a wide variety of transport mechanisms can be realized at present which provides an adequate degree of design flexibility.

The final requirement for realizing the complete system shown in Fig. 1(a) is a suitable scheme for reading and writing data. In the topologies described in Section III, each circuit node must be addressed individually. Present interconnect technology is not capable of providing individual connections at this density, although advances in nanometer scale patterning or self-assembly techniques may provide such capabilities in the near future. In the shorter term, related computational topologies with somewhat reduced functionality can be realized with all input/output ports and program nodes at the periphery of the chip. In that case, all input/output are provided to or retrieved from a few selected nodes at the periphery or edge of the chip. An architecture based on such "edge-driven" paradigm is represented by the general structure proposed in Fig. 1(a). A scheme that can implement logic functions using such a structure has been recently proposed. The interconnect problem is greatly simplified in the "edge-driven" case, since it is necessary to externally access only those islands that communicate with the external world. Of course, conventional bonding technology will not be adequate to access these islands because it does not possess the resolution needed to address individual quantum dots. In fact, typical bonding pads will probably consume the area occupied by about 10 000 islands. Therefore, we need a contact technology capable of virtually atomic resolution. The obvious choice is a scanning tunneling microscope (STM) tip which has been shown to be capable of such resolution [19]. They can also read the voltages on the island. STM tips were proposed for input/output data lines in [6] which visualized an array of tips micromachined into a wafer and permanently attached to input/output ports for data reading and writing. Attaching an STM tip to an individual dot may be accomplished using fine line direct-write lithography followed by metallization. This is a difficult step and significant developmental work should precede implementation. Recently, the operation of an integrated 100 micron size STM fabricated on a chip by standard lithography was demonstrated by Hitachi Research Laboratories [20] which is an important advancement in this direction. It should be noted that the size of the dots in our proposed structures is typically 10 nm so that once the STM tips are correctly attached, thermal drift or vibration is no longer a problem. Additionally, one should note that direct write lithography is being used only for making contacts to the chip and not for delineating the quantum dots or the interconnects between them. Therefore, the throughput will not be unacceptably slow even though direct write lithography is used. Recent work on arrays of scanning tunneling microscope tips, in which each tip has been individually addressed [21] lends further credence to this idea.

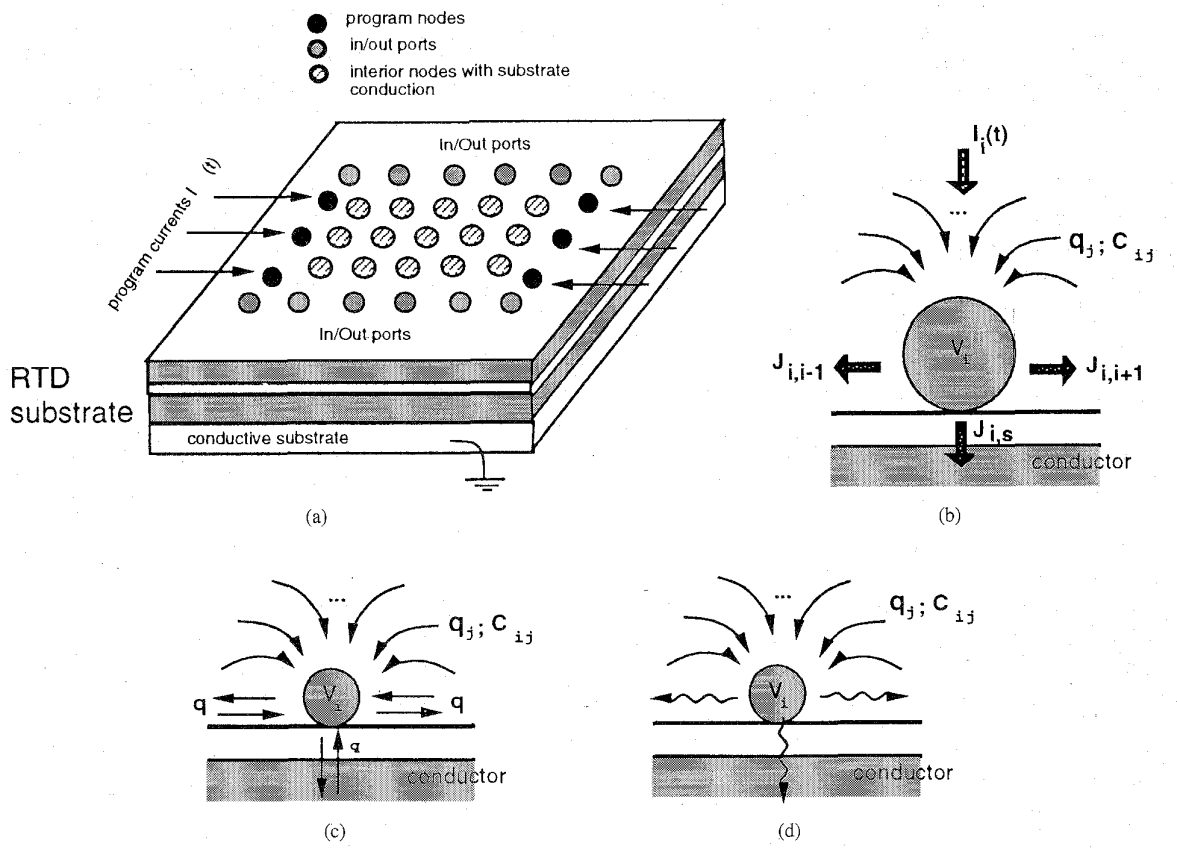


Fig. 1. A generic array of nanometer-sized metallic islands deposited on a resonant tunneling diode (RTD). It is assumed that all islands have direct conductive/capacitive links to their nearest neighbors established, for example, via organic molecular wires. These wires are not shown for the sake of clarity. A subset of the islands serve as program nodes that are driven by external current sources. Another subset of islands serve as input/output ports, and the remaining islands introduce complexity to the system through nonmonotonic nonlinear conductive link to the substrate; (b)–(d) Cross-sectional view showing island i, whose potential v_i is influenced by the charges q_j in the rest of the network through a capacitance matrix. Continuous charge dynamics (where electric charge is a classical continuous variable) is depicted in (b). An analogous system governed by single electron dynamics (charge is a discrete variable) is depicted in (c). Dynamics of networks with quantum links (in which charge transport is phase-coherent) is depicted in (d).

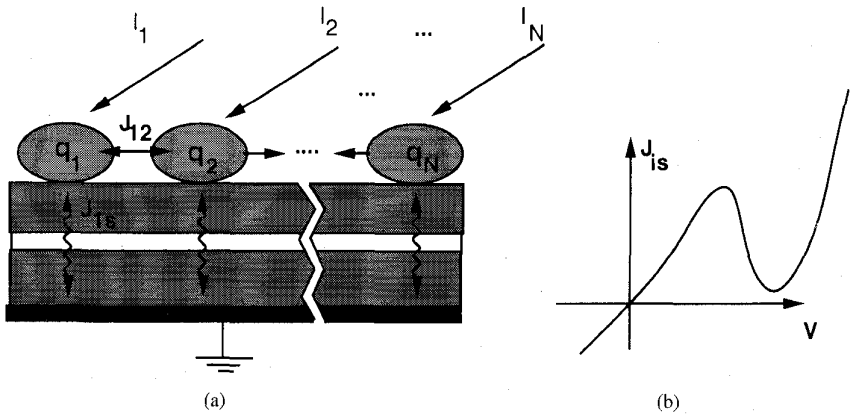
The choice of the system in Fig. 1(a) was motivated by the observation that complex spatial and temporal patterns of the electronic charge distributions on the metallic islands, resulting from the nonlinear interactions amongst thousands of devices (islands) which are collectively driven far from equilibrium by currents applied at the program nodes, may reveal a fundamental kind of computational effect [22]. Indeed, we will show in Section III that this system is tailor made for neuromorphic computation and signal processing.

III. Specific Examples of Neuromorphic Networks Using Quantum Dot Arrays

In this section, we will provide specific examples of useful computational or signal processing functions performed by the generic array of electrically linked nanometer sized metallic islands shown in Fig. 1(a). We will consider, primarily, memory-like circuits which operate on the basis of neuromorphic principles. It is possible to establish a connection between neuromorphic computational models and the charge dynamics in an array of metallic islands, in the presence of each of the different network mechanisms indicated in Fig. 1(b)–(d). For example, when the operation of the network is governed by single-electron effects at each island [see Fig. 1(c)], the choice of a neuromorphic approach is motivated by a straightforward comparison between the granular dynamics of electrons in an array of islands, and the dynamics of discrete Hopfield networks [23]. We will illustrate this in Section III-C with a specific example. Additional impetus for restricting attention to memory applications comes from the realization that single-electron charging dynamics is stochastic in nature, which hinders the conceptualization of logic applications. Associative memory, on the other hand, can benefit from an appropriate kind of stochasticity.

A. Neuromorphic Continuous Charge Network

The first example of neuromorphic networks we consider is a purely classical example where the islands in Fig. 1(a) are large enough (diameter ~100 nm) and the temperature high enough that single electron effects are not prominent. Charge can be considered a continuous (rather than discrete) variable and the corresponding network mechanism is illustrated in Fig. 1(b). A one-dimensional (1D) version of the circuit is shown in Fig. 2 in which we assume that the current between islands i and j is J_{ij}, and that the current between island i



(a) (b)

Fig. 2. (a) A 1D array of islands, whose dynamics is described by (2); (b) a nonmonotone substrate nonlinearity of the kind shown here, is the minimal condition for the realization of collective effects. This characteristic can be produced by a resonant tunneling diode.

and the grounded substrate is J_{is}. Since charge is considered a continuous variable, we can write from Kirchoff's current balance condition that

$$\frac{d}{dt}q_i = C_i\frac{d}{dt}v_i = -\left[J_{is}(v_i) + \sum_{j\neq i} J_{ij}(v_i - v_j)\right] + I_i(t) \qquad (1)$$

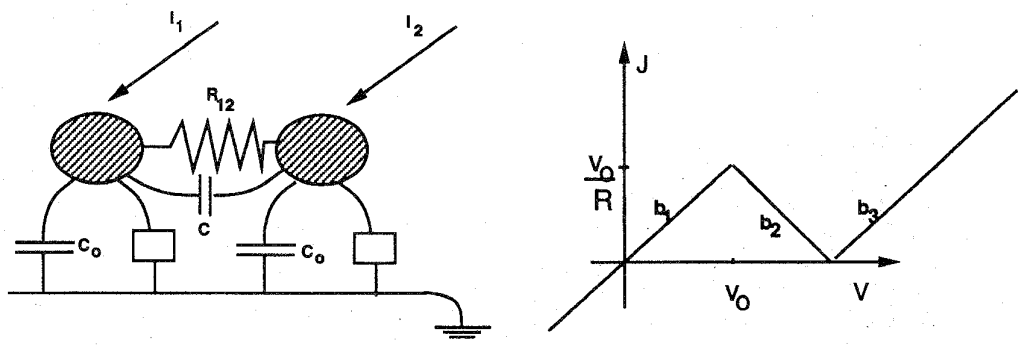
where $I_i(t)$ is the driving current, q_i is the charge, v_i is the potential, and C_i is the capacitance, with the subscript i indicating the relevant island. J_{is} is a nonmonotonic nonlinear function of v_i corresponding to the current-voltage characteristic of an RTD.

1) Operation as an Associative Memory: Qualitatively, the multiple solutions to the nonlinear system of equations which results from (1) under steady-state conditions ($dv_i/dt = 0$ for all i) will be taken as a set of memory states which can be programmed by properly choosing the current biases I_i. The current biases I_i will be assumed to be either time independent, or slowly varying on time scales over which the network relaxes into its memory states. If the network is begun at time $t = 0$, with a certain initial condition $v_i = q_i/C_i$ for all i, arranged, for instance, by an initial impulse of charges q_i at each of the islands, then the network will evolve toward the closest memory state, as programmed by the current biases I_i. This is the functioning of an associative memory.

Equation (1) bears strong similarities to the equations representing the additive short-term memory (STM) (or Content Addressable Memory (CAM)) model of neural networks [24]. Therefore, it is obvious by analogy that the system in Fig. 2 realizes the STM or CAM model. The significant difference is that, while conventional circuit realizations of the STM model require operational amplifiers (whose transfer functions exhibit monotonic sigmoidal nonlinearities) and massively interconnected networks of resistors [24]–[26], all we need is an RTD as a substrate which provides a *nonmonotonic* nonlinearity in the local transport. In [8], we showed that this nonmonotonic nonlinearity is sufficient for the realization of associative memory effects. Op-amps are very costly in terms of real estate on a chip and also consume too much power. As a result, neural networks have been unable to compete with conventional silicon VLSI technology. In contrast, RTD's are very compatible with low-power nanoelectronics. They can be integrated vertically beneath the array of islands so that they do not use up any real estate on the chip. There has been some prior research involving resonant tunneling diodes (RTD) for the realization of neuromorphic systems by Levy and co-workers [27]. Additionally, some early investigation of networks of tunnel diodes has been reported by Stern [28] and by Wilson [29], which also exhibit current-voltage characteristics of the kind shown in Fig. 2(b).

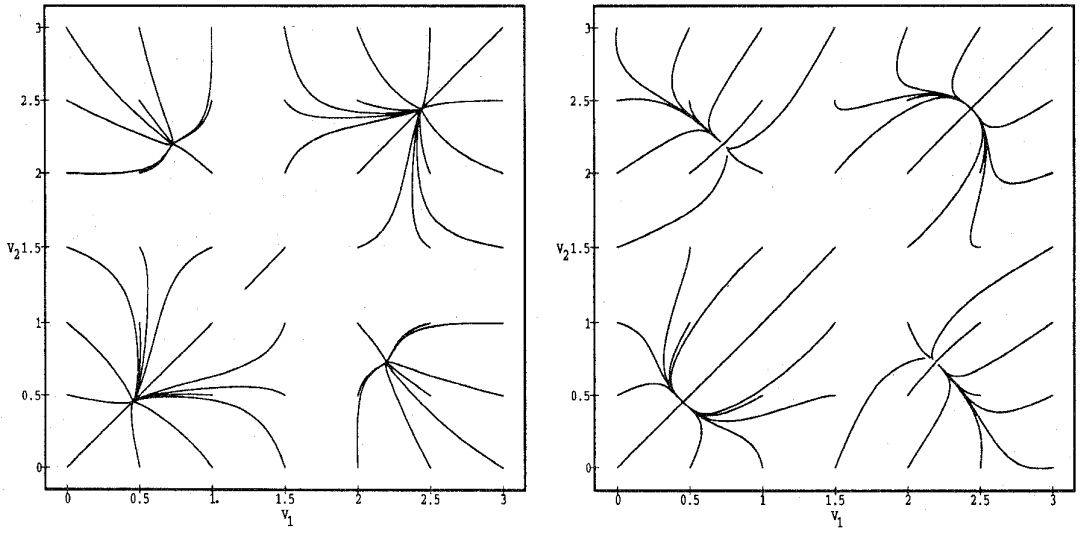
In [8], we proved two important results pertinent to this system. First, based on global stability analysis using Liapunov functions, we showed that the system in (1) is globally stable. This implies that there are no limit cycles, and that every trajectory of the system will converge to one of its equilibrium points. Second, we showed that nonmonotonic nonlinearities in the current-voltage characteristic of local transport, such as that shown in Fig. 2(b), are necessary to obtain *multiple* equilibrium points for nontrivial collective computational activity in these networks. It should be contrasted with the general requirement of monotonic nonlinearities in generic additive short-term memory systems [24]–[26] which is realized through op-amps. This result also has immediate consequences to nanoelectronics, in that staircase nonlinearities, which have been produced in quantum point contact constriction [30] and asymmetric double junction single electron tunnel devices [31] can be seen to be inadequate for the realization of collective activity. However, there are several electronic devices which can produce nonmonotonic nonlinearities, e.g., Esaki diode, IMPATT diode, BARITT diode, etc. [32]. We are interested chiefly in semiconductor heterostructure devices which can be integrated vertically beneath the array of islands. They must also be low power devices. Therefore, the ideal structure is a RTD. Since our work focuses on nanoelectronic realizations, complex circuitry cannot be integrated with the basic elements anyway owing to the small size of the islands. Therefore, an RTD seems to be the optimum choice.

We next provide numerical results based on particular choices of J_{ij}'s and J_{is}'s. Our first example is illustrated in Fig. 3(a), in which the two islands are coupled with each other



(a) (b)

Fig. 3. (a) Two islands coupled by a resistor R_{12} and capacitor C. Each island is also coupled to the substrate by a capacitance C_0 and a nonlinear resistor whose current voltage characteristic is given in (b); (b) Piecewise approximation to the nonmonotonic nonlinearity of the substrate conduction [cf. Fig. 2(b)]. This characteristic defines the quantities R and v_0. Each segment has the same magnitude of slope $1/R$.



(a) (b)

Fig. 4. Phase portrait for two-island system in the continuous-charge model, in which the voltage axes have been scaled with respect to v_0. The parameters are $R_{12} = 5R$, and $I_0 = v_0/2R$. (a) with only substrate capacitance $C_0 = 2q/v_0$,, and (b) with identical mutual and substrate capacitances: $C = C_0$.

through a linear resistor R_{12} and a capacitor C. In addition, we assume that each island is *individually* coupled to the substrate through a capacitance C_0, and a nonlinear resistor whose current-voltage characteristic is shown in Fig. 3(b). Furthermore, each island is driven by a current I_o fed externally. Since the results presented here are numerical in nature, we have minimized the number of parameters by choosing a piecewise linear function to represent the I-V characteristic of the RTD (substrate conduction). Each of the three segments are given slopes of the same magnitude R

$$J_s(v) = \begin{cases} v/R & v < v_0 \\ (2v_0 - v)/R & v_0 \le v \le 2v_0 \\ (v - 2v_0)/R & v > 2v_0 \end{cases}. \qquad (2)$$

The equilibrium points of this two-node system can be found by setting $\dot{v}_1 = \dot{v}_2 = 0$, and the stability properties of those equilibrium points can be ascertained by examining the eigenvalues of the system matrix near the equilibrium points [33], [34]. Provided that the driving current $I_0 < v_0/R$, each island can in principle be on any one of the three branches of the nonlinear function $J_s(v)$. We can, however, show that the system will be unstable if either island is operated on branch b_2. So, it follows that this system can have at most four different globally stable points, since each island is restricted to being on either branch b_1 or b_3. Two of these stable points are trivial ones corresponding to both islands operating on the same branch : either b_1, or b_3. We have determined a necessary and sufficient condition for the existence of all four "memories," and the corresponding phase portraits are shown in Fig. 4.

One can also realize *programmed* associative memory. An example is shown in Fig. 5 where different choices of inter-island resistances lead to the occurrence of either eight, four, or two equilibrium points.

2) Image Processing Network: Fig. 6 shows results of further numerical investigations, where a 2D array of 10×10 islands with *only near-neighbor connections* and the same substrate nonlinearity [as shown in Fig. 3(b)] are used. An

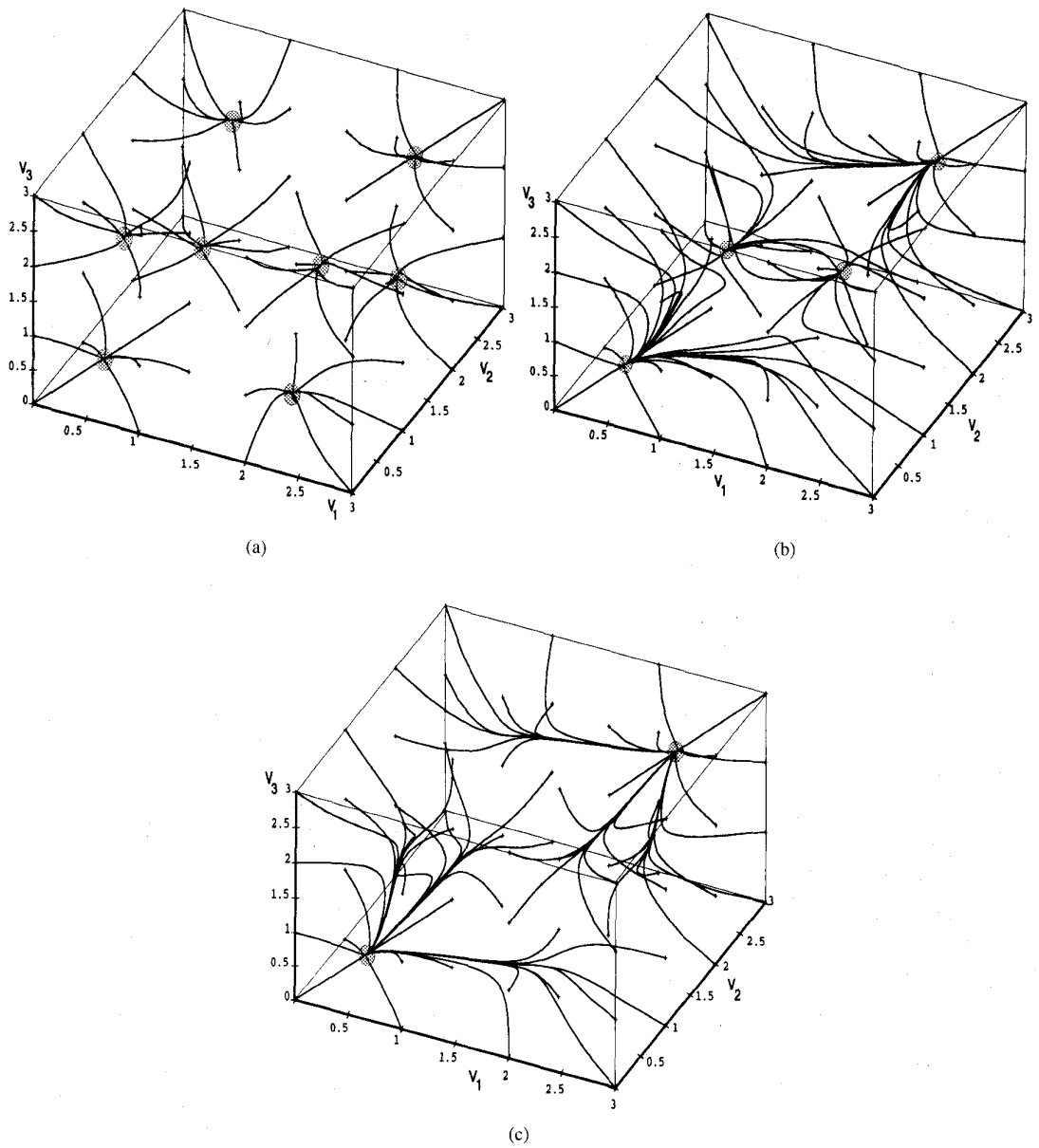


Fig. 5. Phase portrait for a three island system. This figure indicates the possibility of programming a network by choosing resistance parameters appropriately. Only substrate coupling C_0 is permitted. The stable equilibrium points are indicated by the shaded circles. (a) eight states, with $R_{12} = R_{23} = R_{13} = 10R$,; (b) four states, with $R_{12} = R_{23} = 10R$, and $R_{13} = 5R$.; (c) two states, with $R_{12} = R_{23} = R_{13} = 5R$.

input image is digitized to create dark and light pixels. Each pixel generates a voltage on a corresponding island. These voltages lie on a particular branch—b_1, b_2, or b_3, in Fig. 3(b)—of the substrate nonlinearity. Dark pixels place the corresponding voltages on the branch b_3, light pixels on the branch b_1 and intermediate grey pixels on the branch b_2. In example (a), the input contains domains which are either predominantly dark, or light, and the resulting output recovers domains which are either all dark, or all light. This is an example of "smoothing," an important image processing capability. Other image processing functions can be realized as well. We must point out that this 10×10 network consumes an area of 10^{-10} cm^2 so that ten trillion such image processors can be fabricated within an area of 1 cm^2. This is an unprecedented functional density.

B. Single-Electron Charging Effects

We have also considered the same two-island network as in Section III-A, with the assumption that single electron charge effects (granularity of charge) have become pertinent either due to the lowering of temperature, or due to the physical scaling of the metallic islands down to $d \sim 10$ nm. Single-electron effects will become relevant, when the change in potential $\delta V = q/C$, associated with the addition of a single electron charge q to an island, becomes comparable to kT/q, the thermal potential. This condition can be met even at room

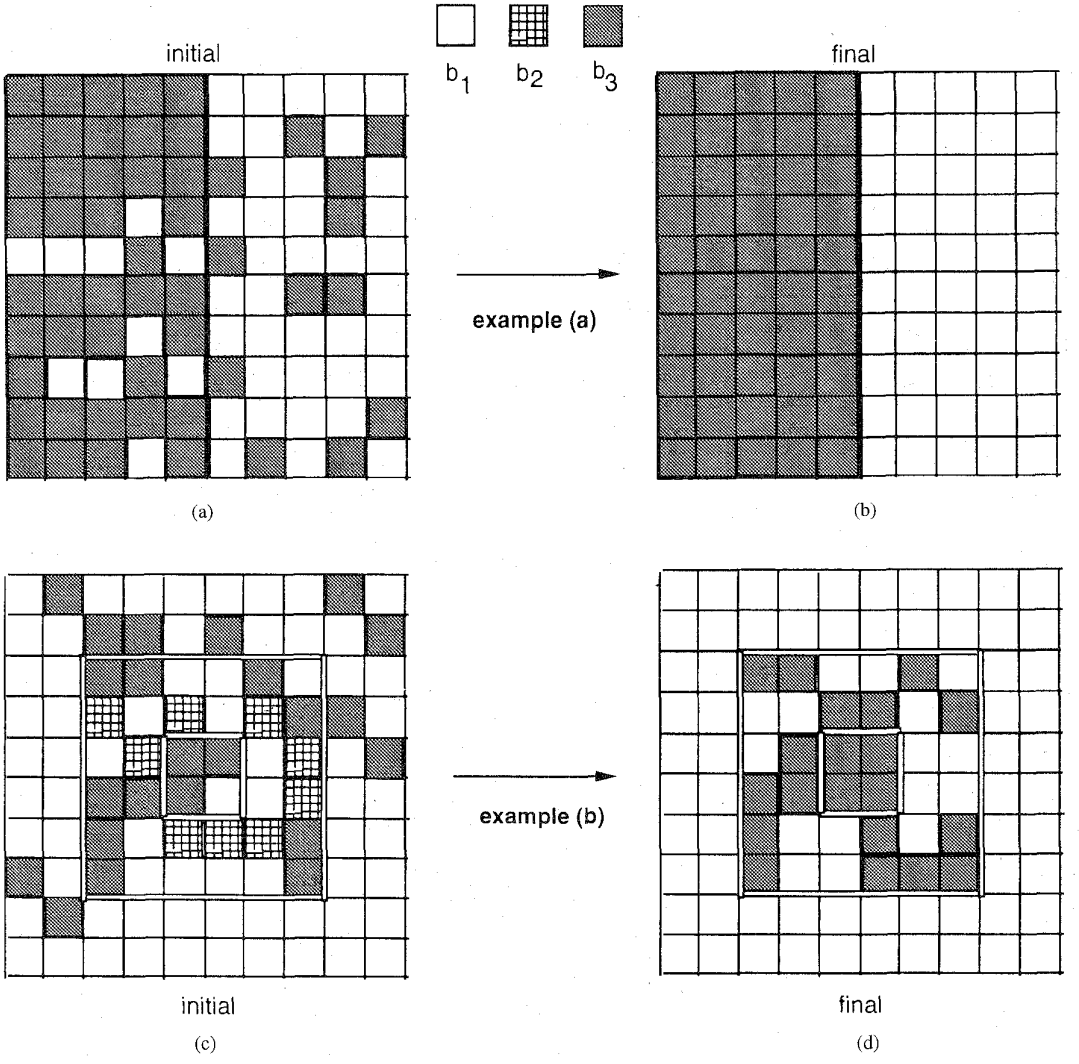


Fig. 6. Rudimentary image processing capability in a *near-neighbor* connected network of 10×10 islands, which are all pumped by the same current $I_0 = v_0/2R$. Each island is colored in accordance with the particular branch—b_1, b_2, or b_3, in Fig. 3(b)—of the substrate nonlinearity, the island potential lies on. (a) The resistive network is uniform $R_{i\pm1,j\pm1} = 6R$. The input contains domains which are either predominantly black, or white, and the resulting output recovers domains which are either all black, or all white. (b) The network is partitioned into three concentric regions. The islands in the outermost and innermost regions are coupled with low resistances $R_{i\pm1,j\pm1} = 3R$, and the islands in the intermediate region are coupled with high resistances $R_{i\pm1,j\pm1} = 13R$. Parts of the network with low resistance produce regions which are either all white, or all black depending on which was predominant in the initial state.

temperature if islands with an effective capacitance smaller than $C \approx 5 \times 10^{-18}$ F are fabricated.

Single electron dynamics are characterized by discrete tunnel events. Therefore, the differential equation systems of (2) cannot be used to model the arrays. We developed a Monte-Carlo simulation technique [35], [36], for the simulation of a current biased network of islands, shown in Figs. 1 and 2. Owing to space limitations, we cannot describe it here, but instead refer the reader to [8].

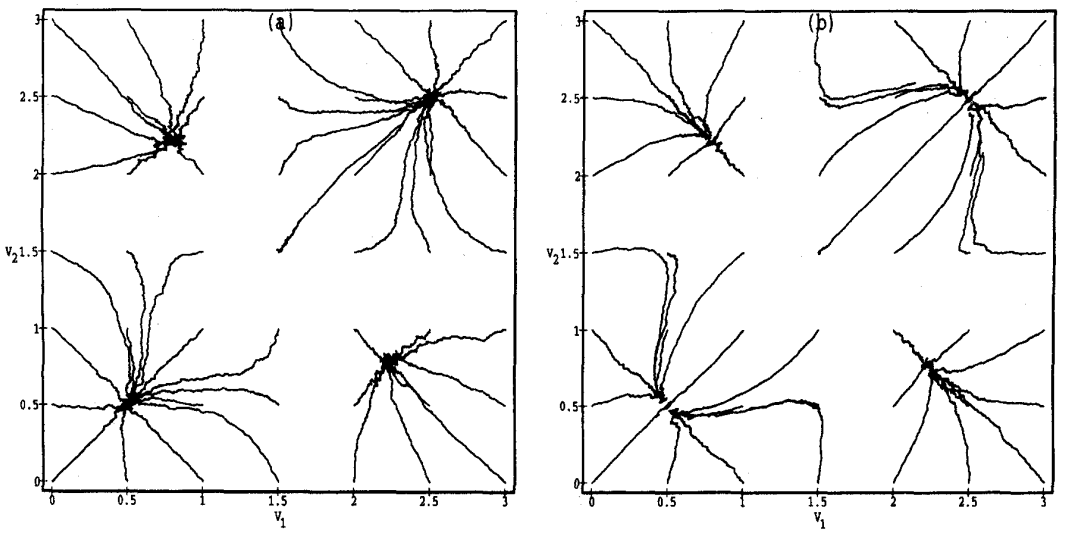
The results based on our numerical simulator show the following:

1) For large enough values of the effective substrate capacitances (C_0), the effect of the single electron dynamics is marginal and the *system is adequately described by the continuous charge models*. Thus even arrays of metallic islands with diameters of few nanometers can exhibit the same associative memory and image processing capabilities studied in Section III-A.
2) If the substrate capacitance is made smaller, the granularity of the trajectories become larger, and for small enough values, the phase portrait breaks out into oscillations [8].

These effects are illustrated in Fig. 7, where the same system shown in Fig. 3 is investigated under single-electron dynamics.

C. Ising-Type Single-Electron Networks

The examples in Section III-A and III-B did not utilize single-electronics in a direct way, i.e., single electron charging effect was not central to the operation of the circuit. However, there are instances when single electronics plays a pivotal role. In [8], it was shown that the evolution of an initial charge distribution toward a stable final equilibrium distribution in a



(a) (b)

Fig. 7. Phase portrait for the same two island system in Fig. 3 where the granularity of charge (single electron charging) has been taken into account. These results are obtained from Monte-Carlo simulation and are discrete charge versions of the two cases in—Fig. 4(a).

system of the type of Fig. 1(a) can be given a neuromorphic interpretation. These properties emerge *purely as a result of the discreteness of electronic charge*, and the only assumption made in establishing this connection is that the inter-island capacitances can be chosen arbitrarily.

In [8], it was shown that the discrete stochastic dynamics of electrons can be viewed as a procedure for simulated annealing. Consequently, several problems from combinatorial optimization can then be mapped to different single-electron networks. A novel mapping methodology tailored specifically for single-electron networks was developed. Owing to space limitations, we cannot address this in greater detail here, but we mention that a specific example we examined is the traveling salesman problem. This NP-complete optimization problem can be solved very fast by an appropriate single electron network. For details, we refer the reader to [8].

IV. Fabrication of Neuromorphic Networks: Self-Assembly

We now address the fabrication of these networks. Conventional nanolithography involving electron beam, ion beam, x-ray or even scanning tip lithography [37] are unsuitable for fabricating single-electron circuits for two basic reasons: 1) they are usually *serial* in nature (direct-write techniques) whereby the patterns on each wafer must be exposed sequentially, resulting in a throughput that is unacceptably slow for commercial mass production; and 2) they often cause significant radiation damage to processed nanostructures [38]–[43]. In contrast, the recently developed techniques for self-assembly of periodic quantum dot arrays [14], [44] suffer from neither of these drawbacks and therefore offer an attractive choice.

Fabrication of the network shown in Fig. 1(a) has three key elements: 1) deposition of a regimented, *periodic* array of nanosized metallic islands on a RTD; 2) electrical isolation of these islands via mesa-etching through the RTD; and 3) linking the islands with molecular wires or some other means. Fabrication of a periodic, 2D array of metallic islands with diameters in the 5–100 nm range has been demonstrated by us using electrochemical self-assembly [44]. This approach has two advantages over conventional direct-write lithography (e.g., e-beam, ion-beam or STM lithography). First, it is a "gentle" technique that does not cause serious processing damage, and second, it is *parallel* in nature whereby large batches of wafers can be processed simultaneously and all patterning on a given wafer is performed simultaneously, resulting in several orders of magnitude improvement in throughput. In order to illustrate the feasibility of realizing nanoscale circuits using these methods, we outline a specific process which employs self-assembly techniques, several of which have been developed by the authors and their collaborators.

First, using molecular beam epitaxy, an RTD structure is synthesized and capped by a thin (3 nm) low-temperature grown GaAs layer (LTG:GaAs), which is highly resistant to oxidation [45] and which serves to passivate underlaying doped layers [45], [46]. Then on the surface of this layer, a thin-film of Al (~100-nm-thick) is resistively evaporated. This film is electropolished in perchloric acid/butyl cellusolve/ethanol/distilled water at 60 V for 30 s resulting in a dimpled surface containing a highly periodic array of crests and troughs as shown in the *raw* atomic force micrograph data in Fig. 8.

The trough regions of this dimpled film can be selectively etched away by bromine/methanol leaving isolated islands of Al (the crests) on the surface (see Fig. 9). The trough regions are etched away before the crests since the Al film is much thinner in these regions (by approximately 50 nm). In fact, the ratio of the Al film thicknesses in the crest and trough regions can be easily made as large as 10:1 which facilitates selective etching of the troughs. This results in a 2D periodic array of nano-sized metallic islands on the surface (vestiges of the crests) which now need to be electrically isolated. For this, we

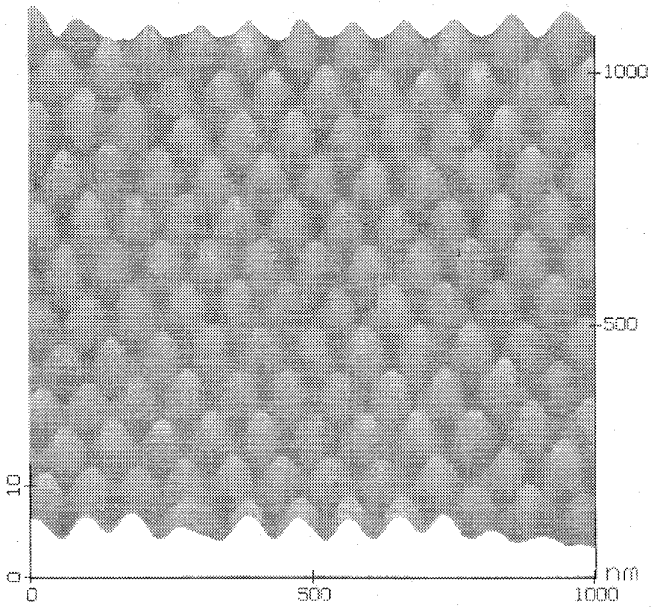


Fig. 8. Atomic force micrograph of a dimpled electropolished Al surface showing a periodic array of crests and troughs. This pattern is self-organized. The height of the crests above the troughs is about 50 nm.

proceed as follows. One can use this periodic array of islands as a mask to shallow-etch electrically isolated mesas capped by the metal Al. The use of the metallic island array as the etching mask for patterning the RTD substrate provides a self-alignment between the metal islands and the semiconductor mesas. Deep etching is not feasible, due to the small areas of the Al dots and the need to keep a relatively planar surface for subsequent interconnect steps. The LTG:GaAs layer allows one to keep the underlying n-GaAs layer very thin without risking oxidation [45]. The isolation etch can be shallow since the removal of the LTG:GaAs layer eliminates the passivation effect, resulting in the depletion of the regions between the islands. The final step is to electrically link the islands. For this, the space between the mesas may be filled up with a chosen material by electrodeposition, sputtering, or low-temperature grown MBE layer to create a resistive and/or capacitive connection between the dots.

Instead of using the electropolished Al technique, one can also deposit a self-assembled, 2D network of metal clusters on the surface of the substrate with adjacent clusters linked by molecular wires. Techniques to deposit ordered arrays of nanometer diameter Au clusters on various flat substrates, to deposit organic molecules (molecular wires) between adjacent clusters have been demonstrated and the in-plane electronic conduction through arrays of 4 nm clusters deposited between lithographically defined contacts has been studied [14], [15], [47]. Again, the deposited cluster network can be used as a self-aligned mask to etch through the RTD and create mesas capped by metal dots (Fig. 10). The inter-island links are already provided by the molecular wires. Although the technology of molecular wires is in its infancy, significant progress has been made in the synthesis, characterization and modeling of molecular wires suitable for this application [48], [49]. The advantages of molecular wires are: 1) great flexibility in choosing the resistance and capacitance between clusters [48]; and 2) electrical access to individual nanometer sized dots may be feasible due to the nanometer size scale of the wires and the ability to deposit wires on selective regions based on the composition of the regions and of the molecular end groups. These capabilities would be necessary for realizing certain processors where one needs variable inter-island resistances and capacitances as well as image processors where one needs to address individual dots.

The fabrication steps outlined to this point have addressed the metallic island array, the interisland linking and the RTD substrate required for the computational cells. The same techniques used to provide resistive linking between islands can provide the linking between islands at the edge of the array and input/output or programming contacts. In "edge-driven" configurations, the computational cells will also require a resistive link between each island and a bias plane, presumably located above the island array, to provide the current bias required to achieve bistability in voltage. This capability appears feasible using either molecular wires or a thin-film resistive layer deposited between the island array and the bias plane. It should be noted that the most time consuming "direct-writing" steps of nanolithography have been replaced by chemical self-assembly in the proposed synthesis techniques. In principle, large batches of wafers can be electropolished and subsequently etched in a large bath, thereby making the electropolishing technique a truly parallel process with fast throughput. The self-assembly synthesis of metallic cluster arrays could also be a high throughput process. This is a significant advantage over "direct" write based fabrication processes for nanoscale circuits.

The ability to realize individual address lines for each island, while beyond the capability of the self-assembly techniques presented here, would allow configurations where individual

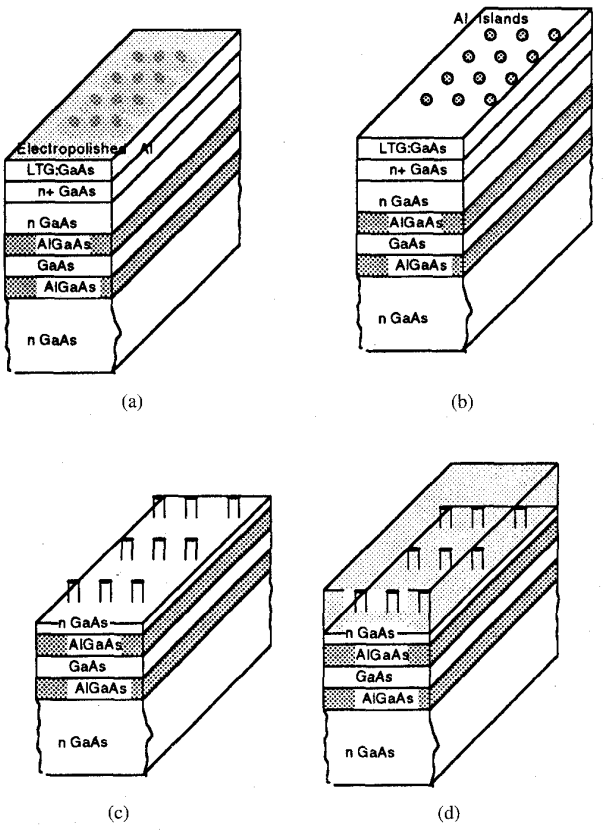


Fig. 9. Fabrication steps to realize the neuromorphic network in Fig. 1(a) using self-assembly techniques. The steps are described in the text. The inter-island connection is made *not* by molecular wires, but by an electrodeposited, sputtered or MBE-grown layer grown on the etched surface. A wide variety of layer materials can be used, resulting in phase-coherent, rectifying, resistive or capacitive links.

islands could be addressed in order to provide input/output or programming, Achieving this type of interconnect configuration at the nanometer scale would require significant advances in technology, but may be possible using scanning probe based lithography.

In order to establish the feasibility of the proposed synthesis techniques, it is informative to consider the ranges of capacitance and resistances achievable with these techniques. Using a conservative estimate for the minimum achievable island diameter of 20 nm, the capacitances between adjacent islands and between an island and the substrate will be on the order of 10^{-18} F, corresponding to Coulomb charging energies of about 70 meV. Molecular wires which have been reported to date have resistances on the order of 20–40 MΩ per molecule when bridged between metal electrodes [15], [48], [49]. Since metallic clusters with 20-nm diameters can have hundreds of molecular wires in parallel between each pair of adjacent clusters, achievable island to island resistances should be on the order of 0.1–10 MΩ [15], [47], [49]. In order to bridge distances significantly longer than 2 nm, networks of these molecular wires may be required. An RTD substrate with peak current density of 1×10^5 A/cm^2 would yield a peak current of 0.3 μA for each semiconductor mesa, assuming that the current density remained constant as device dimensions

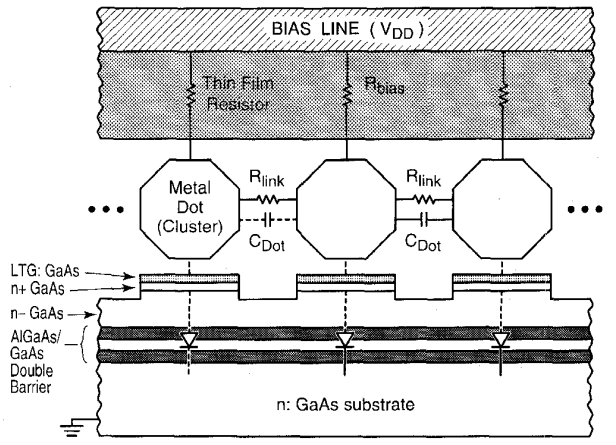


Fig. 10. Another possible fabrication strategy where the metal dots are clusters self-assembled on the surface and linked by molecular wires. $R_{\rm link}$ and $C_{\rm Dot}$ are the interdot resistances and capacitances that are realized by molecular wires. Self-assembly techniques for 2D linked arrays have been demonstrated and the in-plane electronic conduction through such an arrays has been studied (see [14] and [48]).

are scaled down. For a voltage at peak current of 0.5 V, this corresponds to an average resistance of approximately 1.5 MΩ for the RTD characteristic. The use of short-chain molecular wires along with a low-resistance, nonalloyed contact structure [50] should provide an interface coupling resistance of less than 200 KΩ between the metal island and the semiconductor mesa for this island size. The devices can be effectively current biased if the resistance from a bias plane, located above the array, to each island is much greater than the characteristic resistance of the RTD mesa. Since the resistance through certain molecular wires consists of state-assisted tunneling [48], a suitable resistance, e.g., a resistance on the order of 5–10 MΩ, could be achieved by using longer molecular wires to connect each island to the bias plane. It may also be possible to use a thin-film resistive material deposited between the metallic island array and the bias plane to realize the linking of each island both to adjacent islands and to the bias plane. A resistivity of approximately 50 $\Omega \cdot$ cm would be required; an ideal material would also possess an anisotropic resistivity characteristic to allow independent control of the vertical and horizontal linking resistances. It therefore appears feasible to realize appropriate resistance and capacitance elements for the proposed computational cells using the technologies discussed in this section.

V. Conclusion

In conclusion, we have presented a neuromorphic architecture for powerful computing and signal processing applications using an array of metallic islands on a resonant tunneling diode. Some of the components required to fabricate these circuits are in their infancy. Nontheless, the rapid progress in nanoelectronics may make these circuits a reality in not too distant a future.

Acknowledgment

The authors are indebted to numerous colleagues for insightful discussions. We are especially grateful to Dr. J. A. Cooper,

Jr., Dr. P. Balasingam, Dr. M. Cahay, Dr. A. E. Miller, Dr. R. P. Andres, Dr. J. M. Woodall, and Dr. R. Landauer.

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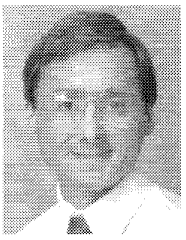

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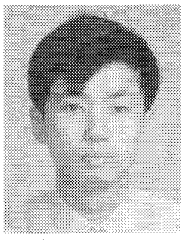

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