# Granular nanoelectronics

## *The logical gateway to the 21st century*

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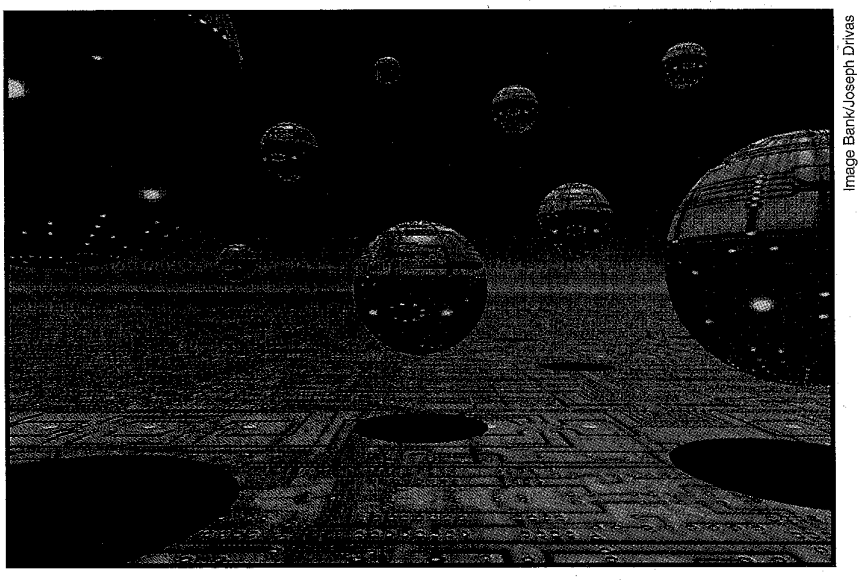
A popular belief among solid state device and circuits engineers is that conventional silicon technology will reach its performance limits in less than ten years. Spurred by this notion, engineers have been proposing a new class of electronic devices that utilize quantum-mechanical principles (as opposed to classical principles) for their operation. These devices are often referred to as *quantum devices* or *nanoelectronic* devices since their physical dimensions are typically smaller than 100 nm.

The granularity of electric charge (namely that it can be found only in quanta of a single electron's charge) is a quantum-mechanical property. Similarly, the granularity of an electron's "spin" (namely that only certain polarizations may be allowed) is also a quantum-mechanical property. These two "granular" properties are quite robust; they, therefore, show much promise in actual device applications.

Ultrafast and ultrasmall electronic devices that utilize the granularity of electric charge (and an associated effect known as Coulomb blockade) have been proposed for years. Boolean logic gates, combinational circuits and sequential memory have been designed with them. "Single electron transistors" (SET) built on this concept have been demonstrated experimentally by researchers in Asia, Europe and U.S.

A newly proposed class of Boolean logic gates utilize a single electron as the primitive logic element (a bistable switch). The spin polarization of the electron (a quantum-mechanical property) encodes binary bits instead of voltage. Physical wires between devices are replaced by quantum-mechanical spin-spin couplings which communicate signals across the chip. These are unusual features which distinguish a "quantum circuit" from a conventional classical architecture.



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The following scheme was conceptualized by us and our co-workers. Consider a two-dimensional array of semiconductor quantum dots (ultrasmall structures) laid out on a wafer. Each dot is so small that it can only host a single conduction band electron. Such dots have been fabricated by many researchers recently. Each conduction band electron in a dot interacts with only its nearest neighbors because the overlap between the wave functions of only the nearest neighbor electrons is non-zero. If this system is subjected to a weak magnetic field, the quantum-mechanical "spin" of every conduction band electron can assume only two possible polarizations: 1) along the field, and 2) opposite to the field.

Therefore, the spin can encode binary bit information and every conduction-band electron can act as a bistable switch. By cleverly manipulating the spin-spin interactions between neighboring electrons (i.e. by arranging the quantum dots in different geometric patterns), it is possible to realize logic gates. Various patterns give rise to various interactions and, thus, various logic functions (AND, NOR, etc.). These can be further manipulated to yield more complex circuits such as full adders and subtractors, sequential memory such as flip-flops, ripple counters and read-only memory (ROM).

These logic circuits are unusual in many ways. A binary signal (spin-state) is communicated from one electron to the next (or one device to the next) by nearest neighbor spin-spin coupling.

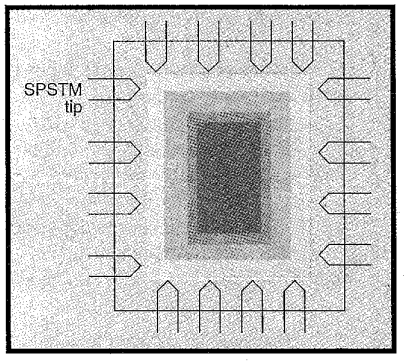


*Fig. 1 A schematic of an edge-driven artificial quantum solid chip. The solid dots represent single electron cells or quantum dots.*


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There are no physical wires connecting devices on a chip; the quantum-mechanical interaction plays the role of wires. This eliminates the "interconnect bottleneck" that plagues ultra-large-scale-integrated circuits (ULSI). It also leads to unprecedented computational speed and a very low power delay product.

The concept of this interconnectless chip (or quantum-coupled circuit) was pioneered by researchers at Texas Instruments. They also suggested the use of cellular automata architecture since it is most synergistic with short-range quantum-mechanical coupling. The problem with the cellular automata approach, as correctly pointed out by Rolf Landauer of IBM, is that one does not know how to load the initial program into the array. Clocking is also difficult. In view of all this, other interconnectless architectures, different from cellular automata may be more suitable.

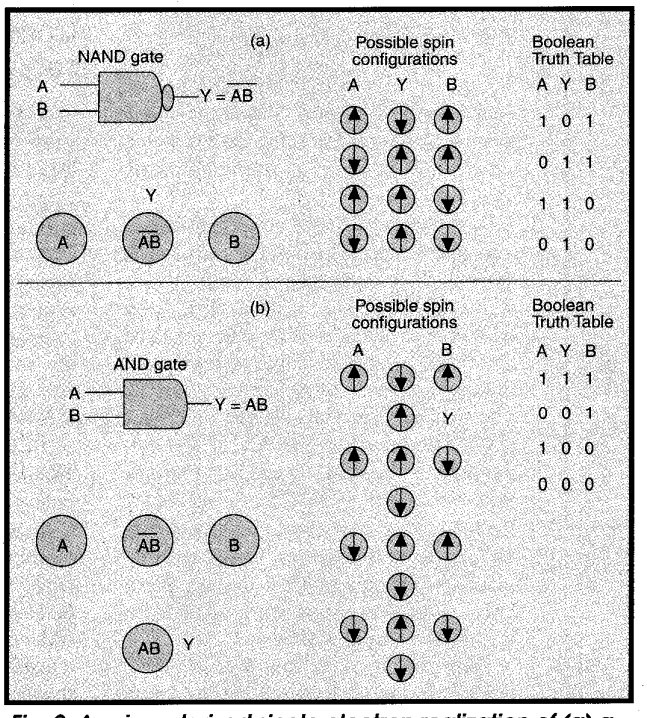


***Fig. 2 A spin-polarized single electron realization of (a) a NAND gate, and (b) an AND gate. Also the four possible spin configurations corresponding to the four binary input combinations viewed as the truth table.***

Even in quantum coupled circuits, all interconnections, of course, cannot be eliminated. Some electrons or devices on the chip must communicate with the external world and the user through physical wires. These electrons (devices) act as the input/output ports which receive data and feed the results of the computation back to the user. These ports (i.e. the corresponding quantum dots) are all placed on the edges of the wafer where the packing of dots are sparse. At the center of the chip, the packing is very dense and individual devices (or dots) cannot be accessed by external contacts (Fig. 1).

## Computing paradigm

We now will describe how such a system of interacting spin-polarized electrons computes. Computation is made possible by quantum-mechanical laws that govern the temporal evolution of the spin orientations (or, equivalently, the logic states) of interacting electrons. Input data is provided to the entire array (or "chip") by aligning the spins of electrons at the edges of the wafer that act as input ports. This is done using spin-polarized scanning tunneling microscope (SPSTM) tips that are permanently attached to the edges (see Fig. 1). SPSTM tips have the spatial resolution to address single quantum dots. They can also orient an electron's spin in such a dot. These tips are micromachined into the chip.

The arrival of the input takes the entire system into a collective excited spin state. The excitation is communicated via nearest neighbor spin-spin coupling from electron to electron throughout the chip. Spins flip in a domino-like fashion dissipating energy (emitting phonons) as the many-electrons system cooperatively relaxes to a new thermodynamic ground state characterized by a new configuration of spins. The interactions are so engineered, that once the new many-body ground state is reached, the logic states (spin orientations) of electrons in quantum dots (output ports) at another edge of the wafer represent the results. The output data string (spin orientation) is then read from these output ports with SPSTM tips and transduced into voltage or current for the user. Different layouts of the quantum dots on the wafer give rise to different interactions and, thus, different logic functions (AND, NOR, etc.). These logic gates are utilized to generate various types of combinational circuits and sequential memory.

An interesting feature of this scheme is that computation proceeds by allowing the devices to collectively relax to their thermodynamic *ground state*. Since individual devices are not accessed, there really is no way of maintaining them in excited states. Therefore, the devices settling back down to ground state is an unavoidable feature. However, it is very desirable since it guarantees a great deal of noise immunity and fault tolerance. If a device strays from its logic state owing to local perturbations, it will still ultimately decay to the ground state and, therefore, the right logic state. In addition, there is no need for refresh cycles which consume 80% of the total power dissipated in a chip. This idea of computing with the ground state is also inherent in Hopfield-type neural networks. In the context of Boolean logic gates, however, it is new and was proposed by researchers at Texas Instruments along with a group of researchers from Boston College.

The concept just described has many unusual features. Note, for instance, that in order to switch a logic bit from 0 to 1 or vice versa, one does not have to move charges from one place to another. (The method used in all conventional devices such as field-effect transistors.) Instead, one merely has to toggle an electron's spin without any physical movement of charges.

This is a great advantage since it eliminates transit time limitations on the switching speed and also resistance capacitance (RC) time constant limitations. (No current flow is required to switch a device.) These two limitations apply to almost all other electronic devices—classical or quantum. Thus, the switching of spin devices can be very fast and perhaps take less than one picosecond. Furthermore, an electron's spin polarization can be very robust. It is not flipped easily by any external perturbation except a strong magnetic field. This promises excellent noise margin. Finally, the bistability of spin polariza-

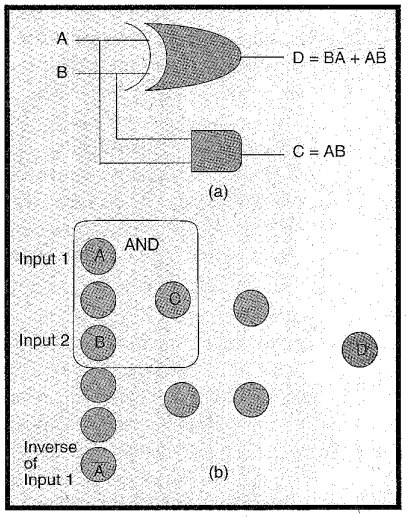


*Fig. 3 (a) A binary half-adder using exclusive-OR and AND gates, (b) a spin-polarized single electron realization.*

tion exists even at quite elevated temperatures—much above room temperature—so that these devices do not require cryogenic operation.

## Boolean logic gates

To design Boolean logic gates, we use only two basic properties of the system we have described: a) antiferromagnetic ordering, i.e. in the ground state any two nearest neighbor electrons have opposite spins, and b) short range interactions, i.e. only nearest neighbor interactions matter. Second-nearest neighbor interactions between cells are unimportant since spin-spin (or the so-called "exchange") interaction between neighboring spins decays exponentially with distance.

Incidentally, the first property is not obvious. However, it turns out to be a fundamental property that is enforced by the exchange interaction. These two properties together imply that if the spin of any one electron in a cell is "up," then the spin of its nearest neighbor must be "down" even if a third "downspin" electron is only incrementally farther away. This is all we need to implement any logic function.

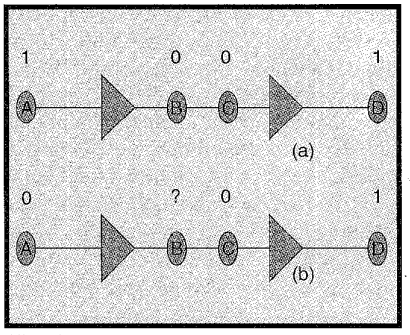


*Fig. 4 Two inverters in (a) the steady state, and (b) the transient state immediately after switching the far left input A.*

In elucidating the construction of logic gates, we will adopt the convention that the "up" spin state is logic level 1 and the "down" spin state is logic level 0. To construct a NAND gate, we need three equally spaced single electron cells (quantum dots) in a linear chain (Fig. 2). The two extreme cells are the two input ports. The one in the middle is the output port. If the spins in the two extreme cells are oriented "up" (i.e. both inputs are held at logic level 1), then the spin in the middle cell must be "down" to preserve antiferromagnetic ordering. Similarly, when the inputs are held at logic level 0, the output will be at 1.

Now, if one of the inputs is 1 and the other is 0, then the output can be either 1 or 0 since these two possibilities appear to energetically degenerate. However, they will not do so if a weak external dc magnetic field is applied globally on the entire chip. Such a field is actually already present since it is required to define the two spin orientations which encode the binary bits. The field induces a small Zeeman splitting between the "up" and "down" spin states and, thus, defines a preferred orientation whenever there is a tie. Let us assume the direction of this field is such that the "up" spin state is favored. Therefore, if any one of the two inputs is at logic level 1, then the output will also be at logic level 1.

We have now realized the truth table shown in Fig. 2. It is easy to verify that this is a NAND gate. The NAND gate can be converted to an AND gate by directing the output of the NAND gate through an inverter. (Any two neighboring cells constitute an inverter because of the antiferromagnetic ordering.) This requires four cells in a non-linear chain as shown. The two extreme cells are the input ports. The one off-line is the output port. The spin orientations in the various cells for various combinations of inputs are shown in Fig. 2 (b). This diagram (which is essentially the "truth table") verifies that this system is an AND gate. (If the direction of the external magnetic field is reversed so that the "downspin" state is favored instead of the "upspin" state, then the same array realizes a NOR gate instead of a NAND gate.)

## Combinational and sequential circuits

A digital computer is required to perform only two basic types of functions: logic operations and memory storage. Logic operations are achieved through combinational digital systems (consisting of logic gates). Random access memory (RAM) can be realized through sequential digital systems. In the following example, we show the design of the most basic combinational digital system used in an arithmetic logic unit. It is the binary half adder.

In a half adder, if $A$ and $B$ are two binary addends, $S$ the sum, $D$ the digit indicating the last digit of the sum and $C$ the carry, then $D$ is the exclusive OR function of $A$ and $B$ (i.e. $D = (A\ B)(AB)$) while $C$ is the AND function of $A$ and $B$. The conventional realization of a half adder is shown in Fig. 3 (a). The actual realization with single electron cells is shown in Fig. 3 (b). In a similar fashion, one can construct code converters, parity checkers, parity encoders, multiplexers, and so forth.

## Problems and pitfalls

There are a few hidden pitfalls in all of this which may not be obvious. Consider two inverters (NOT gates) in a series as shown in Fig. 4. The steady-state situation is shown in the top figure where the output of each inverter is the logic complement of the input. Now, if the logic state at the input of the first inverter (node $A$) is changed from 1 to 0, will the logic state at the output (node $B$) change from 0 to 1 ?

One would hope so, but it is neither automatic nor obvious. Immediately after the switching of node $A$, node $B$ sees node $A$ telling it to change from 0 to 1, while node $C$, which is still at 0, is telling it to stay put. Who does node $A$ listen to?

If it listens to node $C$ (i.e. if the influence from the right is stronger than from the left), then it will not switch. In fact, it will ultimately make node $A$ switch back to 1. This is a catastrophic failure. It also is an example of reflection, or a failure of the logic signal to propagate unidirectionally.

To make sure this does not happen, there must be a non-reciprocal element constituting the inverter. Such an element will allow a signal (or influence) to propagate unidirectionally from left to right (but not from right to left). This way each stage drives its next stage, rather than the reverse.

In conventional circuits, this non-reciprocal element is a transistor. No wonder that all conventional logic families (RTL, DTL, TTL, IIL, ECL, etc.) require a transistor; one cannot make logic circuits with simple passive elements such as resistors, capacitors and inductors which do not provide non-reciprocity.

The spin polarized single electron scheme does not have inherent non-reciprocity. That is, how spin *A* interacts with spin *B* is no different from how spin *B* interacts with spin *A*. The interaction (like most interactions between electrons, including the Coulomb interaction) is completely reciprocal. Therefore, there is a problem.

An appropriate solution to this problem that ensures unidirection signal propagation between the input and output is shown in Fig. 5 (c). Unfortunately, this solution, which requires continuously varying the separation between adjacent cells, limits the size of the system. Varying the inter-cellular separations however cannot be carried on indefinitely. This is because increasing the separation also decreases the strength of the spin-spin coupling. Therefore, the number of cells (the primitive bistable devices) that can be used in a chip is limited.

The size limitation is also an inevitable consequence of "ground state computing." Since external input is provided only to selected cells (input ports) and this drives the computation (which requires at least an energy dissipation of $kTln2$ per switching event to have any noise margin), the amount of energy needed is at least $(M/N)kTln2$ ($M$ = number of cells and $N$ = the number of input ports). Assuming that $N = 10$ and that the maximum energy that can be provided as input to a single cell is limited by the energy required to add another electron to the cell ($\sim q^2/C$; $C$ = capacitance of the cell), we obtain a value of $M = 890$ at room temperature and 3,400 at 77 K if $C = 10^{-19}$ F.

Taking all these aspects into consideration, ultimately the optimum choice probably will be a hybrid chip. It will contain discrete modules of quantum circuits, each having possibly about 1 Kbit capacity, connected by classical interconnects. Each module will be extremely fast and dense. Such a "semi-classical" hybrid chip with quantum coupled modules (QM) interacting classically is schematically depicted in Fig. 6. Such a concept synthesizes the best of both worlds—classical and quantum.

## Read more about it


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Supriyo Bandyopadhyay obtained a B. Tech from the Indian Institute of Technology, Kharagpur, India, in 1980, an M.S. in EE in 1982 and a Ph.D. in EE from Purdue University in 1985.

He is now an Associate Professor at the Department of Electrical Engineering at the University of Notre Dame. He has authored and co-authored more than 150 articles in nanoelectronics, optics and superconductivity.

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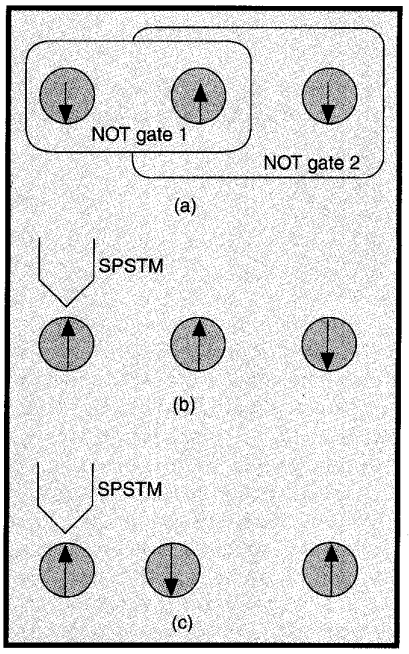


***Fig. 5 An example of failure due to lack of unidirectional isolation.***

*(a) The equilibrium configuration of electron spins (logic states) in two NOT gates in series. (b) The logic state at the input of the first NOT gate is changed by an SPSTM (external source), but the output does not change in response. This is because the central cell is in a logic indeterminate state just after the arrival of the input. If the external magnetic field favors upspin, then the central cell's polarization does not flip and output remains unchanged. Finally, the input will flip back to its original state after the SPSTM is removed. (c) A possible solution. The left cell (input port) is placed closer to the central cell than the right cell (output port). Now the input port has dominant sway and drives the output rather than the reverse.*

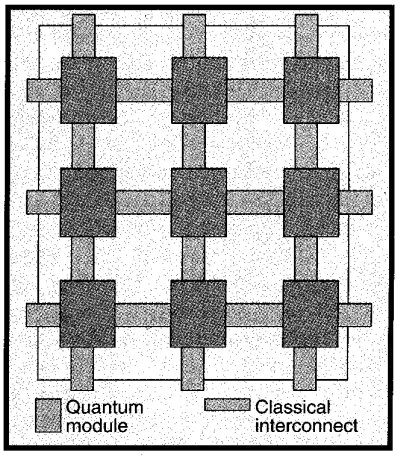


***Fig. 6 A "semi-classical" chip of quantum modules connected classically.***