

Nanoelectronic Architecture for Boolean Logic

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A nanoelectronic implementation of Boolean logic circuits is described where logic functionality is realized through charge interactions between metallic dots self-assembled on the surface of a double-barrier resonant tunneling diode (RTD) structure. The primitive computational cell in this architecture consists of a number of dots with nearest neighbor (resistive) interconnections. Specific logic functionality is provided by appropriate rectifying connections between cells. We show how basic logic gates, leading to combinational and sequential circuits, can be realized in this architecture. Additionally, architectural issues including directionality, fault tolerance, and power dissipation are discussed. Estimates based on the current-voltage characteristics of RTD's and the capacitance and resistance values of the interdot connections indicate that static power dissipation as small as 0.1 nW/gate and switching delay as small as a few picoseconds can be expected. We also present a strategy for fabricating/synthesizing such systems using chemical self-organizing/self-assembly phenomena. The proposed synthesis procedure utilizes several chemical self-assembly techniques which have been demonstrated recently, including self-assembly of uniform arrays of close-packed metallic dots with nanometer diameters, controlled resistive linking of nearest neighbor dots with conjugated organic molecules and organic rectifiers.

I. INTRODUCTION

It is generally accepted in the solid-state community that conventional strategies for integrating electronic devices on a chip will not be suitable for nanometer-sized elements because of the minuscule size of the elements and the corresponding low power handling capacity, low gain, and low fanout. Accordingly, a number of proposals have appeared in the literature that envision novel architectures for nanoelectronic logic circuits. Most of these schemes purport to exploit discrete (single- or few-electron) charge inter-

actions between semiconductor or metallic dots [1]–[10]. Unfortunately, they all suffer from one or more drawbacks. References [3] and [4] propose a paradigm which is plagued by problems associated with unavoidable and ubiquitous background charge fluctuations that make the circuits error prone, [5] requires precise clocking control and lacks sufficient fault tolerance, while [7]–[9] proposes a system that is difficult to fabricate. References [1] and [2]¹ suffer from all the problems associated with [3]–[9] and additionally raise a serious concern in that logic signal cannot propagate unidirectionally from the input to output since the input is linked to the output by Coulomb interaction which is bidirectional (reciprocal). Bidirectional flow of signal does not distinguish between input and output terminals [7]–[15]. There are additional problems in this paradigm such as the lack of isolation between input and output and the problem of unbalanced logic gates which tends to generate wrong answers for certain configurations of gates [16].

In this paper, we propose and demonstrate a novel paradigm for nanoelectronic implementation of Boolean logic that can potentially eliminate the above drawbacks. In this implementation, each computational cell contains nanoscale metallic dots formed into regimented, two-dimensional (2-D) arrays on an active substrate which possesses a non-linear, nonmonotone current-voltage characteristic. Logic functionality is achieved through charge exchange between the metallic dots. In order to demonstrate the feasibility of making these circuits, we also outline a fabrication strategy which exploits chemical self-assembly/self-organization techniques to realize the nanoscale elements and the interelement connections. It appears that all of the individual components of the enabling technology have already been demonstrated and what remains to be achieved is the combination of these components to synthesize the circuits described in this paper. While this is certainly a nontrivial task, it seems that proof of concept demonstra-

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¹This scheme lacks unidirectionality and does not work (see [7]–[15] for a discussion of this issue). Recent modifications of this scheme, whereby each cell is accessed and clocked individually to realize adiabatic switching, provides unidirectionality but results in exceedingly slow speed. There is still the lack of isolation between input and output. Furthermore, it is not clear how “logically irreversible” gates described in this paradigm can be switched adiabatically.

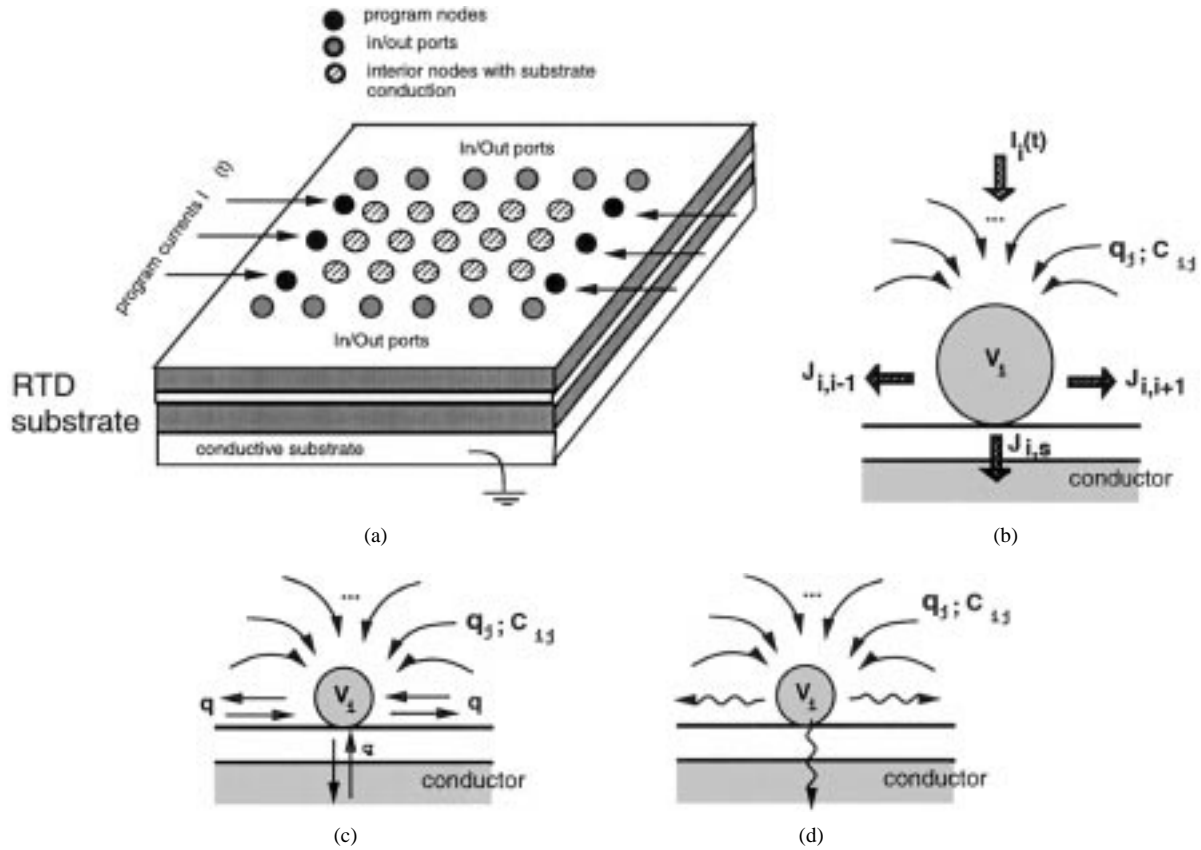


Fig. 1. (a) A generic array of metallic islands deposited on a nonohmic layer which has been grown on a conductive substrate. It is assumed that all islands have direct conductive links to nearest neighbors. A subset of the islands serve as program nodes which are driven by external current sources. Another subset of islands serve as input/output ports, and the remaining islands introduce complexity to the system through nonlinear conductive links to the substrate. The substrate nonlinearity could arise, for example, from resonant tunneling which causes the substrate current–voltage characteristic to have a *nonmonotonicity*. (b)–(d) Cross-sectional view showing island i , whose potential v_i is influenced by the charges q_j in the rest of the network through a capacitance matrix. The different transport mechanisms lead to a rich variety of computational capabilities.

tions of nanoscale computational cells using the proposed architecture will be possible in the relatively near future.

This paper is organized as follows. In Section II, we describe the paradigm, and present theoretical and simulation results to demonstrate the functioning of the logic gates. The rest of the sections are devoted to describing possible routes to fabrication.

II. ARCHITECTURE: ARRAY OF QUANTUM DOTS ON A RESONANT TUNNELING DIODE

A. Basic Computing Block: Background and Motivation

The basic computational block for our logic scheme can be realized by assembling a 2-D periodic array of nanometer-sized metallic islands with resistive nearest neighbor interconnections, on a substrate whose current–voltage characteristic has a *nonmonotonic* nonlinearity. The simplest choice for the substrate is a resonant tunneling diode (RTD). This system is shown in Fig. 1(a). All our circuits utilize this basic structure.

We have already shown that different types of transport nonlinearities in the interdot connections can lead to a wide

variety of global activities in this system; moreover, it is possible to impart computational interpretations to these activities [14], [17]. Additionally, we have shown that within a classical circuit theoretic model (where electric charge is considered a continuous variable), nonmonotone nonlinearities of the substrate conduction can yield global associative memory effects and lead to image processing capabilities [10], [14], [17]. We have also shown that this interpretation remains valid even when granularity of charge (or single-electron effects) come into play, provided that the effective capacitance of the islands is not too small. Finally, we have investigated networks of islands in which the sole nonlinearity in charge transport arises from single-electronics (Coulomb blockade), rather than any inherent nonlinearity in the molecular wires or substrate conduction. These networks exhibit associative memory effects, as well as the ability to yield approximate solutions to certain NP-complete optimization problems such as the traveling salesman problem [10], [17].

Our past work has shown that the functionality of these networks is determined by the type and versatility of the interconnects. Increased functionality can be achieved at

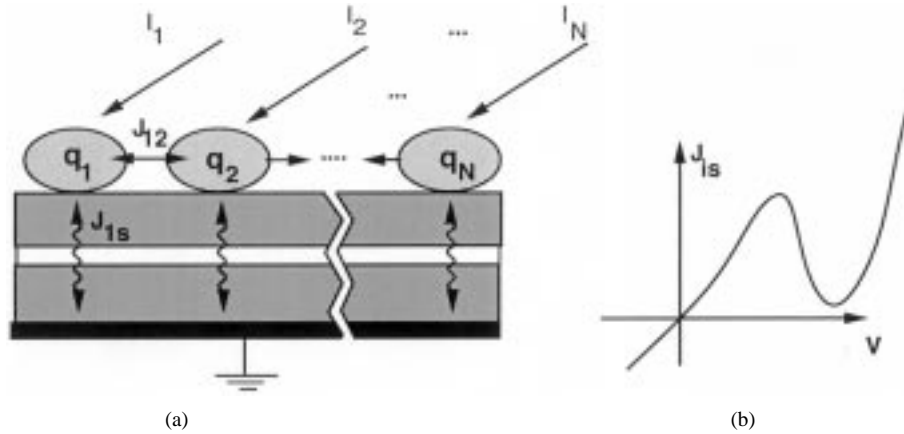


Fig. 2. (a) A 1-D array of islands, whose dynamics is described by (1). (b) A nonmonotone substrate nonlinearity of the kind shown here, is the minimal condition for the realization of collective effects.

the cost of a commensurate increase in the fabrication complexity involved in realizing the underlying networks. Hence, a natural question to ask is: what are the minimal requirements that the lateral interconnects must satisfy so that the underlying computational unit displays useful computational properties?

In this paper, we provide an answer to the above question, and show that the architecture shown in Fig. 1 can realize basic logic functions such as AND gates, OR gates, and multilevel circuits comprising these gates using the simplest of interconnects. We need just nearest-neighbor resistive links, and at certain prespecified locations that demarcate gate boundaries, we need rectifying or diode links.

B. Bistability

In order to make logic gates and circuits, one first needs to demonstrate a bistable device, i.e., a device that is capable of assuming only two possible stable states, one of which can be interpreted as a binary 0 and the other as a binary 1. We shall show later that a bistable device by itself is not sufficient for realizing logic circuits (one also needs to impose “unidirectionality,” a issue that is addressed later in this paper), but bistability is a necessary ingredient. In this section, we demonstrate how bistable devices can be generated using the computational prototype described in Fig. 1.

1) *Networks with Multiple Stable States:* First consider a simple one-dimensional (1-D) version of the network, as shown in Fig. 2. Here we designate the current between islands i and j as J_{ij} , and the current between island i and the grounded substrate as J_{is} . We can then write from Kirchoff’s current balance condition that,

$$\begin{aligned} \frac{d}{dt} q_i &= C_i \frac{d}{dt} v_i \\ &= - \left[J_{is}(v_i) + \sum_{j \neq i} J_{ij}(v_i - v_j) \right] + I_i(t) \quad (1) \end{aligned}$$

where $I_i(t)$ is the driving current, q_i is the charge, v_i is the potential, and C_i is the capacitance, with the subscript i indicating the relevant island.

Qualitatively, the multiple solutions to the nonlinear system of equations which results from (1) under steady-state conditions (i.e., $dv_i/dt = 0$ for all i) will be taken as a set of memory states (or equilibrium points) which can be programmed by properly choosing the current biases I_i , and the transport functions J_{ij} and J_{is} . The current biases I_i will be assumed to be either time independent, or slowly varying on time scales over which the network relaxes into its memory states. If the network is begun at time $t = 0$, with a certain initial condition $v_i = q_i/C_i$ for all i , arranged, for instance, by an initial impulse of charges q_i at each of the islands, then the network will evolve toward the closest memory state, as programmed by the current biases I_i .

In [14], [17], we demonstrated two important properties of this network: 1) it is globally stable and 2) the non-monotonic nonlinearity causes *multiple* (more than one) equilibrium points. The number of equilibrium points can be programmed by appropriate choice of the inter-island resistances. For binary logic, we need only *two* equilibrium points.

We next provide numerical results for multiple equilibrium points that can be observed in our networks by making different choices of J_{ij} ’s and J_{is} ’s. Our example, based on two dots, is illustrated in Fig. 3(a), in which the two islands are coupled with each other through a linear resistor R_{12} and a capacitor C . In addition, we assume that each island is *individually* coupled to the substrate through a capacitance C_0 , and a nonlinear resistor whose nonmonotonic current-voltage characteristic is shown in Fig. 3(b). This characteristic approximates that of a RTD. Since the results presented here are numerical in nature, we have minimized the number of parameters by choosing a piecewise linear function for the characteristic, in which each of the three

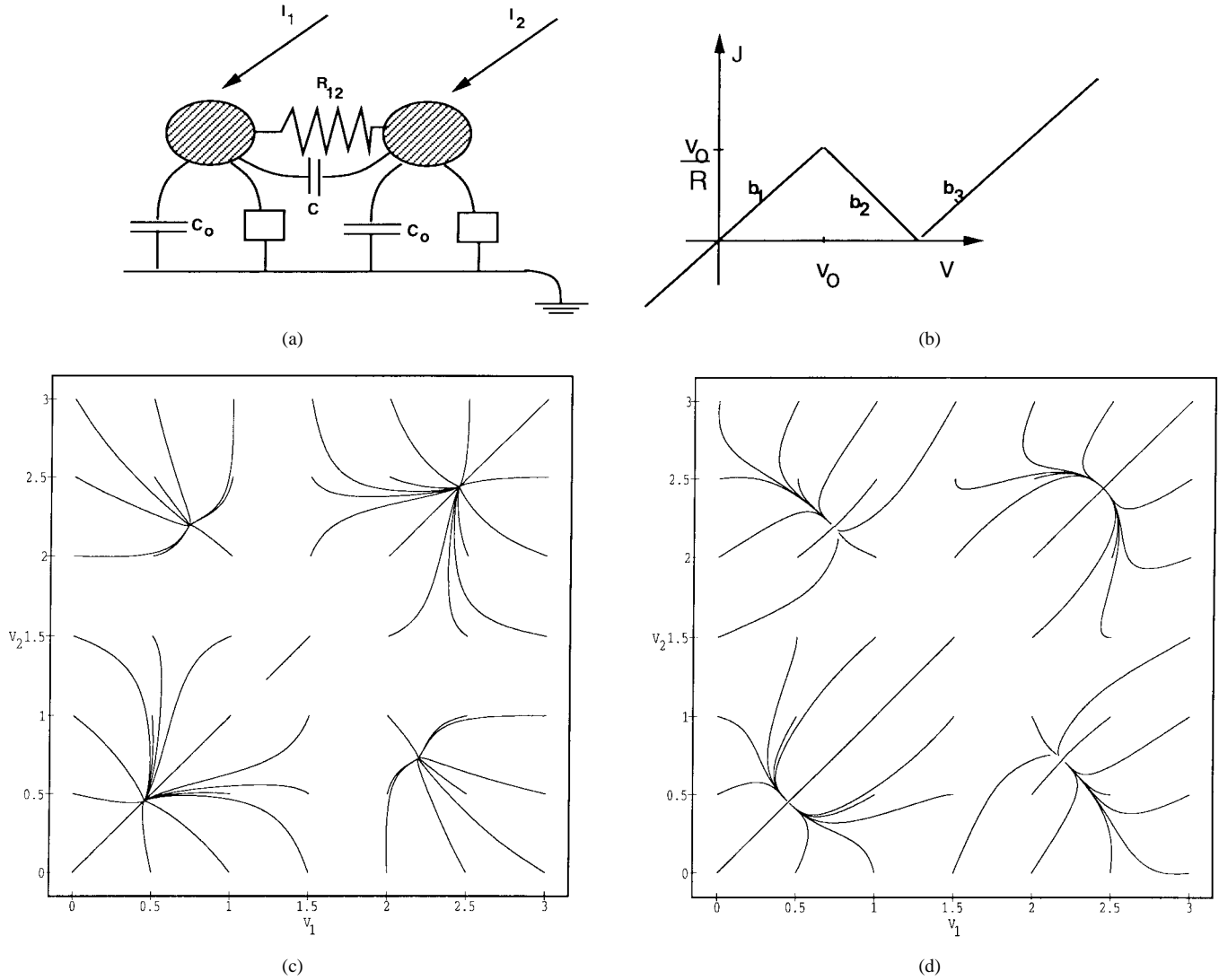


Fig. 3. (a) A network of two islands that are laterally coupled via a linear resistance R_{12} and a capacitance C . Each island is also coupled vertically to the substrate via a capacitance C_0 , and a nonlinear resistive element. (b) The substrate nonlinearity is modeled as a piecewise linear function. We can show theoretically that more realistic nonlinearities due to resonant tunneling, for example, will yield qualitatively the same dynamics as generated by this nonlinearity. The three segments of the function are denoted by b_1 , b_2 , and b_3 . The other two figures show the phase portrait for two-island system in the continuous-charge model, in which the voltage axes have been scaled with respect to v_0 . The parameters are $R_{12} = 5R$, and $I_0 = v_0/2R$. (c) With only substrate capacitance $C_0 = 1$, and (d) with identical mutual and substrate capacitances: $C = C_0$.

segments have slopes of the same magnitude $1/R$

$$J_s(v) = \begin{cases} \frac{v}{R} & v < v_0 \\ \frac{2v_0 - v}{R} & v_0 \leq v \leq 2v_0 \\ \frac{v - 2v_0}{R} & v > 2v_0. \end{cases} \quad (2)$$

The equilibrium points of this two-node system can be found by setting $\dot{v}_1 = \dot{v}_2 = 0$, and the stability properties of those equilibrium points can be ascertained by examining the eigenvalues of the system matrix near the equilibrium points [18], [19]. Provided that the driving current $I_0 < v_0/R$, each island potential can in principle be on any

one of the three branches of the nonlinear function $J_s(v)$ shown in Fig. 3(b). We can, however, show that the system will be unstable if either island is operated on branch b_2 which has a negative differential resistance. So, it follows that this system can have at most four different globally stable points, since each island is restricted to being on either branch b_1 or b_3 . Two of these stable points are trivial ones corresponding to both islands operating on the same branch: either b_1 or b_3 . We have determined a necessary and sufficient condition for the existence of all four “memories,” and the corresponding phase portraits are shown in Fig. 3. The figure shows that if the interdot resistance (R_{12}) is large enough, then all the four possible equilibrium points are stable. In that case, this system can be used as an associative memory.

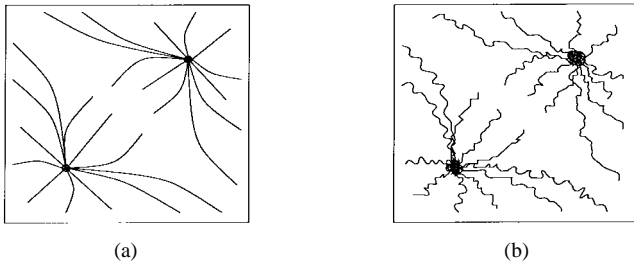


Fig. 4. (a) The phase portrait of the two-island system shown in Fig. 3, when the inter-island resistance is small, e.g., $R_{12} \leq R$. The whole system now behaves as a bistable device with only two stable states. (b) The phase portrait of the same system when single-electron effects and Coulomb blockade are taken into consideration.

2) *Networks with Two Stable States:* Now, if instead of an associative memory application with multiple stable states, one needs a device for binary logic functions, then we have to demonstrate the existence of only two stable points. We consider the same two-island example as described in (2) and Fig. 3. However, instead of choosing a large interdot resistance (i.e., $R_{12} = 5R$), we choose a small interdot resistance (e.g., $R_{12} = R$). Our analysis and simulations (see Fig. 4) show that with small inter-island resistance, instead of having four stable points, the two-node system will have exactly two stable states. These two stable states correspond to the voltages on both islands being on branch b_1 or branch b_3 .

In general, one can consider any large network comprising a collection of n islands [as depicted in Fig. 2 and characterized by (1)] and show that the whole network behaves as a single bistable device when the lateral interconnects have small enough resistances. A proof of this statement follows easily from the preceding analysis of the two-island case, and will be skipped here.

3) *Limits to Continuous Models—Single-Electron Effects:* We now study the same networks, with the assumption that single electron effects have become pertinent either due to the lowering of temperature, or due to the physical scaling of the metallic islands down to $d \sim 10$ nm. Single-electron effects will become relevant when the inter-island resistances exceed \hbar/e^2 (≈ 12 k Ω) and when the change in potential $\delta V = q/C$, associated with the addition of a single charge q to an island, becomes comparable to kT/q , the thermal potential. The latter condition can be met even at room temperature if islands with an effective capacitance smaller than $C \approx 5 \times 10^{-18}$ F are fabricated. In fact, as described in the experimental section of this paper, we have already observed room temperature single-electron effects in the quantum-dot arrays that we have synthesized [20], [21].

Single electron dynamics are characterized by discrete tunnel events, and differential equation systems cannot be used to model the arrays. We have developed a Monte Carlo simulation technique [22], [23] for the simulation of a current biased network of islands shown in Fig. 2(a). This simulator has been described in [17]. The results obtained from this simulator show the following features [see also

Fig. 4(b)]: For large enough values of the effective substrate capacitances (C_0), the effect of the single electron dynamics is marginal and the system is adequately described by the continuous charge models. Thus, even arrays of metallic islands with diameters of few nanometers can exhibit the same associative memory and bistability properties studied in the context of continuous dynamics.

C. Networks for Logic Gates and Functions

The preceding discussions clearly show how a collection of resistively coupled quantum dots with an RTD substrate, can behave as a single bistable device. For the purposes of this section, we shall represent the computational structures described in Figs. 1(a) and 2(a), simply as an array of dots; it will be assumed that the quantum dots are laterally connected by sufficiently low-impedance links, and that there is an RTD substrate underneath the array. The results presented in this section are based on the outputs of the simulators that we have developed for solving the continuous-time (1), as well as, based on the Monte Carlo simulator designed to study the behavior of the networks under single-electron dynamics.

Given such an array, an implementation of a logical OR gate is demonstrated in Fig. 5. We will assume “positive logic” so that the high voltage state corresponds to logic level 1 and the low voltage to logic level 0. The diodes at the boundary provide isolation between the two inputs A and B . The whole array is initialized to a 0 state, and if any of the inputs is a 1 then the array switches its state from a 0 state to 1. An analogous realization of an AND gate is shown in Fig. 6.

An example of the realization of a two-level OR/AND circuit is shown Fig. 7. The figure shows the results of our numerical simulations and establishes how the individual gates can be integrated into realizing Boolean circuits. The first level of the circuit shown in Fig. 7 consists of two 2-input OR gates. In the first step, the OR gates are allowed to operate while the AND gate in the second stage is disabled. Next, the AND gate is enabled by a *clock* pulse and the two OR gates drive the AND gate. Multilayered logic circuits can be also realized by propagating the signals stage by stage. That is, successive levels or stages of the circuit are activate sequentially allowing the signal to propagate from the input to the output of the circuit.

Note that we have not provided a realization of an inverter (or a NOT gate) in our scheme. That is because, without loss of generality, we can assume that for every binary input A , its inverted value \bar{A} is also available as an input. This is the usual assumption made in many currently available schemes for logic implementations, such as the programmable logic arrays (PLA’s), where all the variables and their complements are available as inputs. The inversion of the inputs can be also done at the boundaries of our computational block using nanoscale single electron transistors (SET’s). It can be easily shown from the basic principles of Boolean logic that if input variables and their complements are available, then a two-level OR/AND circuit is universal.

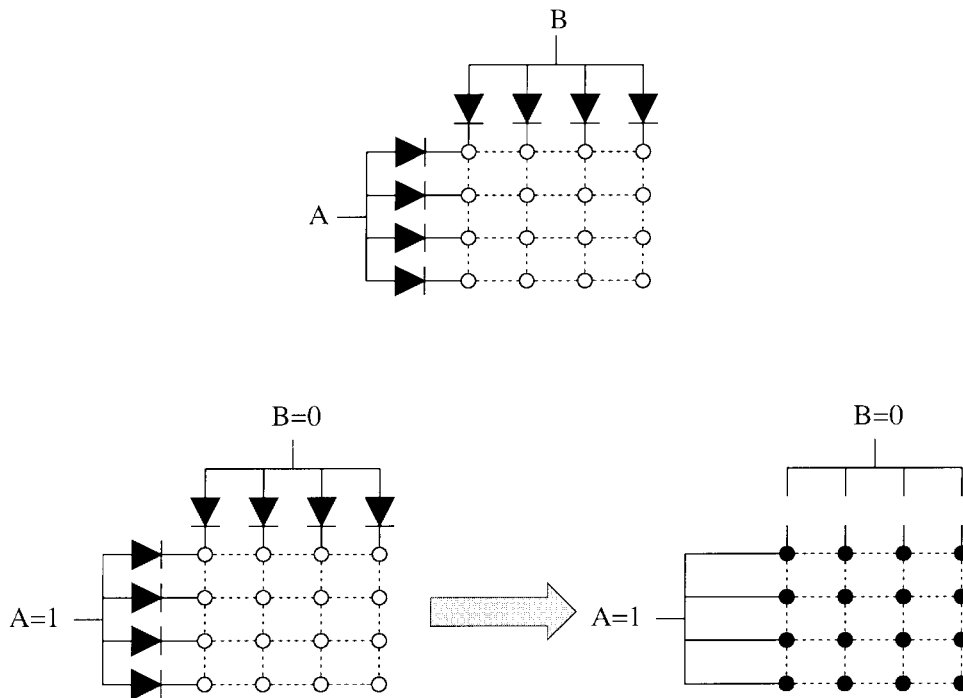


Fig. 5. A schematic description of the realization of a two-input OR gate using arrays of metallic dots deposited on a nonohmic layer. The metallic dots are interconnected with each other by resistive links, and to the inputs by *rectifier* (or *diode*) links. The computation starts by initializing the individual dots to a *low* state, and if any of the inputs is a logical 1, then all the dots will switch to a *high* state (represented by ●).

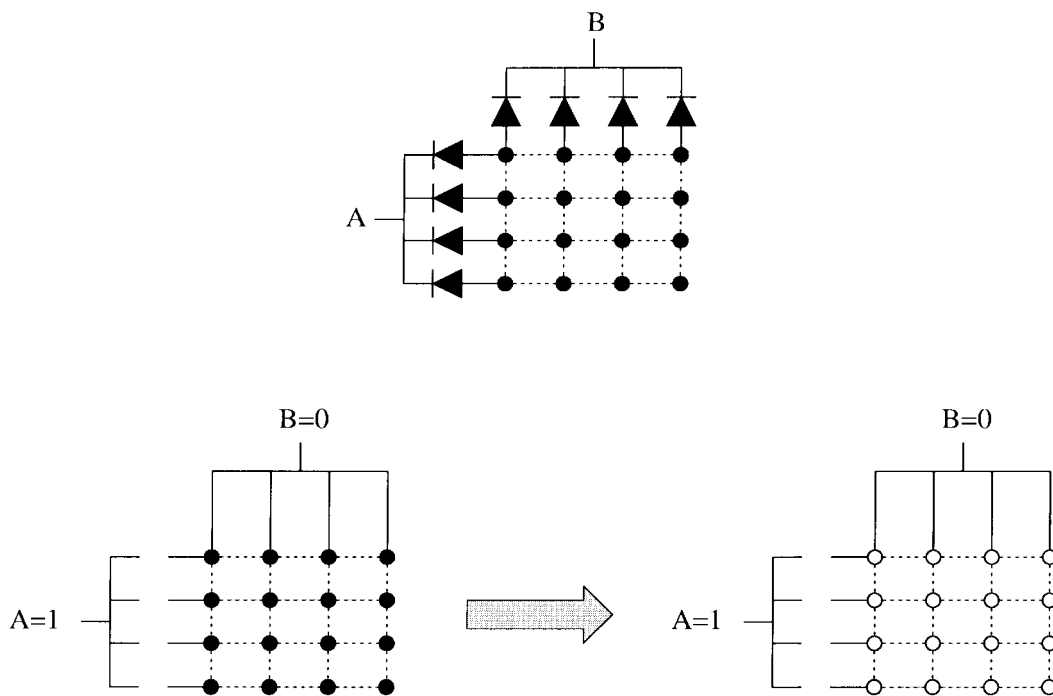


Fig. 6. A schematic description of the realization of a two-input AND gate using arrays of metallic dots deposited on a nonohmic layer. The metallic dots are interconnected with each other by resistive links, and to the inputs by *rectifier* (or *diode*) links. The computation starts by initializing the individual dots to a *high* state, and if any of the inputs is a logical 0, then all the dots will switch to a *low* state.

D. Basic Architectural Issues

In this section, we highlight several architectural issues involved in the scheme that we have developed.

1) *Unidirectionality and Pipelining:* As described in the introduction, a major drawback of the proposals for logic implementations based on bistable devices without direc-

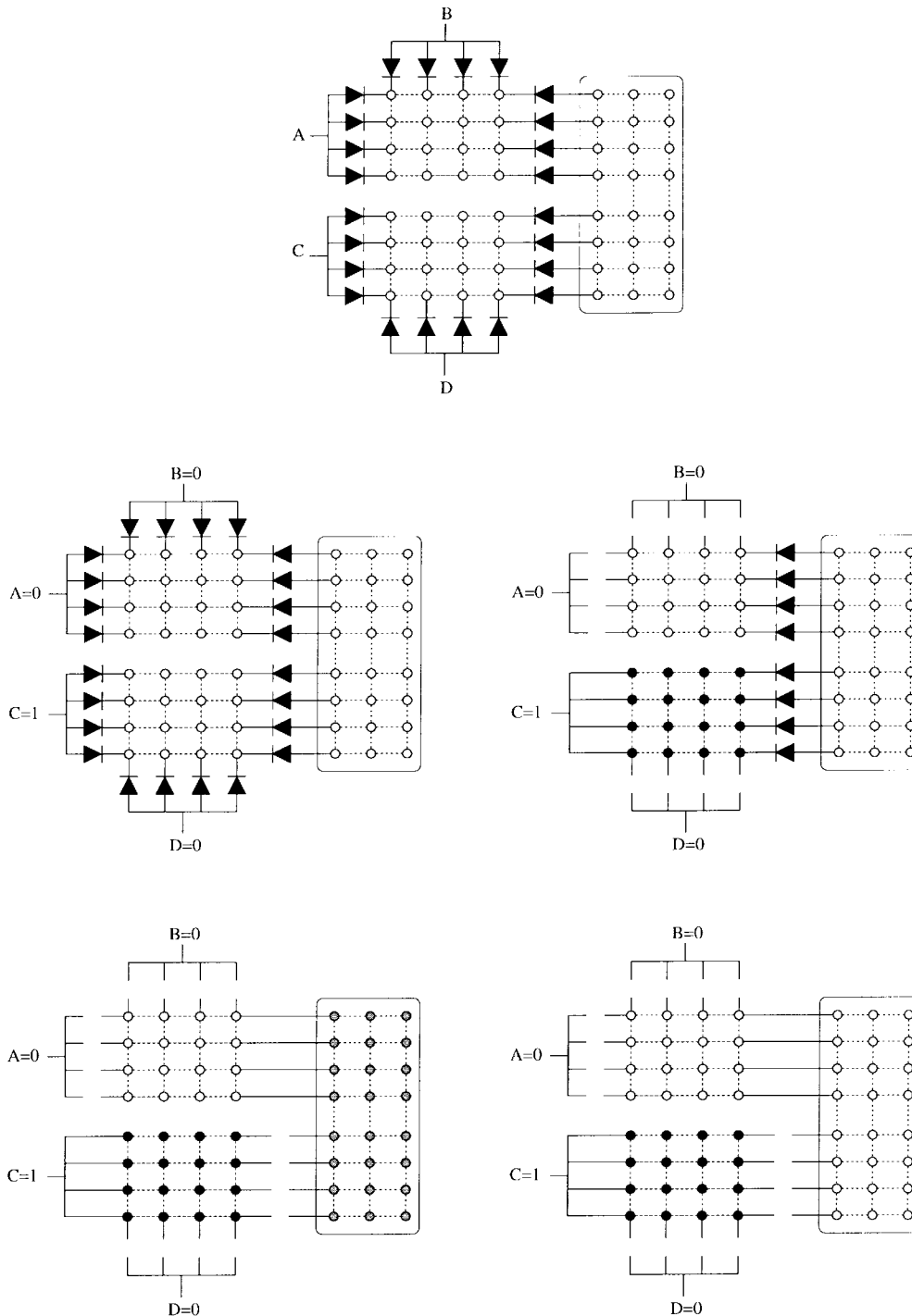


Fig. 7. A schematic description of the realization of a two-level OR/AND circuit using arrays of metallic clusters deposited on a nonohmic layer. Rectifier (or diode) links delineate gate boundaries. The computation starts by initializing all the individual dots to a *low* state. This allows the OR gates to complete their respective computations. This step is followed by an initialization of the AND part of the array to a *high* state. The final state of the AND part will be determined by the already computed states of the OR gates.

tionality [1] lies in their failure to ensure propagation of the logic signal from the input to the output. That is, if two bistable devices are connected together in series, then the one closer to the input terminal should drive the other, and not the other way around. This will ensure that the signals propagate from the input to the outputs and the

whole system does not get stuck in metastable states [12], [13], [15].

As illustrated in Fig. 7, in our scheme, unidirectional signal propagation from the input to the output is effected through a *clocking mechanism*. For example, when the OR gates in the first layer are operational, the AND gate

in the succeeding stage is disabled. Once the OR gates have reached stable states, then a clock pulse is applied to initialize the AND gate. This scheme avoids the potential problem of the AND gate acting as an input to the OR gates, and instead allows the OR gates to drive the AND gate. The same strategy can be extended to the case of multi-level circuits. Such a scheme of multiphase clocking (“push-clock” and “drop-clock”) is also used in conventional charge-coupled devices (CCD’s) [24].

Moreover, the multiphase clocking scheme will enable *pipelining* in our computational blocks. That is, every other level in a multilevel circuit can operate simultaneously, and a new set of inputs can be fed to the circuit every other clock cycle. This allows the implementation of a high throughput logic block.

2) *Fault Tolerance*: Any computational architecture at the nanoscale level should display inherent fault-tolerant properties [12], [13]. Nanostructure devices will probably have more variability in their characteristics than their earlier generation microstructure counterparts. Any scheme that ignores this fact and relies on every quantum dot being perfect will almost inevitably be impractical.

In order to ensure fault-tolerance in our scheme, we allow a cluster of islands to represent a gate rather than a single or just a few dots. Note that the size of the arrays for each gate (as shown in Figs. 5 and 6) can be varied depending on the state of the technology. By providing larger arrays one can increase fault tolerance. We have done extensive simulations of the two-level OR/AND circuit shown in Fig. 7 under different fault conditions. For example, our simulations show that the operation of the circuit remains unimpaired even if up to 15% of the dots fail. Similar behavior holds even if the sizes of the dots are varied up to 100%.

3) *Power Dissipation and Density Issues*: Given the high circuit density of the proposed computational architecture, it is important to consider the power dissipation of the cells. While dynamic power simulations are not available at this time, the static power dissipation can be estimated from the stable current and voltage states. For the case with optimally chosen current bias to each node, the static current level for both stable states of each island will be approximately the valley current level of the RTD mesas; the corresponding voltage levels will be approximately the valley voltage and zero voltage for the high and low voltage states, respectively. For a cell containing 5 nm diameter islands, the static power dissipated in the high voltage state is approximately 0.1 nW per island, while the static power in the low voltage state is approximately zero. This calculation assumes a peak current density of 10^4 A/cm², a peak to valley current ratio of 10:1 and a valley voltage of 0.5 V, all consistent with RTD performance reported in the literature. A computational cell containing 100 islands would therefore dissipate 10 nW and would occupy about 1×10^{-10} cm². To a first approximation, only half of the computational cells will be biased at a given time and only half of the nanoscale islands in the active cells will be in the high voltage state. Therefore, the static power dissipation is

estimated to be 25 W/cm² for a computational circuit with 1×10^{10} cells per cm².

For comparison, projected values for silicon CMOS circuits in the year 2007 are a dissipation of 600 nW per computational cell (logic gate) with a cell density of 5×10^7 cells/cm², corresponding to 30 W/cm² [25]. The CMOS power is primarily dynamic power, so detailed comparisons to the static predictions of the proposed architecture are probably not appropriate. However, the power estimations indicate that the proposed architecture has the potential for significantly reduced power dissipation per cell and comparable power densities, along with the potential for realizing higher functionality per cell and much higher cell densities.

We can also estimate an upper limit for the dynamic energy dissipation during a logic signal swing. This energy is $\sim CV^2$ where C is the capacitance of an island and V is the power supply voltage. Assuming $C = 1$ aF and $V = 1$ V, the energy dissipation (or power-delay product) is 10^{-18} J.

The switching delay is $\sim R_{\text{link}}(C_{\text{sub}} + C_{\text{island}} + C_{\text{link}})$ where R_{link} is the resistance of the interdot resistive link, C_{sub} is the substrate capacitance associated with the RTD’s, C_{link} is the capacitance between nearest neighbor dots, and C_{island} is the capacitance of the metallic island. Assuming that the value of R_{link} is 1 M Ω , a value consistent with the interdot resistances of metal dot arrays described in the next section [21], and all capacitances are on the order of 1 aF, we obtain a switching delay of 3 ps. Therefore, the dynamic power dissipated is about 300 nW per island. However, one should remember that this is an upper limit. Heat-sinking of 1000 W/cm² from a silicon chip was demonstrated more than 15 years ago [26].

III. NANOSCALE FABRICATION

There are several key components required to fabricate computational cells of the proposed architecture, including definition and interconnection of the cell core, i.e., the area covered by a uniform array of metallic nodes, the rectifying interconnects which connect adjacent cell cores and the bias/clocking circuitry. This section provides a brief overview of synthesis techniques that could be employed to realize the required components and interconnections. The basic cell configuration will be briefly reviewed and the requirements for fabricating a logic element using this topology will be discussed.

It should be noted that one of the attractive features of the proposed architecture is its compatibility with fabrication techniques of the type described in this section. In this case, local interconnects between the nanometer scale elements can be uniform resistive links, i.e., it is not necessary to provide arbitrary interconnection paths at the level of the smallest circuit nodes. This feature can be realized with self-organized or self-assembled networks, which can be formed with a relatively high throughput and relatively low cost. The internal connections to each nanometer scale element in the computational cores consist of a bias current

line and a load with a nonmonotone, nonlinear current-voltage relationship. These elements provide a voltage bistability for each element, as well as the power required to switch. The specific functionality of the circuit comes from the intercell interconnections. Since these interconnections can be at larger scales than the nanometer scale nodes, it should be feasible to use lithographic techniques for their delineation and this can provide more arbitrary interconnections.

Since the architecture is intended to be scalable to nanometer dimensions, the underlying assumption of this discussion is that the individual metallic nodes will have dimensions in the range of 5–20 nm and that the computational cells will have dimensions (lengths and widths) in the range of 20–200 nm. The minimum feature sizes are well below those employed in conventional silicon circuits. While the small areas of computational cells would result in very large circuit densities (potentially approaching 1 T gates/cm²), realization of circuits at this scale will require a significant shift in fabrication techniques from those used in conventional silicon processing. Conventional lithographic techniques, including capabilities such as electron beam lithography, might be capable of patterning at the scale of the (larger) cell regions but would not be practical for defining the individual metallic nodes which are much smaller. In contrast, chemical self-assembly or self-organizing techniques, i.e., techniques which exploit chemical affinities rather than lithographic techniques to arrange clusters or molecules, have been developed which can provide highly organized structures with minimum sizes and spacings on the order of 2–10 nm. While these techniques can provide uniform arrays of molecules or metallic islands, they do not appear to be capable of spontaneously forming specific nonuniform patterns or arbitrary interconnect configurations. The fabrication techniques best suited for realizing the structures required for the proposed computational cells will likely be a combination of chemical self-assembly techniques, to realize the networks of nanoscale metallic nodes within a computational cell, and lithographic techniques to define the cells and interconnect structures.

An equivalent circuit representing a 1-D slice through two computational cells is shown in Fig. 8. Each computational cell contains a number of nanoscale metallic nodes, as illustrated in the figure. Adjacent nodes within the cell are coupled resistively via intracell resistances (R_1), as well as capacitively via C_1 . Each nanoscale node is connected to an active element, labeled “RTD” in the figure, which provide the required nonmonotone nonlinearity. The intercell diode connections are configured to realize specific logic functions. Each cell core is biased through a clock electrode; two or more clock phases are required to provide unidirectional propagation of logic signals. When enabled, the clock lines provide the bias voltage to the nanoscale nodes within a given cell. The bias resistance, R_{bias} can be realized through a thin-film resistive layer.

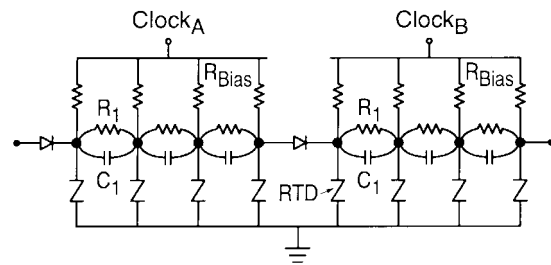


Fig. 8. Circuit schematic corresponding to a 1-D slice through adjacent computational cells. Indicated elements include nodes representing nanoscale metallic islands, bias resistors, bias/clock electrodes, elements with nonlinear nonmonotone current-voltage (provided by semiconductor mesas and labeled as RTD), and intercell rectifying links.

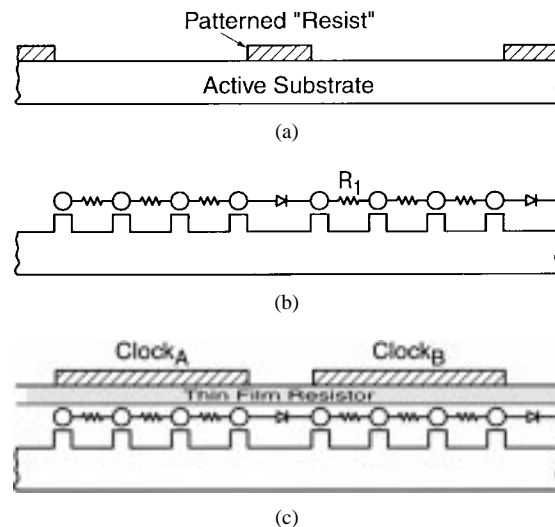


Fig. 9. Cross-sectional view of major steps in fabrication sequence for computational cells. (a) Lithographic patterning of regions in which computational cell cores will be deposited. (b) Self-organized deposition of arrays of nanometer scale metallic islands in patterned core regions. Internode resistive linking and patterning of semiconductor mesas, realized by chemical self-assembly and etching using metallic islands as “natural” masks, respectively, are also shown. (c) Deposition of thin film resistor layer for bias resistance and bias/clock electrodes for each cell, in regions defined by lithographic patterning.

A general synthesis approach can be formulated, based on self-organization and lithography techniques described later. The major steps in the synthesis procedure are illustrated in Fig. 9. The active substrate for this structure is a semiconductor heterostructure which contains layers designed to provide the required nonmonotone nonlinearity. For example, a double barrier RTD structure grown using molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) could provide an appropriate current-voltage relationship. The synthesis procedure begins with the lithographic definition (at a scale of approximately ten times the nanoscale node dimension) of regions which will contain the computational cell core regions, i.e., the regions in which arrays of nanometer diameter metallic islands are deposited. The arrays of metallic islands, along with the internode linking

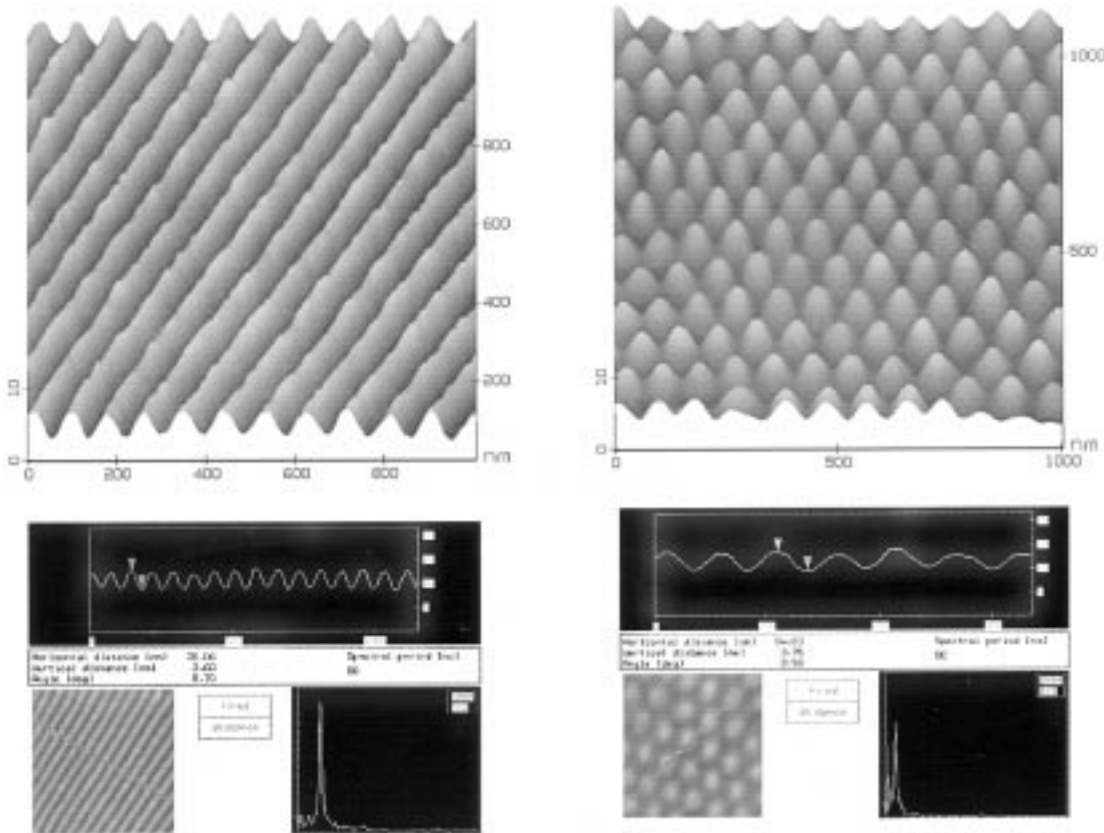


Fig. 10. Two typical patterns produced by electropolishing a thin film of aluminum. The first can be used to produce narrow metallic wire arrays and the last can be used to produce a hexagonal close-packed array of metallic islands. These figures are raw atomic force micrographs. Depth profile along arbitrarily selected directions on the surface are shown with well resolved peaks in the corresponding Fourier spectra indicative of the high degree of periodicity and ordering.

resistors, are deposited in these patterned regions using, for example, self-organizing techniques. The active substrate must be patterned to provide individual mesas for each of the metallic islands. In order to provide self-alignment of the semiconductor mesas with the nanoscale metallic islands, it is desirable to use the metallic island arrays as “natural” masks for etching of the mesas [27], [28]. Next, it is necessary to define the intercell coupling elements, namely the diodes. Finally, a thin film resistive layer, to provide effective bias resistors for each nanoscale metallic island, and bias/clock electrodes must be deposited over each computational cell. The deposition of electrodes for the polyphase clock requires another lithographic step, with registration to the cell definition lithography. Details of these procedures are described below.

A. Nanoscale Elements in Cell Core

The primary features of the computational cell core are 1) a uniform array of nanometer scale metallic islands with controlled resistive coupling between islands, 2) low-resistance coupling of the metallic islands to semiconductor mesas with appropriate nonmonotone nonlinearity, and 3) a thin film resistive layer to provide bias connections to the metallic islands. Fabrication of the metallic nodes and

active substrate connections within a cell have been described previously [14]. There are several techniques based on chemical self-assembly which can provide uniform 2-D arrays of metal islands suitable for cell core applications. Highly ordered, self-organized arrays of quantum dots and wires have been demonstrated using electropolishing of an aluminum film in an acidic solution of perchloric acid, butyl cellusolve, and ethanol [10], [27], [29], [30]. Fig. 10 shows examples of arrays of wires or dots formed by the electropolishing technique. The feature sizes of these patterns can be controlled over the range of approximately 20–100 nm by varying the temperature and composition of the electrolyte and possibly the voltage of electropolishing. The required nanoscale islands can be realized either by directly employing the patterned aluminum film or by pattern transfer to another material [14]. Resistive links between the islands can be provided by depositing a material such as low-temperature MBE grown GaAs on the surface to contact the islands.

Another independent approach that has been demonstrated involves fabricating large area, 2-D close packed arrays of 4 nm diameter gold clusters with controlled intercluster resistances [20]. In this technique, the arrays are formed from colloidal suspensions of neutral, encapsulated gold clusters. The intercluster resistance can be

controlled by exposing the array to conjugated organic molecules with end groups which bind to gold [31], [32]. An example of such a molecule is biphenyl-dithiol. The conjugated molecules bridge the gaps between clusters and result in a strong mechanical link between clusters and a controlled intercluster resistance [20], [21]. The measured in-plane conductance of linked cluster arrays formed using this procedure exhibit significant single electron charging effects at room temperature, consistent with the predicted capacitances for 4 nm diameter clusters and the predicted resistances for the conjugated organic linking molecules [20], [33]. The resistances of the organic molecules deposited between gold surfaces inferred from the array experiments and from scanning tunneling microscope experiments on individual clusters are in the range of 10–40 M Ω per molecule [20], [34]. Theoretical predications indicate that the resistance per molecule can be varied significantly by employing different conjugated organic molecules [33]; experimental evidence supports this prediction. While experiments to date have employed gold clusters, nanometer scale clusters of other metals have been synthesized using similar techniques and it is expected that 2-D arrays could be formed with other materials. In addition, alternate synthesis techniques yield clusters of semiconductor materials such as CdS and CdSe [35].

In order to provide effective coupling to the active substrate mesas, low resistance ohmic contact is required between the nanoscale metallic islands and the semiconductor mesas. The interface between the metallic nodes and the semiconductor surface layer must provide a stable, low-resistance contact without the need for alloying or other high temperature processing, since the self-assembly techniques used to form the metallic island arrays tend to be room temperature processes and nonreactive with the surface. In addition, post-deposition annealing of nanometer diameter islands could result in unacceptable size variation and shape distortion. A nonalloyed ohmic contact structure utilizing low-temperature grown GaAs has been demonstrated which should provide a suitable coupling layer for the node to active substrate interface [36]. This structure provides low-resistance ohmic contacts without annealing and also provides a surface which can remain free of significant oxidation even after hours of air exposure [36], [37]. In addition, this structure results in a controlled effective surface potential, without a significant surface depletion layer, as evidenced by the observation of a midgap band of states in a scanning tunneling spectroscopy experiment performed following air exposure [38]. Layers as thin as 2 nm are effective in providing this surface passivation effect and also allow thin *n*-type layers with very high activated donor densities to be realized immediately below this surface layer [36]. A relatively shallow etch can be used to selectively remove this low-temperature grown GaAs passivation layer, resulting in the depletion of the exposed surface and therefore providing effective patterning. The resulting surface is nearly planar, in contrast to high aspect ratio pillars often reported for

small area device mesas. This near planarity is essential for subsequent fabrication steps, which may include self-assembly deposition of conjugated organic molecules for inter-island linking and the deposition of the thin-film resistive bias layers.

In the proposed cell cores, each nanometer scale metallic island needs to be connected to an individual semiconductor mesa. The requirements for registration between the islands and the mesas dictate a self-aligned technique. One possibility would be to use the self-organized metallic islands themselves as the masking elements, in a “natural” patterning technique comparable to that recently reported for 20–50 nm islands of gold evaporated onto a semiconductor substrate [28]. Other possibilities include using a masking layer, formed using a lithographic technique or a self-organized array, to define the semiconductor mesas and then to nucleate a metallic island on each mesa. Mesa isolation is achieved either by reactive ion etching, or by using the metal islands as a mask and photo-oxidizing the exposed areas in ultraviolet (UV) light.

B. Cell and Interconnect Patterning

While self-assembly techniques can realize highly uniform arrays of metallic islands over relatively large area, the delineation of cell cores, intercell connections and bias/clock lines will require patterning techniques with minimum feature sizes approximately equal to the cell core dimension. For a computational cell in which the nanoscale metallic islands are 10 nm in diameter, the required minimum feature size would be 20–100 nm. High resolution lithography techniques such as electron beam or X-ray lithography can realize features in this range, but these techniques can induce surface damage and generally require photoresist materials that may be incompatible with the self-organizing techniques which may be used for definition of the nanoscale elements. There are, however, several demonstrations of patterning techniques which can provide the required feature sizes and which are compatible with the definition of self-assembled nanoscale arrays in patterned regions. Self-assembled monolayers (SAM's) of organic molecules, the most famous example of which is alkanethiol on gold [39], [40] could potentially be used to define areas for deposition or etching. SAM's on various surfaces, including semiconductors such as Si and GaAs, have been used to passivate the surface or to provide controlled surface characteristics such as hydrophobic/hydrophilic regions [41]. SAM's have also been employed as electron beam or scanning tunneling microscope resists [42]. In addition, deposition of SAM's using elastomer stamp pads or patterning of photoresist materials using nanoimprint lithography techniques can potentially provide low cost, high throughput patterning, provided that issues such as registration are addressed [41], [43]. The characteristics achievable with various SAM's, including small thickness (typically 1–2 nm), uniformity and chemical affinities, makes them well suited for applications involving nanoscale islands. Deposition of gold nanoclusters on organic layers patterned by electron beam lithography has been reported,

indicating that deposition within patterned regions is feasible [44]. In contrast, conventional photoresist materials may prove unsuitable as patterning templates for nanoscale arrays due to the residual surface contamination left after development and the relatively large thickness of the resists, in comparison with the dimensions of the nanoscale metallic islands.

While the fabrication of the proposed computational cells will require several significant development efforts, proof of concept experiments exist for most of the major steps outlined above. One area of difficulty is the need for intercell rectifying elements with relatively low turn-on voltages. There has been a great deal of interest in molecular rectifiers since the paradigm of a donor- π system, σ bonded tunneling bridge and an acceptor- π system was proposed [45]. Theoretically speaking, rectification should occur in nearly any molecule with sufficient asymmetry in the one-electron energy levels [46]. Molecular rectification has been demonstrated unambiguously in Langmuir-Blodgett films [47] although, to our knowledge, there has been no report of rectification by a single molecule as opposed to Langmuir-Blodgett films. Reports of rectifying characteristics for molecules using a TTF/TCNQ donor/acceptor configuration deposited between metal plates [48] indicate that rectification is possible in elements which are compatible with the dimensions and chemical characteristics of the proposed synthesis techniques. However, the reported current densities ($\mu\text{A}/\text{cm}^2$) have been well below the levels required for operation in this application [48]. Assuming that a suitable molecular rectifier is available, it will be a different molecule than the one needed to provide the resistive links between the metallic islands within a cell core. Two levels of molecular self-assembly in patterned regions will therefore be required for the two interconnect functions, namely intracell resistive connections and intercell rectifying connections. Other alternatives, including rectifiers incorporated in the semiconductor active layers, can also be explored.

C. Alternate Molecular Diodes

The molecular diodes described in the previous section are incapable of handling sufficiently large current densities. To overcome this drawback, we can explore two alternate routes for synthesizing diodes to link selected quantum dots. These techniques result in vertical diodes between a molecule and an underlying semiconductor substrate. Consequently, they are not immediately suitable for synthesizing lateral rectifying connections between metallic islands. However, these diodes can carry significantly higher current densities, well in excess of $10^6 \text{ A}/\text{cm}^2$ [49] and are therefore attractive. Needless to say, significant further research needs to be done in this area before these vertical diodes can be modified to provide lateral connections. We describe these diodes below.

1) *Scanning Tunneling Tip Induced Molecular Decomposition*: The combination of a CVD source molecule and a scanning tunneling microscope (STM) provides a way to “direct write” nanometer-sized diodes on a suitable

substrate. In this process, the energy-tunable electron flux from the highly positionable STM-tip is used to decompose the appropriate regions of a deposited layer of CVD source molecules on the substrate. In these regions, a heterojunction diode is formed between the decomposition product and the underlying substrate. This is followed by annealing to remove any unwanted species or undecomposed molecules through thermal desorption [50]. The final product is a designed array of local regions with altered composition forming heterojunction diodes. Organometallics and main group carboranes are potential candidates for CVD source compounds to be used in this approach [51]–[55]. For this process to be truly a selective area process, the source compound must adsorb molecularly rather than dissociatively [50]. Carpinelli *et al.* [50] have shown that such a molecular precursor state exists over a limited coverage range at room temperature for the icosahedral cage molecule *closo*-1, 2-dicarbododecaborane ($\text{C}_2\text{B}_{10}\text{H}_{12}$) on Si. They studied the surface reaction of Si(111)-(7 \times 7) reconstruction with the above molecular species using an STM. The current-voltage characteristic of the $\text{B}_5\text{C}/\text{Si}(111)$ interface (measured with STM) showed anisotropic rectifying behavior indicating that this is truly a process for “direct-writing” nanometer-sized heterojunction diodes.

The above technique is a “direct-write” process and hence serial in nature. Each wafer has to be patterned one at a time resulting in slow throughput. A faster technique is to make the process compatible with masking and exposure. This is realized as follows. Decomposition of *closo*-1, 2-dicarbododecaborane can be achieved by exposing the molecule to either UV or X-ray radiation. UV decomposition of organometallics or cluster source molecules offers better selective chemistry than X-ray, partly because decomposition by X-ray is due to secondary electrons [56], [57]. However, X-ray is superior in that smaller feature sizes can be delineated since the wavelength is shorter. There have been definite indications that a $\text{B}_5\text{C}/\text{Si}(111)$ heterojunction diode can be fabricated by synchrotron (X-ray) induced decomposition of *closo*-1, 2-dicarbododecaborane on Si [58]. This can lead to a projection lithography technique for synthesizing $\text{B}_5\text{C}/\text{Si}(111)$ heterojunction diodes. Since this process involves exposure of the chemisorbed species to the X-ray source through a mask, it will result in a high throughput.

IV. CONCLUSION

We have described a novel architecture for realizing nanoelectronic logic gates and circuits based on arrays of metallic dots assembled on a double-barrier RTD substrate. Resistive connections link nearest neighbor dots within a logic cell and rectifying connections link the cells. The use of minimal complexity in the nanoscale interconnection elements should reduce the processing demands for this architecture. We have presented a theoretical analysis of this architecture, and provided results of simulations to exemplify logic operations. We have shown that the cells

can exhibit bistable voltage states in both the continuous charge and discrete charge (single electron) regimes. Topologies for realizing OR and AND gates as well as somewhat more complex Boolean circuits have been described. With appropriate cell configurations and clocking sequences, unidirectional propagation, fault tolerance, and manageable power dissipation levels can be achieved in the logic circuits. These systems, if realized, could result in extremely dense circuits with high operating speeds and sufficiently low power dissipation for ultra large scale integration.

A fabrication procedure for cells and interconnections of the architecture has been described. The fabrication incorporates self-organization and "natural" patterning techniques to realize the nanometer scale elements, internode resistance, and self-aligned semiconductor mesas required in the cell cores. Cell areas, bias/clock electrodes and interconnect areas are defined using conventional nanolithographic techniques which are compatible with the chemical self-assembly based techniques used for the nanometer scale elements. Although proof of concept experiments exist for the major technologies involved in the fabrication procedure, integration of the overall fabrication sequence, and control of various element values undoubtedly present significant challenges. Nonetheless, these challenges may be overcome with time. Moreover, it is anticipated that this technology could be readily adapted to fabrication of other computational circuits with nanometer scale elements. Thus, we conclude that these architectures and alternate fabrication methodologies for synthesizing them deserve serious attention.

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REFERENCES

[1] P. Bakshi, D. Broido, and K. Kempa, "Spontaneous polarization of electrons in quantum dashes," *J. Appl. Phys.*, vol. 70, p. 5150, 1991, and P. Bakshi (unpublished).

[2] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, "Quantum cellular automata," *Nanotechnology*, vol. 4, p. 49, 1993.

[3] K. K. Likharev and A. N. Korotkov, "Single electron parametron: Reversible computation in a discrete state system," preprint.

[4] A. N. Korotkov, "Wireless single-electron logic biased by alternating electric field," *Appl. Phys. Lett.*, vol. 67, p. 2412, 1995.

[5] R. A. Kiehl and T. Ohshima, "Bistable locking of single electron tunneling elements for digital circuitry," *Appl. Phys. Lett.*, vol. 67, pp. 2494–2496, 1995.

[6] T. Ohshima and R. A. Kiehl, "Operation of bistable phase locked single electron tunneling logic elements," *J. Appl. Phys.*, vol. 80, pp. 912–923, 1996.

[7] S. Bandyopadhyay, B. Das, and A. E. Miller, "Supercomputing with spin polarized single electrons in a quantum coupled architecture," *Nanotech.*, vol. 5, pp. 113–132, 1994.

[8] S. S. Molotkov and S. N. Nazin, "Single electron spin logical gates," *JETP Lett.*, vol. 62, p. 272, 1995.

[9] —, "Single electron computing: Quantum dot logic gates," *Zh. Eksp. Teor. Fiz.*, vol. 110, p. 1439, 1996.

[10] S. Bandyopadhyay and V. P. Roychowdhury, "Computational paradigms in nanoelectronics: Quantum coupled single electron logic and neuromorphic networks," *Jap. J. Appl. Phys.*, vol. 35, pt. 1, pp. 3350–3362, 1996.

[11] —, "Quantum coupled architectures for logic circuits: Issues and problems," in *Proc. Int. Conf. Quantum Dev. Circ.*, Alexandria, Egypt, June 4–8, 1996, K. Ismail, S. Bandyopadhyay, and J.-P. Leburton, Eds. London, U.K.: Imperial College, pp. 271–276.

[12] R. Landauer, "Is quantum mechanics useful?," *Phil. Trans. Royal Soc. London A*, vol. 353, pp. 367–376, 1995.

[13] —, "Need for critical assessment," *IEEE Trans. Elec. Dev.*, vol. 43, pp. 1637–1639, 1996.

[14] V. P. Roychowdhury, D. B. Janes, S. Bandyopadhyay, and X. Wang, "Collective computational activity in self-assembled arrays of quantum dots: A novel neuromorphic architecture for nanoelectronics," *IEEE Trans. Elec. Dev.*, vol. 43, pp. 1688–1699, Oct. 1996.

[15] M. P. Anantram and V. P. Roychowdhury, "Metastable states in a linear array of quantum dots," in *Proc. PHYSCOMP'96*, Boston, Nov. 1996.

[16] J. C. Lusth, B. Dixon, D. J. Jackson, and S. L. Burkett, "Quantum dot cellular automata and the problem of unbalanced logic gates," in *Proc. Int. Conf. Quantum Dev. Circ.*, Alexandria, Egypt, June 4–8, 1996, K. Ismail, S. Bandyopadhyay, and J.-P. Leburton, Eds. London, U.K.: Imperial College, pp. 289–297.

[17] P. Balasingam and V. P. Roychowdhury, "Nanoelectronic functional devices," Tech. Rep. TR-EE 94-24, Sch. Elec. Eng., Purdue Univ., West Lafayette, IN, July 1994.

[18] D. W. Jordan and P. Smith, *Nonlinear Ordinary Differential Equations*. Oxford: Clarendon, 1987.

[19] A. A. Andronov, A. A. Vitt, and S. E. Khaikin, *Theory of Oscillators*. New York: Dover, 1966.

[20] R. P. Andres, J. D. Bielefeld, J. I. Henderson, D. B. Janes, V. R. Kolagunta, C. P. Kubiak, W. J. Mahoney, and R. G. Osifchin, "Self-assembly of a two-dimensional superlattice of molecularly linked metal clusters," *Sci.*, vol. 273, pp. 1690–1693, Sept. 20, 1996.

[21] D. B. Janes, V. R. Kolagunta, R. G. Osifchin, J. D. Bielefeld, R. P. Andres, J. I. Henderson, and C. P. Kubiak, "Electronic conduction through two-dimensional arrays of nanometer diameter metal clusters," *Superlattices and Microstructures*, vol. 18, pp. 275–282, 1995.

[22] N. S. Bakhvalov, G. S. Kazachca, K. K. Likharev, and S. I. Serdyukova, "Single-electron solitons in two-dimensional tunnel structures," *Sov. Phys. JETP*, vol. 68, no. 3, pp. 581–587, Mar. 1989.

[23] U. Geigenmüller and G. Schön, "Single-electron effects in arrays of normal tunnel junctions," *Europhys. Lett.*, vol. 10, pp. 765–770, Dec. 1989.

[24] D. K. Schroder, "Advanced MOS devices," in *Modular Series on Solid State Devices*, G. W. Neudeck and R. F. Pierret, Eds. Reading, MA: Addison-Wesley, 1987.

[25] Semiconductor Industry Assoc., *The National Technology Roadmap for Semiconductors*, 1994.

- [26] D. B. Tuckerman and R. F. W. Pease, *IEEE Elec. Dev. Lett.*, vol. 2, p. 126, 1981.
- [27] S. Bandyopadhyay, A. E. Miller, H.-C. Chang, G. Banerjee, V. Yuzhakov, D.-F. Yue, R. E. Ricker, S. Jones, J. A. Eastman, E. Baugher, and M. Chandrasekhar, "Electrochemically assembled quasiperiodic quantum dot arrays," *Nanotechnology*, vol. 7, pp. 360–371, 1996.
- [28] B. W. Alphenaar, Z. A. K. Durrani, A. P. Heberle, and M. Wagner, "Resistance bistability in resonant tunneling diode pillar arrays," *Appl. Phys. Lett.*, vol. 66, pp. 1234–1236, 1995.
- [29] A. E. Miller, S. Bandyopadhyay, G. Banerjee, D.-F. Yue, and M. Chandrasekhar, unpublished, 1995; S. Bandyopadhyay, A. E. Miller, and M. Chandrasekhar, "Optical, electronic, magnetic, and superconducting properties of quasiperiodic quantum dot arrays synthesized by a novel electrochemical technique," in *Proc. SPIE, Photonics West '95*, San Jose, CA, Feb. 1995, vol. 2397, pp. 11–30.
- [30] R. E. Ricker, A. E. Miller, D.-F. Yue, G. Banerjee, and S. Bandyopadhyay, "Nanofabrication of a quantum dot array: Atomic force microscopy of electropolished aluminum," *J. Elec. Mat.*, vol. 25, pp. 1585–1592, 1996.
- [31] J. M. Tour and J. S. Schumm, "Synthesis of molecular wires by a novel divergent/convergent approach," *Polym. Prepr.*, vol. 34, pp. 368–369, 1993.
- [32] J. I. Henderson, S. Feng, G. M. Ferrence, T. Bein, and C. P. Kubiak, "Self-assembled monolayers of dithiols, diisocyanides and isocyanothiols on gold: 'Chemically sticky' surfaces for covalent attachment of metal clusters and studies of interfacial electron transfer," *Inorg. Chim. Acta*, vol. 242, pp. 115–124, 1996.
- [33] M. P. Samanta, W. Tian, S. Datta, J. I. Henderson, and C. P. Kubiak, "Electronic conduction through organic molecules," *Phys. Rev. B*, vol. 53, p. R7626, 1996.
- [34] R. P. Andres, T. Bein, M. Dorogi, S. Feng, J. I. Henderson, C. P. Kubiak, W. J. Mahoney, R. G. Osifchin, and R. Reifenberger, "Coulomb staircase at room temperature in a self-assembled molecular nanostructure," *Sci.*, vol. 272, p. 1323, 1996.
- [35] S. A. Blanton, A. Dehestani, P. C. Lin, and P. Guyot-Sionnest, "Photoluminescence of single semiconductor nanocrystallite by two-photon excitation spectroscopy," *Chem. Phys. Lett.*, vol. 229, p. 317, 1994; M. E. Schmidt, S. A. Blanton, M. A. Hines, and P. Guyot-Sionnest, "Size-dependent two-photon excitation spectroscopy of CdSe nanocrystals," *Phys. Rev. B*, vol. 53, p. 12629, 1996.
- [36] M. P. Patkar, T. P. Chin, J. M. Woodall, M. S. Lundstrom, and M. R. Melloch, "Very low resistance nonalloyed contacts using low-temperature molecular beam epitaxy of GaAs," *Appl. Phys. Lett.*, vol. 66, p. 1412, 1995.
- [37] T.-B. Ng, D. B. Janes, D. McInturff, and J. M. Woodall, "Inhibited oxidation in low-temperature grown GaAs surface layers observed by photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 69, pp. 3551–3553, 1996.
- [38] S. Hong, D. B. Janes, D. McInturff, R. Reifenberger, and J. M. Woodall, "Stability of a low-temperature grown GaAs surface layer following air exposure using tunneling microscopy," *Appl. Phys. Lett.*, vol. 68, pp. 2258–2260, Apr. 15, 1996.
- [39] R. G. Nuzzo and D. L. Allara, "Adsorption of bifunctional organic disulfides on gold surfaces," *J. Amer. Chem. Soc.*, vol. 105, pp. 4481–4483, 1983.
- [40] P. E. Laibinis, R. G. Nuzzo, and G. M. Whitesides, "Structure of monolayers formed by coadsorption of two n-alkanethiols of different chain lengths on gold and its relation to wetting," *J. Phys. Chem.*, vol. 96, p. 5097, 1992.
- [41] A. Kumar and G. M. Whitesides, "Patterned condensation figures as optical diffraction gratings," *Sci.*, vol. 263, pp. 60–62, 1994.
- [42] M. J. Lercel, R. C. Tiberio, P. F. Chapman, H. G. Craighead, C. W. Sheen, A. N. Parikh, and D. L. Allara, "Self-assembled monolayer electron-beam resists on GaAs and SiO₂," *J. Vac. Sci. Tech. B*, vol. 11, pp. 2823–2828, 1993.
- [43] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Imprint lithography with 25-nanometer resolution," *Sci.*, vol. 272, pp. 85–87, 1996.
- [44] T. Sato, D. G. Hasko, and H. Ahmed, "Patterned deposition of colloidal particle monolayer," *Symp. Single Elec. Nanoelectronic, 190th Meet. Electrochem. Soc.*, San Antonio, TX, Oct. 6–11, 1996.
- [45] A. Aviram and M. A. Ratner, "Molecular rectifiers," *Chem. Phys. Lett.*, vol. 29, pp. 277–283, 1974.
- [46] V. Mujica, M. Kemp, A. Roitberg, and M. Ratner, "Current-voltage characteristics of molecular wires: Eigenvalue staircase, Coulomb blockade and rectification," *J. Chem. Phys.*, vol. 104, pp. 7296–7305, 1996.
- [47] C. M. Fischer, M. Burghard, S. Roth, and K. von Klitzing, "Organic quantum wells: Molecular rectification and single electron tunneling," *Europhys. Lett.*, vol. 28, p. 129, 1994.
- [48] J. R. Sambles and A. S. Martin, "Molecular rectification," *Phys. Scripta*, vol. T-49, pp. 718–720, 1993.
- [49] P. A. Dowben, private communication.
- [50] J. M. Carpinelli, E. W. Plummer, D. Byun, and P. A. Dowben, "Scanning tunneling microscopy study of intermediates in the dissociative adsorption of C₁₀H₈ on Si(111)," *J. Vac. Sci. Tech.*, vol. B-13, pp. 1203–1206, 1995.
- [51] E. E. Ehrichs, S. Yoon, and A. L. deLozanne, "Direct writing of 10 nm features with the scanning tunneling microscope" *Appl. Phys. Lett.*, vol. 53, p. 2287, 1988; E. E. Ehrichs, R. M. Silver, and A. L. deLozanne, "Direct writing with scanning tunneling microscope," *J. Vac. Sci. Tech.*, vol. A-6, p. 540, 1988.
- [52] A. D. Kent, T. M. Shaw, S. von Molnar, and D. D. Awschalom, "Growth of high aspect ratio nanometer scale magnets with chemical vapor deposition and scanning tunneling microscopy," *Sci.*, vol. 262, p. 1249, 1993.
- [53] E. E. Ehrichs and A. L. deLozanne, *Nanostructure Physics and Fabrication*, M. A. Reed and W. P. Kirk, Eds. New York: Academic, 1989, p. 441.
- [54] D. S. Sauly, A. Ermakov, E. L. Garfunkel, and P. A. Dowben, "Electron-beam-induced patterned deposition of allylcyclopentadienyl palladium using scanning tunneling microscopy," *J. Appl. Phys.*, vol. 76, p. 7639, 1994.
- [55] G. Dujardin, R. E. Walkup, and P. Avouris, "Dissociation of individual molecules with electrons from the tip of a scanning tunneling microscope," *Sci.*, vol. 255, p. 1232, 1992.
- [56] T. Urisu and H. Kyuragi, "Synchrotron-radiation-excited chemical vapor deposition and etching," *J. Vac. Sci. Tech.*, vol. B-5, p. 1436, 1987.
- [57] F. K. Perkins, M. Onellion, S. Lee, D. Li, J. Mazuroski, and P. A. Dowben, "Synchrotron radiation induced deposition of boron and boron carbide films from boranes and carboranes II; Nido-2, 3-diethyl-2, 3-dicarbahexaborane," *Appl. Phys.*, vol. A-54, p. 442, 1993.
- [58] D. Byun, S.-D. Hwang, P. A. Dowben, F. K. Perkins, F. Flippin, and N. J. Ianno, "Heterojunction fabrication by selective chemical vapor deposition induced by synchrotron radiation," *Appl. Phys. Lett.*, vol. 64, pp. 1968–1970, 1996.



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