System and Circuit Aspects of Nanoelectronics

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Abstract

This paper analyzes the impact of nano-scale technology on future circuit design and describes several prototypes of logic and memory applications. Resonant tunneling transistors, single electron transistors, and quantum cellular automata are reviewed as relevant nanoelectronic device categories. In regard to the limited interconnectivity and the sensitivity of the devices to parameter variations we discuss bit level systolic arrays, a propagate instruction array processor, and fault tolerant logic. Furthermore, functional integration, that is the possibility of exploiting quantum effects to obtain a function specific behavior, is illustrated as design technique by compact memory cells and logic families with reduced circuit complexity.

1. Introduction

Topic of this paper is to the review the present state of nanoelectronic devices and recent developments of experimental prototype circuits. Although an advanced sub μm Si-CMOS technology will be without doubt the mainstream technology until the year 2010 at least, there is an intensive research activity in novel nanoelectronic device concepts. Principal difference between nanoelectronic devices and this advanced CMOS technology with a minimum feature size of about 100 nm [50] is that quantum and single charge effects are used to obtain a transistor function. Before we focus on different nanoelectronic device and circuit categories, it should be emphasized that there are some general requirements for a successful computer device which have been confirmed by the progress of solid-state electronics in the last five decades [26]:

- The device input has to be well separated from the output.
- A large gain is necessary to restore noisy input signals.
- The device should have sufficient driving capability and at least a fan-out of 2.
- A small leakage current in the non-active state is important for power dissipation.

These are indispensable requirements for all conceivable kinds of nanoelectronic devices and therefore each novel device concept has to be examined by means of these rules.

At the moment it is not clear if there are potential successors for Si-MOSFET's and to which category of nanoelectronic devices this successor belongs. Among the devices being currently under discussion, resonant tunneling transistors (RTT's), single electron transistors (SET's) and quantum cellular automata (QCA's) are the most promising candidates [19], [27], [38].

An interesting trend that can be observed in recent years is that the transition to nanoelectronics will occur in an evolutionary way by combining field effect (FET's) and bipolar junction transistors (BJT's) with novel nanoelectronic devices [27]. In section 2 and 3 we discuss a compact RTT-FET SRAM cell and a single electron-MOSFET memory cell to illustrate this strategy. Section 4 describes two theoretical concepts for quantum dot arrays, the quantum cellular automata and nonlinear RTD-quantum dot networks.

Common features of these devices are sensitivity to background charges and fabrication tolerances as well as reduced driving capabilities. Based on this, the last section gives an outlook in which way system and circuit architectures have to be adapted to the requirements of the devices.

2. Resonant tunneling circuits

2.1. Resonant tunneling transistors

Today, resonant tunneling transistors are the most established nano-scale devices because they already operate at room-temperature. Moreover, from the viewpoint of circuit applications their fabrication and interfacing with FET's and BJT's has reached an advanced level that allows the investigation of small scale circuits [19].

Resonant tunneling devices are based on electron transport via discrete energy levels in double barrier quantum well structures. Since 1974, when Esaki and Chang first observed resonant tunneling [9], the progress in heterostructure epitaxy has lead to quan-

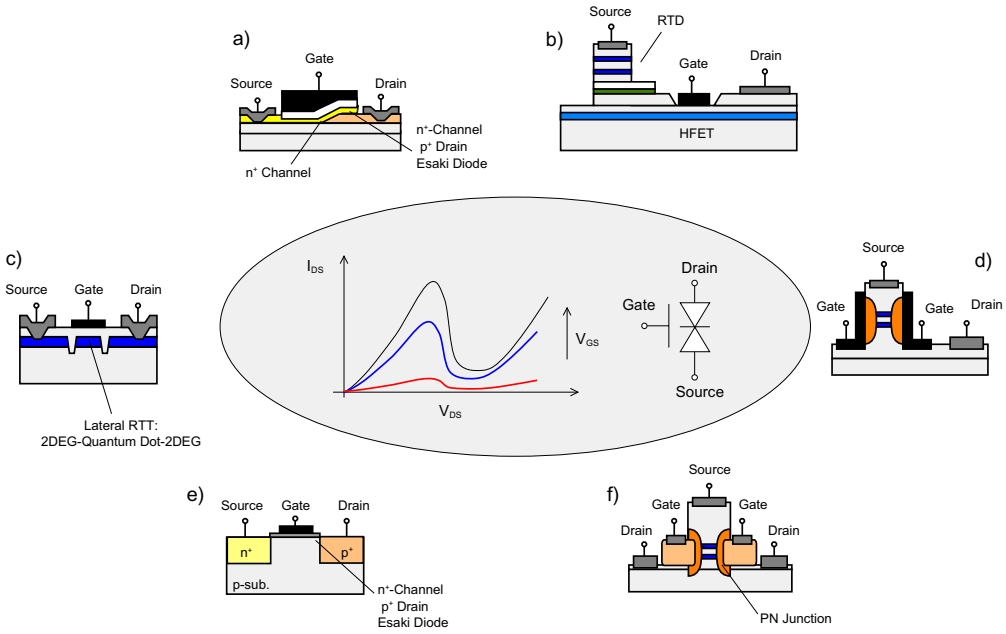

Figure 1: Different implementations of resonant tunneling field effect transistors.

tum effect devices with adjustable peak current densities and peak voltages [12], [44].

For circuit applications a combination of negative differential resistance (NDR) with electronic amplification is very attractive. This has motivated the development of different three terminal devices. Significant examples are planar surface tunneling transistors (figure 1a) [52], resonant tunneling diodes (RTD's) which are placed in the source or drain contact of a heterostructure field effect transistor (HFET) (figure 1b) [5], [10]. Vertical RTT's with Schottky or pn-junction side gates have also been investigated (figure 1d, f) [2], [6] , [43]. Due to the field effect controlled input and the resonant tunneling transport of the electrons between drain and source all these RTT's have in common a gate voltage dependent NDR output characteristics.

The most advanced RTT is a lateral tunneling structure where the transistor function is obtained if the energy levels of the quantum dot are varied by means of the gate voltage (figure 1c) [45]. Moreover, an NDR drain source current has also been observed in a modified Si-MOSFET at room temperature [29]. In this case the drain is p^+ doped to implement an interband (Esaki) tunneling contact between the n-channel and the p^+ drain.

2.2. RTT memory cells

Although these devices are far away from giga-scale integration and further intensive research is necessary, there are several proposals for functional circuit applications which take benefit from the NDR-behavior of RTT's. Since tunneling is a very fast transport process high speed and low power static random access memories (SRAM's) are one of the most interesting circuit applications. Using two RTD's to generate a bistable circuit and combining them with a write HFET to switch the common memory node into a logic "0" or "1" state, the research group of Raytheon Texas Instruments Systems has demonstrated an ultra compact InP SRAM cell (figure 2) [54]. The SRAM cell consumes 50 nW and is an improvement of about 100 times compared with the power consumption of HFET based high speed SRAM-cells. Figure 2b shows that a relatively small peak to valley ratio (PVR) of 1:2 is sufficient to compensate the leakage current of the read and write HFET. For digital circuits the availability of RTD structures with a low peak current density and a low peak voltage is much more important than a large PVR which is usually optimized in analog circuits.

2.3. RTT logic circuits

Concerning logic applications the principal objective of RTT-circuits is to reduce the circuit complexity being required to implement a given logic function by means of multiple-valued logic [36], threshold logic gates [10] or functional X-NOR gates [8].

A typical phenomenon in circuits with RTD load elements and FET's as active element is the occurrence of a hysteresis as it is shown for an inverter in figure 3a [46]. The hysteresis results from the NDR-characteristics of the RTD. Especially if the logic voltage levels and the supply voltage are scaled down below 1.0 V this nonlinear effect might be helpful to increase the noise margins of the circuit.

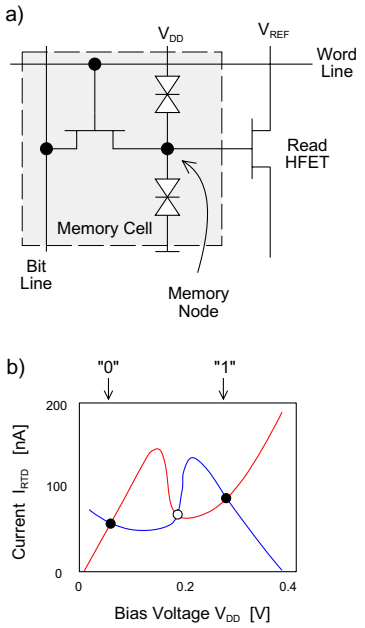

Figure 2: RTD- SRAM cell (a), and bistability (b).

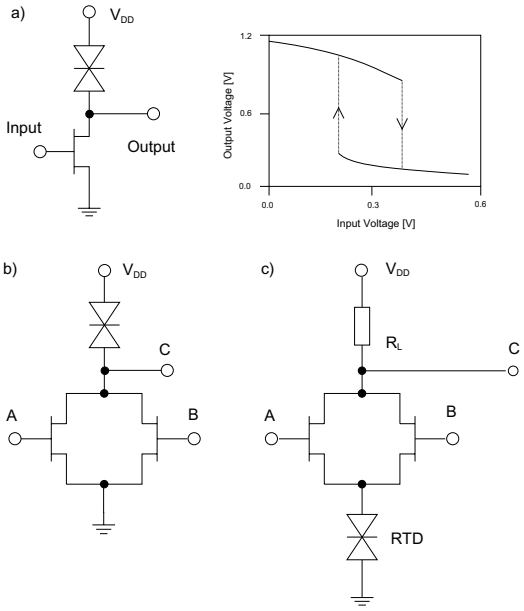

Figure 3: Static RTD-FET logic gates: inverter (a), NOR (b), XNOR (c).

A simple static NOR gate is displayed in 3b. Here, a second FET is added as second input [46] to the inverter. Investigations based on experimental results of a 2-dimensional GaAs MESFET/RTD logic element predict a power delay product of 1.0fJ (comparable to SOI-CMOS) and an active power dissipation of about 1 μW for 0.7 V supply voltage.

Implementing the RTD in the source contact of the FET and including a load resistor, a static XNOR gate has also been proposed [49] (figure 3c). This circuit example follows the original idea of Capasso to reduce the logic depth of the critical path and the number of active devices [8]. In principle such a reduction of circuit complexity might be an alternative to scaling because one could obtain a gain in performance using the same minimum feature size.

In addition to these static logic gates figure 4 shows two dynamic RTT logic gates: the monostable-bistable transition logic element (MOBILE) (a) and an RTD/Schottky XOR gate (b). The MOBILE gate has been proposed by Yamamoto et al. at NTT, Japan, who have recently demonstrated the 35 GBit/s operation of an RTT-HFET inverter latch [32].

The RTD/Schottky XOR gate is investigated at the Mayo Foundation and Hughes Research Laboratories [56]. A complete AND/OR/XOR logic family using this RTD/Schottky gate has been successfully tested at 12 GHz and at 10 GHz for a pipelined operation of two successive gates.

Both types of dynamic logic gates are composed of two identical RTD's (driver and load RTD) and make use of a monostable-bistable transition to switch between logic low and high states. The monostable-bistable transition occurs if the oscillating bias voltage is raised above twice the RTD peak voltage [2] (figure 4c). In this configuration the digital state of the logic gate is self-stabilizing and depends on the sign of the input current during the metastable transition state. As soon as the bias voltage is lowered below twice the RTD peak voltage the gate is automatically reset.

In both cases the logic functionality of these dynamic gates is determined by the input stage, either by two Schottky Diodes and an RTD, or by means of multiple HFET's in parallel to the load and driver RTD. An increased logic functionality of the RTD/Schottky gate results from exploiting the multi stability of the input RTD. This makes it possible to compute the nonlinear separable XOR function with a delay of one circuit layer similar to the static XNOR gate..

The characteristic feature of MOBILE gates is a reduction of the critical path by means of a threshold logic to extend the parallel processing of multiple inputs at the bit level [10], [41]. Compared with a Boolean logic gate, a threshold gate combines an internal multiple-valued computation of the weighted input sum with digital encoded input and output states. Actually, this capability of processing multiple input signals enables the design of circuits with bit-level parallelism and reduced complexity.

If these dynamic RTT-logic gates are arranged in several stages with a two-phase clocking scheme one obtains a bit-level systolic architecture with a pipelined data path as we will see in section 5. Therefore, together with the high frequency operation of RTT's this circuit architecture is ideally suited for future DSP applications where a large data throughput is required.

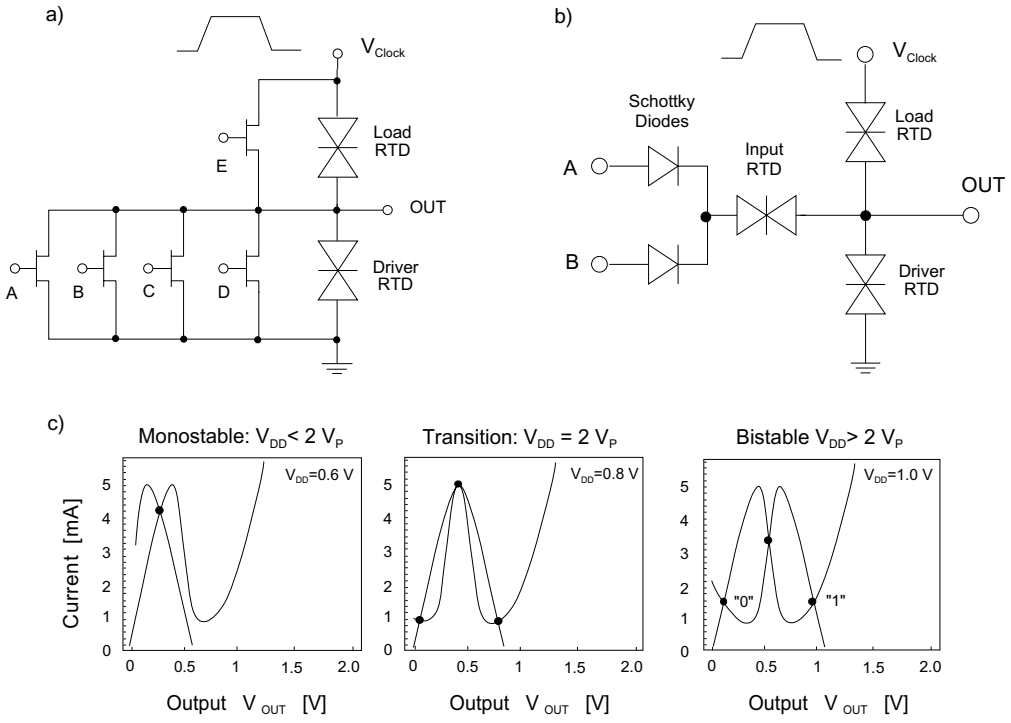

Figure 4: Dynamic RTT/RTD logic gates: RTD/HFET gate (a), RTD/Schottky gates (b), and operating principle of the Monostable-Bistable Logic Transition Element (c).

3. Single electron circuits

3.1. Single electron transistor

The fundamental physical principle of single electron devices is the Coulomb blockade resulting from the quantization of the elementary charge in an isolated node of a double junction structure [1]. To observe Coulomb blockade effects at room temperature, that is the blocking of the electron tunneling through the island, the charging energy has to exceed the thermal energy

$$\frac{1}{2}\ CV^2 \geq k_B T \approx 26\ meV \quad . \tag{1}$$

This corresponds to a tunnel junction capacitance of about $C \approx 10^{-18}$F. Thus, ultra fine structures are a prerequisite for room temperature SET circuits and lithographic progress is of fundamental relevance. To avoid quantum fluctuations the tunneling resistance between the islands has to be larger than the quantum resistance

$$R_T \geq \frac{h}{e^2} \approx 25,9\ k\Omega \quad , \tag{2}$$

so that the electrons are localized in the island. To overcome the Coulomb blockade the voltage between drain and source of the single electron tunnel junction must exceed the threshold voltage (figure 5b):

$$V_C = \frac{e}{2C} \tag{3}$$

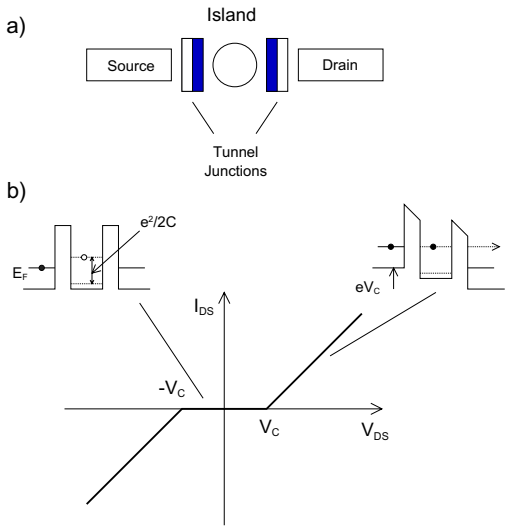

Figure 5: SET tunnel junction (a), and I-V characteristics (b).

In single electron transistors a third gate contact is capacitively coupled to the island and the Coulomb blockade can be compensated by varying the gate voltage.

3.2. SET memories

By combining a SET-multiple tunnel junction made of nano-crystalline silicon and a Si-MOSFET the research

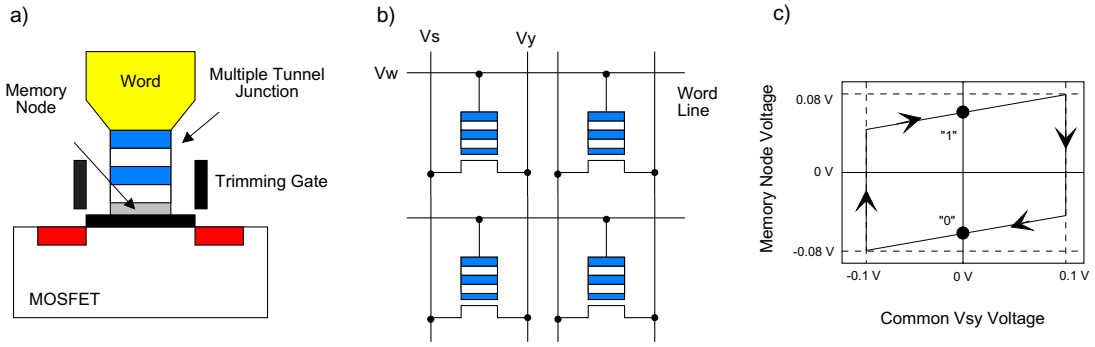

Figure 6: SET-MOS Memory structure (a), memory cell array (b), and hysteresis loop (c).

group at the Hitachi Laboratory at Cambridge has developed a hybrid SET-MOS memory cell [39], [37]. Here, a bit is stored on a memory node similar to floating gate transistors. Depending on the common drain source voltage V_{sy} the multiple tunnel junction leads to a hysteresis loop. The voltage difference of the ”0” and ”1” state is about 0.14 V and corresponds to the presence or absence of 35 electrons on the memory node. The advantage of hybrid SET-MOSFET structures is the improved gain and driving capability due to the field effect while the compactness of this memory cell results from the SET junction.

Based on this memory cell a first 128 Mbit SET/MOS memory has been implemented using a 0.25μm technology (0.145 μm^2/bit cell size) [57]. To double the effective memory density two bits are stacked vertically. A solution to overcome the charge variations is a special verify write and erase scheme.

3.3. SET logic

Among different approaches for SET logic circuits, capacitively coupled tunnel junctions are attractive because they enable a complementary logic family [23]. Figure 7a shows a capacitively coupled SET-inverter composed of four tunnel junctions and three islands. Similar to CMOS the two SET transistors operate in a complementary way because if the ”p-type SET” is conducting the ”n-type SET” is blocked and vice versa. Thus, a load capacitance is charged by the ”p-type SET” and discharged by the ”n-type SET”.

A programmable NAND/NOR gate with two data inputs and one control input to determine the Boolean function is depicted in figure 7b [15]. Although complementary SET circuits are advantageous due to the CMOS-like design style, the small voltage gain (about 4) and the poor stability against background charges lead to severe reliability problems. Resistively coupled complementary SET gates increase the voltage gain but also reduce the voltage swing [59].

There are also approaches to build neural-like gates with an adaptive behavior [20], [24]. The main argument in favor of neural-like gates is the prospect that the threshold voltage shift originating from randomly fluctuating background charges might be compensated by self-adaptation of the circuit.

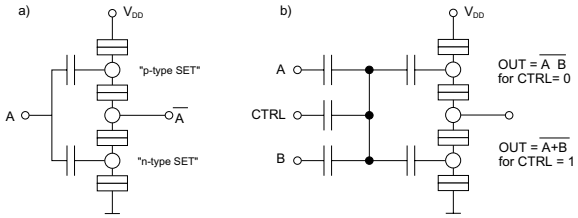

Figure 7: Capacitively coupled SET inverter (a) and SET AND/OR gate (b).

Summarizing the main challenges of SET circuit design, at the moment room temperature operation and background charge compensation are the most critical problems.

4. Quantum dot arrays

4.1. Quantum cellular automata

Quantum dot arrays are the most advanced and probably the ultimate level of solid state electronics. In recent years, the quantum cellular automata, invented by Lent and Porod at the University of Notre Dame, USA, has aroused a great interest due to its wireless architecture [31].

The basic cell of a QCA consists of four quantum dots being arranged in a square. Adding two electrons to a QCA results in two different polarization states which are used to represent the digital information (figure 8). In each of the two polarization states the electrons are located in diagonal quantum dots to minimize their mutual coulomb interaction. To prevent a tunneling of the electrons each cell is surrounded by a rectangular energy well. The most striking feature of QCA’s is the fact that performing a computation is related to a relaxation process of the quantum mechanical system

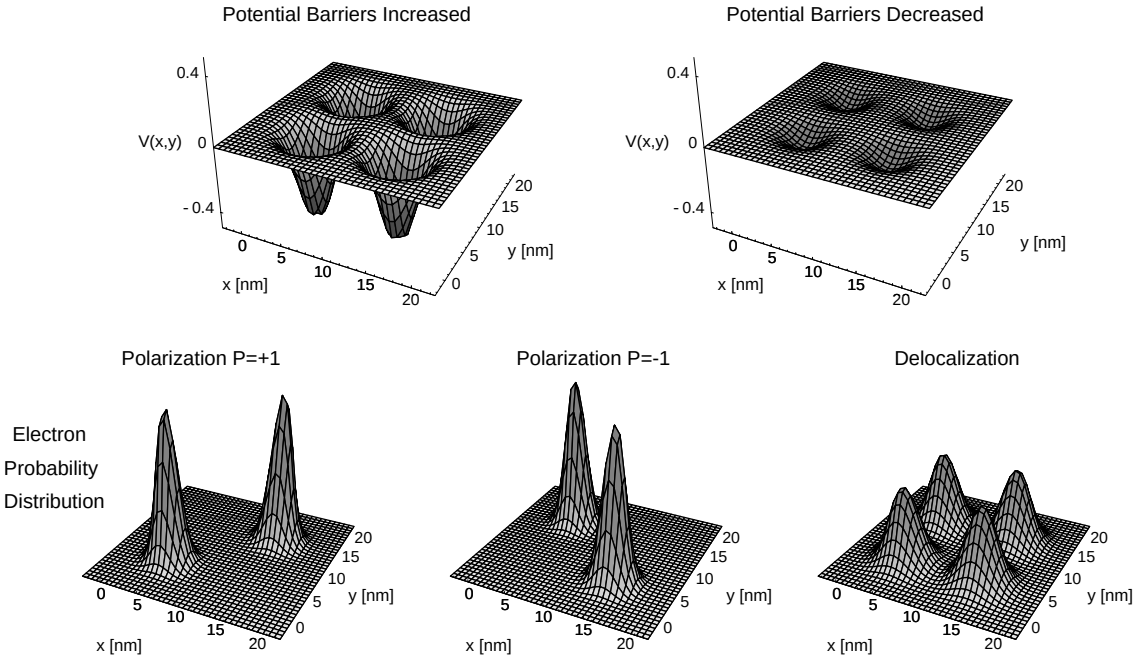

Figure 8: QCA potential and electron probability distribution.

towards one of the two possible ground states.

A cellular automata topology can be obtained if several of these cells are placed on a rectangular grid. In this case the localized electrons of one cell interact with the electrons in the neighbored cells. The most simple QCA element is a one dimensional line of cells that behaves as a wire because the electrons in adjacent cells have the same polarization. Any electrostatic change at the leftmost cell will influence the complete wire and thus propagating a bit of digital information through the QCA is done by flipping the polarization of the input cell without using metallic wires between the cells (figure 9b).

Before the polarization of a cell can be changed one has to lower the inter-cell potential barriers between the quantum dots in an adiabatic way so that the electrons are not longer localized and the tunneling probability into another quantum dot is increased (figure 8). Here, the term adiabatic switching is used in the sense of smoothly changing the inputs while the inter-dot barriers are reduced. During this transition state the probability density of the two electrons is equally distributed to the four quantum dots. If the inter-cell barrier potential is raised again the final polarization state depends on the configuration of the neighboring cells.

Basic computing elements such as an inverter, a wire with a fan-out of 2, and a majority gate are displayed in figure 9. At the moment the QCA is only a theoretical concept and the main obstacle to demonstrate room temperature operation are the precise definition of the quantum dots having a 5nm diameter. In addition, their sensitivity to fabrication tolerances as well as the influence of background charges is as critical as in SET circuits.

From an application point of view signal propagation by means of a four phase adiabatic clocking scheme (active computation, cell locked, cell relaxed, and inactive), fault-tolerant logic schemes, QCA memory components and interfacing with more conventional devices have to be investigated [31], [16].

However, the prospect to store and process one bit of digital information within an area of about $25\,\mathrm{nm}\times 25$ nm might be the ultimate level of solid state electronics and could lead us to the technological and physical limit of nano-scale circuits. To overcome the problems of a lithographic definition, a self-organizing growth of quantum dots might be a possible solution [48].

4.2. RTD-quantum dot networks

Locally coupled nonlinear networks of self-assembled metallic dots are a further example of a wireless quantum dot array [47] (figure 10a). Due to their periodic arrangement on an active resonant tunneling substrate this architecture also behaves like a cellular automata.

The significant difference between QCA's and these nonlinear networks results from the RTD nonlinearity which causes a multi-stable RC-network. This means that the digital information is represented in a more classical way as voltage level of the island capacitance (figure 10 b). The cell interaction is done by resistive and capacitive links. Moreover, as soon as the inter-cell

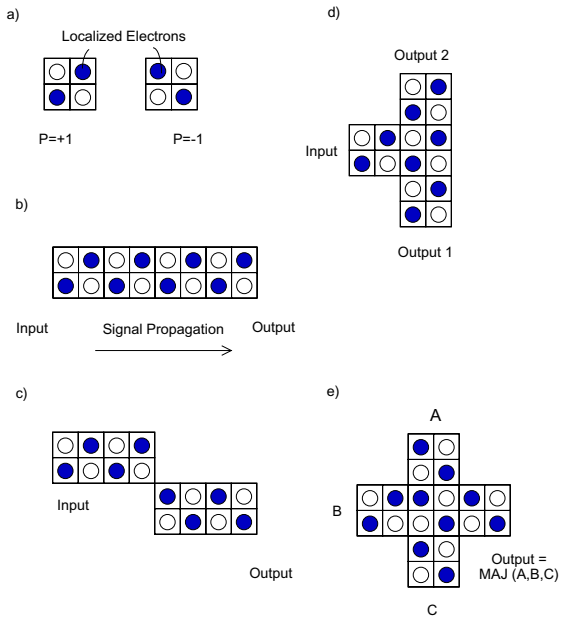

Figure 9: Polarizations of a QCA (a), QCA wire (b), inverter (c), fan-out (d), and majority gate (c).

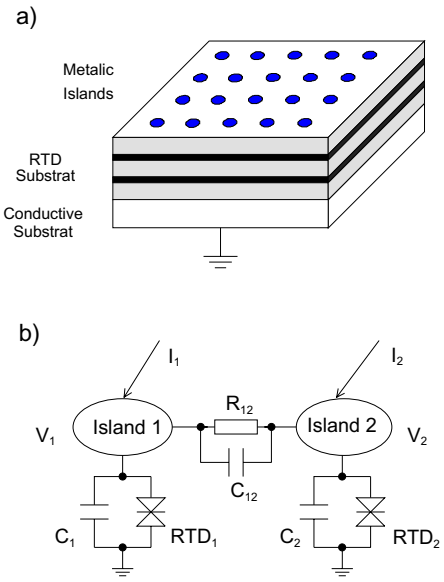

Figure 10: Self assembled nonlinear RTD quantum dot network (a) and bistable two-island equivalent circuit (b).

capacitances and resistances are comparable to $C \approx 10^{-18}$ F and the quantum resistance $R_T \approx 25,9\,\mathrm{k}\Omega$ the network operates in the Coulomb blockade regime and the elementary charge discretization determines the cell interaction. In the classical regime the cell interaction is dominated by continuous charges on the metallic islands. The multi-stability of the network is still preserved in both transport regimes.

The metallic islands are fabricated in a highly uniform way by chemical self-assembly with a controllable feature size of 20-100 nm or by an array of 4 nm diameter encapsulated gold clusters [47].

Preferred applications of nonlinear RTD-quantum dot networks are low level image processing and associative memories [48]. Boolean AND/OR-gates were also studied theoretically by grouping the array in small networks of 4×4 islands for one Boolean gate and solving the coupled set of nonlinear differential equations with appropriate initial and boundary conditions [47].

5. System and design aspects

5.1. Bit-level systolic arrays

After we have reviewed different nanoelectronic devices and circuit prototypes (for a summary see Table 1) the design of computing systems is a major challenge because it seems not reasonable to transfer a CMOS design style to RTT, SET or QCA circuits without modifications [21]. The fundamental relevance of this topic has been emphasized by Ancona in context with single electron transistor circuits for multiplication and Fast Fourier Transform [3]. Independent of the technological realization and the operating principles of the different families of nano-scale devices, important design principles are:

- A regular layout with a small number of different circuit modules.
- Local interconnections on the circuit and the system level to solve the wiring problem.
- Concurrent computation and pipelining at the bit-level to achieve a low latency and a high data throughput.
- Fault tolerant logic schemes to compensate fabrication tolerances and background charges.

Even today most of these principles are a substantial part of modern CMOS-VLSI and it is obvious that the question if nanoelectronic devices will be useful has to be investigated from that point of view, too.

The bit level systolic array is a pipelined logic style that avoids long range interconnections and accelerates the operation of arithmetic computations. In the past this circuit technique has been frequently used in DSP components [34], pipelined adders [14], [30], and array multipliers [35]. In contrast to the system level systolic arrays the processing elements in bit level systolic arrays perform simple Boolean computations.

Typically, each cell receives several one-bit input bits from the neighbored cells such as operand bits, incoming carries, and sum bits. The critical path of a cell comprises a depth 2-3 logic circuit and several D-latches at the edges of the cell to synchronize the signal propagation.

From the viewpoint of nanoelectronics the bit-level systolic array is well suited as circuit architecture for

Table 1: Comparison of Nanoelectronic Devices Categories

Device	Status	Main Problem	Advantages	Application	References
Resonant Tunneling Transistors	room temperature operation, III-V LSI process,	homogeneity, low peak currents, Si-RTD's	reduced circuit complexity	very high speed memory and logic	[2], [6], [11], [42], [43], [46], [52], [54], [56]
Single Electron Transistors	memory prototypes, logic circuits experimental	offset charges, small gain, room temperature operation	Si compatibility, CMOS-like design style, low power dissipation	low power DRAMs and floating gates $\geq$16 GBit	[1], [3], [22], [23], [37], [39]
Quantum Dot Arrays	theoretical	design style, fabrication, memory cells	wireless, very low power dissipation	ultra dense logic	[17], [31], [47], [51]

dynamic RTT circuits based on monostable-bistable transition logic elements (MOBILE's, cf. section 2.2.). As it was pointed out these dynamic RTT circuits have a self-stabilizing output that is controlled by the oscillating bias voltage. If the oscillating bias voltage is used for synchronization the logic part of the cell and the D-latch can be merged together into one circuit with a minimum critical path.

Two examples of bit-level systolic arrays for 8-bit ripple carry addition are shown in figure 11. The input operands and the sum bits propagate vertically whereas the carries are propagating in diagonal direction. The ripple carry adder design in figure 11b indicates how the delay of the adder is improved by adding two pairs of operand bits at a time. This is achieved by the threshold logic design style used in MOBILE circuits. As a result the carry bit for a 2-bit operand block is computed with a minimal delay of one circuit layer only. More details of the threshold logic full adder implementation as well as advanced adder designs based on a threshold logic version of the systolic Brent and Kung carry look-ahead algorithm [7] can be found in [41] and [42].

5.2. Array processors

Concerning the next higher level in the design hierarchy, SIMD type (Single Instruction Multiple Date) parallel array computers are an optimal system architecture for nano-scale integration due to their regular design and local interconnections.

SIMD array processors are a well known special purpose system architecture that has been developed for image processing. Image processing tasks such as noise removal, contrast enhancement and edge detection are computationally expensive and require an enormous local memory to process 8-16 bit images. Typical array sizes for a fine-grain parallelism comprise 1024×1024 pixels and thus the requirement for integrating an array of more than 1 million processing elements on one chip is a great challenge for future nano-scale circuits. An integration on a single processor would significantly increase the performance of these special purpose computers.

The classical SIMD-architecture suffers from the drawback that the instructions for the different image processing tasks have to be transmitted in a global fashion to each processing element. Apart form this there are also a lot of non-local algorithms where pixel values of non-direct neighbors are relevant causing an enormous amount of wiring. Even from today's CMOS perspective there are strong indications that this interconnection problem is a critical performance limiter for future computing systems [33].

The interconnection problem originating from the global instruction flow can be solved by a so-called "Propagate Instruction Processor " (PIP) [17]. The PIP differs from a classical SIMD-processor in the sense that the instructions are pipelined in horizontal direction while the PIP elements perform their computations (figure 12a). Thus, multiple image processing algorithms are simultaneously solved in parallel. Although not going into details the pipelined operation improves the overall system performance as it was previously indicated by bit-level systolic arrays for arithmetic computations.

To store the propagating instructions each processing element contains a local instruction pipeline regis-

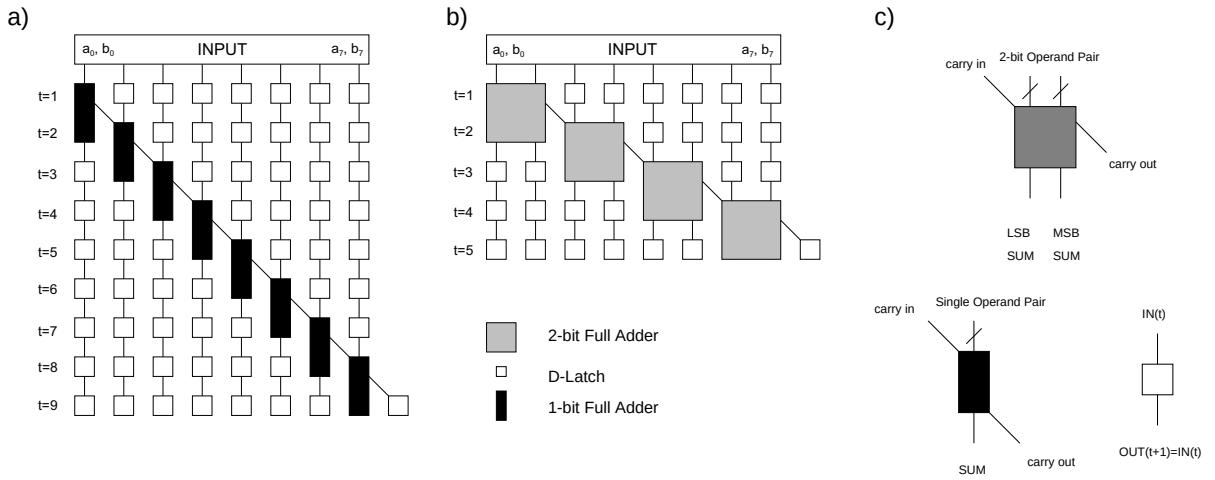

Figure 11: Bit-level systolic ripple carry adder (a), improved design with 2-bit operand addition (b), and cell input/output (c). Each cell is a threshold logic circuit with embedded RTT D-latch.

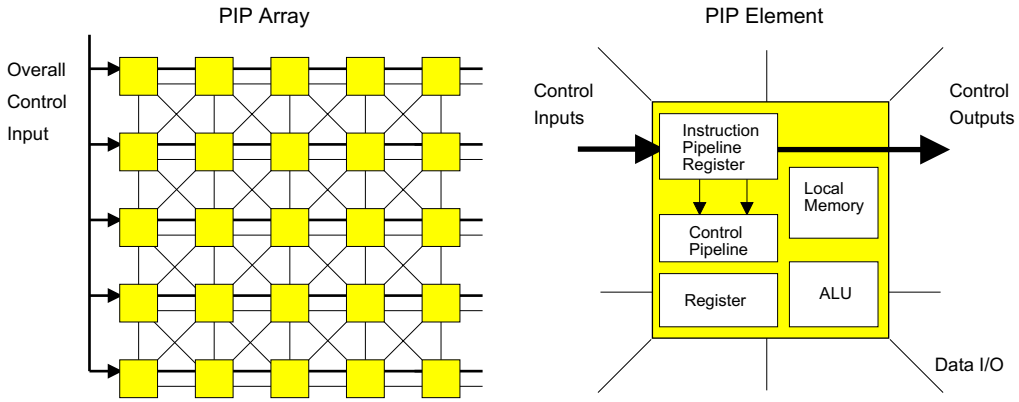

Figure 12: Propagate instruction processor.

ter. Further components are the local memory, a control pipeline, a register, and the arithmetic logic unit (figure 12). The size and the capabilities of a single processing element depends on the complexity of the algorithms and the image resolution.

5.3. Reliability and fault tolerant logic

Fault-tolerant computing schemes are a prerequisite for the reliable operation of future giga-scale integrated circuits. In SET-circuits and QCA's the background charge sensitivity is the principal reason for failures during the computation. If the fabrication tolerances and the resulting deviation of the electrical device parameters from their nominal values are also considered it is very likely that most of today's nanoelectronic devices that are tested in laboratories are not yet suitable for industrial production. Despite of remarkable progress of fabricating reproducible and homogeneous layer structures in the field of RTD's (standard deviations of the peak current and peak voltage below 5% have been reported [44], [12]) the intended lateral scaling of the RTD area into the nm-regime requires fault tolerant logic schemes, too.

In view of similar problems caused by dopant fluctuations in nm-scale MOSFET's this assumption seems to be also valid for future generations of CMOS technology [4], [25] if the threshold voltage is decreased to V_{th} =0.1V.

One of the classical techniques for error correction in logic circuits is triple modular redundancy [18]. Here, fault tolerant behavior is achieved by three identical modules of the logic circuit. The three modules compute the Boolean function simultaneously. Since at least two of the modules compute the same result a majority voter selects the correct output provided that this majority logic operates correct and only one error occurs in the previous stage. The QCA-majority gate being mentioned previously (cf. figure 9e) is an efficient implementation of the voting logic for fault tolerant quantum dot architectures. If the mean error rate of

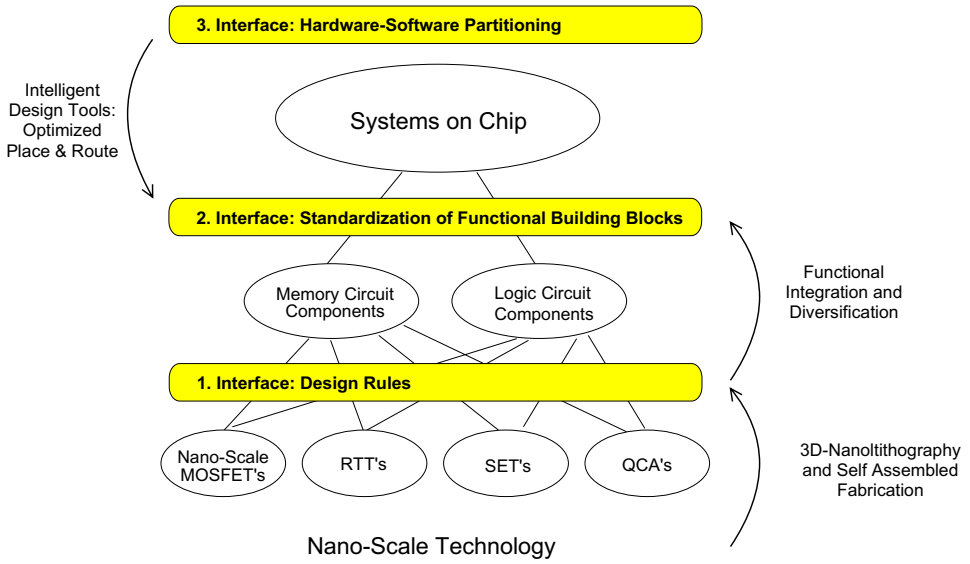

Figure 13: Design hierarchy for nano-scale systems.

a nano-scale circuit technology is larger and one-fault tolerance is not sufficient it might be necessary to cascade triple modular redundant circuits (i.e. triple-triple modular redundancy) [16].

Obviously, the additional circuit overhead, that is three logic circuit instead of one, increases the area of the fault tolerant circuit by at least a factor of three. Thus, the overall increase of the integration density will not automatically contribute to an overall performance increase because a significant number of devices is consumed only to improve the reliability of the circuits. If triple modular redundancy is implemented in a time multiplexed way, that is recomputing the logic function with triplication and voting [58], the area overhead is traded off for a threefold increased latency.

Other well known methods for error detection are algebraic codes and parity prediction where additional information is coded and processed together with the operands [40]. Whenever a disagreement between predicted and processed results occurs, a comparison logic indicates an error.

6. Conclusion and outlook

The industrial relevance of nanoelectronics strongly depends on the silicon compatibility of the devices. Especially for RTT's the challenge is to transfer the circuit architectures developed on III-V based semiconductors to Si-based technology. In the scope of the Advanced Microelectronics Initiative the European Commission has already started several project aiming at investigating Si-Ge RTD's and RTT based circuit design [13].

The most serious problem towards silicon RTT's is the availability of heterostructures with a sufficient barrier height [53]. Due to their large bandgap difference the Si-SiO_2 interface would be an optimal solution [55], [28].

For the next decade the main challenges on the field of nano-scale circuit design are the design complexity caused by the tremendous number of devices, the specification of an adequate design style because of quantum mechanical device phenomena, and the critical interconnection problem.

As we have pointed out nano-scale circuits composed of RTT's, SET's, or QCA's have very different electrical properties. One consequence of this might be that an increase in performance will be caused by an extended diversification if a specific application is implemented with the most suited category of devices (Table 1, figure 13). Regarding the evolution from CMOS dominated microelectronics to nanoelectronics this assumption seems reasonable when considering the general development of an innovative and expanding technology towards a more mature level, where the economic relevance has reached its maximum.

To handle such an increased diversification and to cope with the design complexity it is to expect that intelligent design tools become more and more indispensable within the hierarchical design flow.

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