Defect-Tolerant Molecular Electronics

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The integrated circuit, manufactured by optical lithography, has driven the computer revolution for four decades. If we are to continue to build complex systems of ever-smaller components, we must find a new technology that will allow massively parallel construction of electronic circuits at the atomic scale. To do so we must develop both the molecular electronics building blocks and CAD algorithms for such a reconfigurable technology.

The technical problem we face is to make extremely small electronic components (at the atomic scale), use very large numbers of these components to make very complex circuits, but manufacture these circuits at much less cost than today's integrated circuits. This requires many disciplines to work together. To make them function at the smallest scales we use quantum physics. To achieve massive complexity we use computer architecture. To keep them inexpensive we use low mechanical precision and do self-assembly with chemistry. And to deal with the inevitable defects of chemical self-assembly we use defect tolerant design algorithms.

One potentially scalable device consists of two crossed nanowires sandwiching an electrically addressable molecular species. The approach is extremely simple and inexpensive to implement, and scales from wire dimensions of several micrometers down to nanometer-scale dimensions. This structure can be used to produce crossbar switch arrays, logic devices, memory devices, and communication and signal routing devices. The device is either partially or completely chemically assembled, and the key to the scaling is that the location of the active devices on the substrate are defined after the devices have been assembled, not prior to assembly. This architectural approach allows us to address the functions of interconnect, memory, logic and I/O.

The key task of the architectural community in the immediate future is to develop a sense of the trade-offs between the computational costs of CAD algorithms to repair defects and the manufacturing costs of avoiding defects in the first place. Biology has struck one balance. We need to find the balance for nanotechnology.

Biography: Philip J. Kuekes

Philip Kuekes is chief architect in Quantum Science Research at Hewlett-Packard Laboratories in Palo Alto, California. He has developed various architectures for chemically assembled electronic nanocomputers for the the HP-DARPA Moletronics program. He was project manager for Teramac, a trillion operations per second reconfigurable computer that was the largest defect-tolerant machine ever made. He holds fourten patents in molecular electronics and parallel computer architectures. He received the 2000 Feynman Prize in Nanotechnology (with James R Heath and R. Stanley Williams). He was a member of the National Academies Committee for the Review of the National Nanotechnology Initiative. He was named to the 'Scientific American 50' list of technology leaders for 2002.

In 1990 he was Director of Architecture at Plus Logic, Inc., a Field Programable Gate Array startup company. He defined Plus Logic's next FPGA family including intelligent memory combined with programmable logic.

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In the 1980's he was with TRW. He was Principal Investigator and Architect of the MOSAIC processor, a ten gigaflop heterogeneous supercomputer developed as part of the DARPA/ISTO Strategic Computing Initiative. (1989) Directed a hardware and software development team to create both a gigabyte per second crossbar switch and the dataflow based CAD system to allow a variety of application specific supercomputers to be rapidly configured. He was Principal Investigator and Architect of TRW's Systolic Adaptive Beamformer, a 350 Megaflop linear algebra processor. (1986) This special purpose processor funded by DARPA/NTO and the Navy, went to sea in an experiment using adaptive beamforming in towed hydrophone arrays. He was Program Manager and Architect of the Phoenix Systolic Processor (1981), the first high performance, 280 mega-ops, systolic processor.

From 1974 through 1979 he had a consulting practice, designing hardware and microcode for highly pipelined systems. Clients included: NCR Corporation, Ling Electronics, National Severe Storms Center. From 1972 he was a Project Engineer with Ling Electronics responsible for the Ling Array Processor, a state of the art array processor for vibration testing. In 1970 he was co-designer of the first commercial array processor at Ratheon Computer.

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