Quantum Cellular Automata: New Defects and Faults for New Devices

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Abstract

There has been considerable research on quantum cellular automata (QCA) as a new computing scheme in the nano-scale regimes. In this paper, a detailed simulation-based characterization of defects in different QCA logic and interconnect devices and study of their effects at logic-level are presented. Various failure mechanisms which can potentially happen during nano-manufacturing of these devices have been considered and simulated. Different implementations of QCA logic devices and interconnects are also compared in term of defect tolerance and testability. The same study is performed for new proposed QCA devices too. The simulation results show that additional fault models at logic level must be considered for testing of QCA-based circuits.

1 Introduction

There has been extensive research in recent years to propose novel devices at nano scale to overcome the fundamental problems facing lithography-based CMOS technology due to exponential shrinkage. Among these new devices, *quantum cellular automata* (QCA) not only gives a solution at nano scale, but also it offers a new method of computation and information transformation [9]. In terms of feature size, it is projected that a QCA cell of few nanometer size can be fabricated through molecular implementation by a self-assembly process.

The unique feature of QCA based designs is that logic states are not stored in voltage levels as in conventional electronics, but they are represented by the position of individual electrons.

One of the interesting features of this technology is that it is possible to investigate some of the potential manufacturing defects at nano scale without manufacturing these devices. This can be done based on quantum-mechanics simulation of these devices. So the behavior of these devices at nano scale in the presence of manufacturing defects can be studied through manufacturing-independent simulations. Although a full characterization requires real manufacturing parameters, this type of simulation gives a realistic perspective for a possible test roadmap for this technology.

For QCA the cells must be aligned precisely at nano scales to provide correct functionality, so proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of these circuits.

The basic logic element in this technology is the majority voter. Logic AND and OR can be realized with this gate. We have presented a more complex QCA logic gate, the so-called AOI (And-Or-Inverter) gate, which is able to implement all one-level and most of 2-level logic cells.

In this paper, the simulation-based defect characterization of QCA devices, inclusive of logic devices (majority voter and AOI gate) and interconnection devices (binary wire and inverter chain) has been extensively studied; the effects of defects at logic-level are investigated. Appropriate QCA fault models are derived and compared with conventional fault models in CMOS technology. Different device-level implementation of QCA logic devices are also evaluated in terms of defect tolerance and testability.

The rest of this paper is organized as follows. In Sec. 2, a review of QCA is presented. In Sec. 3 we discuss the defect characterization for QCA and its failure modes. The defects for a basic QCA gate (majority voter) and interconnects are analyzed in Sec. 4 and 5 respectively. In Sec. 6 we present the defect characterization for the QCA AOI gate. Finally, Sec. 7 concludes the paper.

2 Review

QCA is a novel nano device that stores logic states not as voltage levels but rather based on the position of individual electrons. A quantum cell can be viewed as a set of four charge containers or dots, positioned at the corners of a square. The cell contains two extra mobile electrons which can quantum mechanically tunnel between dots, but

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not cells. The electrons are forced to the corner positions by Coulomb repulsion. The two possible polarization states represent logic “0” and logic “1”, as shown in Fig 1.

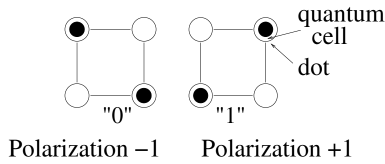
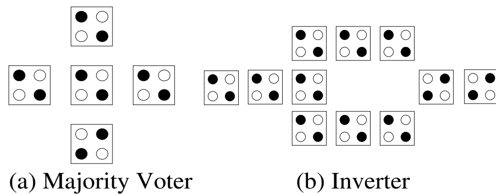


Figure 1. QCA cell polarization

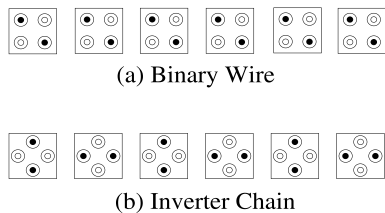
The basic logic gates in QCA are the *majority voter* (MV) and the Inverter (Figure 2). The MV with logic function $Maj(A, B, C) = AB + AC + BC$ can be realized by only 5 QCA cells [9]. Logic AND and logic OR functions can be implemented from a majority voter by setting one input permanently to 0 and 1, respectively. Various logic design using MVs and Inverters have been demonstrated in [1][7][9].



(a) Majority Voter (b) Inverter

Figure 2. Basic QCA devices

Unlike conventional CMOS in which the Inverter is the simplest block, it consumes considerable area in QCA. The ratio of the number of transistors for AND to NOT in CMOS technology is 6/2, while the ratio of the number of cells in QCA technology is 5/12. The binary wire (as interconnect) and the inverter chain are shown in Fig. 3.



(a) Binary Wire

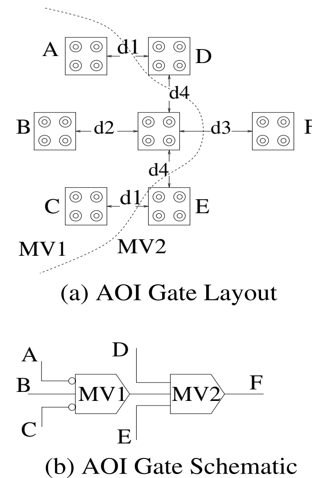
(b) Inverter Chain

Figure 3. Binary wire

Although MV can be easily adapted to realize AND or OR, it suffers from the disadvantage that it is not an universal gate and can not offer the inverting function. This motivated us to build a complex QCA gate with embedded AND, OR and INV functions, and with better usability for synthesis [8]. The device has to be stable, which means that: (1) the output must exhibit a definite polarization; (2) small displacements of individual cells should not change the logic function of the device, i.e. the device should provide certain degree of tolerance to faults and defects; (3) wiring of the device should not change the logic function.

Table 1. Cell placement in the AOI (not wired) gate

$d1$ nm	$d2$ nm	$d3$ nm	$d4$ nm
20	30-40	20-40	20
25	30-40	20-40	20
30	35-40	20-40	20
25	35-40	25-40	25
30	35-40	25-40	25



(a) AOI Gate Layout

(b) AOI Gate Schematic

Figure 4. The AOI gate

The AOI (And Or Inverter) gate is a 5 input flexible gate that offers all elementary logic functions, and can be programmed to realize a variety of logic functions. The layout and corresponding logic schematic is illustrated in Figure 4. The logic function realized by the AOI gate is:

$$\begin{aligned} F &= DE + (D+E)(\overline{A}\,\overline{C} + \overline{A}B + B\overline{C}) \\ &= DE + D\ Maj(\overline{A}, B, \overline{C}) + E\ Maj(\overline{A}, B, \overline{C}) \\ &= Maj(D, E, Maj(\overline{A}, B, \overline{C})) \qquad (1) \end{aligned}$$

where $Maj()$ is the 3-input majority function. By simulation we have found that this AOI gate is relatively stable, i.e. moving marginally the cells does not change its function. We have found that the placement in Table 1 (see Figure 4) yields an AOI gate performing the function described above. In this paper we use a semi-symmetric and stable configuration with $d1$=$d3$=$d4$=$25nm$, $d2$=$35nm$.

The AOI gate is logically equivalent to a concatenation of two MVs with 2 complemented inputs (A and C). From the layout of the AOI gate we can see that this gate can be viewed as two-nested MVs.

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If we set some of the inputs of the AOI gate as programming inputs, we can configure the AOI gate to perform a variety of logic functions, some of these functions are shown in Figure 5. Therefore the AOI gate is universal and offers flexibility for design implementation.

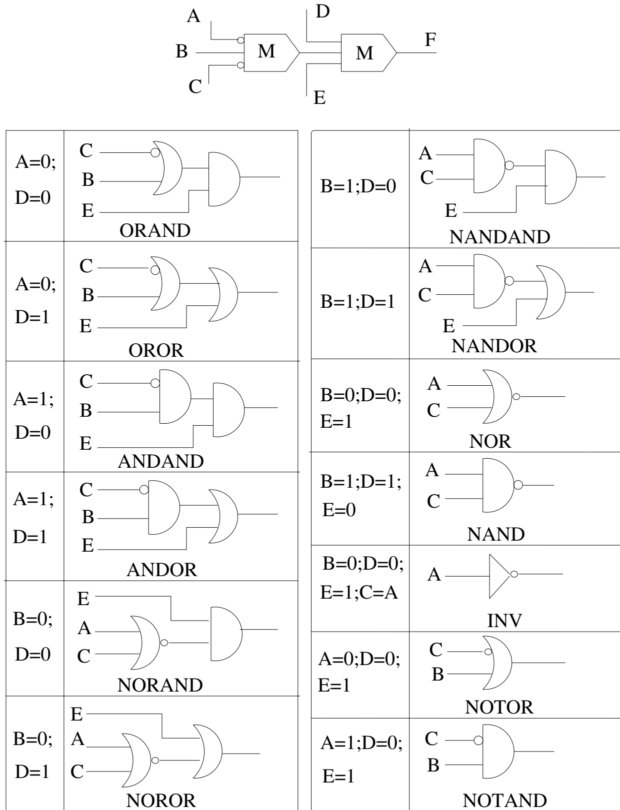
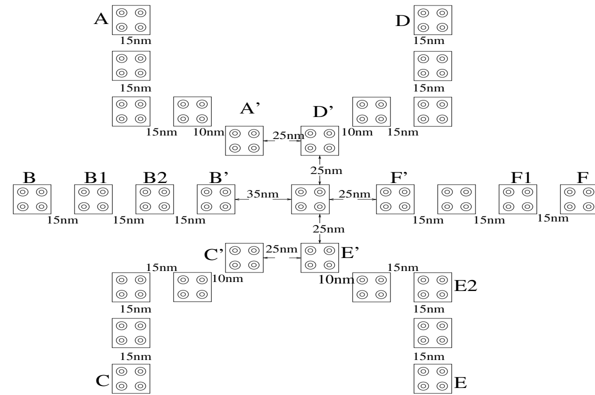


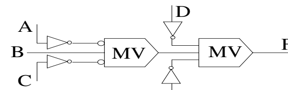
Figure 5. Various logic function realized by an AOI gate

The characterization of the logic block must be considered while the inputs are connected to QCA binary wires. Wiring of the AOI gate has been investigated while still preserving the original logic function. The proposed wiring scheme is shown in Figure 6, the active AOI gate has $d1$=$d3$=$d4$=$25nm$, $d2$=$35nm$.

The main challenge in wiring the AOI gate is to separate the input/output binary wires such that they do not interfere with each other, so we have placed the wires apart to reduce interference among the wire cells. By simulation we have found that the wire for cell A and D (also C and E) must have a distance of more than $25nm$, hence the device is wired as shown in Figure 6, and wiring for inputs A,B,C and D has inverting effects. This is shown as extra inverters for these inputs in Figure 6. Based on simulation, the AOI gate with the above wiring scheme has been found to be quite stable.



(a) Wired AOI Gate



(b) Schematic of Wired AOI Gate

Figure 6. Wired AOI gate

3 Defect and Failure Modes

Various configurations of QCA devices have been studied using the QCADesigner[1] v1.20 simulation tool. For accuracy, the bistable model is used, i.e. a quantum mechanical engine using Jacobi algorithm to calculate the eigenvalues/vectors of the Hamiltonian.

To perform a defect characterization of QCA devices and circuits and study their effects at logic-level, appropriate defect mechanisms and models must be considered which 1) can be simulated using available simulation methods and 2) are realistic to model manufacturing and fabrication defects.

Definition 3.1 A *cell displacement* is a defect in which the defective cell is misplaced within its original direction. Several cell displacement defects are shown in Fig. 7.

Definition 3.2 In a *cell misalignment* defect, the direction of the defective cell is misplaced. Some examples of cell misalignments are shown in Fig.8.

Definition 3.3 In a *cell omission* defect, a particular cell is missing as compared to the original (defect-free) arrangement.

In this paper, the following defects are simulated for QCA devices: all possible combinations of cell displacement with respect to the central cell under different distances, cell misalignment in different directions, and rotation. For QCA majority voter and interconnects, cell omission defects are also simulated.

[1]QCADesigner is the product of an ongoing collaboration between the ATIPS laboratory and University of Notre Dame.

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Cell omission is a special case of the defects such as in the number of dots or electrons. Note that a missing dot (or additional dot) is very unlikely due to the ease of purification of small inorganic molecules, e.g. Nuclear Magnetic Resonance (NMR) has an estimate minimum purity of 99% for model compounds such as the Creutz-Taube Ion (a 2-dot cell model) [6]. Moreover, electrochemical measurements for the CT Ion show that fewer than one molecule in 10^5 are in the incorrect charge state. Another instance of such defects is a defective cell with 1 electron in a binary wire, which behaves as an inverter.

4 Majority Voter Defect Analysis

There has been a study of the fault tolerant properties of the MV under some manufacturing misalignments [2, 3, 4]. Based on this simulation study, a fault tolerant MV block has been proposed. It has been shown that MV is more vulnerable to misalignment in the vertical direction than in the horizontal direction.

In this work, different defects in the MV (cell displacement and misalignment) are considered and simulated. The faulty results for cell displacement and misalignment are shown in Table 2 and 3, respectively. Only faulty entries are shown in the tables. The considered defect free majority voter has a $5nm$ dot and a $20nm \times 20nm$ cell size, with a $5nm$ cell distance.

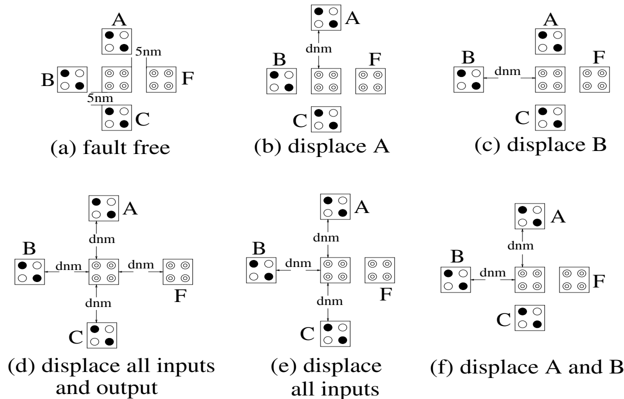

Figure 7. Displacement in Majority Voter

The data shows that in most cases the horizontal input cell (i.e. cell B) is the dominant cell. For misalignment, any single cell misalignment greater or equal to half a cell causes malfunction (fault at logic-level). In some cases the error margin is even smaller.

Cell omission defect on the horizontal input cell (i.e. cell B) does not affect the functionality. However, a cell omission defect on any of the vertical inputs (cell A or C) causes the output to be dominated only by the horizontal input, i.e. the output is shorted to the horizontal input.

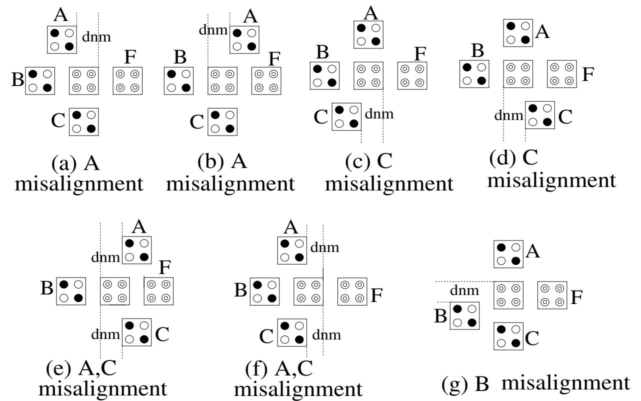

Figure 8. Misalignment in Majority Voter

The cell omission defect on the center cell of a majority voter with vertical input values a and b, and horizontal input value c changes the function to be the majority of a', b', and c. This can be interpreted as unwanted complementation faults on both vertical inputs.

4.1 Defect Analysis of Rotated Majority Voter

The simulation results show that MV is robust with respect to rotation of all input and output cells around the center cell, i.e. the logic-level behavior of the rotated MV is the same as the original device. Based on this observation, some simulations are performed to investigate the robustness of the Rotated MV (RMV). The basic functionality of MVs is based on the Coulombic interaction among four neighboring QCA cells, which strongly depends on the precision and geometry of its implementation. We focus on validating different configurations of MV in the 45° rotation, as shown in Fig. 9.

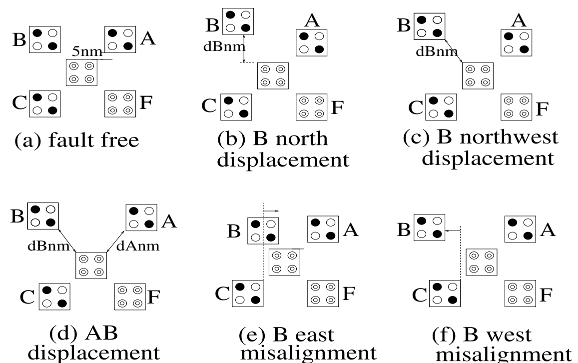

Figure 9. Rotated Majority Voter (fault-free, with displacement or misalignment)

The simulation results show that the RMV functions nor-

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Table 2. Results for displacement in Majority Voter

displace cell A: fig 7(b)			
$d \leq 15nm$ Normal Operation		$d \geq 20nm, F = B$	
displace cell B: fig 7(c)			
$d \leq 40nm$		$d \geq 45nm$	
Normal Operation		ABC	F
		001	Z (no polarization)
		011	Z(no polarization)
		100	Z (no polarization)
		110	Z (no polarization)
displace all input/output cells: fig 7(d)			
$d \leq 10$ or $30 \leq d \leq 40nm$		$15 \leq d \leq 25nm$	
Normal Operation		ABC	F
$d \geq 45nm$		010	0/1
$F = Z$ (no polarization)		101	1/0
displace all input cells: fig 7(e)			
$d \leq 15$ or $d = 40nm$		$d \geq 45nm$	
Normal Operation		$F = Z$ (no polarization)	
$20 \leq d \leq 25$ or $d = 35nm$		$d = 30nm$	
ABC	F	ABC	F
010	0/1	000	0/1
101	1/0	010	0/1
		101	1/0
		111	1/0
displace cells A and B: fig 7(f)			
$d \leq 5nm$ Normal Operation		$d \geq 10nm, F = C$	

mally, except when moving:

- A input north, with $dA \geq 10nm$ for $ABC = 001, 110$ (the output follows the C input). A similar output appears when moving A to northeast with $dB \geq 10\sqrt{2}nm$.
- B input north, with $dB \geq 40nm$. The output is unknown (unpolarized) for $ABC = 001, 011, 100, 110$. A similar output appears when moving B to the northwest with $dB \geq 30\sqrt{2}nm$.
- C input south, with $dC \geq 15nm$ for $ABC = 011, 100$ (the output follows the A input). A similar output appears when moving C to the southwest with $dC \geq 10\sqrt{2}nm$.
- A, B, C or A, B, C, F away for $d \geq 30\sqrt{2}nm$. The output is undefined for all input combinations.
- A and B inputs away with $d \geq 10\sqrt{2}nm$ for $ABC = 001, 110$ (the output follows the C input).
- A and C inputs away with $d \geq 10\sqrt{2}nm$ for $ABC = 010, 101$ (the output follows the B input).
- B and C inputs away with $d \geq 10\sqrt{2}nm$ for $ABC = 011, 100$ (the output follows the A input).

Cell misalignment defects for RMV are also considered (e.g., Fig. 9(e,f)). The following shows the results:

- Shifting the input A west (half/full cell size), leads the output F to follow input A, while shifting A east effects the output such that it follows input C.
- RMV functions normally when input B is shifted west for a half or full cell size. However, the output is undefined for inputs $ABC = 001, 011, 100, 110$ when $dB \geq 40nm$.
- The output follows the input B, when B is shifted east for a half or full cell size.
- The output follows the input A when C is shifted west, and follows C when C is shifted east.

Table 3. Results for misalignment in Majority Voter

move A toward west: fig 8(a)			
$d \leq 5nm$ Normal Operation		$d \geq 10nm, F = B$	
move A toward east: fig 8(b)			
$5 \leq d \leq 15nm$		$d = 20$ or $d = 30nm$	
ABC	F	Normal Operation	
001	0/1		
010	0/1	$d = 25nm$	
101	1/0	$F = A$	
110	1/0		
move C toward west: fig 8(c)			
$d \leq 5nm$		$d \geq 10nm$	
Normal Operation		$F = B$	
move C toward east: fig 8(d)			
$5 \leq d \leq 15nm$		$d = 20$ or $d = 30nm$	
ABC	F	Normal Operation	
010	0/1		
011	1/0	$d = 25nm$	
100	0/1	$F = C$	
101	1/0		
move A, C toward west: fig 8(e)			
$d \geq 5nm$ $F = B$			
move A, C toward east: fig 8(f)			
$d = 5, 20, d \geq 30nm$		$10nm \leq d \leq 15nm$	
$F = B$		ABC	F
$d = 25nm$		000	0/1
Normal Operation		010	0/1
		101	1/0
		111	1/0
move B toward south/north: fig 8(g)			
$d \leq 5nm$		$d \geq 45nm$	
Normal Operation		ABC	F
		001	0/1
		011	1/0
		100	0/1
		110	1/0

4.2 OMV and RMV Comparison

The results for different configurations of the Original Majority Voter (OMV) and the Rotated Majority Voter (RMV) are illustrated in Table 4. MV is completely robust with respect to rotation of all inputs and output cells around the central cell. This gives a significant degree of freedom for synthesizing designs based on QCA, as RMV can be used as the Original Majority Voter block. However, the original block is more dependent on the middle input (B) than the other inputs (A and C), in terms of displacement and misalignment. In the rotated version, this dependency can be completely changed based on the degree of rotation. An overall comparison in the table confirms that RMV is more fault-tolerant than the OMV. Note that only half and

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full misalignments are considered.

Table 4. Original Majority Voter vs. Rotated Majority Voter

Config.	Faults	OMV	RMV
A move	distance	$d \geq 20nm$	$d \geq 10$(N) or $10\sqrt{2}nm$ (NE)
	# of faults	2	2
B move	distance	$d \geq 45nm$	$d \geq 40$(W) or $30\sqrt{2}nm$ (NW)
	# of faults	4	4
C move	distance	$d \geq 20nm$	$d \geq 10$(S) or $10\sqrt{2}nm$ (SW)
	# of faults	2	2
ABC move	distance	$20 \leq d \leq 35$ or $d \geq 45nm$	$d \geq 30\sqrt{2}nm$
	# of faults	2/4/8	8
$ABCF$ move	distance	$15 \leq d \leq 25$ or $d \geq 45nm$	$d \geq 30\sqrt{2}nm$
	# of faults	2/8	8
AB move	distance	$d \geq 7.5nm$	$d \geq 10\sqrt{2}nm$
	# of faults	2	2
AC move	distance	$d \geq 7.5nm$	$d \geq 10\sqrt{2}nm$
	# of faults	2	2
F move	distance	$d \geq 45nm$	$d \geq 30\sqrt{2}nm$
	# of faults	8	8
AC misalignment	# of faults	4	4
B misalign. West	# of faults	4	0
B misalign. East	# of faults	4	2

5 Interconnect Defects

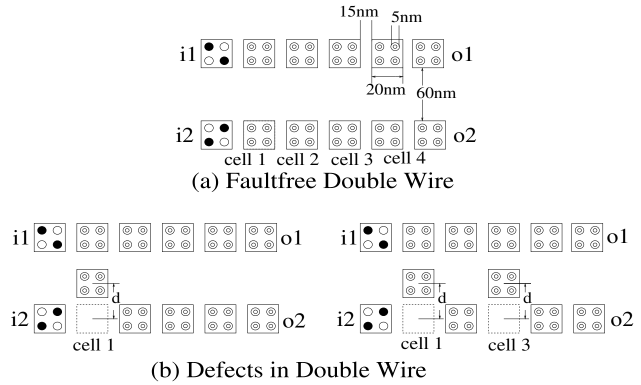
The effect of cell displacement defects on two parallel binary wires as well as two parallel inverter chains are investigated.

5.1 Double Binary Wires

Two defect-free binary wires are shown in Fig. 10(a); the wires are denoted as the upper wire ($i1$ to $o1$) and the lower wire ($i2$ to $o2$). The cells have a size of $20nm \times 20nm$, and the dot diameter is $5nm$. In the defect-free case, the cells in the same wire are separated by $15nm$ and the wire distance is $60nm$.

The displacement defects are simulated by moving one or two cells in the lower wire toward the upper wire (by displacement d) as shown in Fig. 10(b).

The simulation results are shown in Table 5. The results show that the upper wire is dominant in most cases: $o1$ and $o2$ are either equal to $i1$ or $i1'$, depending on which cell(s) are displaced and the value of the displacement, d. In most cases, the upper wire functions normally, i.e. $i1 = o1$. However, in some cases the upper wire behaves as an inverter. Clearly, unlike CMOS designs, the coupling defects at QCA device-level do not behave as the *wired bridging fault* model. However, these defects manifest themselves as



(a) Faultfree Double Wire

(b) Defects in Double Wire

Figure 10. Displacement in Binary Double Wires

Table 5. Results for Double Binary Wires

move cell1 OR cell2				
$d \leq 40nm$ Normal	$d = 45 - 50nm$ $o1 = i1, o2 = i1$	$d \geq 55nm$ $o1 = i1, o2 = Z$		
move cell3 OR cell4				
$d \leq 35nm$ Normal	$d = 40 - 50nm$ $o1 = i1, o2 = i1'$	$d \geq 55nm$ $o1 = i1, o2 = Z$		
move cell1 AND cell2				
$d \leq 35nm$ Normal	$d = 40 - 50nm$ $o1 = i1, o2 = i1$	$d \geq 55nm$ $o1 = i1, o2 = Z$		
move cell1 AND cell4; OR move cell 2 AND cell 3; OR move cell3 AND cell4				
$d \leq 35nm$ Normal	$d = 40 - 50nm$ $o1 = i1, o2 = i1'$	$d \geq 55nm$ $o1 = i1, o2 = Z$		
move cell1 AND cell3				
$d \leq 35nm$ Normal	$d = 40 - 50nm$ $o1 = i1, o2 = i1$	$d = 45nm$ $o1 = i1, o2 = i1'$	$d \geq 55nm$ $o1 = i1, o2 = Z$	
move cell2 AND cell4				
$d \leq 15nm$ Normal	d=20-25nm d=40-45nm $o1 = i1$	d=30-35nm $o1 = i1$ $o2 = i1$	$d = 50nm$ $o1 = i1'$ $o2 = i1$	$d \geq 55nm$ $o1 = i1$ $o2 = Z$

the dominant model (at logic level) in which the output of a wire is determined by the value of the coupled wire.

Removing a single cell from a binary wire does not affect its functionality at logic-level although it may result in some delay faults. In some cases if the cell distance is far (e.g. 15nm in a binary wire with $20 \times 20nm$ cell size), cell omission results in the non-conductivity of the wire. Those L shape binary wires (which change direction in the layout) are very sensitive to the defects on the corner cells. Cell omission defect at the corner cell is equivalent to unwanted complementation fault at logic-level.

5.2 Double Inverter Chains

The double inverter chain is shown in Figure 11(a). The simulation results for moving one cell in the bottom wire toward the upper wire, with displacement d, (Figure 11(b))

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are presented in Table 6. The displacement defects behave as the *dominating bridging fault* model at logic level. Moreover, a comparison with the binary wires shows that binary wires are more defect tolerant than inverter chains for the case of displacement coupling defects.

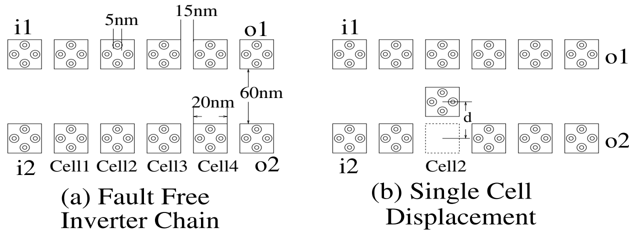

Figure 11. Displacement in Double Inverter Chains

Table 6. Results for Double Inverter Chains

Fault Free: $o1 = i1'$; $o2 = i2'$		
move cell1 OR cell2 OR cell3		
$d \leq 35nm$ Normal	$d = 40nm - 50nm$ $o1 = i1', o2 = i1'$	$d \geq 55nm$ $o1 = i1', o2 = Z$
move cell4		
$d \leq 30nm$ Normal	$d = 35nm - 50nm$ $o1 = i1', o2 = i1'$	$d \geq 55nm$ $o1 = i1', o2 = Z$

A single cell omission in a wire implemented as an inverter chain results in an unwanted complementation at the output of the chain.

6 Defect Characterization of the AOI gate

In this section, the robustness of the AOI gate is investigated. We have simulated cell displacements with respect to the central cell under different distance conditions. Studying the behavior of the AOI gate in the presence of cell displacements not only helps to establish its fault tolerance property but also it gives an insight into cell interactions within the AOI gate structure.

First we move the input and output cells of the AOI gate with respect to the center cell and record the logic function performed by the AOI gate. The simulation results are shown in Table 7.

It can be observed from the simulation results that if we fix $d1$, $d4$ and gradually increase $d2$, $d3$, several defect patterns occur. An important result is that the horizontal input (Cell B) has greater influence on the center device cell than the other inputs, which confirms our results of Sec. 4. We can see that when $d2$ is sufficiently small (i.e. Cell B is sufficiently close to the center cell), then the output is $F = B$. All other inputs have no effect on the output. For this reason in the fault free AOI

Table 7. AOI gate defect characterization

d1	*d4*	*d2*	*d3*	Output Function F
20	20	5-10	5-40	
		15	15-40	
		20	20	B
		15	5-10	
		20-25	5-15	$\overline{D}\,\overline{E} + B\overline{D} + B\overline{E} = M(B, \overline{E}, \overline{D})$
		20	30-40	
		25	25-40	$DE + BE + BD = M(B, D, E)$
		20	25	
		25	20	$\overline{A}B\overline{C} + \overline{A}DE + \overline{C}DE + BE + BD$
		30-40	5-15	$\overline{D}\,\overline{E} + (\overline{D} + \overline{E})(\overline{A}B + B\overline{C} + \overline{A}\,\overline{B}\,\overline{C})$
		30-40	20-40	Normal Operation
25	20	5-10	5-40	
		15	15-40	
		20	20	B
		15	5-10	
		20-25	5-15	$\overline{D}\,\overline{E} + B\overline{D} + B\overline{E} = M(B, \overline{E}, \overline{D})$
		20	25-40	
		25	20-40	$DE + BE + BD = M(B, D, E)$
		30-40	5-15	$\overline{D}\,\overline{E} + (\overline{D} + \overline{E})(\overline{A}B + B\overline{C} + \overline{A}\,\overline{B}\,\overline{C})$
		30-40	20-40	Normal Operation
30	20	5-10	5-40	
		15	15-40	
		20	20	B
		15	5-10	
		20-30	5-15	$\overline{D}\,\overline{E} + B\overline{D} + B\overline{E} = M(B, \overline{E}, \overline{D})$
		20	25-40	
		25-30	20-40	$DE + BE + BD = M(B, D, E)$
		20	25-40	
		35-40	5-15	$\overline{D}\,\overline{E} + (\overline{D} + \overline{E})(\overline{A}B + B\overline{C} + \overline{A}\,\overline{B}\,\overline{C})$
		35-40	20-40	Normal Operation
25-30	25	5-10	5-40	
		15	15-40	
		20	20-40	
		25	25	B
		15	5-10	
		20	5-15	$\overline{D}\,\overline{E} + B\overline{D} + B\overline{E} = M(B, \overline{E}, \overline{D})$
		25-30	5-20	
		25	30-40	
		30	25-40	$DE + BE + BD = M(B, D, E)$
		35-40	5-20	$\overline{D}\,\overline{E} + (\overline{D} + \overline{E})(\overline{A}B + B\overline{C} + \overline{A}\,\overline{B}\,\overline{C})$
		35-40	25-40	Normal Operation
		≥45		For some input combinations $F = Z$(no polarization)
			≥45	For all input combination $F = Z$(no polarization)

gate, cell B is placed further apart than the other input cells. As we increase the distance between B and the center cell (as shown in Table 7), the AOI gate behaves as a MV with $F = DE + BE + BD = M(B, D, E)$ or a MV with inversions at some inputs with $F = \overline{D}\,\overline{E} + B\overline{D} + B\overline{E} = M(B, \overline{E}, \overline{D})$, depending on the distance between the output cell F and the center device cell. In these two configurations, cell B is closer to the center cell than in the fault-free AOI, thus it has a bigger effect on the center cell, eliminating the effects of A and C. Thus thus the AOI gate acts as the MV with inputs B, D and E. When $d2$ is further increased the effects of A and C begin to show, the faulty patterns of $F = \overline{A}B\overline{C} + \overline{A}DE + \overline{C}DE + BE + BD$ and $F = \overline{D}\,\overline{E} + (\overline{D} + \overline{E})(\overline{A}B + B\overline{C} + \overline{A}\,\overline{B}\,\overline{C})$ can be observed. From the results we can see that in all cases when $d3 \geq 45nm$ (i.e. the output cell is placed far apart from

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the center cell), there's no polarization for F with any input combination, which is indicated by $F = Z$ in the table. Also we observe that when B is placed far away from the center cell ($d2 \geq 45nm$), some input combinations cause the output to show no polarization at all. These results are consistent because in QCA, information is transmitted via Coulomb interactions, larger the distance between two cells, weaker the interactions.

As mentioned above, for AOI gate we need to separated wires to avoid interference, therefore investigating the effect of wire bridging faults in AOI gate become important. The displacement defects are simulated by moving a cell in the wiring of the AOI gate. The simulation results show that, unlike CMOS designs, the coupling effects at QCA device-level do not always behave as the *wired bridging fault* model. Some of these results are shown in Table 8. Note that A', B', C', D', and E' are device input cells in defect-free wired AOI gate, where $A' = \overline{A}, B' = B, C' = \overline{C}, D' = \overline{D}$, and $E' = \overline{E}$ (Figure 6).

The simulation results show that in case of coupling effects, either *unwanted complementation* fault is observed or the output is dominated by the coupling input.

Table 8. Coupling faults in AOI wiring

Config. in Fig. 6	Distance (nm)	Faults
Move $B1$ south	5-30	Normal Operation
	35-55	$C' \leftarrow C$
Move $B2$ south	5-30	Normal Operation
	35-55	$C' \leftarrow C$
Move $F1$ south	5-50	$E' \leftarrow E, F \leftarrow E$
	5-50	$E' \leftarrow E, F \leftarrow \overline{E}$
	≥ 55	$E' \leftarrow E, F \leftarrow Z$ (no polarization)
Move $E2$ north	5	$E' \leftarrow E, F \leftarrow E$
	10-40	$E' \leftarrow E, F \leftarrow \overline{E}$

7 Conclusions

Quantum cellular automata (QCA) are novel devices which are promising in the era of nano scale computing. In this paper, a detailed simulation-based defect characterization for QCA logic and interconnect devices has been presented. Various failure mechanisms which can potentially happen during nano-manufacturing of these devices, have been considered and simulated. These include cell omission, misplacement and misalignment.

Simulation results show that the behavior of QCA defects at logic level (i.e. faults) is not similar to conventional faults in CMOS technology. For example, an *Unwanted complementation* fault at logic-level has been observed for a considerable number of cases of coupling defects for both interconnects and active devices. The bridging mechanisms between QCA wires, either in binary wires (interconnects) or inside logic devices (such as those among the wires of the AOI gate) are quite different from conventional wired-or and wired-and bridging faults in a CMOS design. Hence, appropriate fault models for QCA must be developed and used for test generation.

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