The Nano Revolution and Its Effects on Micro/Nano Systems Education

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This Conference

"Educating Tomorrow's Microsystems Designers"

This Talk

"Educating Tomorrow's ~~Micro~~systems Designers"

Nano

In More Detail

- Silicon Rules Today, But ….
- The "End of the Road" is in sight
- With "Nanotechnologies" in daily headlines
  - Potential for another 1,000X Moore's Law
- And: Our Students will live through the transition

How do we prepare them … Today!

Today's Discussion Topics

- The National Nanotechnology Initiative
- A Walk Through Nano Land
- Lessons Best Not Forgotten
- Moving Towards a New Curriculum
- Concluding Thoughts

Acknowledgements & References

- NSF-Sponsored "Molecular Architecture Workshop (MAW)" @ Notre Dame in Nov. 2001
  - (Names in subtitles = MAW participants)
- "Teaching students computer architecture for new, nanotechnologies," M. Niemier & P. Kogge, ISCA Workshop on Computer Architecture Education, May 26, 2002
- Multiple sponsors: NSF, SRC, JPL, …
- http://nano.gov
- Special thanks to Lynn Conway & Mary Jane Irwin

Nano: Science, Engineering, & Technology

"Ability to work at *molecular* level,

atom by atom,

to *create large structures*

with fundamentally new

properties and *functions*"

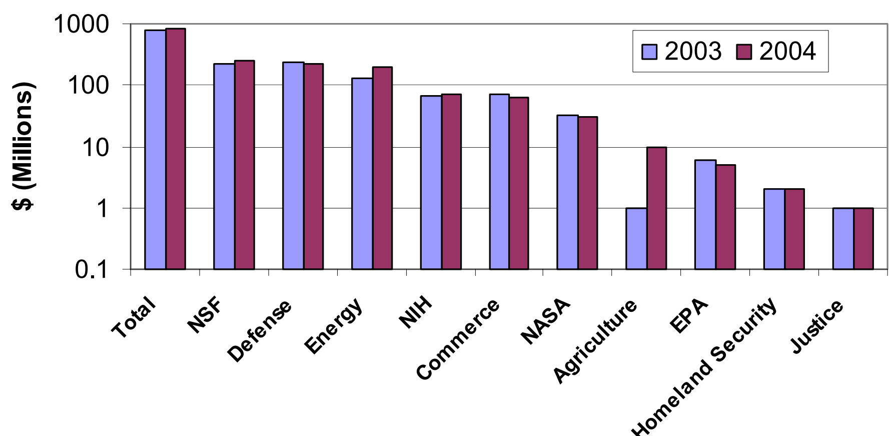
M. Roco, NSF

The National Nanotechnology Initiative (NNI)

NNI: A Brief History

- 1996: Interagency discussions on nano
- 1998: Interagency Working Group on Nanotechnology established
- 1999: "Nanostructure Science & Technology: A World Wide Study"
- 2000: NNI becomes federal initiative
  - 2001 funding authorized @ $464M
- 2001: NSET (Nanoscale Science, Engr, & Technology) subcommittee to provide policy leadership
- May 7, 2003: H.R. 766 authorizes $2.36B over 3 years

The NNI Today



2004: $847M - 9.5% Increase

Where is the $ Going (2002 NSF NIRT)

- Biosystems: 3 @ $5M
- Structures & Phenomena: 18 @ $24
- Theory, Modeling, & Simulation: 2 @ $2.3M
- Manufacturing: 16 @ $17.45M
- Device & *Systems Architecture*: 12 @ $16.6M
  - *Only 3 above the device level (~6%)*

Where is the $ Going (2002 NSF NER)

- Biosystems: 7 @ $585K
- Structures & Phenomena: 21 @ $1.99M
- Theory, Modeling, & Simulation: 6 @ $564K
- Nanoscale in Environment: 6 @ $571K
- Manufacturing: 15 @ $1.39M
- Societal Implications: 2 @ $280K
- Device & *Systems Architecture*: 31 @ $2.69M
  - *only 8 above the device level (~25%)*

Some Key Planned NNI Outcomes

(from "Small Wonders, Endless Frontiers" Nat. Academy Press)

- 2005:
  - 50% of research institutions have nano scale lab access
  - Nano education in 25% of research institutions
  - Catalyse new markets depending on 3D nanostructures
  - 3D modeling for practical system & architecture design
- 2006:
  - Demo terabit nano electronic memory chip
  - Use nano for contaminant monitoring
  - Nanoscale manufacturing for 3 new technologies
  - 10 R&D Centers support facilities for nanoscale testing & manufacturing

Post 2006

- Incorporate biological molecules into electronic devices
- Blueprints for nanomachines & synthetic molecular processors
- Incorporate photovoltaic proteins into nanosystems
- Incorporate "insect hearing organs" into nanosystems

Bottom Line Goal

- **Create new industry**
- **Based on molecular scale devices**
- **That produces "large structures"**
- **With new "functions"**
- ***Within the college career of this year's freshman class***

List of Nano Courses

(from http://www.nsf.gov/home/crssprgm/nano/courses.htm

- **Advanced Quantum Devices, University of Notre Dame**
- **Nano-course, Cornell Nanofabrication Facility**
- **New Technologies, University of Wisconsin, Madison**
- **Nanostructured Materials, Renssellaer Polytechnic Institute**
- **Colloid Chemical Approach to Construction of Nanoparticles and Nanostructured Materials, Clarkson University**
- **Nanoparticles Processes, Yale University**
- **Nanorobotics, South California University**
- **Nanotechnology, Virginia Commonwealth University**
- **Chemistry and Physics of Nanomaterials, University of Washington**
- **Scanning Probes and Nanostructure Characterization, Clemson**
- **Nano-scale Physics, Clemson University**
- **Capstone Course on Nanotechnology, Penn State Nanofab Facility**
- **Nanomanufacturing Processes, U. of Arkansas Oklahoma & Nebraska**
- **Nanoscale Science and Engineering, Purdue University**
- **Visual Quantum Mechanics, Kansas State University**
- **Mathematics in Nanoscale Science and Engineering, UCLA**
- **Nanotechnology: What's So Big About the Science of the Very Small, Rice**

A Walk Through Nano Land
(with a Stop at QCA)

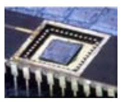
Technology paradigms 101

- **Past 7 decades, Zeus's paradigm, current switches dominate:**

Electromechanical relay

Vacuum tubes

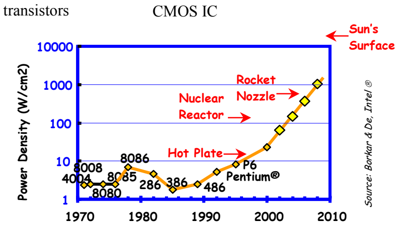
Solid-state transistors



CMOS IC

- **But problems lurk…**

Technical:
Quantum effects, e^- tunneling, power dissipation, slow wires, dopant concentrations, lithography resolutions, chip I/O, testing



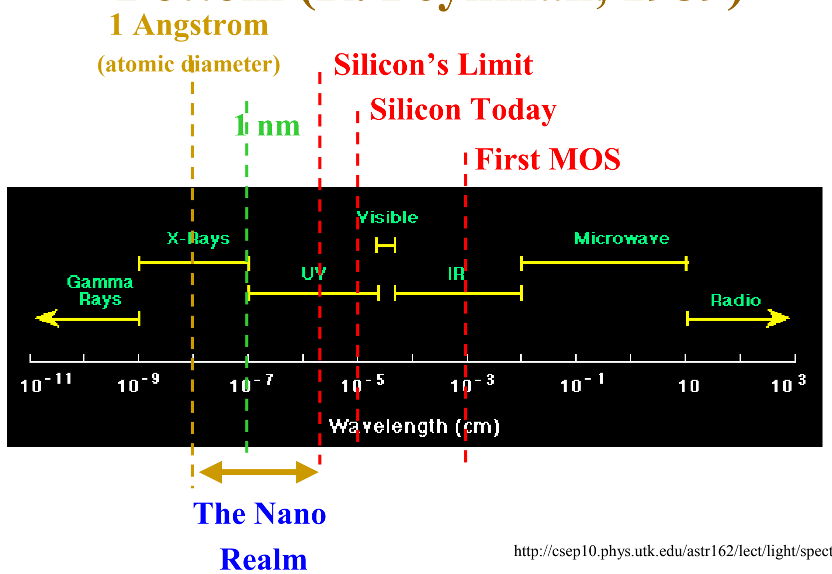
Economical:
In 2010 a fabrication plant may cost $200 billion!

The “Silicon” Limits

- **Silicon 2016:**
  - **22 nm gate lengths,**
  - **28 GHz clocks,**
  - **310 sq.mm die**
- **Roadblocks:**
  - **Smaller devices won’t work**
  - ***Significant changes in key design ratios***

Mse_03.ppt Nano Revolution: MSE – June 1, 2003 Slide 19

There’s Plenty of Room at the Bottom (R. Feynman, 1959)



http://csep10.phys.utk.edu/astr162/lect/light/spectrum.html

Mse_03.ppt Nano Revolution: MSE – June 1, 2003 Slide 20

Computational Paradigms at the Nano Scale

- Classical digital logic
- Neural Net
- Chemical-based
- DNA-based
- Quantum

Working at Nano Dimensions

(Weiss)

- Circuit limits: mean free path & coherence length of electron
  - Ultimate computing device ~ trapping single electron in quantum dot
- Growing capability to manipulate
  - Properties of single molecules
  - Placement into monolayer films
  - With sharp boundaries
- Molecular alignment & conductance states heavily influenced by neighboring molecules
- May provide basis for self-assembly

Design Challenges in Moving to Molecular Realm

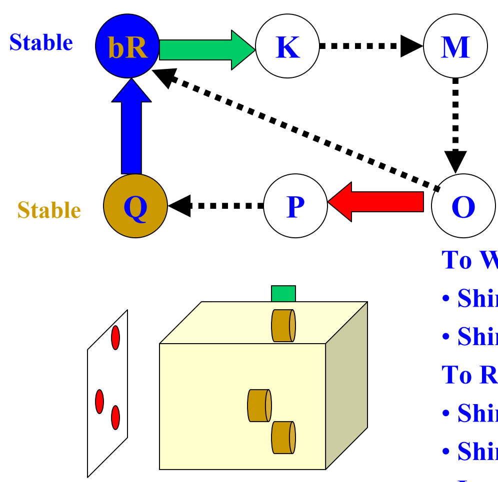
(Edwards, SRC)

What is needed to "commercialize"

- Reliability: what are new failure mechanisms
- "Software Reconfigurability" in the field
- Controlling design time as complexity grows
- Speed: maintaining Moore's Law
- Mixed Signal: needed for "Systems on a Chip"
- Test: coverage, procedures, fixtures
- Cost: development, unit costs, components of cost

Protein Computing

States of the bacteirorhodopsin molecules as a function of light:



To Write:

- Shine green into slice
- Shine red to desired bits

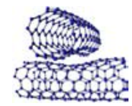
To Read

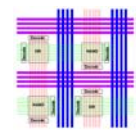
- Shine green into slice
- Shine low red thru all
- Look at red output

Nano Tubes & Nano Wires

(Fuhrer, Goldstein, Dehon)

- Nanotube: nm wide metallic or semiconducting tube
- Producible in numbers in lab
- Applications: interconnect, single electron FETs, micromechanical switches, levers, relays ...
- Most promising structures: arrays, crossbars, FPGAs, fabrics
- "Compile to space, not time"
- Challenges:
  - Alignment
  - Defect recovery/repair, fault tolerance
  - Micro-nano interfacing
  - Gain/signal restoration
  - Customization

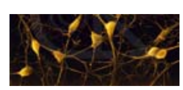


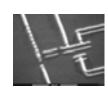


"Network"-Driven Technology Developments

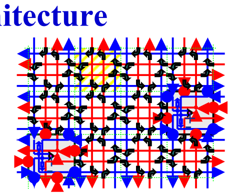
(Likarev, Porod, Chong)

- "Neural Net" as a natural fault-tolerant robust system architecture
- Silicon neural nets too small
  - Brain = 10^{10} cells with 10^{14} synapses

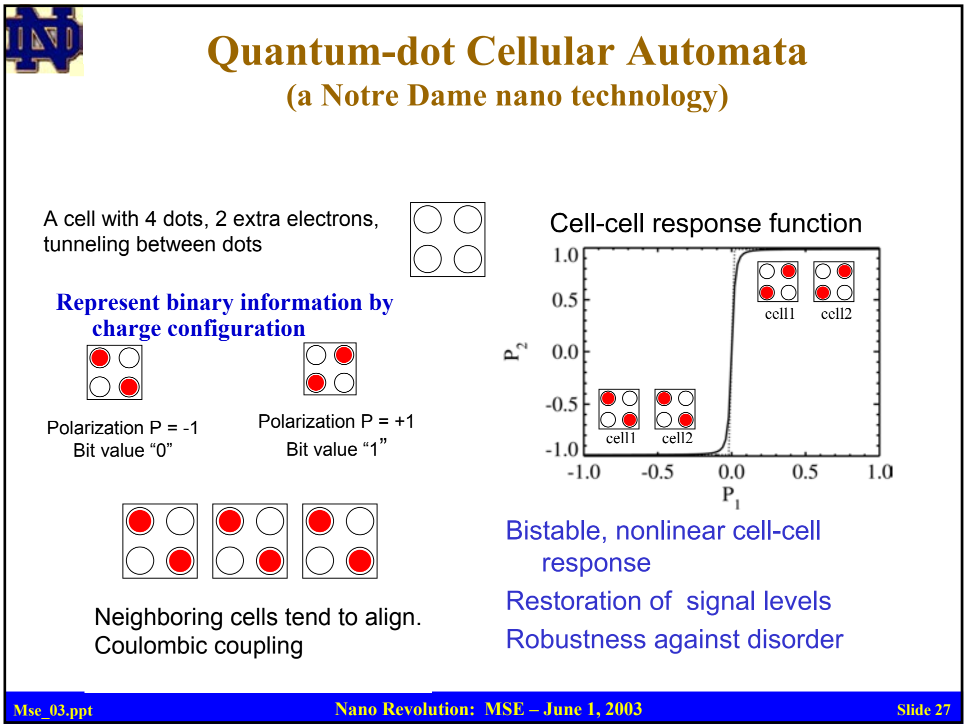




- Enabling nanotechnology: single electron transistors with randomized analog crossbar network architecture
- Growth to system: "Silicon" sandwich of
  - CMOS interconnect logic
  - SET processing elements
  - "Sensors"



- Similar: "sensor nets" merged into "environment"
  - Programming small nodes for aggregate behavior


Quantum-dot Cellular Automata
(a Notre Dame nano technology)
A cell with 4 dots, 2 extra electrons, tunneling between dots
Represent binary information by charge configuration
Polarization P = -1
Bit value "0"
Polarization P = +1
Bit value "1"
Neighboring cells tend to align.
Coulombic coupling
Cell-cell response function
1.0
0.5
0.0
-0.5
-1.0
-1.0
-0.5
0.0
0.5
1.0
P2
P1
cell1
cell2
cell1
cell2
Bistable, nonlinear cell-cell response
Restoration of signal levels
Robustness against disorder
Mse_03.ppt
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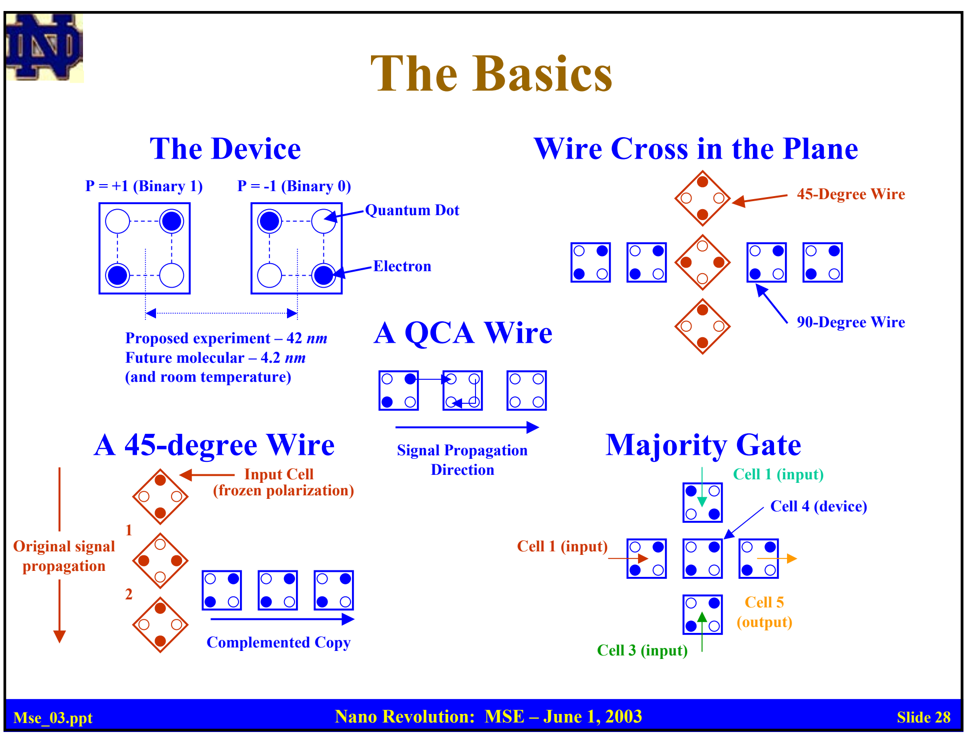
Slide 27


The Basics
The Device
P = +1 (Binary 1)
P = -1 (Binary 0)
Quantum Dot
Electron
Proposed experiment – 42 nm
Future molecular – 4.2 nm
(and room temperature)
Wire Cross in the Plane
45-Degree Wire
90-Degree Wire
A QCA Wire
Signal Propagation Direction
A 45-degree Wire
Input Cell
(frozen polarization)
Original signal propagation
1
2
Complemented Copy
Majority Gate
Cell 1 (input)
Cell 4 (device)
Cell 1 (input)
Cell 5
(output)
Cell 3 (input)
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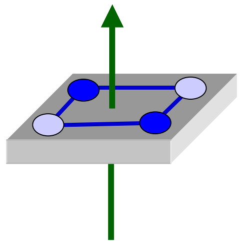
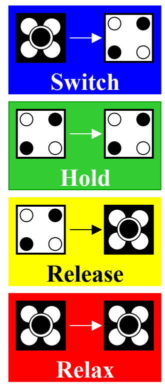
The QCA "Clock"



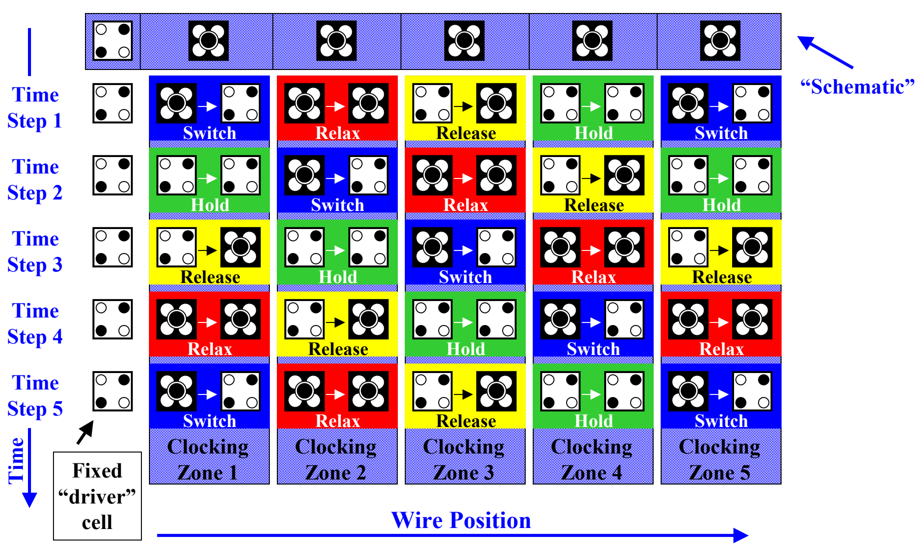
"Clock = E field that controls tunneling between dots



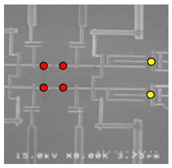
- Cells begin unpolarized
- Barriers raised, cells "latched"
- Barriers are held high
- Used as input to next zone
- Barriers are lowered
- Cells relax to unpolarized state
- Cell barriers remain lowered
- Unpolarized, neutral state stays

The QCA Clock "Phases"

A clocking example



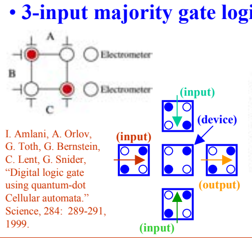
Experimental QCA



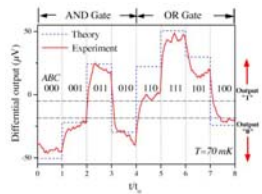
- Early and current work – metal dots
- 70 *mK*
- Metal dot "ideas" transfer to/across different QCA implementations

A. Orlov, I. Amlani, G. Bernstein, C. Lent, G. Snider, "Realization of a functional cell for quantum-dot cellular automata." Science, 277:928-930, 1997.

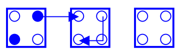
- 3-input majority gate logic demonstrated



I. Amlani, A. Orlov, G. Toth, G. Bernstein, C. Lent, G. Snider, "Digital logic gate using quantum-dot Cellular automata." Science, 284: 289-291, 1999.

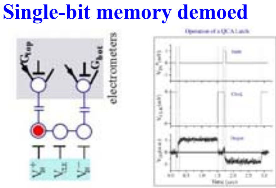


- QCA wire demonstrated



A. Orlov, I. Amlani, C. Lent, G. Bernstein, G. Snider, "Experimental demonstration of a binary wire for quantum-dot cellular automata." Applied Physics Letters, 74: 2875-77, 1999.

- Single-bit memory demoed



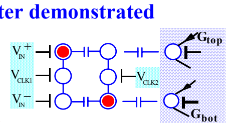
A. Orlov, R. Kummamuru, R. Ramasubramaniam, G. Toth, C. Lent, G. Bernstein, G. Snider, "Experimental demonstration of a latch in Clocked quantum-dot cellular automata: Review and recent Experiments." J. of Appl. Physics, 85: 4283-85, 1999.

- Molecular QCA

C. Lent, "Molecular electronics: Bypassing the transistor paradigm." Science, 288:1597-1599, 2000.

- Shift register demonstrated

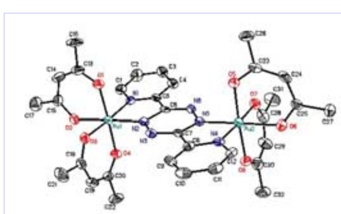
A. Orlov, I. Amlani, R. Kummamuru, R. Ramasubramaniam, G. Toth, C. Lent, G. Bernstein, G. Snider, "Experimental demonstration of clocked single-electron switching in quantum-dot cellular automata." Applied Physics Letters, 77(5): 738-740 2000.

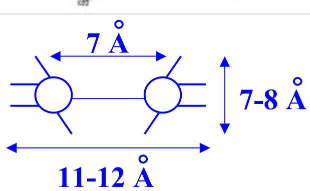


2-Dot QCA Molecules

From ND DARPA Moletronics project

Mixed-valance ruthenium dimers

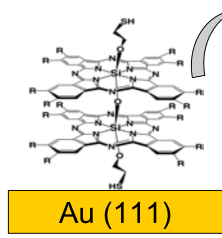


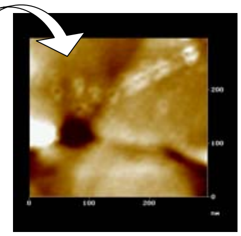


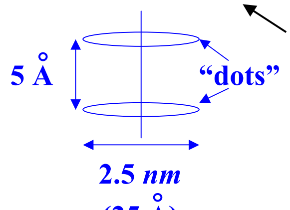
(Center distance of adjacent molecules: ~14 Angstroms)

(M. Lieberman, et al, 2002)

Silicon phthalocyanine dimers





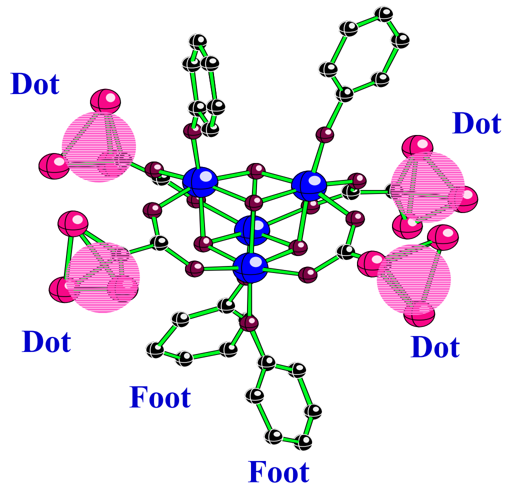


Binds flat on Au surface
Forms self-limiting monolayer
(M. Lieberman)

Appears to self-align
(E. Greenbaum)

These molecules are *real* - in lab now

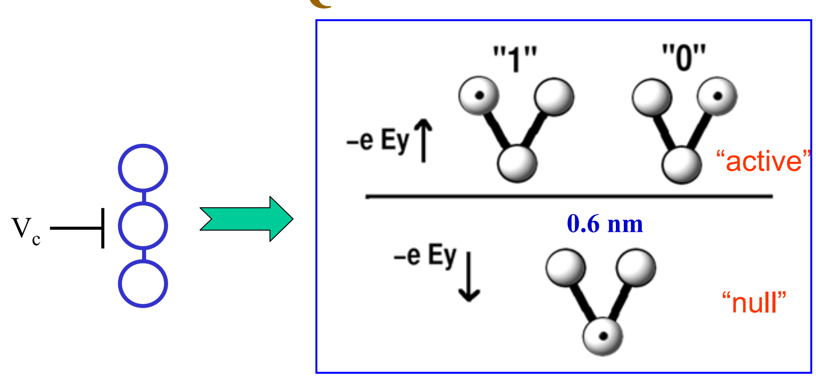
4 dot
Core-cluster molecules



Variants with "feet" for surface binding and orientation

From ND DARPA Moletronics project

New Device Focus: 3 dot
3D QCA molecules

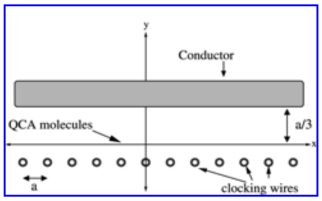


metal dot cell

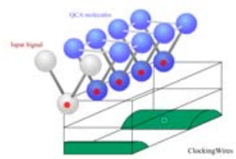
molecular cell

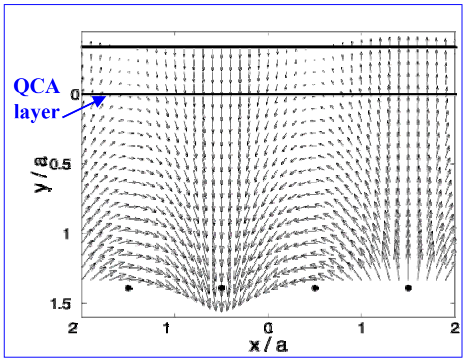
Note: "null state" has some valuable circuit properties
- and may allow for "CMOS" static programming

Mixed Technology Clocking



Hennessey and Lent, JVST (2001)

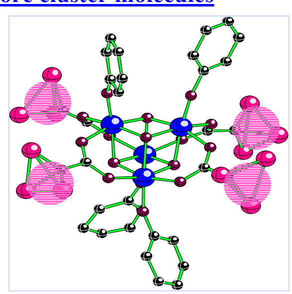




Clocking field is provided by buried Si wires (CMOS controlled).
ITRS 2016 wire pitch: 22 nm ~ 5-10X molecular cell size.

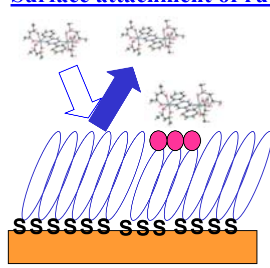
Attachment mechanisms

Core cluster molecules



Variations with "feet" for surface binding and orientation

Surface attachment of ruthenium dimers



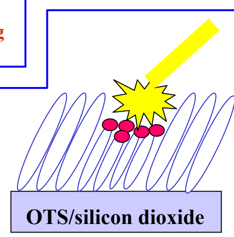
Self-limiting binding to hyrdophilic surfaces

No binding to hydrophobic surfaces

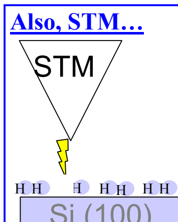
(M. Lieberman, G. Bernstein)

Electron-beam lithography

(OTS: M. Lieberman)
(E-beam: G. Berstein)
(30nm tracks from 5nm primary beam)

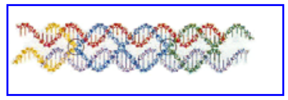
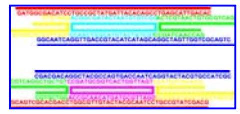


Also, STM…

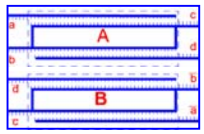


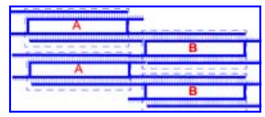
Non-lithographic patterning with DNA tiles

- **Double-crosslinked DNA tiles**
  (Winfree, Lu, Wenzler, and Seeman, *Nature* 394, p. 539 (1998))

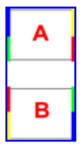



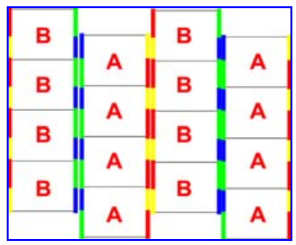
- **Watson-Crick complement**



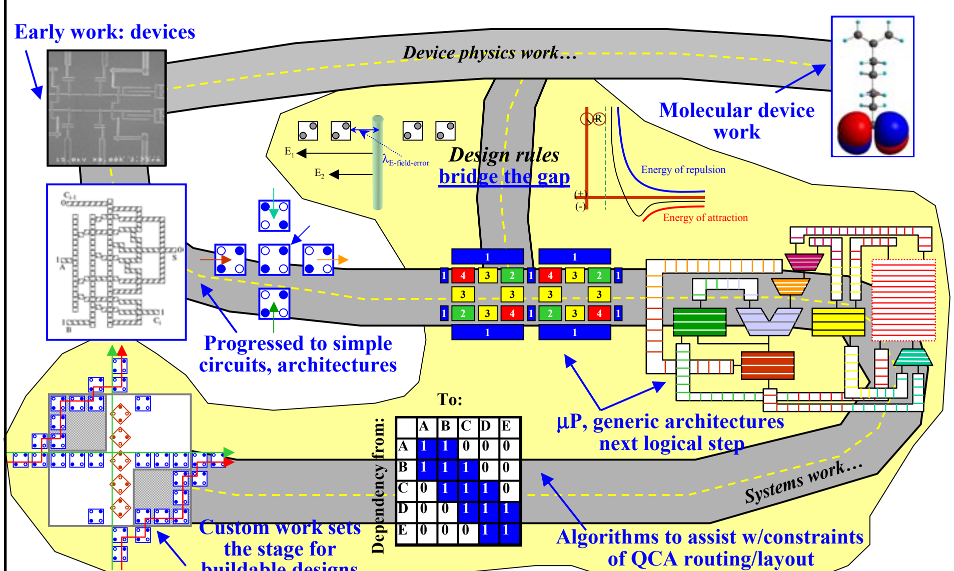


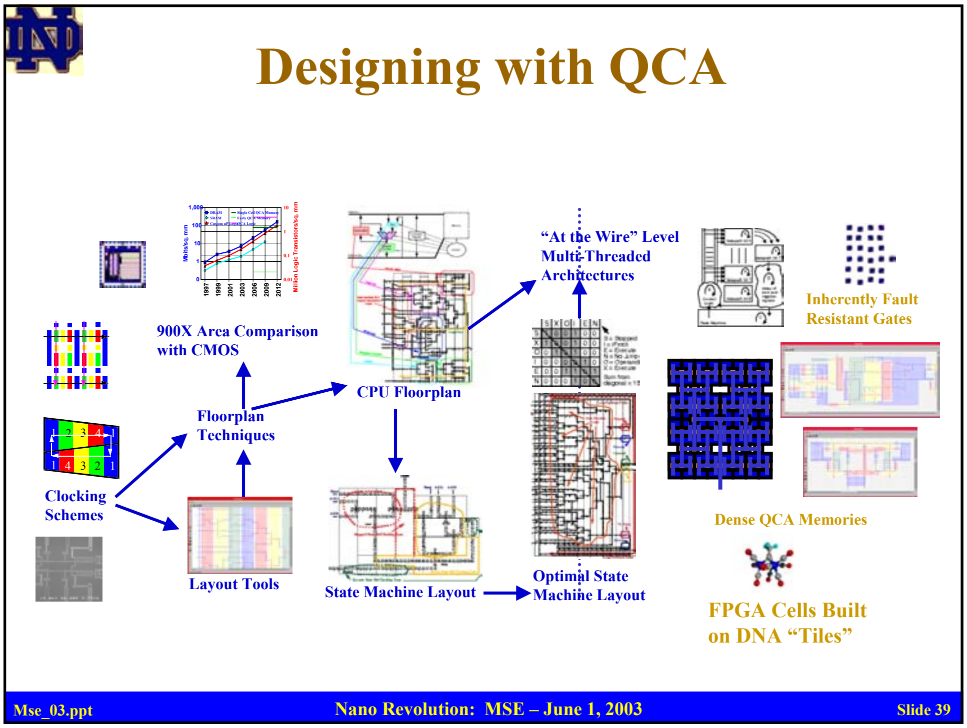
- **Wang tiles**

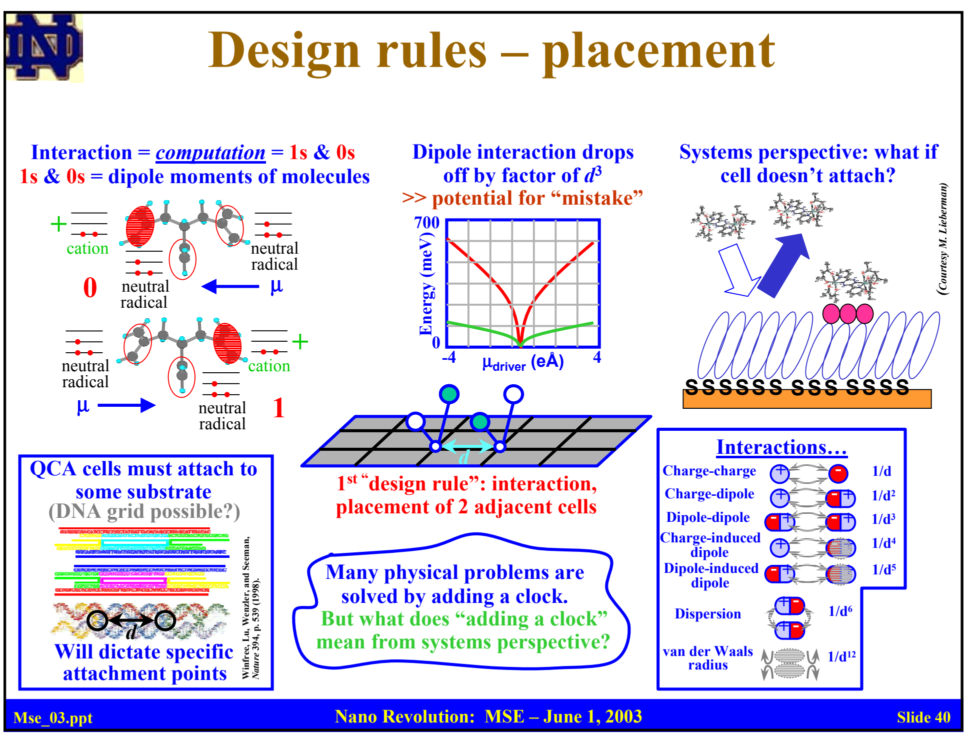




A "QCA Logic Roadmap"




Designing with QCA
900X Area Comparison with CMOS
CPU Floorplan
"At the Wire" Level Multi-Threaded Architectures
Inherently Fault Resistant Gates
Floorplan Techniques
Clocking Schemes
Layout Tools
State Machine Layout
Optimal State Machine Layout
Dense QCA Memories
FPGA Cells Built on DNA "Tiles"
Mse_03.ppt
Nano Revolution: MSE – June 1, 2003
Slide 39


Design rules – placement
Interaction = computation = 1s & 0s
1s & 0s = dipole moments of molecules
cation
neutral radical
neutral radical
0
μ
neutral radical
cation
neutral radical
μ
1
Dipole interaction drops off by factor of d³
>> potential for "mistake"
700
Energy (meV)
0
-4
μdriver (eÅ)
4
Systems perspective: what if cell doesn't attach?
(Courtesy M. Lieberman)
SSSSSS SSS SSSS
QCA cells must attach to some substrate
(DNA grid possible?)
d
Will dictate specific attachment points
Winfree, Liu, Wenzler, and Seeman, Nature 394, p. 539 (1998).
d
1st "design rule": interaction, placement of 2 adjacent cells
Many physical problems are solved by adding a clock.
But what does "adding a clock" mean from systems perspective?
Interactions…
Charge-charge 1/d
Charge-dipole 1/d²
Dipole-dipole 1/d³
Charge-induced dipole 1/d⁴
Dipole-induced dipole 1/d⁵
Dispersion 1/d⁶
van der Waals radius 1/d¹²
Mse_03.ppt
Nano Revolution: MSE – June 1, 2003
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Design rules – functionality

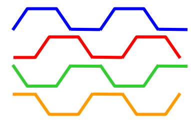
E-field needs certain magnitude to push e^-/h^+ up to active site

Function of molecule, packing distance, etc.

So, what does the clock do for the system designer?

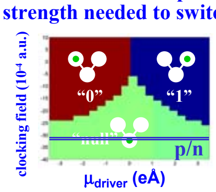
E-field makes cells active or null
Active cells = computation
E-field determines area of computation

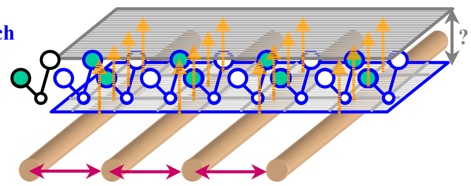
Data moves in phases



π/2 phase shift on wires

Clock – affects dipole strength needed to switch





Clock wire distance ↑ = information density ↓

Functional density still the same

So what about a "clock"?

- Really an E-field
- Makes cells active…
- …or makes cells null
- Can be generated by CMOS wires under attachment substrate

Clock wires have *numbers* associated with them…

Driven by "conventional" lithography

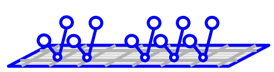
Poly/metal pitch
90 *nm*, 2004
65 *nm*, 2007

Will also determine clock rate…

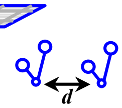
- Only interested in E-field's y-component
- Makes cells active or null
- Driver controls 1s or 0s
- Add a conductor
- Where do we place conductor?

Fault Modeling

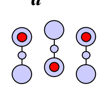
- **Background charge**
  - **Possible substrates:**
    - SiO_2, organic monolayer on top of SiO_2 DNA tiles
  - **All subject to stray charge…**
    - Stray charge can excite a cell out of ground state (source of error)
- **Defects**
  - **Error in placing cells**
    - Cells simply may not attach



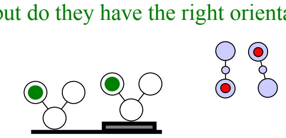
  - **Distance between cells**
    - At what distance will 1 cell not influence another?



  - **Alignment/Rotation**
    - Cells must "line up to talk" (easier with square cells)



  - **Orientation**
    - Cells may "line up" in a straight line, but do they have the right orientation to talk?
  - **Rough attachment surfaces**
    - cells may not line up in the y-plane



(Conversations with Marya Lieberman)

Summary Comparisons

Base Technology	Silicon	Nano
Component Count	Billions	Uncountable
Fabrication	In layers	Self-Assembly
Memory vs Logic	In same technology	Very technology dependent
Clocking	In same technology	Very technology dependent
Power Distribution	In same technology	Very technology dependent
I/O	In same technology	Very technology dependent
Fault Models	Small	Very visible

Lessons Best Not Forgotten

Or:
We've Been Down This Road Before!

Some Key Insights from MAW

- What made the initial technology viable
- What allowed follow-on technologies to
  - Not only survive development
  - But be deployable so quickly
- The MAW Workshop Experts:
  - Conway (Michigan): "The Revolution"
  - Abraham (Texas): "Testing & Verification"
  - Irwin (Penn State): "Why the Roadblock"

Conway on Architects

- Don't care about physics, only rules for composition
- Look at designs in layers (hierarchies)
- Successful ones work with others: circuit designers, CAD, packaging, layout, fab…
- Tend to translate new technologies into different forms of old (abstraction)

Conway on Technology circa 1977: RTL

- **Design flow:**

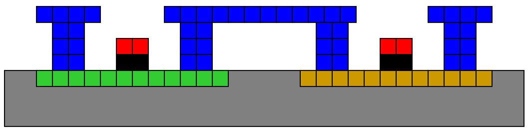
  system arch => logic designers => fab
  - **With very little interaction**
- **Devices looked at <u>in cross section</u>, NOT overhead *("Just like Today!!")***
- **"You just wire'em up"**
- **MOSFET: "slow & sloppy"**

The Mead/Conway Revolution

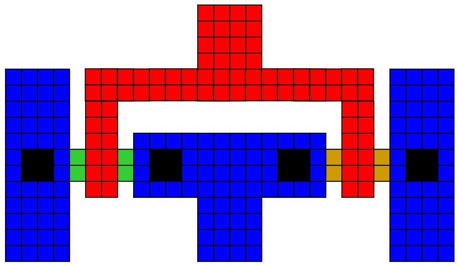
- **Self-aligned gate enables simplified fab**
- **Realization that scaling to 0.25u was feasible**
- **Energized academic design community**
  - ***Scaling rules for technology independent design***
  - ***<u>Some</u> simple but useful circuit primitives***
  - ***A focus on interconnect, not cross section***
- **Early work considered toy-like, unoptimizable**
  - ***UNTIL MOSIS enabled inexpensive, adventuresome prototyping***

The Mead/Conway Revolution: A Change in Perspective

From This



To This

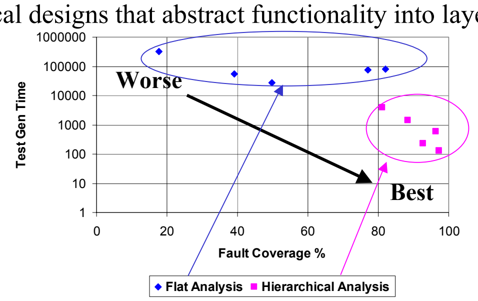


The Power of Hierarchies & Abstraction

(abstracted from J. Abraham)

Observations:
- 200 bits covers more states than there are protons in universe
- Many key design questions NP-complete: Critical paths, verification, fault coverage, ...

Lesson Learned from CMOS CAD
- Direct attack on "flat designs" rapidly becomes impossible
- Hierarchical designs that abstract functionality into layers are manageable



What Are *We Now* Good At?

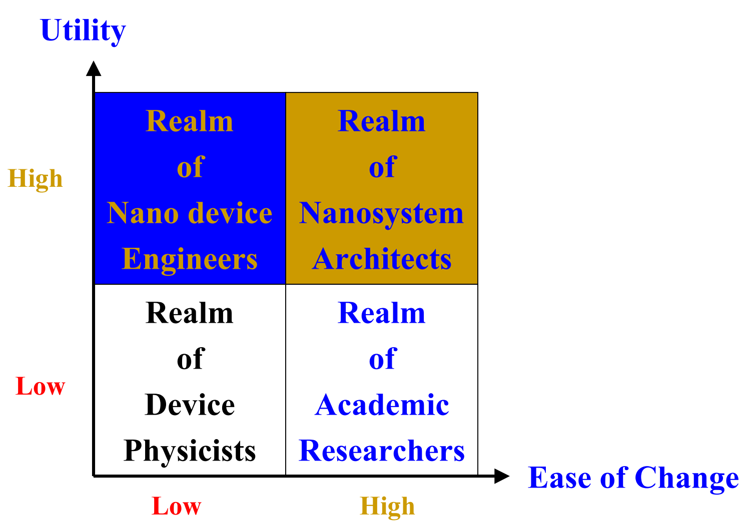
- The Digital Paradigm: a time-tested model
  - State machines, data path, memory, busses, ...
- "Abstracting Out" the physics
- Focus on Interconnect, not devices
- Hierarchical design from day one
- Portable design styles
- Working with device & circuit designers to
  - Invent new structures
  - That permit more efficient designs
- Automating routine design activities
- Fabricating real chips on student schedules

A Transitional Curriculum

Our Objectives

- Train the next generation
- To design systems
- With billions (“and billions”) of components
- That interface with the real world
- That work
- When we may not understand the technology today

Where Should We Focus



Considerations

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Our Ideal Students: The "Dream Nano Team"

- Device physicists:
  - Simplified technology description teachable quickly to "anyone"
  - Description of "Key Parameters" that affect circuit level performance
  - Simple basic circuits
- Architects:
  - Develop abstractions for hierarchical designs
- CAD Engineers:
  - Leverage existing hierarchical design systems where possible
- Physical Designers:
  - Simple interfaces to conventional technology & environment

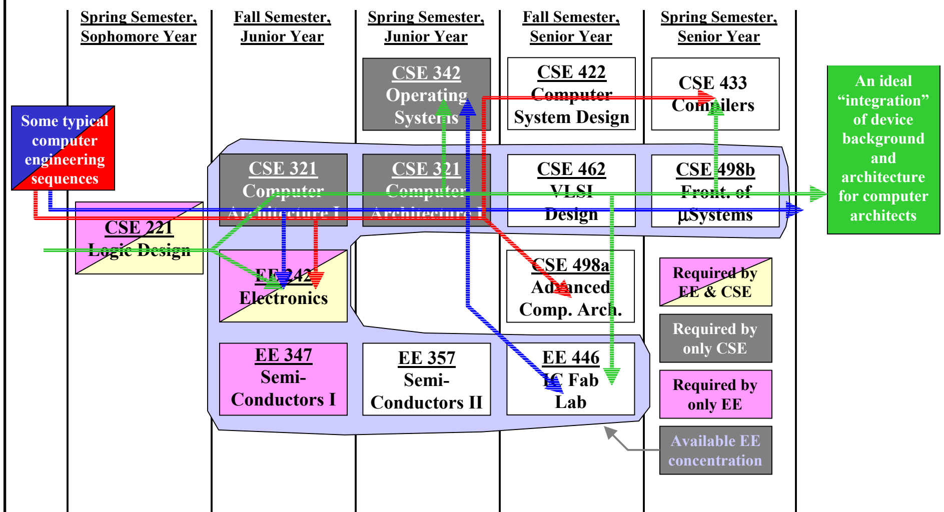
What to Keep from Current Curriculum

- "Logic" as a paradigm
- Abstraction
- Design Rules
- Hierarchies
- Layout orientation
- Timing
- Relationship between microarchitecture, architecture (ISA), languages, support tools

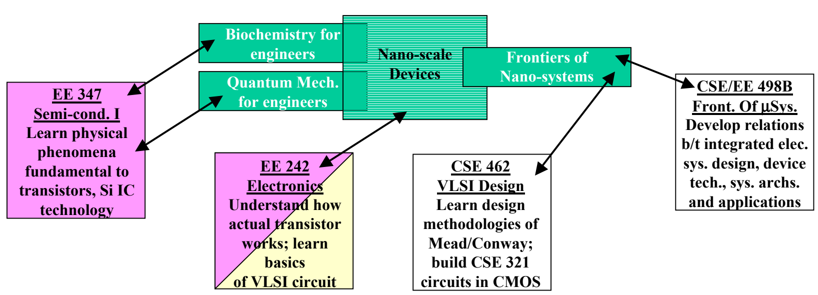
What to Add

- Enough physics to justify new, generic "device types"
- More emphasis on fault models
- Fault redundancy techniques
- Mixed technology interfacing
- Self-assembly
- New computational paradigms

"You're friendly, neighborhood school for computer architects"

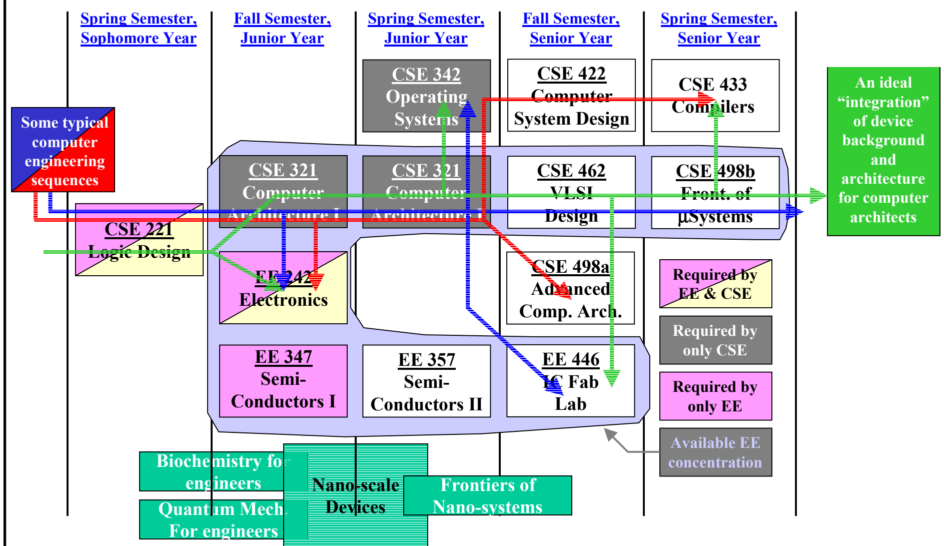


What's new?



- Biochemistry/QM for engineers vs Semi-conductors:
  - All teach about materials computational devices built from
- Nano-scale devices vs Electronics:
  - Both teach about how computational devices actually function
- Frontiers of nano-systems vs VLSI/Frontiers of µSystems
  - Currently nano-"capstone" course = combination of MOS capstone course – goal is to help students *evolve*

“You’re friendly, neighborhood school for nano-architects”



The Technology Package

- Engineering-oriented ground rules
  - Projectable into future technology generations
- Can be taught quickly
- Simple models of speed, power, area
- Permit hierarchical design
  - Primitive composition rules
  - Reasonable I/O
  - Leverage test & validation technologies
- Basic tool sets readily available
- Matched with “readily accessible prototyping service”

A Desirable Nano Prototyping Facility

- "Open" to wide group of potential users
- Permit Spectrum of Activities
  - Student design exercises
  - New circuit experiments
  - New architectural prototypes
- Rapidly reach "Proof of Concept" stage

Concluding Thoughts

Conclusions

- Our students *will* see nano .. and soon
- We *can* introduce "nano" at the device level today
- We *must* do so in a design friendly way
- We also need to *plan for* new topics:
  - Self assembly, fault tolerance
- Working with the device physicists *will help*
- As will availability of nano lab facilities

Needed Insight

- Understanding & modeling of molecular interactions
  - And abstraction into simple "engineering" models
- What is resulting "electronic nanotechnology"
- "Killer Apps"/new computing models
- Construction of hierarchy of abstractions
  - With "interface" to conventional environments
  - Most reasonable starting point: FPGA-like arrays
- How to provide reliability from the beginning

A Followup Activity

- "Nano Training Bootcamp"
  - Basic theory
  - Nano device structure
  - Fabrication techniques
  - Characterization
- Institute for Nanotechnology, Northwestern
- July 8-11, Evanston Il
- www.asme.org/nano/bootcamp