# Power gain in a quantum-dot cellular automata latch

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We present an experimental demonstration of power gain in quantum-dot cellular automata (QCA) devices. Power gain is necessary in all practical electronic circuits where power dissipation leads to decay of logic levels. In QCA devices, charge configurations in quantum dots are used to encode and process binary information. The energy required to restore logic levels in QCA devices is drawn from the clock signal. We measure the energy flow through a clocked QCA latch and show that power gain is achieved. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1499511]

In all practical electronic circuits, dissipation of signal power occurs through irreversible loss processes. For an electronic architecture to be viable, it must have a mechanism for restoring signal power. In conventional electronic devices, power lines and transistors are used to achieve power gain and logic level restoration. While there are conventional logic schemes, such as those based on pass transistors, that do not provide power gain, signal degradation occurs along the circuit path and gain stages are required to ensure signal integrity. In the area of molecular electronics, power gain is particularly important since most proposed molecular devices lack power gain[1] and will require the introduction of gain stages.

Quantum-dot cellular automata (QCA)[2,3] is a device architecture that uses changes in quantum dot arrays and can provide power gain and miniaturize digital logic circuits to the molecular level, well beyond what can be achieved using field effect transistors. In recent years, several QCA devices such as a QCA cell,[4] majority gate,[5] leadless cell,[6] and a latch,[7] have been fabricated and tested. In this letter, we discuss how power gain is achieved in QCA devices, using the cell's clock to restore lost signal power,[8] and experimentally demonstrate power gain using a QCA latch.

Figure 1(a) shows the scanning electron micrograph of a QCA latch fabricated using aluminum/aluminum oxide tunnel junction technology.[9] $D_1$, $D_2$, and $D_3$ are the aluminum islands (also called dots) that form the latch and $E_1$, $E_2$, and $E_3$ are the electrometers used to measure the potentials on the dots. Figure 1(b) shows a schematic diagram of the device. The size of our tunnel junctions limits the temperature of operation of the device to below 200 mK. The experiment is performed in a dilution refrigerator at a base temperature of 15 mK, in an ambient magnetic field of 1 T to suppress the superconductivity of aluminum.

The QCA latch is a short-term memory element capable of storing a single bit for one clock cycle. Switching in a QCA latch was discussed in Ref. 3, developed for metal-based QCA systems in Refs. 10 and 11, and experimentally demonstrated in Ref. 7. In the QCA latch, a bit is encoded by the presence of an electron in the top or bottom dot and is detected by measuring potentials on these dots. An electron occupying the top dot would induce a negative potential on the dot and is considered a polarization of ''−1'' and a bit value of ''0'' and vice versa.

It is helpful to have a nomenclature that classifies the behavior of the latch according to the clock voltage. Switching is accomplished by moving an electron between the top and bottom dots, by adjusting the effective barrier between them. In metal-based QCA devices, this adjustable barrier is formed by the middle dot, whose potential is controlled by an applied clock signal. When the effective switching barrier is low (clock voltage $V_c \geqslant 0$), the latch is in the ''null'' state and holds no information. As the barrier height is increased, ($V_c$ becomes negative) the latch becomes ''active'' and the polarization takes on a definite value determined by the inputs applied to the top and bottom dots. When the barrier height is large enough to suppress switching over the relevant time scale, we say the latch is in the ''locked'' state. In the locked state, the latch polarization is independent of the neighboring latches and it becomes a single-bit memory element. Three junctions are used between each pair of dots [Fig. 1(b)] in order to reduce cotunneling, and enhance retention time of the latch.[7]

A shift register[10,11] consists of a line of latches where each latch, in its locked state, acts as an input to the next.

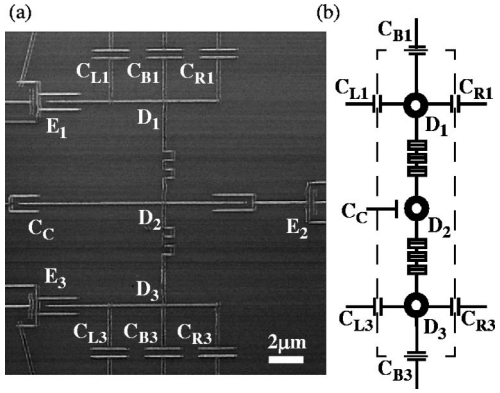


FIG. 1. (a) Scanning electron microscopy micrograph of the latch. (b) Schematic diagram of the QCA latch.

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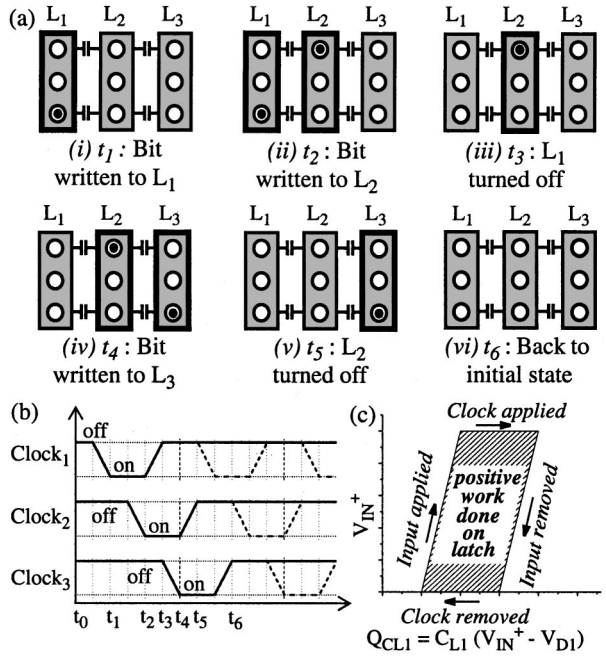


FIG. 2. (a) The sequence of events describing the operation of a QCA shift register. For this experiment, latches $L_1$ and $L_3$ are simulated using voltages applied to capacitors. (b) Clock sequence applied to the shift register. The solid line shows a single bit being transferred from $L_1$ to $L_3$ while the dotted line shows multiple periods of the clock signals. (c) Example of a $Q-V$ plot where, $Q_{CL1}$ is the charge on the capacitor $C_{L1}$ and $V_{\mathrm{IN}}^+$ is the input voltage applied to the capacitor. The shaded region gives the work done by the input on the latch. A clockwise path indicates positive work done.

Binary information is transferred along the line by applying a sequence of phase-shifted clock signals to successive latches Fig. 2(a) and 2(b). At time $t_0$, all the clock signals are off and all latches are in the null state. The first cell ($L_1$) latches to its input when its clock signal (clock$_1$) is applied at $t_1$. While latch $L_1$ switches, the downstream latch ($L_2$) is kept in the null state, so that it does not contribute any ''backinfluence.'' Then (at $t_2$) the second clock signal (clock$_2$) is applied to $L_2$. This copies the information from the first latch to the second. Again, the downstream latch (now $L_3$) is kept in the null state. Then (at $t_3$) the input latch $L_1$ is switched off and the information remains stored in $L_2$. At $\pm_4$ the clock signal (clock$_3$) is applied to and the information is copied into latch $L_3$. This process is continued and binary information is transferred down the line. Each latch is an inverter, and so, the bit is inverted at every step as it moves along the shift register.

To demonstrate power gain in a QCA device, we focus on the energy flow through a single latch in a QCA shift register. There are four paths for energy transfer in a QCA latch: the input signal, the output signal, the clock signal, and irreversible power dissipation. The work done on the latch by its neighboring latches or vice versa constitutes energy flow due to the input and output signals. While the input and output signals are determined by the latches in the shift register, the clock is an external signal that can be used as an energy source or sink for the latch. To evaluate the change in the signal power as it passes through a latch, we measure the energy of the input and output signals averaged over one clock cycle.

Work done on a latch over a given time interval, by a particular lead voltage is

$$W = \int V\, dQ = \int_0^{t'} V_L(t) \frac{dQ_c(t)}{dt} dt,$$

where $V_L(t)$ is the voltage applied to the lead and $Q_C(t)$ is charge on the capacitor coupling the dot to the voltage lead. For an input $V_{\mathrm{IN}+}$, applied to the latch through capacitor $C_{L1}$ [Fig. 1(b)] this equation becomes

$$W_{\mathrm{IN}+} = \int_0^{t'} V_{\mathrm{IN}+}(t) \frac{d\{C_{L1}[V_{\mathrm{IN}+}(t) - V_{D1}(t)]\}}{dt} dt,$$

where $V_{D1}(t)$ is the potential on dot $D_1$. When the lead voltage is plotted in relation to the charge on the capacitor for a periodic experiment, the $Q-V$ plot has a closed path, and the area enclosed by the plot gives the work done on the cell [Fig. 2(c)].

Power gain is the ratio of output to input signal power

$$\text{Power gain} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{W_{\mathrm{out}}/T}{W_{\mathrm{in}}/T}.$$

To calculate this, we measure the work done on the latch by its predecessor ($W_{\mathrm{in}}$) and the work done by the latch on its successor ($W_{\mathrm{out}}$), in one clock cycle. For the experiment, the system must be returned to its initial state at the end of the clock cycle. This requirement excludes the contribution of constant bias voltages to power gain calculations, and eliminates the possibility of a latch achieving gain using energy stored temporarily in it.

In a QCA shift register gain greater than unity occurs when the input signal seen by one of the latches is weak. A small input is sufficient to decide the direction of switching, and when a weak input occurs, the clock provides the energy required to switch the latch and restore logic levels. To demonstrate power gain we simulate a weak input latch. The experiment is performed with a single latch ($L_2$) by simulating the presence of a latch on either side of it, ($L_1$ and $L_3$). Voltages $V_{L1}^+$, $V_{L1}^-$, $V_{L3}^+$ and $V_{L3}^-$ ($V_{L1}$ and $V_{L3}$ in short) are applied to identical capacitors $C_{L1}$, $C_{L3}$, $C_{R1}$, and $C_{R3}$ [Fig. 1(b)], respectively, to simulate latches $L_1$ and $L_3$. The capacitor $C_C$ is used as the clock gate while $C_{B1}$ and $C_{B3}$ along with $C_C$ are used to bias the latch.

Figure 3 shows the sequence of input and clock voltages applied to the latch $L_2$ in one clock cycle and the measured dot potentials on $D_1$ and $D_3$. Measurements on $L_2$ show that a normal latch produces a dot potential swing of 100 $\mu$V. A signal of 100 $\mu$V is used to simulate a normal latch $L_3$ while a smaller signal (50 $\mu$V) is used to simulate a weak latch $L_1$. The times $t_0-t_6$ correspond to those in the schematic diagrams in Fig. 2(a). Initially, the input and clock signals are off and the latch is in the null state. When the clock is applied, $L_2$ switches, and then stays locked irrespective of the inputs. When the clock signal is removed, $L_2$ returns to the null state and the dot potential returns to zero.

The work done by each input voltage ($V$) is calculated by first calculating the charge ($Q$) stored on each of the input capacitors, and then measuring the area enclosed by the $Q-V$ plot. Figure 4 shows the $Q-V$ plots for the signals $V_{L1}$ and $V_{L3}$. The sequence of events defines the direction of the $Q-V$ loops. Between $t_0$ and $t_1$, the input from the left ($V_{L1}$)

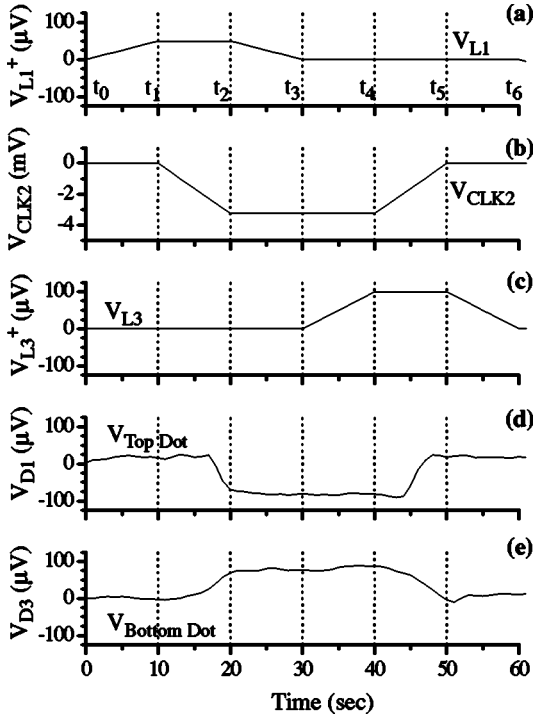


FIG. 3. Input and clock signals applied to the device ($L_2$), and the measured potentials on dots $D_1$ and $D_3$. $V_{L1}^+$ and $V_{L3}^+$ are applied to dot $D_1$ while $V_{L1}^-$ $(=-V_{L1}^+)$ and $V_{L3}^-$ $(=-V_{L3}^+)$ is applied to dot $D_3$. (a) Weak input signal from latch 1. (b) Clock signal applied to the device ($L_2$). (c) Simulated signal from latch $L_3$ (same magnitude as the dot potential swing in $L_2$). (d) Experimentally measured potential on dot $D_1$. (e) Experimentally measured potential on dot $D_3$.

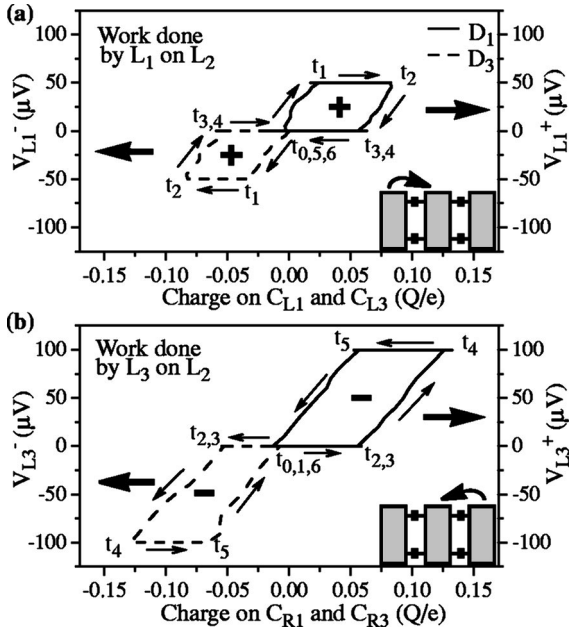


FIG. 4. $Q-V$ plot of the data shown in Fig. 3. Work done by a given input $V$ (connected to $L_2$ by capacitor $C$ with charge $Q$) is the area enclosed by the path (shown by the arrows) in the $Q-V$ plot. (a) A clockwise path signifies positive work done on $L_2$ and (b) an anticlockwise path signifies negative work done on $L_2$, i.e., positive work done by $L_2$. Work done by $L_2$ on $L_3$ is approximately twice the work done by $L_1$ on $L_2$. $P_{out}/P_{in}=2.07$.

is increased from 0 to 50 $\mu$V, but no switching occurs, and so while $Q_L$ (charge on $C_L$) changes by only a small amount. From $t_1$ to $t_2$, the clock is applied and $L_2$ switches, so $Q_L$ and $Q_R$ (charge on $C_R$) change while $V_{L1}$ and $V_{L3}$ remain unchanged. From $t_2$ to $t_3$, $V_{L1}$ is removed, but $L_2$ retains its state. From $t_3$ to $t_4$, $V_{L3}$ is applied. From $t_4$ to $t_5$, the clock is removed and $L_2$ turns off. Finally, from $t_5$ to $t_6$, $V_{L3}$ is removed and the system returns to its initial state. The $Q-V$ plot for $V_{L1}$ [Fig. 4(a)] shows a clockwise direction indicating that $L_1$ performs work on $L_2$. However, the $Q-V$ plot for $V_{L3}$ [Fig. 4(b)] shows a counter-clockwise direction indicating that $L_2$ performs work on $L_3$. Hence, work is being performed in the same direction as the transfer of the bit. The ratio of the area enclosed by the plot in Fig. 4(b) to the area enclosed by the plot in Fig. 4(a) gives the power gain. This ratio calculated from Fig. 4 is 2.07.

The area of a parallelogram is given by the product of its height and width. In the $QV$ plot, the height is given by the input signal, while the width is given by the charge induced on the input capacitor due to switching of a single electron in latch $L_2$. Irrespective of the input signal, the charge transferred is only a single electron and so the work done is proportional to the input rather than to the square of the input. Since all capacitors are identical, widths of the parallelograms in Figs. 4(a) and 4(b) are equal, and so the expected power gain is the ratio of $V_{L3}$ and $V_{L1}$, i.e., 2, which agrees closely with experiment.

The voltage transfer function of a QCA cell is nonlinear, giving enough gain to restore the system to a saturated logic level. Though a weak input results in a large power gain, from a practical standpoint an infinitesimally small input would not result in an infinite gain, since the input would be lost in noise, leading to errors. Therefore, error sources impose a lower limit on the size of the input signal. Because power gain is possible, very small input signals (large enough to eliminate errors) are sufficient to decide the direction of switching in the device. Therefore, with the help of the clock, logic levels are automatically and weak signals do not lead to a loss of information.

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