Defect Characterization and Yield Analysis of Array-Based Nanoarchitecture

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Abstract— **With molecular-scale materials and fabrication techniques recently developed, high-density computing systems in nanometer domain emerge. An array-based nanoarchitecture has been recently proposed based on nanowires such as carbon nanotubes (CNTs), silicon nanowires (SiNWs). High-density nanoarray-based systems consisting of nanometer-scale elements are likely to have many imperfections; thus, defect-tolerance is considered as one of the most significant challenges. In this paper, we propose a probabilistic yield model for the array-based nanoarchitecture. The proposed yield model can be used 1) to accurately estimate the raw and net array densities, and 2) to design and optimize more defect and fault-tolerant systems based on the array-based nanoarchitecture.**

I. INTRODUCTION

The end of photolithography as the driver for Moore's Law is predicted within seven to twelve years [1]. Although this might be seen as an ominous development, nanotechnologies are emerging that are expected to continue the technological revolution [2]. One of the most promising nanotechnologies is the crossbar-based architecture, a two-dimensional array (nanoarray) formed by the intersection of two orthogonal sets of parallel and uniformly-spaced nanometer-sized wires [3], [7], such as carbon nanotubes (CNTs) and silicon nanowires (SNWs). Experiments have shown that such wires can be aligned to construct an array with nanometer-scale spacing using a form of directed self-assembly.

Recently, DeHon has proposed a promising array-based nanoarchitecture based on nanowire crossbars, nanoscale address decoders and microscale global interconnects. In the proposed architecture, nanowires are organized to form crossbars, in which crosspoints can be used as FETs or memory cells. Those crossbars of nanowires can form both NOR logic planes or OR logic planes [3]. Based on that, any other logic can be realized.

Although we can directly apply a voltage to the CNTs/SiNWs in the array so that we can change the state or logic of the crosspoint, this will result in a as lower array density as the density of microscale wire architecture. So "2-hot" address decoder with imprinted

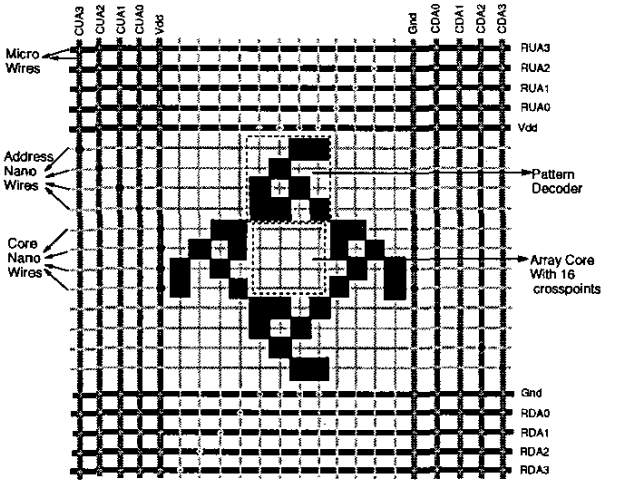

Fig. 1. A 4×4 nano-array with imprinted pattern decoder

pattern during fabrication is used to address the nanoarray [3]. In [4], one of the state-of-the-art nanoscale address decoding technique called "h-hot addressing" is reported. Unlike the conventional binary address decoding scheme, in which N_a address wires address 2^{N_a} address locations, only two "hot" (i.e., activated) address wires are required to access an address location; in other words, $\binom{N_a}{2}$ address locations can be accessed by N_a address lines, if $h = 2$.

N_a could be as small as $O(logN)$ wires (N is the number of addressable nanowires), if we use the binary address decoding scheme; however, if we use such a dense encoding, a single fault in the address wires could render half of the array inaccessible. Instead, 2-hot addressing needs $N_a = O(\sqrt{N})$ and guarantees that we only lose $O(\sqrt{N})$ wires on any address fault.

In the decoder pattern, where the pattern leaves blank, the two orthogonal CNTs are contacted to produce a strongly coupled FET; where the pattern leaves black, the two crossed wires are kept far enough to prevent coupling

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each other. By using this kind of address decoder, we can access each intersection in the nanoarray.

Nanoarrays offer both an opportunity and a challenge. The opportunity is to achieve ultra-high density which has never been achieved by photolithography. The challenge is to make them *defect-tolerant*, since high-density systems consisting of nanometer-scale elements are likely to have many imperfections. In order to effectively introduce and evaluate different defect-tolerance techniques for the array-based nanoarchitecture, a realistic yield model should be developed.

In [3], DeHon also proposed a simple yield model for the proposed array-based nanoarchitecture. In this paper, we will further improve and extend DeHon's basic model by: 1) Introducing more defect factors to make the model more practical, 2) Using a more general h – *hotaddressing* technique to make the model more flexible, and 3) Modifying the model to be more accurate so that the number of core nanowires N can be continuous value instead of some discrete value.

By using the proposed extended yield model, we can accurately estimate both raw and net array densities. Also, different defect tolerance techniques for the proposed architecture can be compared so that quantitative design and optimization can be done based on that.

II. Yield Modeling

Let us consider a single array core with N nano wires and N_a micro address lines and using the *h-hot addressing scheme*. In order to get the yield for the single element array, we need to identify how many different factors many impact the yield, first. The following factors are considered in this paper: 1) *Nanowire crosspoint fails:* In the array, the crosspoint of two nanowire/nanotube can work as a FET [3] and the connection has a probability P_{nj} that the physical character of the junction is sufficiently poor as to be defective, 2) *Contact between nanowire and microwire fails:* The microwires are used to address the crosspoint in the nanoarray and provide power supply. So the contact also has a probability P_{mj} to be defective, 3) *Decoder pattern fails:* In the nanoarray, a decoder pattern that is customized during directed self-assembly is used to program the array (see Figure 1). The black blocks are used to keep two crossing nanowires far away enough to interfere each other. For those black blocks, P_{bp} is the probability to be defective, and 4) *Length/Break fails:* With probability P_l, there is an open or short in a nanowire.

First, we need to calculate the yield of a single addressable nanowire. In a single decoder row or column, there are total $h \cdot N$ blank blocks(FETs). So for each addressable nanowire there are $Q_1 = (h \cdot N)/N_a$ FETs in the decoder sections. As well as there are $N_a \cdot N - h \cdot N$ black blocks in the decoder and for each address wire, there are $Q_2 = (N_a \cdot N - h \cdot N)/N_a$ black blocks.

Also we need to calculate the length of each address nanowire. The width taken by each nanowire is W_{nano} and the width taken by each microwire is W_{micro}, including pitch. Considering we also have power supply provided by microwires, so the length of each nanowire/nanotube is:

$$L = 4 \cdot N_a \cdot W_{micro} + (2 \cdot N_a + N) \cdot W_{nano} \quad (1)$$

Considering the current manufacturing process, we assume that the $W_{micro} = 20 \cdot W_{nano}$. In the following discussion, we use nanowire width as unit length of 1 and scale down the W_{micro} by the nanowire width.

From the architecture, we can see there is only one junction to microwire in each address line. So for a single address nanowire to yield:

$$\begin{aligned} P_{half-add} &= (1 - P_{mj}) \cdot (1 - P_l)^L \\ &\quad \cdot (1 - P_{nj})^{Q_1} \cdot (1 - P_{bp})^{Q_2} \end{aligned} \quad (2)$$

If we further look at the array architecture, we need to account the upper and lower decoders to address a nanowire in the array core. This means we must have a pair of functional address nanowires to correctly address one core nanowire. So the yield should be modified to: $P_{add} = P_{half-add}^2$.

Second, we need to calculate the yield for a single nanowire in the array core. For each core nanowire, there are $2h + N$ blank blocks (FETs) in the core array and decoder. Also there are $2 \cdot (N_a - h)$ black blocks in the decoder area and 2 junctions with microwires. So the yield for a single core nanowire is:

$$\begin{aligned} P_{core-wire} &= (1 - P_{mj})^2 \cdot (1 - P_l)^L \\ &\quad \cdot (1 - P_{nj})^{(2h+N)} \\ &\quad \cdot (1 - P_{bp})^{2 \cdot (N_a - h)} \end{aligned} \quad (3)$$

If using a $h - hot$ addressing technique, the number of lines can be addressed by N_a address lines is:

$$N_{la}(N_a) = \frac{N_a!}{h! \cdot (N_a - h)!} \quad (4)$$

Then, let us calculate the expectation of how many core nanowires in the rows are addressable by N_a address lines:

$$\begin{aligned} E(N) &= \frac{N}{N_{la}(N_a)} \cdot \sum_{m=0}^{m=N_a} N_{la}(N_a - m) \cdot C(N_a, m) \\ &\quad \cdot P_{add}^{N_a - m} \cdot (1 - P_{add})^m \end{aligned} \quad (5)$$

where the $C(N, M)$ is the number of combinations of taking M things from N at a time. And then we can calculate the net row yield $Yield_{row}$:

$$Yield_{row} = \frac{E(N)}{N} \cdot P_{core-wire} \quad (6)$$

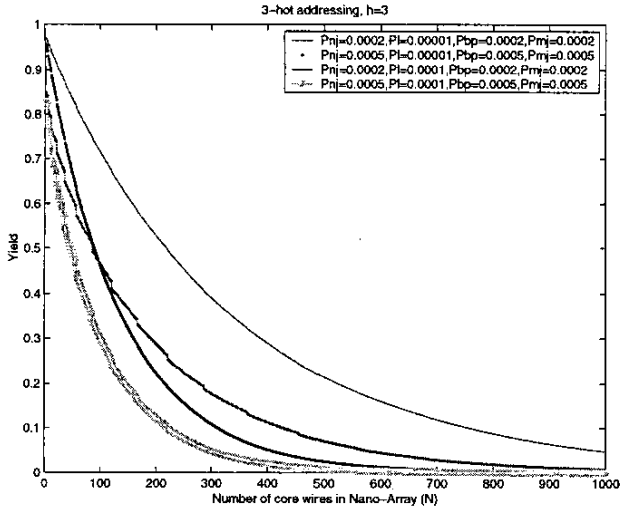

Fig. 2. Yield of single nanoarray versus array size with 3-hot addressing

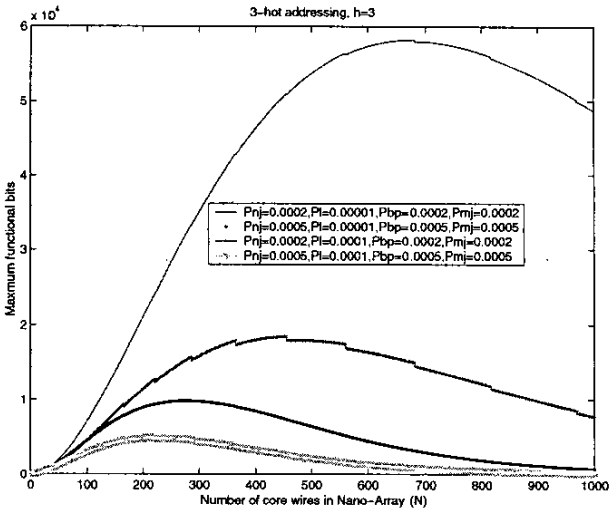

Fig. 3. Maximum functional bits can be achieved with 3-hot addressing

This is about the row yield, by symmetry, we can get the column yield all the same way. Thus the final yield of the array core is:

$$Yield_{core} = Yield_{row} \cdot Yield_{column} \quad (7)$$

Based on current reports [8], [12] on the reliable growth of SiNWs and yield of junctions, we assume the P_{nj} from 0.0002 to 0.0005 as well as the P_{bp} and P_{mj} and assume P_l from 0.00001 to 0.0001. We can also calculate the maximum number of functional bits in the array and find out the optimal point by the equation:

$$Q_{function-bits} = Yield_{core} \cdot N^2 \quad (8)$$

If we choose $h = 3$ (i.e., 3-hot addressing scheme), the results are showing in Figures (2) and (3).

From figure (3), we can conclude that the maximum density can be achieved approximately at $N = 700$, 450, 250 and 200, respectively.

III. Conclusion

In this draft, We have introduced various defect parameters such as the crosspoint failure rate, nano-wire to micro-wire connection failure rate, decoder failure rate, etc. Based on those characterized defects, a comprehensive probabilistic yield model for the array-based nanoarchitecture has been proposed and verified. Then we have used a series of numerical simulations to obtain simulation results such as the nano array yields and subarray densities using a wide variety of parameter sets. Also we introduce a way to find the optimal subarray density, in which we can achieve the largest number of functional bits in the subarray. Finally, we compare the results from different $h-hotaddressing$ schemes. Using the proposed probabilistic yield model and some experimental/industry data, we can accurately estimate the yield and subarray density. Also, we can compare the efficiency of different fault tolerance techniques.

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