Failure Analysis Requirements for Nanoelectronics

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***Abstract*—Failure analysis (FA) plays a vital role in the development and manufacture of integrated circuits. However, instrumental limits are already threatening FA in the tenth-micron CMOS realm, and nanoelectronic devices will find key analytical tools two orders of magnitude removed in capability. This paper will introduce state-of-the-art microelectronic failure analysis processes, instrumentation, and principles. It will discuss the major limitations and future prospects determined from industry roadmaps. Specifically highlighted is the need for a fault isolation methodology for failure analysis of fully integrated nanoelectronics devices.**

***Index Terms*—Failure analysis (FA), fault diagnosis, inspection, microscopy, testing.**

NOMENCLATURE

AFM	Atomic force microscope.
CC SEM	Charge contrast scanning electron microscopy.
CMP	Chemical–mechanical polishing.
CT AFM	Conductive tip AFM.
DFD	Design for diagnosability.
FIR	Far infrared.
FMI	Fluorescent microthermal imaging.
ITRS	International technology roadmap for semiconductors.
LCE	Laser chemical etch.
LIVA	Light-induced voltage alteration.
LVP	Laser voltage probe.
MFM	Magnetic force microscopy.
NB-OBIC	Nonbiased OBIC.
NIR	Near infrared.
OBIC	Optical-beam-induced current.
OBIRCH	Optical-beam-induced resistance change.
PEM	Photon emission microscopy.
PFI	Physical fault isolation.
PICA	Picosecond imaging circuit analysis.
RIE	Reactive ion etch.
SEI	Seebeck effect imaging.
SET	Single-electron transistor.
SPM	Scanning probe microscopy.
SQUID	Superconducting quantum interference device.
SRL	Shift register latch.
SSM	Scanning SQUID microscopy.
SThM	Scanning thermal microscopy.
STM	Scanning tunneling microscopy.
STM	Schlieren thermal mapping.
TEM	Transmission electron microscopy.
TIVA	Temperature-induced voltage alteration.
XRT	X-ray tomography.

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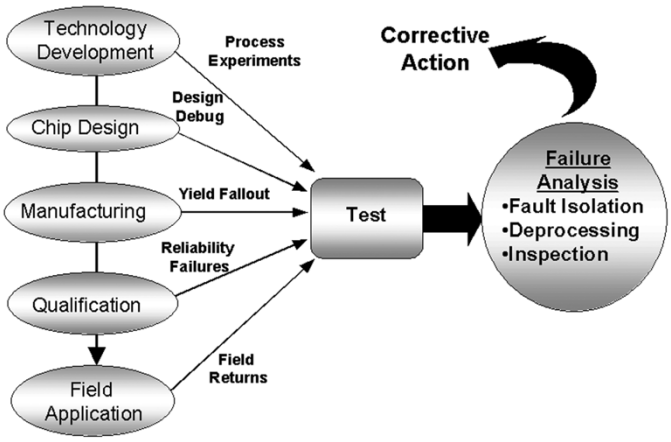

Fig. 1. Sources of failure during integrated circuit lifecycle, and basic failure analysis steps.

I. INTRODUCTION

FAILURES OF ICs come from a variety of sources, as seen in Fig. 1. Failure analysis (FA) is essential in shortening time to market, controlling manufacturing costs, and ensuring high reliability [1]. The basic process (Fig. 1) localizes an electrical fault to a specific area on the IC that is then deprocessed and inspected to identify the mechanism responsible and determine its source.

The analytical instrumentation used has inherent physical and electrical limitations that affect productivity and eventually basic ability. Future CMOS FA challenges [2]–[6] are determined by examining the International Technology Roadmap for Semiconductors (ITRS) and other such prospective works [7]–[9]. Of added interest is the impact of next-generation computing technology on FA capability. The Technology Roadmap for Nanoelectronics [10] and related publications describe devices and architectures that will require especially robust analytical capability when mature, and fully integrated into working circuits and systems.

The term *microelectronic(s)* and *CMOS* will be used interchangeably to describe classical complementary-metal-oxide-silicon technology and its derivatives. *Nanoelectronic(s)* will be used to broadly denote emerging next-generation logic building blocks and proposed interconnection architectures thereof, including QCA, RTD, SET, RSFQ, CNT, and molecular devices.

Section II reviews the state of the art in microelectronics FA. Section III discusses major challenges posed and looks ahead to long-term projected needs for functional nanoelectronic ICs. The material focuses on logic devices only (as opposed to memory), and excludes the field of chemical and materials analysis.

II. Overview of Microelectronics FA

A. Inspection

The raw spatial resolution of commonly used electron and scanning probe microscopes (SEM, TEM, and SPM) is more than adequate for minimum-sized CMOS defects of 20 nm and less (projected to occur in the middle of the next decade). However, high magnification trades off field-of-view and depth-of-field, placing major limits on inspection area. So defects must be prelocalized to a precise horizontal region and vertical level. X-ray tomography (XRT) is an emerging technique that can help isolate defects nondestructively for higher resolution inspection [11], [12]. It combines transmitted absorption and phase contrast with three–dimensional (3-D) reconstruction. Nondestructive images of multilevel conductors buried in insulator have been produced at resolution below 100 nanometers.

B. Deprocessing

Deprocessing uncovers defects intact for inspection or more localized fault isolation. A combination of wet chemistry, plasma etching, and chemical–mechanical polishing (CMP) is used for removing films across the entire chip surface. Laser ablation, focused ion beam (FIB), and ion milling, often gas-enhanced for improved selectivity, remove material in much smaller areas. The key parameters are removal rate and material selectivity.

C. Physical Fault Isolation (PFI)

PFI localizes defects for subsequent deprocessing and inspection using light, heat, and electric or magnetic field. In so-called passive mode a steady-state photon emission, thermal gradient, or magnetic field image is made with the defective circuit energized. Short circuits are particularly active because of localized high current density. This class of techniques includes photon emission microscopy (PEM), infrared imaging, Schlieren thermal mapping (STM), and scanning SQUID (superconducting quantum interference device) microscopy (SSM) [13]–[18].

Another group, often referred to as active techniques, uses the chip's electrical response to a scanned laser or electron beam that alters electrical properties of the defect or the circuit it affects by inducing a photocurrent, thermal potential, or resistance change [19], [20]. The corresponding change is detected at the circuit's input, output, or power supply pins where the signal is amplified and correlated to the position of the beam at the time of the change. Temperature- or light-induced voltage alteration (TIVA/LIVA), optical beam induced resistance change (OBIRCH), optical beam induced current (OBIC), and charge contrast SEM (CC SEM) are the most commonly used. Fig. 2(a) illustrates a typical PFI setup with Fig. 2(b) showing selected examples.

A third class of techniques [21]–[23] examines time-dependent events. Picosecond imaging circuit analysis (PICA) is an extension of PEM that time-resolves the photon emission. Laser voltage probing (LVP) creates waveforms from transistors using charge-density modulation of an incident laser probe.

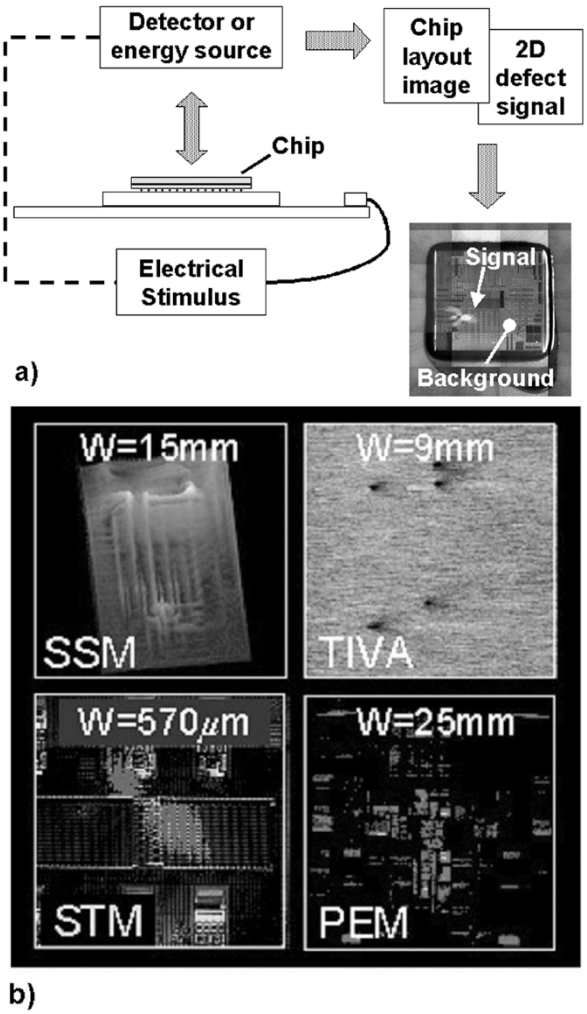

Fig. 2. (a) PFI setup showing overlay of defect signal (scanning SQUID microscopy in this case) with background NIR image. (b) Example PFI image overlays showing approximated width of background area (W) on which signal is overlaid.

PFI is now performed predominantly through the backside of the chip (i.e., through the silicon substrate) because dense wiring patterns on the topside impede signals. Near-infrared (NIR) radiation above 900 nm is used for imaging and probing on chips that have been thinned and polished to improve optical transmission through the relatively absorptive doped silicon.

D. Electrical Fault Isolation

Electrical fault isolation differs from PFI in that localization is accomplished using the chip's output logic data and defective circuit simulation. Combinatorial logic is designed with strings of shift register latches (SRLs) throughout called *scan chains*, as seen in Fig. 3(a). When an output fails, latches in the scan chains hold the failing bits. The latches thus identify an input *cone of logic*. Fault simulation then determines probabilities of defective logic nodes and circuit blocks (e.g., NAND gates) within the cone by seeding faults at known locations and comparing results to actual chip data [24]–[28]. Fig. 3(b) shows how failing nodes are physically mapped and located on the chip layout.

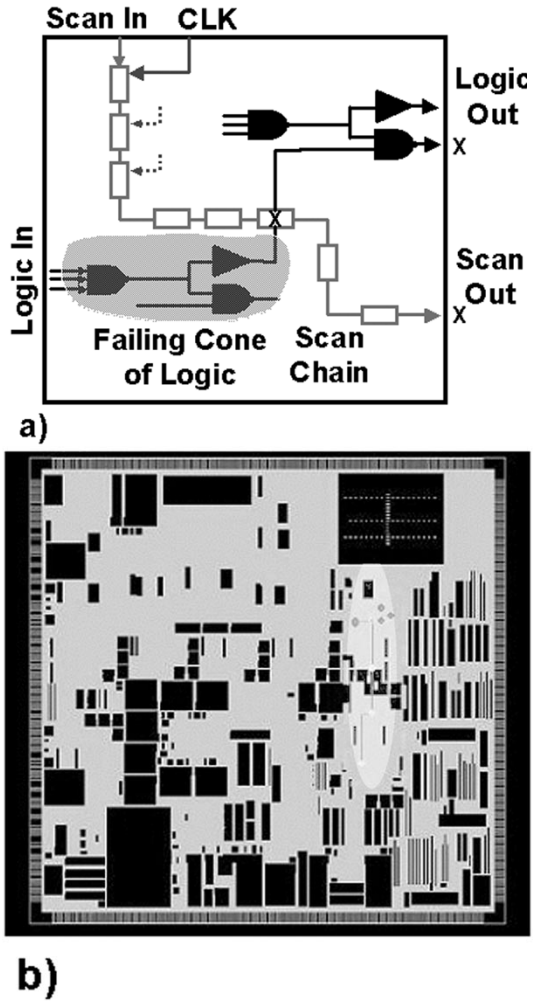

Fig. 3. (a) Electrical fault isolation design showing sequential chains of shift-register latches placed throughout combinatorial logic, failures detected (denoted by "X"), and failing "cone of logic" identified for subsequent fault simulation and diagnostics. (b) Failing logic nodes (highlighted oval) mapped onto physical chip layout. Chip is approximately 12 mm square.

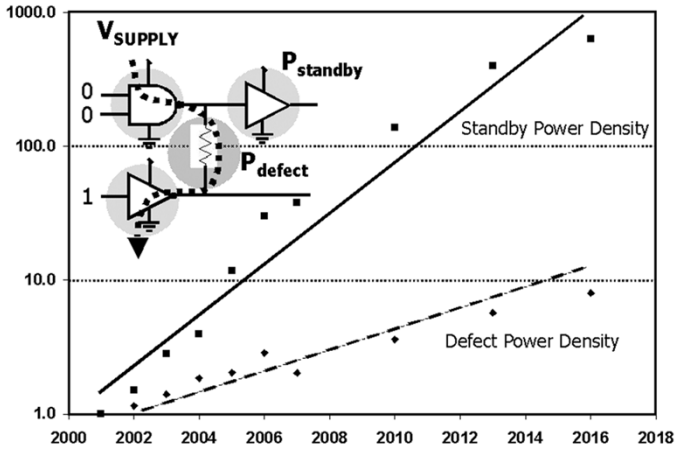

Fig. 4. Relative rates of increase in calculated defect power density versus chip standby power density (normalized to 2001) for a typical internode short-circuit defect (shown in inset). Derived from fundamental ITRS data.

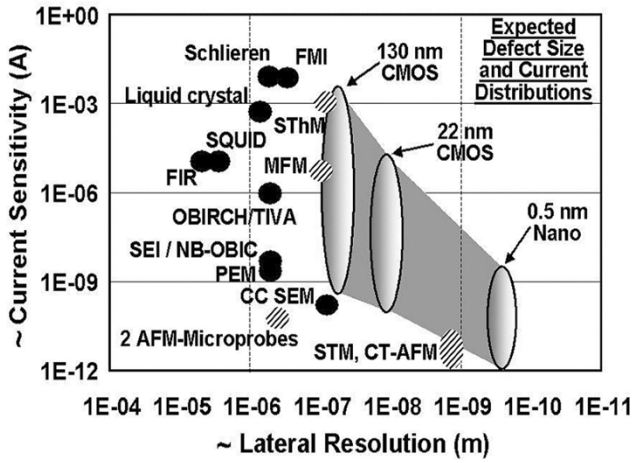

Fig. 5. Matrix of approximate current sensitivity versus lateral spatial resolution for physical fault isolation methods. Expected current-draw and size distribution for minimum-sized defects from state-of-the-art CMOS through projected molecular-scale devices is shown for comparison (solid ovals indicate far-field measurements; crosshatched ovals denote near-field probes).

III. Sub-0.1 μm CMOS Limitations and Nanoelectronics FA Outlook

Resolving power versus projected defect sizes is more than adequate with current microscopes, even for nanoscale devices. But nondestructive inspection of low-charge quantum and single-electron devices may be prohibitive as damaging electrical effects of high-energy incident radiation are already observed [29] on relatively robust CMOS devices. The SPM is an obvious alternative, already in prevalent use on nanodevices [30]–[32], but it necessitates surface exposure of defects, and so-called 'nonvisible' defects are already encountered on microelectronic devices. The single-electron and atomic scale of nanoelectronic devices will likely be equally if not more susceptible. Thus, fault isolation and deprocessing will become more critical in precisely isolating invisible faults on complex nanoscale integrated circuits in three dimensions, and nondestructively exposing them for inspection.

Base technology for full-chip deprocessing historically comes from IC manufacturing methods. This trend must continue, at least for '"bottom-up" nanoelectronics where radical new assembly processes are already emerging. The SPM already plays a major role in nano-manipulation and assembly [33] and could provide local deprocessing techniques for disassembly as well.

The above inspection and deprocessing limitations will strongly drive the need for better fault isolation. PFI capability depends primarily on signal-to-noise ratio. For CMOS it is already threatened as shown by Fig. 4, where sub-threshold transistor leakage may cause standby power density to grow at an accelerated rate versus typical defect power density. The overall relationship between demonstrated current sensitivity vs. spatial resolution for numerous PFI methods, including early nanoelectronic device measurements, is shown in Fig. 5. Not shown are the timing methods PICA and LVP. Both may be intractable in the nanoelectronic realm primarily because of their dependence on NIR imaging, which is diffraction-limited to just under 1 μm.

Electrical fault isolation is independent of technology scaling, but resolution is limited in the best case to one logical node or

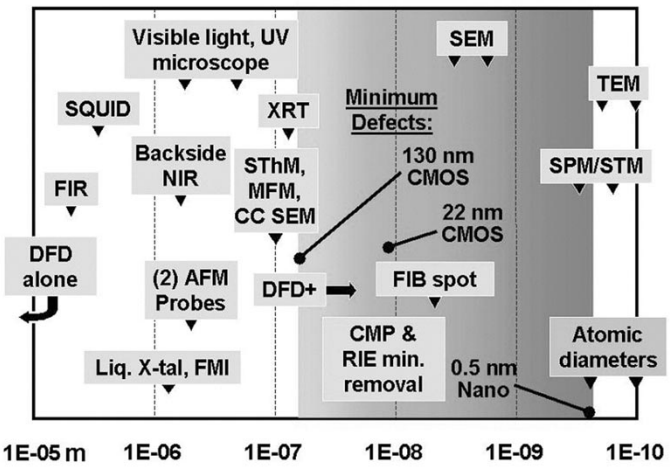

Fig. 6. Overall comparison of lateral spatial resolution of failure analysis tools and techniques compared with projected minimum defect sizes (equal to one-half of the minimum technology feature size) for future IC technology nodes.

circuit block, more typically to less than ten. While the search volume is much reduced from that of an entire chip, it is still prohibitively large. A single faulty node of average-length on a modern logic chip has a ratio of search volume to minimum-sized defect volume of about 8×10^7-to-1 (versus about 2×10^{14}-to-1 for the entire 10-mm-square chip). However, resolution improves orders of magnitude when the identified node is convolved with PFI data, layout information, or inline defect location. Some faults, like power supply short circuits and analog failures, are not diagnosable with scan diagnostics and must rely solely on the physical isolation alternatives discussed.

IV. Conclusions

A broad overview of CMOS failure analysis and its limitations for fully integrated nanoelectronic ICs has been presented. Fig. 6 summarizes the spatial resolution of a number of FA techniques compared with expected defect sizes. The generic process of fault isolation, deprocessing, and inspection appears adequate, at least for traditional "bottom-up" assembly. While microscopy is not an issue, disassembly and deprocessing methods that leave defects intact must be developed concurrently with nanoelectronic manufacturing methods.

With the exception of near-field transistor-level probes like STM and CT-AFM, PFI instruments severely lack resolution for nanoelectronic scale ICs. Innovation and development are needed for improved sensors and detection schemes for far-field imaging of signals in the picoampere to nanoampere range. Wide-area imaging or perturbation of quantum device properties might provide active PFI alternatives.

Electrical fault isolation provides the greatest leverage and as such it is critical that diagnosability be designed into nanoelectronic ICs. New devices and architectures like multistate logic may offer improved potential. The lack of a timing probe will also be critical and must be overcome to understand mechanisms that will undoubtedly limit high gigahertz and terahertz operation.

Self-assembly poses altogether new challenges, as the traditional analytical approach is heavily dependent on *a priori* knowledge of circuit layout and electrical response. Finally, reconfigurable and fault-tolerant architectures may certainly allay the need for FA, but it is unreasonable to expect they will obviate it altogether.

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