A Circuit Model for Carbon Nanotube Interconnects: Comparative Study with Cu Interconnects for Scaled Technologies

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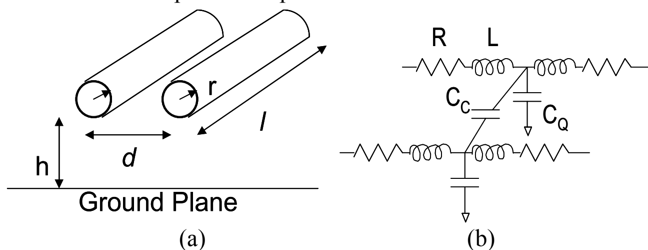
Abstract: Semiconducting carbon nanotubes (CNTs) have gained immense popularity as possible successors to silicon as the channel material for ultra high performance field effect transistors. On the other hand, their metallic counterparts have often been regarded as ideal interconnects for the future technology generations. Owing to their high current densities and increased reliability, metallic-single walled CNTs (SWCNTs) have been subjects of fundamental research both in theory as well as experiments. Metallic CNTs have been modeled for RF applications in [1] using an LC model. In this paper we present an efficient circuit compatible RLC model for metallic SW CNTs, and analyze the impact of SW CNTs on the performance of ultra scaled digital VLSI design [2].

I. INTRODUCTION

Carbon nanotubes [3] are sheets of graphite rolled into cylinders of diameters varying from 0.6nm to about 3nm. Depending on the direction in which they are rolled (called chirality), a CNT can be semiconducting with a distinct bandgap or it can be metallic with no bandgap. Metallic carbon nanotubes have been identified as a possible interconnect material of the future technology generations and be heir to Al and Cu interconnects. Leading theoreticians as well as experimentalists have started research in the earnest to understand the transport mechanisms and the conducting properties of the metallic CNTs [4]. Both single-walled carbon nanotubes (SWCNTs) as well as multi-walled carbon nanotubes (MWCNTs) are being investigated for performance and scalability. It has been demonstrated that MWCNTs are diffusive and have high IR drops whereas in SWCNTs, ballistic transport (drift) can be achieved and would be suitable for interconnect designs. However, in both SWCNTs and MWCNTs, very high current densities have been noted with very little performance degradation. For example, Wei et al.[5] showed that the current carrying capacity of CNTs did not degrade after 350h at current densities of ~10^{10} A/cm^2 at 250 °C. The thermal conductivity of CNTs [6] is about 1700–3000 W/m K. In this paper, for the first time, we envisage a realistic scenario where carbon nanotube interconnects with their intrinsic resistances and capacitances and the extrinsic (or parasitic) capacitances and inductances have been evaluated for performance. We have compared the performance of metallic SWCNTs with scaled Cu interconnects. We have used an RLC based circuit-compatible model for Cu interconnects. In the practical scenario, a damascene process is used in Cu technology to make narrow trenches and fill it up with Cu. This results in reduced interconnect dimensions and high scalability. However, it comes with the price of increased surface and grain boundary scattering. These effects have been introduced in our circuit compatible model of Cu interconnects.



(a) (b)

Fig. 1: (a) Geometry of CNT (b) RLC model of parallel CNTs

II. MODELING CARBON NANOTUBE INTERCONNECTS

Let us consider a system of parallel carbon nanotubes, as shown in fig. 1a. Let the radius of the nanotubes be r, the separation between nanotubes be d and let the length of a nanotube be l. We can describe the interconnect behavior of the nanotube as that of a transmission line with an RLC model as illustrated in fig. 1b and proposed in [1]. However, in [1] the diffusive component, R was not modeled and was taken to be in the ballistic limit. In such a case, the intrinsic impedance (also called the contact or quantum resistance) is given by h/e^2 where e is the electronic charge and h is Plank's constant [7]. However, this is an optimistic assumption and under high bias or long interconnects lengths, electron-phonon interactions start to play an important role and the effects of scattering need to be incorporated.

In the next three subsections, we will elaborate the R, L and C models used in our simulations.

A. Resistance

Recent experiments by Ji-Yong Park et. al. [8] have measured the dc resistance of SW metallic CNTs of diameter 1.8nm (r=0.9nm). In this incoherent limit for four such channels of conduction, the differential resistance of a nanotube of length l (> λ) is given by [7]:

$$R_{diff} = \frac{dV}{dI} = \left(\frac{h}{4e^2}\right)\frac{l}{\lambda} \qquad (1)$$

where, V is the applied voltage, I is the current thorugh the CNT and λ is the mean free path (*mfp*). If $l < \lambda$, the resistance is a constant given by the quantum resistance for four channels ($h/4e^2$).

The value of λ is given by the scattering mechanism and is dependant on the length of the nanotube and the applied bias. For low biases ($V_{critical}$<160mV), the principle scattering mechanism is due to acoustic phonons having a *mfp* of about 1.6µm (λ_{acc}). For higher supply biases the optical phonon (λ_{op} ~ 200nm) and zone boundary phonon (λ_{zo}~30nm) scattering becomes dominant. Thus it is evident that the resistance of a CNT will be a function of the bias voltage (V_{bias}) as well as the length. Hence depending on the bias, the differential resistance can be expressed as:

For V< $V_{critical}$:

$$R_{diff}^{low} = \frac{dV}{dI} = \left(\frac{h}{4e^2}\right)\Theta\left(\frac{l}{\lambda_{low}}\right) \quad (2a)$$

For V> $V_{critical}$

$$R_{diff}^{high} = \frac{dV}{dI} = \left(\frac{h}{4e^2}\right)\Theta\left(\frac{l}{\lambda_{high}}\right) \quad (2b)$$

where,

$\Theta(x) = 1$ for x<1

=x otherwise

$\lambda_{low} = \lambda_{acc}$ and $\lambda_{high} = (\lambda_{op}^{-1} + \lambda_{zo}^{-1})^{-1}$.

We have validated this resistance model described by (2) against recently published experimental data. Fig. 2 shows how the proposed model corroborates with experimental data presented in [8] both for high as well as low voltage biases.

It should be noted that eqn. (2) describes the *differential resistance* of a metallic CNT. It is necessary to obtain the net (or dc) resistance of the CNT. Hence the overall dc resistance (the ratio of the total current, I_{net} to the corresponding bias voltage V_{bias}) can be written as:

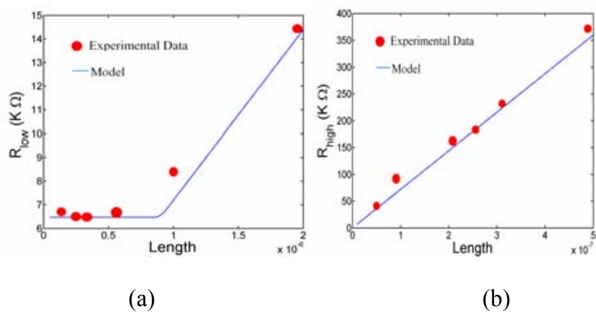
For V< $V_{critical}$:

$$R^{low} = R_{diff}^{low} \quad (3a)$$

For V> $V_{critical}$

$$R^{high} = \left(\frac{V_{critical}}{V_{bias}}\left(\frac{1}{R_{diff}^{low}} - \frac{1}{R_{diff}^{high}}\right) + \frac{1}{R_{diff}^{high}}\right)^{-1} \quad (3b)$$

Thus we have developed a length and bias dependant piecewise linear resistance model which has been verified with experimental data. For short lengths of the nanotube, under small bias voltages, the quantum resistance limit (or, ballistic transport) can be reached. However, for longer lengths of the current saturates to a constant value of around 25µ A. We have used this resistance model for circuit simulations using SPICE.



(a) (b)

Fig. 2: Differential resistance of a CNT : Validation of the proposed model with experimental data [8] : (a) for low bias (b) for high bias

B. Inductance

To obtain the inductance of the CNT we follow the procedure explained in reference [1,9]. Let us first consider the magnetic inductance between a CNT and the ground plane. In the presence of a ground plane, the magnetic inductance per unit length is given by [9] :

$$L_{magnetic} = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{2h}{d}\right) \quad (4)$$

This is calculated by relating the total magnetic energy and relating it to the current flowing in the wire. For a typical situation, the nanotube is on top of an insulating (typically silicon-dioxide) substrate, with a conducting medium below. A typical oxide thickness is between 10nm and 1 µ m whereas a typical nanotube radius of 1nm-2 nm. It can be noted that the magnetic inductance is a relatively weak function of the factor (*h/d*) and for typical geometries it can be estimated to be around 1nH/µm.

For one dimensional conductors, the kinetic inductance is as important as the magnetic inductance. The details of its derivation can be found in [1]. The kinetic inductance is given by

$$L_{kinetic} = \frac{h}{2e^2 v_F} \quad (5)$$

~ 16nH/µm

Hence, in the transmission line model (fig. 1b) we have considered kinetic inductance only ($L = L_{kinetic}$) and have neglected magnetic inductance.

C. Capacitance

For CNT interconnects laid down in parallel, two distinct capacitances would be important. One of them is the coupling electrostatic capacitance, C_C and the other is the quantum capacitance of the metallic nanotube. Equating this with the energy stored in the quantum capacitance we obtain [9]

$$C_Q = \frac{2e^2}{hv_F} \quad (6)$$

~ 100 aF/µm

Apart from the quantum capacitance, the electrostatic capacitance is also important in parallel layout of CNT interconnects. The coupling capacitance between two CNTs each of radius *r* laid out at a distance *d* between them is given by

$$C_C = \frac{\varepsilon\pi l}{\ln\left(\frac{d}{2r} + \sqrt{\left(\frac{d}{2r}\right)^2 + 1}\right)} \quad (7)$$

Thus we have a complete RLC model for the CNT interconnects.

II. MODELING Cu INTERCONNECTS

For the purpose of comparison, we have also modeled and simulated Cu interconnects (fig 3).

A. Resistance

Grain boundary and surface scattering effects have been incorporated in a manner described in [4] to determine the resistivity of copper. The surface scattering effects can be modeled using a correction term to the intrinsic resistivity of Cu. The size dependant resistivity is given by [11]

$$\rho_{size} = \rho_i \left[1 - \frac{3}{2k}(1-p)\int_1^{\infty}\left(\frac{1}{t^3} - \frac{1}{t^5}\right)\frac{1-e^{-kt}}{1-pe^{-kt}}dt \right]^{-1} \quad (8)$$

where k is the ratio of the film thickness (h_{cu}) and the electron mean free path and p ($0 \le p \le 1$) is the surface scattering coefficient. Similarly the grain boundary scattering can be included in the resistivity model using

$$\rho_{grain} = \frac{\rho_i}{3}\left[\frac{1}{3} - \frac{1}{2}\alpha + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]^{-1} \quad (9)$$

$$\alpha = \frac{\lambda}{d_g}\frac{R}{1-R}$$

where d_g is the grain diameter, λ is the electron mean free path and R ($0 \le R \le 1$) is the grain boundary reflection coefficient. In a manner described in [11] we have assumed $p=0.6$ and $R=0.4$. The grain boundary is also assumed to be equal to the width of the copper wire and hence $d_g = w_{cu}$. Hence the total resistance of each Cu wire is given by

B. Capacitance

The coupling capacitance between adjacent copper wires is given by the simple parallel plate capacitance formula

$$C_C = \frac{\varepsilon h_{cu} l}{(d - w_{cu})} \quad (10)$$

C. Inductance

The self inductance and mutual inductances of the Cu interconnects have been determined using the software tool MIND [12]. It involves calculation of the magnetic energy of a set of parallel wires and equating the total magnetic energy with that

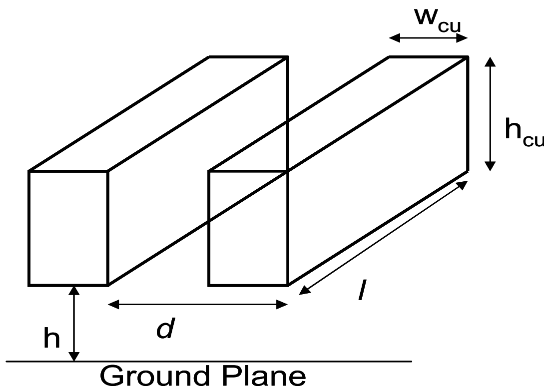


Fig. 3: Layout of parallel Cu interconnects showing the interconnect dimensions. Note that h_{cu} is the height of a Cu wire whereas h is its height from the ground plane.

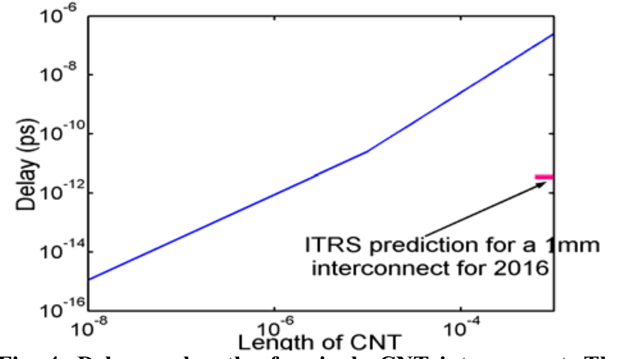


Fig. 4: Delay vs. length of a single CNT interconnect. The ITRS prediction has been marked. Note: The length of the CNT is in meters.

stored in an equivalent inductance. The details of the derivation can be found in [12] and will not be discussed here.

Thus we have developed an equivalent RLC model for Cu interconnects and this has been used in comparing performance of Cu interconnects vis-à-vis CNT interconnects.

III. SWITCHING DELAY USING SINGLE AND MULTIPLE CARBON NANOTUBES

In the next few sections, we will estimate the switching delay of a CNT interconnect and compare it with traditional Cu interconnect. Also the implications of scaling on CNT interconnects will be discussed.

A Single CNT interconnect

First, let us consider a single CNT used as an interconnect. Consider a step input of maximum voltage 500mV to such a CNT. Fig. 4 shows the switching delay as a function of length for a single CNT interconnect. It can be noted that the switching delay for the CNT is several orders of magnitude higher than that predicted by ITRS. This is due to the large resistance of a single CNT. Even for perfect contacts and at low bias the minimum resistance of a CNT interconnect is $h/(4e^2)$, which is approximately 6KΩ. This resistance increases as the length of the interconnect increases and as the voltage across the CNT exceeds $V_{critical}$. As a result the switching delay increases fast and far exceeds the ITRS prediction. Hence we conclude from here that *a single CNT would be insufficient to act as a high speed interconnect* for the future technology.

B. Parallel CNT interconnects

The next logical step would be to use CNTs in parallel that can be used to route a single signal. The corresponding layout is demonstrated in fig. 5 where N_x parallel interconnects have been used as a single effective interconnect wire. It has been noted earlier that CNTs have a typical current handling capacity of 25uA/nanotube. Let us consider a current requirement of 500uA. Hence we would require 20 nanotubes in parallel (N_x = 20). With a spacing of 2r (r=1.8nm) between the nanotubes, it will take a width ($w = 2r(N_x-1)$) of 80nm.

For comparison, let us consider a copper interconnect of the same width (w_{cu} = 80nm). The maximum current handling capacity is much lower ($J_{max} \sim 10^6$A/cm^2). However, the damascene process allows making deep trenches and using copper interconnects which are far deeper than they are wide. In our example, for a J_{max} of

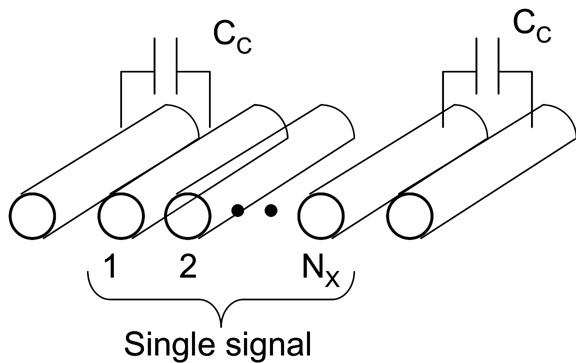


Fig. 5: Layout of parallel CNTs. N_X CNTs have been used to route the same signal. Only the 1st and the N_x^{th} CNT feels the coupling capacitor C_C

10^6A/cm^2 the height, h_{cu} needs to be 625nm in order to supply 500uA. This aspect ratio of 1:8 is easily possible in Cu technologies.

Fig. 6, shows the switching delay of 20 parallel CNT interconnects and the copper interconnect (w_{cu} = 80nm and h_{cu} = 625nm). It can be noted that the CNT has a much higher switching delay than copper, in spite of its higher current density. This apparently counter-intuitive result can be easily understood by noting that:

- Practical complementary MOS circuits are voltage driven and not current driven. In other words, the capacitors (gate capacitance + parasistics) are charged through resistive paths by a constant voltage source (V_{dd}).
- In voltage driven circuits the resistance of the interconnect wire and not its current density is important for performance. An ideal current source can pump a high current through the small cross-sectional area of the CNT. However, the resistance offered by the CNT is intrinsically high and controls the RLC switching delay.
- The damascene process allows a high aspect ratio (ratio of h_{cu} to w_{cu}) of the Cu interconnects which substantially reduces the resistance of the Cu wire.

It should thus be noted that for a *voltage driven circuit the interconnect resistance and not the current density determines the switching speed.*

C. Oscillator frequency

In the previous sub-sections we have considered the RLC switching delay of CNT interconnects and compared with Cu. Now let us consider a three-stage ring oscillator [13] made of scaled silicon MOSFETs. Simulations have been carried out using BPTM

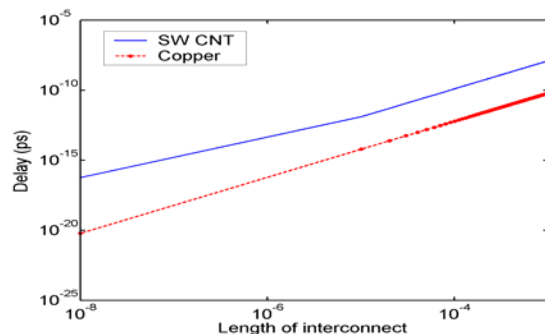


Fig. 6: Comparison of delay of 20 parallel CNT interconnects with copper interconnect having the same equivalent width (w=80nm). Note: The interconnect length is in meters.

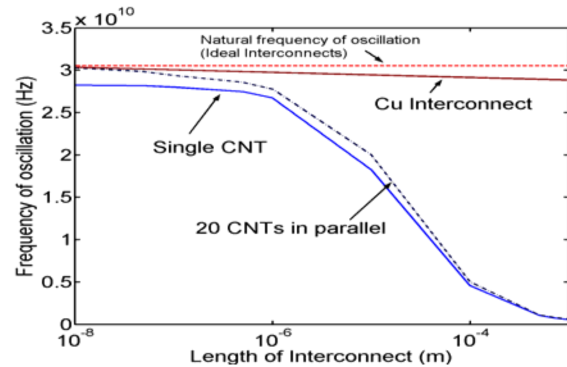


Fig. 7: The effect of interconnect on the oscillation frequency of a three-stage ring oscillator. Note how the CNT interconnects degrade the performance because of their high intrinsic resistance.

MOSFET models of 45nm channel length [14]. Fig. 11 shows the effect of interconnects on the frequency of oscillation.

It can be observed that CNT interconnects can reduce the frequency of oscillation by orders of magnitude if the interconnect is longer than 1μm. For shorter interconnects the degradation of performance is small. If parallel CNTs are used then the effective interconnect resistance reduces. However the resistance offered by Cu interconnects is orders of magnitude smaller than CNT and it has been shown in fig. 11.

IV. CONCLUSION

This paper, for the first time, provides a realistic RLC model for CNT interconnects. Inspite of the high current density, CNT interconnects suffer from very high intrinsic resistance and kinetic inductance and severely limits high frequency of operation. Performance can be improved by routing the same signal through parallel CNTs. It has been shown that it requires a substantial increase in the number of metal layers to meet the performance of copper in the same die area. Thus CNTs provide reliable interconnect solutions but are limited in terms of performance in the high performance digital VLSI.

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