Circuit Modeling of Carbon Nanotube Interconnects and their Performance Estimation in VLSI Design*

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The *International Technology Roadmap for Semiconductors* (ITRS) emphasizes on the need for reliable, high speed interconnects for the future technology generations. Innovative materials are being extensively studied and carbon nanotubes (CNTs) have emerged as a promising material for future generation ICs. Recent experiments have shown that CNTs can handle extremely high current densities (~10^{10} A/cm^2) for hours without significant degradation of performance. In this paper we have developed a comprehensive RLC transmission line model for metallic CNTs (Fig 1) [1], and evaluated their performance in high speed VLSI design.

Recent experiments by Ji-Yong Park et. al. [2] have measured the dc resistance of SW metallic CNTs of diameter 1.8nm (r=0.9nm). For low biases ($V_{critical}$<160mV), the principle scattering mechanism is due to acoustic phonons having a mfp of about 1.6μm (λ_{acc}). For higher supply biases the optical phonon (λ_{op} ~ 200nm) and zone boundary phonon (λ_{zo}~30nm) scattering becomes dominant. Thus it is evident that the resistance of a CNT will be a function of the bias voltage (V_{bias}) as well as the length. Hence depending on the bias, the differential resistance can be expressed as:

From this we have arrived at the dc resistance of the CNT and this has been validated against

For $V < V_{critical}$:

$$R_{diff}^{low} = \frac{dV}{dI} = \left(\frac{h}{4e^2}\right)\Theta\left(\frac{l}{\lambda_{low}}\right) \quad (1a)$$

For $V > V_{critical}$

$$R_{diff}^{high} = \frac{dV}{dI} = \left(\frac{h}{4e^2}\right)\Theta\left(\frac{l}{\lambda_{high}}\right) \quad (1b)$$

where, $\Theta(x) = 1$ for x<1
=x otherwise

$\lambda_{low} = \lambda_{acc}$ and $\lambda_{high} = (\lambda_{op}^{-1} + \lambda_{zo}^{-1})^{-1}$

experimental data (Fig 2). The capacitance and inductance models have been derived in a manner described in [1].

Fig. 3a shows the switching delay as a function of length for a single CNT interconnect. Fig 3b shows the switching delay vs. length for a parallel arrangement of 20 CNTs. The delay of a Cu interconnect of equivalent width has been shown for comparison. It can be noted that the switching delay for the CNT is several orders of magnitude higher than that predicted by ITRS. This is due to the large resistance and high kinetic inductance of the CNT. Even for perfect contacts and at low bias the minimum resistance of a CNT interconnect is $h/(4e^2)$.

It can be also noted that the CNT has a much higher switching delay than copper, in spite of its higher current density. This is because for a given number of metal layers, *it is not current per unit area, but current per unit width, that plays a more significant role.* Copper has much higher current per unit width because its cross sectional area is much larger than CNT. In order to gain benefit of the high current density of CNTs, in any design using CNT interconnects, we would require a larger number (~ 200 for each Cu layer) of metal layers.

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References:
[1] P. J. Burke, IEEE Trans. On Nanotech, Vol 1(3), Sept 2002, pp: 129-143
[2] Ji-Yong, et. al., cond-mat/0309641, Sept. 28, 2003.

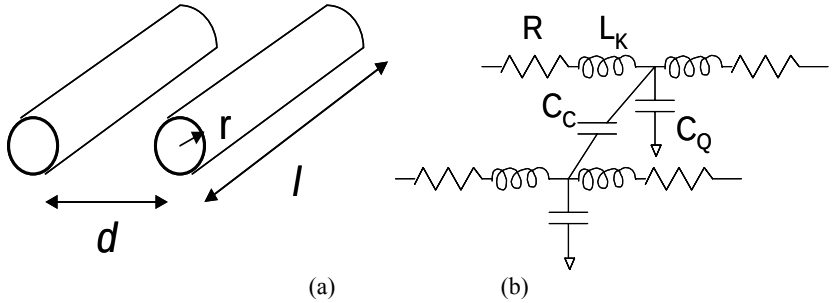
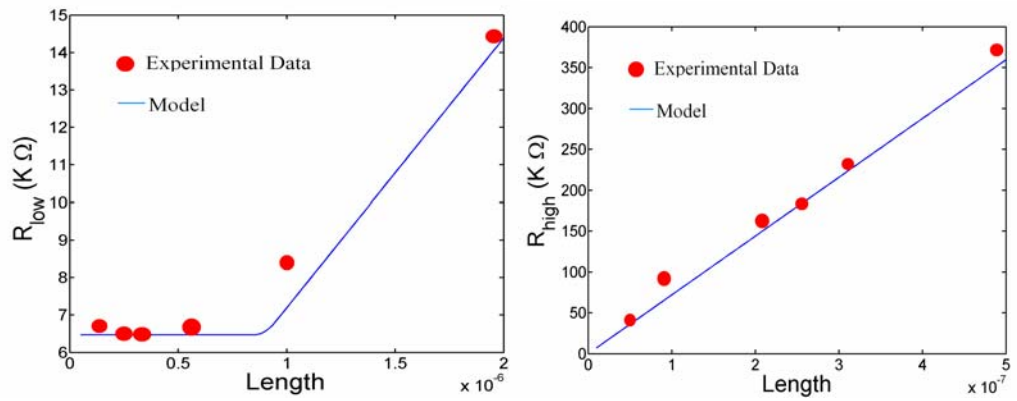
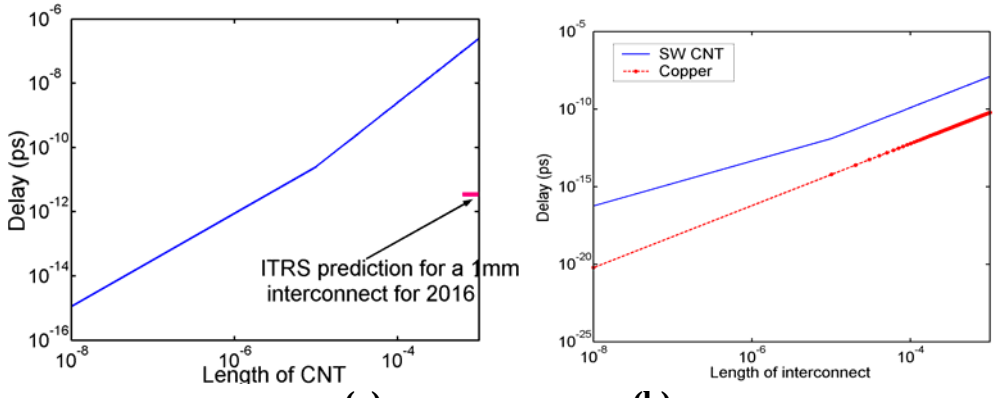


Fig 1: (a) Geometry of CNT (b) RLC model of parallel CNTs



(a) (b)

Fig 2: DC resistance of a CNT : Validation of the proposed model with experimental data [2] (a) for how bias (b) for high bias [Length is in m]



(a) (b)

Fig 3: (a) Delay vs length of a single CNT interconnect. The ITRS prediction has been marked. (b) Comparison of delay of 20 parallel CNT interconnects with copper interconnect having the same equivalent width (w=80nm) [Length is in m]