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# A Comparative Scaling Analysis of Metallic and Carbon Nanotube Interconnections for Nanometer Scale VLSI Technologies

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## Abstract

This paper addresses the critical issue of scaling limits of local interconnects, contact plugs and local vias made of metal. It is shown that the current carrying capacity of copper vias/contacts fails to meet ITRS current density requirements beyond the 45 nm technology node. Additionally, the electrical properties of local interconnects/vias made of carbon nanotube (CNT) arrays are analyzed in comparison with copper and process technology requirements are laid out that would make interconnects composed of CNT arrays a viable solution to meet the challenges of nanometer scale interconnects.

## Introduction

Interconnect parasitics leading to excessive delay and interconnect reliability issues are at the forefront of design challenges in the deep-submicron regime. The scaling of local wire dimensions closely follows device scaling in order to support the aggressive wiring requirements of increasingly densely packed devices [1]. In current and imminent technologies, the cross-sectional dimensions of these local wires are of the order of the mean free path of copper, which is about 40 nm at room temperature [2]. At such dimensions, the effect of scattering of current carrying electrons at the conductor surface as well as at the grain boundaries of the conducting material causes resistance of conductors to increase manifold [2]. In addition, the highly resistive diffusion barrier layer needed for copper interconnects occupies nearly 20% of drawn wire width at each technology node [1], thereby reducing the effective conducting area of these wires, which further increases their resistance. The increasingly high resistance thus seen on local interconnects raises concerns about their impact on performance and reliability of VLSI circuits.

Moreover, vertical metal links such as contacts and local vias that are pitch-matched to wire widths of the Metal1 layer have the smallest cross-sectional dimensions among all on-chip interconnects. As a result, the current density in local vias and contacts increases at a much faster rate than that for other interconnects (**Fig. 1**) as technology continues to scale beyond 90 nm. This makes metallic contacts and local vias most susceptible to electromigration and thermal failures. The number of contacts and vias that can be used is also constrained by routing area due to the via blockage effect [3]. Hence, efficient design of contacts and vias is pivotal to the robustness and reliability of nanometer scale integrated circuits.

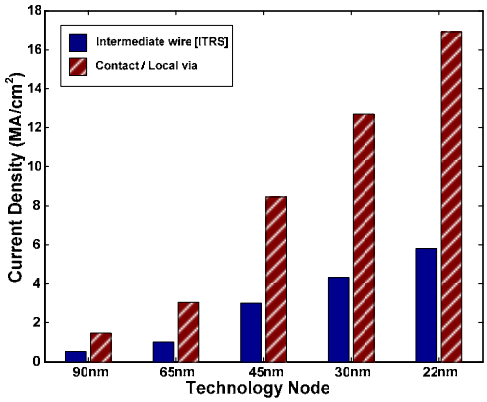


**Fig. 1.** Current density in intermediate level wiring as given by ITRS vs. current density calculated for contacts and local vias that are pitch matched to local wire widths, as technology scales. It is assumed that current flowing through intermediate wire flows through a single contact/via at the local level.

In this paper we first analyze the impact of small dimensions (and high resistance) of metallic local interconnects, contacts and vias on circuit performance and reliability. We find that the electrical limitations of metals, especially in contacts and local vias, are much more severe than has been shown in earlier works [4] and the limits of their current carrying capacities make them prohibitively expensive beyond the 45nm technology node.

Secondly, we evaluate carbon nanotubes (CNTs) as a possible replacement material for local interconnects, contacts and vias. Carbon nanotube arrays have recently been proposed as a possible replacement for metal interconnects [5, 6]. CNTs have very high current carrying capacity [7, 8] which makes them attractive candidates to solve the reliability/thermal problems posed by small dimension local interconnects and vias. However, there is no well-defined roadmap for the use of CNTs as interconnects, nor are there any guidelines for process designers about the requirements that will make this new technology a practical reality. This paper also examines the properties of interconnects/vias made of CNT arrays vis-a-vis Cu interconnects/vias and ascertains the requirements from process technology that would make the former a viable solution to meet future interconnect challenges.

## Resistivity Increase of Nanometer Scale Metal Interconnects

The resistivity of wires with dimensions in the range of or less than the mean free path of metal (Copper: 40 nm, Tungsten: 34 nm at room temperature) has been modeled and experimentally verified on sub-50 nm copper wires [2]. The Fuchs-Sondheimer model [2] provides an approximate resistivity formula for surface scattering in wires with circular or quadratic cross-sections (Eq. 1).

$$\frac{\rho}{\rho_0} = 1 + \frac{3}{4}(1-p)\frac{l}{d} \qquad (1)$$

Here $\rho_0$ is resistivity of the bulk material, $p$ is the fraction of electrons scattered specularly at the surface, $d$ is width of the wire and $l$ is mean free path.

The scattering of electrons at grain boundaries has been modeled by the theory of Mayadas and Shatzkes [9]. In this case the grain boundaries are treated as additional internal scattering surfaces. The resistivity from grain boundary scattering is given by Eqs. 2 and 3.

$$\frac{\rho_0}{\rho} = 3\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right] \qquad (2)$$

$$\alpha = \frac{l}{d}\frac{R}{1-R} \qquad (3)$$

Here $R$ is the reflectivity coefficient that denotes the fraction of electrons that are not scattered by the potential barrier at a grain boundary, and $d$ is the average distance between grain boundaries.

The combined effects of these phenomena, along with the presence of a finite diffusion barrier layer that reduces the effective copper conducting area, cause a sharp rise in the resistivity of interconnects when dimensions are of the order of the mean free path of electrons. **Fig. 2** shows the values of Cu resistivity at sub-90 nm technology nodes when these effects are taken into account. It can be observed that the resisitivity of Cu increases many times over its bulk value of 1.9 μΩ-cm.

## Scaling Limits of Metallic Local Interconnects, Contacts and Vias

For the scaling analysis, we consider a typical local interconnection wire in a cell-based layout with unit cell dimension 9λ, where λ is the technology-dependent layout parameter (half the minimum feature size). **Fig. 3** shows a typical NAND gate layout with pitch-matched contacts and vias in all local routes. In order to study the effect of via resistance on circuit performance, we consider a local interconnect of length 9λ between two logic gates across a unit cell. Based on Fig. 3, we can assume that the typical local interconnect traverses 2 contacts and 2 vias. It is noteworthy that the ITRS does not mention any scaling guidelines for local via heights. We have therefore assumed three scaling scenarios for contact and local via heights, as explained in **Fig. 4**.

**Fig. 4** and **Fig. 5** provide a comparison of the increasing resistance of local interconnections and that of just the vertical connections (contact plugs + vias) that form part of these interconnects, as technology scales. Evidently, the resistance of contacts and vias overwhelmingly dominates the local interconnect resistance in technologies beyond 50 nm. This is firstly because, although local interconnect length scales with technology as devices are packed closer together, the inter-metal-layer distance (which decides the conducting length of a via) does not scale as rapidly.

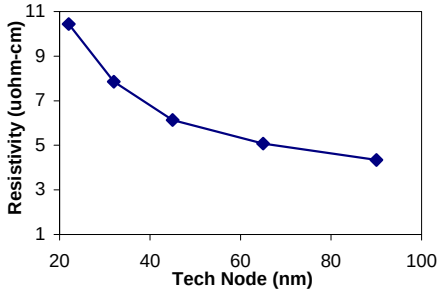


**Fig. 2.** Copper interconnection resistivity as a result of enhanced scattering and finite barrier layer at dimensions of the order of the mean free path of electrons (at Temp = 120°C).

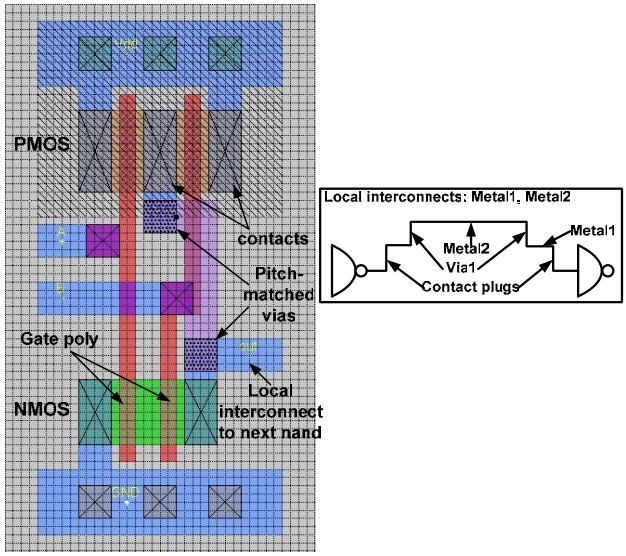


**Fig. 3.** NAND gate layout showing typical local interconnections. A minimum of 2 contacts and 2 local level vias occur on any local gate-to-gate interconnect route, as shown in the layout and schematic diagram.

Secondly, the local vias and contacts being pitch-matched to the first metal layer have much smaller cross-sectional area (and higher resistance) compared to the interconnects themselves. The use of Tungsten (W) as a contact plug metal leads to an even higher resistance (**Fig. 5b**). **Fig. 6** shows the impact of the substantial increase in local interconnect resistance on performance. Although the fractional delay suffered by local wires compared to nominal gate delay remains small, the fraction is shown to be increasing sharply. It must be noted that the inclusion of the interface

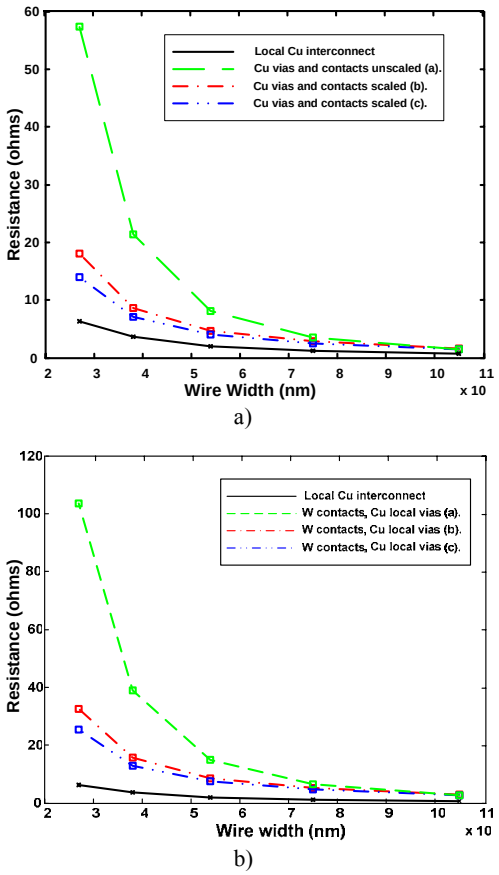


**Fig. 4.** Resistance of: **(a)** Cu contacts + Cu vias, **(b)** W contacts + Cu vias, versus that of a typical local interconnect, as technology scales. Local interconnect length assumed to be 9λ, with 2 contacts and 2 vias per interconnect as shown in Figure 3. **Contact and local via height scaling scenarios:** (a) height is constant, (b) aspect ratio is constant (height=1.4*width), (c) aspect ratio follows ITRS spec for intermediate level vias.

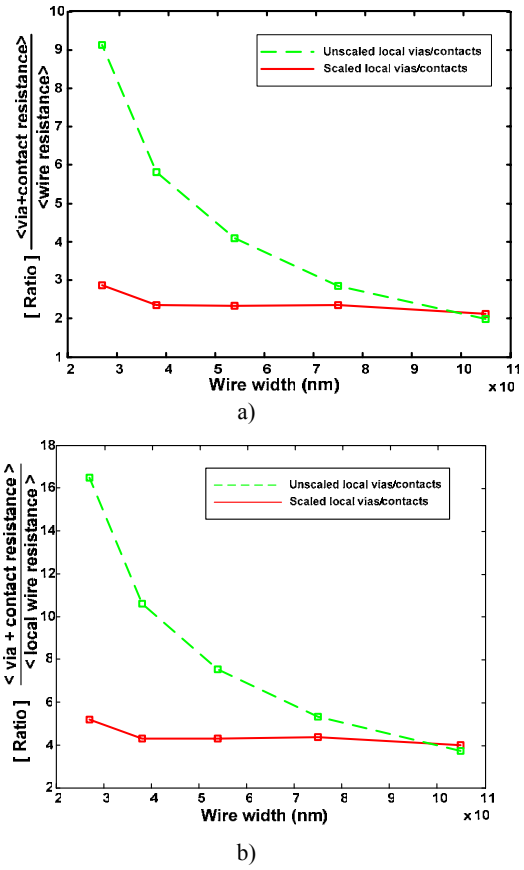


**Fig. 5.** Ratio of: **(a)** Cu via + Cu contact, **(b)** Cu via + W contact resistance to the resistance of a typical local interconnect, as technology scales. Local interconnect length assumed to be 9λ, with 2 contacts and 2 vias per interconnect as shown in Figure 3. Local vias/contacts are assumed to scale as per scenarios (a)-unscaled and (c)-scaled, which are described in Figure 4.

contact resistance would further increase the proportion of interconnect delay. However, for the purpose of this analysis we have focused on the contribution of metal resistances only.

**Fig. 7** and **Fig. 8** show the impact of high resistance in local vias on interconnect reliability based on the self-consistent methodology described in [10]. The self-consistent metal temperature (due to self-heating and electromigration) of copper vias is found to be substantially higher (Fig. 7) than that reported in earlier works [4, 10] mainly because of the inclusion of grain boundary scattering in the evaluation of effective resistivity of metal for very thin wires. Self-heating of the highly resistive local interconnects further exacerbates their reduced current carrying capacity due to small dimensions and electromigration/thermal constraints, making them more prone to electromigration/thermal failures. The maximum allowed RMS current density ($J_{rms}$) for a particular average current density ($J_{avg}$) increases as the duty ratio ($r$) decreases, as a direct effect of the relation:

$$J_{rms}{}^2 = \frac{J_{avg}{}^2}{r}$$

On the other hand, the larger self-heating at low duty ratios leads to a decrease in the maximum allowed RMS current density. The combined effect of these two competing factors is shown in the plot of Fig. 8. We observe that the maximum allowed RMS current density registers a drop at low duty ratios. This is because the large self-heating at low duty ratios limits the current carrying capacity significantly enough to offset the direct effect of a decrease in duty ratio. This phenomenon becomes evident because of the large resistance seen in these small dimension vias. As technology scales, the onset of this drop in maximum allowed current density occurs at increasingly higher duty ratios as the resistivity of the metallic vias becomes higher. In fact, the maximum allowed current density falls below the ITRS [1] projected requirements beyond the 45 nm node.

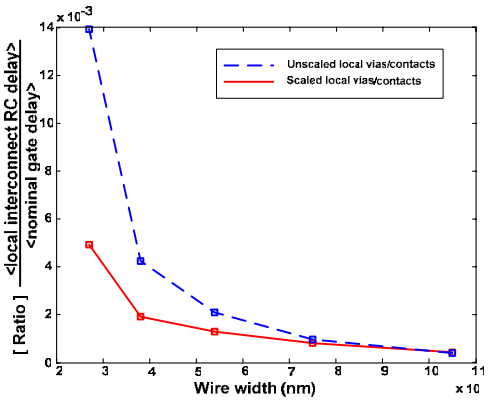


**Fig. 6.** Ratio of local interconnect RC delay (including W contacts + Cu local vias) to nominal gate delay as per ITRS, as technology scales. Vias/contacts are scaled as per scenarios (a)-unscaled and (c)-scaled which are described in Figure 4.

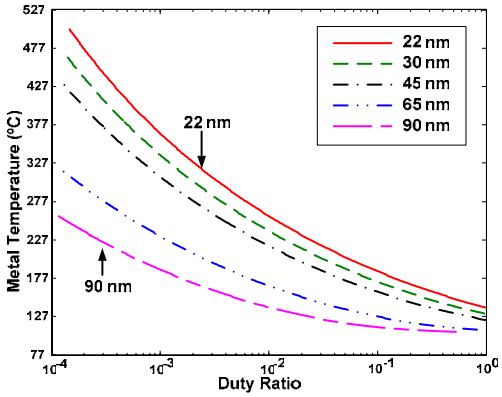


**Fig. 7.** Self-consistent metal temperature of local vias (due to self-heating and electromigration) for different duty ratios, as technology scales. Reference die temperature =105°C as per ITRS.

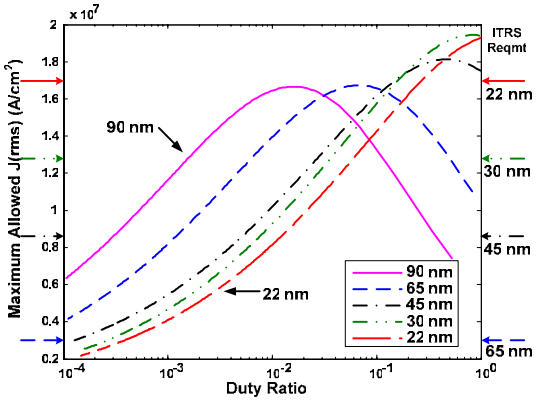


**Fig. 8.** Maximum allowed $J_{rms}$ for local vias under self-consistent joule heating and electromigration lifetime constraints evaluation at different technology (reference die Temp=105°C). The arrows on both sides of the axes show the design rule current densities required to support the ITRS specified intermediate wiring current. Electromigration/thermal constraints make the current density requirements unachievable beyond the 45 nm technology node.

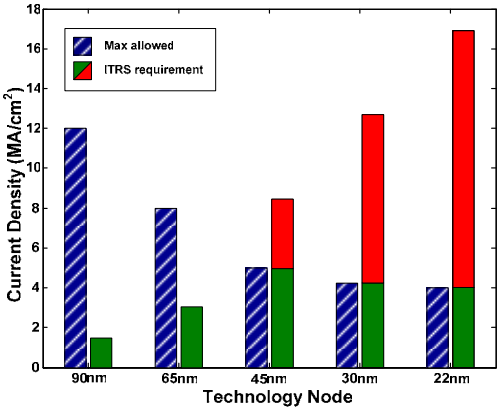


**Fig. 9.** Maximum allowed current density (duty ratio=0.001) in local vias from self-consistent electromigration lifetime estimation vs. the ITRS requirement for current density in local vias, as technology scales. The most optimistic scaling scenario for via height (case c), as described in Figure 4, is assumed.

**Table 1.** Number of vias needed to keep maximum allowed $J_{rms}$ (due to self-consistent joule heating and electromigration constraint evaluation) higher than design rule current specifications at different technology nodes for different ranges of duty ratios.

| Duty Ratio | Technology Node (nm) | | |
|---|---|---|---|
| | 45 nm | 30 nm | 22 nm |
| r >= 0.1 | 1 | 1 | 2 |
| r >= 0.01 | 2 | 2 | 3 |
| r >= 0.001 | 3 | 4 | 6 |

**Fig. 9** shows the deficit in the current carrying capacity of local vias, which grows to three times the maximum allowed current density at the 22 nm node. Often multiple vias are placed in parallel to reduce the electromigration and thermal stress on each via at the cost of routing congestion resulting from the via blockage effect [3]. **Table 1** gives a measure of the number of such parallel copper vias that will be needed to support the ITRS design rule current requirements. Evidently this cost becomes prohibitive for nanometer-scale circuits with high packing densities that are severely constrained for routing area.

## Carbon Nanotube Arrays in Interconnect Applications

Carbon nanotubes are known to exhibit extraordinary properties of high current carrying capacity, mechanical stability, and thermal conductivity (**Table 2**), because of which numerous applications, including interconnects, have been proposed for CNTs [5, 6]. The growth of an array of several CNTs forming parallel connections inside via holes, suitable for interconnect applications, has been recently demonstrated [5, 11, 12].

**Table 2.** Electrical and thermal properties of CNTs and Cu interconnects summarized. The current carrying capacity of single CNT is much larger than that of a Cu via.

| | Single CNT | Cu via 22 nm node |
|---|---|---|
| Resistance (ohms) | $6.5\text{x}10^3$ [13] | 4 |
| Max current density ($A/cm^2$) | ~$1\text{x}10^9$ [7, 8] | ~$1\text{x}10^7$ |
| Temp. coeff. of resistivity (/°C) | $-1.5\text{x}10^{-3}$ [15] | $+4\text{x}10^{-3}$ |
| Thermal conductivity (W/mK) | 6600 [17] | 400 |

To evaluate the conductance of a carbon nanotube, the two-terminal Landauer-Buttiker formula is used. This formula states that, for a 1-D system with $N$ channels in parallel, the conductance $G=(Ne^2/h)T$, where $T$ is the transmission coefficient for electrons through the sample [13]. In a carbon nanotube, due to spin degeneracy and sublattice degeneracy of electrons in graphene, each channel is fourfold degenerate ($N=4$). Hence the conductance of a single ballistic single-walled CNT (SWCNT) assuming perfect contacts ($T= 1$), is given by $4e^2/h$ = 155 μS, yielding a resistance of about 6.45 KΩ [13]. This is the fundamental resistance associated with a SWCNT that cannot be avoided [14]. Multi-wall CNTs (MWCNTs) have multiple 1-D conducting shells and their conductance will thus be higher depending on the number of conducting shells [5]. The second source of resistance for a CNT is the presence of scattering that yields a mean free path, typically 1 μm for a CNT [13]. For the CNT applications we consider here, local interconnect lengths (9λ), and via heights, are usually less than 1 μm, hence interconnect length or via height does not contribute any additional resistance for CNT arrays. Finally, imperfect metal-nanotube contacts will give rise to an additional contact resistance. Recent process solutions have been able to reduce metal-nanotube contact resistances below 1 KΩ [8] per CNT-metal contact. The total resistance of a CNT is then expressed as the sum of resistances arising from the above three aspects: the fundamental one-dimensional system (CNT) contact resistance, scattering resistance and the imperfect metal-nanotube contact resistance.

The winning aspect of CNTs in interconnect applications is their ability to sustain high current stress ~$1\text{x}10^9 A/cm^2$ (see Table 2) without the electromigration problems which plague Cu. However, it is important to note that although a single CNT is capable of carrying the maximum current flowing through a via (for < 45 nm nodes), the resistance of a single CNT is high (as discussed above). Interconnect resistance needs to be controlled due to performance and thermal concerns, hence the need for an *array of numerous CNTs in parallel*. It must also be ensured that the number of CNTs in an array is such that the current distribution does not exceed the range of a few micro-Amps per CNT as the resistance of CNTs increases substantially beyond this range [16].

In order to compare copper interconnects to those formed by CNT arrays, we assume a packed CNT array configuration, with 1 nm diameter SWCNTs, each occupying a square area of side 1 nm (as shown in inset of **Fig. 10**). This assumes process technology will be able to achieve packing densities of 1 CNT per nanometer-square area. It must be noted that for these densities of CNTs, the current through each CNT is much less than 1 μA and keeps the CNTs in a bias range where they exhibit excellent ohmic behavior [16].

**Fig. 10** compares the resistance of packed CNT array vias (assuming perfect contacts) to Cu vias for 45, 30 and 22 nm tech nodes. CNT arrays formed from 1nm diameter SWCNTs show an improved resistance compared to unscaled Cu vias, while those formed from MWCNTs show similar resistance values as the optimistically scaled Cu vias. **Fig. 11** compares the resistances of a typical local interconnect made of Cu to that made of a packed SWCNT array, as technology scales. In the case of imperfect metal-nanotube contacts we assume an additional contact resistance of 1KΩ per CNT contact. It is evident from Figs. 10 and 11 that with these high packing densities for CNT arrays their resistance is comparable to copper interconnects/vias while they have high current carrying capacities, thereby eliminating the major limitation of metallic interconnects.

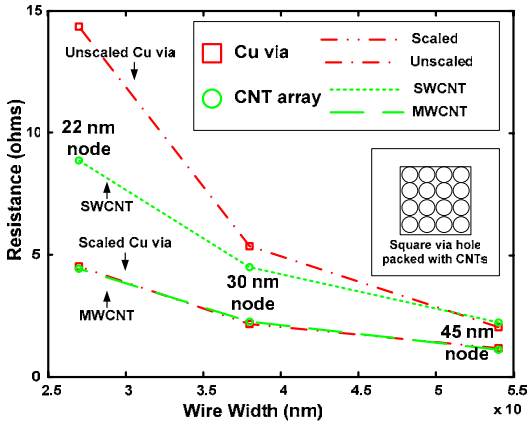


**Fig. 10.** Via resistance with Cu vias and CNT array vias, as technology scales. CNTs are assumed to be densely packed as shown in inset. Vias are scaled as per scenarios (a) and (c) which are described in Fig. 4.

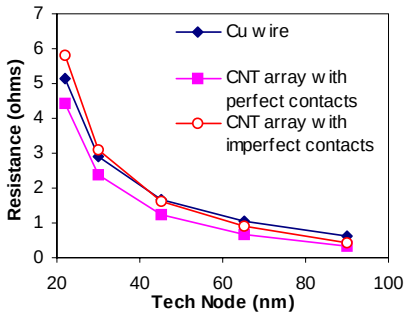


**Fig. 11.** Resistance of a typical local interconnect of Cu versus packed CNT array (see inset of Fig. 10) with perfect and imperfect metal-nanotube contacts. Interconnect length scaled as explained in Fig 4.

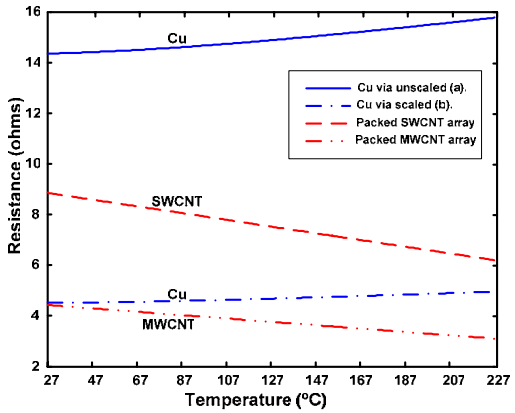


**Fig. 12.** Temperature dependent resistance of Cu via compared to a packed CNT array via (see inset of Fig 10) at the 22 nm technology node.

Another advantage of CNT vias is their negative temperature coefficient of resistance [15] that, as shown in **Fig. 12**, makes them more suitably disposed for the high temperature environment of local vias (Fig. 7). **Table 3** shows the progress of via resistance for CNT array vias for different packing densities of CNTs, and shows what densities will be needed as technology scales even beyond the ITRS roadmap. It is evident that process technology needs to achieve densities of the order of $10^6$ CNTs per square-micron (or 1 CNT per nm-square area) in order to keep the resistance of local vias and contacts under control. Published works today have demonstrated densities of less than 100 CNTs per square-micron [5, 12].

**Table 3.** Resistance (Ohms) of CNT array vias (using 1 nm diameter MWCNTs) for different densities of CNTs per square micron area as via dimensions scale with technology. Vias are assumed to be square. Last column shows resistance (Ohms) for Cu vias for the sake of comparison.

| Via size | Number of CNTs per square-micron area | | | | | Scaled Cu via |
|---|---|---|---|---|---|---|
| | $10^2$ /um-sq | $10^3$ /um-sq | $10^4$ /um-sq | $10^5$ /um-sq | $10^6$ /um-sq | |
| 54 nm | 3227 | 1075 | 107 | 11 | 1 | 1 |
| 38 nm | 3227 | 1613 | 215 | 22 | 2 | 2 |
| 27 nm | 3227 | 3227 | 403 | 44 | 4 | 4 |
| 20 nm | 3227 | 3227 | 645 | 78 | 8 | - |
| 15 nm | 3227 | 3227 | 1075 | 140 | 14 | - |
| 10 nm | 3227 | 3227 | 1613 | 293 | 31 | - |

## Conclusions

In the analysis presented in this paper it is shown for the first time that current carrying capacity arising from electromigration lifetime and thermal constraints, and not interconnect delay, will be the major limiting factor for nanometer dimension metallic local interconnects used in VLSI. More specifically, we show that metal contacts and local vias fail to meet the current density requirements of sub-45 nm technologies. It is also highlighted that carbon nanotube arrays are a possible alternative material for these local vias and contacts, given their high current carrying capacity and thermal conductivity. However, in order for them to be a viable alternative, process designers need to grow CNTs reliably with densities of about 1 per square-nm, a capability that has yet to be demonstrated.

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