NANO LETTERS

2003
Vol. 3, No. 4
443−445

Nanoimprint Lithography for Hybrid Plastic Electronics

Michael C. McAlpine,[†] Robin S. Friedman,[†] and Charles M. Lieber*[,†,‡]

Department of Chemistry and Chemical Biology, Harvard University, 12 Oxford Street, Cambridge, Massachusetts 02138, and Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts 02138

Received January 15, 2003

ABSTRACT

The merger of nanoscale devices with flexible, low cost plastics could enable a broad spectrum of electronic and photonic applications, although difficulties in processing plastics at the nanoscale have limited exploration of this potential. Here we describe the use of room temperature nanoimprint lithography for the general fabrication of nanometer- through millimeter-scale patterns on polymer substrates. Specifically, we demonstrate the patterning of arrays of nanoscale source–drain electrode pairs with continuous interconnects to the millimeter length scale, and the fabrication of hundred-nanometer gate features hierarchically patterned over large areas. These patterned plastic substrates have also been used in conjunction with semiconductor nanowires to assemble field-effect transistors.

Efficient fabrication of integrated circuits requires reliable, high-throughput processing to form device elements and interconnects. The most successful patterning technique used over the past several decades has been photolithography, although developments in this technique that have pushed feature resolution to the 100 nm range have come at the expense of increasingly complex and costly fabrication equipment.[1] To address these concerns, significant effort has been placed on developing alternative methods of nanoscale patterning, including electron-beam, scanning probe, extreme ultraviolet, dip-pen, and nanoimprint lithographies.[2−5] Nanoimprint lithography (NIL) is an especially interesting approach for nanoscale pattern generation since it is in principle scalable, parallel, and cost-effective.[5] NIL has been used most widely for creating features with a resolution of 100 nm,[6] although sub-25 nm features have also been reported.[5,7]

In NIL, a relief pattern is generated via compression molding of a deformable polymer by a hard inorganic stamp. This pattern is typically transferred to the underlying substrate by anisotropic reactive ion etching (RIE), followed by material deposition and liftoff of the remaining polymer. In general, polymers used for NIL must be heated above the glass transition temperature (ca. 200 °C) to enable flow during the imprinting step.[8] This heating process limits the application of NIL to flexible plastic substrates envisioned for a broad range of emerging applications, since many of these plastics deform at elevated temperatures. Interestingly, recent studies have reported room-temperature nanometer-scale imprinting of polymers on silicon substrates,[9,10] although the procedures were not elaborated by subsequent etching and deposition. Herein we describe reproducible NIL at room temperature on plastic substrates with hundred nanometer resolution metal electrode structures that are hierarchically patterned out to the millimeter scale. Our new results demonstrate that imprint lithography is capable of uniformly patterning flexible, polymeric surfaces in a single ambient temperature step with nanometer scale resolution. Furthermore, we show that the electrodes patterned by NIL can be naturally combined with inorganic semiconductor nanowires to generate nanoscale transistors, which offer the potential for single-crystal semiconductor device properties on flexible substrates.[11]

The overall scheme for our NIL process (Figure 1) highlights key features required for reliable nanoscale patterning.[12] First and central to our work is the deposition of a resist for room-temperature imprinting. We have found that lift-off resist (LOR 3A, MicroChem Corp.) functions as a good material since it can be (i) reproducibly imprinted at room temperature, (ii) removed cleanly from the inorganic stamp without antiadhesion agents,[13] and (iii) etched at controlled rates by RIE. LOR is deposited over a thin SiO_2 layer on the plastic substrate material; the SiO_2 is used to improve metal adhesion and was not found to affect flexibility. Second, the LOR is imprinted at room temperature using Si/SiO_2 stamps (400 μm/600 nm; Silicon Sense), where 100 nm scale oxide features were produced using standard electron beam lithography and deposition procedures.[14] In general, we find that these stamps can be reused tens of times without significant wear or loss of resolution. Finally, the

* Corresponding author. E-mail: cml@cmliris.harvard.edu
[†] Department of Chemistry and Chemical Biology.
[‡] Division of Engineering and Applied Sciences.

10.1021/nl034031e CCC: $25.00
Published on Web 03/07/2003

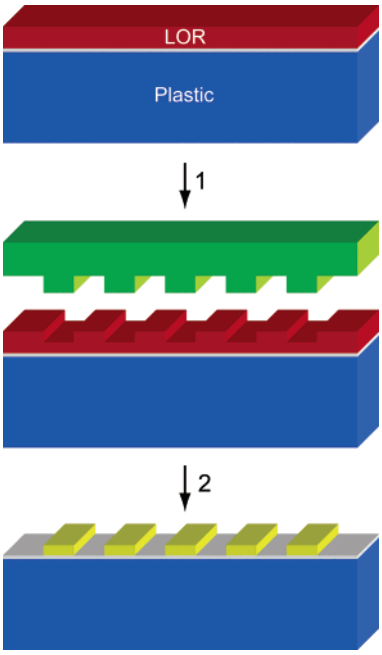

Figure 1. Schematic of the nanoimprint process on plastic substrates. Plastic substrates (blue) coated with SiO_2 (gray) and LOR (red) were imprinted (1) using a Si/SiO_2 stamp (green). The NIL pattern was transferred to the substrate in successive RIE, metal deposition, and lift-off steps (2).

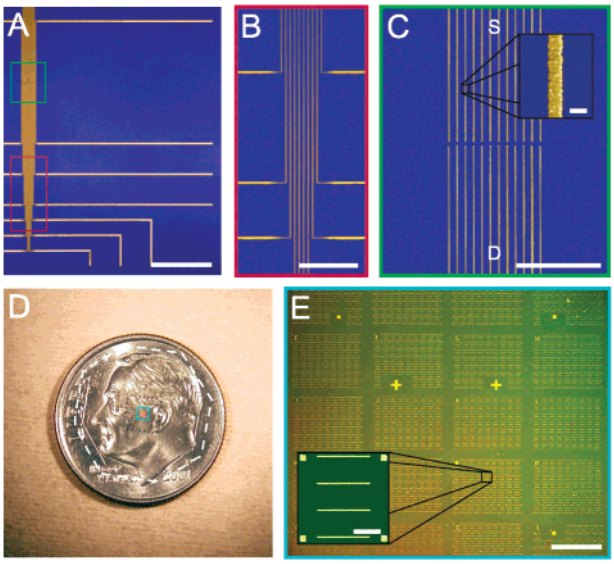

Figure 2. (A) Optical image of S−D array and interconnect wires; the scale bar is 100 μm. (B) Optical image of 200 nm S−D lines and 1 μm interconnect lines from an area highlighted by the red box in (A). Scale bar is 25 μm. (C) Field-emission scanning electron microscopy (SEM) image of S−D array; scale bar is 20 μm. (inset) SEM image of ca. 200 nm width channel lines; scale bar is 200 nm. (D) Optical image of patterned Mylar substrate with border outlined by the white dashed line and the patterned gate array highlighted by the central blue box. (E) Optical image of hierarchically patterned arrays of gate electrodes; the scale bar is 100 μm. (inset) SEM image of a gate array block, where corner squares are alignment marks. Scale bar is 5 μm.

imprinted LOR was etched to the SiO_2 layer using RIE, and metal electrodes were deposited by thermal evaporation.[12]

This general approach has been used to fabricate reproducibly nanometer scale metal features over large areas on plastic substrates (Figure 2). First, we have patterned arrays of split-electrode pairs that can function as source−drain (S−D) contacts with integrated interconnects for field-effect transistors (FETs). Figure 2A shows an array of S−D electrodes and interconnect wires extending over several hundred microns. The larger scale interconnects consist of 1 μm width features. Higher resolution imaging shows clearly two important features. First, the micron width interconnect lines transition smoothly to ca. 200 nm width S−D lines, even with right-angle turns used to route the lines from the array (Figure 2B). Second, the 200 nm width S−D electrode array is uniform with a 2 μm pitch and a 500 nm gap between each split electrode pair (Figure 2C). We believe that this straightforward and repeatable technique could be exploited to assemble parallel arrays of nanowire or carbon nanotube devices on flexible plastic or hard substrates by exploiting selective chemical modification[15] of the S−D electrode pairs and/or with electric fields.[16]

Room-temperature NIL has also been used to pattern arrays of single metal lines that could be used as gate electrodes in FETs or as floating gates in nonvolatile memory applications.[17] A low-resolution image of a patterned substrate superimposed on a coin (Figure 2D) highlights the transparent character of our plastic substrates and the fact that patterning is carried out over a sufficiently large area to be visible to the naked eye. Higher resolution images (Figure 2E) show clearly that NIL can readily yield ca. 300 nm width gate lines in highly regular 135 × 105 μm arrays that are tiled over the substrate to the millimeter scale. In addition, this image highlights micron-wide crosses and squares that were patterned simultaneously with the gate electrodes; these latter features can be used to enable subsequent lithographic alignment and device fabrication.

Significantly, these gate electrodes have been used to create silicon nanowire (SiNW) FETs on flexible plastic substrates (Figure 3) by combining bottom-up assembly with the top-down NIL approach. Specifically, a solution of p-type SiNWs were flow-aligned in a direction perpendicular to the gate electrode arrays, thereby producing a nanoscale FET at the cross point between a gate and SiNW (Figure 3A).[18−20] Figure 3B shows current versus S−D voltage ($I-V_{sd}$) data recorded on a typical crossed-junction SiNW FET. The $I-V_{sd}$ curves, which were recorded at different gate voltages (V_g), are very linear thus suggesting that the S−D contacts are ohmic. As V_g is increased, the slopes of the individual $I-V_{sd}$ curves decrease as expected for a p-type FET. Plots of the conductance versus V_g (Figure 3C) show that the transconductance of this device is ca. 750 nA V^{-1}. This value is within a factor of 2 of that recently reported for core/shell nanowire devices that were fabricated on conventional single-crystal Si/SiO_2 substrates.[21] It should be noted that this is not an optimized structure and the device performance could be improved by, for example, decreasing the dopant concentration and/or minimizing trap states in the dielectric.[22]

In summary, we have demonstrated NIL of nanometer through millimeter-scale features on flexible plastic substrates over large areas at room temperature. The ambient temper-

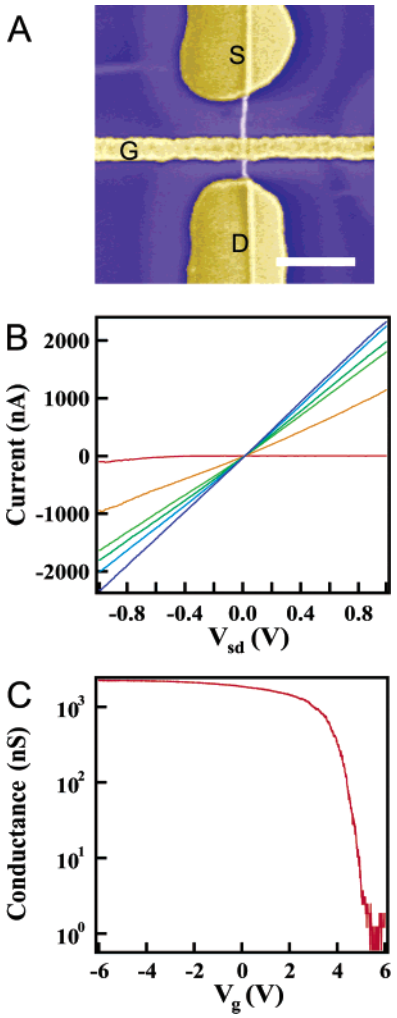

Figure 3. (A) SEM image of a 20 nm p-SiNW (vertical) crossing an imprint-patterned metal gate (G) electrode; scale bar is 1 μm. (B) Gate-dependent $I-V_{sd}$ curves recorded on a 20 nm p-SiNW. The V_g were -3, -1, 0, 1, 3, and 5 V, when read from top to bottom at positive V_{sd}. (C) Plot of $I-V_g$ from the data in (B) for $V_{sd} = 1$ V.

ature NIL patterning technique has been shown to produce uniform features in a parallel and repeatable manner and, moreover, has been combined with bottom up assembly to fabricate SiNW FETs on flexible plastic substrates with device performances similar to nanowire FETs fabricated on conventional single-crystal substrates. We believe that our development of simple and reproducible high-resolution patterning of plastics using NIL combined with the versatile function of nanowire building blocks[23] could open up exciting opportunities over many length scales for plastic electronics and photonics.

Acknowledgment. We thank Y. Cui for useful discussions and SiNWs. M.C.M. thanks the NSF for predoctoral fellowship support. C.M.L. acknowledges support of this work by the Defense Advanced Projects Research Agency.

Note Added after ASAP. This paper was originially posted 3/7/2003. Figure 3 was revised with corrected axis labels in part C. The revised paper was reposted on the Web on 3/18/2003.

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NL034031E