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Single-crystal metallic nanowires and metal/semiconductor nanowire heterostructures

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Substantial effort has been placed on developing semiconducting carbon nanotubes[1–3] and nanowires[4] as building blocks for electronic devices—such as field-effect transistors—that could replace conventional silicon transistors in hybrid electronics or lead to stand-alone nanosystems[4,5]. Attaching electric contacts to individual devices is a first step towards integration, and this step has been addressed using lithographically defined metal electrodes[1–4,6–8]. Yet, these metal contacts define a size scale that is much larger than the nanometre-scale building blocks, thus limiting many potential advantages. Here we report an integrated contact and interconnection solution that overcomes this size constraint through selective transformation of silicon nanowires into metallic nickel silicide (NiSi) nanowires. Electrical measurements show that the single crystal nickel silicide nanowires have ideal resistivities of about 10 $\mu\Omega$ cm and remarkably high failure-current densities, $>10^8$ A cm^{-2}. In addition, we demonstrate the fabrication of nickel silicide/silicon (NiSi/Si) nanowire heterostructures with atomically sharp metal–semiconductor interfaces. We produce field-effect transistors based on those heterostructures in which the source–drain contacts are defined by the metallic NiSi nanowire regions. Our approach is fully compatible with conventional planar silicon electronics and extendable to the 10-nm scale using a crossed-nanowire architecture.

Our focus on NiSi nanowires is motivated by previous investigations of metal silicides, which can exhibit low resistivity, compatibility with conventional silicon manufacturing, and the ability to form ohmic contacts to both p- and n-type silicon[9]. We prepared NiSi nanowires using an approach (Fig. 1a) involving deposition of nickel metal onto single-crystal Si nanowires[10,11], solid-state reaction at 550 °C to form NiSi, followed by removal of remaining metal by wet etching (see Methods). Low-resolution transmission electron microscopy (TEM) studies (Fig. 1b) of materials prepared in this

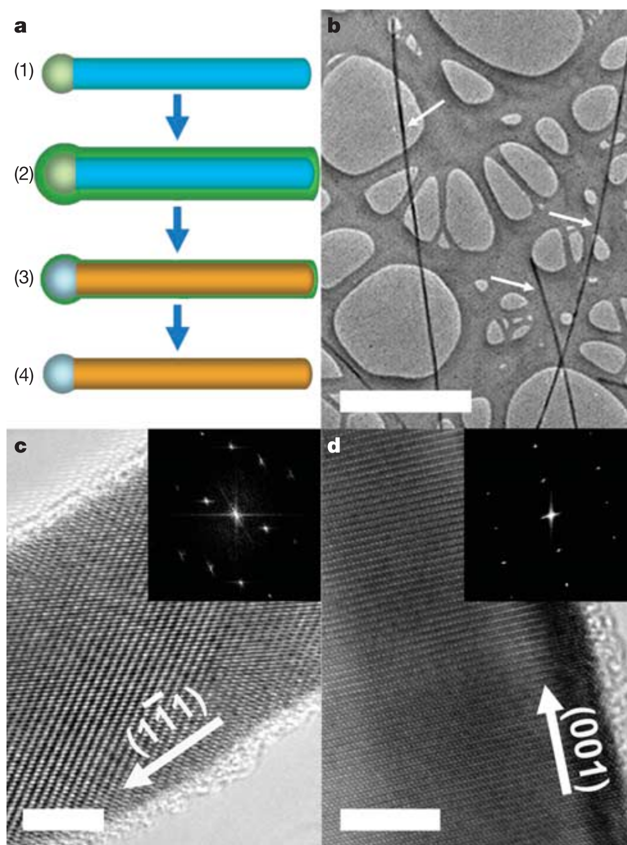

Figure 1 Preparation and structural characterization of single-crystal NiSi nanowires. **a**, Preparation of single-crystal NiSi nanowires. (1) Si nanowires (blue) of uniform diameter are (2) coated with Ni metal (green) to a total thickness comparable to the Si nanowire diameter, (3) reacted at 550 °C to form NiSi nanowires (brown), and then (4) etched to remove any excess Ni metal. **b**, TEM image of three NiSi nanowires prepared using Si nanowires with an average diameter of about 20 nm. The NiSi nanowires are highlighted by white arrows; scale bar is 1 μm. **c** and **d**, High-resolution TEM images of single-crystal NiSi nanowires. **c**, TEM image of a 20-nm NiSi nanowire prepared using Si nanowires of average diameter 20 nm. The white arrow indicates the growth front of the nanowire. Inset, two-dimensional Fourier transform of the image showing the $[10\bar{1}]$ zone axis of NiSi. **d**, Image of a 32-nm NiSi nanowire prepared using Si nanowires of average diameter 30 nm. The white arrow indicates the growth front of the nanowire. Inset, two-dimensional Fourier transform of the image depicting the $[2\bar{1}0]$ zone axis of NiSi. The scale bars in **c** and **d** are 5 nm.

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way show nanowires that have uniform diameters and contrast, which are properties indicative of single-crystal structures, and lengths of tens of micrometres. Analysis of samples prepared from Si nanowires with diameters of 20.3 ± 2.3 nm yielded materials with diameters of 22.8 ± 3.4 nm. The increase in average diameter agrees with the value of 22.4 nm, expected for conversion of Si to NiSi on the basis of different unit-cell volumes[12]. In addition, energy dispersive X-ray spectroscopy (EDS) measurements show that the Ni:Si atom ratio in the nanowires is 1.03:1, as expected for NiSi.

High-resolution TEM studies (Figs 1c and d) demonstrate clearly that the nanowires are single-crystal NiSi. The reciprocal lattice peaks, which were obtained from two-dimensional Fourier transforms (2DFT) of the lattice-resolved images (insets to Figs 1c and d) can be indexed to the orthorhombic structure of NiSi[12] with the zone axes along the $[10\bar{1}]$ and $[2\bar{1}0]$ directions, respectively. This analysis enables assignment of the growth front of NiSi to be the $(1\bar{1}1)$ and (001) planes for the 20- and 30-nm-diameter nanowires in Figs 1c and d, respectively. The different NiSi nanowire growth directions may be explained by different growth directions of the starting silicon nanowires[11], although future work will be required to quantify this relationship. These high-resolution data also show that the NiSi nanowires have smooth surfaces with very little (<1 nm) amorphous coating. Taken together, these results demonstrate that our approach yields uniform conversion of single-crystal Si nanowires to single-crystal NiSi nanowires. Lastly, similar studies with germanium (Ge) nanowires show that metallic single-crystal NiGe nanowires can also be prepared by our approach (Y.W., J.X. & C.M.L., unpublished results).

Representative electrical transport data recorded on a 29-nm-diameter NiSi nanowire (Fig. 2a) show linear current (I) versus voltage (V) behaviour with two- and four-terminal resistances of 886 and 184 Ω, respectively. The current levels observed from 30-nm NiSi nanowires typically exceed 100 μA at 100 mV bias, are quite remarkable in comparison to the starting Si nanowires, and are clearly indicative of the expected metallic nature of NiSi. Indeed, calculation of the resistivity on the basis of the four-terminal data yields a value of 9.5 μΩ cm, close to the value of 10 μΩ cm for NiSi single crystals[13]. These low-resistivity values have been observed for NiSi nanowires with diameters from about 15 to 45 nm, and thus demonstrate that these single-crystal wires can be scaled to ultrasmall dimensions without degradation of properties. Temperature-dependent measurements (inset to Fig. 2a) further show that the nanowire resistance decreases monotonically down to about 30 K and then saturates as expected for a metal. The similarity of NiSi nanowire resistivities to the bulk value, the temperature dependence of the resistance, and the scaling of resistance with length (to 6 μm) are indicative of diffusive transport. Using a previously reported carrier density value for NiSi[13] we estimate the scattering mean free path to be of the order of 5 nm. Hence, it should be possible to retain the attractive metallic transport in NiSi nanowires down to the sub-10-nm-diameter scale, and also to study the effects of fundamental properties, such as dephasing, in a pure metal regime that should be accessible from recently reported molecular-scale silicon nanowires[11] using our synthetic approach.

We have also characterized the maximum transport current for the metallic NiSi nanowires. For example, the 29-nm-diameter nanowire discussed above could carry a current of 1.84 mA before failure (Fig. 2b). Notably, this yields a maximum current density, J_{max}, of 3×10^8 A cm^{-2}. This large value of J_{max} is reproducible, and is approximately independent of nanowire diameter. For example, a nanowire of diameter 40–45 nm exhibited a failure current of 5.5 mA, and $J_{max} > 3 \times 10^8$ A cm^{-2}. In general, failure occurs in the middle of the nanowires, which is where the peak temperature is expected to occur, owing to dissipative self-heating; this suggests the breakdown mechanism is due to melting. The high J_{max} values can be attributed to the single-crystal structures, which preclude energy dissipation and void diffusion[14] at the grain boundary and defect sites that are common in lithographically defined wires.

The J_{max} for the NiSi nanowires is comparable to the best values—10^9 A cm^{-2}— reported for single-walled carbon nanotubes[15]. We believe this finding is important because the high J_{max} values are achieved in essentially every NiSi nanowire, without the need to find and connect the metallic versus semiconducting carbon nanotubes. In addition, the maximum current can be scaled through the growth of specific-diameter NiSi nanowires. The J_{max} for the NiSi nanowires is also about two orders of magnitude larger than that observed in lithographically defined noble metal lines[16]. This suggests an immediate advantage of NiSi nanowires over lithographically defined nanoscale metal lines: for example, they could be used as local- and intermediate-level interconnects to nanowire field-effect transistors that might be key components in hybrid nanoelectronics.

Importantly, the approach outlined above can also be used to transform selectively single-crystal silicon nanowires to produce NiSi/Si heterostructures and superlattices. To demonstrate this

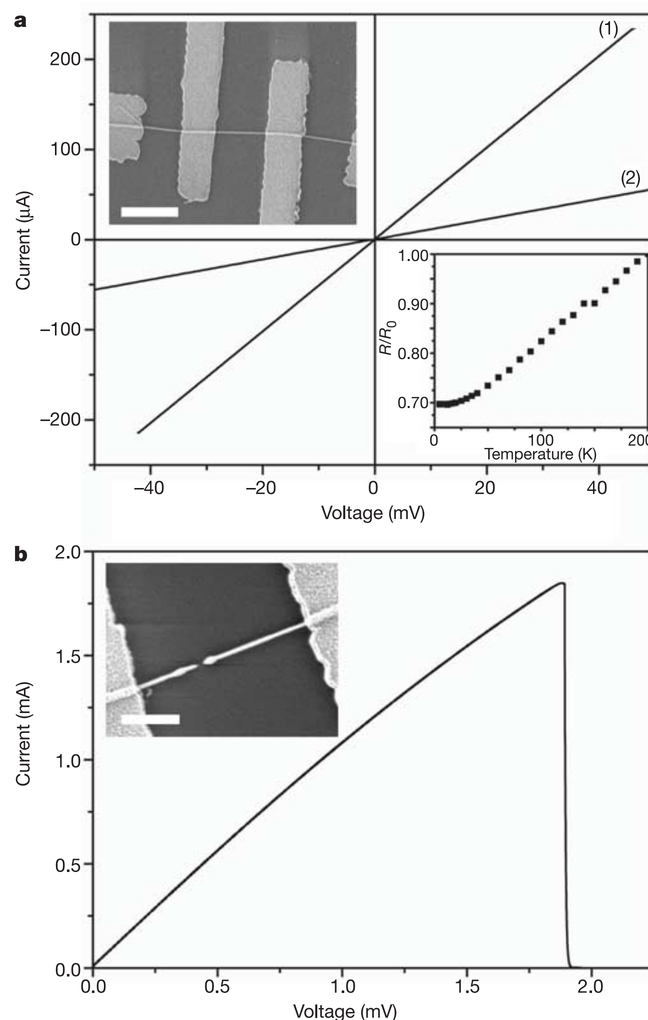

Figure 2 Transport measurements on individual single-crystal NiSi nanowires. **a**, Current versus voltage curves recorded on a 29-nm NiSi nanowire, with line (1) and line (2) corresponding to four- and two-terminal measurements, respectively, taken from the device shown in the SEM image (inset, upper left). The scale bar in the image is 1 μm. Lower inset, temperature-dependent normalized resistance obtained from a four-terminal device; the resistance, R, is normalized by the value at 200 K, R_0. **b**, I–V data recorded at large applied voltages. The rapid drop at about 1.8 V corresponds to the failure point of this nanowire. Inset, SEM image of the nanowire after breakdown. The image highlights the break close to the middle of the nanowires. Scale bar, 500 nm.

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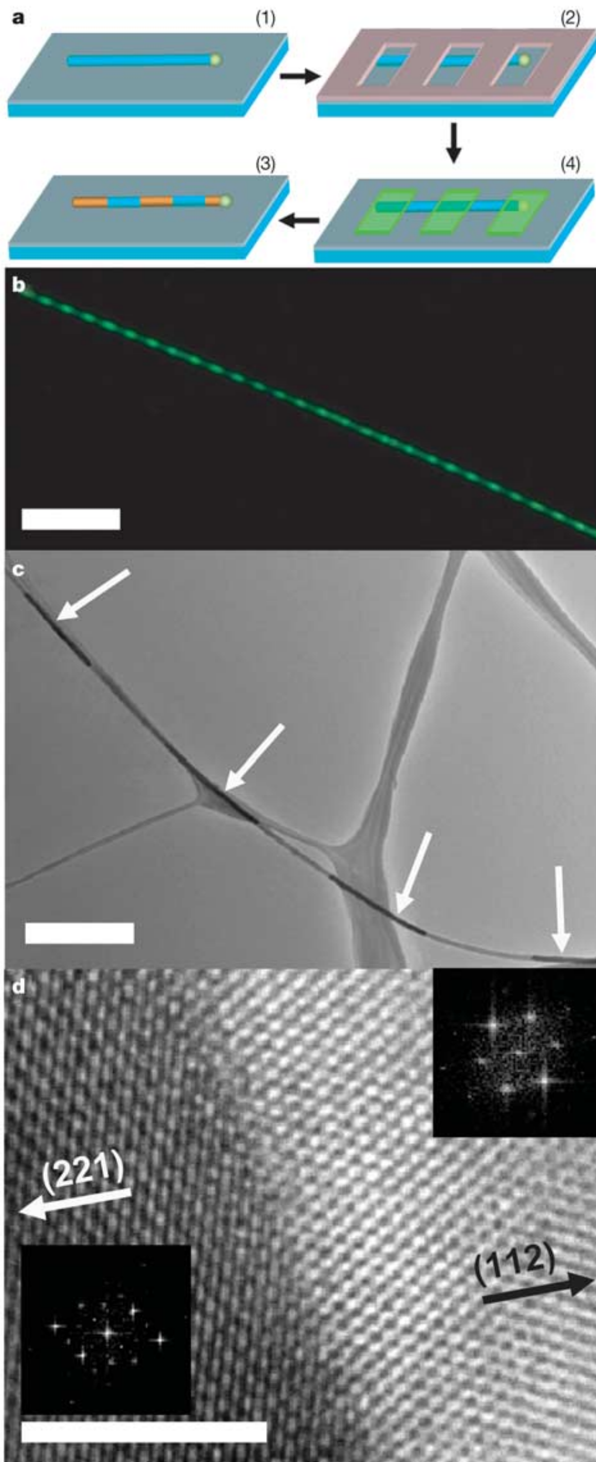
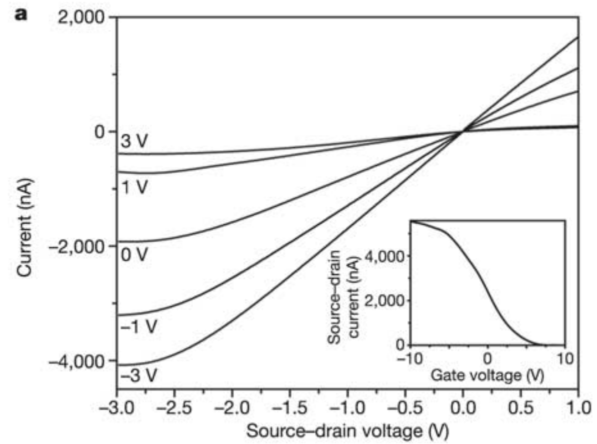


Figure 3 Fabrication and structural characterizations of NiSi/Si nanowire heterostructures and superlattices. **a**, Fabrication of NiSi/Si nanowire heterostructures and superlattices. (1) Si nanowires (blue) dispersed on a substrate are (2) coated with photoresist (grey) and lithographically patterned, (3) selectively coated with Ni metal (green) to a total thickness comparable to the Si nanowire diameter, and (4) reacted at 550 °C to form NiSi nanowires. **b**, Dark-field optical image of a single NiSi/Si nanowire heterostructure. The bright green segments correspond to silicon and the dark segments to NiSi. Scale bar is 10 μm. **c**, TEM image of a NiSi/Si heterostructured nanowire. The bright segments of the nanowire correspond to silicon and the dark segments, which are highlighted with arrows, correspond to NiSi. Scale bar is 1 μm. **d**, High-resolution TEM image of the junction between NiSi and Si showing an atomically abrupt interface. Insets, two-dimensional Fourier transforms of the image depicting the [110] and [111] zone axes of NiSi and Si, respectively, where the arrows highlight the growth fronts of the NiSi (221) and Si (112). Scale bar is 5 nm.

concept (Fig. 3a) we patterned nickel metal onto silicon nanowires and then transform the nickel-containing regions to NiSi (see Methods). A dark-field optical image of a nanowire patterned in this way using 1-μm-wide nickel regions on a 2-μm pitch (Fig. 3b) exhibits periodic variations in contrast extending over the full length of the 65-μm-long nanowire. Analysis of the image shows



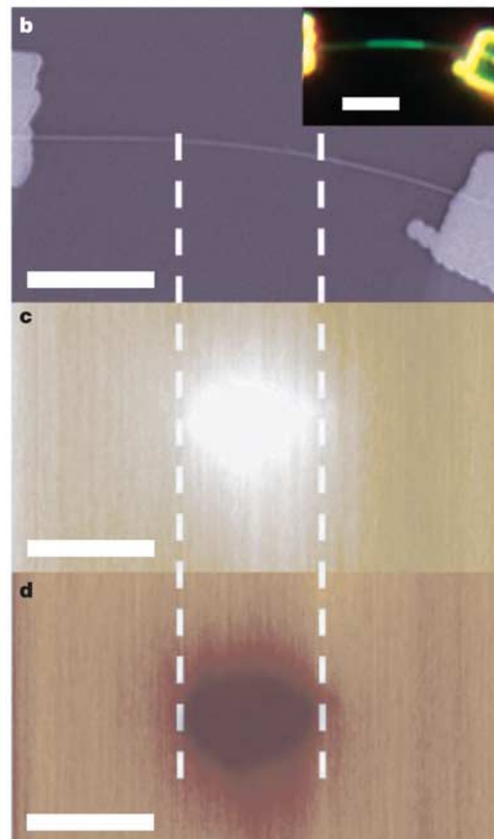


Figure 4 Transport properties of a NiSi/p-Si/NiSi heterojunction field-effect transistor. **a**, I versus V_{sd}, exhibiting the typical characteristics of a NiSi/p-Si/NiSi heterojunction transistor. Inset, gate sweep obtained from the same device in the saturation regime with $V_{sd} = -3$ V. The device was fabricated using a 30-nm diameter p-Si nanowire (dopant density $= \sim 1 \times 10^{18}\,cm^{-3}$) on a heavily doped silicon substrate with 600 nm of thermal oxide; the channel length is 3 μm. **b**, SEM image of a field-effect transistor device fabricated using a NiSi/p-Si/NiSi nanowire heterojunction. Inset, dark-field optical image of the same device, where the bright green segment corresponds to silicon and the dark segments to NiSi. Scale bars, 3 μm. **c** and **d,** SGM images show reduced conductance with +9 V (Fig. 4c) and enhanced conductance with −9 V gate voltage (Fig. 4d) on the atomic force microscope tip. The dotted lines mark the interface between the NiSi and p-Si regions. Scale bars, 3 μm.

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that the average lengths of the Si and NiSi regions are both 1 μm, and in good agreement with the width and pitch of nickel metal deposited on the nanowire during fabrication.

TEM images of similar NiSi/Si nanowire heterostructures (Fig. 3c) show a similar periodic variation in contrast that is consistent with NiSi (dark) and Si (light) materials within the heterostructure. This assignment was confirmed by EDS analysis: the dark and light regions corresponded to an Ni:Si ratio of 1.02:1.00 and pure Si, respectively. Analysis of the images also shows that the average lengths of the Si and NiSi regions are 0.93 ± 0.10 and 1.03 ± 0.11 μm, respectively. The good agreement with the expected pattern demonstrates clearly that our approach enables spatially controlled transformation of silicon to metallic NiSi nanowire heterostructures. Notably, detailed examination of NiSi/Si heterostructure by high-resolution TEM (Fig. 3d) shows that the transformation yields an atomically abrupt interface (irrespective of any axial diffusion). The reciprocal lattice peaks, which were obtained from two-dimensional Fourier transforms of the lattice-resolved image (insets to Fig. 3d) correspond to the [110] and [111] zone axes of NiSi and Si, with (221) and (112) nanowire growth fronts, respectively.

The atomically sharp metal–semiconductor interfaces produced in these nanowire heterostructures have the potential to yield a range of precisely defined electronic devices and device arrays on individual nanowires. To explore this opportunity we have prepared field-effect transistor (FET) devices in which the critical source–drain regions are defined by metallic NiSi nanowire sections on p-type Si nanowire. Current versus source–drain voltage (V_{sd}) data (Fig. 4a) are linear to $|V_{sd}| \leq 1$ V, which suggests that the NiSi/Si contacts behave for practical purposes as ohmic contacts at room temperature, although preliminary temperature-dependent measurements show a barrier at low temperature. The room-temperature behaviour can be explained by the reported segregation of dopant to the NiSi/Si interface during NiSi formation[9], although other factors may also contribute to the ohmic response at room temperature. Notably, I–V_{sd} data recorded at different back gate voltages (V_g) exhibit the behaviour expected[17] of a depletion mode p-FET with a high hole mobility of 325 cm^2 V s (see Methods).

To demonstrate that the active channel of this device was defined by the separation between NiSi nanowire regions, and not the much larger lithographically defined metal contacts, we carried out scanning gate microscopy (SGM) measurements. SGM images recorded with the scanning gate voltages of −9 V (Fig. 4c) and +9 V (Fig. 4d) respectively show enhanced (accumulation) and reduced (depletion) conductance only in the silicon region over the overall device (Fig. 4b). These data thus confirm that our approach yields spatially and electronically well-defined metal–semiconductor devices.

Lastly, we have investigated scaling of our approach by assembling[18] crossed-nanowire arrays in which the crossed nanowires function as masks defining active channels in NiSi/Si/NiSi heterostructures (see Methods) and could also function as local gates (Fig. 5a). TEM images recorded on a device following removal of the crossed-nanowire mask (Fig. 5b) show a well-defined silicon channel of 20 nm in this 10-nm-diameter NiSi/Si/NiSi heterostructure. This channel length is comparable to the best that can be achieved in state-of-the-art planar devices[19]. The TEM results indicate lateral diffusion of several nanometres during the formation of NiSi, and suggest that it should be possible to prepare shorter channel devices in a well-defined manner simply by varying the diameter of the nanowire mask. More generally, the capability of transforming Si to NiSi in a spatially well-defined manner to form NiSi/Si nanowire heterostructures and superlattices with atomically sharp metal–semiconductor interfaces opens up the possibility of integrating both active devices and high-performance interconnects from a single nanoscale building block. By extending our approach to crossed nanowires as shown above it should become possible to assemble large and dense arrays, perhaps using Langmuir–Blodgett assembly techniques[20], of transistors and other devices that could enable hybrid integrated circuits and could represent a key step towards stand-alone integrated nanosystems. □

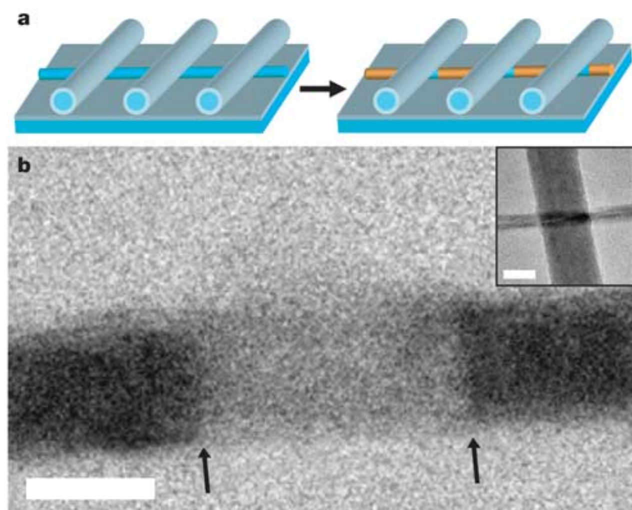

Figure 5 Self-aligned nanoscale NiSi/Si/NiSi devices. **a**, Schematic illustrating Si nanowire (blue) crossed with three Si/SiO_2 core (blue)–shell (grey) nanowires[21]. Deposition, annealing and removal of excess Ni yields NiSi (brown) regions separated by Si in the nanowire. **b**, TEM image of the NiSi/Si/NiSi nanowire heterostructure. The dark regions correspond to NiSi and the light region to Si with NiSi/Si interfaces highlighted by black arrows. Scale bar is 10 nm. Inset, TEM image of the same nanowire before silicidation. The crossed Si/SiO_2 core–shell nanowire (approximately vertical in image) was used as a mask to define the Si region and removed after silicidation. Scale bar is 20 nm. The sample was prepared and imaged on a 50-nm-thick Si_3N_4 membrane.

Methods

Preparation of single-crystal metallic NiSi nanowires

Si nanowires were synthesized via chemical vapour deposition using monodisperse gold nanoclusters (Ted Pella) as catalysts, silane (SiH_4) as the vapour-phase reactant, diborane as the dopant and hydrogen as the carrier gas[10,11]. The silicon nanowires produced in this manner have clean surfaces with no visible amorphous oxide[11]. Immediately following synthesis, the growth substrate with uniform diameter, free-standing Si nanowires was loaded into a metal deposition system, and then Ni metal was deposited to a thickness comparable to the average Si nanowire diameter. NiSi nanowires were produced by annealing the Ni-metal-coated Si nanowires at 550 °C. Excess Ni was completely removed by etching (TFG, Transene) for one hour at 50 °C, followed by post-annealing at 600 °C. Each of the annealing steps was carried out in forming gas (N_2:H_2 ratio, 90:10) for 5 min in a rapid thermal annealer (Heatpulse 610, Metron Technology).

Preparation of NiSi/Si nanowire heterostructures

Si nanowires dispersed in ethanol were deposited on a Si wafer with 600 nm of thermal oxide, and then the substrate was coated with photoresist (Shipley 1813, Rohm and Haas Electronics Materials). The photoresist was exposed for about 2 s on an ABM photoaligner using a simple striped pattern with a 2-μm pitch: 1 μm linewidth and 1 μm spacing. After developing for 1 min, the wafer was transferred to a thermal evaporator and Ni was evaporated with a thickness equal to the average nanowire diameter. After lift-off, the samples were annealed and etched as described above. Ultrasmall NiSi/Si/NiSi nanowire heterostructures were fabricated using crossed Si/SiO_2 core-shell nanowires[21] as masks to define the lengths of the unreacted Si regions. The crossed-nanowire structures were assembled on Si_3N_4 membrane window grids (Structure Probe) by fluidic assembly[18], and then Ni was evaporated and annealed as described above. The Si/SiO_2 core–shell nanowires were removed with hydrogen fluoride solution (Transene) to enable direct TEM imaging of the NiSi/Si/NiSi heterostructure on the Si_3N_4 membranes.

Calculation of device characteristics

The hole mobility, μ, is computed using a standard model[17]. In the small bias linear transport region, the mobility is expressed in terms of the transconductance, g_m, as $g_m = \mu C V_{sd}/L^2$, where V_{sd} is the source–drain voltage, L is the device channel length, and C is the gate capacitance, which was estimated using $C = 2\pi\epsilon\epsilon_0 L/\ln(2t_{ox}/r)$ (where ϵ is the effective dielectric constant, t_{ox} is the SiO_2 dielectric thickness, and r is the nanowire radius). For the device in Fig. 3a, g_m was evaluated for V_g from −3 to + 3 V at $V_{sd} = -1$ V, and has a value of 275 nS.

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Evidence for deep-water production in the North Pacific Ocean during the early Cenozoic warm interval

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The deep-ocean circulation is responsible for a significant component of global heat transport. In the present mode of circulation, deep waters form in the North Atlantic and Southern oceans where surface water becomes sufficiently cold and dense to sink. Polar temperatures during the warmest climatic interval of the Cenozoic era (∼65 to 40 million years (Myr) ago) were significantly warmer than today, and this may have been a consequence of enhanced oceanic heat transport[1]. However, understanding the relationship between deep-ocean circulation and ancient climate is complicated by differences in oceanic gateways[2], which affect where deep waters form and how they circulate. Here I report records of neodymium isotopes from two cores in the Pacific Ocean that indicate a shift in deep-water production from the Southern Ocean to the North Pacific ∼65 Myr ago. The source of deep waters reverted back to the Southern Ocean 40 Myr ago. The relative timing of changes in the neodymium and oxygen isotope records indicates that changes in Cenozoic deep-water circulation patterns were the consequence, not the cause, of extreme Cenozoic warmth.

Slow deep-water renewal in the modern North Pacific is a consequence of climatic and tectonic factors. Relatively high precipitation in the North Pacific[3] results in sea-surface salinities too low to enable downwelling (∼33 parts per thousand (p.p.t.) as compared to ∼35 p.p.t. in the North Atlantic[3]). Further, the Bering Strait sill does not permit dense, cold Arctic bottom waters to enter the North Pacific[4]. In addition, most of the bottom waters formed in the Ross Sea (the Pacific sector of the Southern Ocean) are prevented from flowing northward into the Pacific basin by the eastward flow of the Antarctic circumpolar current and the mid-ocean ridge[4].

However, a different set of climatic and tectonic boundary conditions prevailed during the early Cenozoic interval of extreme warmth, about 65–40 Myr ago. Global deep-water temperatures were about 8–12 °C (ref. 5), too warm for permanent polar ice to exist. The configuration of continents and ocean basins was also different from the present (Fig. 1). The Tasman Sea and Drake Passage had not yet opened, and Tethyan and Caribbean seaways still existed[2]. In addition, the Norwegian and Greenland seas began forming ∼55 Myr ago[6], so North Atlantic deep waters would not have existed during this time interval.

Such different thermal and palaeogeographic regimes should have affected deep-sea circulation patterns, and conversely, a different mode of thermohaline circulation may have influenced the evolution of global climate. To investigate the relationship between early Cenozoic climate and thermohaline circulation patterns, I generated records of the neodymium isotopic composition of fossil fish debris from Ocean Drilling Program (ODP) Sites 1209 and 1211 (Shatsky rise, in the present-day northwestern Pacific).

Neodymium isotopic ratios (^{143}Nd/^{144}Nd, expressed as ϵ_{Nd}; ref. 7) track deep-water mass circulation because Nd has a short oceanic residence time (∼1,000 yr; ref. 8) relative to oceanic mixing (∼1,500 yr; ref. 9). The ϵ_{Nd} composition of individual deep-water masses is derived from the composition of Nd discharging into the source regions of the water masses[10–12]. South Pacific surface

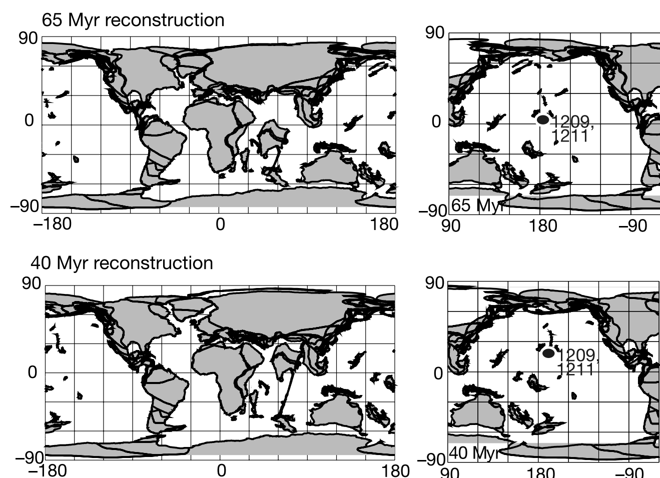

Figure 1 Palaeogeographic reconstructions during two intervals of the early Cenozoic. The location of Ocean Drilling Program (ODP) Sites 1209 and 1211 are shown for 65 Myr ago (top panels) and 40 Myr ago (bottom panels). Note that the location of Sites 1209 and 1211 did not change significantly over the time interval investigated. Reconstructions created by the Ocean Drilling Stratigraphic Network (www.odsn.de).

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