Adoption of OPC and the Impact on Design and Layout

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ABSTRACT
With the adoption of various combinations of resolution enhancement techniques (RET) for IC lithography, different process constraints are placed on the IC layout. The final layout used for mask production is dramatically different than the original designer's intent. To insure that EDA tools developed for applying RET techniques can have optimal performance, layout methodology must change to create a true "target" layer that represents the actual design intent. Verification of the final layout is then expanded from LVS and DRC to also include lithography process simulation, which compares results to this desired "target" and governs the application of RET.

General Terms
Algorithms, Design, Reliability, Standardization, Verification.

Keywords
RET, OPC, PSM, SRAF, scattering bars, lithography, phase-shifting, OAI, off-axis illumination, Quasar, quadrupole.

1. INTRODUCTION
The adoption of resolution enhancement techniques (RET) has grown at an exponential rate in recent years. [1,2] Manufacturing solutions are now in common production for the 180 nm node and beyond.

RET generally includes three distinct variations, each targeted at one of the physical properties of a wavefront on the mask. Wave direction is controlled by designing special illuminators (off-axis illumination, or OAI), wavefront amplitude is controlled by changing aperture sizes and shapes (optical and process correction, or OPC) and local wavefront phase is controlled by changing material properties or etching structures into the surface of the mask (phase-shifting masks, or PSM).

The selection of various combinations of these techniques depends on the resources available to individual wafer fabs. For example, if a company has an internal mask shop, a captive supply of phase-shifting masks may make the technique more attractive and easier to adopt. Other trade-offs can also occur.

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In this paper, we will focus on the adoption of two distinct combinations of RET, and their impact on the design and layout process. These are 1) the adoption of off-axis illumination with sub-resolution assist features (SRAF) for gate layers, and 2) the adoption of attenuated phase shifting with OPC for contact layers. Both of these techniques are finding wide adoption for manufacturing at 180 nm and development at 130 nm.

2. POLY WITH OAI AND SRAF
One common solution to resolution enhancement on the poly-gate layer is the adoption of off-axis illumination, augmented with sub-resolution assist features.

Off-axis illumination is a standard production tool for resolution enhancement [3,4]. When the illumination is chosen to fall on the mask at angles resonant with the pitch of periodic structures in the layout (ideal for IC arrays such as DRAM), the imaging characteristics of these periodic features are significantly enhanced. The on-axis components of the image, which do not add contrast, are reduced or eliminated. This is illustrated in Figure 1.

There are many geometric configurations of off-axis illumination, including dipole illumination, quadrupole illumination, and annular illumination [4].

There are two imaging problems this can introduce. First, only certain pitches and periodic patterns are enhanced, while others are reduced. For example, with Quasar Illumination by ASML, in which four sections of an annulus form four poles similar to a quadrupole system, light falls on the mask from 4 orientations at ±45°. This provides excellent enhancement for Manhattan geometries, but many pitches at 45° orientations scatter this light poorly, and therefore are not imaged on the wafer at all. This leads to some highly constrained design rules for these cases [5].

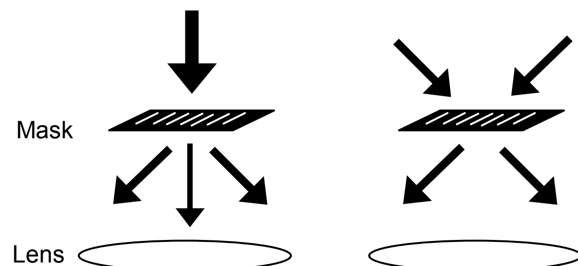

Figure 1: Left: Conventional Illumination. A strong on-axis component remains, which diminishes contrast on the wafer.

Right: Off-axis Illumination enhances the diffracted orders and removes the on-axis zero order.

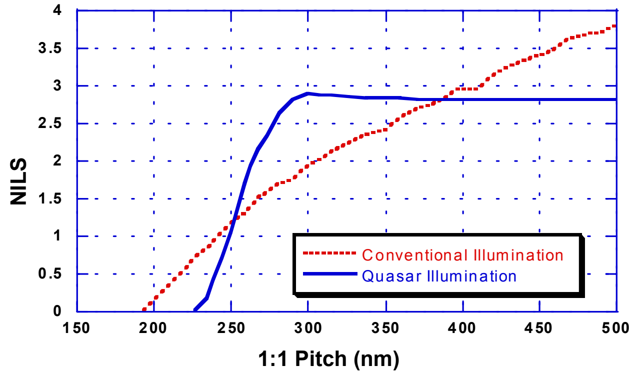

Figure 2: Performance of Quasar Illumination for small pitches. The y-axis is Normalized Image Log-Slope (NILS), a measure of image contrast. Exposure conditions are λ=248 nm, NA= 0.7, σ = 0.85 (conventional). For 1:1 pitches between 255 nm and 385 nm (feature sizes of 127 nm to 192 nm), the off-axis illumination gives a clear advantage.

The enhancement that can be achieved for small, dense pitches using Quasar illumination is shown in Figure 2. There is significant enhancement for smaller pitches, and the ability to reduce the resolvable feature size by nearly a factor of two makes the technique very attractive, in spite of the drawbacks.

However, the second process problem – that of iso-dense bias [6]- can be amplified with OAI. Iso-dense bias arises when features on the mask with the same linewidth print on the wafer with different dimensions. This is especially pronounced when comparing isolated and dense lines using off-axis illumination.

Normally, an isolated line scatters light uniformly over the lens used for wafer lithography, while an array of dense lines creates a distinct diffraction pattern that uses only certain parts of the lens. The angle of the light leaving the mask depends on the pitch of the mask structures, and diffracted light at higher angles (smaller pitches) can be attenuated. This leads to the bias effects found between isolated and dense lines.

Because the OAI technique further enhances the diffraction to the outer portions of the lens, the impact on isolated lines can be even more severe. This can give rise to another kind of "forbidden pitches", in which a line of a particular feature size would be prohibited from being placed in certain pitches [7].

Compensation for the iso-dense bias can be achieved using an inverse bias, applied as a design rule over the layout [8]. However, the isolated and dense lines still diffract differently in the lens, and various other imaging properties (such as depth of focus) can still be dissimilar.

It has been long known that sub-resolution features can be added to a mask layout to improve pattern fidelity. [9]. Recently, there has been a great deal of experimentation with sub-resolution assist features (SRAFs) [10,11], especially with SRAFs in combination with off-axis illumination [11,12,13]. By placing small additional features on the mask near isolated or semi-isolated lines, the diffraction pattern from the mask becomes similar to that of a dense line. Similar parts of the lens are used, similar transfer properties are observed, and the iso-dense bias is reduced. This is illustrated in Figure 3.

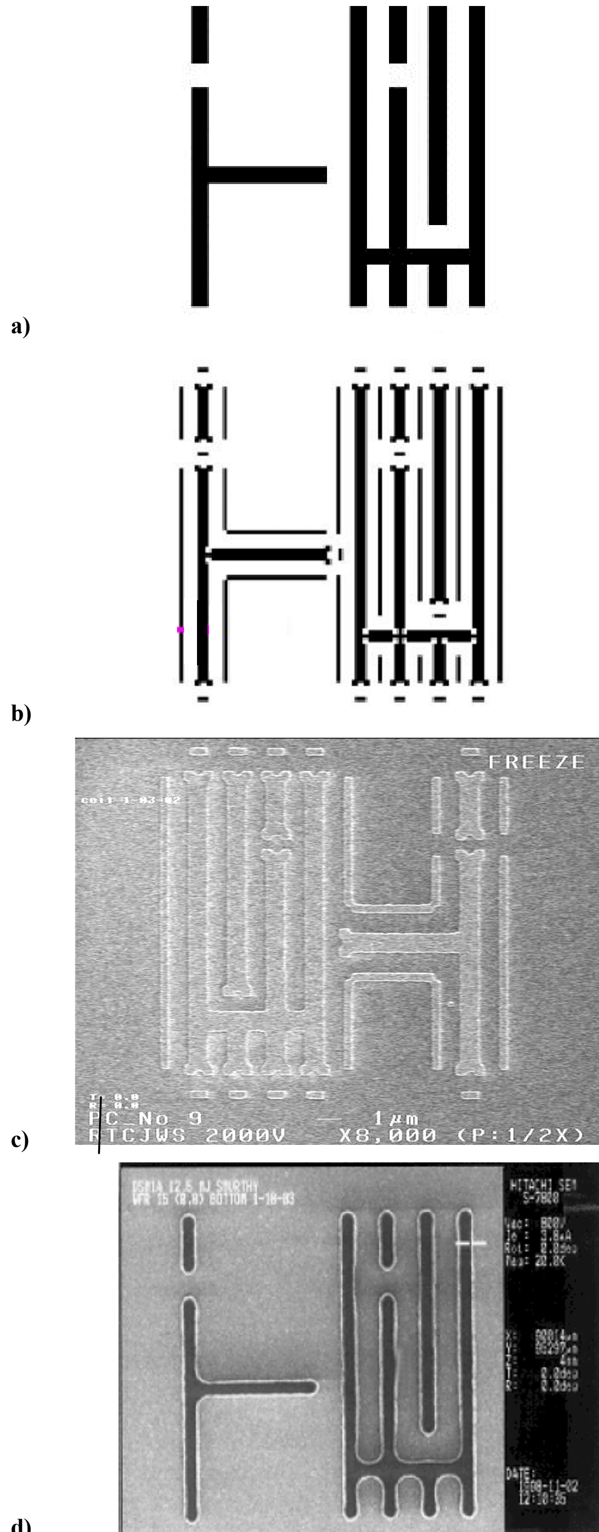

Figure 3: a) Original intended layout; b) Layout after the addition of SRAFs and serifs, c) SEM micrograph of the mask fabricated using the layout of b), and d) SEM micrograph of the wafer pattern formed using the mask of c). The final wafer pattern is very close to the original designer's intent.

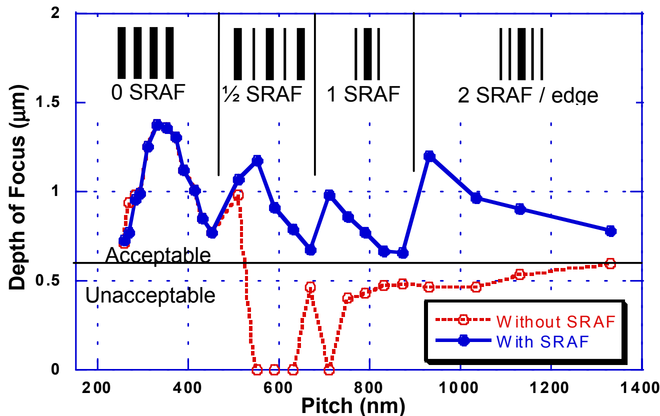

Figure 4: Pitch behavior for 130 nm features and Quasar Illumination. An acceptable DOF is greater than 0.6 µm. Without the addition of SRAFs, the "forbidden pitches" of 600 and 710 nm are dramatic process failures. With the appropriate insertion of a suitable number of SRAFs per edge, however, acceptable performance of the 130 nm feature is obtained at all pitches. Data adapted from reference [7].

The improvement that can be achieved using SRAFs to compensate for both the "forbidden pitches" and the iso-dense bias is shown in Figure 4. Here, the performance of a 130 nm line in various pitches is shown. Although dense features have a large performance latitude, pitches of 600 and 710 nm (130 nm lines with spaces of 470 nm and 580 nm) completely fail [7]. By inserting the appropriate combination of ½ , 1, or 2 SRAFs along the edges of each isolated or semi-isolated feature, as shown in the Figure, the failing of the off-axis illumination can be compensated.

The addition of SRAFs to compensate for lithography problems, especially those introduced by off-axis illumination, is manufacturable at some additional cost. Patterning a mask with the sub-resolution features, for example, is typically much more expensive than a standard mask. On the other hand, unlike some kinds of phase-shifting mask, masks with SRAFs can be manufactured, inspected, and repaired using standard fabrication tools found in most advanced mask shops. Since many wafers will typically be fabricated using each mask, the additional cost is balanced by the increased performance.

However, verification becomes more complicated. The layout for the mask, as Figure 3 dramatically illustrates, no longer resembles the intended designed layout and a DRC check of the mask layout will utterly fail. There is therefore a need to recognize the existence of a separation between the mask layouts that RET will generate and the designer's intent. Design flows must ensure that a "target" layout, as in Figure 3a, is also provided as a reference.

Using first principles simulation tools, such as PROLITH from KLA-Tencor, or various EDA products that incorporate wafer process simulation, such as Calibre ORC, the wafer image itself can be generated, and then checked using conventional design rules. Although the mask layout will fail these DRC checks, the wafer image will not. Modifying the verification flow to include these additional simulation tools is a requirement as the adoption of RET forces even more dramatic separations between mask layout and the designer's intent.

3. CONTACTS WITH AttPSM & OPC

In contrast to the simple rules that govern the placement of SRAFs, model-based OPC represents a very different style of OPC [14,15]. In model-based OPC, the flow for generation of the mask layout itself contains a process simulation step which predicts the final result on the wafer, and adapts the layout until convergence between the final image and the original physical design intent is achieved. This is typically inserted as part of the verification process in most design flows [16].

For imaging layers with contact holes, the production of arrays of these small features is now routinely executed using masks with attenuated phase shifting materials [17,18,19]. These are hybrid masks, in which the opaque material (typically chrome) is replaced with a slightly transparent material that also causes a uniform phase shift of 180°. This passes only enough light to cause a dark interference fringe to form at the boundaries of the features, enhancing image contrast and increasing image integrity, but typically does not allow enough light to pass through the mask to actually expose the photoresist in the dark areas.

Low light levels transmitted through multiple regions can cause some undesired artifacts on the wafer to occur. This takes place when constructive interference from adjacent contacts occurs, and an additional bright spot over the exposure threshold forms on the wafer. The circuit design clearly does not include these additional features, called "sidelobes", and this can have a severe impact on the device yield. The sidelobe problem is illustrated in Figure 5.

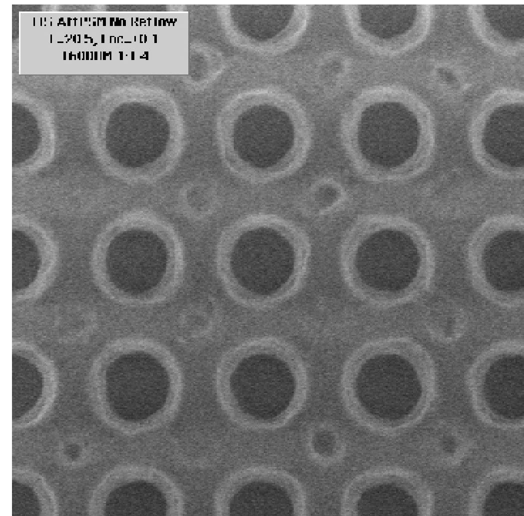

Figure 5: SEM micrograph of a contact layer with sidelobes.

An obvious way to address this is to remove additional light from the areas where sidelobes form. This is done by adding an opaque chrome patch to the mask, in an additional patterning step. Common patterning techniques using three layer mask blanks can be used to carry out this technique. However, the definition for these regions requires an additional steps in the mask layout process flow.

To insert these blocking structures, the layout software must first identify the locations where they occur. Predicting this can be more complicated when the areas of the contact apertures are being dynamically modified by model-based OPC programs. This

is accomplished by performing an additional check using the verification tool suite, as the model-based OPC simultaneously alters the aperture shapes for improved fidelity. When a sidelobe is detected, a patch of chrome to cover it is generated, and the OPC continues with the chrome patch in place. The final reticle layout will contain three layers, one for attenuated material, one for clear areas, and a third for chrome patches. This mask is often called a “tri-tone” mask.

This process can also be generalized to any layer fabricated using attenuated material, as shown in Figure 6. In this case, sidelobes do form near the contact structures, but can be identified and appropriate patches placed on the mask to correct them.

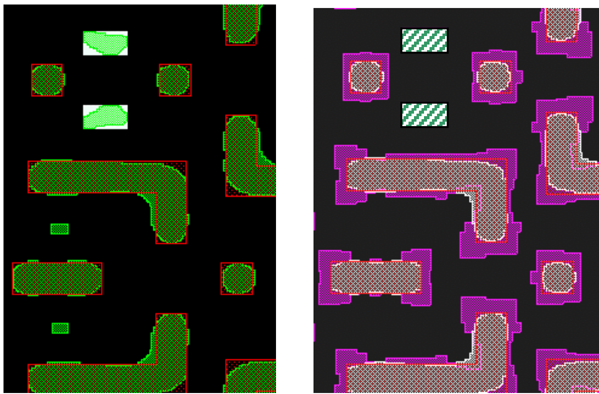

Figure 6: Left) Simulation result, identifying areas in which sidelobes occur, and right) a final reticle layout, compensated using model-based OPC and chrome patches to counter balance sidelobes.

Unlike the previous case using SRAFs, this technique is not significantly more expensive, with attenuated phase shifting mask blanks commonly available at typically ≈2x the cost of the normal mask. The final cost of ownership for this technique, typically used for contact layers as well as local interconnect layers, is much smaller than for the SRAF technique, and is far more widely adopted.

However, as with the SRAF technique, the mask layout again is dramatically different from the designer’s intent. The ability for layout verification tools to have reference to the “target” layer, representing the intent for the silicon wafer, and the ability to simulate the wafer image corresponding to the modified reticle layout and compare that to the “target”, become fundamental to the adoption of this technique.

4. CONCLUSIONS

No matter which RET technique is chosen, the differences between the original physical design of the circuit and the layout used to write the mask are now large and growing more extreme with each new IC generation. We have shown two examples of the use of combinations of RET in which significant numbers of non-printing polygons are added to the mask layout to ensure the image formed by lithography equipment ends up being as close as possible to the designer’s intent.

The routine adoption of these techniques further emphasizes the need for layout tools to produce layers that in fact reflect the exact physical design intended. These layers then serve as a reference point for the various compensation procedures that are required to make various RET predictable and reliable.

5. ACKNOWLEDGMENTS

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