Weekly Report

May 29 - June 05, 2005

Changbo Long

1 Paper Reading

1. Gone through some papers on physical design of power supply and sleep transistors such as
   "sleep transistor sizing using timing criticality and temporal currents"
   "Optimiizing C4 Bump placements for a peripheral I/O design"

2 Paper Writting

1. Finished proof-read of "micro-architecture and floorplanning co-optimization" and submitted this review version to TCAD. Unfortunately, this revision took too long and edit-in-chief sent email to say that it need to be submitted as a new submission.
2. Re-submitted "micro-architecture and floorplanning co-optimization" as a new paper to TCAD.
3. Gone through the review comments for "Placement of sleep transistors in power supply network", and come up with ways to revise the paper. Need more discussion with Jinjun and Prof. He.

3 Coding

1. Got the design of linear voltage regulator from Fei.