This week I focused on the FPGA interconnect power variation. For the leakage power, we have the following power model:

$$P = P_0 e^{-(c_1 \Delta V + c_2 \Delta L + c_3 \Delta T)}$$

Where  $P_0$  is the nominal value of leakage power,  $\Delta V$ ,  $\Delta L$ , and  $\Delta T$  are the variation of threshold voltage, effective channel length and oxide thickness, respectively. Let:

$$\Delta V = V_g + V_l$$
$$\Delta L = L_g + L_l$$
$$\Delta T = T_g + T_l$$

Where  $V_g$ ,  $L_g$ , and  $T_g$  are the global variation of V<sub>th</sub>, L<sub>eff</sub>, and T<sub>ox</sub>, respectively, and  $V_l$ ,  $L_l$ , and  $T_l$  are the local variation of V<sub>th</sub>, L<sub>eff</sub>, and T<sub>ox</sub>, respectively. Then the leakage power can be expressed as:

$$P = P_0 e^{-(c_1 V_g + c_2 L_g + c_3 \Delta T_g) - (c_1 V_l + c_2 L_l + c_3 \Delta T_l)}$$

For the local variation, because there are large number of interconnect buffers, we can applied the central limit theorem. Then for a given global variation, we have:

$$E[P | V_g, L_g, T_g] = P_0 e^{-(c_1 V_g + c_2 L_g + c_3 \Delta T_g)} E[e^{-(c_1 V_l + c_2 L_l + c_3 \Delta T_l)}]$$
  
=  $P_0 e^{-(c_1 V_g + c_2 L_g + c_3 \Delta T_g)} \iiint e^{-(c_1 V_l + c_2 L_l + c_3 \Delta T_l)} pdf(V_l, L_l, T_l) dV_l dL_l dT_l$   
=  $P_0 e^{-(c_1 V_g + c_2 L_g + c_3 \Delta T_g)} e^{-(\frac{c_1^2 \sigma_1^2}{2} + \frac{c_2^2 \sigma_2^2}{2} + \frac{c_3^2 \sigma_3^2}{2})}$ 

Where  $\sigma_1$ ,  $\sigma_2$ ,  $\sigma_3$  are the standard variance of V<sub>th</sub>, L<sub>eff</sub>, and T<sub>ox</sub> respectively. Here we assume that the distribution of both the local and global variable are normal. For the global variation, we can apply Monte Carlo simulation to estimate the variation of interconnect leakage power.

For the dynamic power, we have:

$$P_{H} = \frac{1}{2} f \cdot sw \cdot C_{load} \cdot V_{dd}^{2}$$
$$P_{L} = \frac{1}{2} f \cdot sw \cdot C_{load} \cdot V_{dd} (V_{dd} - c_{4} (V_{th0} - V_{g} - V_{l}))$$

Where P<sub>H</sub> and P<sub>L</sub> are the dynamic power for high Vdd buffer and low Vdd buffer, respectively. For

local variation, we apply central limit theorem. Similar to the leakage power model, given the global variation, we have:

$$\begin{split} E[P_{L} | V_{g}] &= E[\frac{1}{2}f \cdot sw \cdot C_{load} \cdot V_{dd}(V_{dd} - c_{4}(V_{th0} - V_{g} - V_{l})) | V_{g}] \\ &= \frac{1}{2}f \cdot sw \cdot C_{load} \cdot V_{dd}(V_{dd} - c_{4}(V_{th0} - V_{g} - E[V_{l}])) \\ &= \frac{1}{2}f \cdot sw \cdot C_{load} \cdot V_{dd}(V_{dd} - c_{4}(V_{th0} - V_{g})) \end{split}$$

For the global variation, we can apply Monte Carlo simulation to obtain the variation of interconnect dynamic power.