

## 1. TIME SLACK ALLOCATION WITH WIRE SEGMENTS OF DIFFERENT LENGTHS

we use the net-based formulation which partitions the constraints on path delay into constraints on delay across circuit elements or routing. Let  $a(v)$  be the arrival time for vertex  $v$  in  $\mathcal{G}$  and the timing constraints for PI and PO are as below,

$$a(v) \leq T_{spec} \quad \forall v \in \mathcal{PO} \quad (1)$$

$$a(v) = 0 \quad \forall v \in \mathcal{PI} \quad (2)$$

For the edges corresponding to routing in  $\mathcal{G}$ , the constraints considering slack can be expressed as

$$\begin{aligned} a(p_{i0}) + d(p_{i0}, p_{ik}) + S_{ik} &\leq a(p_{ik}) \\ 0 \leq i < N_r \wedge \forall p_{ik} \in \mathcal{FO}_{p_{i0}} \end{aligned} \quad (3)$$

where vertex  $p_{i0}$  is the source of  $\mathcal{R}_i$  in  $\mathcal{G}$ , vertex  $p_{ik}$  is  $k^{th}$  sink of  $\mathcal{R}_i$  in  $\mathcal{G}$ ,  $S_{ik}$  is the slack allocated to  $k^{th}$  sink in  $\mathcal{R}_i$  and  $d(p_{i0}, p_{ik})$  is the delay from  $p_{i0}$  to  $p_{ik}$  in  $\mathcal{R}_i$  using VddH. For the edges other than routing in  $\mathcal{G}$ , the constraints can be expressed as

$$a(u) + d(u, v) \leq a(v) \quad \forall u \in \mathcal{V} \wedge u \notin \mathcal{SRC} \wedge v \in \mathcal{FO}_u \quad (4)$$

where  $\mathcal{SRC}$  is a subset of  $\mathcal{V}$  and gives the set of vertices corresponding to routing tree sources.

There is an upper bound for slack, which is the delay increase when VddL is assigned to all the switches in a tree. Clearly, slack more than the upper bound cannot lead to more VddL switches. We define the *useful slack* of each routing tree sink as the slack less than this upper bound. For the rest part of the paper, we use slack to represent the useful slack. The slack upper bound constraints can be expressed as

$$0 \leq S_{ik} \leq D_{ik} \quad 0 \leq i < N_r \wedge 1 \leq k \leq N_k(i) \quad (5)$$

where  $N_k(i)$  is the number of sinks in  $\mathcal{R}_i$  and  $D_{ik}$  is the delay increase of the path from the source to  $k^{th}$  sink in  $\mathcal{R}_i$  when VddL is assigned to all the switches in that path.

Given a routing tree with arbitrary topology and allocated slack for each sink, we need to estimate power reduction that can be achieved. We use  $l_{ik}$  represent the number of switches in the path from the source to  $k^{th}$  sink in  $\mathcal{R}_i$ . We first transform slack  $S_{ik}$  into  $s_{ik}$ , which is expressed in number of switches as follows,

$$s_{ik} = \frac{S_{ik}}{D_{ik}} \cdot l_{ik} \quad (6)$$

We then estimate the VddL switch number that can be achieved using  $s_{ik}$ . We use  $C_{ik}$  to represent the total load capacitance of the switches in the path from the source to  $k^{th}$  sink in  $\mathcal{R}_i$ . We use  $c_{ij}$  to represent the load capacitance of  $j^{th}$  switch in  $\mathcal{R}_i$ . We define *sink list*  $\mathcal{SL}_{ij}$  as the set of sinks in the fanout cone of  $j^{th}$  switch

in  $\mathcal{R}_i$ . We then estimate the number of VddL switches that can be achieved given the allocated slack as

$$F_n(i) = \sum_{j=0}^{N_s(i)-1} \min\left(\frac{s_{ik}}{C_{ik}} \cdot c_{ij} : \forall k \in \mathcal{SL}_{ij}\right) \quad (7)$$

To estimate the number of VddL switches that can be achieved in tree  $\mathcal{R}_i$ , we first deliberately distribute the slack  $s_{ik}$  to the switches in the path from source to  $k^{th}$  sink in  $\mathcal{R}_i$  considering the load capacitance of each switch. For a switch with multiple sinks in its fanout cone, we choose the minimum  $s_{ik}c_{ij}/C_{ik}$  as the slack distributed to the switch. We then add the slack distributed to all the switches in  $\mathcal{R}_i$ . and get the estimated number of VddL switches. The rationale is that we consider  $k^{th}$  sink with minimum  $s_{ik}c_{ij}/C_{ik}$  in sink list  $\mathcal{SL}_{ij}$  as the most critical sink to  $j^{th}$  switch in  $\mathcal{R}_i$ .

We then estimate the power reduction of  $\mathcal{R}_i$ . The dynamic power reduction of the tree  $\mathcal{R}_i$  is estimated as the sum of the dynamic power reduction of each switch in  $\mathcal{R}_i$  and can be expressed as,

$$P_{dr}(i) = 0.5f_{clk} \cdot \Delta V dd^2 \cdot f_s(i) \sum_{j=0}^{N_s(i)-1} [\min\left(\frac{s_{ik}}{C_{ik}} \cdot c_{ij} : \forall k \in \mathcal{SL}_{ij}\right) \cdot c_{ij}] \quad (8)$$

The leakage power reduction of  $\mathcal{R}_i$  is also the sum of the leakage power reduction of each switch in  $\mathcal{R}_i$  and can be expressed as,

$$P_{lr}(i) = \sum_{j=0}^{N_s(i)-1} [\min\left(\frac{s_{ik}}{C_{ik}} \cdot c_{ij} : \forall k \in \mathcal{SL}_{ij}\right) \cdot \Delta P_s(i, j)] \quad (9)$$

where  $\Delta P_s(i, j)$  is the leakage power difference of  $j^{th}$  switch in  $\mathcal{R}_i$  between VddH and VddL. Wire segments with different lengths might be driven by switches with different sizes. The objective is to maximize power reduction given by the sum of (8) and (9). To incorporate (8) and (9) into mathematical programming, we introduce a variable  $f_n(i, j)$  for  $j^{th}$  switch in  $\mathcal{R}_i$  and some additional constraints. The new objective function after transformation plus the *additional constraints* can be expressed as

$$\begin{aligned} \text{Maximize} \quad & \sum_{i=0}^{N_r-1} 0.5f_{clk} \Delta V dd^2 \sum_{j=0}^{N_s(i)-1} f_n(i, j) f_s(i, j) c_{ij} \\ & + \sum_{i=0}^{N_r-1} \sum_{j=0}^{N_s(i)-1} f_n(i, j) \Delta P_s(i, j) \end{aligned} \quad (10)$$

s.t.

$$f_n(i, j) \leq \frac{s_{ik}}{C_{ik}} c_{ij} \quad 0 \leq i < N_r \wedge 0 \leq j < N_s(i) \wedge \forall k \in \mathcal{SL}_{ij} \quad (11)$$

We formulate the *time slack allocation problem* using objective function (10), additional constraints (11), slack upper bound constraints (5), plus timing constraints (1), (2), (3) and (4). It is

easy to verify that (1), (2), (5)  $\sim$  (4) and (11) are linear, and the objective function (10) is linear too. Hence we have the following theorem.

**THEOREM 1.** *The time slack allocation problem is a linear programming (LP) problem.*

Therefore, we can first solve the extended time slack allocation problem and then perform net-level assignment and refinement for the interconnects using wire segments of different lengths.

## 2. STATISTICAL DELAY AND POWER MODELS

We consider the variation in threshold voltage ( $V_{th}$ ), effective channel length ( $L_{eff}$ ), and gate oxide thickness ( $T_{ox}$ ). Similar to [1] where ASIC is assumed, each variation ( $\Delta P$ ) is decomposed into global (die-to-die) variation ( $\Delta P_g$ ) and local (within-die) variation ( $\Delta P_l$ ). Both global and local variations are modeled as normal random variables. To make presentation simple, we denote  $\Delta L_{eff}$ ,  $\Delta V_{th}$  and  $\Delta T_{ox}$  as  $L$ ,  $V$  and  $T$ , respectively.  $L$ ,  $V$  and  $T$  can be decomposed into local ( $L_l$ ,  $V_l$ ,  $T_l$ ) and global ( $L_g$ ,  $V_g$ ,  $T_g$ ) components.

Power reduction of an interconnect switch by changing the Vdd-level from VddH to VddL considering process variation is presented as below,

$$\Delta P = \Delta P_0 e^{-c_1 L} e^{-c_2 V} e^{-c_3 T} \quad (12)$$

$$\Delta E = \Delta E_0 + \frac{\partial \Delta E}{\partial V} \Delta V = \Delta E_0 + c_4 \Delta V \quad (13)$$

$\Delta P$  is leakage power reduction,  $\Delta E$  is dynamic energy per signal switch reduction when driving unit load capacitance.  $c_1$ ,  $c_2$ ,  $c_3$  and  $c_4$  are curve fit parameters.  $\Delta P_0$  and  $\Delta E_0$  are the nominal values.  $\Delta P$  exponentially depends on  $L$ ,  $V$  and  $T$ , and it can be modeled as a lognormal (LN) random variable. We assume a first-order Taylor expansion of dynamic energy reduction  $\Delta E$  is adequate, which therefore can be modeled as a normal random variable. A first-order Taylor expansion of circuit element delay is also assumed as adequate,

$$d = d_0 + \frac{\partial d}{\partial L} \Delta L + \frac{\partial d}{\partial V} \Delta V = d_0 + c_5 L + c_6 V \quad (14)$$

where  $d_0$  is the nominal value of circuit element delay,  $c_4$  and  $c_5$  are curve fit parameters. Delay  $d$  is a normal random variable under this model.

## 3. STATISTICAL POWER OPTIMIZATION

### 3.1 Chip-level Time Slack Allocation

To handle the variability of process parameters, we reformulate the time slack allocation problem as a robust linear program problem which can be solved efficiently using interior-point convex methods [2]. We first the objective function (10) into an equivalent formulation as below, which places the power reduction into the constraint set

$$\text{Minimize } \sum_{i=0}^{N_r-1} \sum_{k=0}^{N_s(i)-1} S_{ik} \quad (15)$$

s.t.

$$\sum_{i=0}^{N_r-1} \sum_{j=0}^{N_s(i)-1} \Delta P_d(i, j) f_n(i, j) \geq \Delta \hat{P}_{dyn}$$

$$\Delta P_d(i, j) = \Delta E c_{ij} f_{clk} f_s i, j \quad (16)$$

$$\sum_{i=0}^{N_r-1} \sum_{j=0}^{N_s(i)-1} \Delta P_s(i, j) f_n(i, j) \geq \Delta \hat{P}_{leak} \quad (17)$$

where  $\Delta \hat{P}_{dyn}$  and  $\Delta \hat{P}_{leak}$  are the optimal dynamic and leakage power reduction achieved by the time slack allocation problem without considering process variation.

### 3.2 Net-level Bottom-up Assignment

## 4. REFERENCES

- [1] R. Rao, A. Devgan, D. Blaauw, and D. Sylvester, "Parametric yield estimation considering leakage variability," in *Proc. Design Automation Conf.*, June 2004.
- [2] S. Boyd and L. Vandenberghe, *Convex Optimization*. Cambridge, 2004.