I/O standards supported by Altera Stratix

Table 4–1. I/O Standard Applications & Performance (Part 1 of 2) Note (1)

I/O Standard	Application	Performance
3.3-V LVTTL/LVCMOS	General purpose	350 MHz
2.5-V LVTTL/LVCMOS	General purpose	350 MHz
1.8-V LVTTL/LVCMOS	General purpose	250 MHz
1.5-V LVCMOS	General purpose	225 MHz
PCI/CompactPCI	PC/embedded systems	66 MHz
PCI-X 1.0	PC/embedded systems	133 MHz
AGP 1× and 2×	Graphics processors	66 to 133 MHz
SSTL-3 class I and II	SDRAM	167 MHz
SSTL-2 class I and II	DDR I SDRAM	160 to 400 Mbps
HSTL class I	QDR SRAM/SRAM/CSIX	150 to 225 MHz
HSTL class II	QDR SRAM/SRAM/CSIX	150 to 250 MHz
Differential HSTL	Clock interfaces	150 to 225 MHz
GTL	Backplane driver	200 MHz
GTL+	Pentium processor interface	133 to 200 MHz
LVDS	Communications	840 Mbps
HyperTransport technology	Motherboard interfaces	800 Mbps
LVPECL	PHY interface	840 Mbps
PCML	Communications	840 Mbps
Differential SSTL-2	DDR I SDRAM	160 to 400 Mbps
CTT	Back planes and bus interfaces	200 MHz

Note to Table 4–1:

(1) These performance values are dependent on device speed grade, package type (flip-chip or wirebond) and location of I/Os (top/bottom or left/right). See the *DC & Switching Characteristics* chapter of the *Stratix Device Handbook, Volume 1*.

Explanation for some general purpose I/O standards

3.3-V Low Voltage Transistor-Transistor Logic (LVTTL) - EIA/JEDEC Standard JESD8-B

The 3.3-V LVTTL I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVTTL standard defines the DC interface parameters for digital circuits operating from a 3.0-V or 3.3-V power supply and driving or being driven by LVTTL-compatible devices.

The LVTTL input standard specifies a wider input voltage range of $-0.5\ V \leq V_I \leq 3.8\ V$. Altera allows an input voltage range of $-0.5\ V \leq V_I \leq 4.1\ V$. The LVTTL standard does not require input reference voltages or board terminations.

Stratix and Stratix GX devices support both input and output levels for 3.3-V LVTTL operation.

3.3-V LVCMOS - EIA/JEDEC Standard JESD8-B

The 3.3-V low voltage complementary metal oxide semiconductor (LVCMOS) I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVCMOS standard defines the DC interface parameters for digital circuits operating from a 3.0-V or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices.

The LVCMOS standard specifies the same input voltage requirements as LVTTL ($-0.5\ V \leq V_I \leq 3.8\ V$). The output buffer drives to the rail to meet the minimum high-level output voltage requirements. The 3.3-V I/O standard does not require input reference voltages or board terminations.

Stratix and Stratix GX devices support both input and output levels for 3.3-V LVCMOS operation.

2.5-V LVTTL Normal Voltage Range - EIA/JEDEC Standard EIA/JESD8-5

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices. The input and output voltage ranges are:

- The 2.5-V normal range input standards specify an input voltage range of $-0.3\ V \leq V_I \leq 3.0\ V$.
- The normal range minimum high-level output voltage requirement (V_{OH}) is 2.1 V.

Stratix and Stratix GX devices support both input and output levels for 2.5-V LVTTL operation.

2.5-V LVCMOS Normal Voltage Range - EIA/JEDEC Standard EIA/JESD8-5

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts. The input and output voltage ranges are:

- The 2.5-V normal range input standards specify an input voltage range of $-0.5\ V \leq V_I \leq 3.0\ V$.
- The normal range minimum V_{OH} requirement is 2.1 V.

Stratix and Stratix GX devices support both input and output levels for 2.5-V LVCMOS operation.

1.8-V LVTTL Normal Voltage Range - EIA/JEDEC Standard EIA/JESD8-7

The 1.8-V I/O standard is used for 1.8-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts. The input and output voltage ranges are:

- The 1.8-V normal range input standards specify an input voltage range of – 0.5 V $\leq V_I \leq$ 2.3 V.
- The normal range minimum V_{OH} requirement is V_{CCIO} – 0.45 V.

Stratix and Stratix GX devices support both input and output levels for 1.8-V LVTTL operation.

1.8-V LVCMOS Normal Voltage Range - EIA/JEDEC Standard EIA/JESD8-7

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V devices. The input and output voltage ranges are:

- The 1.8-V normal range input standards specify an input voltage range of – 0.5 V $\leq V_I \leq$ 2.5 V.
- The normal range minimum V_{OH} requirement is V_{CCIO} – 0.45 V.

Stratix and Stratix GX devices support both input and output levels for 1.8-V LVCMOS operation.

1.5-V LVCMOS Normal Voltage Range - EIA/JEDEC Standard JESD8-11

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices. The input and output voltage ranges are:

- The 1.5-V normal range input standards specify an input voltage range of – 0.5 V $\leq V_I \leq$ 2.0 V.
- The normal range minimum V_{OH} requirement is 1.05 V.

Stratix and Stratix GX devices support both input and output levels for 1.5-V LVCMOS operation.

1.5-V HSTL Class I & II - EIA/JEDEC Standard EIA/JESD8-6

The high-speed transceiver logic (HSTL) I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range. This standard defines single ended input and output specifications for all HSTL-compliant digital integrated circuits. The single ended input standard specifies an input voltage range of $-0.3\ V \leq V_I \leq V_{CCIO} + 0.3\ V$. Stratix and Stratix GX devices support both input and output levels specified by the 1.5-V HSTL I/O standard. The input clock is implemented using dedicated differential input buffers. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a differential output clock. Additionally, the 1.5-V HSTL I/O standard in Stratix and Stratix GX devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE and APEX 20KC devices because the input and output voltage thresholds are compatible. See Figures 4–1 and 4–2. Stratix and Stratix GX devices support both input and output levels with V_{REF} and V_{TT}.

Figure 4–1. HSTL Class I Termination

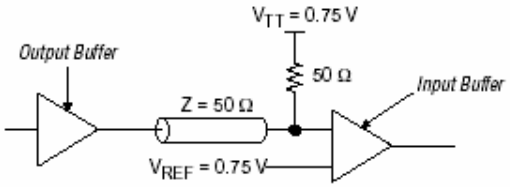
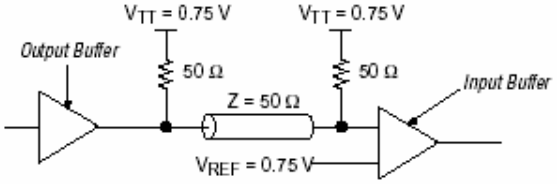


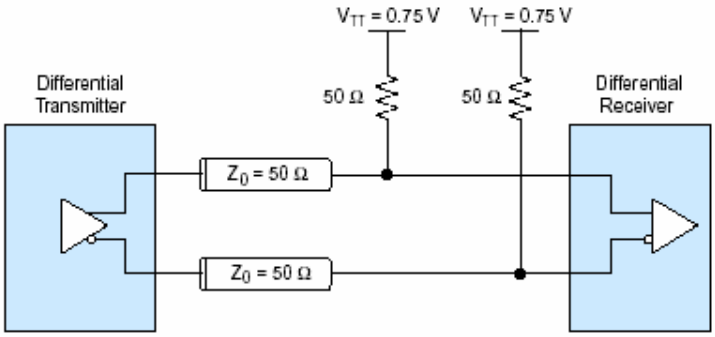
Figure 4–2. HSTL Class II Termination



1.5-V Differential HSTL - EIA/JEDEC Standard EIA/JESD8-6

The differential HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces. The differential HSTL specification is the same as the single ended HSTL specification. The standard specifies an input voltage range of $-0.3\ V \le V_I \le V_{CCIO} + 0.3\ V$. Differential HSTL does not require an input reference voltage, however, it does require a 50 Ω resistor termination resistor to V_{TT} at the input buffer (see Figure 4–3). Stratix and Stratix GX devices support both input and output clock levels for 1.5-V differential HSTL. The input clock is implemented using dedicated differential input buffer. Two single-ended output buffers are automatically programmed to have opposite polarity so as to implement a differential output clock.

Figure 4–3. 1.5-V Differential HSTL Class I Termination



Drive Strength

Each I/O standard supported by Stratix and Stratix GX devices drives out a minimum drive strength. When an I/O is configured as LVTTL or LVCMOS I/O standards, you can specify the current drive strength, as summarized in Table 4–7.

Standard Current Drive Strength

Each I/O standard supported by Stratix and Stratix GX devices drives out a minimum drive strength. Table 4–6 summarizes the minimum drive strength of each I/O standard.

Table 4–6. Minimum Current Drive Strength of Each I/O Standard

I/O Standard	Current Strength, I_{OL}/I_{OH} (mA)
GTL	40 *(1)*
GTL+	34 *(1)*
SSTL-3 Class I	8
SSTL-3 Class II	16
SSTL-2 Class I	8.1
SSTL-2 Class II	16.4
SSTL-18 Class I	6.7
SSTL-18 Class II	13.4
1.5-V HSTL Class I	8
1.5-V HSTL Class II	16
CTT	8
AGP 1X	$I_{OL} = 1.5$, $I_{OH} = -0.5$

Note to Table 4–6:

(1) Since this I/O standard uses an open drain buffer, this value refers to I_{OL}.

Programmable Current Drive Strength

The Stratix and Stratix GX device I/O pins support various output current drive settings as shown in Table 4–7. These programmable drive strength settings help decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the I_{OH} and I_{OL} specifications for the corresponding I/O standard.

Table 4–7. Programmable Drive Strength

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	24 *(1)*, 16, 12, 8, 4
3.3-V LVCMOS	24 *(2)*, 12 *(1)*, 8, 4, 2
2.5-V LVTTL/LVCMOS	16 *(1)*, 12, 8, 2
1.8-V LVTTL/LVCMOS	12 *(1)*, 8, 2
1.5-V LVCMOS	8 *(1)*, 4, 2

Notes to Table 4–7:
(1) This is the Quartus II software default current setting.
(2) I/O banks 1, 2, 5, and 6 do not support this setting.

These drive-strength settings are programmable on a per-pin basis (for output and bidirectional pins only) using the Quartus II software. To modify the current strength of a particular pin, see "Programmable Drive Strength Settings" on page 4–40.

Altera Stratix II

Below is the I/O standards supported by Stratix II. For general purpose I/O standards, refer to Stratix on the above.

Table 4–1. I/O Standard Applications

I/O Standard	Application
LVTTL	General purpose
LVCMOS	General purpose
2.5 V	General purpose
1.8 V	General purpose
1.5 V	General purpose
3.3-V PCI	PC and embedded system
3.3-V PCI-X	PC and embedded system
SSTL-2 class I	DDR SDRAM
SSTL-2 class II	DDR SDRAM
SSTL-18 class I	DDR2 SDRAM
SSTL-18 class II	DDR2 SDRAM
1.8-V HSTL class I	QDRII SRAM/RLDRAM II/SRAM
1.8-V HSTL class II	QDRII SRAM/RLDRAM II/SRAM
1.5-V HSTL class I	SRAM
1.5-V HSTL class II	QDRII SRAM/SRAM
Differential SSTL-2 class I	DDR SDRAM
Differential SSTL-2 class II	DDR SDRAM
Differential SSTL-18 class I	DDR2 SDRAM
Differential SSTL-18 class II	DDR2 SDRAM
1.8-V differential HSTL class I	Clock interfaces
1.8-V differential HSTL class II	Clock interfaces
1.5-V differential HSTL class I	Clock interfaces
1.5-V differential HSTL class II	Clock interfaces
LVDS	High-speed communications
HyperTransport™ technology	PCB interfaces
Differential LVPECL	Video graphics and clock distribution

Table 4–2. I/O Standard Performance Target *Notes (1), (2), (3)*

I/O Standard	Clock Rate / Single Data Rate (MHz)	Double Data Rate (Mbps)
LVTTL	300	600
LVCMOS	300	600
2.5 V	300	600
1.8 V	250	500
1.5 V	200	400
3.3-V PCI	66	-
3.3-V PCI-X	133	266
SSTL-2 class I	200	400
SSTL-2 class II	200	400
SSTL-18 class I	267	533
SSTL-18 class II	267	533
1.8-V HSTL class I	300	600
1.8-V HSTL class II	300	600
1.5-V HSTL class I	250	500
1.5-V HSTL class II	250	500
Differential SSTL-2 class I	200	400
Differential SSTL-2 class II	200	400
Differential SSTL-18 class I	267	533
Differential SSTL-18 class II	267	533
1.8-V differential HSTL class I	300	600
1.8-V differential HSTL class II	300	600
1.5-V differential HSTL class I	300	600
1.5-V differential HSTL class II	300	600
LVDS	500	1000
HyperTransport technology	500	1000
Differential LVPECL	450	900

I/O Standards and voltage level

Table 4–6. Stratix II I/O Standards & Voltage Levels (Part 1 of 2) *Note (1)*

I/O Standard	V_{CCIO} (V)				Input V_{REF} (V)	Termination V_{TT} (V)
	Input Operation		Output Operation			
	Top & Bottom I/O Banks	Left & Right I/O Banks	Top & Bottom I/O Banks	Left & Right I/O Banks		
LVTTL	3.3/2.5	3.3/2.5	3.3	3.3	NA	NA
LVCMOS	3.3/2.5	3.3/2.5	3.3	3.3	NA	NA
2.5 V	3.3/2.5	3.3/2.5	2.5	2.5	NA	NA
1.8 V	1.8/1.5	1.8/1.5	1.8	1.8	NA	NA
1.5 V	1.8/1.5	1.8/1.5	1.5	1.5	NA	NA
3.3-V PCI	3.3	NA	3.3	NA	NA	NA
3.3-V PCI-X	3.3	NA	3.3	NA	NA	NA
SSTL-2 class I	2.5	2.5	2.5	2.5	1.25	1.25
SSTL-2 class II	2.5	2.5	2.5	2.5	1.25	1.25
SSTL-18 class I	1.8	1.8	1.8	1.8	0.90	0.90
SSTL-18 class II	1.8	1.8	1.8	NA	0.90	0.90
1.8-V HSTL class I	1.8	1.8	1.8	NA	0.90	0.90
1.8-V HSTL class II	1.8	1.8	1.8	NA	0.90	0.90
1.5-V HSTL class I	1.5	1.5	1.5	NA	0.75	0.75
1.5-V HSTL class II	1.5	1.5	1.5	NA	0.75	0.75
Differential SSTL-2 class I	2.5	2.5	2.5	2.5	1.25	1.25
Differential SSTL-2 class II	2.5	2.5	2.5	2.5	1.25	1.25
Differential SSTL-18 class I	1.8	1.8	1.8	1.8	0.90	0.90
Differential SSTL-18 class II	1.8	1.8	1.8	NA	0.90	0.90
1.8-V differential HSTL class I	1.8	1.8	1.8	NA	0.90	0.90
1.8-V differential HSTL class II	1.8	1.8	1.8	NA	0.90	0.90

Table 4–6. Stratix II I/O Standards & Voltage Levels (Part 2 of 2) *Note (1)*

I/O Standard	V_{CCIO} (V)				Input V_{REF} (V)	Termination V_{TT} (V)
	Input Operation		Output Operation			
	Top & Bottom I/O Banks	Left & Right I/O Banks	Top & Bottom I/O Banks	Left & Right I/O Banks		
1.5-V differential HSTL class I	1.5	1.5	1.5	NA	0.75	0.75
1.5-V differential HSTL class II	1.5	1.5	1.5	NA	0.75	0.75
LVDS *(2)*	3.3/2.5/1.8/1.5	2.5	3.3	2.5	NA	NA
HyperTransport technology *(2)*	3.3/2.5/1.8/1.5	2.5	3.3	2.5	NA	NA
Differential LVPECL *(2)*	3.3/2.5/1.8/1.5	NA	3.3	NA	NA	NA

Notes to Table 4–6:

(1) Any input pins with PCI-clamping-diode enabled force the V_{CCIO} to 3.3 V.

(2) LVDS, HyperTransport, and LVPECL output operation in the top and bottom banks is only supported in PLL banks 9-12. The V_{CCIO} level for differential output operation in the PLL banks is 3.3 V. The V_{CCIO} level for output operation in the left and right I/O banks is 2.5 V.

Xilinx Virtex II

I/O Standards, see Altera Stratix on the above for general purpose standards LVTTL and LVCMOS

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

- HSTL (Class I, II, III, and IV)
- SSTL (3.3V and 2.5V, Class I and II)
- AGP-2X

The digitally controlled impedance (DCI) I/O feature automatically provides on-chip termination for each I/O element.

The IOB elements also support the following differential signaling I/O standards:

- LVDS
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Voltage level

Table 1: **Supported Single-Ended I/O Standards**

IOSTANDARD Attribute	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/R(3)	N/R
LVCMOS33	3.3	3.3	N/R	N/R
LVCMOS25	2.5	2.5	N/R	N/R
LVCMOS18	1.8	1.8	N/R	N/R
LVCMOS15	1.5	1.5	N/R	N/R
PCI33_3	3.3	3.3	N/R	N/R
PCI66_3	3.3	3.3	N/R	N/R
PCI-X	3.3	3.3	N/R	N/R
GTL	Note (1)	Note (1)	0.8	1.2
GTLP	Note (1)	Note (1)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III _18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL18_I(2)	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL3_I	3.3	N/R	1.5	1.5
SSTL3_II	3.3	N/R	1.5	1.5
AGP-2X/AGP	3.3	N/R	1.32	N/R

Notes:

1. V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. Example: If the pin High level is 1.5V, connect V_{CCO} to 1.5V.
2. SSTL18_I is not a JEDEC-supported standard.
3. N/R = no requirement.

Table 2: **Supported Differential Signal I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LVPECL_33	3.3	N/R(1)	N/R	0.490 - 1.220
LDT_25	2.5	N/R	N/R	0.500 - 0.700
LVDS_33	3.3	N/R	N/R	0.250 - 0.400
LVDS_25	2.5	N/R	N/R	0.250 - 0.400
LVDSEXT_33	3.3	N/R	N/R	0.440 - 0.820
LVDSEXT_25	2.5	N/R	N/R	0.440 - 0.820
BLVDS_25	2.5	N/R	N/R	0.250 - 0.450
ULVDS_25	2.5	N/R	N/R	0.500 - 0.700

Notes:
1. N/R = no requirement.

Table 3: **Supported DCI I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33(1)	3.3	3.3	N/R(4)	Series
LVDCI_DV2_33(1)	3.3	3.3	N/R	Series
LVDCI_25(1)	2.5	2.5	N/R	Series
LVDCI_DV2_25(1)	2.5	2.5	N/R	Series
LVDCI_18(1)	1.8	1.8	N/R	Series
LVDCI_DV2_18(1)	1.8	1.8	N/R	Series
LVDCI_15(1)	1.5	1.5	N/R	Series
LVDCI_DV2_15(1)	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL18_I_DCI(3)	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL3_I_DCI(2)	3.3	3.3	1.5	Split
SSTL3_II_DCI(2)	3.3	3.3	1.5	Split
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDSEXT_25_DCI	2.5	2.5	N/R	Split

Notes:
1. LVDCI_XX and LVDCI_DV2_XX are LVCMOS controlled impedance buffers, matching the reference resistors or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

Table 5: **Summary of Voltage Supply Requirements for All Input and Output Standards**

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
LVDS_33	3.3	N/R	N/R[1]	N/R	N/R
LVDSEXT_33			N/R	N/R	N/R
LVPECL_33			N/R	N/R	N/R
SSTL3_I			1.5	N/R	N/R
SSTL3_II			1.5	N/R	N/R
AGP			1.32	N/R	N/R
LVTTL		3.3	N/R	N/R	N/R
LVCMOS33			N/R	N/R	N/R
LVDCI_33			N/R	Series	N/R
LVDCI_DV2_33			N/R	Series	N/R
PCI33_3			N/R	N/R	N/R
PCI66_3			N/R	N/R	N/R
PCIX			N/R	N/R	N/R
SSTL3_I_DCI			1.5	N/R	Split
SSTL3_II_DCI			1.5	Split	Split
LVDS_25	2.5	N/R	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCMOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split

Table 5: **Summary of Voltage Supply Requirements for All Input and Output Standards *(Continued)***

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
HSTL_III_18	1.8	N/R	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVCMOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	N/R	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVCMOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTLP_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTL_DCI	1.2	1.2	0.8	Single	Single
GTLP	N/R	N/R	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:
1. N/R = no requirement.

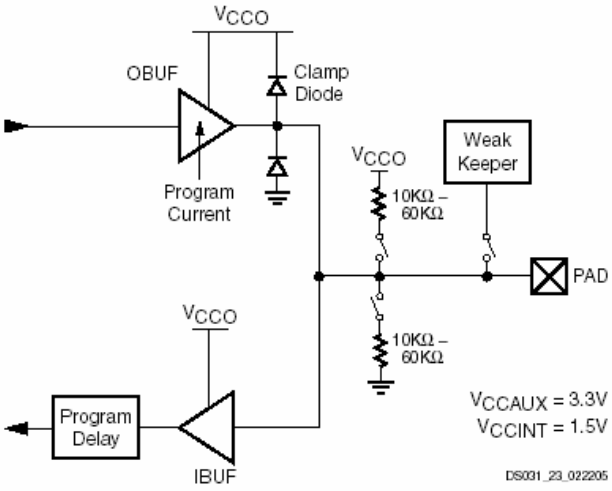


Figure 5: **LVTTL, LVCMOS or PCI SelectI/O-Ultra Standards**

Input/Output Individual Options

Each device pad has optional pull-up and pull-down in all SelectI/O-Ultra configurations. Each device pad has optional weak-keeper in LVTTL, LVCMOS, and PCI SelectI/O-Ultra configurations, as illustrated in Figure 5. Values of the optional pull-up and pull-down resistors are in the range 10 - 60 KΩ, which is the specification for V_{CCO} when operating at 3.3V (from 3.0 to 3.6V only). The clamp diode is always present, even when power is not.

The optional weak-keeper circuit is connected to each user I/O pad. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. An enabled pull-up or pull-down overrides the weak-keeper circuit.

LVTTL sinks and sources current up to 24 mA. The current is programmable for LVTTL and LVCMOS SelectI/O-Ultra standards (see Table 4). Drive-strength and slew-rate controls for each output driver, minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew-rate controls are not available.

Drive Current

Table 4: **LVTTL and LVCMOS Programmable Currents (Sink and Source)**

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Input/Output Blocks (IOBs)

IOB Overview

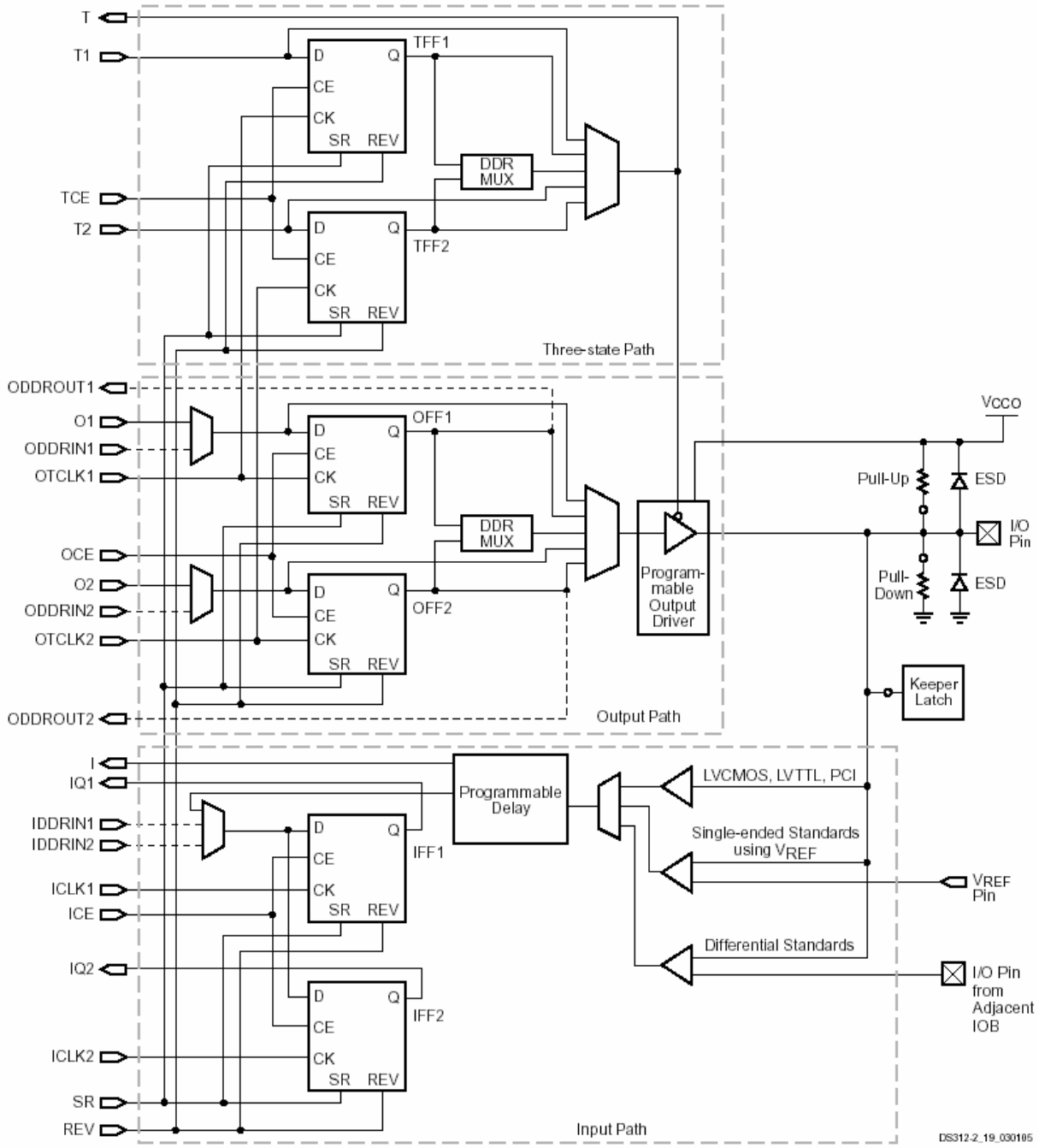
The Input/Output Block (IOB) provides a programmable, unidirectional or bidirectional interface between a package pin and the FPGA's internal logic. The IOB is similar to that of the Spartan-3 family with the following differences:

- Input-only blocks are added
- Programmable input delays are added to all blocks
- DDR flip-flops can be shared between adjacent IOBs

The unidirectional input-only block has a subset of the full IOB capabilities. Thus there are no connections or logic for an output path. The following paragraphs assume that any reference to output functionality does not apply to the input-only blocks. The number of input-only blocks varies with device size, but is never more than 25% of the total IOB count.

Figure 1, page 2 is a simplified diagram of the IOB's internal structure. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see **Storage Element Functions**. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. After the delay element, there are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 lead to the FPGA's internal logic. The delay element can be set to ensure a hold time of zero (see **Input Delay Functions**).
- The output path, starting with the O1 and O2 lines, carries data from the FPGA's internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA's internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.



Notes:

1. All IOB signals communicating with the FPGA's internal logic have the option of inverting polarity inside the IOB.
2. Signals shown with dashed lines connect to the adjacent IOB in a differential pair only, not to the FPGA fabric.

Figure 1: **Simplified IOB Diagram**

Input Delay Functions

Each IOB has a programmable delay block that can delay the input signal from 0 to nominally 4000 ps. In Figure 2, the signal is first delayed by either 0 or 2000 ps (nominal) and is then applied to an 8 tap delay line. This delay line has a nominal value of 250 ps per tap. All 8 taps are available via a multiplexer for use as an asynchronous input directly into the FPGA fabric. In this way, the delay is programmable from 0 to 4000 ps in 250 ps steps. Four of the 8 taps are also available via a multiplexer to the D inputs of the synchronous storage elements. The delay inserted in the path to the storage element can be varied from 0 to 4000 ps in 500 ps steps. The first, coarse delay element is common to both asynchronous and synchronous paths, and must be either used or not used for both paths.

The delay values are set up in the silicon once at configuration time—they are non-modifiable in device operation.

The primary use for the input delay element is as an adequate delay to ensure that there is no hold time requirement when using the input flip-flop(s) with a global clock. The necessary value for this function is chosen by the Xilinx software tools and depends on device size. If the design is using a DCM in the clock path, then the delay element can be safely set to zero in the user's design, and there is still no hold time requirement.

Both asynchronous and synchronous values can be modified by the user, which is useful where extra delay is required on clock or data inputs, for example, in interfaces to various types of RAM.

See Module 3 of the Spartan-3E data sheet for exact values for the delay elements.

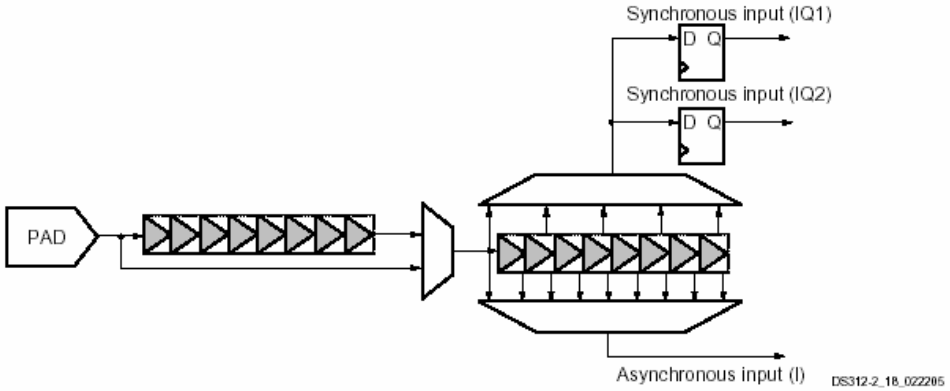


Figure 2: **Input Delay Elements**

Supported Standards

Table 3: **Single-Ended IOSTANDARD Bank Compatibility**

Single-Ended IOSTANDARD	V_{CCO} Supply/Compatibility						Input Requirements	
	1.2 V	1.5 V	1.8 V	2.5 V	3.0 V	3.3 V	V_{REF} for Inputs	Board Termination Voltage (V_{TT})
LVTTL	-	-	-	-	-	Input/ Output	N/R	N/R
LVCMOS33	-	-	-	-	-	Input/ Output	N/R	N/R
LVCMOS25	-	-	-	Input/ Output	Input	Input	N/R	N/R
LVCMOS18	-	-	Input/ Output	Input	Input	Input	N/R	N/R
LVCMOS15	-	Input/ Output	Input	Input	Input	Input	N/R	N/R
LVCMOS12	Input/ Output	Input	Input	Input	Input	Input	N/R(1)	N/R
PCI33_3	-	-	-	-	Input/ Output	Input	N/R	N/R
PCI66_3	-	-	-	-	Input/ Output	Input	N/R	N/R
PCIX					Input/ Output	Input	N/R	N/R
HSTL_I_18	-	-	Input/ Output	Input	Input	Input	0.9	0.9
HSTL_III_18	-	-	Input/ Output	Input	Input	Input	1.1	1.8
SSTL18_I	-	-	Input/ Output	Input	Input	Input	0.9	0.9
SSTL2_I	-	-	-	Input/ Output	Input	Input	1.25	1.25

Notes:

1. N/R - Not required for input operation.

Keeper Circuit

Each I/O has an optional keeper circuit (see Figure 9) that keeps bus lines from floating when not being actively driven. The KEEPER circuit retains the last logic level on a line after all drivers have been turned off. Apply the KEEPER attribute or use the KEEPER library primitive to use the KEEPER circuitry. Pull-up and pull-down resistors override the KEEPER settings.

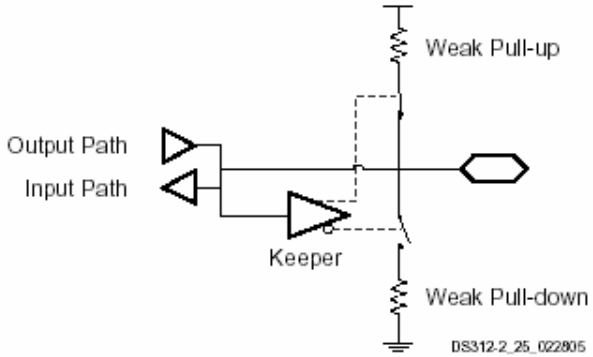


Figure 9: **Keeper Circuit**

Drive Current

Table 5: **Programmable Output Drive Current**

Signal Standard	Output Drive Current (mA)					
	2	4	6	8	12	16
LVTTL	✓	✓	✓	✓	✓	✓
LVCMOS33	✓	✓	✓	✓	✓	✓
LVCMOS25	✓	✓	✓	✓	✓	-
LVCMOS18	✓	✓	✓	✓	-	-
LVCMOS15	✓	✓	✓	-	-	-
LVCMOS12	✓	-	-	-	-	-

Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting it to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (ODDR2).

Table 1 describes the signal paths associated with the storage element.

Table 1: **Storage Element Signal Description**

Storage Element Signal	Description	Function
D	Data input	Data at this input is stored on the active edge of CK and enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q.
Q	Data output	The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q mirrors the data at D.
CK	Clock input	Data is loaded into the storage element on this input's active edge with CE asserted.
CE	Clock Enable input	When asserted, this input enables CK. If not connected, CE defaults to the asserted state.
SR	Set/Reset input	This input forces the storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0.
REV	Reverse input	This input is used together with SR. It forces the storage element into the state opposite from what SR does. The SYNC/ASYNC attribute setting determines whether the REV input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0.

As shown in Figure 1, the upper registers in both the output and three-state paths share a common clock. The OTCLK1 clock signal drives the CK clock inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 drives the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2.

The OCE enable line controls the CE inputs of the upper and lower registers on the output path. Similarly, TCE controls the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path.

The Set/Reset (SR) line entering the IOB controls all six registers, as is the Reverse (REV) line.

In addition to the signal polarity controls described in **IOB Overview**, each storage element additionally supports the controls described in Table 2.

References

[1] Literature: Stratix Device Handbook at http://www.altera.com/literature/lit-stx.jsp

[2] Literature: Stratix II Devices at http://www.altera.com/literature/lit-stx2.jsp

[3] Virtex-II Data Sheets at http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?sGlobalNavPick=&sSecondaryNavPick=&category=-18774&iLanguageID=1

[4] Spartan-3E Data Sheets at http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?sGlobalNavPick=&sSecondaryNavPick=&category=-1211389&iLanguageID=1