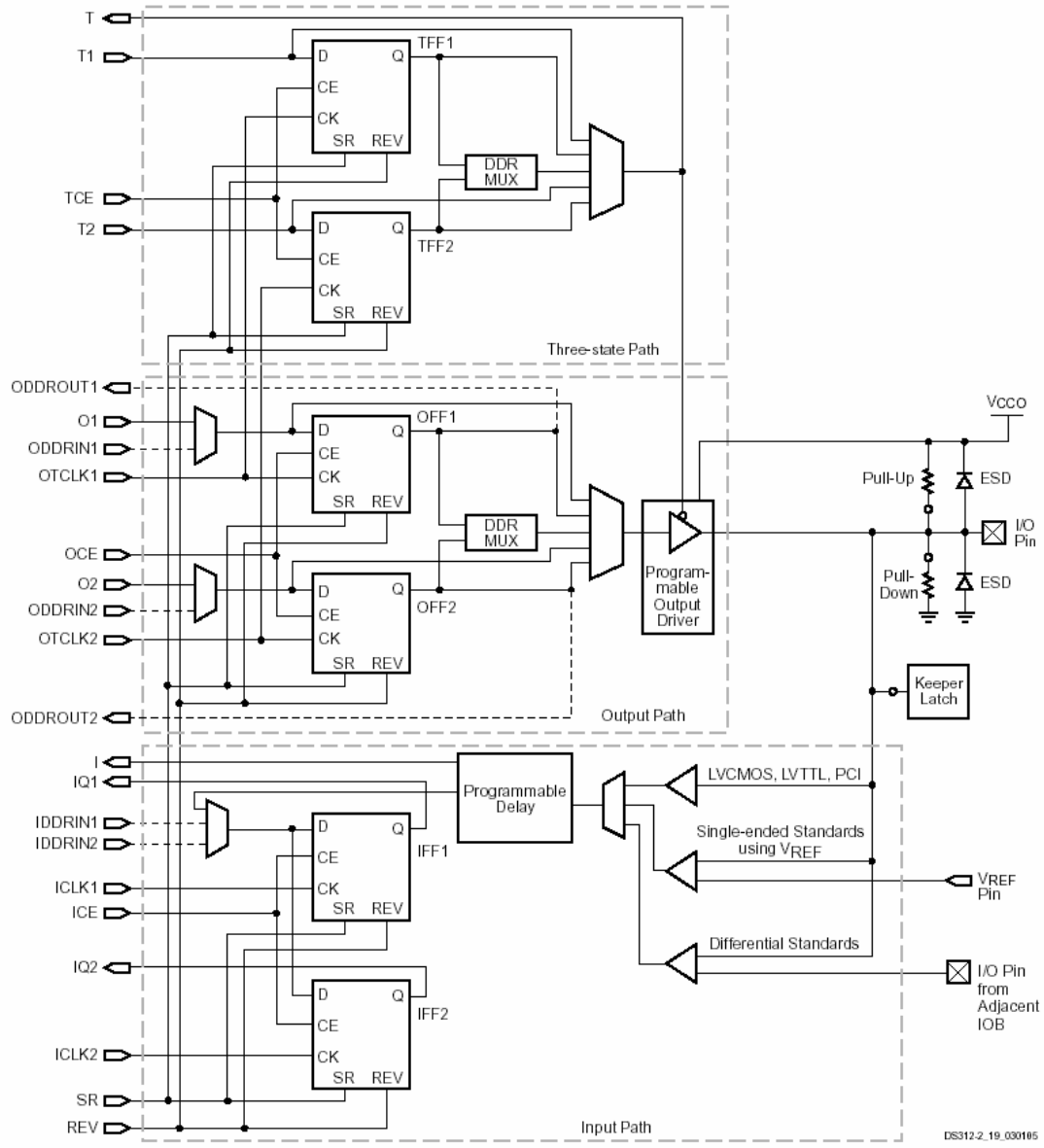
Typical I/O standards for general purpose

I/O Standard	Application	Voltage	Drive Current (mA)[1]	Performance (MHZ)
LVTTL (Low Voltage Transistor-Transistor Logic)	General Purpose	3.3v	24, 16, 12, 8, 4	350
		2.5v	16, 12, 8, 2	350
		1.8v	12, 8, 2	250
LVCMOS (Low Voltage CMOS)	General Purpose	3.3v	24, 12, 8, 4, 2	350
		2.5v	16, 12, 8, 2	350
		1.8v	12, 8, 2	250
		1.5v	8, 4, 2	225

(1) Programmable Output Drive Current may differ from Altera to Xilinx FPGA chip. Here shows the Altera Stratix spec.

Diagram of IOB from Xilinx Spartan-3



Notes:

1. All IOB signals communicating with the FPGA's internal logic have the option of inverting polarity inside the IOB.
2. Signals shown with dashed lines connect to the adjacent IOB in a differential pair only, not to the FPGA fabric.

Figure 1: **Simplified IOB Diagram**

Input Delay Circuit from Xilinx Spartan-3

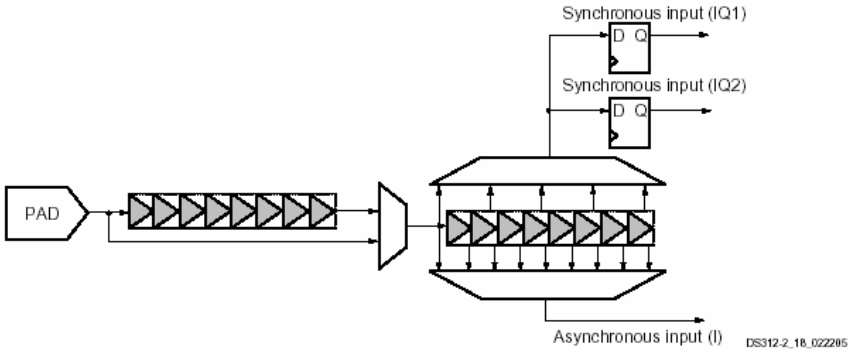


Figure 2: **Input Delay Elements**

Keeper Circuit from Xilinx Spartan-3

Keeper Circuit

Each I/O has an optional keeper circuit (see Figure 9) that keeps bus lines from floating when not being actively driven. The KEEPER circuit retains the last logic level on a line after all drivers have been turned off. Apply the KEEPER attribute or use the KEEPER library primitive to use the KEEPER circuitry. Pull-up and pull-down resistors override the KEEPER settings.

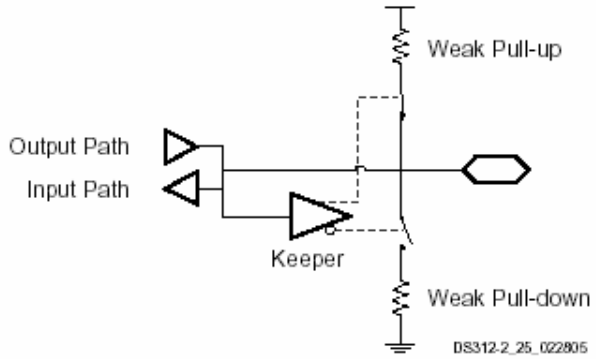


Figure 9: **Keeper Circuit**