Typical I/O standards for general purpose

I/O Standard	Application	Voltage	Drive Current	Performance
		-	$(mA)^{l}$	(MHZ)
LVTTL	General	3.3v	24, 16, 12, 8, 4	350
(Low Voltage	Purpose	2.5v	16, 12, 8, 2	350
Transistor-Transistor		1.8v	12, 8, 2	250
Logic)				
LVCMOS	General	3.3v	24, 12, 8, 4, 2	350
(Low Voltage CMOS)	Purpose	2.5v	16, 12, 8, 2	350
		1.8v	12, 8, 2	250
		1.5v	8, 4, 2	225

(1) Programmable Output Drive Current may differ from Altera to Xilinx FPGA chip. Here shows the Altera Stratix spec.

Diagram of IOB from Xilinx Spartan-3

Functional Description

T TFF1 Q T1 🗖 D CE ск REV SR Т DDR TCE 🗩 D T2 🗖 Q TFF2 CE ск SR REV Three-state Path ODDROUT1 🗲 _____ Vcco OFF1 01 🗖 D Q ODDRIN1 🕞 CE OTCLK1 🗖 Pull-Up 💈 **太** ESD СК SR REV DDR MUX - 🛛 1/0 Pin OCE 🗩 ^orogram mable Pull-**太** esd 02 Q D Output Driver ODDRIN2 🗩 OFF2 CE 4 OTCLK2 🕞 СК SR REV Keeper Latch o Output Path ODDROUT2 🗢 LVCMOS, LVTTL, PCI Programmable Delay IDDRIN1 🕞 Q Single-ended Standards using V_{REF} D IFF1 CE C VREF Pin ICLK1 🗩 ск SR REV ICE 🕞 Differential Standards -X I/O Pin from Adjacent IOB IQ2 🗢 D Q IFF2 CE ICLK2 🗖 СК SR REV SR 🗩 REV 🗩 Input Path DS312-2_19_030105

Notes:

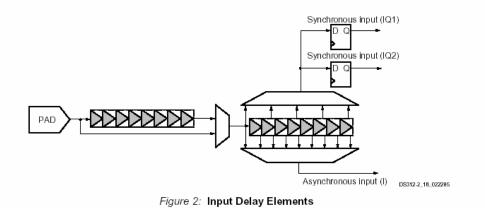
All IOB signals communicating with the FPGA's internal logic have the option of inverting polarity inside the IOB. Signals shown with dashed lines connect to the adjacent IOB in a differential pair only, not to the FPGA fabric. 1.

2.

Figure 1: Simplified IOB Diagram

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Input Delay Circuit from Xilinx Spartan-3



Keeper Circuit from Xilinx Spartan-3

Keeper Circuit

Each I/O has an optional keeper circuit (see Figure 9) that keeps bus lines from floating when not being actively driven. The KEEPER circuit retains the last logic level on a line after all drivers have been turned off. Apply the KEEPER attribute or use the KEEPER library primitive to use the KEEPER circuitry. Pull-up and pull-down resistors override the KEEPER settings.

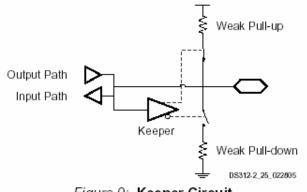


Figure 9: Keeper Circuit