Virtex-4 Data Sheet: DC and Switching Characteristics

DS302 (v1.4) February 24, 2005

Preliminary Product Specification

Virtex-4 Electrical Characteristics

Virtex-4™ FPGAs are available in -12, -11, -10 speed grades, with -12 having the highest performance.

Virtex-4 DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -10 speed grade industrial device are the same as for a -10 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-4 Data Sheet, part of an overall set of documentation on the Virtex-4 family of FPGAs, is available on the Xilinx web site:

- Virtex-4 Family Overview
- Virtex-4 User Guide
- Virtex-4 Configuration Guide
- XtremeDSP Design Considerations
- Virtex-4 Packaging Specification
- PCB Designers Guide
- Virtex-4 RocketIO Multi-Gigabit Transceiver Guide
- Tri-mode Ethernet Media Access Controller
- PowerPC™ 405 Processor Block Reference Guide

All specifications are subject to change without notice.

Virtex-4 DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.05	V
V_{REF}	Input reference voltage	–0.3 to 3.75	V
V_{IN}(3)	3.3V I/O input voltage relative to GND (user and dedicated I/Os)	–0.3 to 4.05	V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 3.3V output (user and dedicated I/Os)	–0.3 to 4.05	V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(2)	+220	°C
T_J	Maximum junction temperature(2)	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the *Virtex-4 Packaging Specifications* on the Xilinx website.
3. 3.3V I/O absolute maximum limit applied to DC and AC signals.
4. For 3.3V I/O operation, refer to the *Virtex-4 User Guide*.

Table 2: **Recommended Operating Conditions**

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0° C to +85° C	Commercial	1.14	1.26	V
	Internal supply voltage relative to GND, T_J = –40° C to +100° C	Industrial	1.14	1.26	V
V_{CCAUX}(1)	Auxiliary supply voltage relative to GND, T_J = 0° C to +85° C	Commercial	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_J = –40° C to +100° C	Industrial	2.375	2.625	V
V_{CCO}(2,4,5)	Supply voltage relative to GND, T_J = 0° C to +85° C	Commercial	1.14	3.45	V
	Supply voltage relative to GND, T_J = –40° C to +100° C	Industrial	1.14	3.45	V
V_{IN}	3.3V supply voltage relative to GND, T_J = 0° C to +85° C	Commercial	GND – 0.20	3.45	V
	3.3V supply voltage relative to GND, T_J = –40° C to +100° C	Industrial	GND – 0.20	3.45	V
	2.5V and below supply voltage relative to GND, T_J = 0° C to +85° C	Commercial	GND – 0.20	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_J = –40° C to +100° C	Industrial	GND – 0.20	V_{CCO} + 0.2	V
V_{BATT}(3)	Battery voltage relative to GND, T_J = 0° C to +85° C	Commercial	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40° C to +100° C	Industrial	1.0	3.6	V

Notes:
1. Recommended maximum voltage drop for V_{CCAUX} is 10 mV/ms.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
4. For 3.3V I/O operation, refer to the *Virtex-4 User Guide*.
5. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.9			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0			V
I_{REF}	V_{REF} current per pin			10	µA
I_L	Input or output leakage current per pin (sample-tested)			10	µA
C_{IN}	Input capacitance (sample-tested)			10	pF
I_{RPU}(1)	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V			185	µA
I_{RPD}(1)	Pad pull-down (when selected) @ V_{IN} = 2.5V			185	µA
I_{BATT}(1)	Battery supply current		75		nA

Notes:
1. Typical values are specified at nominal voltage, 25°C.

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Typ(1)	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC4VLX15	46		mA
		XC4VLX25	77		mA
		XC4VLX40	121		mA
		XC4VLX60	167		mA
		XC4VLX80	220		mA
		XC4VLX100	292		mA
		XC4VLX160	384		mA
		XC4VLX200	489		mA
		XC4VSX25	94		mA
		XC4VSX35	140		mA
		XC4VSX55	271		mA
		XC4VFX12	47		mA
		XC4VFX20	71		mA
		XC4VFX40	139		mA
		XC4VFX60	203		mA
		XC4VFX100	311		mA
		XC4VFX140	442		mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC4VLX15	1.25		mA
		XC4VLX25	1.25		mA
		XC4VLX40	1.25		mA
		XC4VLX60	1.5		mA
		XC4VLX80	1.5		mA
		XC4VLX100	1.75		mA
		XC4VLX160	2.5		mA
		XC4VLX200	2.5		mA
		XC4VSX25	1.25		mA
		XC4VSX35	1.25		mA
		XC4VSX55	1.5		mA
		XC4VFX12	1.25		mA
		XC4VFX20	1.25		mA
		XC4VFX40	1.25		mA
		XC4VFX60	1.5		mA
		XC4VFX80	1.5		mA
		XC4VFX100	1.75		mA
		XC4VFX140	2.5		mA

Table 4: **Quiescent Supply Current *(Continued)***

Symbol	Description	Device	Typ(1)	Max	Units
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC4VLX15	31		mA
		XC4VLX25	36		mA
		XC4VLX40	43		mA
		XC4VLX60	74		mA
		XC4VLX80	83		mA
		XC4VLX100	95		mA
		XC4VLX160	133		mA
		XC4VLX200	150		mA
		XC4VSX25	62		mA
		XC4VSX35	70		mA
		XC4VSX55	91		mA
		XC4VFX12	31		mA
		XC4VFX20	35		mA
		XC4VFX40	69		mA
		XC4VFX60	80		mA
		XC4VFX100	98		mA
		XC4VFX140	143		mA

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Power Estimator or XPOWER™ tool.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

V_{CCAUX} and V_{CCO} can power on at any ramp rate. Power supplies can be turned on in any sequence, though V_{CCAUX} must powered on before or with V_{CCO} for the specifications shown in Table 5. Xilinx does not specify the current when V_{CCAUX} is not powered on first.

Table 5 shows the minimum current required by Virtex-4 devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the XPOWER™ tool to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-4 Devices**

Device	$I_{CCINTMIN}$		$I_{CCAUXMIN}$		I_{CCOMIN}		Units
	Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
XC4VLX15	110		56				mA
XC4VLX25	157		83				mA
XC4VLX40	226		111				mA
XC4VLX60	303		222				mA
XC4VLX80	388		278				mA
XC4VLX100	492		333				mA
XC4VLX160	684		500				mA
XC4VLX200	849		500				mA
XC4VSX25	174		111				mA
XC4VSX35	245		167				mA
XC4VSX55	407		222				mA
XC4VFX12	111		56				mA
XC4VFX20	151		56				mA
XC4VFX40	244		167				mA
XC4VFX60	339		222				mA
XC4VFX100	511		278				mA
XC4VFX140	702		500				mA

Notes:
1. Typical values are specified at nominal voltage, 25°C.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels**

Input/Output Standards	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.2	0.8	2.0	3.45	0.4	2.4	Note(3)	Note(3)
LVCMOS33	–0.2	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18	–0.3	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.3	0.4	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15	–0.3	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.3	0.4	V_{CCO} – 0.45	Note(4)	Note(4)
PCI33_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI66_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI-X(5)	–0.2	35% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
GTLP	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	–	0.6	N/A	36	n/a
GTL	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	–	0.4	N/A	32	n/a
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
HSTL IV(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	48	–8
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	0.5	V_{CCO} – 0.5	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	–	–

Notes:
1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33_3, PCI66_3, and PCIX refer to the *Virtex-4 User Guide*, *SelectIO Resources, Chapter 6*.

LDT DC Specifications (LDT_25)

Table 8: **LDT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15		15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OCM}	Change in V_{OS} Magnitude		–15		15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15		15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15		15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.602	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.898			V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	440	–	820	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-4 User Guide*: *Chapter 6, SelectIO Resources*.

Table 11: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{IH}	Input High Voltage	0.7 V_{CC}			V
V_{IL}	Input Low Voltage			0.3 V_{CC}	V
	Differential Input Voltage	0.100		1.5(1)	V

Notes:
1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-4 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the **Switching Characteristics**, page 11.

Table 12 provides pin-to-pin values including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 12: **Pin-to-Pin Performance**

Description	Device Used & Speed Grade	Pin-to-Pin (with I/O delays)	Units
Basic Functions			
16-bit Address Decoder			ns
32-bit Address Decoder			ns
64-bit Address Decoder			ns
4:1 Multiplexer			ns
8:1 Multiplexer			ns
16:1 Multiplexer			ns
32:1 Multiplexer			ns
Combinatorial (pad to LUT to pad)			ns
Memory			
Block RAM			
Pad to Setup			ns
Clock to Pad			ns
Distributed RAM			
Pad to Setup			ns
Clock to Pad		(no clock skew)	ns

Table 13 shows internal (register-to-register) performance.

Table 13: **Register-to-Register Performance**

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
Basic Functions			
16-bit Address Decoder			MHz
32-bit Address Decoder			MHz
64-bit Address Decoder			MHz
4:1 Multiplexer			MHz
8:1 Multiplexer			MHz
16:1 Multiplexer			MHz
32:1 Multiplexer			MHz
Register to LUT to Register			MHz
8-bit Adder			MHz
16-bit Adder			MHz
32-bit Adder			MHz
64-bit Adder			MHz
128-bit Adder			MHz
24-bit Counter			MHz
48-bit Counter			MHz
64-bit Counter			MHz
48-bit Accumulator			MHz
Multiplier 18 x 18 (with block RAM inputs)			MHz
Multiplier 18 x 18 (with register inputs)			MHz
Memory			
Cascaded block RAM (32K)			
Block RAM Non-Pipelined			
Single-Port 4096 x 4 bits			MHz
Single-Port 2048 x 9 bits			MHz
Single-Port 1024 x 18 bits			MHz
Single-Port 512 x 36 bits			MHz
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits			MHz
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits			MHz
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits			MHz

Table 13: **Register-to-Register Performance *(Continued)***

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
Block RAM Pipelined			
Single-Port 4096 x 4 bits			MHz
Single-Port 2048 x 9 bits			MHz
Single-Port 1024 x 18 bits			MHz
Single-Port 512 x 36 bits			MHz
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits			MHz
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits			MHz
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits			MHz
Distributed RAM			
Single-Port 16 x 8-bit			MHz
Single-Port 32 x 8-bit			MHz
Single-Port 64 x 8-bit			MHz
Dual-Port 16 x 8			MHz
Shift Register Chain			
16-bit		N/A	MHz
32-bit		N/A	MHz
64-bit		N/A	MHz
128-bit		N/A	MHz
256-bit		N/A	MHz
Dedicated Arithmetic Logic			
DSP48 48-bit Accumulator			MHz
48-bit Counter			MHz
DSP48 8-bit Adder			MHz
DSP48 16-bit Adder			MHz
DSP48 32-bit Adder			MHz
DSP48 48-bit/36-bit Adder			MHz
Pipelined Multiplier Block			MHz
DSP48 Based Multiplier 18 x 18 Pipelined			MHz
DSP48 Based Multiplier 35 x 35 Pipelined			MHz
DSP48 Direct 4-tap FIR Filter Pipelined			MHz
Systolic N-Tap Filter Pipelined			MHz
DSP48 Multiply Accumulate Pipelined			MHz

Table 14: **I/O and Interface Performances**

Description	Device Used & Speed Grade		
	-10	-11	-12
I/O			
Single-ended, CSE, DDR	400 Mb	540 Mb	600 Mb
LVDS	800 Mb	900 Mb	1 Gb
Clocking			
Maximum Clock Tree Frequency			
Networking Applications			
SFI-4.1 (SDR Interface)			
SFI-4.2 (DDR Interface)			
Memory Interfaces			
DDR			
DDR2			
QDR			
RLDRAM			

Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-4 device with a corresponding speed file version 1.52 designation.

Table 15: **Virtex-4 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC4VLX15	-11, -10		
XC4VLX25	-11, -10		
XC4VLX40	-11, -10		
XC4VLX60	-11, -10		
XC4VLX80	-11, -10		
XC4VLX100	-11, -10		
XC4VLX160	-11, -10		
XC4VLX200	-11, -10		

Table 15: **Virtex-4 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC4VSX25	-11, -10		
XC4VSX35	-11, -10		
XC4VSX55	-11, -10		
XC4VFX12	-11, -10		
XC4VFX20	-11, -10		
XC4VFX40	-11, -10		
XC4VFX60	-11, -10		
XC4VFX100	-11, -10		
XC4VFX140	-11, -10		

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-4 devices.

IOB Pad Input/Output/3-State Switching Characteristics

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 17 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 16: **IOB Switching Characteristics**

	T_{IOPI}			T_{IOOP}			T_{IOTP}			
Speed Grade	**-12**	**-11**	**-10**	**-12**	**-11**	**-10**	**-12**	**-11**	**-10**	**Units**
LVDS_25		1.15	1.28		1.29	1.44		1.29	1.44	ns
LVDSEXT_25		1.16	1.30		1.34	1.49		1.34	1.49	ns
LDT_25		1.15	1.28		1.26	1.40		1.26	1.40	ns
BLVDS_25		1.15	1.28		1.73	1.93		1.73	1.93	ns
ULVDS_25		1.15	1.28		1.27	1.41		1.27	1.41	ns
PCI33_3 (PCI, 33 MHz, 3.3V)		0.87	0.97		2.34	2.61		2.34	2.61	ns
PCI66_3 (PCI, 66 MHz, 3.3V)		0.87	0.97		2.34	2.61		2.34	2.61	ns
PCI-X		0.87	0.97		2.34	2.61		2.34	2.61	ns
GTL		1.47	1.63		2.31	2.57		2.31	2.57	ns
GTLP		1.51	1.68		3.59	3.99		3.59	3.99	ns
HSTL_I		1.47	1.64		1.64	1.82		1.64	1.82	ns
HSTL_II		1.47	1.64		1.25	1.39		1.25	1.39	ns

Table 16: **IOB Switching Characteristics *(Continued)***

	T_{IOPI}			T_{IOOP}			T_{IOTP}			
Speed Grade	**-12**	**-11**	**-10**	**-12**	**-11**	**-10**	**-12**	**-11**	**-10**	**Units**
HSTL_III		1.47	1.64		1.50	1.66		1.50	1.66	ns
HSTL_IV		1.47	1.64		1.33	1.47		1.33	1.47	ns
HSTL_I _18		1.44	1.60		1.66	1.85		1.66	1.85	ns
HSTL_II _18		1.44	1.60		1.39	1.54		1.39	1.54	ns
HSTL_III _18		1.44	1.60		1.50	1.66		1.50	1.66	ns
HSTL_IV_18		1.44	1.60		1.32	1.47		1.32	1.47	ns
SSTL2_I		1.51	1.68		1.95	2.17		1.95	2.17	ns
SSTL2_II		1.51	1.68		1.54	1.71		1.54	1.71	ns
LVTTL, Slow, 2 mA		0.87	0.97		7.76	8.63		7.76	8.63	ns
LVTTL, Slow, 4 mA		0.87	0.97		5.24	5.84		5.24	5.84	ns
LVTTL, Slow, 6 mA		0.87	0.97		4.25	4.72		4.25	4.72	ns
LVTTL, Slow, 8 mA		0.87	0.97		3.29	3.66		3.29	3.66	ns
LVTTL, Slow, 12 mA		0.87	0.97		2.78	3.09		2.78	3.09	ns
LVTTL, Slow, 16 mA		0.87	0.97		1.92	2.13		1.92	2.13	ns
LVTTL, Slow, 24 mA		0.87	0.97		1.92	2.13		1.92	2.13	ns
LVTTL, Fast, 2 mA		0.87	0.97		6.55	7.29		6.55	7.29	ns
LVTTL, Fast, 4 mA		0.87	0.97		3.61	4.01		3.61	4.01	ns
LVTTL, Fast, 6 mA		0.87	0.97		2.94	3.27		2.94	3.27	ns
LVTTL, Fast, 8 mA		0.87	0.97		1.87	2.08		1.87	2.08	ns
LVTTL, Fast, 12 mA		0.87	0.97		1.67	1.86		1.67	1.86	ns
LVTTL, Fast, 16 mA		0.87	0.97		1.44	1.61		1.44	1.61	ns
LVTTL, Fast, 24 mA		0.87	0.97		1.44	1.61		1.44	1.61	ns
LVCMOS33, Slow, 2 mA		0.87	0.97		7.47	8.31		7.47	8.31	ns
LVCMOS33, Slow, 4 mA		0.87	0.97		5.10	5.68		5.10	5.68	ns
LVCMOS33, Slow, 6 mA		0.87	0.97		4.12	4.59		4.12	4.59	ns
LVCMOS33, Slow, 8 mA		0.87	0.97		3.18	3.54		3.18	3.54	ns
LVCMOS33, Slow, 12 mA		0.87	0.97		2.70	3.00		2.70	3.00	ns
LVCMOS33, Slow, 16 mA		0.87	0.97		1.87	2.08		1.87	2.08	ns
LVCMOS33, Slow, 24 mA		0.87	0.97		1.87	2.08		1.87	2.08	ns
LVCMOS33, Fast, 2 mA		0.87	0.97		6.31	7.03		6.31	7.03	ns
LVCMOS33, Fast, 4 mA		0.87	0.97		3.52	3.92		3.52	3.92	ns
LVCMOS33, Fast, 6 mA		0.87	0.97		2.81	3.13		2.81	3.13	ns
LVCMOS33, Fast, 8 mA		0.87	0.97		1.84	2.05		1.84	2.05	ns
LVCMOS33, Fast, 12 mA		0.87	0.97		1.67	1.85		1.67	1.85	ns
LVCMOS33, Fast, 16 mA		0.87	0.97		1.50	1.67		1.50	1.67	ns

Table 16: **IOB Switching Characteristics *(Continued)***

	T_{IOPI}			T_{IOOP}			T_{IOTP}			
Speed Grade	**-12**	**-11**	**-10**	**-12**	**-11**	**-10**	**-12**	**-11**	**-10**	**Units**
LVCMOS33, Fast, 24 mA		0.87	0.97		1.50	1.67		1.50	1.67	ns
LVCMOS25, Slow, 2 mA		0.80	0.88		6.85	7.63		6.85	7.63	ns
LVCMOS25, Slow, 4 mA		0.80	0.88		4.77	5.31		4.77	5.31	ns
LVCMOS25, Slow, 6 mA		0.80	0.88		3.89	4.33		3.89	4.33	ns
LVCMOS25, Slow, 8 mA		0.80	0.88		2.97	3.31		2.97	3.31	ns
LVCMOS25, Slow, 12 mA		0.80	0.88		2.54	2.83		2.54	2.83	ns
LVCMOS25, Slow, 16 mA		0.80	0.88		1.91	2.12		1.91	2.12	ns
LVCMOS25, Slow, 24 mA		0.80	0.88		1.91	2.12		1.91	2.12	ns
LVCMOS25, Fast, 2 mA		0.80	0.88		5.59	6.23		5.59	6.23	ns
LVCMOS25, Fast, 4 mA		0.80	0.88		3.28	3.65		3.28	3.65	ns
LVCMOS25, Fast, 6 mA		0.80	0.88		2.50	2.79		2.50	2.79	ns
LVCMOS25, Fast, 8 mA		0.80	0.88		1.74	1.93		1.74	1.93	ns
LVCMOS25, Fast, 12 mA		0.80	0.88		1.43	1.59		1.43	1.59	ns
LVCMOS25, Fast, 16 mA		0.80	0.88		1.39	1.55		1.39	1.55	ns
LVCMOS25, Fast, 24 mA		0.80	0.88		1.39	1.55		1.39	1.55	ns
LVCMOS18, Slow, 2 mA		1.12	1.25		6.74	7.50		6.74	7.50	ns
LVCMOS18, Slow, 4 mA		1.12	1.25		5.10	5.68		5.10	5.68	ns
LVCMOS18, Slow, 6 mA		1.12	1.25		3.69	4.10		3.69	4.10	ns
LVCMOS18, Slow, 8 mA		1.12	1.25		3.73	4.15		3.73	4.15	ns
LVCMOS18, Slow, 12 mA		1.12	1.25		3.41	3.80		3.41	3.80	ns
LVCMOS18, Slow, 16 mA		1.12	1.25		2.37	2.64		2.37	2.64	ns
LVCMOS18, Fast, 2 mA		1.12	1.25		4.61	5.13		4.61	5.13	ns
LVCMOS18, Fast, 4 mA		1.12	1.25		2.64	2.93		2.64	2.93	ns
LVCMOS18, Fast, 6 mA		1.12	1.25		2.13	2.37		2.13	2.37	ns
LVCMOS18, Fast, 8 mA		1.12	1.25		2.03	2.26		2.03	2.26	ns
LVCMOS18, Fast, 12 mA		1.12	1.25		1.76	1.96		1.76	1.96	ns
LVCMOS18, Fast, 16 mA		1.12	1.25		1.50	1.67		1.50	1.67	ns
LVCMOS15, Slow, 2 mA		1.20	1.34		9.13	10.16		9.13	10.16	ns
LVCMOS15, Slow, 4 mA		1.20	1.34		6.85	7.63		6.85	7.63	ns
LVCMOS15, Slow, 6 mA		1.20	1.34		4.88	5.43		4.88	5.43	ns
LVCMOS15, Slow, 8 mA		1.20	1.34		4.55	5.07		4.55	5.07	ns
LVCMOS15, Slow, 12 mA		1.20	1.34		3.07	3.42		3.07	3.42	ns
LVCMOS15, Slow, 16 mA		1.20	1.34		3.03	3.37		3.03	3.37	ns
LVCMOS15, Fast, 2 mA		1.20	1.34		4.15	4.61		4.15	4.61	ns
LVCMOS15, Fast, 4 mA		1.20	1.34		3.46	3.85		3.46	3.85	ns

Table 16: **IOB Switching Characteristics *(Continued)***

	T_{IOPI}			T_{IOOP}			T_{IOTP}			
Speed Grade	**-12**	**-11**	**-10**	**-12**	**-11**	**-10**	**-12**	**-11**	**-10**	**Units**
LVCMOS15, Fast, 6 mA		1.20	1.34		2.54	2.83		2.54	2.83	ns
LVCMOS15, Fast, 8 mA		1.20	1.34		2.15	2.39		2.15	2.39	ns
LVCMOS15, Fast, 12 mA		1.20	1.34		1.75	1.94		1.75	1.94	ns
LVCMOS15, Fast, 16 mA		1.20	1.34		1.71	1.90		1.71	1.90	ns
LVDCI_33		0.87	0.97		2.44	2.72		2.44	2.72	ns
LVDCI_25		0.80	0.88		2.34	2.61		2.34	2.61	ns
LVDCI_18		1.12	1.25		2.28	2.54		2.28	2.54	ns
LVDCI_15		1.20	1.34		2.26	2.52		2.26	2.52	ns
LVDCI_DV2_25		0.80	0.88		1.66	1.85		1.66	1.85	ns
LVDCI_DV2_18		1.12	1.25		1.68	1.87		1.68	1.87	ns
LVDCI_DV2_15		1.20	1.34		1.95	2.17		1.95	2.17	ns
GTL_DCI		1.36	1.51		2.29	2.55		2.29	2.55	ns
GTLP_DCI		1.11	1.23		3.61	4.01		3.61	4.01	ns
HSTL_I_DCI		1.47	1.64		1.64	1.82		1.64	1.82	ns
HSTL_II_DCI		1.47	1.64		1.40	1.56		1.40	1.56	ns
HSTL_III_DCI		1.47	1.64		1.50	1.66		1.50	1.66	ns
HSTL_IV_DCI		1.47	1.64		3.06	3.40		3.06	3.40	ns
HSTL_I_DCI_18		1.44	1.60		1.66	1.85		1.66	1.85	ns
HSTL_II_DCI_18		1.44	1.60		1.39	1.54		1.39	1.54	ns
HSTL_III_DCI_18		1.44	1.60		1.50	1.66		1.50	1.66	ns
HSTL_IV_DCI_18		1.44	1.60		2.78	3.09		2.78	3.09	ns
SSTL2_I_DCI		1.51	1.68		1.84	2.05		1.84	2.05	ns
SSTL2_II_DCI		1.51	1.68		1.83	2.03		1.83	2.03	ns
LVPECL_25		1.59	1.77		1.19	1.32		1.19	1.32	ns
SSTL18_I		1.51	1.68		1.91	2.13		1.91	2.13	ns
SSTL18_II		1.51	1.68		1.64	1.83		1.64	1.83	ns
SSTL18_I_DCI		1.51	1.68		1.71	1.90		1.71	1.90	ns
SSTL18_II_DCI		1.51	1.68		1.59	1.77		1.59	1.77	ns

Table 17: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	**Description**	**Speed Grade**			**Units**
		-12	**-11**	**-10**	
T_{IOTPHZ}	T input to Pad high-impedance		1.01	1.12	ns

Input/Output Logic Switching Characteristics

Table 18: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK		0.66 –0.23	0.79 –0.25	ns
T_{ICECK}/T_{ICKCE}	DLYCE pin Setup/Hold with respect to CLKDIV		0.19 0.13	0.23 0.16	ns
T_{IRSTCK}/T_{ICKRST}	DLYRST pin Setup/Hold with respect to CLKDIV		–0.02 0.45	–0.02 0.54	ns
T_{IINCCK}/T_{ICKINC}	DLYINC pin Setup/Hold with respect to CLKDIV		0.01 0.43	0.01 0.51	ns
T_{ISRCK}/T_{ICKSR}	SR/REV pin Setup/Hold with respect to CLK		1.33 –0.59	1.59 –0.68	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay		0.28 –0.11	0.34 –0.13	ns
T_{IDOCKD}/T_{IOCKDD}	D pin Setup/Hold with respect to CLK (IOBDELAY_TYPE = DEFAULT)		6.14 –5.09	7.38 –6.11	ns
	D pin Setup/Hold with respect to CLK (IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)		1.06 –0.77	1.28 –0.93	ns
Combinatorial					
T_{IDI}	D pin to O pin propagation delay, no Delay		0.20	0.24	ns
T_{IDID}	D pin to O pin propagation delay (IOBDELAY_TYPE = DEFAULT)		5.42	6.50	ns
	D pin to O pin propagation delay (IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)		0.98	1.18	ns
Sequential Delays					
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay		0.59	0.71	ns
T_{IDLOD}	D pin to Q1 pin using flip-flop as a latch (IOBDELAY_TYPE = DEFAULT)		6.45	7.75	ns
	D pin to Q1 pin using flip-flop as a latch (IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)		1.37	1.65	ns
T_{ICKQ}	CLK to Q outputs		0.60	0.72	ns
T_{ICE1Q}	CE1 pin to Q1 using flip-flop as a latch, propagation delay		1.06	1.27	ns
T_{RQ}	SR/REV pin to OQ/TQ out		2.03	2.44	ns
T_{GSRQ}	Global Set/Reset to Q outputs		1.73	2.03	ns
Set/Reset					
T_{RPW}	Minimum Pulse Width, SR/REV inputs		0.59	0.70	ns, Min

Table 19: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK		0.62 –0.23	0.75 –0.28	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK		0.64 –0.36	0.77 –0.43	ns
T_{OSRCK}/T_{OCKSR}	SR/REV pin Setup/Hold with respect to CLK		1.18 –0.55	1.42 –0.61	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK		0.62 –0.23	0.75 –0.28	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK		0.64 –0.36	0.77 –0.43	ns
Combinatorial					
T_{ODQ}	D1 to OQ out		0.65	0.76	ns
T_{OTQ}	T1 to TQ out		0.65	0.76	ns
Sequential Delays					
T_{IOSRON}	REV pin to TQ out		1.37	1.64	ns
T_{OCKQ}	CLK to OQ/TQ out		0.49	0.59	ns
T_{RQ}	SR/REV pin to OQ/TQ out		1.37	1.64	ns
T_{GSRQ}	Global Set/Reset to Q outputs		1.73	2.03	ns
Set/Reset					
T_{RPW}	Minimum Pulse Width, SR/REV inputs		0.59	0.70	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 20: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Setup/Hold for Control Lines					
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV		0.34 –0.16	0.40 –0.13	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)		0.57 –0.30	0.69 –0.25	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)		0.14 –0.03	0.16 –0.02	ns
T_{ISCCK_DLYCE} / T_{ISCKC_DLYCE}	DLYCE pin Setup/Hold with respect to CLKDIV		0.19 0.13	0.23 0.16	ns
T_{ISCCK_DLYINC}/ T_{ISCKC_DLYINC}	DLYINC pin Setup/Hold with respect to CLKDIV		0.01 0.43	0.01 0.51	ns
T_{ISCCK_DLYRST}/ T_{ISCKC_DLYRST}	DLYRST pin Setup/Hold with respect to CLKDIV		–0.02 0.45	–0.02 0.54	ns
T_{ISCCK_REV}	REV pin Setup with respect to CLK		1.03	1.23	ns
T_{ISCCK_SR}	SR pin Setup with respect to CLKDIV		0.77	0.92	ns
Setup/Hold for Data Lines					
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK (IOBDELAY = IBUF or NONE)		0.28 –0.14	0.34 –0.17	ns
	D pin Setup/Hold with respect to CLK (IOBDELAY = IFD or BOTH, IOBDELAY_TYPE = DEFAULT)		6.05 –5.90	7.27 –7.09	ns
	D pin Setup/Hold with respect to CLK(1) (IOBDELAY = IFD or BOTH, IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)		0.97 –0.82	1.17 –0.99	ns
T_{ISDCK_DDR} /T_{ISCKD_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (IOBDELAY = IBUF or NONE)		0.28 –0.14	0.34 –0.17	ns
	D pin Setup/Hold with respect to CLK at DDR mode (IOBDELAY = IFD or BOTH, IOBDELAY_TYPE = DEFAULT)		6.05 –5.90	7.27 –7.09	ns
	D pin Setup/Hold with respect to CLK at DDR mode(1) (IOBDELAY = IFD or BOTH, IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)		0.97 –0.82	1.17 –0.99	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin		0.71	0.85	ns
Propagation Delays					
$T_{ISDO\_DO\_IOBDELAY\_IFD}$	D input to DO output pin (IOBDELAY = IFD)		0.20	0.24	ns
$T_{ISDO\_DO\_IOBDELAY\_NONE}$	D input to DO output pin (IOBDELAY = NONE)		0.20	0.24	ns

Table 20: **ISERDES Switching Characteristics *(Continued)***

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
$T_{ISDO\_DO\_IOBDELAY\_BOTH}$	D input to DO output pin (IOBDELAY = BOTH, IOBDELAY_TYPE = DEFAULT)		5.32	6.39	ns
	D input to DO output pin(1) (IOBDELAY = BOTH, IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)		0.89	1.07	ns
$T_{ISDO\_DO\_IOBDELAY\_IBUF}$	D input to DO output pin (IOBDELAY = IBUF, IOBDELAY_TYPE = DEFAULT)		5.32	6.39	ns
	D input to DO output pin(1) (IOBDELAY = IBUF, IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)		0.89	1.07	ns

Notes:
1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRCE report.

Input Delay Switching Characteristics

Table 21: **Input Delay Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
$T_{IDELAYRESOLUTION}$	IDELAY Chain Delay Resolution		75	75	ps
$T_{IDELAYCTRLCO\_RDY}$	Reset to Ready for IDELAYCTRL		3.00	3.00	µs
$F_{IDELAYCTRL\_REF}$	REFCLK frequency		200	200	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision		±1000	±1000	ppm
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width		50.0	50.0	ns

Output Serializer/Deserializer Switching Characteristics

Table 22: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Setup/Hold					
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV		0.42 –0.04	0.50 –0.03	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK		0.52 –0.19	0.62 –0.23	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV		0.42 –0.04	0.50 –0.03	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK		0.53 0.02	0.64 0.03	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV		0.80	0.96	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK		0.53 0.02	0.64 0.03	ns
Sequential Delays					
T_{OSCKO_OQ}	Clock to out from CLK to OQ		0.49	0.59	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ		0.49	0.59	ns
Combinatorial					
T_{OSDO_TTQ}	T input to TQ Out		0.65	0.76	ns
T_{OSCO_OQ}	Asynchronous Reset to OQ		1.37	1.64	ns
T_{OSCO_TQ}	Asynchronous Reset to TQ		1.37	1.64	ns

Notes:
1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRCE report.

CLB Switching Characteristics

Table 23: **CLB Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Combinatorial Delays					
T_{ILO}	4-input function: F/G inputs to X/Y outputs		0.17	0.20	ns, Max
T_{IF5}	5-input function: F/G inputs to F5 output		0.40	0.46	ns, Max
T_{IF5X}	5-input function: F/G inputs to X output		0.49	0.57	ns, Max
T_{IF6Y}	FXINA or FXINB inputs to YMUX output		0.34	0.39	ns, Max
T_{INAFX}	FXINA input to FX output via MUXFX		0.23	0.27	ns, Max
T_{INBFX}	FXINB input to FX output via MUXFX		0.23	0.26	ns, Max
T_{BXX}	BX input to XMUX output		0.65	0.76	ns, Max
T_{BYY}	BY input to YMUX output		0.48	0.56	ns, Max
T_{BXCY}	BX input to C_{OUT} output – Getting into carry chain(2)		0.66	0.78	ns, Max
T_{BYCY}	BY input to C_{OUT} output – Getting into carry chain(2)		0.54	0.63	ns, Max
T_{BYP}	C_{IN} input to C_{OUT} output – Carry chain delay(2)		0.08	0.09	ns, Max
T_{OPCYF}	F input to C_{OUT} output – Getting out from carry chain(2)		0.50	0.58	ns, Max
T_{OPCYG}	G input to C_{OUT} output – Getting out from carry chain(2)		0.48	0.57	ns, Max
Sequential Delays					
T_{CKO}	FF Clock CLK to XQ/YQ outputs		0.31	0.36	ns, Max
T_{CKLO}	Latch Clock CLK to XQ/YQ outputs		0.41	0.48	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T_{DICK}/T_{CKDI}	BX/BY inputs		0.28 0.09	0.33 0.11	ns, Min
T_{CECK}/T_{CKCE}	CE input		0.52 0.00	0.61 0.00	ns, Min
T_{FXCK}/T_{CKFX}	FXINA/FXINB inputs		0.35 0.04	0.41 0.05	ns, Min

Table 23: **CLB Switching Characteristics *(Continued)***

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
T_{SRCK}/T_{CKSR}	SR/BY inputs (synchronous)		1.03 –0.58	1.21 –0.62	ns, Min
T_{CINCK}/T_{CKCIN}	C_{IN} Data Inputs (DI) – Getting out from carry chain(2)		0.45 –0.05	0.53 –0.06	ns, Min
Set/Reset					
T_{RPW}	Minimum Pulse Width, SR/BY inputs		0.59	0.70	ns, Min
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)		1.15	1.35	ns, Max
F_{TOG}	Toggle Frequency (MHz) (for export control)		1205	1028	MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 24: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Sequential Delays					
T_{SHCKO}	Clock CLK to X outputs (WE active)		1.77	2.08	ns, Max
$T_{SHCKOF5}$	Clock CLK to F5 output (WE active)		1.69	1.98	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS}/T_{DH}	BX/BY data inputs (DI)		0.84 –0.31	1.07 –0.37	ns, Min
T_{AS}/T_{AH}	F/G address inputs		0.85 0.25	1.00 0.29	ns, Min
T_{WS}/T_{WH}	WE input (SR)		0.59 0.19	0.70 0.22	ns, Min
Clock CLK					
T_{WPH}	Minimum Pulse Width, High		0.59	0.69	ns, Min
T_{WPL}	Minimum Pulse Width, Low		0.60	0.70	ns, Min
T_{WC}	Minimum clock period to meet address write cycle time		0.84	0.98	ns, Min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRCE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 25: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Sequential Delays					
T_{REG}	Clock CLK to X/Y outputs		2.19	2.57	ns, Max
T_{REGXB}	Clock CLK to XB output via MC15 LUT output		1.74	2.04	ns, Max
T_{REGYB}	Clock CLK to YB output via MC15 LUT output		1.85	2.17	ns, Max
T_{CKSH}	Clock CLK to Shiftout		1.70	1.99	ns, Max
T_{REGF5}	Clock CLK to F5 output		2.11	2.47	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{WS}/T_{WH}	WE input (SR)		0.34 –0.17	0.39 –0.16	ns, Min
T_{DS}/T_{DH}	BX/BY data inputs (DI)		0.83 –0.55	1.02 –0.65	ns, Min
Clock CLK					
T_{WPH}	Minimum Pulse Width, High		0.59	0.69	ns, Min
T_{WPL}	Minimum Pulse Width, Low		0.60	0.70	ns, Min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 26: **Block RAM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Sequential Delays					
T_{RCKO_DORA}	Clock CLK to DOUT output (without output register)(2)		1.83	2.10	ns, Max
T_{RCKO_DOA}	Clock CLK to DOUT output (with output register)(3)		0.80	0.92	ns, Min
Setup and Hold Times Before Clock CLK					
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs		0.37 0.28	0.43 0.33	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(4)		0.20 0.28	0.23 0.33	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	EN input		0.45 0.28	0.52 0.33	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register		0.27 0.28	0.32 0.33	ns, Min
$T_{RCCK\_SSR}/T_{RCKC\_SSR}$	RST input		0.27 0.28	0.32 0.33	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	WEN input		0.65 0.28	0.75 0.33	ns, Min
Maximum Frequency					
F_{MAX}	Write first and no change mode		450	400	MHz
F_{MAX}	Read first mode		450	400	MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{RCKO_DORA} includes T_{RCKO_DOWA}, T_{RCKO_DOPAR}, and T_{RCKO_DOPAW} as well as the B port equivalent timing parameters.
3. T_{RCKO_DOA} includes T_{RCKO_DOPA} as well as the B port equivalent timing parameters..
4. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.

Table 27: **FIFO Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Sequential Delays					
T_{FCKO_DO}	Clock CLK to DO output (2)		0.80	0.92	ns, Max
T_{FCKO_FLAGS}	Clock CLK to FIFO flags outputs (3)		1.04	1.19	ns, Max
$T_{FCKO\_POINTERS}$	Clock CLK to FIFO pointer outputs (4)		1.29	1.48	ns, Max
Setup and Hold Times Before Clock CLK					
T_{FDCK_DI}/T_{FCKD_DI}	DI input (5)		0.20 0.28	0.23 0.33	ns, Min
T_{FCCK_EN}/T_{FCKC_EN}	Enable inputs (6)		0.73 0.28	0.84 0.33	ns, Min
Reset Delays					
T_{FCO_FLAGS}	Reset RST to FLAGS (7)		1.46	1.68	ns, Max
Maximum Frequency					
F_{MAX}	FIFO in all modes		450	400	MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{FCKO_DO} includes parity output (T_{FCKO_DOP}).
3. T_{FCKO_FLAGS} includes the following parameters: T_{FCKO_AEMPTY}, T_{FCKO_AFULL}, T_{FCKO_EMPTY}, T_{FCKO_FULL}, T_{FCKO_RDERR}, T_{FCKO_WRERR}.
4. $T_{FCKO\_POINTERS}$ includes both $T_{FCKO\_RDCOUNT}$ and $T_{FCKO\_WRCOUNT}$.
5. T_{FDCK_DI} includes parity inputs (T_{FDCK_DIP}).
6. T_{FCCK_EN} includes both WRITE and READ enable.
7. T_{FCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT and WRCOUNT.

XtremeDSP™ Switching Characteristics

Table 28: **XtremeDSP Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Setup and Hold of CE Pins					
$T_{DSPCCK\_CE}/T_{DSPCKC\_CE}$	Setup/Hold of all CE inputs of the DSP48 slice		0.43 0.10	0.49 0.12	ns
$T_{DSPCCK\_RST}/T_{DSPCKC\_RST}$	Setup/Hold of all RST inputs of the DSP48 slice		0.36 0.10	0.40 0.12	ns
Setup and Hold Times of Data					
$T_{DSPDCK\_\{AA, BB, CC\}}$/ $T_{DSPCKD\_\{AA, BB, CC\}}$	Setup/Hold of {A, B, C} input to {A, B, C} register		0.28 0.26	0.32 0.29	ns
$T_{DSPDCK\_\{AM, BM\}}$/ $T_{DSPCKD\_\{AM, BM\}}$	Setup/Hold of {A, B} input to M register		2.03 0.00	2.28 0.00	ns
Sequential Delays					
T_{DSPCKO_PP}	Clock to out from P register to P output		0.71	0.79	ns
T_{DSPCKO_PM}	Clock to out from M register to P output		2.65	2.98	ns
Combinatorial					
$T_{DSPDO\_\{AP, BP\}L}$	{A, B} input to P output (LEGACY_MODE = MULT18X18)		3.92	4.41	ns
Maximum Frequency					
F_{MAX}	From {A, B} register to P register (LEGACY_MODE = MULT18X18)		285.7	253.9	MHz
	Fully Pipelined		450	400	MHz

Configuration Switching Characteristics

Table 29: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Power-up Timing Characteristics					
T_{PL}	Program Latency		0.5	0.5	µs/frame Max
T_{POR}	Power-on-Reset		T_{PL} + 10	T_{PL} + 10	ms, Max
T_{ICCK}	CCLK (output) delay		500	500	ns, Min
$T_{PROGRAM}$	Program Pulse Width		300	300	ns, Max
Master/Slave Serial Mode Programming Switching					
T_{DCC}/T_{CCD}	DIN Setup/Hold, slave mode		0.5 1.0	0.5 1.0	ns, Min
T_{DSCK}/T_{SCKD}	DIN Setup/Hold, master mode		0.5 1.0	0.5 1.0	ns, Min
T_{CCO}	DOUT		7.5	7.5	ns, Max
T_{CCH}	High Time		2.0	2.0	ns, Min
T_{CCL}	Low Time		2.0	2.0	ns, Min
F_{CC_SERIAL}	Maximum Frequency, master mode with respect to nominal CCLK.		100	100	MHz, Max
F_{MCCTOL}	Frequency Tolerance, master mode with respect to nominal CCLK.		±50	±50	%
SelectMAP Write Timing Characteristics					
T_{SMDCC}/T_{SMCCD}	D0-7 Setup/Hold		2.0 0.0	2.0 0.0	ns, Min
T_{SMCSCC}/T_{SMCCCS}	CS_B Setup/Hold		1.0 0.5	1.0 0.5	ns, Min
T_{SMCCW}/T_{SMWCC}	RDWR_B Setup/Hold		6.0 1.0	6.0 1.0	ns, Min
T_{SMCKBY}	BUSY Propagation Delay		8.0	8.0	ns, Max
$F_{CC\_SELECTMAP}$	Maximum Frequency, master mode with respect to nominal CCLK.		100	100	MHz, Max
F_{MCCTOL}	Frequency Tolerance, master mode with respect to nominal CCLK.		±50	±50	%
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}	TMS and TDI Setup time before TCK		1.0	1.0	ns, Min
T_{TCKTAP}	TMS and TDI Hold time after TCK		2.0	2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid		6.0	6.0	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency		66	66	MHz, Max
F_{TCKB}	Maximum boundary-scan TCK clock frequency		50	50	MHz, Max

Clock Buffers and Networks

Table 30: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold		0.29 0.00	0.34 0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold		0.29 0.00	0.34 0.00	ns
T_{BCCKO_O}	BUFGCTRL delay		0.29	0.34	ns

Notes:
1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.

Table 31: **I/O and Regional Clock Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
$T_{BUFIOCKO\_O}$	BUFIO delay				ns
	I/O clock input to output delay across one clock region(1)				ns
	I/O clock input to output delay across multiple clock regions(1)				ns
	I/O clock tree net MAX frequency				MHz
T_{BRCKO_O}	BUFR delay without BUFR_DIVIDE attribute				ns
	BUFR delay with BUFR_DIVIDE attribute				ns
T_{BRDO_CLRO}	Clear to Out for BUFR				ns
	Regional clock input to output delay across one clock region(1)(2)				ns
	Regional clock input to output delay across multiple clock regions(1)(2)				ns
	Regional clock tree net MAX frequency				MHz

Notes:
1. Measured using LVCMOS25, 12mA, fast slew rate.
2. Measured on the edge column.

DCM and PMCD Switching Characteristics

Table 32: **Operating Frequency Ranges for DCM in Maximum Speed (MS) Mode**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Outputs Clocks (Low Frequency Mode)					
CLKOUT_FREQ_1X_LF_MS_MIN	CLK0, CLK90, CLK180, CLK270		32	32	MHz
CLKOUT_FREQ_1X_LF_MS_MAX			150	150	MHz
CLKOUT_FREQ_2X_LF_MS_MIN	CLK2X, CLK2X180		64	64	MHz
CLKOUT_FREQ_2X_LF_MS_MAX			300	300	MHz
CLKOUT_FREQ_DV_LF_MS_MIN	CLKDV		2	2	MHz
CLKOUT_FREQ_DV_LF_MS_MAX			100	100	MHz
CLKOUT_FREQ_FX_LF_MS_MIN	CLKFX, CLKFX180		32	32	MHz
CLKOUT_FREQ_FX_LF_MS_MAX			210	210	MHz
Input Clocks (Low Frequency Mode)					
CLKIN_FREQ_DLL_LF_MS_MIN	CLKIN (using DLL outputs)(1)		32	32	MHz
CLKIN_FREQ_DLL_LF_MS_MAX			150	150	MHz
CLKIN_FREQ_FX_LF_MS_MIN	CLKIN (using DFS outputs only)(2)		1	1	MHz
CLKIN_FREQ_FX_LF_MS_MAX			210	210	MHz
PSCLK_FREQ_LF_MS_MIN	PSCLK		1	1	KHz
PSCLK_FREQ_LF_MS_MAX			450	400	MHz
Outputs Clocks (High Frequency Mode)					
CLKOUT_FREQ_1X_HF_MS_MIN	CLK0, CLK90, CLK180, CLK270		150	150	MHz
CLKOUT_FREQ_1X_HF_MS_MAX			450	400	MHz
CLKOUT_FREQ_2X_HF_MS_MIN	CLK2X, CLK2X180		300	300	MHz
CLKOUT_FREQ_2X_HF_MS_MAX			450	400	MHz
CLKOUT_FREQ_DV_HF_MS_MIN	CLKDV		9.4	9.4	MHz
CLKOUT_FREQ_DV_HF_MS_MAX			300	267	MHz
CLKOUT_FREQ_FX_HF_MS_MIN	CLKFX, CLKFX180		210	210	MHz
CLKOUT_FREQ_FX_HF_MS_MAX			315	280	MHz
Input Clocks (High Frequency Mode)					
CLKIN_FREQ_DLL_HF_MS_MIN	CLKIN (using DLL outputs)(1)		150	150	MHz
CLKIN_FREQ_DLL_HF_MS_MAX			450	400	MHz
CLKIN_FREQ_FX_HF_MS_MIN	CLKIN (using DFS outputs only)(2)		50	50	MHz
CLKIN_FREQ_FX_HF_MS_MAX			315	280	MHz
PSCLK_FREQ_HF_MS_MIN	PSCLK		1	1	KHz
PSCLK_FREQ_HF_MS_MAX			450	400	MHz

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

Table 33: **Operating Frequency Ranges for DCM in Maximum Range (MR) Mode**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Outputs Clocks (Low Frequency Mode)					
CLKOUT_FREQ_1X_LF_MR_MIN	CLK0, CLK90, CLK180, CLK270		19	19	MHz
CLKOUT_FREQ_1X_LF_MR_MAX			36	32	MHz
CLKOUT_FREQ_2X_LF_MR_MIN	CLK2X, CLK2X180		38	38	MHz
CLKOUT_FREQ_2X_LF_MR_MAX			72	64	MHz
CLKOUT_FREQ_DV_LF_MR_MIN	CLKDV		1.2	1.2	MHz
CLKOUT_FREQ_DV_LF_MR_MAX			24	21.3	MHz
CLKOUT_FREQ_FX_LF_MR_MIN	CLKFX, CLKFX180		16.8	16.8	MHz
CLKOUT_FREQ_FX_LF_MR_MAX			36	32	MHz
Input Clocks (Low Frequency Mode)					
CLKIN_FREQ_DLL_LF_MR_MIN	CLKIN (using DLL outputs)(1)		19	19	MHz
CLKIN_FREQ_DLL_LF_MR_MAX			36	32	MHz
CLKIN_FREQ_FX_LF_MR_MIN	CLKIN (using DFS outputs only)(2)		1	1	MHz
CLKIN_FREQ_FX_LF_MR_MAX			32	28	MHz
PSCLK_FREQ_LF_MR_MIN	PSCLK		1	1	KHz
PSCLK_FREQ_LF_MR_MAX			236	210	MHz

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

Table 34: **Input Clock Tolerances**

Symbol	Description	Frequency Range	Value	Units
Duty Cycle Input Tolerance (in %)				
CLKIN_PSCLK_PULSE_RANGE_1	PSCLK only	< 1 MHz	25 - 75	%
CLKIN_PSCLK_PULSE_RANGE_1_50	PSCLK and CLKIN	1 - 50 MHz	25 - 75	%
CLKIN_PSCLK_PULSE_RANGE_50_100		50 - 100 MHz	30 - 70	%
CLKIN_PSCLK_PULSE_RANGE_100_200		100 - 200 MHz	40 - 60	%
CLKIN_PSCLK_PULSE_RANGE_200_400		200 - 400 MHz	45 - 55	%
CLKIN_PSCLK_PULSE_RANGE_400		> 400 MHz	45 - 55	%
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)		**Speed Grade**		
		-12	**-11**	**-10**	**Units**
CLKIN_CYC_JITT_DLL_LF	CLKIN (using DLL outputs)(1)		±300	±350	ps
CLKIN_CYC_JITT_FX_LF	CLKIN (using DFS outputs)(2)		±300	±350	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)					
CLKIN_CYC_JITT_DLL_HF	CLKIN (using DLL outputs)(1)		±150	±180	ps
CLKIN_CYC_JITT_FX_HF	CLKIN (using DFS outputs)(2)		±150	±180	ps
Input Clock Period Jitter (Low Frequency Mode)					
CLKIN_PER_JITT_DLL_LF	CLKIN (using DLL outputs)(1)		±1.0	±1.15	ns
CLKIN_PER_JITT_FX_LF	CLKIN (using DFS outputs)(2)		±1.0	±1.15	ns
Input Clock Period Jitter (High Frequency Mode)					
CLKIN_PER_JITT_DLL_HF	CLKIN (using DLL outputs)(1)		±1.0	±1.15	ns
CLKIN_PER_JITT_FX_HF	CLKIN (using DFS outputs)(2)		±1.0	±1.15	ns
Feedback Clock Path Delay Variation					
CLKFB_DELAY_VAR_EXT	CLKFB off-chip feedback		±1.0	±1.15	ns

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. If both DLL and DFS outputs are used, follow the more restrictive specifications.

Output Clock Jitter

Table 35: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade			Units
			-12	-11	-10	
Clock Synthesis Period Jitter						
CLK0	CLKOUT_PER_JITT_0			±100	±100	ps
CLK90	CLKOUT_PER_JITT_90			±150	±150	ps
CLK180	CLKOUT_PER_JITT_180			±150	±150	ps
CLK270	CLKOUT_PER_JITT_270			±150	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X			±200	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1			±150	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2			±300	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX			Note 1	Note 1	ps

Notes:
1. Values for this parameter are available at www.xilinx.com.

Output Clock Phase Alignment

Table 36: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade			Units
			-12	-11	-10	
Phase Offset Between CLKIN and CLKFB						
CLKIN/CLKFB	CLKIN_CLKFB_PHASE			±120	±120	ps
Phase Offset Between Any DCM Outputs						
All CLK outputs	CLKOUT_PHASE			±140	±140	ps
Duty Cycle Precision						
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL(3)			±150	±150	ps
DFS outputs(2)	CLKOUT_DUTY_CYCLE_FX			±200	±200	ps

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.

Table 37: **Miscellaneous Timing Parameters**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Time Required to Achieve LOCK					
T_LOCK_DLL_240	DLL output – Frequency range > 240 MHz (1)		20	20	µs
T_LOCK_DLL_120_240	DLL output – Frequency range 120 - 240 MHz (1)		63	63	µs
T_LOCK_DLL_60_120	DLL output – Frequency range 60 - 120 MHz (1)		225	225	µs
T_LOCK_DLL_50_60	DLL output – Frequency range 50 - 60 MHz(1)		325	325	µs
T_LOCK_DLL_40_50	DLL output – Frequency range 40 - 50 MHz (1)		500	500	µs
T_LOCK_DLL_30_40	DLL output – Frequency range 30 - 40 MHz (1)		900	900	µs
T_LOCK_DLL_24_30	DLL output – Frequency range 24 - 30 MHz(1)		1250	1250	µs
T_LOCK_DLL_30	DLL output – Frequency range < 30 MHz (1)		1250	1250	µs
T_LOCK_FX_MIN	DFS outputs(2)		10	10	ms
T_LOCK_FX_MAX			10	10	ms
T_LOCK_DLL_FINE_SHIFT	Multiplication factor for DLL lock time with Fine Shift		2	2	
Fine Phase Shifting					
FINE_SHIFT_RANGE_MS	Absolute shifting range in maximum speed mode		7	7	ns
FINE_SHIFT_RANGE_MR	Absolute shifting range in maximum range mode		10	10	ns
Delay Lines					
DCM_TAP_MS_MIN	Tap delay resolution (Min) in maximum speed mode		5	5	ps
DCM_TAP_MS_MAX	Tap delay resolution (Max) in maximum speed mode		40	40	ps
DCM_TAP_MR_MIN	Tap delay resolution (Min) in maximum range mode		10	10	ps
DCM_TAP_MR_MAX	Tap delay resolution (Max) in maximum range mode		60	60	ps

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

Table 38: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Table 39: **DCM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
T_{DMCCK_PSEN}/ T_{DMCKC_PSEN}	PSEN Setup/Hold		0.93 0.00	1.07 0.00	ns
$T_{DMCCK\_PSINCDEC}$/ $T_{DMCKC\_PSINCDEC}$	PSINCDEC Setup/Hold		0.93 0.00	1.07 0.00	ns
T_{DMCKO_PSDONE}	Clock to out of PSDONE		0.60	0.69	ns

Table 40: **PMCD Switching Characteristic**

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
T_{PMCCCK_REL}/ T_{PMCCKC_REL}	REL Setup/Hold for all outputs		0.60 0.00	0.60 0.00	ns
$T_{PMCCO\_CLK\{A1,B,C,D\}}$	RST assertion to clock output deassertion		4.00	4.50	ns
$T_{PMCCKO\_CLK\{A1,B,C,D\}}$	Max clock propagation delay of PMCD for all outputs		4.60	5.20	ns
PMCD_CLK_SKEW	Max phase between all outputs assuming all inputs		±150	±150	ps
CLKIN_FREQ_PMCD_CLKA_MAX	Max input/output frequency		450	400	MHz
CLKIN_PSCLK_PULSE_RANGE (1)	Max duty cycle input tolerance (Same as DCM)		Table 34	Table 34	
PMCD_REL_HIGH_PULSE_MIN	Min pulse width for REL		1.11	1.25	ns
PMCD_RST_HIGH_PULSE_MIN	Min pulse width for RST		1.11	1.25	ns

Notes:
1. Refer to Table 34 parameter: CLKIN_PSCLK_PULSE_RANGE.

System-Synchronous Switching Characteristics

Virtex-4 Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 41. Values are expressed in nanoseconds unless otherwise noted.

Table 41: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, With DCM**

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM.						
$T_{ICKOFDCM}$	Global Clock and OFF with DCM	XC4VLX15				ns
		XC4VLX25				ns
		XC4VLX40				ns
		XC4VLX60				ns
		XC4VLX80				ns
		XC4VLX100				ns
		XC4VLX160				ns
		XC4VLX200				ns
		XC4VSX25				ns
		XC4VSX35				ns
		XC4VSX55				ns
		XC4VFX12				ns
		XC4VFX20				ns
		XC4VFX40				ns
		XC4VFX60				ns
		XC4VFX100				ns
		XC4VFX140				ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 42: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, Without DCM**

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM.						
T_{ICKOF}	Global Clock and OFF without DCM	XC4VLX15				ns
		XC4VLX25				ns
		XC4VLX40				ns
		XC4VLX60				ns
		XC4VLX80				ns
		XC4VLX100				ns
		XC4VLX160				ns
		XC4VLX200				ns
		XC4VSX25				ns
		XC4VSX35				ns
		XC4VSX55				ns
		XC4VFX12				ns
		XC4VFX20				ns
		XC4VFX40				ns
		XC4VFX60				ns
		XC4VFX100				ns
		XC4VFX140				ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Virtex-4 Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 43. Values are expressed in nanoseconds unless otherwise noted.

Table 43: **Global Clock Setup and Hold for LVCMOS25 Standard, With DCM**

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)						
T_{PSDCM}/ T_{PHDCM}	No Delay Global Clock and IFF(2) with DCM	XC4VLX15				ns
		XC4VLX25				ns
		XC4VLX40				ns
		XC4VLX60				ns
		XC4VLX80				ns
		XC4VLX100				ns
		XC4VLX160				ns
		XC4VLX200				ns
		XC4VSX25				ns
		XC4VSX35				ns
		XC4VSX55				ns
		XC4VFX12				ns
		XC4VFX20				ns
		XC4VFX40				ns
		XC4VFX60				ns
		XC4VFX100				ns
		XC4VFX140				ns

Notes:
1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   CLK0 DCM jitter
   Worst-case duty-cycle distortion using CLK0.
   IFF = Input Flip-Flop or Latch

Table 44: **Global Clock Setup and Hold for LVCMOS25 Standard, Without DCM**

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)						
T_{PSFD}/ T_{PHFD}	Full Delay Global Clock and IFF(2) without DCM	XC4VLX15				ns
		XC4VLX25				ns
		XC4VLX40				ns
		XC4VLX60				ns
		XC4VLX80				ns
		XC4VLX100				ns
		XC4VLX160				ns
		XC4VLX200				ns
		XC4VSX25				ns
		XC4VSX35				ns
		XC4VSX55				ns
		XC4VFX12				ns
		XC4VFX20				ns
		XC4VFX40				ns
		XC4VFX60				ns
		XC4VFX100				ns
		XC4VFX140				ns

Notes:
1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

ChipSync™ Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-4 source-synchronous transmitter and receiver data-valid windows.

Table 45: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion (1)	All				ns
T_{CKSKEW}	Global Clock Tree Skew (2)	XC4VLX15				ns
		XC4VLX25				ns
		XC4VLX40				ns
		XC4VLX60				ns
		XC4VLX80				ns
		XC4VLX100				ns
		XC4VLX160				ns
		XC4VLX200				ns
		XC4VSX25				ns
		XC4VSX35				ns
		XC4VSX55				ns
		XC4VFX12				ns
		XC4VFX20				ns
		XC4VFX40				ns
		XC4VFX60				ns
		XC4VFX100				ns
		XC4VFX140				ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All				ns
	I/O clock tree skew across one clock region	All				ns
$T_{BUFIOSKEW}$	I/O clock tree skew across multiple clock regions	All				ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All				ns
	Regional clock tree skew across one clock region	All				ns
$T_{BUFRSKEW}$	Regional clock tree skew across multiple clock regions	All				ns

Notes:
1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 46: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC4VLX15	SF363		ps
			FF668		ps
		XC4VLX25	SF363	90	ps
			FF668	110	ps
		XC4VLX40	FF668	110	ps
			FF1148	150	ps
		XC4VLX60	FF668	130	ps
			FF1148	140	ps
		XC4VLX80	FF1148		ps
		XC4VLX100	FF1148	140	ps
			FF1513	180	ps
		XC4VLX160	FF1148		ps
			FF1513		ps
		XC4VLX200	FF1513	180	ps
		XC4VSX25	FF668		ps
		XC4VSX35	FF668	100	ps
		XC4VSX55	FF1148	145	ps
		XC4VFX12	SF363	90	ps
			FF668	100	ps
		XC4VFX20	FF672		ps
		XC4VFX40	FF672		ps
			FF1152		ps
		XC4VFX60	FF672		ps
			FF1152		ps
		XC4VFX100	FF1152		ps
			FF1517		ps
		XC4VFX140	FF1517		ps
			FF1760		ps

Notes:
1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 47: **Sample Window**

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All				ns
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO	All				ns

Notes:
1. This parameter indicates the total sampling error of Virtex-4 DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation.
2. These measurements include:
   - CLK0 DCM jitter
   - Worst-case duty-cycle distortion, T_{DCD_CLK}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.

Table 48: **Example Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
Example Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin.(1) Using DCM and Global Clock Buffer.						
T_{PSDCM_0}/T_{PHDCM_0}	No Delay Global Clock and IFF(2) with DCM	XC4VLX15				ns
		XC4VLX25				ns
		XC4VLX40				ns
		XC4VLX60				ns
		XC4VLX80				ns
		XC4VLX100				ns
		XC4VLX160				ns
		XC4VLX200				ns
		XC4VSX25				ns
		XC4VSX35				ns
		XC4VSX55				ns
		XC4VFX12				ns
		XC4VFX20				ns
		XC4VFX40				ns
		XC4VFX60				ns
		XC4VFX100				ns
		XC4VFX140				ns
	Setup/Hold of I/O clock across one clock region	All				ns
	Setup/Hold of I/O clock across multiple clock regions	All				ns

Table 48: **Example Pin-to-Pin Setup/Hold: Source-Synchronous Configuration *(Continued)***

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
	Setup/Hold of regional clock across one clock region	All				ns
	Setup/Hold of regional clock across multiple clock regions	All				ns

Notes:
1. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include:
   - CLK0 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and T_{DCD_CLK}
   - Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/02/04	1.0	Initial Xilinx release. Printed Handbook version.
09/09/04	1.1	Edits in Tables 12, 13, 18, 19, 20, 22, 26, 28, 37, and 38. Removed Table 39.
01/18/05	1.2	Added parameters to Tables 4 and 5. Removed System Monitor and ADC parameters.
02/01/05	1.3	Changed parameters in Tables 1, 2, 3, 7, and 11. Added **Performance Characteristics** section. Added **Switching Characteristics** section and Table 15. Added parameters to the following tables: 4 - 6, 14, 16 - 30, 32 - 40, and 46.
02/24/05	1.4	Changed the notes in Table 2. Added Set/Reset parameters to Table 18 and Table 19. Changed description in Table 21. Changed Set/Reset in Table 23. Changed PSCLK units in Table 32. Added parameters to Table 33. Changed DCM_TAP_MS_MIN in Table 37.