FPGA Temperature Dependent Leakage Modeling
Week 2 Progress Report 1/21/05
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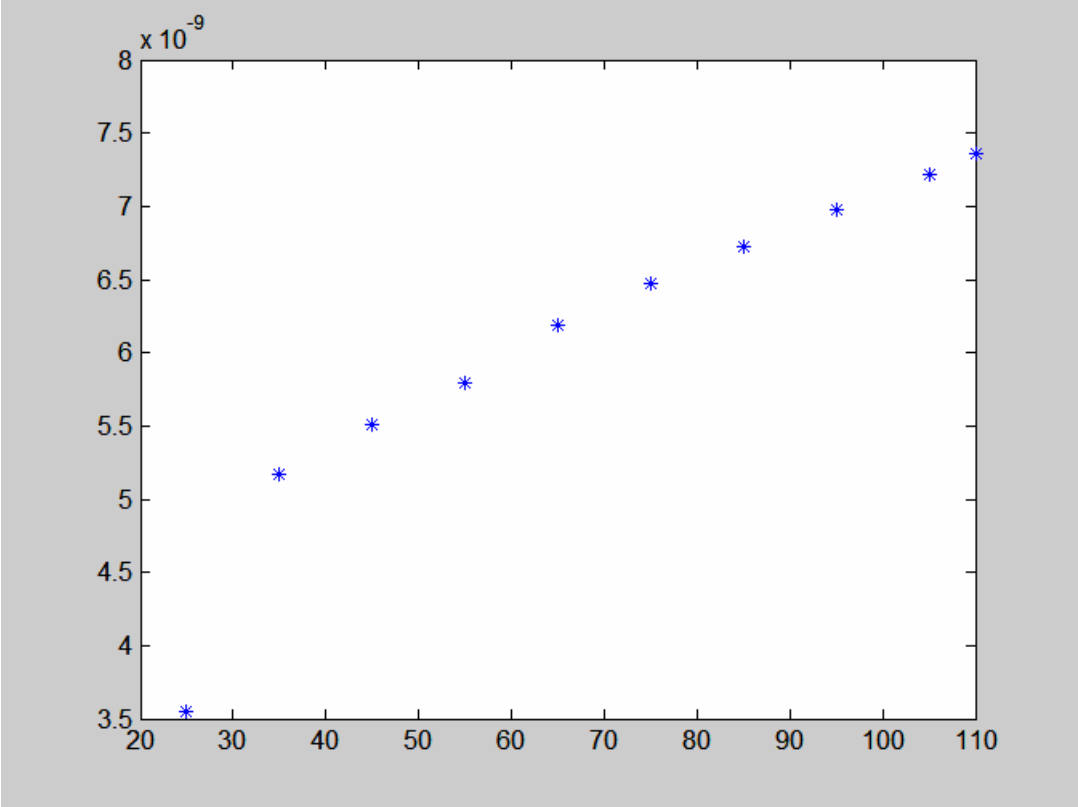
1. SRAM and LUT leakage did not demonstrate a monotonic behavior with temperature. After different trials, it was found that if the SRAM word line voltage is set to a higher value, the problem disappears. So for now, the simulation setting is Vdd=1V, Vt=0.2V, Vt_SRAM=0.65V, and V_word line is 1.35V.

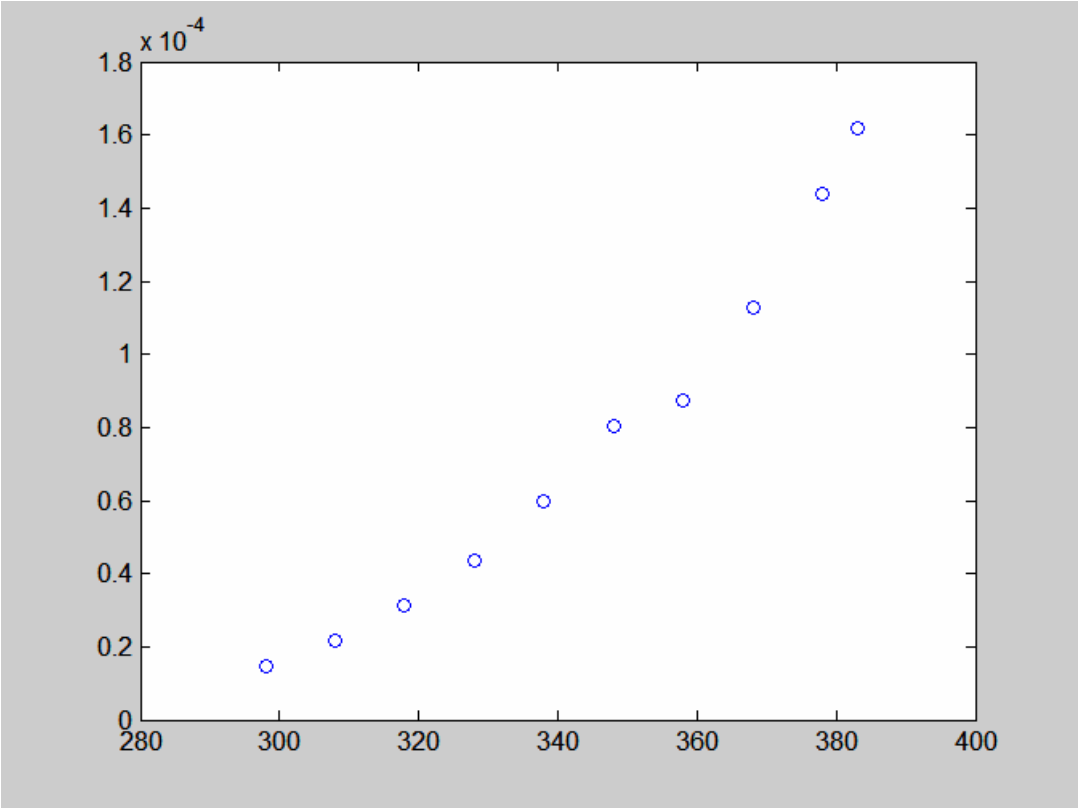
2. The above device setting is verified to be valid by testing the read and write operation in SRAM.

3. All the leakage current components required by the power simulator are simulated using HSPICE. The curves are as follows. Curve fitting will be done as the next step.

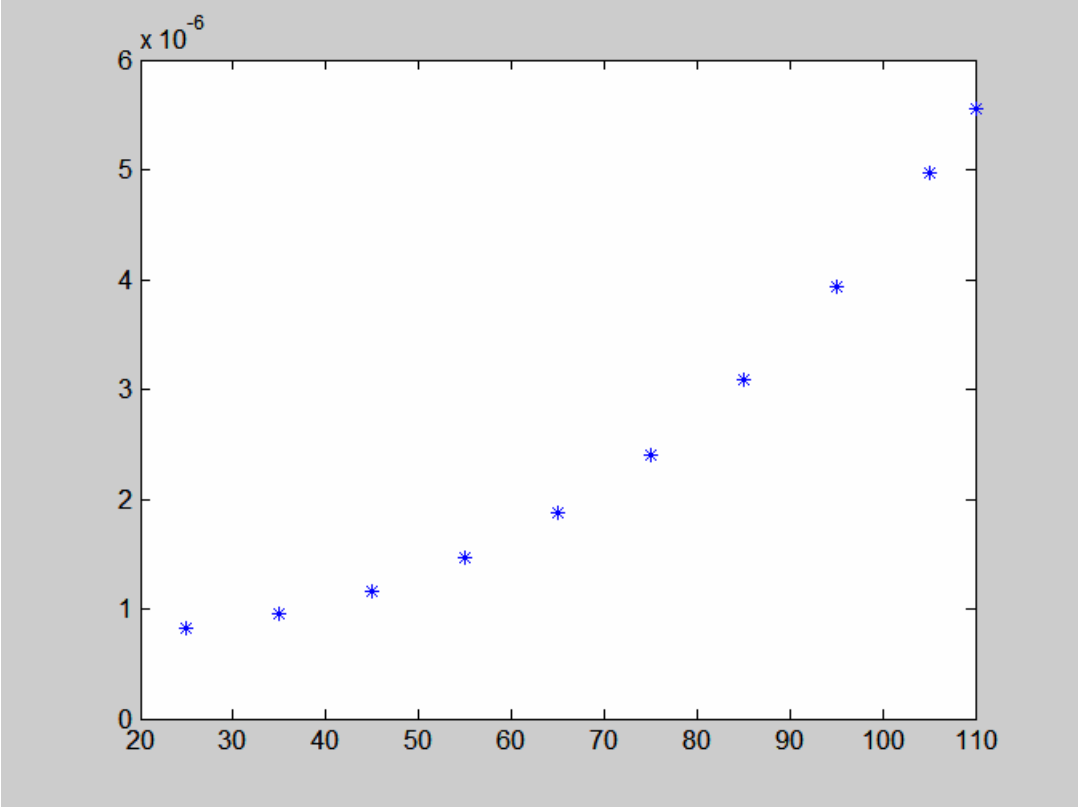
SRAM Leakage VS Temperature



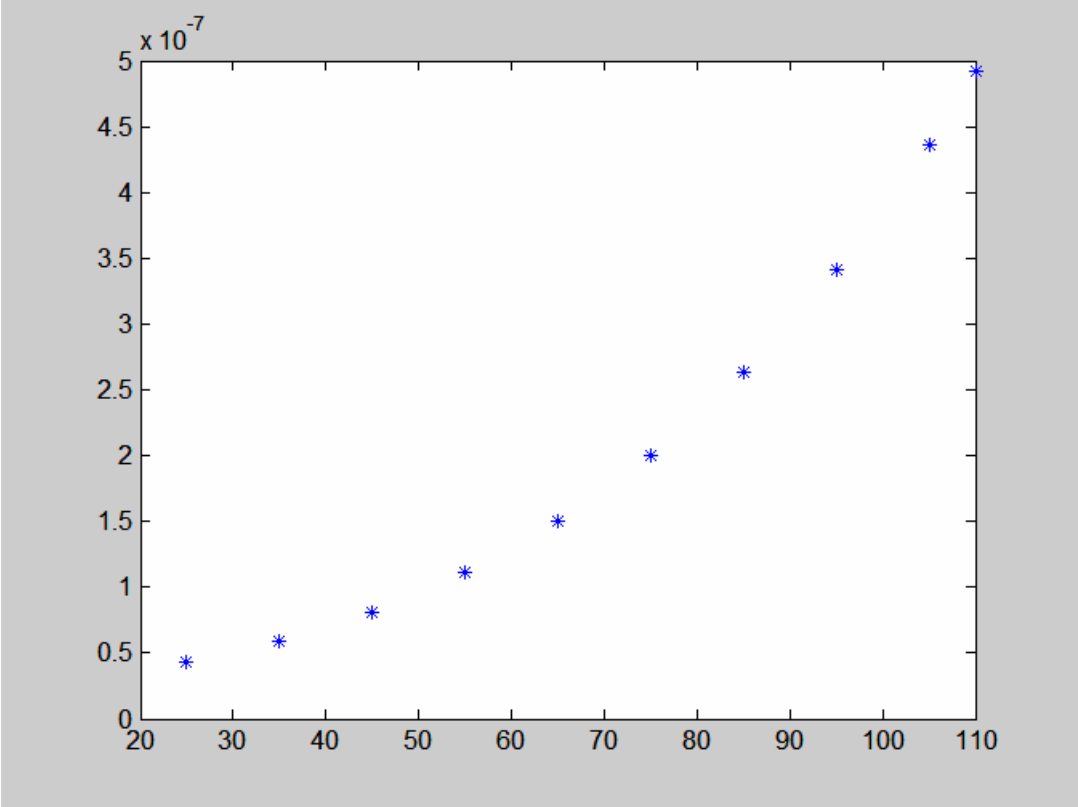
SRAM (32x32) with precharge logic, word line driver



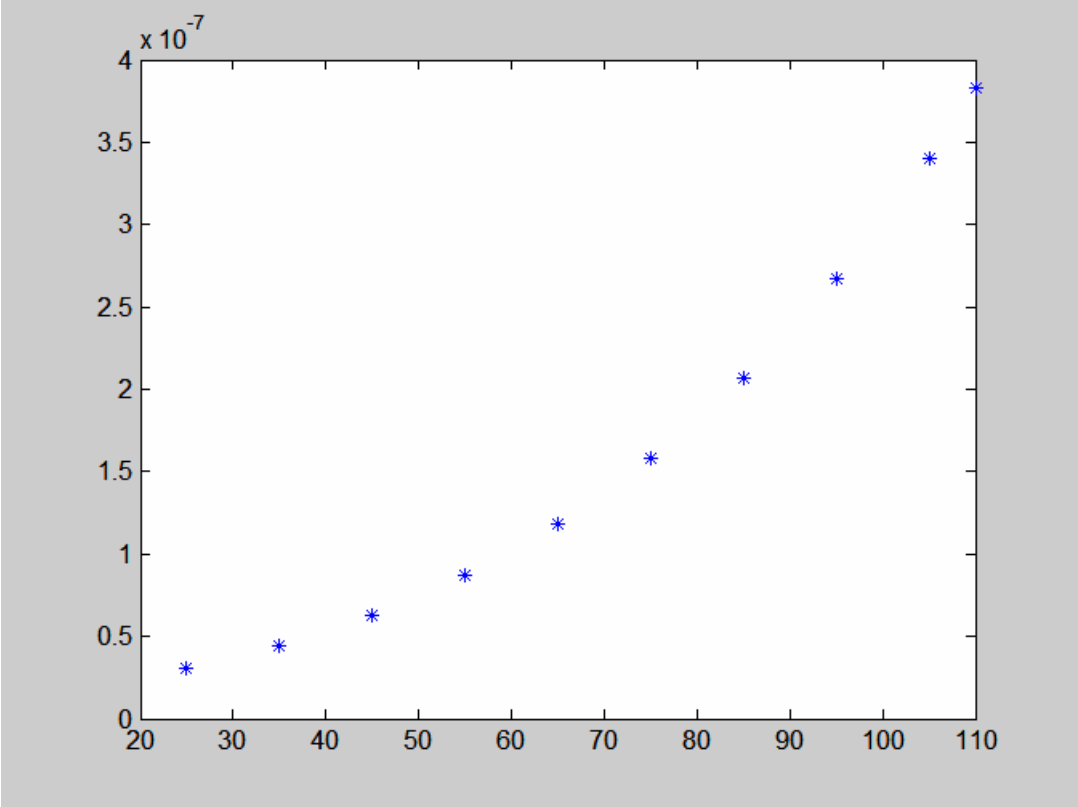
LUT4 Leakage VS Temperature



DFF Leakage VS Temperature



Buffer 4x Leakage VS Temperature


x 10^-7
4
3.5
3
2.5
2
1.5
1
0.5
0
20
30
40
50
60
70
80
90
100
110