Weekly report 1/21/05 Yan Lin

Study of mix of Vdd-gateable and Vdd-programmable interconnects

FPGA routing architecture to be studied:

Partition a routing channel into two regions, Vdd-gateable interconnects with high-Vdd and Vdd-programmable interconnects. The ratio of Vdd-gateable to Vdd-programmable interconnects is set to 1:1.

Algorithms:

Approach 1: Perform single-Vdd routing and then perform segment based bottom-up assignment for the routing trees that are routed on Vdd-programmable interconnects. Generate BC-netlist for mixed interconnects and perform power simulation. Count SRAM number and calculate area etc.

Some results by approach 1

	Vdd-Gateable	Vdd-Programmable	Mixed Interconnects
Total Area Overhead	56.77%	147.75%	~98%
Interconnect Area Overhead	80.34%	214.16%	~147%
Total Power Saving	45.84%	53.93%	49.91%
Interconnect Power Saving	63.68%	76.32%	69.95%

The experimental results are based on architecture N 10 k 4 and VddH 1.3v VddL 0.9v. The baseline uses Single-Vdd.

On average, VddL can be assigned to 85.83% interconnects using programmable Vdd while VddL can be assigned to 46.22% interconnect switches using mixed interconnects

If compared to Vdd-gateable interconnects, the mixed interconnects can reduce 7.5% power at cost of 17% area overhead.

Approach 2

The big picture is to perform power-aware routing for mixed interconnects based on criticality analysis. Perform segment based bottom-up assignment after power-aware routing. Generate BC-netlist and perform power simulation. Count SRAM number and calculate area etc.

Step I:

Calculate the criticality(i, j) for the connection between the source and j^{th} sink of routing tree i. Criticality(i, j) is defined as (# of VddH switches)/(# of switches) in the connection.

Step II:

Perform power-aware routing based on criticality from Step I. Try to route the critical tree using VddH-gateable interconnects and non-critical tree using Vdd programmable interconnects.

Step III:

Perform segment based bottom-up assignment after power-aware routing.

Step I and Step II have been finished. The ongoing work includes debugging Step II and implementing Step III.

More VddL interconnect switches and more power reduction are expected to be achieved

compared the first approach using power-aware routing.

The next step will include extending the power-aware routing for mix of VddH-gateable, VddL-gateable and Vdd programmable interconnects to achieve more power saving with smaller area overhead. However, this will probably introduce performance degradation due to layout constraint. Actually I expect even the power aware routing for mix of vddH interconnects and Vdd programmable interconnects will introduce performance degradation compared to single-Vdd routing.