Summary of FPGA I/O Related Information

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Xilinx Virtex-4 FPGA Family

1. Virtex-4 FPGA Family Members

Pay attention to the last two columns that shows the total I/O banks and maximum usable IOBs.

Device	Configurable Logic Blocks (CLBs)(1)				XtremeDSP Slices(2)	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transciever Blocks	Total I/O Banks	Max User I/O
	Array Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VLX15	64 x 24	13,824	6,144	96	32	48	864	4	0	N/A	N/A	N/A	9	320
XC4VLX25	96 x 28	24,192	10,752	168	48	72	1,296	8	4	N/A	N/A	N/A	11	448
XC4VLX40	128 x 36	41,472	18,432	288	64	96	1,728	8	4	N/A	N/A	N/A	13	640
XC4VLX60	128 x 52	59,904	26,624	416	64	160	2,880	8	4	N/A	N/A	N/A	13	640
XC4VLX80	160 x 56	80,640	35,840	560	80	200	3,600	12	8	N/A	N/A	N/A	15	768
XC4VLX100	192 x 64	110,592	49,152	768	96	240	4,320	12	8	N/A	N/A	N/A	17	960
XC4VLX160	192 x 88	152,064	67,584	1056	96	288	5,184	12	8	N/A	N/A	N/A	17	960
XC4VLX200	192 x 116	200,448	89,088	1392	96	336	6,048	12	8	N/A	N/A	N/A	17	960
XC4VSX25	64 x 40	23,040	10,240	160	128	128	2,304	4	0	N/A	N/A	N/A	9	320
XC4VSX35	96 x 40	34,560	15,360	240	192	192	3,456	8	4	N/A	N/A	N/A	11	448
XC4VSX55	128 x 48	55,296	24,576	384	512	320	5,760	8	4	N/A	N/A	N/A	13	640
XC4VFX12	64 x 24	12,312	5,472	86	32	36	648	4	0	1	2	N/A	9	320
XC4VFX20	64 x 36	19,224	8,544	134	32	68	1,224	4	0	1	2	8	9	320
XC4VFX40	96 x 44	41,904	15,552	243	48	144	2,592	8	4	2	4	12	11	448
XC4VFX60	128 x 52	56,880	25,280	395	128	232	4,176	12	8	2	4	16	13	576
XC4VFX100	160 x 68	94,896	42,176	659	160	376	6,768	12	8	2	4	20	15	768
XC4VFX140	192 x 84	142,128	63,168	987	192	552	9,936	20	8	2	4	24	17	896

2. Virtex-4 SelectIO Technology

- Wide selections of I/O standards from 1.5V to 3.3V,
- Up to 960 user I/Os
- True differential termination
- Selected low-capacitance I/Os for improved signal integrity

- Same edge capture at input and output I/Os
- Memory interface support for DDR and DDR-2 SDRAM, QDR-II, RLDRAM-II, and FCRAM-II
- Extremely high performance
  - 600 Mb/s HSTL & SSTL (on all single-ended I/O)
  - 1 Gb/s LVDS (on all differential I/O pairs)
- Built-In ChipSync™ Source-Synchronous Technology
  - Integrated with SelectIO technology to simplify source-synchronous interfaces
  - Per-bit deskew capability built in all I/O blocks (variable input delay line)
  - Dedicated I/O and regional clocking resources (pin and trees)
  - Built in data serializer/deserializer logic in all I/O and clock dividers
  - Memory/Networking/Telecommunication interfaces up to 1 Gb/s+

- Digitally-controlled impedance (DCI) active I/O termination
  - Optional series or parallel termination
  - Temperature compensation

- Fine grained I/O banking (Configuration in one bank)

3. Virtex-4 Input/Output Blocks (SelectIO IOB)

IOBs are programmable and can be categorized as follows:
- Programmable single-ended or differential (LVDS) operation
- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register
- Bidirectional block
- Per-bit deskew circuitry
- Dedicated I/O and regional clocking resources
- Built in data serializer/deserializer

The IOB registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended standards:
- LVTTL
- LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI (33 and 66 MHz)
- PCI-X
- GTL and GTLP
- HSTL 1.5V and 1.8V (Class I, II, III, and IV)
- SSTL 1.8V and 2.5V (Class I and II)

The DCI I/O feature can be configured to provide on-chip termination for each single-ended I/O standard and some differential I/O standards.

The IOB elements also support the following differential signaling I/O standards:
- LVDS and Extended LVDS (2.5V only)
- BLVDS (Bus LVDS)
- ULVDS
- Hypertransport™
- Differential HSTL 1.5V and 1.8V (Class II)
- Differential SSTL 1.8V and 2.5V (Class II)

Two adjacent pads are used for each differential pair.

Two or four IOB blocks connect to one switch matrix to access the routing resources.

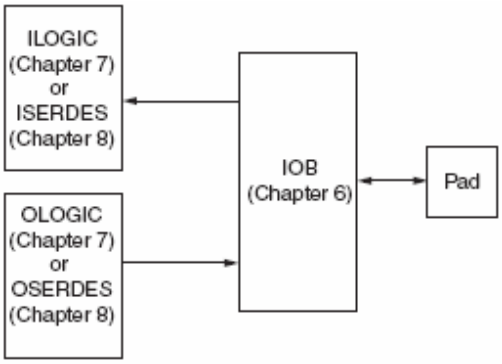
Per-bit deskew circuitry allows for programmable signal delay internal to the FPGA. Per-bit deskew flexibly provides fine-grained increments of delay to carefully produce a range of signal delays. This is especially useful for synchronizing signal edges in source synchronous interfaces.

General purpose I/O in select locations (four per bank) are designed to be "regional clock capable" I/O by adding special hardware connections for I/O in the same locality. These regional clock inputs are distributed within a limited region to minimize clock skew between IOBs. Regional I/O clocking supplements the global clocking resources.

Data serializer/deserializer capability is added to every I/O to support source synchronous interfaces. A serial-to-parallel converter with associated clock divider is included in the input path, and a parallel-to-serial converter in the output path.

4. Virtex-4 I/O Resources

An I/O tile contains two IOBs, two ILOGICs, and two OLOGICs.



All Virtex-4 FPGAs have configurable high-performance SelectIO drivers and receivers, supporting a wide variety of standard interfaces. The robust feature set includes programmable control of output strength and slew rate, and on-chip termination using Digitally Controlled Impedance (DCI). All banks can support 3.3V I/O.

Each IOB contains both input, output, and 3-state SelectIO drivers. These drivers can be configured to various I/O standards. Differential I/O uses the two IOBs grouped together in one tile.

- Single-ended I/O standards (LVCMOS, LVTTL, HSTL, SSTL, GTL, PCI)
- Differential I/O standards (LVDS, LDT, CSE Differential HSTL and SSTL)

Virtex-4 I/O Bank Rules

The number of banks available in Virtex-4 devices is not limited to eight as in previous Xilinx architectures. In Virtex-4 devices, with some exceptions in the center column, an I/O bank consists of 64 IOBs (32 CLBs and two clock regions). As a result, the number of banks depends upon the device size.

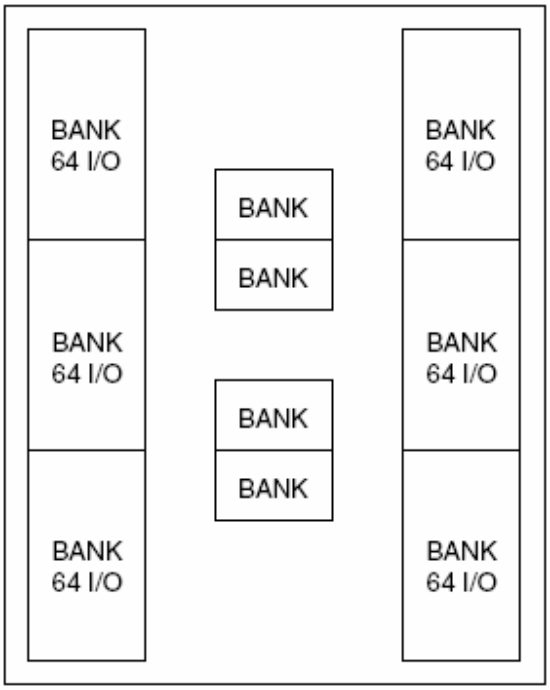


Fig. Virtex-4 XC4VLX25 I/O Banks

3.3V I/O Support: The Virtex-4 architecture supports 3.3V single-ended I/O standards in all banks.

Reference Voltage (VREF) Pins: Low-voltage, single-ended I/O standards with a differential amplifier input buffer require an input reference voltage (VREF). VREF is an external input into Virtex-4 devices. Within each I/O bank, one of every 16 I/O pins is automatically configured as a VREF input, if using a single-ended I/O standard requiring a differential amplifier input buffer.

Output Drive Source Voltage (VCCO) Pins: Many of the low-voltage I/O standards supported by Virtex-4 devices require a different output drive voltage (VCCO). As a result, each device often supports multiple output drive source voltages. Output buffers within a given VCCO bank must share the same output drive source voltage. The following input buffers use the VCCO voltage: LVTTL, LVCMOS, PCI, LVDCI and other DCI standards.

Digitally Controlled Impedance (DCI): To terminate a trace, resistors are traditionally added to make the output and/or input match the impedance of the receiver or driver to the impedance of the trace. However, due to increased device I/Os, adding resistors close to the device pins increases the board area and component count, and can in some cases be physically impossible. To address these issues and to achieve better signal integrity, Xilinx developed the Digitally Controlled Impedance (DCI) technology. DCI adjusts the output impedance or input termination to accurately match the characteristic impedance of the transmission line. DCI actively adjusts the impedance of the I/O to equal an external reference resistance. This compensates for changes in I/O impedance due to process variation. It also continuously adjusts the impedance of the I/O to compensate for variations of temperature and supply voltage fluctuations.

In the case of controlled impedance drivers, DCI controls the driver impedance to match two reference resistors, or optionally, to match half the value of these reference resistors. DCI eliminates the need for external series termination resistors. DCI provides the parallel or series termination for transmitters or receivers. This eliminates the need for termination resistors on the board, reduces board routing difficulties and component count, and improves signal integrity by eliminating stub reflection. Stub reflection occurs when termination resistors are located too far from the end of the transmission line. With DCI, the termination resistors are as close as possible to the output driver or the input buffer, thus, eliminating stub reflections.

DCI uses two multi-purpose reference pins in each bank to control the impedance of the driver or the parallel termination value for all of the I/Os of that bank. The N reference pin (VRN) must be pulled up to VCCO by a reference resistor, and the P reference pin (VRP) must be pulled down to ground by another reference resistor. The value of each reference resistor should be equal to the characteristic impedance of the PC board traces, or should be twice that value (configuration option). When a DCI I/O standard is used on a particular bank, the two multi-purpose reference pins cannot be used as regular I/Os. However, if DCI I/O standards are not used in the bank, these pins are available as regular I/O pins.

Some I/O standards, such as LVCMOS, must have a drive impedance matching the characteristic impedance of the driven line. DCI can provide controlled impedance output drivers to eliminate reflections without an external source termination. The impedance is set by the external reference resistors with resistance equal to the trace impedance. The DCI I/O standards supporting the controlled impedance driver are: LVDCI_15, LVDCI_18, LVDCI_25, and LVDCI_33.

DCI also provides drivers with one half of the impedance of the reference resistors. The DCI I/O standards supporting controlled impedance drivers with half-impedance are LVDCI_DV2_15, LVDCI_DV2_18, and LVDCI_DV2_25.

Some I/O standards require an input termination to VCCO. DCI can also provide input termination to VCCO using single termination. The termination resistance is set by the reference resistors. Both GTL and HSTL standards are controlled by 50 Ω reference resistors. The DCI I/O standards supporting single termination are: GTL_DCI, GTLP_DCI, HSTL_III_DCI, HSTL_III_DCI_18, HSTL_IV_DCI, and HSTL_IV_DCI_18.

Some I/O standards (e.g., HSTL Class I and II) require an input termination voltage of VCCO/2. This is equivalent to having a split termination composed of two resistors. One terminates to VCCO, the other to ground. The resistor values are 2R. DCI provides termination to VCCO/2 using split termination. The termination resistance is set by the external reference resistors, i.e., the resistors to VCC and ground are each twice the reference resistor value. Both HSTL and SSTL standards need 50 Ω external reference resistors. The DCI I/O standards supporting split termination are: HSTL_I_DCI, HSTL_I_DCI_18, HSTL_II_DCI, HSTL_II_DCI_18, SSTL2_I_DCI, SSTL2_II_DCI, STL18_I_DCI, and SSTL18_II_DCI.

Some I/O standards (e.g., HSTL Class IV) require an output termination to VCCO. DCI can provide an output termination to VCCO using single termination. In this case, DCI only controls the impedance of the termination, but not the driver. Both GTL and HSTL standards need 50 Ω external reference resistors. The DCI I/O standards supporting drivers with single termination are: GTL_DCI, GTLP_DCI, HSTL_IV_DCI, and HSTL_IV_DCI_18.

Some I/O standards, such as HSTL Class II, require an output termination to VCCO/2. DCI can provide output termination to VCCO/2 using split termination. DCI only controls the impedance of the termination, but not the driver. Both HSTL and SSTL standards need 50 Ω external reference resistors. The DCI I/O standards supporting drivers with split termination are: HSTL_II_DCI, HSTL_II_DCI_18, SSTL2_II_DCI, and SSTL18_II_DCI.

To correctly use DCI in a Virtex-4 device, users must follow the following rules:
1. VCCO pins must be connected to the appropriate VCCO voltage based on the IOSTANDARDs in that bank.
2. Correct DCI I/O buffers must be used in the software either by using IOSTANDARD attributes or instantiations in the HDL code.
3. External reference resistors must be connected to multipurpose pins (VRN and VRP) in the bank. These two multipurpose pins cannot be used as regular user I/Os. Refer to the Virtex-4 pinout tables for the specific pin locations. Pin VRN must be pulled up to VCCO by its reference resistor. Pin VRP must be pulled down to ground by its reference resistor.
4. The value of the external reference resistors should be selected to give the desired output

impedance. If using GTL_DCI, HSTL_DCI, or SSTL_DCI I/O standards, then the external reference resistors should be 50 Ω.
5. The values of the reference resistors must be within the supported range (20 Ω– 100 Ω).
6. Follow the **DCI I/O banking rules**:
   a. VREF must be compatible for all of the inputs in the same bank.
   b. VCCO must be compatible for all of the inputs and outputs in the same bank.
   c. No more than one DCI I/O standard using single termination type is allowed per bank.
   d. No more than one DCI I/O standard using split termination type is allowed per bank.
e. Single termination and split termination, controlled impedance driver, and controlled impedance driver with half impedance can co-exist in the same bank.
7. The following packages to not support DCI in Banks 1 and 2: SF363, FF668, FF676, FF672, and FF1152.
8. In addition, the following devices do not support DCI in Banks 1 and 2: XC4VLX15, XC4VLX25, XC4VSX25,

5. Virtex-4 logic resources

Virtex-4 FPGAs contain all of the basic I/O logic resources from Virtex-II/Virtex-II Pro FPGAs. These resources include the following:
- Combinatorial input/output
- 3-state output control
- Registered input/output
- Registered 3-state output control
- Double-Data-Rate (DDR) input/output
- DDR output 3-state control

In addition, the following architectural improvements have been implemented:
- IDELAY provides users control of an adjustable, fine-resolution input delay element.
- SAME_EDGE output DDR mode
- SAME_EDGE and SAME_EDGE_PIPELINED input DDR mode
- Input serial-to-parallel converters (ISERDES) and output parallel-to-series converters (OSERDES) support very fast I/O data rates, and allow the internal logic to run up to ten times slower than the I/O.
- The Bitslip sub-module can re-align data to word boundaries, detected with the help of a training pattern.

Altera Stratix II FPGA Family

1. Stratix II FPGA Family Features

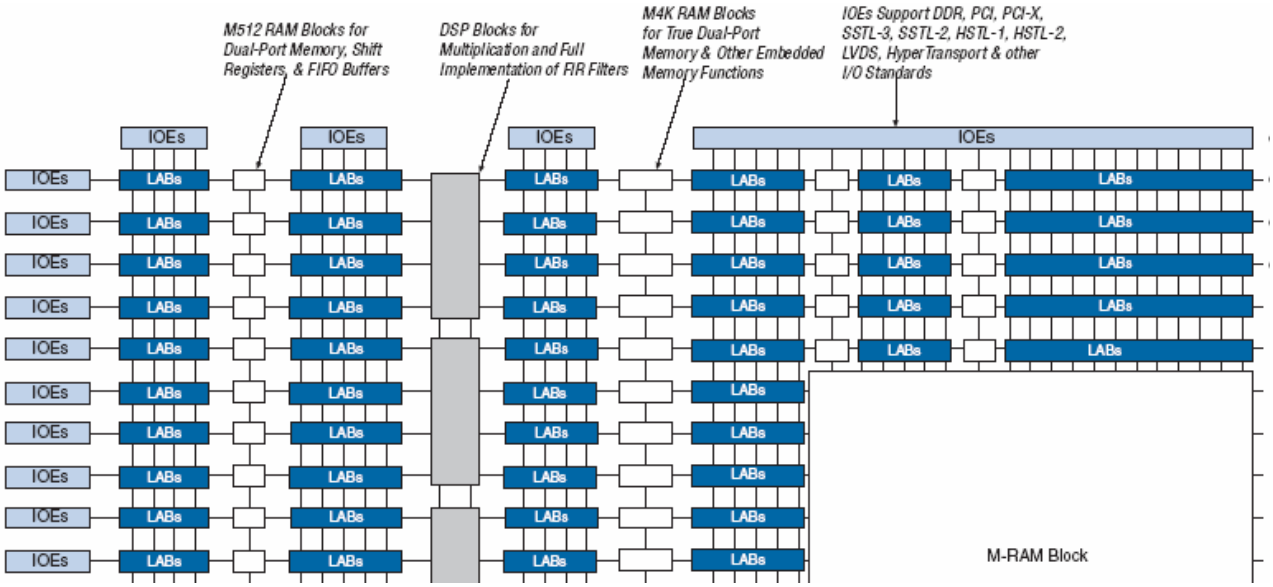
Pay attention to the last column for the number of I/O pins.

Feature	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
ALMs	6,240	13,552	24,176	36,384	53,016	71,760
Adaptive look-up tables (ALUTs) *(1)*	12,480	27,104	48,352	72,768	106,032	143,520
Equivalent LEs *(2)*	15,600	33,880	60,440	90,960	132,540	179,400
M512 RAM blocks	104	202	329	488	699	930
M4K RAM blocks	78	144	255	408	609	768
M-RAM blocks	0	1	2	4	6	9
Total RAM bits	419,328	1,369,728	2,544,192	4,520,488	6,747,840	9,383,040
DSP blocks	12	16	36	48	63	96
18-bit × 18-bit multipliers *(3)*	48	64	144	192	252	384
Enhanced PLLs	2	2	4	4	4	4
Fast PLLs	4	4	8	8	8	8
Maximum user I/O pins	366	500	718	902	1,126	1,170

2. I/O Structure

Stratix II devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures (M512 RAM, M4K RAM, and M-RAM blocks), and digital signal processing (DSP) blocks.

Each Stratix II device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR and DDR2 SDRAM, RLDRAM II, and QDR II SRAM devices. High-speed serial interface channels with dynamic phase alignment (DPA) support data transfer at up to 1 Gbps using LVDS or HyperTransportTM technology I/O standards.



The Stratix II IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- On-chip driver series termination
- On-chip termination for differential standards
- Programmable pull-up during configuration
- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The IOE in Stratix II devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

The IOEs are located in I/O blocks around the periphery of the Stratix II device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects

The Stratix II device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

Stratix II devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

In addition to the six I/O registers in each IOE, Stratix II devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM. In every Stratix II device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36.

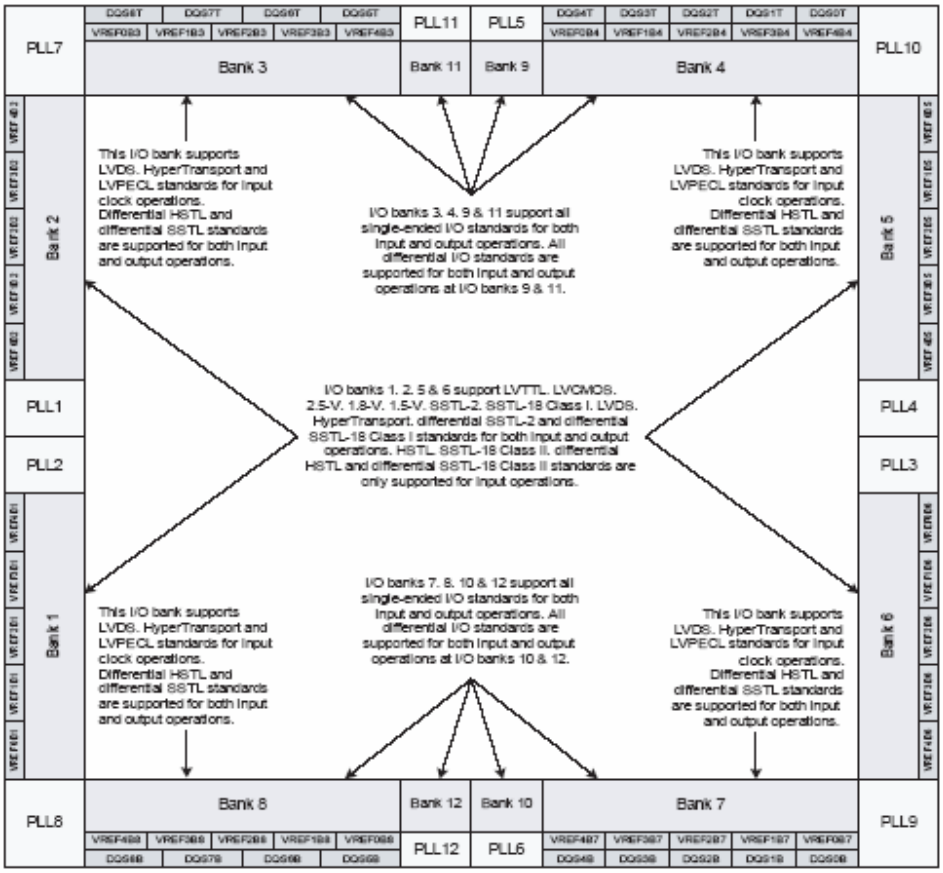
The output buffer for each Stratix II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that the user can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the IOH/IOL of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Each Stratix II device I/O pin provides an optional programmable pullup resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the VCCIO level of the output pin's bank.

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5-V LVCMOS	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X mode 1	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	2.5 *(3)*	N/A
LVPECL *(1)*	Differential	N/A	3.3	N/A
HyperTransport technology	Differential	N/A	2.5 *(3)*	N/A
Differential 1.5-V HSTL class I and II *(2)*	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-18 class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-2 class I and II *(2)*	Differential	1.25	2.5	1.25
1.5-V HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25

Stratix II device IOEs support the following I/O standards:

Stratix II devices contain eight I/O banks and four enhanced PLL external clock output banks. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS and HyperTransport inputs and outputs. These banks support all Stratix II I/O standards except PCI or PCI-X I/O pins, and SSTL-18 class II and HSTL outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, enhanced PLL external clock output banks allow clock output capabilities such as differential support for SSTL and HSTL.



Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different VCCIO level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same VCCIO for input and output pins. Each bank can support one VREF voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

Stratix II devices provide differential (for the LVDS or HyperTransport technology I/O standard) and series on-chip termination to reduce reflections and maintain signal integrity. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to eflections.

Stratix II devices provide three types of termination:

- Differential termination (RD)
- Series termination (RS) without calibration
- Series termination (RS) with calibration

On-Chip Termination Support	I/O Standard Support	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)
Series termination without calibration	3.3-V LVTTL	✓	✓
	3.3-V LVCMOS	✓	✓
	2.5-V LVTTL	✓	✓
	2.5-V LVCMOS	✓	✓
	1.8-V LVTTL	✓	✓
	1.8-V LVCMOS	✓	✓
	1.5-V LVTTL	✓	
	1.5-V LVCMOS	✓	
	SSTL-2 class I and II	✓	✓
	SSTL-18 class I and II	✓	✓*(1)*
	1.8-V HSTL class I	✓	
	1.8-V HSTL class II	✓	
	1.5-V HSTL class I	✓	
Series termination with calibration	3.3-V LVTTL	✓	
	3.3-V LVCMOS	✓	
	2.5-V LVTTL	✓	
	2.5-V LVCMOS	✓	
	1.8-V LVTTL	✓	
	1.8-V LVCMOS	✓	
	1.5-V LVTTL *(2)*	✓	
	1.5-V LVCMOS *(2)*	✓	
	SSTL-2 class I and II	✓	
	SSTL-18 class I and II	✓	
	1.8-V HSTL class I	✓	
	1.8-V HSTL class II	✓	
	1.5-V HSTL class I	✓	
Differential termination *(2)*	LVDS	✓	
	HyperTransport technology	✓	

The Stratix II architecture supports the MultiVolt I/O interface feature that allows Stratix II devices in all packages to interface with systems of different supply voltages. The Stratix II VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V VCCINT level, input pins are 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems).

The Stratix II VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

Table 2–20. Stratix II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)				
	1.5	1.8	2.5	3.3	1.5	1.8	2.5	3.3	5.0
1.5	✓	✓	✓ (2)	✓ (2)	✓				
1.8	✓ (2)	✓	✓ (2)	✓ (2)	✓ (3)	✓			
2.5			✓	✓	✓ (3)	✓ (3)	✓		
3.3			✓ (2)	✓	✓ (3)	✓ (3)	✓ (3)	✓	✓

References

[1] Virtex-4 Data Sheets: Virtex-4 Family Overview, http://direct.xilinx.com/bvdocs/publications/ds112.pdf
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[3] Stratix II Device Handbook, http://www.altera.com/literature/hb/stx2/stratix2_handbook.pdf
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