

Net-Ordering for Optimal Sharing of Cross-Capacitances in Nanometer Interconnect Design

ABSTRACT

This paper addresses the problem of ordering and sizing parallel wires in a single metal layer within an interconnect bus of a given width, such that cross-capacitances are optimally shared for circuit timing optimization. Using an Elmore delay model including cross capacitances for a bundle of wires, we show that an optimal wire ordering is uniquely determined, such that best timing can be obtained by proper allocation of wire widths and inter-wire spaces. The optimal order, called BMI (Balanced Monotonic Interleaved) depends only on the size of drivers for a wide range of cases. The paper also addresses wire ordering for minimizing circuit delay uncertainty induced by crosstalk. Monotonic ordering according to driver strength is shown to be advantageous, hence BMI order is recommended for both nominal delay and delay uncertainty minimization. Heuristics are presented for simultaneous ordering, sizing and spacing of bus wires. Examples for 90-nanometer technology are analyzed and discussed.

1. INTRODUCTION

Cross-capacitances between wires in interconnect structures have a major effect on circuit timing. The importance of this effect grows with technology scaling. Since cross-capacitance between two wires depends on inter-wire spacing and affects the delays of both wires, allocation of inter-wire spaces and wire widths becomes an optimization problem for bus structures under a total area constraint [1]. This paper addresses a more general problem, where delays in a bundle of parallel wires (with different drivers and loads) are minimized by choosing an optimal ordering of the nets, in addition to optimal allocation of wire widths and inter-wire spaces. The total width of the structure is a given constraint. The problem is motivated by the following example: assume a bus of $2n$ signals, n of them with strong drivers of size A (small effective output resistance) and n others with weak drivers of size B (large driver resistance). Two different arrangements of the bus, presented in Fig.1 a and Fig.1 b result in different circuit timing. In the second case inter-wire spaces are shared more effectively due to grouping of wires of each type together and as a result, circuit timing is better. This example demonstrates that wire ordering according to driver strength can improve results of delay minimization. Ordinary delay minimization ignores the net-ordering degree of freedom and treats the order of signals in the bus as given. A brute-force approach to determine the best ordering is to generate all signal permutations in the bus, and for each permutation solve the wire-width and space optimization problem. This approach, however, is computationally infeasible for practical buses. This paper proves the existence of an optimal wire ordering that yields best delay minimization after wire sizing and space allocation. The paper describes an efficient algorithm to find the optimal order for a wide range of practical cases. The paper also presents and evaluates heuristics for solving the most general cases of this problem.

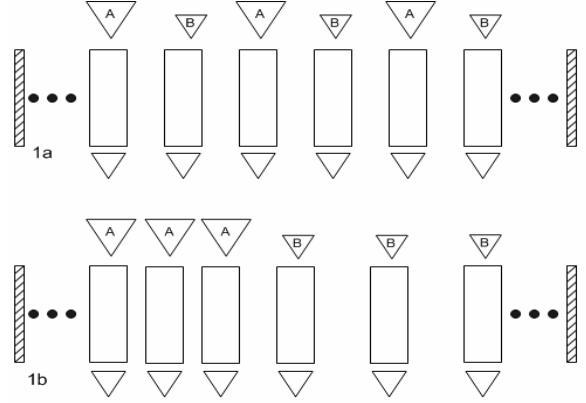


Figure 1. Two ways to order an interleaved bus. "A" – strong drivers (small resistance), "B" – weak drivers (large resistance). Case a: interleaved placement, all wires share equal spaces. Case b: sorted placement, wires with weak drivers share large spaces and wires with strong drivers share small spaces, with improved circuit timing.

1.1 Related Works

The problem of allocating widths and spaces to maximize performance in bus structures was proposed in [1]. The wire sizing problem has been addressed in [2] and [3] for a single net. Sizing and spacing multiple nets with consideration of coupling capacitance has been addressed in [4] for general interconnect layouts by converting cross capacitance to effective fringe capacitance. Coupling capacitance has been addressed explicitly in the context of physical design for minimizing crosstalk noise [5,6] or dynamic power [7]. Some authors treated the problem of throughput optimization in buses using uniform wire widths and spaces [21, 23,24]. Several variants of net-reordering have been applied for improving layout efficiency [8], and for noise reduction [6, 9, 10, 11, 12]. Swapping of wires for power reduction was applied in [13]. Vittal et al. [11] have suggested without proof to reduce capacitive coupling noise by sorting wires in order of driver strength, which is closely related to our results.

2. PROBLEM FORMULATION

2.1 Interconnect configuration and delay model

Circuit structure and notation are shown in Figure 2, illustrating n signal nets $\sigma_0, \dots, \sigma_{n-1}$ between two shield wires. S_i and S_{i+1} , respectively, denote spaces to the left and right neighbors of wire σ_i . W_i is the wire width. The length of all the wires is L . The total sum of wire widths and spaces is constrained to be A , representing the area available for laying out the bus.

$$g(\bar{W}, \bar{S}) = \sum_{j=0}^{n-1} W_j + \sum_{j=0}^n S_j = A \quad (2.1)$$

The delay Δ_i of signal σ_i can be calculated from the π -model equivalent circuit shown in Figure 3, where R_i is the effective output resistance of the driver, R_{w_i} is the wire resistance, C_{w_i} is the area and fringe capacitance, C_{c_i} and $C_{c_{i+1}}$ are the coupling capacitances to the right and left neighboring signals, and C_i is the capacitive load of the receiver's input.

Using an Elmore model with first order approximation for capacitances [19], the delay can be expressed as [18]:

$$\Delta_i = \left(a + \frac{b}{W_i} + \frac{dm_{i,j}}{W_i S_i} + \frac{dm_{i,j+1}}{W_i S_{i+1}} + \frac{eC_i}{W_i} + kR_i W_i + gR_i + \frac{hR_i m_{i,j}}{S_i} + \frac{hR_i m_{i,j+1}}{S_{i+1}} + R_i C_i \right) \quad (2.2)$$

where coefficients of wire widths, spaces, driver resistances and load capacitances are technology-dependent constants denoted a, b, d, e, k, g, h and $m_{i,j}$ is Miller factor between wires i and j . If all wires can switch simultaneously, the cross-capacitance terms are typically multiplied by a uniform $m_{i,j}$ of 2. For this worst-case assumption, inter-wire tradeoffs become very significant in optimizing the bus layout. For nominal delays, $m_{i,j} = 1$ is assumed. Derivations in this paper use this assumption. Despite its simplicity, this Elmore-based modeling approach is widely used in practical interconnect optimizations. A multiplicative factor of 0.7 is generally used to fit the Elmore model with 50% signal delay. With more elaborate empirical parameter tuning, the model accuracy can be improved further: In [18], good absolute accuracy versus circuit simulation has been obtained by applying a parameter fitting procedure to a very similar wire delay model.

2.2 Objective functions

Let f_1 given in (2.3) be the objective function we wish to minimize. f_1 denotes the sum of all signal delays. It is commonly used in early design stages since it captures the contributions of all signals to circuit timing.

$$f_1 = \sum_{i=0}^{n-1} \left(a + \frac{b}{W_i} + \frac{d}{W_i S_i} + \frac{d}{W_i S_{i+1}} + \frac{eC_i}{W_i} + kR_i W_i + gR_i + \frac{hR_i}{S_i} + \frac{hR_i}{S_{i+1}} + R_i C_i \right) \quad (2.3)$$

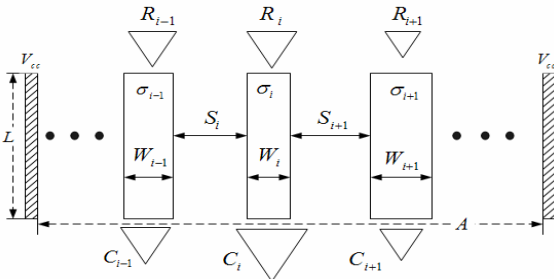


Figure 2. Interconnect configuration. The total bus width is A and the length is L . Each wire σ_i is of width W_i , with spaces to neighbors S_i and S_{i+1} , driven by a gate with effective resistance R_i and loaded by a gate with capacitance C_i .

For final performance tuning, it is appropriate to speed-up the slowest signal in the bus. The objective function for such MinMax optimization is

$$f_2 = \max_{0 \leq i \leq n-1} \left\{ \left(a + \frac{b}{W_i} + \frac{d}{W_i S_i} + \frac{d}{W_i S_{i+1}} + \frac{eC_i}{W_i} + kR_i W_i + gR_i + \frac{hR_i}{S_i} + \frac{hR_i}{S_{i+1}} + R_i C_i \right) \right\} \quad (2.4)$$

When required times of signals are specified, the corresponding objective functions are sum of slacks and the worst slack among all signals. Minimizing the sum of slacks is equivalent to minimizing f_1 . The case of minimizing worst slack can be transformed to minimizing worst wire delay f_2 . Section 3 covers optimization of f_1 , and section 4 considers optimization of f_2 . Section 5 discusses minimization of delay uncertainty metrics.

3. ORDERING OF WIRES FOR SUM OF DELAYS OPTIMIZATION

Let each wire have width W_i assigned as follows:

$$W_i = \frac{1}{\psi(R_i)}, \quad (3.1)$$

where ψ is a monotonically non-decreasing functions of R_i . Such assignment is practically common, as one attempts to balance the resistance of the driver and the resistance of the driven line and is known as "impedance matching". Notice that the case of uniform width wires is also covered by (3.1). f_1 is a function of $n+1$ variables S_i . The solution of minimizing f_1 under the constraint g (in (2.1)) implies

$$\frac{\partial f_1}{\partial S_j} + \lambda \frac{\partial g}{\partial S_j} = 0, \quad 0 \leq j \leq n \quad (3.2)$$

where λ is a Lagrange multiplier. Taking partial derivatives of f_1 and g with respect to S_i , substituting to (3.2) and rearranging we obtain

$$S_0^2 + S_2^2 + S_4^2 + \dots + S_{n-1}^2 = S_1^2 + S_3^2 + S_5^2 + \dots + S_n^2 \quad (3.3)$$

Notice that (3.3) holds regardless of wire widths, reflecting the fact that adjacent wires in the bus share common spaces. Equations (3.2) can be solved for S_i and λ . By

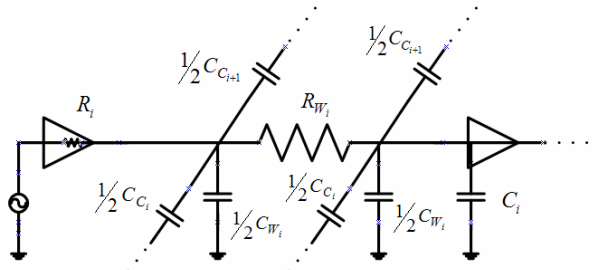


Figure 3. Equivalent circuit for calculating the i^{th} signal delay

substitution to (2.3), the minimal total sum of delays is expressed in terms of technology parameters, bus area constraint, wire driver resistances and load capacitances:

$$f_1 = na + b \sum_{i=0}^{n-1} \psi(R_i) + k \sum_{i=0}^{n-1} \frac{R_i}{\psi(R_i)} + g \sum_{i=0}^{n-1} R_i + e \sum_{i=0}^{n-1} \psi(R_i) C_i + \sum_{i=0}^{n-1} C_i R_i + \frac{1}{A - \sum_{i=0}^{n-1} \frac{1}{\psi(R_i)}} \left(\sum_{i=0}^{n-2} \sqrt{(d\psi(R_i) + d\psi(R_{i+1}) + hR_i + hR_{i+1})} + \sqrt{d\psi(R_0) + hR_0} + \sqrt{d\psi(R_{n-1}) + hR_{n-1}} \right)^2 \quad (3.4)$$

The quadratic last term of (3.4) depends on wire ordering. Consequently, there exists an order which minimizes the total sum of delays. The important conclusion from expression (3.4) is that **for wire widths assigned as in (3.1), wire ordering affects the minimal sum of delays via driver resistances, while the effect of load capacitances is order-insensitive.**

We now describe how to obtain the optimal order, and prove that this order is indeed the optimal one. Such order takes the driver with the largest resistance to reside at the center of the bus channel. The other drivers are taken in monotonically decreasing order of driver resistance, and located alternately on the left and right of the signal bus as shown in figure 4. We call the resulting order **BMI (Balanced Monotonic Interleaved)**. The advantage of BMI order stems from the fact that spaces are shared by wires with similar driver resistances, since the shield wires at the sidewalls effectively have zero-resistance drivers.

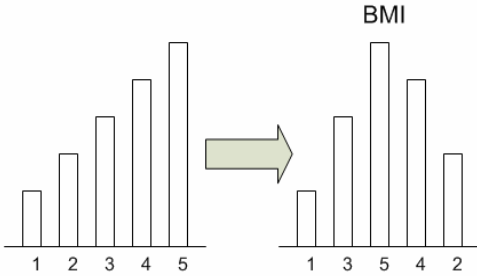


Figure 4. Building BMI order from a set of wires sorted according to driver resistance

Definition (BMI order): Given a bus of n signals with driver resistances R_0, \dots, R_{n-1} , the permutation of signals

$\Pi^* = (R_0, \dots, R_{n-1})$ is called **Balanced Monotonic Interleaved (BMI)** if it satisfies

$$R_0 < R_{n-1} < R_1 < R_{n-2} < \dots < R_{\lfloor \frac{n}{2} \rfloor - 1} < R_{\lfloor \frac{n}{2} \rfloor + 1} < R_{\lfloor \frac{n}{2} \rfloor}. \quad (3.5)$$

Notice that the reversed permutation which satisfies $R_{n-1} < R_0 < R_{n-2} < R_1 < \dots$, is also BMI.

Theorem 1 (Optimal order): Let wire width be a monotonic non-increasing function of driver resistance. The net-ordering yielding minimal sum of delays is then BMI.

Proof outline: Induction used on the number of wires. For one or two wires the order is undefined. For 3 wires, optimality of BMI order can be simply shown, based on properties of the sum

of square roots in the last term of (3.4). For additional wires, it can be shown by induction that after adding a new wire to the bus and rearranging the wires, BMI order will yield minimal total sum of delays. ■

The function $\psi(R)$ (3.1) needs to be selected carefully.

Although the theorem holds for equal-width wires, the goal is to approach the absolute minimum which could be achieved in the space of all orderings, wire width and wire spacing assignments. A simple, yet practical, wire width function is the inverse linear

$$W_i(R_i) = \frac{\alpha}{\beta + \gamma R_i}, \quad (3.6)$$

where α , β and γ are positive constants.

In the most general case, both wire widths and spaces can vary arbitrarily, yielding $2n+1$ equations. In this case the optimal wire ordering may depend on the values of capacitive loads and is not necessarily BMI. The next theorem defines conditions for optimality of BMI order in the most general case.

Theorem 2: For a given set of n wires $\{\sigma_0, \sigma_1, \dots, \sigma_{n-1}\}$, if each pair of wires σ_i and σ_j with driver resistances and load capacitances (R_i, C_i) and (R_j, C_j) satisfy $R_i > R_j$ and $C_i \leq C_j$, then the optimal order of this set of wires is BMI, under total sum of wire delays objective function.

If the conditions of the theorem are not met, the solution of the most general problem is very complex, as it involves the exploration of many permutations.

In order to make the computational effort reasonable, the following heuristic is proposed. It is based on the BMI order and yields near-optimal solutions. The complex optimization problem is divided into two successive simpler ones. First, theorem 2 is checked. If it is satisfied, the optimal order is BMI. Otherwise, the heuristic assigns wire widths by some parameterized monotonic non-increasing function such as (3.6). BMI order is now guaranteed to be optimal. Then continuous optimization is applied, exploring for the optimal values of inter-wire spaces and the width-function parameters (e.g. α , β and γ in (3.6)). This heuristic reduces time complexity of the optimization problem by factor of $O(n!)$ and reduces the number of unknown parameters from $2n+1$ to $n+p$, where p is the number of parameters in the width function. Experiments show that a well-chosen width-function yields orderings, widths and spaces that result in total sum of delays which is very close to the global optimum.

4. OPTIMAL ORDERING OF WIRES UNDER MAXIMUM DELAY OBJECTIVE

In this section, we examine ordering optimization for minimizing worst wire delay (2.4). It can be shown that the objective function of total sum of delays (2.3), and the objective function of worst delay (2.4) are the norms $\|\cdot\|_1$ and $\|\cdot\|_\infty$, respectively. Relying on the *norm equivalence theorem* we expect similar properties of both objectives. We aim to demonstrate optimality of BMI order for minimization of worst wire delay as well. However, since (2.4) is not differentiable, the

technique used for deriving optimal order for total sum of delays cannot be applied here.

Let's rewrite (2.2) in the following way, with $m_{i,j} = 1$:

$$\Delta_i = a + \frac{b}{W_i} + \frac{eC_i}{W_i} + kR_iW_i + gR_i + R_iC_i + \left(\frac{1}{S_i} + \frac{1}{S_{i+1}}\right) \cdot \left(\frac{d}{W_i} + hR_i\right) \quad (4.1)$$

It has been reported in [22] that after minimization of worst wire delay in a bus, delays of all wires are equal (equal-delay property). Using this property it can be shown from (4.1) that at the minimum delay point, wire width is a monotonically decreasing function of driver resistance. We can assume then that wire width is of the form (3.1), where $\psi(R_i)$ is convex or linear monotonic non-decreasing function in wire driver resistance. If in addition, we assume that all load capacitances are equal, then (4.1) can be rewritten in the form:

$$\alpha(R_i) + \beta(R_i) \left(\frac{1}{S_i} + \frac{1}{S_{i+1}}\right) = const \quad (4.2)$$

where $\alpha(R_i)$ and $\beta(R_i)$ are monotonic non-decreasing functions in R_i due to (3.1). From (4.2) it follows that stronger drivers will be assigned smaller inter-wire spaces and weaker drivers – larger inter-wire spaces. It matches our result for total sum of delays optimization, since the order providing the best sharing of inter-wire spaces is BMI. From (4.2) it follows immediately that for two adjacent wires

$$R_i > R_{i+1} \Rightarrow S_i > S_{i+2} \quad (4.3)$$

Property (4.3) can be used to determine optimal order for minimizing worst delay. In 3- and 4-wire cases BMI order has been proven analytically to be optimal. Since we don't have a complete proof for n wires, we have demonstrated experimentally that BMI order is optimal under maximum delay objective in most cases. We have created about 1000 random problem instances for 5 wires and 100 random problem instances for 6 wires and obtained BMI optimal order in most cases (the computational effort is infeasible for a larger number of wires). We have found that when not all load capacitances are equal, in about 80-85% of cases the optimal order is BMI. When all load capacitances are the same, the relative number of optimal BMI orders arises to 93-95%. We have found that with equal capacitances, the cases which deviated from BMI (7-5 %) were caused by effects of proximity to the shield wires at the sides, since spaces to the shield wires are not shared by a pair of signals. These effects become significant only if driver resistances are nearly equal. Further details are omitted here to save space.

5. OPTIMAL ORDERING OF WIRES FOR MINIMIZING DELAY UNCERTAINTY

Capacitive coupling is the primary source of noise in sub-micron digital CMOS and becomes worse with technology scaling. One of the most important characteristics of capacitive noise is delay uncertainty [20]. As in the case of delays where we dealt with total sum of delays and worst delay, we introduce two new objective functions for minimizing delay uncertainty:

$$f_3 = \sum_i \Delta t_{\max,i} \quad (5.1)$$

and

$$f_4 = \max_i \Delta t_{\max,i}, \quad (5.2)$$

where $\Delta t_{\max,i}$ is maximum delay uncertainty of signal i and can be expressed according to [20] as

$$\Delta t_{\max,i} = \Delta_i \log \left(\frac{V_p}{V_{dd}} + 1 \right) \quad (5.3)$$

V_p denotes peak noise [9]. Since peak noise is bounded, (5.1) and (5.2) are similar to the objective functions for minimizing total sum of delays and worst delay. Therefore, in this case it is reasonable to expect BMI optimal order. Thus, the same optimal order can minimize both delay and delay uncertainty characteristics. Examples for simultaneous minimization of delay and delay uncertainty objectives are shown in the next section.

6. RESULTS AND DISCUSSION

Numerical experiments for various problem instances were performed using 90 nanometer technology parameters calculated based on [15]. We used continuous optimization, and verified the results for allowed discrete sizes as required in modern layout tools. All the computation was performed in Matlab, and we have simulated some circuits before and after optimization to verify the delay improvement in Spice.

In the first experiment we evaluated 20 random problem instances using five signals. Each signal was assigned a driver randomly. The range of driver resistances was 100 Ω to 2 $K\Omega$ and load capacitances in the range 200 fF to 10 fF were assigned accordingly, to avoid excessive driver loading, such that the conditions of theorem 2 are always satisfied. For each problem the wire widths and spaces were optimized to yield minimum total sum of delays and minimum worst wire delay. This was done for all the $5!=120$ possible order permutations. The procedure was repeated for five different bus widths $A = 5, 10, 15, 20$ and $25 \mu m$, and five different bus lengths $L = 300, 500, 1000, 5000$ and $10000 \mu m$. The optimization impact (% improvement of best versus worst ordering, after width/space optimization, averaged for 20 random problem instances) is presented in Table 1. In each cell, the upper half cell (colored in gray) represents total sum of delays optimization and the lower half cell – worst wire delay optimization. Worst case crosstalk was assumed (i.e. Miller factor of 2). This experiment demonstrates that net ordering can significantly improve results of wire sizing and spacing optimization, especially when width is tightly constrained. The worst wire delay objective is affected more than sum of delays. Since theorem 2 is always satisfied in this example, all obtained optimal orders for total sum of delays minimization are BMI. On the other hand, only 80% of the obtained optimal orders for minimization of worst delay are BMI. It can be explained by influence of shield wires and varying load capacitances. For buses with 32 or 64 wires we could not perform the exhaustive search, but we confirmed that

BMI net ordering could improve worst wire delay by a significant percentage.

The second example shows in Table 2 the effect of signal ordering on buses with both strong and weak drivers. A bus of 7 signals with driver – load pairs of (100 Ω – 50 fF) or (1.9 K Ω – 5 fF) was examined for various numbers of the weak drivers. Bus width and length were A=12 μm and L=600 μm . As could be

Table 1
Average improvement (best vs. worst ordering) for random problem instances, in sum-of-delays (upper half-cell) and worst wire delay (lower half-cell)

	A=5 μm	A=10 μm	A=15 μm	A=20 μm	A=25 μm
L=300 μm	7.14%	6.13%	5.13%	4.25%	3.62%
	18.60%	13.23%	9.89%	7.68%	6.14%
L = 500 μm	8.41%	7.39%	6.31%	5.40%	4.71%
	20.73%	16.17%	12.91%	10.56%	8.79%
L = 1000 μm	9.51%	8.57%	7.65%	6.71%	5.97%
	22.14%	18.83%	16.05%	13.82%	12.03%
L = 5000 μm	9.65%	8.67%	7.97%	7.24%	6.63%
	20.64%	19.41%	17.75%	16.19%	14.79%
L=10000 μm	8.62%	7.91%	7.29%	6.59%	5.99%
	18.61%	18.05%	16.71%	15.37%	14.14%

expected, when the numbers of strong and weak drivers were about equal, signal ordering was most effective. The worst ordering was indeed the interleaved one described in Figure 1a, while the best one was clearly BMI. Miller factor of 1 was assumed (nominal delays).

Table 2
% improvement of best versus worst ordering, after width/space optimization, for a bus with two driver strengths

No. of weak drivers	Worst delay optimization	Sum of delays optimization
1	0.17%	0.39%
2	8.94%	4.81%
3	13.81%	8.12%
4	18.17%	11.19%
5	11.99%	7.52%
6	6.16%	3.55%

In the third example, delays obtained by exhaustive simultaneous ordering/sizing/spacing optimization are compared with results of heuristics using BMI order for total sum of delays objective. We used the same set of 20 instances as in example 1. The heuristic described in section 3 with the inverse linear width function (eq. 3.5) was applied. The results are presented in Table 3. For each value of bus width and length, the delay interval between the optimal result of exhaustive search and the optimal result of the heuristic is presented as a fraction of the delay

interval between best and worst results of the exhaustive search. As can be seen, by using parametric width optimization, the global minimum was approached as closely as 0.37% on average.

Table 3
Relative delay distance between heuristic result and the global minimum

	A=5 μm	A=10 μm	A=15 μm	A=20 μm	A=25 μm
L=300 μm	0.16%	0.14%	0.42%	0.19%	1.34%
L = 500 μm	0.20%	0.25%	0.15%	0.18%	0.29%
L = 1000 μm	0.13%	0.14%	0.19%	0.28%	0.35%
L = 5000 μm	0.17%	0.21%	0.28%	0.45%	0.65%
L =10000 μm	0.25%	0.28%	0.38%	0.52%	0.66%
Average	0.182%	0.204%	0.284%	0.324%	0.658%

In the last experiment, we analyze minimization of delay uncertainty objective functions. We generated 20 random instances of 8 wires with wire drivers chosen randomly from the range 100 Ω to 2 K Ω and all load capacitances are 10 fF. The width of the bus is 18 μm . Miller factor of 1 was assumed. For each set of wires, we assumed worst order similar to Fig 1.a, and BMI order has been taken as the best one. After that, we performed optimal wire width and inter wire space allocation for each case, calculated relative differences in objective functions between these two orders and averaged all differences. The operation was repeated for 5 different bus lengths, as presented in Table 4. As can be seen, ordering improved delay uncertainty in all cases by about 30-40%. These experiments demonstrate the effectiveness of BMI ordering for both delay and delay uncertainty minimization.

Table 4
Advantage of BMI order vs. worst order

Bus width, μm	Total sum of delays impact, %	Worst delay impact, %	Total sum of delay uncertainty impact, %	Worst delay uncertainty impact, %
300	2.73	6.70	29.82	37.73
500	3.53	9.27	30.34	39.97
1000	4.44	12.14	30.83	40.56
5000	4.82	14.03	30.18	35.07
10000	4.36	13.21	28.72	34.27

7. CONCLUSION

We have shown that reordering of wires can improve results of timing optimization by wire-sizing and spacing, for a wiring channel of constrained width. It has been shown that the optimal order of wires generally depends on both wire driver resistances and load capacitances. Analysis of sum-of-delays minimization (which is equivalent to minimization of the average signal delay) with shield wires at the sides of the channel, showed that when wire widths are uniform or are specified by a monotonic non-increasing function of wire driver resistance, the optimal order is BMI (Balanced Monotonic Interleaved) and depends on driver resistances only. The general problem of simultaneous net-ordering, wire-sizing and spacing optimization was presented, and solution heuristics were proposed, reducing complexity by factor of $O(n!)$, and the number of optimization variables from $2n+1$ to $n+p$. Numerical experiments demonstrated heuristic results approaching the global optimum within approximately 0.5%. Ordering optimization has been shown to be advantageous for simultaneous minimization of total sum of delays, worst delay, sum of uncertainties and worst delay uncertainty.

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