Statistical Gate Delay Model Considering Multiple Input Switching

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Abstract

There is an increased dominance of intra-die process variations, creating a need for an accurate and fast statistical timing analysis. Most of the recent proposed approaches assume a Single Input Switching model. Our experiments show that SIS underestimates the mean delay of a stage by upto 20% and overestimates the standard deviation upto 26%. We also show that Multiple Input Switching has a greater impact on statistical timing, than regular static timing analysis. Hence, we propose a modeling technique for gate delay variability, considering MIS. Our model can be efficiently incorporated into most of the statistical timing analysis frameworks. On average over all test cases, our approach underestimates mean delay of a stage by 0.01% and overestimates the standard deviation by only 2%, hence increasing the robustness to process variations. Our modeling technique is independent of the deterministic MIS model, and we show that its sensitivity to variations in the MIS model is small.

Categories and Subject Descriptors
B.8.2 [Performance and Reliability]: Performance analysis
General Terms
Algorithms, performance, reliability

1 Introduction

Static Timing Analysis (STA) has become the mainstay of performance verification of today's designs. It functions on the principle of propagating arrival times from the inputs to the outputs of a circuit. Unlike timing simulation, STA requires only a single pass through the circuit to obtain the final delay and hence has a linear run-time complexity with circuit size. However, STA trades off its efficient run-time with a conservative estimate of the circuit delay. Moderate conservatism is acceptable for performance analysis, as an optimistic estimate can lead to timing failures while a conservative estimate will, at worst, lead to over design. STA tools have gained extensive popularity due to their ability to perform fast and thorough timing checks on even the largest chips.

Since the advent of STA, it has faced a number of accuracy issues related to false paths, multiple input switching (MIS) and slope propagation. Considerable amount of work has been performed to address these issues in the past decade. In recent technologies, the variability of circuit delay due to process variations has become a significant concern. As process geometries continue to shrink, the ability to control critical device parameters is becoming increasingly difficult, and significant variations in device length, doping concentrations, and oxide thicknesses have resulted. Traditional corner-analysis has been successfully used in the past to model die-to-die variations, however, it is not able to accurately model variations within a single die.

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In this paper, we focus on delay variability due to process variations. Process variations are broadly classified as inter- and intra-die variations. Inter-die variations are changes in device features that are manifested between different die, across wafers and wafer lots, whereas intra-die variations are fluctuations in device features within a single die. Intra-die variations exhibit spatial correlations, where devices close to each other have a higher likelihood of having similar features.

With increasing awareness of process variations, a number of techniques were developed which model gate delay variations and perform Statistical Static Timing Analysis (SSTA). These can be classified into *block-based* analysis approaches [1-7] and *path-based* analysis approaches [8-10]. These methods aim to obtain the probability distribution associated with the path delay or circuit delay random variables. Unlike path-based analysis, block-based analysis requires the computation of a statistical maximum of input arrival time random variables, for a multi-input gate. The computation of the exact statistical maximum is difficult, and introduces errors due to the lack of exact correlation information between the input arrival time random variables. Obtaining the exact correlation information requires extensive computation and storage of dependencies. Some of the sources of this correlation are circuit reconvergence, and spatial correlation.

Block-based SSTA approaches, which address the issues of reconvergence and spatial correlation, have been proposed in [1-7]. In [4] it was shown that ignoring correlations due to reconvergence is conservative and produces an upper bound on the circuit delay cdf (cumulative distribution function). Recently in [1], the authors proposed a novel method for propagating arrival times as piecewise linear cdfs, and also showed that the conservatism introduced by ignoring reconvergence is small. In [2][3], novel methods for handling spatial correlation were proposed. In most of these approaches, a lot of importance was given to the correct computation of the statistical maximum, taking into consideration proper correlations. However, one of the most important sources of error in the computation of the statistical maximum is due to multiple input switching (MIS), which has been completely ignored in these previous methods.

MIS is a significant problem, and neglecting it can introduce large timing errors. The problem arises when multiple inputs of a

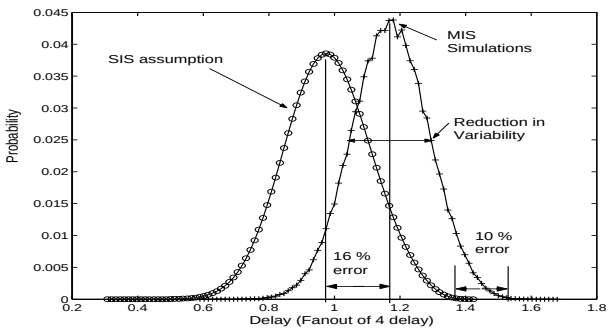

Figure 1. Shows errors in the statistical delay computation assuming SIS

gate switch in temporal proximity, in which case the max delay is more than the corresponding pin-to-pin delays, or the min delay is lesser than the pin-to-pin delays. Considering MIS makes the timing analysis conservative, as the probability of having an MIS event on every multi-input gate along a critical path may be very small. Some very useful approaches for the MIS problem were suggested in [11,12] for deterministic STA, but no work has yet been done for SSTA. MIS needs to be incorporated into SSTA because past techniques, such as corner-analysis, typically model intra-die process variations conservatively, and will be even more conservative assuming the worst case MIS. Also, neglecting it completely could be optimistic. Note that due to process variations, arrival times which were nominally far apart in STA, could get close with a finite probability in SSTA, hence giving rise to a possible MIS situation.

In this paper, we propose a statistical gate delay model that includes MIS effects and which can be easily incorporated into SSTA. Our work is focussed on including MIS into the maximum delay computation, however, our modeling technique and algorithms can be applied to the minimum delay case too. We evaluate the effect of MIS on the statistical delay computation through a multi-input gate considering zero mean input arrival time pdfs. We compare the output delay distribution obtained by assuming MIS and performing SPICE based Monte-Carlo simulations, with the Single Input Switching (SIS) assumption, and demonstrate the large difference between the two approaches as shown in Figure 1. Our results on a number of test cases show that SIS underestimates the mean delay of a gate by upto 20% and overestimates the standard deviation of gate delay upto 26%.

We then propose a technique to model gate delay variability, in the presence of arrival time PDFs at the inputs of a multi-input gate. We also propose algorithmic methods to incorporate our model into SSTA. We test our approach on a number of benchmark circuits, and demonstrate its efficiency and accuracy. On average, our approach underestimates mean delay of a gate by 0.01% and overestimates its standard deviation by only 2%. The presence of MIS significantly reduces the delay variability of a circuit in absolute terms and also as a percentage of mean and hence increases the robustness of the circuit, which is a key observation from our work. With the proposed model, it is possible to accurately capture this increased robustness in SSTA.

The remainder of this paper is organized as follows. In Section 2, along with some basic definitions, we present our golden model and our motivation for modeling MIS in statistical timing. In Section 3 we present our approach for statistical modeling of MIS, and its application to SSTA. In Section 4 we present our results, and compare our MIS approach to the best possible SIS approach. Finally, in Section 5 we draw our conclusions.

2 Modeling Assumptions

In this section, we explain our modeling assumptions and experimental setup.

In this paper, we consider the combined impact of MIS and intra-die process variations on gate delay. After a chip has been manufactured the process parameters have a fixed deterministic value, however, at design time, process parameters, delay and arrival times are considered as random variables (R.V.s). These R.V.s are represented either by continuous or discrete probability density functions (pdfs), as shown in Figure 2.

In this paper, we consider process variability due to the transistor gate lengths L_e of a gate. We assume gaussian distributions truncated at their 3σ points, for statistical modeling of L_e. Also, in our analysis we focus on the independent component of intra-die variations, which signifies that transistors in a gate can vary independently of each other. If necessary, correlation of transistor gate lengths in a single gate could be modeled by expressing the total gate length of a transistor as the sum of an independent component and a shared, dependent component.

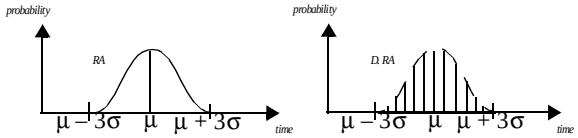

Figure 2. a) Delay/Arrival time pdf b) Discretized pdf

2.1 Current Methodology and Our Formal Model

SSTA works on the principle of propagating arrival time pdfs through the circuit. In abstract terms, this is performed using convolution and maximum operations, where the output arrival time pdf for a single-input gate is obtained by convolving its gate delay pdf with the input arrival time pdf, and that for a multi-input gate is obtained by taking the statistical maximum of its input arrival time pdfs convolved with the pin-to-pin delay pdfs. The computation of the statistical maximum at a multi-input gate assumes SIS, meaning that two or more inputs of a gate do not switch in close proximity of each other, or if they do, they do not affect the pin-to-pin delay of each other. We show through our experiments that assuming SIS leads to very optimistic estimates of the max circuit delay, and pessimistic estimates of delay variability.

As shown in Figure 3a, we first obtain the arrival time pdf A_s at the output O of gate g_1 considering SIS. The arrival times at inputs I_1 and I_2 of gate g_1 are considered to be zero mean R.V.s represented by pdfs A_1 and A_2, respectively. Assuming SIS, we propagate pdf A_1 through the arc I_1 to O, to obtain pdf A_{s1}, and similarly propagate A_2 through the arc I_2 to O, to obtain pdf A_{s2}. Propagation is performed by convolving the pin-to-pin delay pdf of the gate with the corresponding input arrival time pdf. Convolution assumes independence between the two convolved pdfs. However, unlike some of the previous approaches [1][4][6][7] we do not consider the edge delay pdfs of a single gate to be independent, and our simulation results validate this. Finally, we take a statistical maximum of the two pdfs A_{s1} and A_{s2} considering the appropriate correlations, to obtain the final output arrival time pdf A_s.

When considering MIS, on the other hand, we obtain the output arrival time pdf A_m at the output O of gate g_1 as shown in Figure 3b.

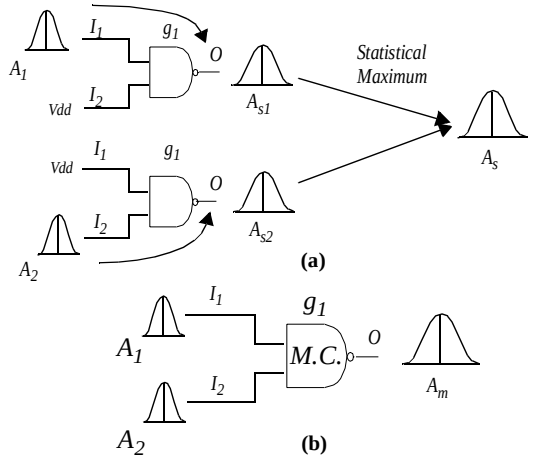

Figure 3. a) Current Statistical Assumption b) Exact Simulation

We use the same pdfs A_1 and A_2 for the input arrival time R.V.s, as used in the SIS case. But instead of propagating these pdfs forward, we perform SPICE based Monte-Carlo simulations on A_1, A_2 and the transistor gate lengths L_e's of gate g_1, to obtain the A_m pdf. We consider this to be exact and our formal model for comparisons.

Note that for SIS, the delay pdfs for arc I_1 to O and arc I_2 to O, are obtained through SPICE based Monte-Carlo simulations on the different L_e's of gate g_1, to avoid modeling errors. These arc delay pdfs tend to be correlated, with a certain correlation coefficient ranging between 0 and 1. Hence, the statistical maximum is performed considering the exact correlation between A_{s1} and A_{s2}, to obtain the best possible SIS result. This is compared against the MIS result obtained by Monte-Carlo simulations. The output delay PDFs obtained by both the methods are shown in Figure 1. The large difference between the SIS and MIS cases motivates the need for considering MIS in SSTA. Note that we do not consider variability of slope in our current experiments, but our framework can be extended to include this as well. In the following section, we describe our proposed approach for modeling the MIS gate delay pdfs and show how it can be incorporated into SSTA.

3 Proposed MIS Approach

As seen in the previous section, our formal model for capturing the effect of MIS on statistical delay calculation is based on SPICE based Monte-Carlo simulations. As this method is computationally expensive, we need faster modeling solutions.

In this section, we present a simple yet effective method for modeling the effects of MIS on the statistical max delay calculation, which can be easily included in the current statistical algorithms framework. We assume in our analysis that we consider cases where MIS causes an increase in the gate delay, which is important for max delay analysis. Cases where MIS causes a decrease in the gate delay are useful for min delay analysis and can be modeled similarly. The gate delay R.V. is a function of different instances of input arrival time R.V.s. Hence, in our modeling technique we model the gate delay R.V. as a function of input arrival time instances.

A straightforward approach for modeling the gate delay R.V.s would be to store a pdfs of the gate delay for to each possible difference between the input arrival time instances of a gate. However, in this case the storage requirement would be extremely high and grows exponentially with the number of gate inputs. Instead, if we make a gaussian approximations for the shape of these pdfs, we need to store only the mean and standard deviations of gate delay pdfs for each combination of input arrival time instances. This however, still has a high storage requirement.

Hence, we propose a more compact modeling technique where we store the mean and standard deviations for each SIS arc only. Based on some observations, we then propose an approximate method for obtaining the standard deviations for all other scenarios of input arrival times. We also make approximations for the mean of the gate delay pdfs, by assuming that a deterministic MIS model is available, and that this can be used to approximate the mean due to L_e variations. We will show the validity of this assumption.

3.1 Modeling MIS for SSTA

We now propose our modeling approach, which assumes that a deterministic model for MIS is available, similar to [11], from which we can obtain delay "push-out" *D.PO.* values for various combinations of input arrival time instances. (*D.PO.* is defined as the additional delay introduced in the SIS delay of a particular input-to-output arc due to the temporal proximity of another input). It is important to note that we are not trying to solve the deterministic MIS problem, but given a deterministic model, trying to solve the statistical gate delay problem. Initially, we assume that the deterministic MIS model is perfect, although later in Section 3.5 we check for robustness of our model incase the deterministic MIS prediction has errors.

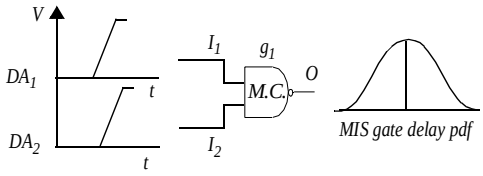

Figure 4. delay pdfs obtained with input arrival time instances for MIS

We start with our model for a two-input gate, and then extend it for multiple inputs. We first performed several experiments to determine the gate delay pdfs for different combinations of input arrival time instances DA_1 and DA_2 at inputs I_1 and I_2, by performing a SPICE based Monte-Carlo simulation on the L_e's of gate g_1 as shown in Figure 4. We then plotted the mean and standard deviations of the gate delay pdfs for different values of DA_2 - DA_1 as shown in Figure 5. The standard deviation of the MIS gate delay pdfs σ_m, was the least when DA_1 and DA_2 were perfectly aligned. As the distance between DA_1 and DA_2 was increased in either direction, σ_m converged with the standard deviation of SIS arc delay pdf σ_s, corresponding to the later of the two arrival times DA_1 and DA_2. Similarly the mean of the gate delay pdfs μ_m, was the maximum when DA_1 and DA_2 were perfectly aligned. This is shown in the bottom chart of Figure 5. As the distance between DA_1 and DA_2 was increased in either direction, μ_m converged with the mean of the SIS arc delay pdf μ_s, corresponding to the later of the two arrival times DA_1 and DA_2, making the SIS modeling accurate for those situations.

Based on these observations, in our modeling approach we first approximate the mean of the MIS delay distribution μ_m, using the SIS delay corresponding to the latest of the two arrival time instances DA_1 and DA_2, added with the *D.PO.* of the arrival time combination. The *D.PO.* value is assumed to be obtained from a deterministic MIS model, based on ΔDA, where ΔDA is DA_2 - DA_1. This approximation is possible since, μ_m has a weak depen-

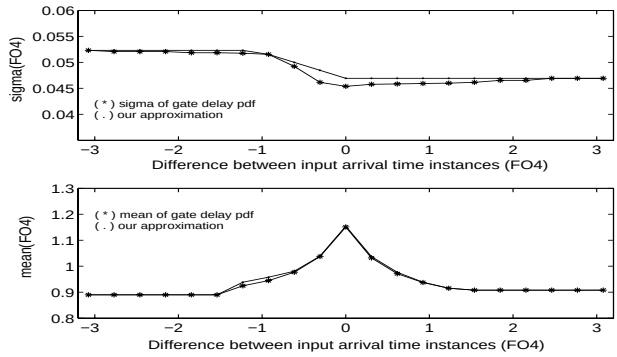

Figure 5. Change in standard deviation and mean of the MIS gate delay pdf, for different input arrival times

dence on the standard deviation of transistor gate lengths, and we can safely ignore this dependence. The bottom chart of Figure 5 shows the difference between μ_m and its approximation using a deterministic MIS model. The error is negligible in most cases.

Also, according to our observation, dependence of σ_m on ΔDA, can be captured by using approximation techniques based on σ_s and ΔDA, without introducing significant errors. Hence, we then approximate σ_m, by a weighted sum of sigma of the two SIS delay distributions σ_{s1} and σ_{s2} as follows :

$$\sigma_m = \sigma_s \cdot \alpha + \sigma_{s,min} \cdot (1 - \alpha) \quad \text{(EQ 1)}$$

where,

$$\alpha = |\Delta DA| / X \quad \text{(EQ 2)}$$

$$\sigma_{s,min} = min(\sigma_{s1}, \sigma_{s2}) \quad \text{(EQ 3)}$$

$$If""\Delta DA < 0, \sigma_s = \sigma_{s1} \ , If""\Delta DA > 0, \sigma_s = \sigma_{s2} \quad \text{(EQ 4)}$$

X is the distance between arrival time instances beyond which the effect of MIS becomes negligible for a multi-input gate, also defined as the proximity window in [11]. If $|\Delta DA| > X$, $|\Delta DA|$ is considered to be X, signifying the SIS case. We can see that α ranges from 0 to 1, and when $\Delta DA \geq X$, $\alpha = 1$, and $\sigma_m = \sigma_{s2}$, similarly when $-\Delta DA \geq X$, $\alpha = 1$, and $\sigma_m = \sigma_{s1}$. Hence, our model captures the SIS corner cases perfectly, and makes a linear approximation for the MIS cases. When the deterministic input arrival times are perfectly aligned, i.e. when $\Delta DA = 0$, $\alpha = 0$, and σ_m is $min(\sigma_{s1}, \sigma_{s2})$. The top chart of Figure 5 shows the difference between σ_m and our approximation. Again, the error is negligible in most cases.

3.2 Statistical Static Timing Analysis using our Model

We now show how our proposed model can be applied to SSTA. As shown in Figure 6, we consider input arrival times at inputs I_1 and I_2 of gate g_1 to be random variables represented by discrete pdfs, and denoted by $D.RA_1$ and $D.RA_2$, respectively. These discrete pdfs are discretized versions of pdfs A_1 and A_2 as shown in the experimental setup of Figure 3.

We start with enumerating all pairs of arrival time instances of discretized pdfs $D.RA_1$ and $D.RA_2$. For simplicity of the example, we assume the input arrival time pdfs to be uncorrelated (similar assumption was made for our formal model in Section 2), however, our modeling technique can be used for completely or partially correlated arrival time pdfs. Then, for each pair of arrival time instances at the inputs, we obtain the MIS gate delay pdf using our above model. The standard deviation of the MIS gate delay pdf is obtained by using EQ1, and mean is obtained using a table look-up for deterministic MIS, based on ΔDAs. However, it is important to note that our modeling is independent of the deterministic MIS model, and we can use any MIS model. We then shift the MIS gate delay pdf by adding to it the maximum of the two input arrival time instances. The shifted pdf is scaled by the joint probability of the pair of input arrival time instances. Finally, we perform a sum of all the shifted and scaled pdfs, to obtain the final output delay pdf.

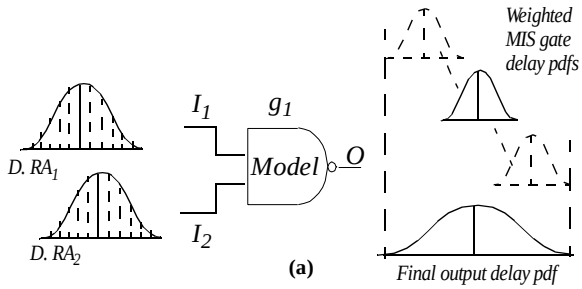

Figure 6. Computation of the output delay pdf using our modeling technique

3.3 Application of our Model to Multiple Inputs

We now generalize our proposed framework for more than two inputs. A straightforward method for extending our approach would be to enumerate all combinations of arrival time instances for each input. For each such combination, a shifted and scaled MIS gate delay pdf could be obtained and summed, similar to Section 3.2. However, this method has an exponential run-time complexity with the number of inputs. Hence, we propose a heuristic approach for multiple inputs, using a repeated application of our two-input model.

Consider a three-input gate, with input arrival time pdfs *A*, *B* and *C* associated with each of the three inputs, respectively. We first order these input pdfs with respect to their mean values, with the lowest mean being the first. Assume that *A* is first in the ordering, then *B*, and *C* is last. We start with the first two input pdfs *A* and *B*, and apply our two-input model to obtain the output delay distribution. We compare this distribution with that of *B* switching alone, obtained by SIS propagation. The difference between the mean of the two distributions is stored as $\Delta\mu_{ab}$, and the difference between the variances is stored as $\Delta\sigma^2_{ab}$.

Then, we again apply our two-input model successively to input pdfs *B* and *C*. However, this time we capture the effect that *A* has on *B*, while combining *B* and *C*. First, we modify *B* by reducing its variance by $\Delta\sigma^2_{ab}$. Next, while combining *B* and *C*, we enumerate all pairs of arrival time instances. For each pair (B_i, C_i), we obtain the corresponding mean value μ_m, and add it to the maximum of (B_i+$\Delta\mu_{ab}$, C_i), to obtain the shifted μ_m. We obtain σ_m again by using EQ1-EQ4. These pdfs are scaled by the joint probability of the arrival time pair (B_i, C_i). Finally, we sum all the shifted and scaled pdfs to obtain the final output delay pdf. Hence, our final output pdf captures the combined effect of all three inputs switching together. Note that our heuristic correctly captures all the corner cases, where the distance between the means of *A*, *B* and *C* is large. Also, for most of our test cases with input pdfs perfectly aligned, this heuristic was found to work well, giving rise to only a small amount of error.

We performed SSTA by applying our modeling technique to a large number of benchmark cases, and there was a very good match between the SPICE based Monte-Carlo simulations for MIS, and our SSTA approach. Figure 7 shows the PDFs of the output gate delay distribution for the MIS and SIS case, and also the MIS distribution obtained by our modeling approach.

3.4 Algorithmic Complexity

We now evaluate the algorithmic complexity of MIS modeling as compared to SIS modeling. In terms of storage, the computation for σ_m requires that all σ_{si} are stored, which is the same as SIS. Similarly, for the computation of μ_m, the storage requirement is the same as the deterministic MIS model that is used. For a specific pair of input arrival times, the computation time for obtaining σ_m is again minimal, as seen in EQ1-EQ4. However, the computational bottleneck lies in using this statistical MIS information, to obtain the output arrival time pdf. As we described in the previous section, the input arrival time pdfs are discretized and we perform a complete enumeration of all combinations of arrival time instances. Note that we do this for pairs of gate inputs in successive fashion. Hence, the complexity of this approach is n^2, where n is the size of the discretized pdf. We then add the computed pdf for that arrival pair to the output pdf at the ouptut node using a weighted summation. This procedure has linear complexity with n. Thus, the overall complexity of the approach is $O(n^3)$. This compares relatively favorably with the computation of the output pdf in the SIS case, which has complexity $O(n^2)$. Note also that previously it was shown that the number of necessary discretization is typically small, in the range of 5 - 10. Also, the run time complexity is linear with the number of gate inputs, which is an important property of the proposed method.

3.5 Robustness

We performed several experiments to test the robustness of our modeling approach. In one set of experiments, we verified the robustness of our model with σ_s characterization errors. We added a +/- 20% error in the computation of σ_s, which increased the error in the sigma of the output pdf. However, as compared to SIS assumption the error was still small. Hence, we still obtain an increased robustness of the delay to process variations as compared to SIS.

In another set of experiments, we introduced variability in the delay push-out *D.PO*. estimation. This was to simulate the current scenario, where most of the suggested deterministic models for MIS, have certain errors. Our models correctly predicted the output delay distribution with minimal errors for as much as +/- 20% errors in the delay push-out. This is because the errors occur randomly for different input arrival time combinations, and in most cases tend to cancel out the effect of each other. Hence, we show that our modeling technique is robust, and its sensitivity to variations in the deterministic MIS model is small. The results are shown in Table 3.

4 Results

We performed extensive SPICE based Monte-Carlo simulations over 150 different test cases of multi-input gates, and obtained data for SIS simulations and the MIS simulations. We used this statistical data to show the difference between the SIS output pdf and MIS output pdf, assuming zero mean input arrival time random variables, as shown in Figure 1. We then performed SSTA on all the test cases using our proposed modeling approach for MIS, and compared it against SPICE based Monte-Carlo, as shown in Figure 7.

The test cases were generated by choosing different logic gates, with varying number of inputs and power levels, from a standard cell library of an industrial 90nm technology. For each of these standard cells, we varied the output loading and input slope, to include scenarios where the difference between SIS and MIS, was both low and high both. We also obtained the input arrival time pdfs, and their standard deviations from a working version of a statistical timing tool, for intra-die variations. 80,000 runs of Monte-Carlo simulations were performed in SPICE to obtain our formal model, by varying the L_e of the transistors in the gate, and the input arrival time instances.

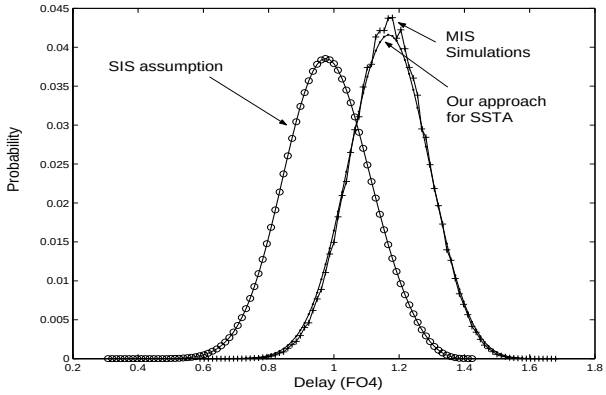

Figure 7. PDFs of SIS and MIS simulations, and PDF obtained by MIS modeling

Figure 8 shows the % errors in mean and standard deviations of the SIS delay pdf as compared to our formal model, over all test cases, with the means of input arrival time pdfs perfectly aligned. The largest % error in the SIS mean is -20%, whereas the largest % error in the SIS sigma is 26%. The average % errors over all test cases, is -10.22% for the mean and 13.15% for the sigma.

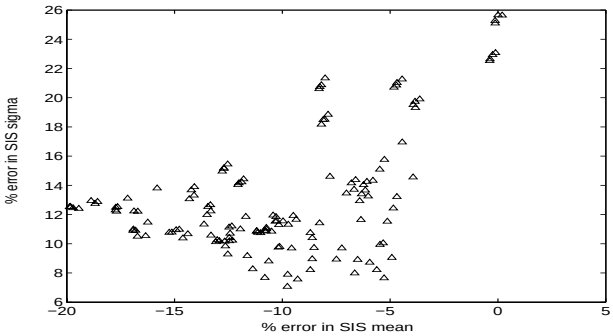

Figure 8. % Errors in mean and standard deviations between SIS and MIS simulations over all test cases

Figure 9 shows the % errors in mean and standard deviations of the delay pdfs obtained by performing SSTA using our model as compared to our formal model, over all test cases. The largest % error in the mean is 0.20%, whereas the largest % error in the sigma is 7%. The average % error over all test cases is 0.01% for the mean and 2.07% for the sigma.

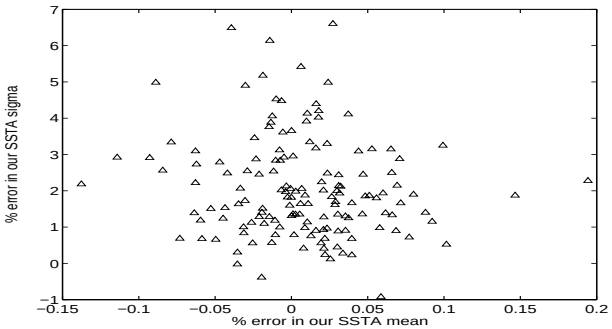

Figure 9. % Errors in mean and standard deviations between our SSTA and MIS simulations over all test cases

Table 1 shows the mean and sigma values for the output delay pdfs, obtained by SIS, MIS, and our SSTA, for some randomly chosen benchmark cases. *Column* 2 shows the mean and sigma values of the output delay pdf obtained by SIS simulations. *Column* 3 shows the mean and sigma values of the output delay pdf obtained by MIS simulations. *Column* 4 shows the mean and sigma values of the output delay pdf obtained by performing SSTA using our model. *Column* 5 shows the % errors in mean and sigma values of the output delay pdf obtained by SIS simulations as compared to MIS simulations. *Column* 6 shows the % errors in mean and sigma values of the output delay pdf obtained by our SSTA approach as compared to MIS simulations.

Table 1. Results for randomly selected benchmark ckts w/ input pdf means perfectly aligned

B.M.	SIS mean/ sigma (FO4)	Monte-Carlo mean/sigma (FO4)	Model mean/sigma (FO4)	%diff SIS mean/ sigma	%diff Model mean/sigma
B1	1.68/0.136	1.79/0.123	1.79/0.124	-6.50/9.93	-0.01/0.62
B2	0.89/0.130	0.96/0.114	0.96/0.116	-6.97/14.1	0.03/1.34
B3	1.10/0.132	1.17/0.116	1.17/0.118	-6.08/13.9	0.03/1.98
B4	1.40/0.148	1.46/0.126	1.46/0.128	-4.40/16.96	0.05/1.21
B5	1.66/0.160	1.66/0.130	1.66/0.132	-0.09/22.94	-0.02/1.17
B6	1.82/0.160	1.95/0.143	1.95/0.143	-6.38/11.76	0.03/0.01
B7	2.04/0.166	2.15/0.149	2.15/0.149	-5.11/11.34	-0.05/0.01
B8	1.13/0.143	1.19/0.118	1.19/0.120	-4.41/20.77	0.07/1.29

Table 2 shows the % error values in mean and sigma values for the output delay pdfs, obtained by SIS and our SSTA as compared to MIS simulations over all benchmark cases. The different cases shown in this table are generated by changing the relative distance between the means of the input arrival time pdfs. *Column* 1 shows the values for relative distance between input pdf means. *Column* 2 and 4 show the Average % error in SIS mean and sigma over all test cases for the corresponding relative distance. *Column* 3 and 5 show the Average % error in our SSTA mean and sigma over all test cases. We can see that on an average we perform better than the SIS assumption in both the mean and sigma predictions.

Table 2. Results for different alignment of input pdf means as an average over all benchmark cases

input skew (FO4)	Average% error in SIS mean	Average% error in our mean	Average % error in SIS sigma	Average % error in our sigma
0.00	-10.22	-0.03	13.15	2.07
0.08	-9.73	-0.01	15.75	2.26
0.16	-8.88	-0.01	18.50	2.40
0.24	-7.76	-0.008	20.43	2.47
0.32	-6.51	-0.008	20.93	2.50
0.40	-5.25	-0.007	20.12	2.51
0.48	-4.05	-0.006	18.42	2.49
0.56	-2.96	-0.003	16.32	2.45
0.64	-2.04	-0.003	14.16	2.42
0.72	-1.20	-0.003	12.10	2.39

Table 3 shows the robustness of our MIS model for SSTA. We test for %errors in the mean and standard deviation of the output delay pdf by our SSTA, against the MIS simulations. We assume that the deterministic MIS model we are using has an error in predicting the *D.PO.* values. The % error in the *D.PO.* is shown in *Column* 1. *Column* 2 shows the % error in the σ_s values. *Column* 3 and 4 show the average % error in mean and standard deviation.

Table 3. Results for variations in the deterministic MIS model, and SIS sigma characterization

% error in *D.PO.*	% error in SIS characterization	Average % error in our SSTA mean	Average % error in our SSTA sigma
+/- 10	0	0.007	2.38
+/- 20	0	0.04	3.28
0	+/- 10	0.00009	4.83
0	+/- 20	0.00006	7.75

5 Conclusions

In this paper, we have addressed a novel aspect of statistical timing analysis. We have shown through our simulations the amount of error introduced by the current statistical assumption of Single Input Switching at every stage. A key result of our experiments was to show that SIS overestimates delay variability, and underestimates mean delay. This motivates the need to model MIS statistically. Hence, we developed a method for modeling MIS, and incorporating it into SSTA. We also proposed an efficient heuristic for handling 3 or more input gates in our approach. We demonstrated the accuracy and robustness of our modeling approach over a large number of test cases. Future work includes handling slope variability in our model, and studying the impact of MIS on larger blocks.

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