A MULTI-LEVELED INCREMENTAL DECAP ALLOCATION AND PLACEMENT WITH PACKAGE MACRO-MODEL
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ABSTRACT

We propose an efficient decap allocation procedure for power /ground plane of package design. A structured model reduction is used to match as much as possible poles during the model reduction such that a small ordered model is obtained to approximate the original system. The reduced model is realized in a MIMO admittance form, and then is partitioned based on the regularity of the structure, where the correlation between partitioned system is considered. Therefore, each small partitioned system is represented by the admittance response at the pre-specified ports. The verification of nodal voltage response in frequency domain is formulated as a linear programming problem. Based on the detailed voltage verification results at every specified node as the possible decap location, we then present a multi-level decap placement to reduce the voltage resonance.

1. INTRODUCTION

As increasingly faster devices packed non-uniformly on a single chip, it becomes important to accurately model the combined chip-package considering nonuniform switching current and power consumption. The voltage fluctuation in power and ground distribution has become a significant factor, and hence the robust power ground design needs accurate but yet efficient verification for further decap allocation.

We propose an efficient decap allocation procedure for power /ground plane of package design. A structured model reduction is used to match as much as possible poles during the model reduction such that a small ordered model is obtained to approximate the original system. The reduced model is realized in a MIMO admittance form, and then is partitioned based on the regularity of the structure, where the correlation between partitioned system is considered by the Kuhn's tearing method. Therefore, each small partitioned system is represented by the admittance response at the pre-specified ports. The decap allocation is then formulated as a linear programming problem, where the modified admittance of the partitioned system is used during the optimization to reduce the computation time and increase the capacity of the solver.

2. REGULARITY OF STRUCTURED SYSTEM

Most power grid, package PG plane, and substrate can be modeled by PEEC model with regular structure.

i) the obviously large size of model needs more efficient model reduction; ii) the large number of ports (mostly are observation ports) needs explore the regularity. Note that the correlation between partitioned system can not be ignored.

3. STRUCTURE MODEL REDUCTION

The results in [**?**] can be naturally extensible to partitions other than 2-by-2. Consider a linear system in frequency domain:

$$\begin{bmatrix} G & A^T \\ -A & 0 \end{bmatrix} x(s) + s \begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} x(s) = B v_p$$
$$i_p = B^T x(s) \qquad (1)$$

where G, C, L the are conductance, capacitance and inductance matrix ($n \times n$), $x(s)$ is the state variable, B is the incidence matrix at ports (n_p ports), and i_p, u_p are the port current/voltage variables. Suppose we have the following partitions:

$$B = \begin{bmatrix} B_{1(n_p \times n_1)} \\ B_{2(n_p \times n_2)} \\ \vdots \\ B_{d(n_p \times n_d)} \end{bmatrix}, \quad G = \begin{bmatrix} G_{11} & G_{12} & \dots & G_{1d} \\ G_{21} & G_{22} & \dots & G_{2d} \\ \vdots & \vdots & \ddots & \vdots \\ G_{d1} & G_{d2} & \vdots & G_{dd} \end{bmatrix} \qquad (2)$$

and similarly for A, C, and L, where $\sum_{n_i} = n$. By applying PRIMA we obtain the qth-order of basis matrix V_q. We further partition V_q according to the block size of G:

$$V_d^{(q)} = \begin{bmatrix} V_{1(n_p \times n_1)} \\ V_{2(n_p \times n_2)} \\ \vdots \\ V_{d(n_p \times n_d)} \end{bmatrix} \qquad (3)$$

and reconstruct it to

$$\widetilde{V}_d^{(q)} = \begin{bmatrix} V_{1(n_p \times n_1)} & 0 & \cdots & 0 \\ 0 & V_{2(n_p \times n_2)} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & V_{d(n_p \times n_d)} \end{bmatrix} \quad (4)$$

and we can obtain the order reduced state matrices by projecting $\widetilde{V}_d$:

$$\widetilde{G}_d = \widetilde{V}_d^{(q)\,T} G \widetilde{V}_d^{(q)}, \qquad \widetilde{C}_d = \widetilde{V}_d^{(q)\,T} C \widetilde{V}, \qquad \widetilde{B}_d = \widetilde{V}_d^{(q)\,T} B. \quad (5)$$

We can obtain a reduced model that can match at least twice poles as PRIMA such that the reduction efficiency is improved. Furthermore, this structured model reduction can preserve the block structure of the original system.

The transfer function of the reduced system is:

$$Y'(s) = \begin{bmatrix} Y'_{1,1} & \cdots & Y'_{1,n_p} \\ \vdots & \vdots & \vdots \\ Y'_{n_p,1} & \cdots & Y'_{n_p,n_p} \end{bmatrix} \quad (6)$$

where

$$Y'_{i,j} = c^{i,j} + \sum_{m=1}^{q} \frac{k_i^{i,j}}{s - p_m}, \quad (7)$$

q is the number of poles (model order) for the approximation, k_i and p_i are the residues and poles. It can be realized according to Fig. **??**, where

$$Y_{ii} = \sum_{j=1}^{n_p} Y'_{ij}, \qquad Y_{ij} = -Y'_{ij} \quad (8)$$

Experiments compare the waveform accuracy of different structure sized circuits.

4. CORRELATION-CONSIDERED PARTITION

Unfortunately the efficiency of the reduced model degrades as the number of external ports to the circuits increases. Partition is a technique which divides a circuit into parts, obtains solutions for the parts and combines these partial solutions to find a global solution. It converts a large problem into a number of smaller problems which can be solved separately.

Assume the original system is divided into K subdivisions. Usually for if the original matrix is structured, there will be $K-1$ to be identical sub-matrices ($\mathbf{Y}_k$) but the last one is always different as it is the *global connection circuit* ($\mathbf{Y}_0$) as the common interconnection. For the kth partitioned block, we have following nodal equation

$$\mathbf{Y}_k V_k = I_k + \widetilde{I}_k \quad (9)$$

where V_k, I_k are nodal voltage and current vector at ports of kth partition, and $\widetilde{I}_k$ is the correlation current from the other partitioned block through the interconnection block. We also have following branch equation at interconnection network

$$\mathbf{Y}_0 V_0 = I_0 \quad (10)$$

where $\mathbf{Y}_0$ is the impedance of branches at interconnection network, and V_c and I_c are branch voltage and current vectors.Note that the nodal voltage/ current vectors V_k /I_k of partitioned block are related to the branch voltage voltage /current vectors V_c/I_c of interconnection block:

$$\widetilde{I}_k = C_{k0} I_0, \qquad V_0 = -\sum_{k=1}^{K} C_{k0}^T V_k \quad (11)$$

Therefore, we have following hybrid matrix equation

$$\begin{bmatrix} \mathbf{Y}_1 & 0 & \cdots & 0 & -C_{10} \\ 0 & \mathbf{Y}_2 & \cdots & 0 & -C_{20} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 0 & \mathbf{Y}_K & -C_{K0} \\ C_{10}^T & C_{20}^T & \cdots & C_{K0}^T & \mathbf{Y}_0^{-1} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_K \\ I_0 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_K \\ 0 \end{bmatrix} \quad (12)$$

The block current I_k then can be solved

$$V_k = \sum_{l=1}^{K} \mathcal{Z}_{kl} I_l = \mathcal{Z}_k I \quad (13)$$

where the impedance of interconnection block and each partitioned block is modified

$$\mathcal{Z}_{kk} = \mathbf{Y}_k^{-1} - \mathbf{Y}_k^{-1} C_{k0} \mathbf{Y}_0 C_{k0}^T \mathbf{Y}_k^{-1} \quad (14)$$

$$\mathcal{Z}_{kl} = -\mathbf{Y}_k^{-1} C_{k0} \mathbf{Y}_0 C_{l0}^T \mathbf{Y}_l^{-1} \quad (15)$$

5. MULTI-LEVEL INCREMENTAL DECAP ALLOCATION

In each block, we search the maximum peak impedance response by n ac sweeps in the desired frequency range. With the efficient nodal voltage response information of all possible decap locations, we can further deploy a multi-level decap placement method to efficiently reduce the voltage resonance. It is simply to choose the largest slack located in one level. We iterate the procedure until it converges. The incremental here means whenever we add one decoupling capacitor to the original circuits, we can easily add it to the branch admittance Y_{ii} at the desired port withouts further repeating the model reduction process.

6. EXPERIMENT

6.0.1. Package Plane

Geometry:
Technology (material):
FastHenry mesh extraction:

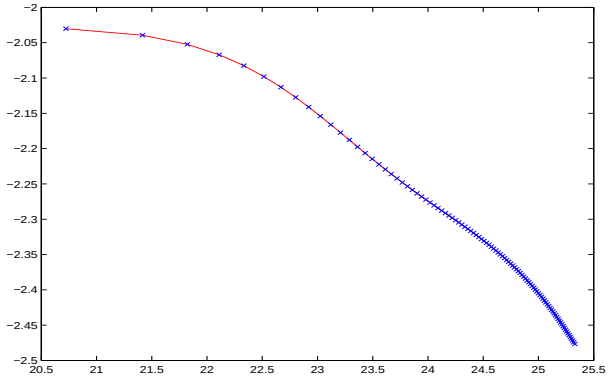

Figure 1: Structured model reduction of a 4x4 mesh.

6.0.2. Switching Circuit

Model maximum current switching by triangle waveform.

6.0.3. Comparison

(1) frequency domain verification; (2) time domain effect; (3) compare with SA based method.