ABSTRACT

1. INTRODUCTION

2. PRELIMINARIES

Consider an interconnect segment of resistance r per unit length and capacitance c per unit length buffered by repeaters of unit driving resistance r_s, unit input capacitance c_p and unit output capacitance c_o. Suppose an interconnect segment is of length l and the repeaters are of size s, then the delay of the segment including the repeaters is

$$\tau = r_s(c_o + c_p) + \frac{r_s}{s}cl + rlsc_o + \frac{1}{2}rcl^2$$

and the delay per unit length is

$$log_e 2\frac{\tau}{l} = log_e 2\left(\frac{1}{l}r_s(c_o + c_p) + \frac{r_s}{s}c + rsc_o + \frac{1}{2}rcl\right) \quad (1)$$

In equation (1), the driving strength of a repeater depends on the operating V_{dd} and V_{th} level. The driving resistance can be approximated as

$$r_s = K_1\frac{V_{dd}}{I_{dsat}} \quad (2)$$

where K_1 is a fitting parameter and I_{dsat} is the saturated drain current of a minimum sized NMOS or PMOS transistor with both V_{gs} and V_{ds} equal to V_{dd}. According to the alpha-power law, I_{dsat} can be modeled as

$$\begin{aligned} I_{dsat} &= K_2(V_{gs} - V_{th})^\alpha \\ &= K_2(V_{dd} - V_{th})^\alpha \end{aligned} \quad (3)$$

By plugging (3) into (2), we can obtain r_s as a function of V_{dd} and V_{th}.

$$r_s = K_3\frac{V_{dd}}{(V_{dd} - V_{th})^\alpha} \quad (4)$$

For a given V_{dd} and V_{th} level, the delay per unit length is optimal when

$$l_{opt} = \sqrt{\frac{2r_s(c_o + c_p)}{rc}} \qquad s_{opt} = \sqrt{\frac{r_s c}{rc_o}}$$

and

$$(\frac{\tau}{l})_{opt} = 2\sqrt{r_s c_o rc}\left(1 + \sqrt{\frac{1}{2}\left(1 + \frac{c_p}{c_o}\right)}\right)$$

If some amount of delay penalty can be tolerated, there is a family of solution sets $\{V_{dd}, V_{th}, l, s\}$ that satisfy the relaxed delay constraint. Our objective is to select from the feasible solutions the one which gives the minimum total power dissipation for the line. For an interconnect of fixed length L, the total power including the inserted repeaters is $P_{repeater}\frac{L}{l}$, where $\frac{P_{repeater}}{l}$ is a function of $\{V_{dd}, V_{th}, l, s\}$. Therefore, the problem can be fomulated mathematically as

$$\begin{aligned} min \quad & \frac{P_{repeater}}{l}(V_{dd}, V_{th}, l, s) \\ subject\ to \quad & \frac{\tau}{l}(V_{dd}, V_{th}, l, s) = (1 + f)(\frac{\tau}{l})_{opt} \end{aligned}$$

where f is the delay penalty.

3. METHODOLOGY

The power dissipation of a repeater is comprised of three parts: dynamic, leakage, and short circuit. Each of them is described in the following.

A. Dynamic Power

Dynamic power is the power dissipated when switching input signals cause the loading capacitance being charged or discharged. It is given by

$$P_{switching} = a(s(c_o + c_p) + lc)V_{dd}^2 f_{clk}$$

where a is the switching activity of a repeater, and f_{clk} is the clock frequency.

B. Leakage Power

The primary sources of leakage power come from the subthreshold leakage and the gate leakage. According to the ITRS 2003 roadmap, high-K gate dielectric is required to control the direct gate tunneling current for low standby power devices in process technology nodes below 90nm. The use of high-K gate dielectric will allow orders of magnitude reduction in the gate leakage current, so it is not included in our leakage current model. The subthreshold leakage current of a minimum sized NMOS transistor is given by

$$I_{sub} = I_{off_0} e^{\frac{(V_{th_0} - V_{th})}{n v_T}}$$

where I_{off_0} and V_{th_0} the reference subthreshold leakage current, threshold voltage for a given technology; n the slope shape factor; v_T the thermal voltage. The model assumes the transistor is at OFF state where $V_{gs} = 0$ and $V_{ds} = V_{dd}$. The average leakage power of a repeater is

$$\begin{aligned} P_{leakage} &= V_{dd} I_{sub} \\ &= \frac{1}{2}(I_{off n_0} W_{n_{min}} + I_{off p_0} W_{p_{min}}) V_{dd} e^{\frac{(V_{th_0} - V_{th})}{n v_T}} s \end{aligned}$$

C. Short-Circuit Power

The short circuit power dissipation depends on the the transition time at the input and output of an inverter. Assuming symmetric high-to-low and low-to-high transitionsat the input and output of the repeaters, the short circuit power is given by

$$P_{short-circuit} = a\tau_r V_{dd} W_{n_{min}} s I_{short-circuit} f_{clk}$$

where a is the same switching factor as in the dynamic power expression. Assuming that $V_{t_n} = V_{t_p} \simeq (\frac{1}{4})V_{dd}$, the transistion time can be approximated by

$$\begin{aligned} t_r &= \tau log_e \left(\frac{V_{dd} - V_{th_p}}{V_{th_n}} \right) \\ &= \tau log_e 3 \end{aligned}$$

Therefore, the total power can be given by

$$\begin{aligned} P &= k_1 V_{dd}^2 (s(c_p + c_o) + lc) + k_2 V_{dd} e^{\frac{(V_{th_0} - V_{th})}{n v_T}} s + k_3 V_{dd} s\tau \\ &= k_1 V_{dd}^2 (s(c_p + c_o) + lc) + k_2 V_{dd} e^{\frac{(V_{th_0} - V_{th})}{n v_T}} s \\ &+ k_3 V_{dd} (1+f)(\frac{\tau}{l})_{opt} sl \\ &= k_1 V_{dd}^2 (s(c_p + c_o) + lc) + k_2 V_{dd} e^{\frac{(V_{th_0} - V_{th})}{n v_T}} s + k_3' sl \end{aligned}$$

where

$$\begin{aligned} k_1 &= af_{clk} \\ k_2 &= \frac{1}{2}(I_{offn_0} W_{n_{min}} + I_{offp_0} W_{p_{min}}) \\ k_3 &= aW_{n_{min}} f_{clk} log_e 3 \\ k_3' &= k_3(1+f)(\frac{\tau}{l})_{opt} \end{aligned}$$

and f is the specified delay penalty.

The design space of the problem is four dimensinal. By expressing one of the variables in terms of the other three variables, we are able to force this variable to satisfy the delay constraint. Combining equations (2) and (1), we can express V_{th} as a function of V_{dd}, l, and s that satisfies the delay constraint. That is, from equation (2), we can obtain V_{th} in terms of V_{dd} and r_s.

$$V_{th} = V_{dd} - \left(\frac{K_3 V_{dd}}{r_s} \right)^{\frac{1}{\alpha}}$$

And from equation (1), r_s can be expressed as a function of l and s:

$$r_s = \frac{(1+f)(\frac{\tau}{l})_{opt} - rsc_o - \frac{1}{2}rcl}{\frac{c_o + c_p}{l} + \frac{c}{s}}$$

The total power can thus be expressed as a function of three variables V_{dd}, l and s. By solving the gradient of the function $\frac{P}{l}$ equal to zero, we can obtain three nonlinear equations of three variables.

$$\begin{aligned} \frac{\partial \frac{P}{l}}{\partial V_{dd}} &= 2k_1 V_{dd} \left(\frac{s}{l}(c_o + c_p) + c \right) \\ &+ k_2 e^{\frac{-V_{th}(V_{dd},l,s)}{n v_T}} \frac{s}{l} \\ &- \frac{1}{n v_T} \frac{\partial V_{th}}{\partial V_{dd}} k_2 V_{dd} e^{\frac{-V_{th}(V_{dd},l,s)}{n v_T}} \frac{s}{l} + k_3' s = 0 \\ \frac{\partial \frac{P}{l}}{\partial s} &= k_1 V_{dd}^2 \frac{c_o + c_p}{l} \\ &+ k_2 V_{dd} e^{\frac{-V_{th}(V_{dd},l,s)}{n v_T}} \frac{1}{l} \\ &- \frac{1}{n v_T} \frac{\partial V_{th}}{\partial s} k_2 V_{dd} e^{\frac{-V_{th}(V_{dd},l,s)}{n v_T}} \frac{s}{l} + k_3' V_{dd} = 0 \\ \frac{\partial \frac{P}{l}}{\partial l} &= -k_1 V_{dd}^2 (c_o + c_p) \frac{s}{l^2} \\ &- k_2 V_{dd} e^{\frac{-V_{th}(V_{dd},l,s)}{n v_T}} \frac{s}{l^2} \\ &- \frac{1}{n v_T} \frac{\partial V_{th}}{\partial l} k_2 V_{dd} e^{\frac{-V_{th}(V_{dd},l,s)}{n v_T}} \frac{s}{l} = 0 \end{aligned}$$

where

$$\begin{aligned} \frac{\partial V_{th}}{\partial V_{dd}} &= 1 - \frac{1}{\alpha} (\frac{K_3}{r_s})^{\frac{1}{\alpha}} V_{dd}^{\frac{1}{\alpha} - 1} \\ \frac{\partial V_{th}}{\partial s} &= \frac{1}{\alpha} (K_3 V_{dd})^{\frac{1}{\alpha}} r_s^{-\frac{1}{\alpha} - 1} \frac{\partial r_s}{\partial s} \\ \frac{\partial V_{th}}{\partial l} &= \frac{1}{\alpha} (K_3 V_{dd})^{\frac{1}{\alpha}} r_s^{-\frac{1}{\alpha} - 1} \frac{\partial r_s}{\partial l} \end{aligned}$$

and

$$\begin{aligned} \frac{\partial r_s}{\partial s} &= \frac{-rc \left(\frac{c_o + c_p}{l} + \frac{c}{s} \right) + \frac{c}{s^2} \left((1+f)(\frac{\tau}{l}_{opt} - rsc_o - \frac{1}{2}rcl \right)}{\left(\frac{c_o + c_p}{l} + \frac{c}{s} \right)^2} \\ \frac{\partial r_s}{\partial s} &= \frac{-\frac{1}{2}rc \left(\frac{c_o + c_p}{l} + \frac{c}{s} \right) + \frac{c_o + c_p}{l^2} \left((1+f)(\frac{\tau}{l}_{opt} - rsc_o - \frac{1}{2}rcl \right)}{\left(\frac{c_o + c_p}{l} + \frac{c}{s} \right)^2} \end{aligned}$$

4. EXPERIMENTAL RESULTS

5. CONCLUSIONS